

## EMC 性能优异的 ISO7710-Q1 高速单通道增强型数字隔离器

### 1 特性

- 符合汽车应用要求
- 具有符合 AEC-Q100 标准的下列特性：
  - 器件温度等级 1：-40°C 至 125°C 环境温度范围
  - 器件 HBM ESD 分类等级 3A
  - 器件 CDM ESD 分类等级 C6
- 功能安全型**
  - 可提供用于功能安全系统设计的文档
- 100Mbps 数据速率
- 稳健可靠的隔离栅：
  - 在 1500V<sub>RMS</sub> 工作电压下预计寿命超过 30 年
  - 隔离等级高达 5000V<sub>RMS</sub>
  - 浪涌能力高达 12.8kV
  - CMTI 典型值为 ±100kV/μs
- 宽电源电压范围：2.25V 至 5.5V
- 2.25V 至 5.5V 电平转换
- 默认输出高电平 (ISO7710) 和低电平 (ISO7710F) 选项
- 低功耗，1Mbps 时的电流典型值为 1.7mA
- 低传播延迟：典型值为 11ns (5V 电源)
- 优异的电磁兼容性 (EMC)
  - 系统级 ESD、EFT 和浪涌抗扰性
  - 在整个隔离栅具有 ±8kV IEC 61000-4-2 接触放电保护
  - 低辐射
- 宽体 SOIC (DW-16) 和窄体 SOIC (D-8) 封装选项
- 安全相关认证
  - 符合 DIN EN IEC 60747-17 (VDE 0884-17) 标准的 VDE 增强型绝缘
  - UL 1577 组件认证计划
  - IEC 62368-1、IEC 61010-1、IEC 60601-1 和 GB 4943.1 认证

### 2 应用

- 混合动力、电动和动力总成系统 (EV/HEV)**
  - 电池管理系统 (BMS)
  - 车载充电器
  - 牵引逆变器
  - 直流/直流转换器
  - 逆变器和电机控制

### 3 说明

ISO7710-Q1 器件是一款高性能单通道数字隔离器，可提供符合 UL 1577 的 5000V<sub>RMS</sub> (DW 封装) 和 3000V<sub>RMS</sub> (D 封装) 隔离额定值。此器件还通过了 VDE、TUV、CSA 和 CQC 认证。

在隔离互补金属氧化物半导体 (CMOS) 或者低电压互补金属氧化物半导体 (LVCMOS) 数字 I/O 的同时，ISO7710-Q1 器件还可提供高电磁抗扰度和低辐射，同时具备低功耗特性。隔离通道的逻辑输入和输出缓冲器由双电容二氧化硅 (SiO<sub>2</sub>) 绝缘栅相隔离。如果输入功率或信号出现损失，不带后缀 F 的器件默认输出高电平，带后缀 F 的器件默认输出低电平。更多详细信息，请参阅 [器件功能模式](#) 部分。

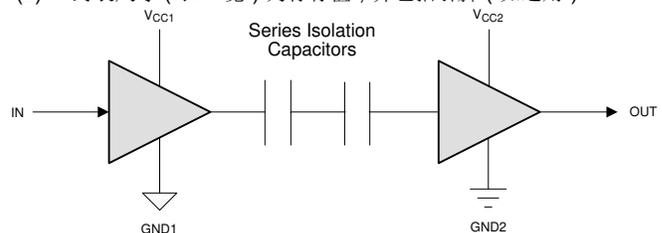
该器件与隔离式电源搭配使用，有助于防止数据总线 (例如，CAN 和 LIN) 或其他电路上的噪声电流进入本地接地以及干扰或损坏敏感电路。凭借独创的芯片设计和布线技术，ISO7710-Q1 器件的电磁兼容性得到了显著增强，可缓解系统级 ESD、EFT 和浪涌问题并符合辐射标准。ISO7710-Q1 器件可提供 16 引脚 SOIC 宽体 (DW) 和 8 引脚 SOIC 窄体 (D) 封装。

#### 封装信息

器件型号	封装 <sup>(1)</sup>	封装尺寸 <sup>(2)</sup>	本体尺寸 (标称值)
ISO7710-Q1	SOIC (D, 16)	4.90mm × 6mm	4.90mm × 3.91mm
	SOIC (DW, 16)	10.30mm × 10.30mm	10.30mm × 7.50mm

(1) 有关更多信息，请参阅 [节 28](#)。

(2) 封装尺寸 (长 × 宽) 为标称值，并包括引脚 (如适用)。



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#### 简化版原理图



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## 4 Pin Configuration and Functions

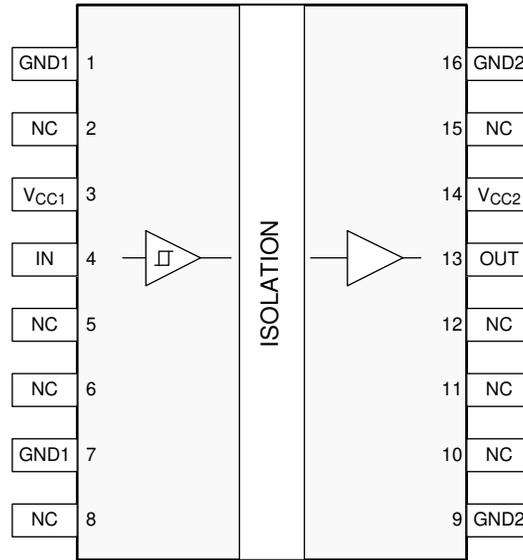


图 4-1. DW Package 16-Pin SOIC Top View

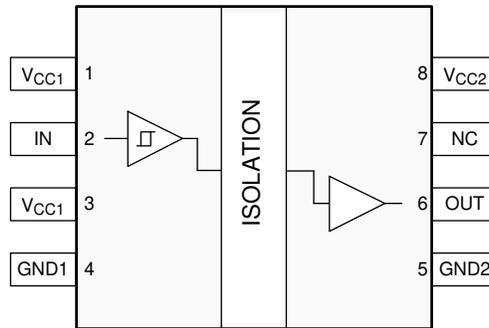


图 4-2. D Package 8-Pin SOIC Top View

表 4-1. Pin Functions

NAME	PIN NO.		Type	DESCRIPTION
	DW	D		
V <sub>CC1</sub>	3	1, 3	—	Power supply, V <sub>CC1</sub>
V <sub>CC2</sub>	14	8	—	Power supply, V <sub>CC2</sub>
GND1	1, 7	4	—	Ground connection for V <sub>CC1</sub>
GND2	9, 16	5	—	Ground connection for V <sub>CC2</sub>
IN	4	2	I	Input channel
OUT	13	6	O	Output channel
NC	2, 5, 6, 8, 10, 11, 12, 15	7	—	No connect pin; no internal connection

## 5 Specifications

## 6 Absolute Maximum Ratings

 See<sup>(1)</sup>

		MIN	MAX	UNIT
V <sub>CC1</sub> , V <sub>CC2</sub>	Supply Voltage <sup>(2)</sup>	-0.5	6	V
V	Voltage at INx, OUTx	-0.5	V <sub>CCX</sub> + 0.5 <sup>(3)</sup>	V
I <sub>O</sub>	Output current	-15	15	mA
T <sub>J</sub>	Junction temperature		150	°C
T <sub>stg</sub>	Storage temperature	-65	150	°C

- (1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
- (2) All voltage values except differential I/O bus voltages are with respect to the local ground terminal (GND1 or GND2) and are peak voltage values
- (3) Maximum voltage must not exceed 6 V.

## 7 ESD Ratings

			VALUE	UNIT
V <sub>ESD</sub>	Electrostatic discharge	Human body model (HBM), per AEC Q100-002 <sup>(1)</sup>	±6000	V
		Charged device model (CDM), per AEC Q100-011	±1500	
		Contact discharge per IEC 61000-4-2; Isolation barrier withstand test <sup>(2) (3)</sup>	±8000	

- (1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.
- (2) IEC ESD strike is applied across the barrier with all pins on each side tied together creating a two-terminal device.
- (3) Testing is carried out in air or oil to determine the intrinsic contact discharge capability of the device.

## 8 Recommended Operating Conditions

		MIN	NOM	MAX	UNIT
$V_{CC1}, V_{CC2}$	Supply voltage	2.25		5.5	V
$V_{CC(UVLO+)}$	UVLO threshold when supply voltage is rising		2	2.25	V
$V_{CC(UVLO-)}$	UVLO threshold when supply voltage is falling	1.7	1.8		V
$V_{HYS(UVLO)}$	Supply voltage UVLO hysteresis	100	200		mV
$I_{OH}$	High level output current	$V_{CC2} = 5\text{ V}$		-4	mA
		$V_{CC2} = 3.3\text{ V}$		-2	
		$V_{CC2} = 2.5\text{ V}$		-1	
$I_{OL}$	Low level output current	$V_{CC2} = 5\text{ V}$		4	mA
		$V_{CC2} = 3.3\text{ V}$		2	
		$V_{CC2} = 2.5\text{ V}$		1	
$V_{IH}$	High level Input voltage	$0.7 \times V_{CC1}$		$V_{CC1}$	V
$V_{IL}$	Low level Input voltage	0		$0.3 \times V_{CC1}$	V
$DR^{(1)}$	Data Rate	0		100	Mbps
$T_A$	Ambient temperature	-55	25	125	°C

(1) 100 Mbps is the maximum specified data rate, although higher data rates are possible.

## 9 Thermal Information

THERMAL METRIC <sup>(1)</sup>		ISO7710-Q1		UNIT
		DW (SOIC)	D(SOIC)	
		(16-Pin)	(8-Pin)	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	94.4	146.1	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	57.3	63.1	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	57.1	80.0	°C/W
$\psi_{JT}$	Junction-to-top characterization parameter	40.0	9.6	°C/W
$\psi_{JB}$	Junction-to-board characterization parameter	56.8	79.0	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	—	—	°C/W

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application note

## 10 Power Ratings

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>ISO7710-Q1</b>						
$P_D$	Maximum power dissipation (both sides)	$V_{CC1} = V_{CC2} = 5.5\text{ V}$ , $T_J = 150^\circ\text{C}$ , $C_L = 15\text{ pF}$ , Input a 50-MHz 50% duty cycle square wave			55	mW
$P_{D1}$	Maximum power dissipation (side-1)				13	mW
$P_{D2}$	Maximum power dissipation (side-2)				42	mW

## 11 Insulation Specifications

PARAMETER		TEST CONDITIONS	VALUE		UNIT
			DW-16	D-8	
<b>IEC 60664-1</b>					
CLR	External clearance <sup>(1)</sup>	Shortest terminal-to-terminal distance through air	8	4	mm
CPG	External creepage <sup>(1)</sup>	Shortest terminal-to-terminal distance across the package surface	8	4	mm
DTI	Distance through the insulation	Minimum internal gap (internal clearance)	17	17	μm
CTI	Comparative tracking index	DIN EN 60112 (VDE 0303-11); IEC 60112; UL 746A	>600	>600	V
	Material Group	According to IEC 60664-1	I	I	
	Overvoltage category per IEC 60664-1	Rated mains voltage ≤ 150 V <sub>RMS</sub>	I - IV	I-IV	
		Rated mains voltage ≤ 300 V <sub>RMS</sub>	I - IV	I-III	
		Rated mains voltage ≤ 600 V <sub>RMS</sub>	I - IV	n/a	
		Rated mains voltage ≤ 1000 V <sub>RMS</sub>	I-III	n/a	
<b>DIN EN IEC 60747-17 (VDE 0884-17)<sup>(2)</sup></b>					
V <sub>IORM</sub>	Maximum repetitive peak isolation voltage	AC voltage (bipolar)	2121	637	V <sub>PK</sub>
V <sub>IOWM</sub>	Maximum working isolation voltage	AC voltage; time-dependent dielectric breakdown (TDDB) test, see 节 25.2.3.1	1500	450	V <sub>RMS</sub>
		DC voltage	2121	637	V <sub>DC</sub>
V <sub>IOTM</sub>	Maximum transient isolation voltage	V <sub>TEST</sub> = V <sub>IOTM</sub> , t = 60 s (qualification); V <sub>TEST</sub> = 1.2 × V <sub>IOTM</sub> , t = 1 s (100% production)	8000	4242	V <sub>PK</sub>
V <sub>IMP</sub>	Maximum impulse voltage <sup>(3)</sup>	Tested in air, 1.2/50- μs waveform per IEC 62368-1	8000	5000	V <sub>PK</sub>
V <sub>IOSM</sub>	Maximum surge isolation voltage <sup>(4)</sup>	V <sub>IOSM</sub> ≥ 1.3 × V <sub>IMP</sub> ; Tested in oil (qualification test), 1.2/50-μs waveform per IEC 62368-1	12800	10000	V <sub>PK</sub>
q <sub>pd</sub>	Apparent charge <sup>(5)</sup>	Method a: After I/O safety test subgroup 2/3, V <sub>ini</sub> = V <sub>IOTM</sub> , t <sub>ini</sub> = 60 s; V <sub>pd(m)</sub> = 1.2 × V <sub>IORM</sub> , t <sub>m</sub> = 10 s	≤ 5	≤ 5	pC
		Method a: After environmental tests subgroup 1, V <sub>ini</sub> = V <sub>IOTM</sub> , t <sub>ini</sub> = 60 s; V <sub>pd(m)</sub> = 1.6 × V <sub>IORM</sub> , t <sub>m</sub> = 10 s	≤ 5	≤ 5	
		Method b: At routine test (100% production) and preconditioning (type test); V <sub>ini</sub> = 1.2 × V <sub>IOTM</sub> , t <sub>ini</sub> = 1 s; V <sub>pd(m)</sub> = 1.875 × V <sub>IORM</sub> (ISO7710), t <sub>m</sub> = 1 s (method b1) or V <sub>pd(m)</sub> = V <sub>ini</sub> , t <sub>m</sub> = t <sub>ini</sub> (method b2)	≤ 5	≤ 5	
C <sub>IO</sub>	Barrier capacitance, input to output <sup>(6)</sup>	V <sub>IO</sub> = 0.4 × sin (2 π ft), f = 1 MHz	≈0.4	≈0.4	pF
R <sub>IO</sub>	Insulation resistance <sup>(6)</sup>	V <sub>IO</sub> = 500 V, T <sub>A</sub> = 25°C	> 10 <sup>12</sup>	> 10 <sup>12</sup>	Ω
		V <sub>IO</sub> = 500 V, 100°C ≤ T <sub>A</sub> ≤ 125°C	> 10 <sup>11</sup>	> 10 <sup>11</sup>	
		V <sub>IO</sub> = 500 V at T <sub>S</sub> = 150°C	> 10 <sup>9</sup>	> 10 <sup>9</sup>	
	Pollution degree		2	2	
	Climatic category		55/125/ 21	55/125/ 21	
<b>UL 1577</b>					
V <sub>ISO</sub>	Withstand isolation voltage	V <sub>TEST</sub> = V <sub>ISO</sub> , t = 60 s (qualification); V <sub>TEST</sub> = 1.2 × V <sub>ISO</sub> , t = 1 s (100% production)	5000	3000	V <sub>RMS</sub>

- (1) Creepage and clearance requirements should be applied according to the specific equipment isolation standards of an application. Care must be taken to maintain the creepage and clearance distance of a board design to verify that the mounting pads of the isolator on the printed-circuit board do not reduce this distance. Creepage and clearance on a printed-circuit board become equal in certain cases. Techniques such as inserting grooves, ribs, or both on a printed circuit board are used to help increase these specifications.
- (2) This coupler is designed for *safe electrical insulation* only within the safety ratings. Compliance with the safety ratings shall be ensured by means of suitable protective circuits.

- (3) Testing is carried out in air to determine the surge immunity of the package
- (4) Testing is carried out in oil to determine the intrinsic surge immunity of the isolation barrier.
- (5) Apparent charge is electrical discharge caused by a partial discharge (pd).
- (6) All pins on each side of the barrier tied together creating a two-terminal device.

## 12 Safety-Related Certifications

VDE	CSA	UL	CQC	TUV
Certified according to DIN EN IEC 60747-17 (VDE 0884-17)	Certified according to IEC 62368-1 and IEC 60601-1	Certified according to UL 1577 Component Recognition Program	Certified according to GB4943.1	Certified according to EN 61010-1 and EN 62368-1
Maximum transient isolation voltage, 8000 V <sub>PK</sub> (DW-16, Reinforced) and 4242 V <sub>PK</sub> (D-8); Maximum repetitive peak isolation voltage, 2121 V <sub>PK</sub> (DW-16, Reinforced) and 637 V <sub>PK</sub> (D-8); Maximum surge isolation voltage, 12800 V <sub>PK</sub> (DW-16, Reinforced) and 10000 V <sub>PK</sub> (D-8)	Reinforced insulation per CSA 62368-1 and IEC 62368-1, 800 V <sub>RMS</sub> (DW-16) and 400 V <sub>RMS</sub> (D-8) max working voltage (pollution degree 2, material group I); 2 MOPP (Means of Patient Protection) per CSA 60601-1 and IEC 60601-1, 250 V <sub>RMS</sub> (DW-16) max working voltage	DW-16: Single protection, 5000 V <sub>RMS</sub> ; D-8: Single protection, 3000 V <sub>RMS</sub>	DW-16: Reinforced Insulation, Altitude ≤ 5000 m, Tropical Climate, 700 V <sub>RMS</sub> maximum working voltage; D-8: Basic Insulation, Altitude ≤ 5000 m, Tropical Climate, 400 V <sub>RMS</sub> maximum working voltage	5000 V <sub>RMS</sub> (DW-16) and 3000 V <sub>RMS</sub> (D-8) Reinforced insulation per EN 61010-1 up to working voltage of 600 V <sub>RMS</sub> (DW-16) and 300 V <sub>RMS</sub> (D-8) 5000 V <sub>RMS</sub> (DW-16) and 3000 V <sub>RMS</sub> (D-8) Reinforced insulation per EN 62368-1 up to working voltage of 800 V <sub>RMS</sub> (DW-16) and 400 V <sub>RMS</sub> (D-8)
Certificate number: 40040142	Master contract number: 220991	File number: E181974	Certificate numbers: CQC21001304083 (DW-16) CQC15001121656 (D-8)	Client ID number: 77311

### 13 Safety Limiting Values

Safety limiting<sup>(1)</sup> intends to minimize potential damage to the isolation barrier upon failure of input or output circuitry. A failure of the I/O can allow low resistance to ground or the supply and, without current limiting, dissipate sufficient power to overheat the die and damage the isolation barrier potentially leading to secondary system failures.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>DW-16 PACKAGE</b>					
I <sub>S</sub>	Safety input, output, or supply current	R <sub>θJA</sub> = 94.4°C/W, V <sub>I</sub> = 5.5 V, T <sub>J</sub> = 150°C, T <sub>A</sub> = 25°C		241	mA
		R <sub>θJA</sub> = 94.4°C/W, V <sub>I</sub> = 3.6 V, T <sub>J</sub> = 150°C, T <sub>A</sub> = 25°C		368	
		R <sub>θJA</sub> = 94.4°C/W, V <sub>I</sub> = 2.75 V, T <sub>J</sub> = 150°C, T <sub>A</sub> = 25°C		482	
P <sub>S</sub>	Safety input, output, or total power	R <sub>θJA</sub> = 94.4°C/W, T <sub>J</sub> = 150°C, T <sub>A</sub> = 25°C		1324	mW
T <sub>S</sub>	Maximum safety temperature			150	°C
<b>D-8 PACKAGE</b>					
I <sub>S</sub>	Safety input, output, or supply current <sup>(1)</sup>	R <sub>θJA</sub> = 146.1°C/W, V <sub>I</sub> = 5.5 V, T <sub>J</sub> = 150°C, T <sub>A</sub> = 25°C		156	mA
		R <sub>θJA</sub> = 146.1°C/W, V <sub>I</sub> = 3.6 V, T <sub>J</sub> = 150°C, T <sub>A</sub> = 25°C		238	
		R <sub>θJA</sub> = 146.1°C/W, V <sub>I</sub> = 2.75 V, T <sub>J</sub> = 150°C, T <sub>A</sub> = 25°C		311	
P <sub>S</sub>	Safety input, output, or total power <sup>(1)</sup>	R <sub>θJA</sub> = 146.1°C/W, T <sub>J</sub> = 150°C, T <sub>A</sub> = 25°C		856	mW
T <sub>S</sub>	Maximum safety temperature <sup>(1)</sup>			150	°C

- (1) The maximum safety temperature, T<sub>S</sub>, has the same value as the maximum junction temperature, T<sub>J</sub>, specified for the device. The I<sub>S</sub> and P<sub>S</sub> parameters represent the safety current and safety power respectively. The maximum limits of I<sub>S</sub> and P<sub>S</sub> should not be exceeded. These limits vary with the ambient temperature, T<sub>A</sub>.

The junction-to-air thermal resistance, R<sub>θJA</sub>, in the [§ 9](#) table is that of a device installed on a high-K test board for leaded surface-mount packages. Use these equations to calculate the value for each parameter:

T<sub>J</sub> = T<sub>A</sub> + R<sub>θJA</sub> × P, where P is the power dissipated in the device.

T<sub>J(max)</sub> = T<sub>S</sub> = T<sub>A</sub> + R<sub>θJA</sub> × P<sub>S</sub>, where T<sub>J(max)</sub> is the maximum allowed junction temperature.

P<sub>S</sub> = I<sub>S</sub> × V<sub>I</sub>, where V<sub>I</sub> is the maximum input voltage.

## 14 Electrical Characteristics—5-V Supply

$V_{CC1} = V_{CC2} = 5\text{ V} \pm 10\%$  (over recommended operating conditions unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{OH}$	High-level output voltage	$I_{OH} = -4\text{ mA}$ ; see 图 23-1	$V_{CC2} - 0.4$	4.8		V
$V_{OL}$	Low-level output voltage	$I_{OL} = 4\text{ mA}$ ; see 图 23-1		0.2	0.4	V
$V_{IT+(IN)}$	Rising input threshold voltage			$0.6 \times V_{CC1}$	$0.7 \times V_{CC1}$	V
$V_{IT-(IN)}$	Falling input threshold voltage		$0.3 \times V_{CC1}$	$0.4 \times V_{CC1}$		V
$V_{I(HYS)}$	Input threshold voltage hysteresis		$0.1 \times V_{CC1}$	$0.2 \times V_{CC1}$		V
$I_{IH}$	High-level input current	$V_{IH} = V_{CC1}$ at INx			10	$\mu\text{A}$
$I_{IL}$	Low-level input current	$V_{IL} = 0\text{ V}$ at INx	-10			$\mu\text{A}$
CMTI	Common mode transient immunity	$V_I = V_{CC1}$ or $0\text{ V}$ , $V_{CM} = 1200\text{ V}$ ; see 图 23-3	85	100		$\text{kV}/\mu\text{s}$
$C_i$	Input Capacitance (1)	$V_I = V_{CC}/2 + 0.4 \times \sin(2\pi ft)$ , $f = 1\text{ MHz}$ , $V_{CC} = 5\text{ V}$ ;		2		pF

(1) Measured from input pin to same side ground.

## 15 Supply Current Characteristics—5-V Supply

$V_{CC1} = V_{CC2} = 5\text{ V} \pm 10\%$  (over recommended operating conditions unless otherwise noted)

PARAMETER	TEST CONDITIONS	SUPPLY CURRENT	MIN	TYP	MAX	UNIT	
<b>ISO7710-Q1</b>							
Supply current - DC signal	$V_I = V_{CC1}$ (ISO7710-Q1), $V_I = 0\text{ V}$ (ISO7710-Q1 with F suffix)	$I_{CC1}$		0.5	1.2	mA	
		$I_{CC2}$		0.6	1.2		
	$V_I = 0\text{ V}$ (ISO7710-Q1), $V_I = V_{CC1}$ (ISO7710-Q1 with F suffix)	$I_{CC1}$		1.6	2.4		
		$I_{CC2}$		0.6	1.2		
Supply current - AC signal	All channels switching with square wave clock input; $C_L = 15\text{ pF}$	1 Mbps	$I_{CC1}$		1.1		1.8
			$I_{CC2}$		0.6		1.3
		10 Mbps	$I_{CC1}$		1.1		1.9
			$I_{CC2}$		1.1		1.9
		100 Mbps	$I_{CC1}$		1.4	2.3	
			$I_{CC2}$		5.9	7.4	

## 16 Electrical Characteristics—3.3-V Supply

 $V_{CC1} = V_{CC2} = 3.3 \text{ V} \pm 10\%$  (over recommended operating conditions unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{OH}$	High-level output voltage	$I_{OH} = -2\text{mA}$ ; see 图 23-1	$V_{CC2} - 0.3$	3.2		V
$V_{OL}$	Low-level output voltage	$I_{OL} = 2\text{mA}$ ; see 图 23-1		0.1	0.3	V
$V_{IT+(IN)}$	Rising input threshold voltage			$0.6 \times V_{CC1}$	$0.7 \times V_{CC1}$	V
$V_{IT-(IN)}$	Falling input threshold voltage		$0.3 \times V_{CC1}$	$0.4 \times V_{CC1}$		V
$V_{I(HYS)}$	Input threshold voltage hysteresis		$0.1 \times V_{CC1}$	$0.2 \times V_{CC1}$		V
$I_{IH}$	High-level input current	$V_{IH} = V_{CC1}$ at INx			10	$\mu\text{A}$
$I_{IL}$	Low-level input current	$V_{IL} = 0 \text{ V}$ at INx	-10			$\mu\text{A}$
CMTI	Common mode transient immunity	$V_I = V_{CC1}$ or $0 \text{ V}$ , $V_{CM} = 1200 \text{ V}$ ; see 图 23-3	85	100		kV/ $\mu\text{s}$

## 17 Supply Current Characteristics—3.3-V Supply

 $V_{CC1} = V_{CC2} = 3.3 \text{ V} \pm 10\%$  (over recommended operating conditions unless otherwise noted)

PARAMETER	TEST CONDITIONS	SUPPLY CURRENT	MIN	TYP	MAX	UNIT	
<b>ISO7710-Q1</b>							
Supply current - DC signal	$V_I = V_{CC1}$ (ISO7710-Q1), $V_I = 0 \text{ V}$ (ISO7710-Q1 with F suffix)	$I_{CC1}$		0.5	1.2	mA	
		$I_{CC2}$		0.6	1.1		
	$V_I = 0 \text{ V}$ (ISO7710-Q1), $V_I = V_{CC1}$ (ISO7710-Q1 with F suffix)	$I_{CC1}$		1.6	2.4		
		$I_{CC2}$		0.6	1.2		
Supply current - AC signal	All channels switching with square wave clock input; $C_L = 15 \text{ pF}$	1 Mbps	$I_{CC1}$		1.1		1.8
			$I_{CC2}$		0.6		1.2
		10 Mbps	$I_{CC1}$		1		1.8
			$I_{CC2}$		1.1		1.7
		100 Mbps	$I_{CC1}$		1.3	2.1	
			$I_{CC2}$		4.3	5.6	

## 18 Electrical Characteristics—2.5-V Supply

$V_{CC1} = V_{CC2} = 2.5\text{ V} \pm 10\%$  (over recommended operating conditions unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{OH}$	High-level output voltage	$I_{OH} = -1\text{mA}$ ; see 图 23-1	$V_{CC2} - 0.2$	2.45		V
$V_{OL}$	Low-level output voltage	$I_{OL} = 1\text{mA}$ ; see 图 23-1		0.05	0.2	V
$V_{IT+(IN)}$	Rising input threshold voltage			$0.6 \times V_{CC1}$	$0.7 \times V_{CC1}$	V
$V_{IT-(IN)}$	Falling input threshold voltage		$0.3 \times V_{CC1}$	$0.4 \times V_{CC1}$		V
$V_{I(HYS)}$	Input threshold voltage hysteresis		$0.1 \times V_{CC1}$	$0.2 \times V_{CC1}$		V
$I_{IH}$	High-level input current	$V_{IH} = V_{CC1}$ at $IN_x$			10	$\mu\text{A}$
$I_{IL}$	Low-level input current	$V_{IL} = 0\text{ V}$ at $IN_x$	-10			$\mu\text{A}$
CMTI	Common mode transient immunity	$V_I = V_{CC1}$ or $0\text{ V}$ , $V_{CM} = 1200\text{ V}$ ; see 图 23-3	85	100		$\text{kV}/\mu\text{s}$

## 19 Supply Current Characteristics—2.5-V Supply

$V_{CC1} = V_{CC2} = 2.5\text{ V} \pm 10\%$  (over recommended operating conditions unless otherwise noted)

PARAMETER	TEST CONDITIONS	SUPPLY CURRENT	MIN	TYP	MAX	UNIT	
<b>ISO7710-Q1</b>							
Supply current - DC signal	$V_I = V_{CC1}$ (ISO7710-Q1), $V_I = 0\text{ V}$ (ISO7710-Q1 with F suffix)	$I_{CC1}$		0.5	1.2	mA	
		$I_{CC2}$		0.6	1.1		
	$V_I = 0\text{ V}$ (ISO7710-Q1), $V_I = V_{CC1}$ (ISO7710-Q1 with F suffix)	$I_{CC1}$		1.6	2.3		
		$I_{CC2}$		0.6	1.2		
Supply current - AC signal	All channels switching with square wave clock input; $C_L = 15\text{ pF}$	1 Mbps	$I_{CC1}$		1.1		1.8
			$I_{CC2}$		0.6		1.2
		10 Mbps	$I_{CC1}$		1.1		1.8
			$I_{CC2}$		0.9		1.5
		100 Mbps	$I_{CC1}$		1.2	2	
			$I_{CC2}$		3.4	4.6	

## 20 Switching Characteristics—5-V Supply

$V_{CC1} = V_{CC2} = 5\text{ V} \pm 10\%$  (over recommended operating conditions unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{PLH}, t_{PHL}$	Propagation delay time	See 图 23-1	6	11	17	ns
PWD	Pulse width distortion <sup>(1)</sup> $ t_{PHL} - t_{PLH} $					
$t_{sk(pp)}$	Part-to-part skew time <sup>(2)</sup>				4.5	ns
$t_r$	Output signal rise time	See 图 23-1		1.8	3.9	ns
$t_f$	Output signal fall time					
$t_{DO}$	Default output delay time from input power loss	Measured from the time $V_{CC1}$ goes below 1.7V. See 图 23-2		0.1	0.3	$\mu\text{s}$
$t_{ie}$	Time interval error	$2^{16} - 1$ PRBS data at 100 Mbps		1		ns

(1) Also known as pulse skew.

(2)  $t_{sk(pp)}$  is the magnitude of the difference in propagation delay times between any terminals of different devices switching in the same direction while operating at identical supply voltages, temperature, input signals and loads.

## 21 Switching Characteristics—3.3-V Supply

$V_{CC1} = V_{CC2} = 3.3\text{ V} \pm 10\%$  (over recommended operating conditions unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{PLH}, t_{PHL}$	Propagation delay time	See 图 23-1	6	11	18.5	ns
PWD	Pulse width distortion <sup>(1)</sup> $ t_{PHL} - t_{PLH} $					
$t_{sk(pp)}$	Part-to-part skew time <sup>(2)</sup>				4.5	ns
$t_r$	Output signal rise time	See 图 23-1		0.7	3	ns
$t_f$	Output signal fall time					
$t_{DO}$	Default output delay time from input power loss	Measured from the time $V_{CC1}$ goes below 1.7V. See 图 23-2		0.1	0.3	$\mu\text{s}$
$t_{ie}$	Time interval error	$2^{16} - 1$ PRBS data at 100 Mbps		1		ns

(1) Also known as pulse skew.

(2)  $t_{sk(pp)}$  is the magnitude of the difference in propagation delay times between any terminals of different devices switching in the same direction while operating at identical supply voltages, temperature, input signals and loads.

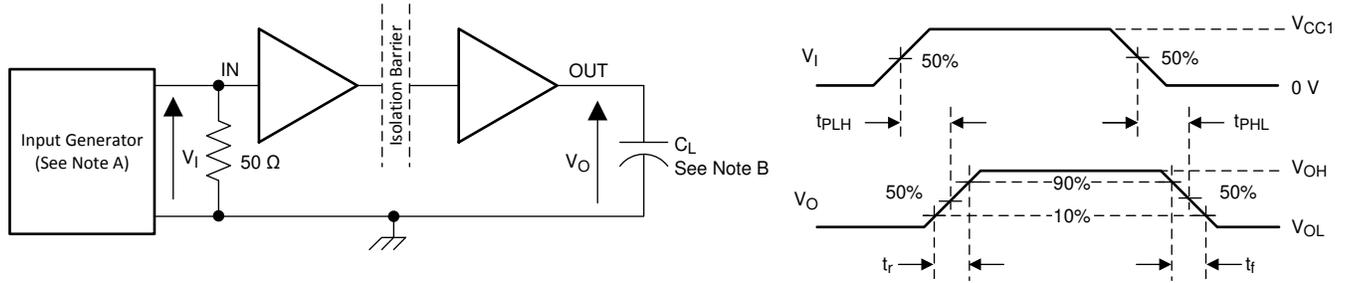
## 22 Switching Characteristics—2.5-V Supply

$V_{CC1} = V_{CC2} = 2.5\text{ V} \pm 10\%$  (over recommended operating conditions unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{PLH}, t_{PHL}$	Propagation delay time	See 图 23-1	7.5	12	21	ns
PWD	Pulse width distortion <sup>(1)</sup> $ t_{PHL} - t_{PLH} $			0.2	5.9	ns
$t_{sk(pp)}$	Part-to-part skew time <sup>(2)</sup>				4.6	ns
$t_r$	Output signal rise time	See 图 23-1		1	3.5	ns
$t_f$	Output signal fall time			1	3.5	ns
$t_{DO}$	Default output delay time from input power loss	Measured from the time $V_{CC1}$ goes below 1.7V. See 图 23-2		0.1	0.3	$\mu\text{s}$
$t_{ie}$	Time interval error	$2^{16} - 1$ PRBS data at 100 Mbps		1		ns

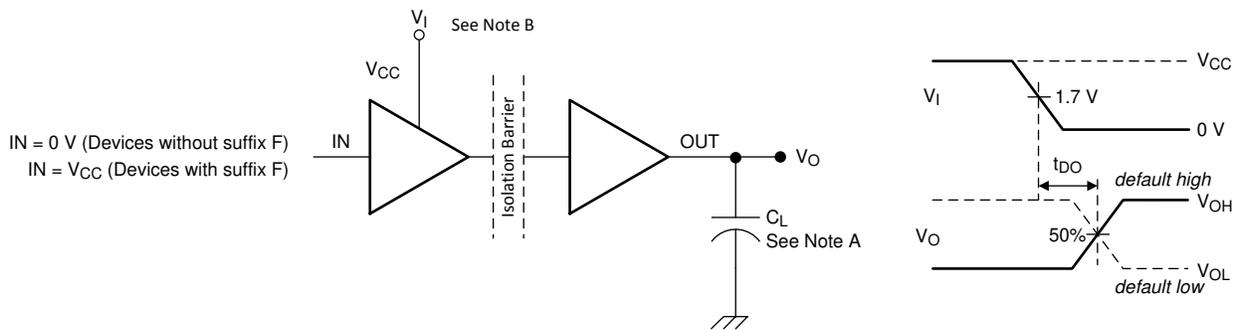
- (1) Also known as pulse skew.  
 (2)  $t_{sk(pp)}$  is the magnitude of the difference in propagation delay times between any terminals of different devices switching in the same direction while operating at identical supply voltages, temperature, input signals and loads.

## 23 Parameter Measurement Information



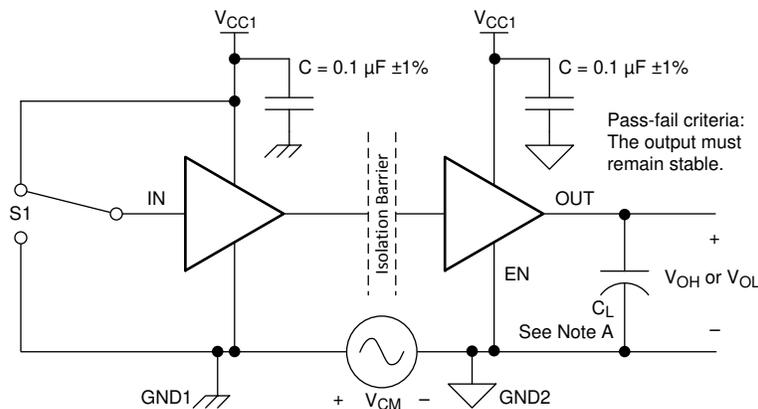
- A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 50 kHz, 50% duty cycle,  $t_r \leq 3$  ns,  $t_f \leq 3$  ns,  $Z_0 = 50 \Omega$ . At the input, 50 Ω resistor is required to terminate Input Generator signal. The 50 Ω resistor is not needed in actual application.
- B.  $C_L = 15$  pF and includes instrumentation and fixture capacitance within ±20%.

图 23-1. Switching Characteristics Test Circuit and Voltage Waveforms



- A.  $C_L = 15$  pF and includes instrumentation and fixture capacitance within ±20%.
- B. Power Supply Ramp Rate = 10 mV/ns

图 23-2. Default Output Delay Time Test Circuit and Voltage Waveforms



- A.  $C_L = 15$  pF and includes instrumentation and fixture capacitance within ±20%.

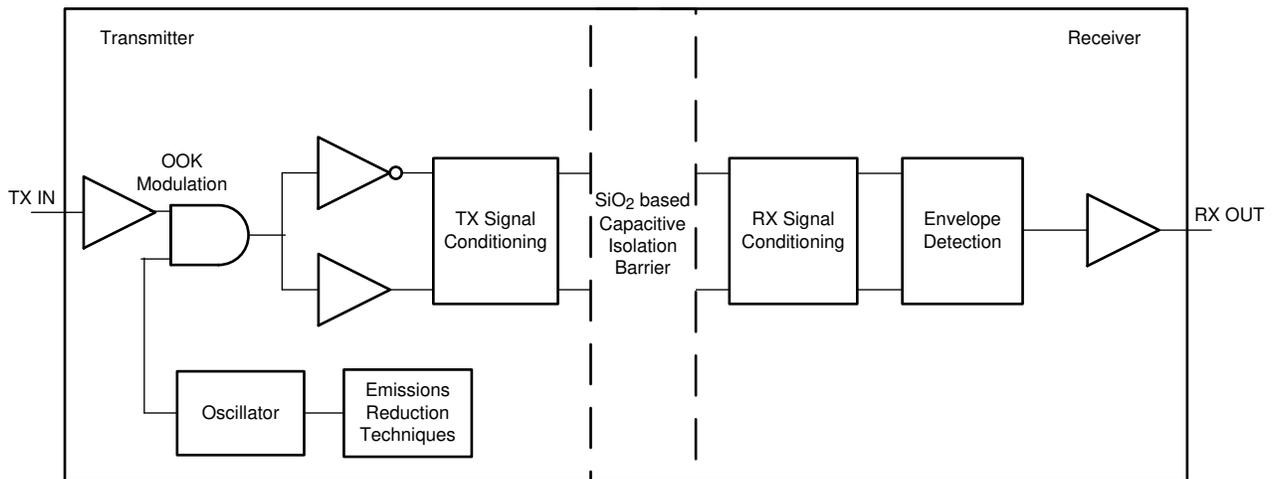
图 23-3. Common-Mode Transient Immunity Test Circuit

## 24 Detailed Description

### 24.1 Overview

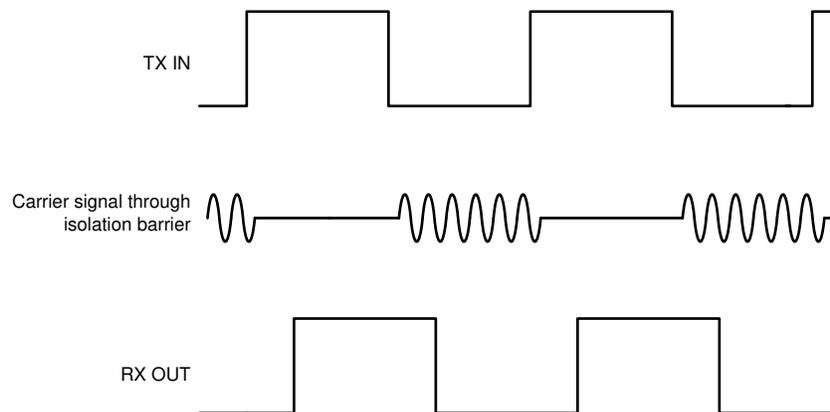
The ISO7710-Q1 device has an ON-OFF keying (OOK) modulation scheme to transmit the digital data across a silicon dioxide based isolation barrier. The transmitter sends a high frequency carrier across the barrier to represent one digital state and sends no signal to represent the other digital state. The receiver demodulates the signal after advanced signal conditioning and produces the output through a buffer stage. The device also incorporates advanced circuit techniques to maximize the CMTI performance and minimize the radiated emissions due the high frequency carrier and IO buffer switching. The conceptual block diagram of a digital capacitive isolator, [图 24-1](#), shows a functional block diagram of a typical channel.

### 24.2 Functional Block Diagram



**图 24-1. Conceptual Block Diagram of a Digital Capacitive Isolator**

[图 24-2](#) shows a conceptual detail of how the OOK scheme works.



**图 24-2. On-Off Keying (OOK) Based Modulation Scheme**

## 24.3 Feature Description

The ISO7710-Q1 device is available in two default output state options to enable a variety of application uses. [表 24-1](#) lists the device features.

**表 24-1. Device Features**

PART NUMBER	MAXIMUM DATA RATE	CHANNEL DIRECTION	DEFAULT OUTPUT STATE	PACKAGE	RATED ISOLATION <sup>(1)</sup>
ISO7710-Q1	100 Mbps	1 Forward, 0 Reverse	High	DW-16	5000 V <sub>RMS</sub> / 8000 V <sub>PK</sub>
				D-8	3000 V <sub>RMS</sub> / 4242 V <sub>PK</sub>
ISO7710-Q1 with F suffix	100 Mbps	1 Forward, 0 Reverse	Low	DW-16	5000 V <sub>RMS</sub> / 8000 V <sub>PK</sub>
				D-8	3000 V <sub>RMS</sub> / 4242 V <sub>PK</sub>

(1) See the *Safety-Related Certifications* section for detailed isolation ratings.

### 24.3.1 Electromagnetic Compatibility (EMC) Considerations

Many applications in harsh industrial environment are sensitive to disturbances such as electrostatic discharge (ESD), electrical fast transient (EFT), surge and electromagnetic emissions. These electromagnetic disturbances are regulated by international standards such as IEC 61000-4-x and CISPR 22. Although system-level performance and reliability depends, to a large extent, on the application board design and layout, the ISO7710-Q1 device incorporates many chip-level design improvements for overall system robustness. Some of these improvements include:

- Robust ESD protection cells for input and output signal pins and inter-chip bond pads.
- Low-resistance connectivity of ESD cells to supply and ground pins.
- Enhanced performance of high voltage isolation capacitor for better tolerance of ESD, EFT and surge events.
- Bigger on-chip decoupling capacitors to bypass undesirable high energy signals through a low impedance path.
- PMOS and NMOS devices isolated from each other by using guard rings to avoid triggering of parasitic SCRs.
- Reduced common mode currents across the isolation barrier by providing purely differential internal operation.

## 24.4 Device Functional Modes

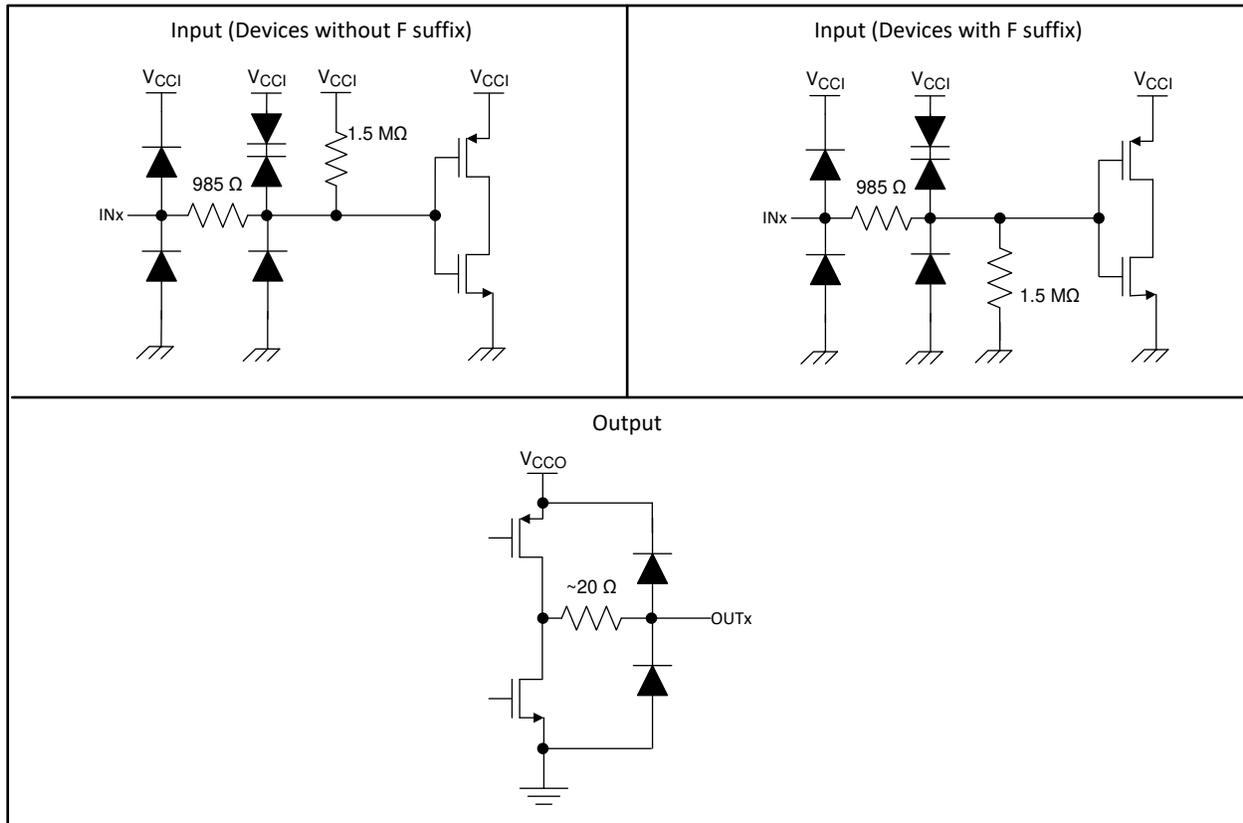
表 24-2 lists the functional modes of ISO7710-Q1 device.

表 24-2. Function Table

$V_{CC1}$ <sup>(1)</sup>	$V_{CC2}$	INPUT (IN) <sup>(3)</sup>	OUTPUT (OUT)	COMMENTS
PU	PU	H	H	Normal Operation: A channel output assumes the logic state of the input.
		L	L	
		Open	Default	Default mode: When IN is open, the corresponding channel output goes to the default logic state. Default is <i>High</i> for ISO7710-Q1 and <i>Low</i> for ISO7710-Q1 with F suffix.
PD	PU	X	Default	Default mode: When $V_{CC1}$ is unpowered, a channel output assumes the logic state based on the selected default option. Default is <i>High</i> for ISO7710-Q1 and <i>Low</i> for ISO7710-Q1 with F suffix. When $V_{CC1}$ transitions from unpowered to powered-up, a channel output assumes the logic state of the input. When $V_{CC1}$ transitions from powered-up to unpowered, channel output assumes the selected default state.
X	PD	X	Undetermined	When $V_{CC2}$ is unpowered, a channel output is undetermined <sup>(2)</sup> . When $V_{CC2}$ transitions from unpowered to powered-up, a channel output assumes the logic state of the input

- (1) PU = Powered up ( $V_{CC} \geq 2.25$  V); PD = Powered down ( $V_{CC} \leq 1.7$  V); X = Irrelevant; H = High level; L = Low level  
 (2) The outputs are in undetermined state when  $1.7$  V <  $V_{CC1}$ ,  $V_{CC2}$  <  $2.25$  V.  
 (3) A strongly driven input signal can weakly power the floating  $V_{CC}$  using an internal protection diode and cause undetermined output.

### 24.4.1 Device I/O Schematics



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图 24-3. Device I/O Schematics

## 25 Application and Implementation

### 备注

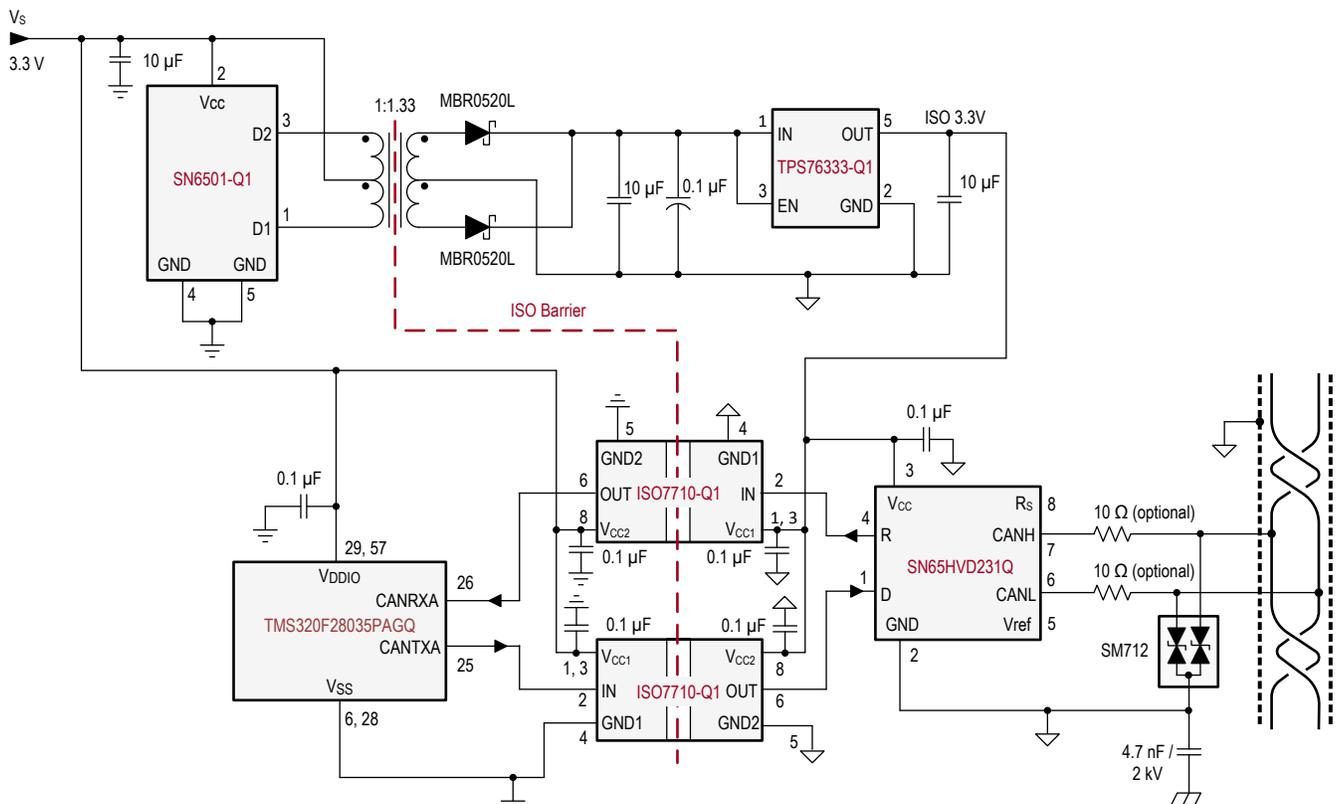
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### 25.1 Application Information

The ISO7710-Q1 device is a high-performance, single-channel digital isolator. The device uses single-ended CMOS-logic switching technology. The supply voltage range is from 2.25 V to 5.5 V for both supplies,  $V_{CC1}$  and  $V_{CC2}$ . When designing with digital isolators, keep in mind that because of the single-ended design structure, digital isolators do not conform to any specific interface standard and are only intended for isolating single-ended CMOS or TTL digital signal lines. The isolator is typically placed between the data controller (that is,  $\mu C$  or UART), and a data converter or a line transceiver, regardless of the interface type or standard.

### 25.2 Typical Application

The ISO7710-Q1 device can be used with Texas Instruments' mixed signal microcontroller, CAN transceiver, transformer driver, and low-dropout voltage regulator to create an Isolated CAN Interface as shown below.



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图 25-1. Isolated CAN Interface

### 25.2.1 Design Requirements

To design with this device, use the parameters listed in 表 25-1.

表 25-1. Design Parameters

PARAMETER	VALUE
Supply voltage, $V_{CC1}$ and $V_{CC2}$	2.25 V to 5.5 V
Decoupling capacitor between $V_{CC1}$ and GND1	0.1 $\mu$ F
Decoupling capacitor from $V_{CC2}$ and GND2	0.1 $\mu$ F

### 25.2.2 Detailed Design Procedure

Unlike optocouplers, which require components to improve performance, provide bias, or limit current, the ISO7710-Q1 device only requires two external bypass capacitors to operate.

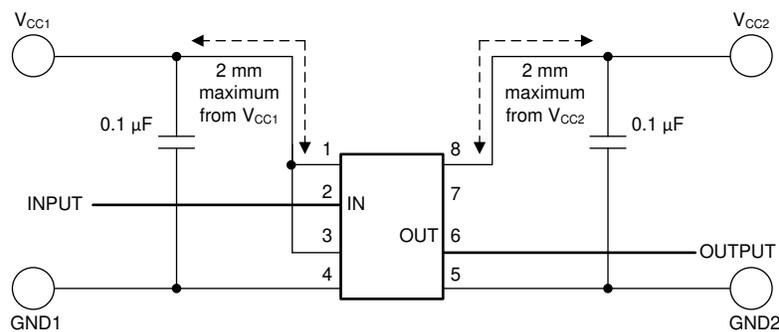


图 25-2. Typical ISO7710-Q1 Circuit Hook-up

### 25.2.3 Application Curve

The following typical eye diagram of the ISO7710-Q1 device indicates low jitter and wide open eye at the maximum data rate of 100 Mbps.

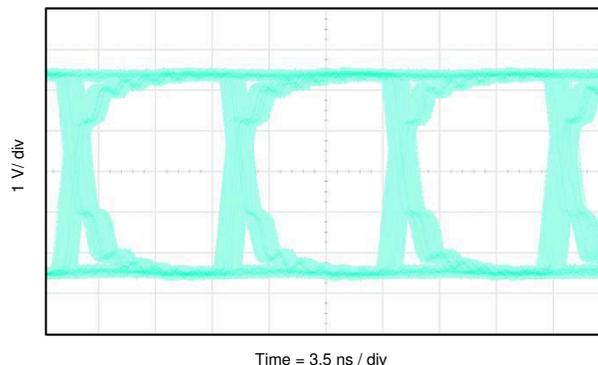


图 25-3. ISO7710-Q1 Eye Diagram at 100 Mbps PRBS, 5-V Supplies and 25°C

#### 25.2.3.1 Insulation Lifetime

Insulation lifetime projection data is collected by using industry-standard Time Dependent Dielectric Breakdown (TDDB) test method. In this test, all pins on each side of the barrier are tied together creating a two-terminal device and high voltage applied between the two sides; See 图 25-4 for TDDB test setup. The insulation breakdown data is collected at various high voltages switching at 60 Hz over temperature. For reinforced insulation, VDE standard requires the use of TDDB projection line with failure rate of less than 1 part per million

(ppm). Even though the expected minimum insulation lifetime is 20 years at the specified working isolation voltage, VDE reinforced certification requires additional safety margin of 20% for working voltage and 50% for lifetime which translates into minimum required insulation lifetime of 30 years at a working voltage that's 20% higher than the specified value.

图 25-5 shows the intrinsic capability of the isolation barrier to withstand high voltage stress over the lifetime of the device. Based on the TDDB data, the intrinsic capability of the insulation is 1500 V<sub>RMS</sub> with a lifetime of 36 years. Other factors, such as package size, pollution degree, material group, and more, can further limit the working voltage of the component. The working voltage of DW-16 package is specified up to 1500 V<sub>RMS</sub> and D-8 package up to 450 V<sub>RMS</sub>. At the lower working voltages, the corresponding insulation lifetime is much longer than 36 years.

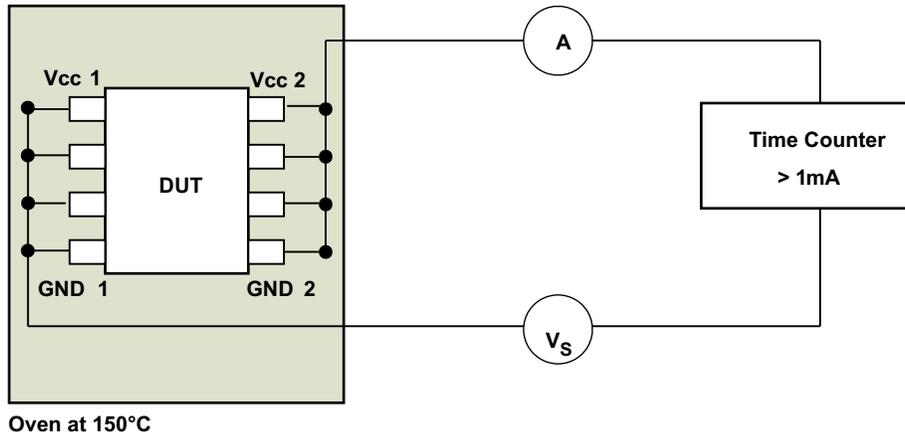


图 25-4. Test Setup for Insulation Lifetime Measurement

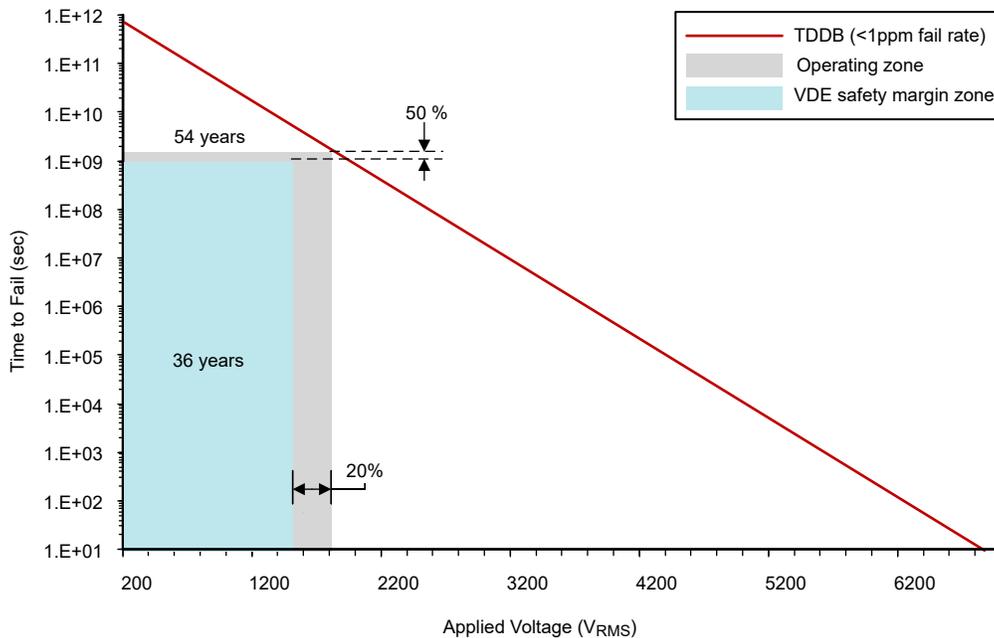


图 25-5. Insulation Lifetime Projection Data

### 25.3 Power Supply Recommendations

To help provide reliable operation at data rates and supply voltages, a 0.1- μ F bypass capacitor is recommended at the input and output supply pins (V<sub>CC1</sub> and V<sub>CC2</sub>). The capacitors must be placed as close to the supply pins

as possible. If only a single primary-side power supply is available in an application, isolated power can be generated for the secondary-side with the help of a transformer driver such as Texas Instruments' [SN6501-Q1](#). For such applications, detailed power supply design and transformer selection recommendations are available in [SN6501-Q1 Transformer Driver for Isolated Power Supplies](#).

## 25.4 Layout

### 25.4.1 Layout Guidelines

A minimum of four layers is required to accomplish a low EMI PCB design (see [图 25-6](#)). Layer stacking must be in the following order (top-to-bottom): high-speed signal layer, ground plane, power plane and low-frequency signal layer.

- Routing the high-speed traces on the top layer avoids the use of vias (and the introduction of via inductances) and allows for clean interconnects between the isolator and the transmitter and receiver circuits of the data link.
- Placing a solid ground plane next to the high-speed signal layer establishes controlled impedance for transmission line interconnects and provides an excellent low-inductance path for the return current flow.
- Placing the power plane next to the ground plane creates additional high-frequency bypass capacitance of approximately 100 pF/in<sup>2</sup>.
- Routing the slower speed control signals on the bottom layer allows for greater flexibility as these signal links typically have margin to tolerate discontinuities such as vias.

If an additional supply voltage plane or signal layer is needed, add a second power or ground plane system to the stack to keep the planes symmetrical. This design makes the stack mechanically stable and prevents warping. Also the power and ground plane of each power system can be placed closer together, thus increasing the high-frequency bypass capacitance significantly.

For detailed layout recommendations, refer to the [Digital Isolator Design Guide](#).

#### 25.4.1.1 PCB Material

For digital circuit boards operating at less than 150 Mbps, (or rise and fall times greater than 1 ns), and trace lengths of up to 10 inches, use standard FR-4 UL94V-0 printed circuit board. This PCB is preferred over cheaper alternatives because of lower dielectric losses at high frequencies, less moisture absorption, greater strength and stiffness, and the self-extinguishing flammability-characteristics.

#### 25.4.2 Layout Example

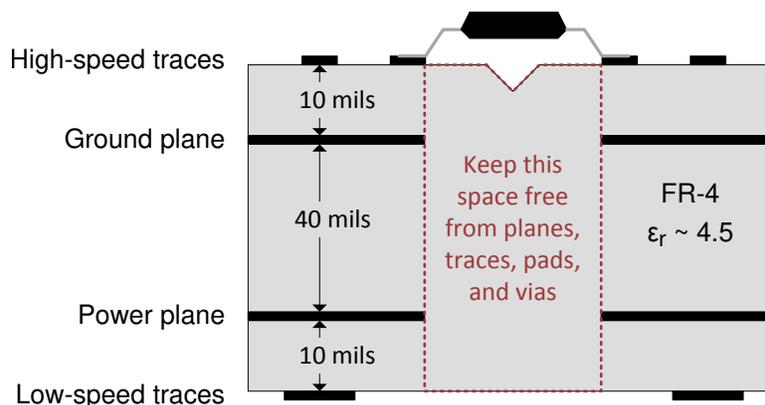


图 25-6. Layout Example

## 26 Device and Documentation Support

### 26.1 Documentation Support

#### 26.1.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, [Digital Isolator Design Guide](#), application note
- Texas Instruments, [Isolation Glossary](#), application note
- Texas Instruments, [How to use isolation to improve ESD, EFT, and Surge immunity in industrial systems](#), analog design journal
- Texas Instruments, [SN6501-Q1 Transformer Driver for Isolated Power Supplies](#), data sheet
- Texas Instruments, [SN65HVD231Q Automotive 3.3-V CAN Transceiver](#), data sheet
- Texas Instruments, [TPS76333-Q1 Low-Power 150-mA Low-Dropout Linear Regulators](#), data sheet
- Texas Instruments, [TMS320F28035PAGQ Piccolo™ Microcontrollers](#), data sheet

#### 26.2 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

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#### 26.4 支持资源

[TI E2E™ 中文支持论坛](#) 是工程师的重要参考资料，可直接从专家处获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题，获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的 [使用条款](#)。

#### 26.5 Trademarks

Piccolo™ is a trademark of Texas Instruments.

TI E2E™ is a trademark of Texas Instruments.

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#### 26.6 静电放电警告



静电放电 (ESD) 会损坏这个集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

#### 26.7 术语表

[TI 术语表](#) 本术语表列出并解释了术语、首字母缩略词和定义。

## 27 Revision History

注：以前版本的页码可能与当前版本的页码不同

<b>Changes from Revision B (October 2020) to Revision C (December 2024)</b>	<b>Page</b>
• 将整个文档中的标准名称从“DIN V VDE V 0884-11:2017-01”更改为“DIN EN IEC 60747-17 (VDE 0884-17)” .....	1
• 通篇删除了对标准 IEC/EN/CSA 60950-1 的引用.....	1
• 通篇删除了所有标准名称中的标准版本和年份参考.....	1
• 更新了整个文档中的表格、图和交叉参考的编号格式.....	1
• Added "Contact discharge per IEC 61000-4-2" specification of 8000V .....	5
• Changed "Signaling rate" to "Data rate" and added table note.....	6
• Updated maximum power dissipation in the power ratings section.....	7
• Updated distance through isolation, while maintaining other insulation specifications.....	8
• Updated DW-16 package $V_{IORM}$ and $V_{IOWM}$ values.....	8
• Added TDDDB figure reference to $V_{IOWM}$ .....	8
• Updated $V_{IOSM}$ , $V_{IOTM}$ , $q_{pd}$ test conditions.....	8
• Updated maximum total current consumption values throughout the supply current characteristics sections.	11
• Updated maximum propagation delay specifications throughout the switching characteristics sections.....	14
• Updated TDDDB plot and the projected lifetime.....	21
• Changed working voltage lifetime margin from: 87.5% to: 50%, minimum required insulation lifetime from: 37.5 years to: 30 years and insulation lifetime per TDDDB from: 135 years to: 169 years per DIN EN IEC 60747-17 (VDE 0884-17).....	21
• Changed <a href="#">图 25-5</a> per DIN EN IEC 60747-17 (VDE 0884-17).....	21

<b>Changes from Revision A (April 2020) to Revision B (October 2020)</b>	<b>Page</b>
• 在 <a href="#">节 1</a> 中添加了“功能安全”要点.....	1
• Added D-8 values for TUV.....	9

<b>Changes from Revision * (March 2017) to Revision A (April 2020)</b>	<b>Page</b>
• 通篇进行了编辑性和修饰性更改.....	1
• 将“隔离栅寿命：超过 40 年”更改为“在 1500V <sub>RMS</sub> 工作电压下预计寿命超过 100 年”（位于 <a href="#">节 1</a> ）.....	1
• 在 <a href="#">节 1</a> 中添加了“隔离等级高达 5000V <sub>RMS</sub> ” .....	1
• 在 <a href="#">节 1</a> 中添加了“浪涌能力高达 12.8kV” .....	1
• 在 <a href="#">节 1</a> 中添加了“在整个隔离栅具有 ±8kV IEC 61000-4-2 接触放电保护” .....	1
• 将“符合 DIN V VDE V 0884-10 (VDE V 0884-10):2006-12 标准的 VDE 增强型绝缘”更改为“符合 DIN VDE V 0884-11:2017-01 标准的 VDE 增强型绝缘”（位于 <a href="#">节 1</a> ）.....	1
• 使用 <a href="#">节 1</a> 中的标准名称，将 CSA、CQC 和 TUV 要点合并为一个要点.....	1
• 删除了 <a href="#">节 1</a> 中的“完成 DW-16 封装的 VDE、UL、CSA 和 TUV 认证；已规划其他所有认证”要点.....	1
• 更新了 <a href="#">节 2</a> 部分的应用列表.....	1
• 更新了 <a href="#">简化版原理图</a> ，以便显示两个串联的隔离电容器，而不是单个隔离电容器.....	1
• Added Climatic category.....	8
• Updated CSA column and changed DW package to (DW-16).....	9
• Changed $t_{ie}$ TYP value from 1.5 to 1 in Switching Characteristics tables throughout the document.....	14
• Corrected ground symbols for "Input (Devices with F suffix)" in <a href="#">节 24.4.1</a> .....	19
• Fixed <a href="#">图 25-2</a> INPUT wire connection .....	21
• Added <a href="#">节 25.2.3.1</a> sub-section under <a href="#">节 25.2.3</a> section .....	21

- Added '*How to use isolation to improve ESD, EFT, and Surge immunity in industrial systems*' to [节 26.1](#) section ..... 24
- 

## 28 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

**PACKAGING INFORMATION**

Orderable part number	Status (1)	Material type (2)	Package   Pins	Package qty   Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
<a href="#">ISO7710FQDRQ1</a>	Active	Production	SOIC (D)   8	2500   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	(7710F, 7710FQ)
ISO7710FQDRQ1.A	Active	Production	SOIC (D)   8	2500   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	(7710F, 7710FQ)
<a href="#">ISO7710FQDWRQ1</a>	Active	Production	SOIC (DW)   16	2000   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	(ISO7710F, ISO7710FQ)
ISO7710FQDWRQ1.A	Active	Production	SOIC (DW)   16	2000   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	(ISO7710F, ISO7710FQ)
<a href="#">ISO7710QDRQ1</a>	Active	Production	SOIC (D)   8	2500   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	(7710, 7710Q)
ISO7710QDRQ1.A	Active	Production	SOIC (D)   8	2500   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	(7710, 7710Q)
<a href="#">ISO7710QDWRQ1</a>	Active	Production	SOIC (DW)   16	2000   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	(ISO7710, ISO7710Q)
ISO7710QDWRQ1.A	Active	Production	SOIC (DW)   16	2000   LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	(ISO7710, ISO7710Q)

<sup>(1)</sup> **Status:** For more details on status, see our [product life cycle](#).

<sup>(2)</sup> **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

<sup>(3)</sup> **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

<sup>(4)</sup> **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

<sup>(5)</sup> **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

<sup>(6)</sup> **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "-" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

**Important Information and Disclaimer:** The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

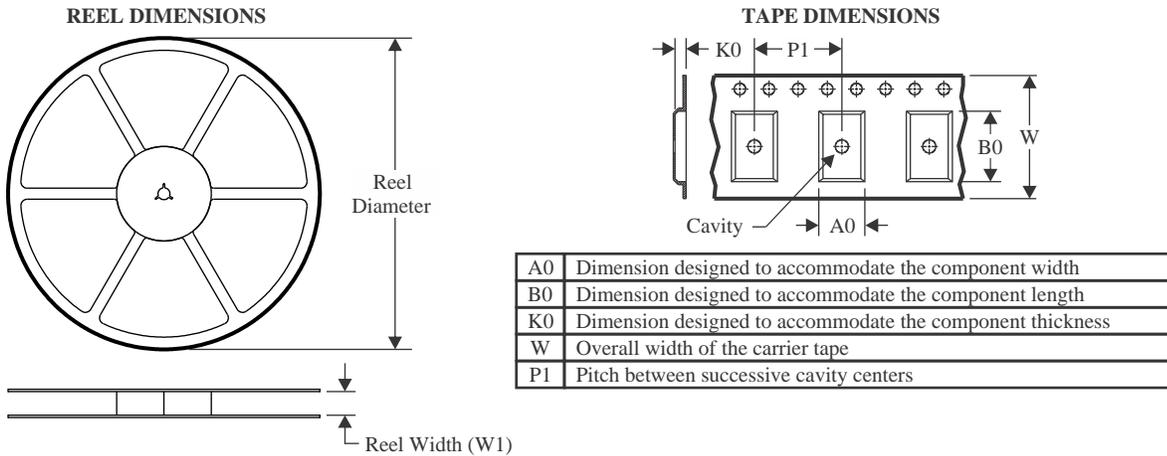
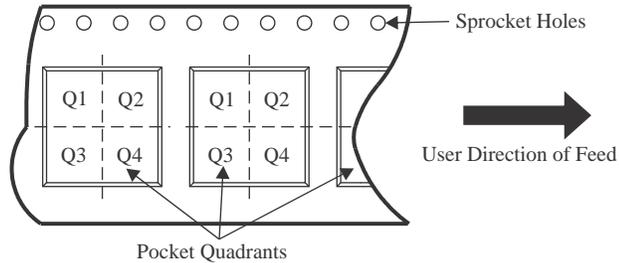
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**OTHER QUALIFIED VERSIONS OF ISO7710-Q1 :**

- Catalog : [ISO7710](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ISO7710FQDRQ1	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
ISO7710FQDRQ1	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
ISO7710FQDWRQ1	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1
ISO7710QDRQ1	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
ISO7710QDWRQ1	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ISO7710FQDRQ1	SOIC	D	8	2500	353.0	353.0	32.0
ISO7710FQDRQ1	SOIC	D	8	2500	350.0	350.0	43.0
ISO7710FQDWRQ1	SOIC	DW	16	2000	353.0	353.0	32.0
ISO7710QDRQ1	SOIC	D	8	2500	353.0	353.0	32.0
ISO7710QDWRQ1	SOIC	DW	16	2000	353.0	353.0	32.0

## GENERIC PACKAGE VIEW

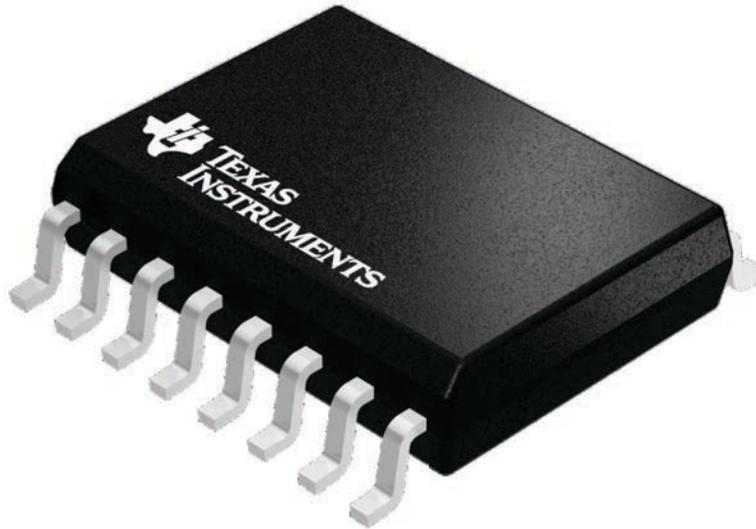
**DW 16**

**SOIC - 2.65 mm max height**

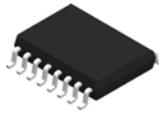
7.5 x 10.3, 1.27 mm pitch

SMALL OUTLINE INTEGRATED CIRCUIT

This image is a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.



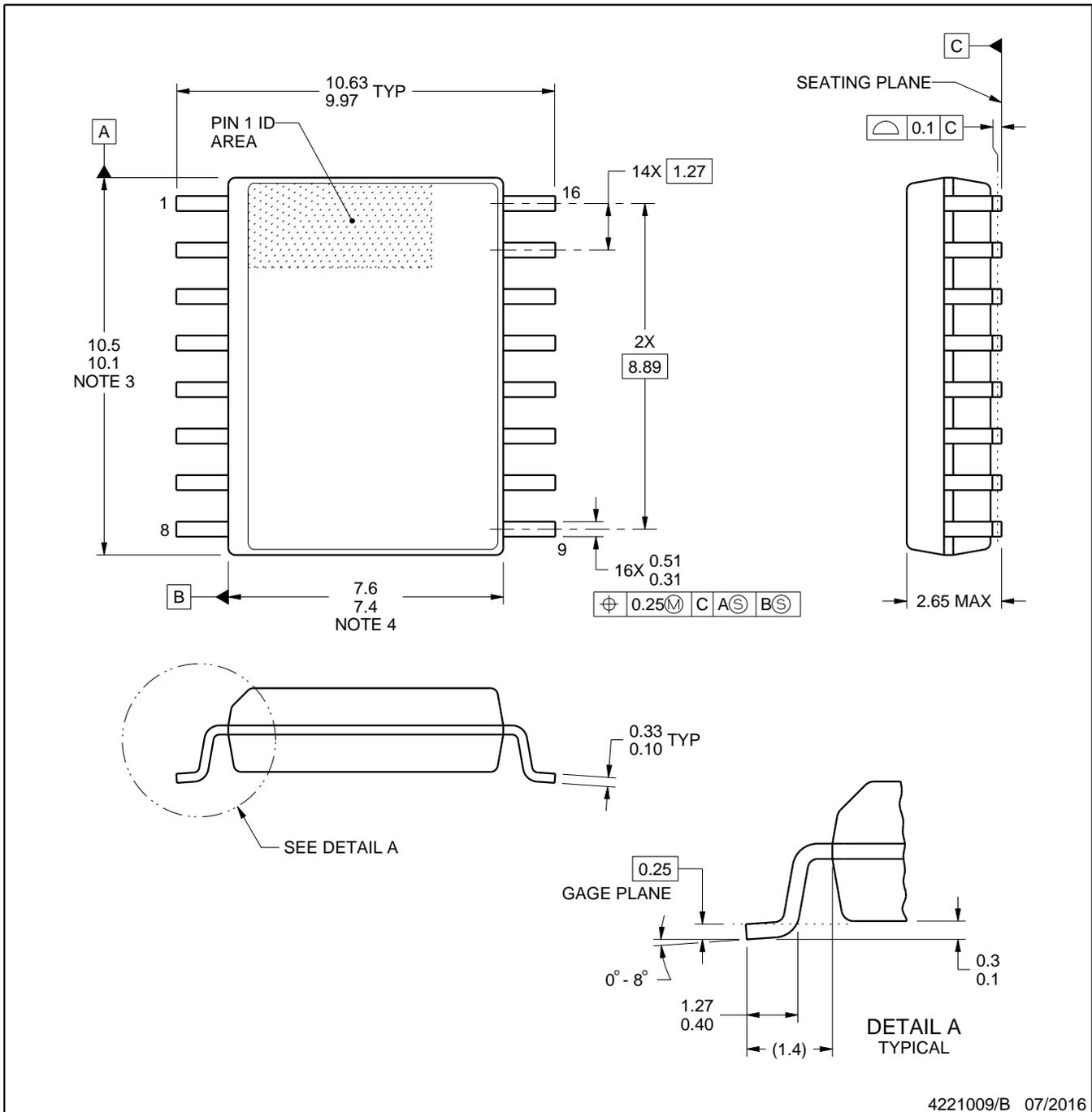
4224780/A



# DW0016B

# PACKAGE OUTLINE SOIC - 2.65 mm max height

SOIC



4221009/B 07/2016

### NOTES:

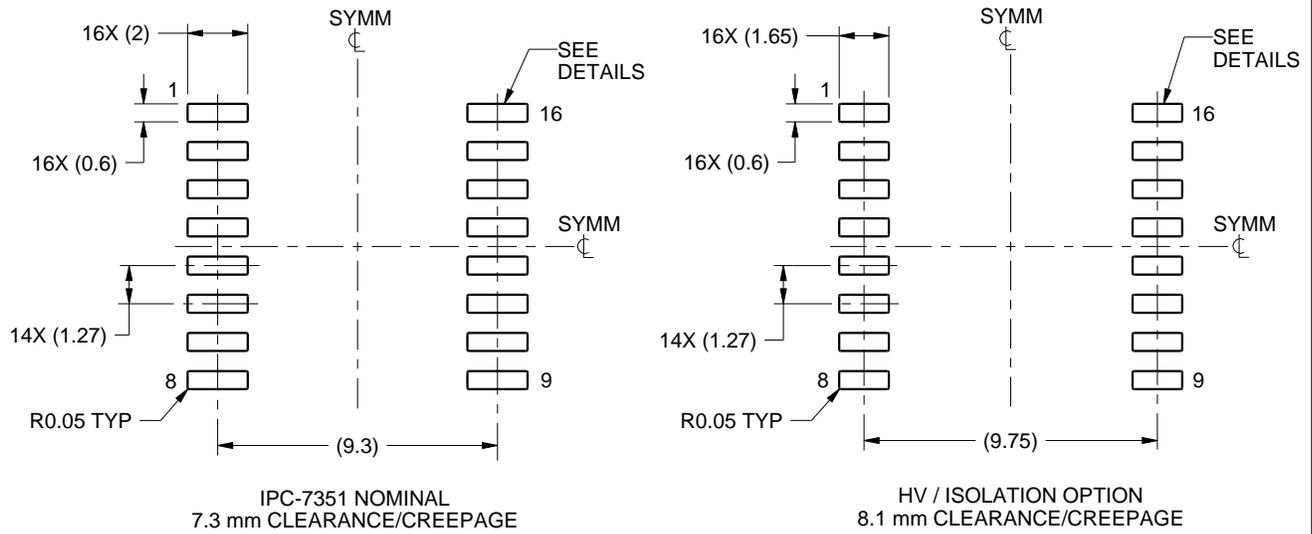
1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.
5. Reference JEDEC registration MS-013.

# EXAMPLE BOARD LAYOUT

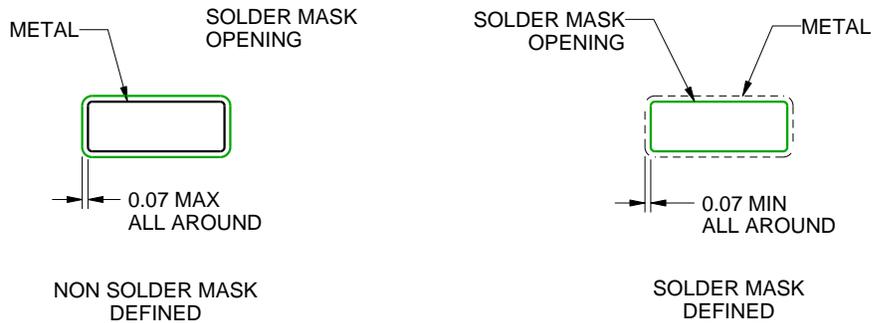
DW0016B

SOIC - 2.65 mm max height

SOIC



LAND PATTERN EXAMPLE  
SCALE:4X



SOLDER MASK DETAILS

4221009/B 07/2016

NOTES: (continued)

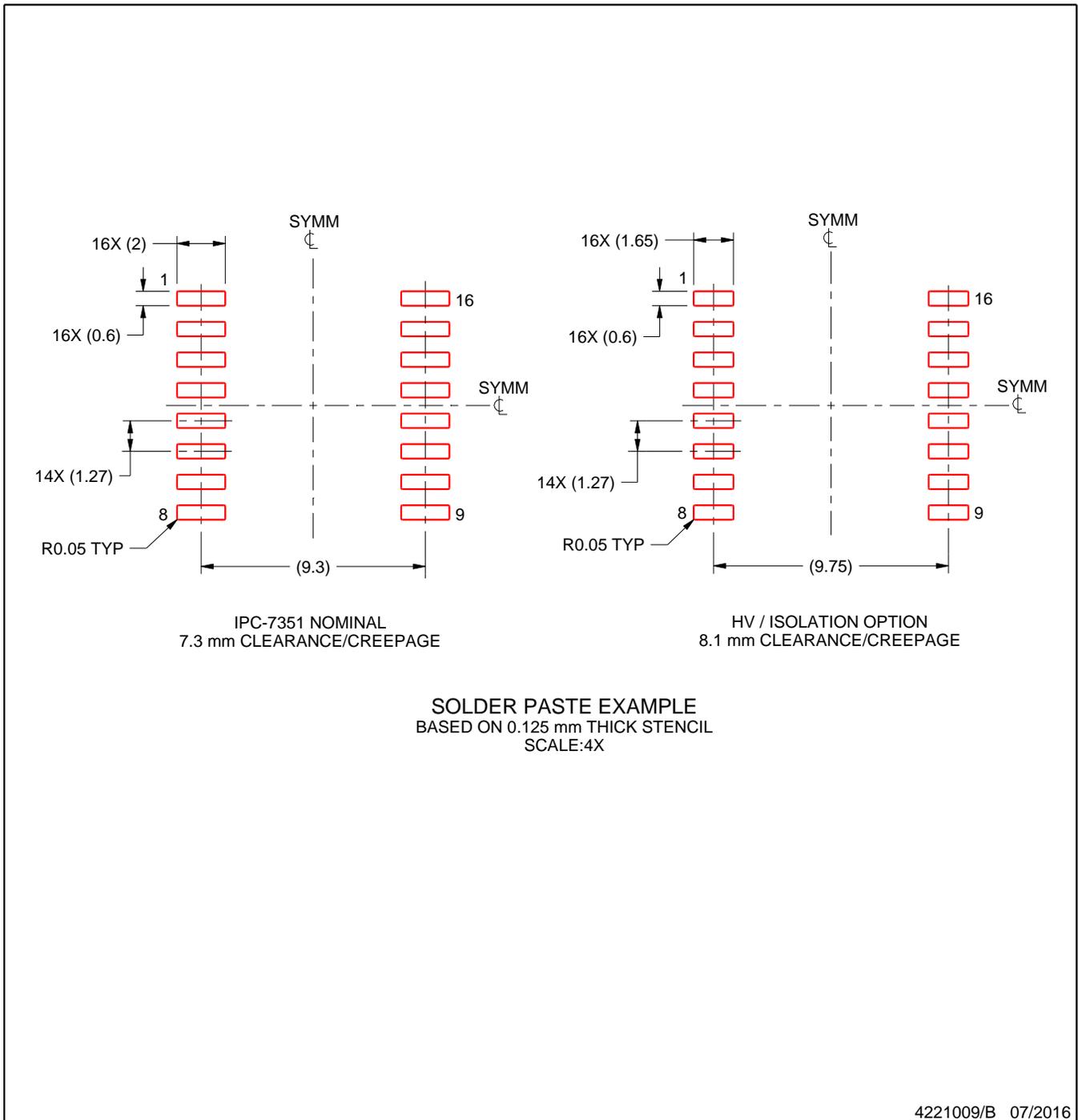
- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

DW0016B

SOIC - 2.65 mm max height

SOIC



NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

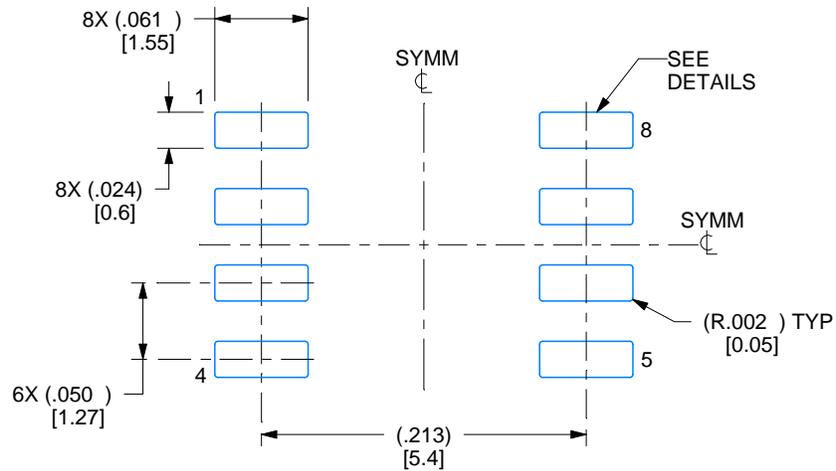


# EXAMPLE BOARD LAYOUT

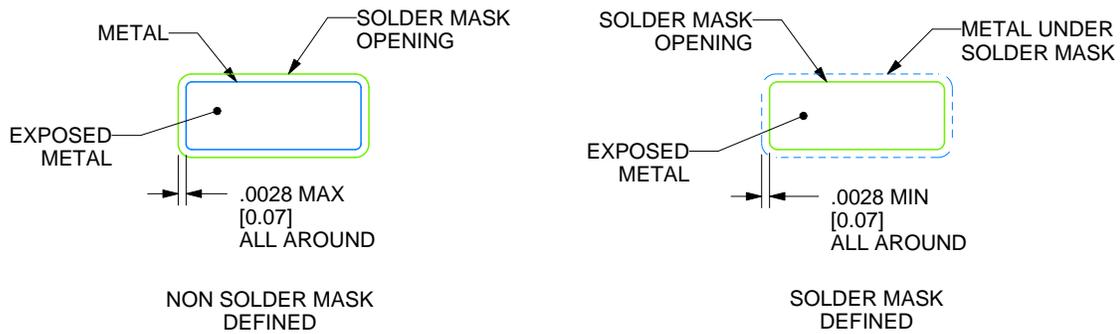
D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

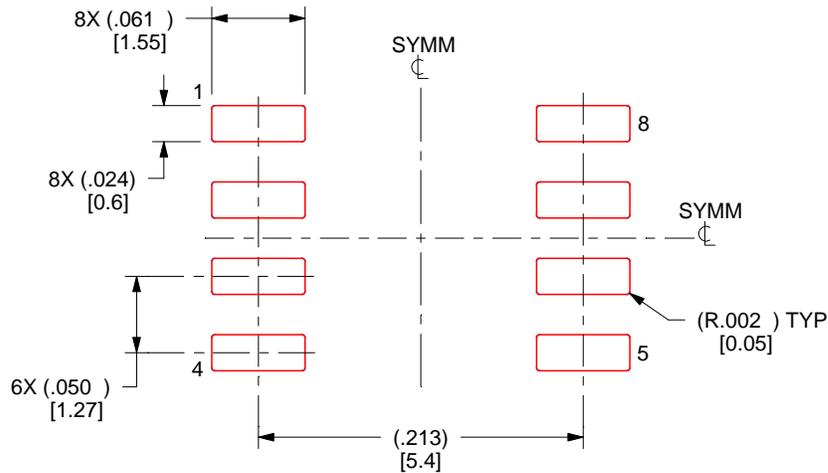
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE  
BASED ON .005 INCH [0.125 MM] THICK STENCIL  
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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