ISOW14x2 具有集成式高效低辐射低噪声直流/直流转换器的隔离式 RS-485/RS-422 收发器

1 特性

- 符合或超出 TIA/EIA-485A 标准要求
- 数据速率
  - ISOW1412：500kbps
  - ISOW1432：12Mbps
- 低排放、低噪声的集成式低排放直流/直流转换器
  - 符合 CISPR 32 B 类和 EN 55032 B 类要求，并在两层 PCB 上留有裕度
  - 25MHz 的低频电源转换器可实现低噪声性能
- 其他 2Mbps GPIO 通道
- 高效率输出功率
  - 典型效率：46%
  - V_{ISOOUT} 精度：±5%
  - 额外输出电流：20mA
- 用于 RS-485 和直流/直流的独立电源
  - 逻辑电源 (V_{IO})：1.71V 至 5.5V
  - 电源转换器电源 (V_{DD})：3V 至 5.5V
- RS-485 与 PROFIBUS 兼容
  - 开路、短路和空闲总线失效防护
  - 1/8 单位负载：多达 256 个总线节点
  - 上电和断电无干扰
- 增强型和基础型隔离选项
- 高 CMTI：100kV/μs（典型值）
- 高 ESD 总线保护
  - HBM：±16kV
  - IEC 61000-4-2 接触放电：±8kV
- 工作温度范围：-40°C 至 125°C
- 电流限制和热关断
- 20 引脚宽体 SOIC 封装
- 节 8.6：
  - 符合 DIN VDE V 0884-11:2017-01 标准的 VDE 增强型和基础型绝缘
  - UL 1577 组件认证计划
  - IEC 62368-1、IEC 61010-1、IEC 60601-1 和 GB 4943.1-2011 认证

2 应用

- 工厂自动化
- 楼宇自动化
- 工业运输
- 光伏逆变器，保护继电器
- 电机驱动器

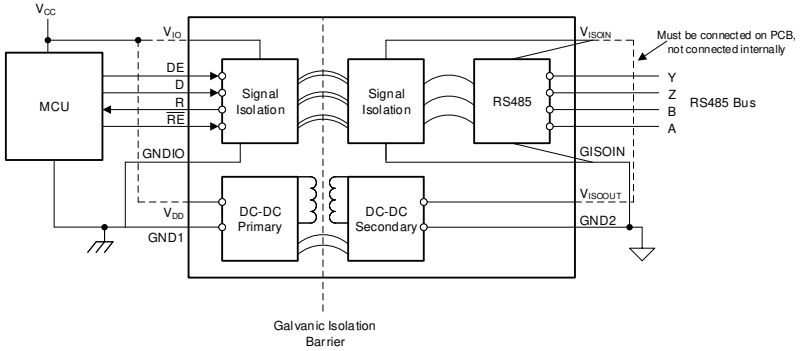
3 说明

ISOW14x2 器件是 电隔离 RS-485/RS-422 收发器，内置隔离式直流/直流转换器，无需在空间受限的隔离式设计中使用单独的隔离式电源。低辐射、隔离式直流/直流转换器符合 CISPR 32 辐射发射 B 类标准，在简单的两层 PCB 上仅使用两个铁氧体磁珠。额外的 20mA 输出电流可用于为板上的其他电路供电。集成的 2Mbps GPIO 通道有助于去除用于诊断、LED 指示或电源监控的任何额外数字隔离器或光耦合器。

器件信息

特性	ISOW1412 ISOW1432	ISOW1412B ISOW1432B
保护级别	增强版	基本版
浪涌测试电压	$10kV_{PK}$	$7.8kV_{PK}$
隔离额定值	$5000V_{RMS}$	$5000V_{RMS}$
工作电压	$1000V_{RMS}/1500V_{PK}$	$1000V_{RMS}/1500V_{PK}$
封装(1)	DFM (20)	DFM (20)
封装尺寸	12.83mm x 7.5mm	12.83mm x 7.5mm

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。



简化版原理图

Table of Contents

4 Revision History

注：以前版本的页码可能与当前版本的页码不同

Changes from Revision * (May 2018) to Revision A (May 2021)	Page
• 更新了数据表以包含 ISOW1432 器件	1

Changes from Revision A (May 2021) to Revision B (October 2021)	Page
• 将 ISOW1412 从“预告信息”更改成了“量产数据”。	1

5 说明（续）

提供了两个数据速率选项：ISOW1412 针对最大 500kbps 进行了优化，ISOW1432 适合最大 12Mbps 数据速率。除了旁路电容器外，这些器件不需要任何其他外部元件即可实现隔离式 RS-485 端口，非常适合远距离通信。隔离会破坏通信节点之间的接地回路，从而获得更大的共模电压范围。信号和电源路径均按照 UL1577 进行 $5kV_{RMS}$ 隔离，并符合 VDE、TUV、CSA 和 CQC 的增强型和基础型隔离要求。

ISOW14x2 通过将 V_{IO} 和 V_{DD} 一起连接到 PCB 上，可在 3V 至 5.5V 的单一电源下运行。如果需要较低的逻辑电平，1.71V 至 5.5V 逻辑电源 (V_{IO}) 可与 3V 至 5.5V 的电源转换器电源 (V_{DD}) 分开并相互独立。这些器件支持从 –40°C 到 +125°C 的宽工作环境温度范围，并采用 20 引脚 DFM (SOIC-20 尺寸兼容封装）提供至少 8 毫米的爬电距离和间隙。

6 Device Comparison Table

Part number	Isolation	Duplex	Data Rate	Package
ISOW1412/ISOW1412B	Reinforced/Basic	Full	500 kbps	20-DFM(SOIC)
ISOW1432/ISOW1432B	Reinforced/Basic	Full	12 Mbps	20-DFM(SOIC)

7 Pin Configuration and Functions

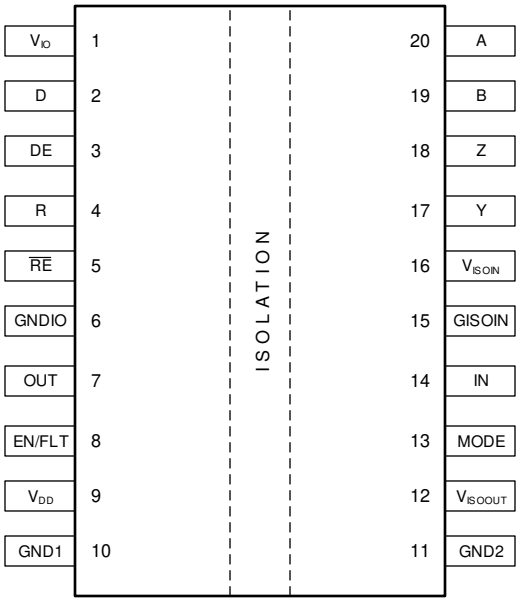


图 7-1. ISOW14x2 20-pin DFM Top View

表 7-1. Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
V_{IO}	1	--	Side 1 logic supply
D	2	I	Data input
DE	3	I	Driver enable. If pin is floating, driver is disabled (internal pull-down resistor)
R	4	O	Received data output
$\overline{RE}$	5	I	Receiver enable. If pin is floating, receiver buffer is disabled (internal pull-up resistor)
GNDIO	6	--	Ground connections for V_{IO} . GNDIO and GND1 need be shorted directly on PCB.
OUT	7	O	General purpose logic output
EN/FLT	8	I/O	Multi-function power converter enable input pin or fault output pin. Can only be used as either an input pin or an output pin. • If it's used as Power converter enable input pin, it enables and disables the integrated DC-DC power converter. Connect directly to microcontroller or through a series current limiting resistor to use as an enable input pin. DC-DC power converted is enabled when EN is high (connected to V_{IO}) and disabled when low (connected to GND1). If EN is floating, DC-DC converter is enabled (internal pull-up resistor) • If it's used as Fault output pin, it gives an alert signal if power converter is not operating properly. This pin is active low. Connect to microcontroller through a 5 kΩ or greater pull-up resistor in order to use as a fault outpin pin.
V_{DD}	9	--	Side 1 DC-DC converter power supply
GND1	10	--	Ground connection for V_{IO}. GNDIO and GND1 need be shorted directly on PCB.
GND2	11	--	Ground connection for V_{ISOOUT}. GND2 and GISOIN need be shorted direclty on PCB, or connected through a ferrite bead.
V_{ISOOUT}	12	--	Isolated power converter output voltage. V_{ISOOUT} and V_{ISOIN} need be shorted directly on PCB, or connected through a ferrite bead.
MODE	13	I	Mode select. For RS-485 transceiver to operate at 3.3V supply, connect MODE to GND2. For RS-485 transceiver to operate in 5V supply PROFIBUS mode, connect MODE to V_{ISOOUT} (internal pull-down resistor)
IN	14	I	General purpose logic input
GISOIN	15	--	Ground connections for V_{ISOIN}. GND2 and GISOIN need be shorted direclty on PCB, or connected through a ferrite bead.
V_{ISOIN}	16	--	Side 2 supply voltage for RS485. V_{ISOOUT} and V_{ISOIN} need be shorted directly on PCB, or connected through a ferrite bead.
Y	17	O	RS-485 driver non-inverting output
Z	18	O	RS-485 driver inverting output
B	19	I	RS-485 receiver inverting input
A	20	I	RS-485 receiver non-inverting input

8 Specifications

8.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1) (2)

		MIN	MAX	UNIT
V_{DD}	Power converter supply voltage	– 0.5	6	V
V_{ISOIN}	Isolated supply voltage, input supply for RS-485 transceiver	– 0.5	6	V
V_{ISOOUT}	Isolated supply voltage, Power converter output at RS485 mode (MODE = GND2)	– 0.5	4	V
V_{ISOOUT}	Isolated supply voltage, Power converter output at Profibus mode (MODE = V_{ISOOUT})	– 0.5	6	V
V_{IO}	Logic supply voltage	– 0.5	6	V
V_{BUS}	Voltage on bus pins (A, B, Y, Z with respect to GND2)	– 12	15	V
V_{LOGIC_IO}	Logic I/O voltage level (D, DE, $\overline{RE}$, R, EN, OUT)	– 0.5	V_{IO} + 0.5(3)	V
	IN	-0.5	V_{ISOIN} + 0.5	V
	MODE	-0.5	V_{ISOOUT} + 0.5	V
I_O	Output current on R and OUT pins	– 15	15	mA
T_J	Junction temperature	– 40	150	°C
T_{stg}	Storage temperature	– 65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Rating* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the deviceat these or any other conditions beyond those indicated under *Recommended Operating Condition*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) All voltage values except differential I/O bus voltages are with respect to the local ground pin (GND1 or GND2). All voltage values except differential I/O bus voltages are peak voltage values.

(3) The maximum voltage must not be greater than 6 V.

8.2 Recommended Operating Conditions

			MIN	NOM	MAX	UNIT
V_{IO}	Logic supply voltage	1.8-V operation	1.71		1.89	V
		2.5-V, 3.3-V, and 5-V operation	2.25		5.5	
V_{DD}	Power converter supply voltage		3		5.5	V
$V_{DD(UVLO+)}$	Positive threshold when power converter supply is rising			2.8	2.93	V
$V_{DD(UVLO-)}$	Positive threshold when power converter supply is falling		2.40	2.55		V
$V_{HYS1(UVLO)}$	Power converter supply voltage hysteresis		0.15	0.25		V
$V_{IO(UVLO+)}$	Rising threshold of logic supply voltage				1.7	V
$V_{IO(UVLO-)}$	Falling threshold of logic supply voltage		1			V
$V_{HYS2(UVLO)}$	Logic supply voltage hysteresis		75	125		mV
V_{BUS}	Input voltage at any bus terminal (seperately w.r.t GND2 or common mode)		–7		12	V
V_{IH}	High-level input voltage (D, DE, EN, and $\overline{RE}$ inputs)		0.7 × V_{IO}		V_{IO}	V
	High- level input voltage (IN input)		0.7 × V_{ISOIN}		V_{ISOIN}	V
V_{IL}	Low-level input voltage (D, DE, EN, and $\overline{RE}$ inputs)		0		0.3 × V_{IO}	V
	Low- level input voltage (IN input)		0		0.3 × V_{ISOIN}	V
V_{ID}	Differential input voltage (receiver terminals A w.r.t B)		–12		12	V
$I_{O(DRV)}$	Output current, driver (Y, Z)		–60		60	mA
I_O	Output current, R and OUT pins	V_{IO} = 4.5 to 5.5 V	–4		4	mA
		V_{IO} = 3 to 3.6 V	-2		2	mA
		V_{IO} = 2.25 to 2.75 V, 1.71 to 1.89 V	-1		1	mA
R_L	Differential load resistance on bus		54			Ω
$1/t_{UI}$	Signaling rate	ISOW1412			500	kbps
$1/t_{UI}$	Signaling rate	ISOW1432			12	Mbps
DR	Data rate for GPIO channel				2	Mbps
t_{pwrup}	Power up time after applying input supply(Isolated output supply reaches 90% of setpoint and data transmission can start after this)			5		ms
T_A	Ambient operating temperature (MODE= GND2), no extra current availalbe on V_{ISOUT} (1)		–40		125	°C
	Ambient operating temperature (MODE= GND2), 20 mA extra current available on V_{ISOUT} (1)		–40		105	°C
	Ambient operating temperature (MODE= V_{ISOOUT}), 50% duty cycle on DE, no extra current available on V_{ISOUT} (1)		–40		125	°C
	Ambient operating temperature (MODE= V_{ISOOUT}), no extra current available on V_{ISOUT} (1)		–40		105	°C
	Ambient operating temperature (MODE= V_{ISOOUT}), 20 mA extra current available on V_{ISOUT} (1)		–40		85	°C

(1) Extra current is only available at VDD=5 V ± 10% mode

8.3 Thermal Information

THERMAL METRIC(1)		ISOW14x2 DFM 20 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	68.5	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	20.9	°C/W

THERMAL METRIC(1)		ISOW14x2 DFM 20 PINS	UNIT
$R_{\theta JB}$	Junction-to-board thermal resistance	44.8	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	13	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	44	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	--	°C/W

(1) For more informationabout traditional and new thermal metrics, see the*Semiconductor andIC Package Thermal Metrics* application report.

8.4 Power Ratings

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
P_D	Maximum power dissipation (both sides)	V_{DD} = V_{IO} = 5.5V, MODE = V_{ISOOUT}, T_J = 150°C, Y-Z load = 54Ω||50pF, Y shorted to A, Z shorted to B(loopback), Load on R = 15pF, Input a 250kHz 50% duty cycle square wave to D pin with V_{DE} = V_{IO}, V_{RE} = GND1, ISOW1412			1060	mW
P_{D1}	Maximum power dissipation (side-1)				490	mW
P_{D2}	Maximum power dissipation by (side-2)				570	mW
P_D	Maximum power dissipation (both sides)	V_{DD}= V_{IO}= 5.5V, MODE= V_{ISOOUT}, T_J=150°C, Y-Z load= 54Ω||50pF, Y shorted to A, Z shorted to B(loopback), Load on R=15pF, Input a 6MHz 50% duty cycle square wave to D pin with V_{DE}=V_{IO}, V_{RE}=GND1, ISOW1432			1110	mW
P_{D1}	Maximum power dissipation (side-1)				510	mW
P_{D2}	Maximum power dissipation by (side-2)				610	mW

8.5 Insulation Specifications

PARAMETER		TEST CONDITIONS	VALUE	UNIT
GENERAL				
CLR	External clearance(1)	Shortest terminal-to-terminal distance through air	> 8	mm
CPG	External creepage(1)	Shortest terminal-to-terminal distance across the package surface	> 8	mm
DTI	Distance through the insulation	Minimum internal gap (internal clearance – capacitive signal isolation)	> 17	um
		Minimum internal gap (internal clearance- transformer power isolation)	> 120	
CTI	Comparative tracking index	DIN EN 60112 (VDE 0303-11); IEC 60112	> 600	V
	Material group	According to IEC 60664-1	I	
	Overvoltage category per IEC 60664-1	Rated mains voltage ⩽ 150 V_{RMS}	I-IV	
		Rated mains voltage ⩽ 300 V_{RMS}	I-IV	
		Rated mains voltage ⩽ 600 V_{RMS}	I-IV	
		Rated mains voltage ⩽ 1000 V_{RMS}	I-III	
DIN VDE V 0884-11:2017-01(2)				
V_{IORM}	Maximum repetitive peak isolation voltage	AC voltage (bipolar)	1500	V_{PK}
V_{IOWM}	Maximum working isolation voltage	AC voltage (sine wave) Time dependent dielectric breakdown (TDDB) test	1000	V_{RMS}
		DC voltage	1500	V_{DC}
V_{IOTM}	Maximum transient isolation voltage	$V_{TEST} = V_{IOTM}$, t = 60 s (qualification); $V_{TEST} = 1.2 \times V_{IOTM}$, t = 1 s (100% production)	7071	V_{PK}
V_{IOSM}	Maximum surge isolation voltage ISOW14x2(3)	Test method per IEC 62368-1, 1.2/50 µs waveform, $V_{TEST} = 1.6 \times V_{IOSM} = 10\ kV_{PK}$ (qualification)	6250	V_{PK}
V_{IOSM}	Maximum surge isolation voltage ISOW14x2B(3)	Test method per IEC 62368-1, 1.2/50 µs waveform, $V_{TEST} = 1.3 \times V_{IOSM} = 7.8\ kV_{PK}$ (qualification)	6000	V_{PK}
q_{pd}	Apparent charge(4)	Method a: After I/O safety test subgroup 2/3, $V_{ini} = V_{IOTM}$, t_{ini} = 60 s; $V_{pd(m)} = 1.2 \times V_{IORM}$, t_m = 10 s	⩽ 5	pC
		Method a: After environmental tests subgroup 1, $V_{ini} = V_{IOTM}$, t_{ini} = 60 s; ISOW14x2: $V_{pd(m)} = 1.6 \times V_{IORM}$, t_m = 10 s. ISOW14x2B: $V_{pd(m)} = 1.2 \times V_{IORM}$, t_m = 10 s	⩽ 5	
		Method b1: At routine test (100% production) and preconditioning (type test) $V_{ini} = 1.2 \times V_{IOTM}$, t_{ini} = 1 s; ISOW14x2: $V_{pd(m)} = 1.875 \times V_{IORM}$, t_m = 1 s. ISOW14x2B: $V_{pd(m)} = 1.5 \times V_{IORM}$, t_m = 1 s	⩽ 5	
C_{IO}	Barrier capacitance, input to output(5)	V_{IO} = 0.4 sin (2 π ft), f = 1 MHz	~3.5	pF
R_{IO}	Isolation resistance, input to output(5)	V_{IO} = 500 V, T_A = 25°C	> 10^{12}	Ω
		V_{IO} = 500 V, 100°C ⩽ T_A ⩽ 125°C	> 10^{11}	Ω
		V_{IO} = 500 V at T_S = 150°C	> 10^{9}	Ω
	Pollution degree		2	
	Climatic category		40/125/21	
UL 1577				
V_{ISO}	Withstand isolation voltage	$V_{TEST} = V_{ISO}$ = 5000 V_{RMS}, t = 60 s (qualification); $V_{TEST} = 1.2 \times V_{ISO}$ = 6000 V_{RMS}, t = 1 s (100% production)	5000	V_{RMS}

(1) Creepage and clearance requirements should be applied according to the specific equipment isolation standards of an application. Care should be taken to maintain the creepage and clearance distance of a board design to ensure that the mounting pads of the isolator on the printed-circuit board do not reduce this distance. Creepage and clearance on a printed-circuit board become equal in certain cases. Techniques such as inserting grooves and/or ribs on a printed circuit board are used to help increase these specifications.
(2) ISOW14x2 is suitable for *safe electrical insulation* and ISOW14x2B is suitable for *basic electrical insulation* only within the safety ratings.. Compliance with the safety ratings shall be ensured by means of suitable protective circuits.
(3) Testing is carried out in air or oil to determine the intrinsic surge immunity of the isolation barrier.
(4) Apparent charge is electrical discharge caused by a partial discharge (pd).
(5) All pins on each side of the barrier tied together creating a two-terminal device

8.6 Safety-Related Certifications

VDE	CSA	UL	TUV	CQC
Certified according to DIN VDE V 0884-11 :2017-01	Certified according to IEC 62368-1, IEC 61010-1 and IEC 60601-1	Certified under UL 1577 Component Recognition Program	Certified ccording to EN 61010-1:2010/ A1:2019 and EN 62368-1:2014	Plan to certify according to GB4943.1-2011
Maximum transient isolation voltage 7071 V_{PK}; Maximum repetitive peak isolation voltage, 1500 V_{PK}; Maximum surge isolation voltage, ISOW14x2: 6250 V_{PK} (Reinforced), ISOW14x2B: 6000 V_{PK} (Basic)	Per CSA62368-1:19, IEC 62368-1:2018 Ed. 3, CSA 61010-1-12+A1 and IEC 61010-1 3rd Ed., ISOW14x2 (Reinforced): 600 V_{RMS}, ISOW14x2B (Basic): 1000 V_{RMS} maximum working voltage (pollution degree 2, material group I, ambient temperature 90 ℃), 2 MOPP (Means of Patient Protection) per CSA 60601-1:14 . IEC 60601-1 (ISOW14x2 only) Ed.3+A1, 250 V_{RMS} maximum working voltage	Single protection, 5000 V_{RMS}	ISOW14x2 (Reinforced): 5000 V_{RMS} reinforced insulation per EN 61010-1:2010/A1:2019 and EN 62368-1:2014 up to working voltage of 600 V_{RMS} . ISOW14x2B (Basic): 1000 V_{RMS}	Reinforced insulation, Altitude ≤ 5000 m, Tropical Climate, 700 V_{RMS} maximum working voltage.
Certification number: 40040142. ISOW1432 planned	Master Contract Number: 220991. ISOW1432 planned	File number: E181974. ISOW1432 planned	Client ID number: 77311. ISOW1432 planned	Certificate number: CQC21001297517. ISOW1432 planned

8.7 Safety Limiting Values

Safety limiting intends to minimize potential damage to the isolation barrier upon failure of input or output circuitry.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_S	Safety input, output, or supply current(1)	$R_{\theta JA}$ = 68.5°C/W, V_I = 5.5 V, T_J = 150°C, T_A = 25°C , See 图 8-1			332	mA
		$R_{\theta JA}$ = 68.5°C/W, V_I = 3.6 V, T_J = 150°C, T_A = 25°C , See 图 8-1			507	
P_S	Safety input, output, or total power(1)	$R_{\theta JA}$ = 68.5°C/W, T_J = 150°C, T_A = 25°C , See 图 8-2			1826	mW
T_S	Safety temperature(1)				150	°C

(1) The maximum safety temperature,T_S, has the same value as the maximum junction temperature,T_J, specified for the device. The I_S and P_S parameters represent the safety current and safety power respectively.The maximum limits of I_S and P_S should not beexceeded. These limits vary with the ambient temperature, T_A.
The junction-to-air thermal resistance, $R_{\theta JA}$, in the *Thermal Information* table is that of a device installed on a high-K test board forleaded surface-mount packages. Use these equations to calculate the value for each parameter:
$T_J = T_A + R_{\theta JA} \times P$, where P is the power dissipated in the device.
$T_{J(max)} = T_S = T_A + R_{\theta JA} \times P_S$, where $T_{J(max)}$ is the maximum allowed junction temperature.
$P_S = I_S \times V_I$, where V_I is the maximum input voltage.

8.8 Electrical Characteristics

Over recommended operating conditions, typical values are at V_{DD} = V_{IO} = 3.3 V and T_A =25°C, GND1 = GNDIO, GND2 = GISOIN (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Device						
V_{ISOOUT}	Isolated output supply voltage	MODE=GND2, DE=GND1, D, $\overline{RE}$ and IN floating	3.135	3.3V	3.465	V
	Isolated output supply voltage	MODE=V_{ISOOUT}, DE=GND1, D, $\overline{RE}$ and IN floating	4.75	5	5.25	V
V_{OH}	Output high voltage on OUT pin	V_{IO} = 5 V ± 10%, I_{OH} = – 4 mA, IN=V_{ISOIN}	V_{IO} – 0.4			V
	Output high voltage on OUT pin	V_{IO} = 3.3 V ± 10% , I_{OH} = – 2 mA, IN=V_{ISOIN}	V_{IO} – 0.3			V
	Output high voltage on OUT pin	V_{IO} = 2.5 V ± 10% , I_{OH} = – 1 mA, IN=V_{ISOIN}	V_{IO} – 0.2			V
	Output high voltage on OUT pin	V_{IO} = 1.8 V ± 5%, I_{OH} = – 1 mA, IN=V_{ISOIN}	V_{IO} – 0.2			V
V_{OL}	Output low voltage on OUT pin	V_{IO} = 5 V ± 10%, I_{OL} = 4 mA, IN=GND2			0.4	V
	Output low voltage on OUT pin	V_{IO} = 3.3 V ± 10% , I_{OL} = 2 mA, IN=GND2			0.3	V
	Output low voltage on OUT pin	V_{IO} = 2.5 V ± 10%, I_{OL} = 1 mA, IN=GND2			0.2	V
	Output low voltage on OUT pin	V_{IO} = 1.8 V ± 5%, I_{OL} = 1 mA, IN=GND2			0.2	V
I_I	Input current, IN	IN at 0 V or V_{ISOIN}	– 25		25	µA
I_I	Input current, EN	EN at 0 V or V_{IO}	– 25		25	µA
$\|CM_H\|$	High-level common-mode transient immunity	Driver and receiver path, V_{CM} = 1000 V, see 图 9-4		100		kV/µs
$\|CM_L\|$	Low-level common-mode transient immunity	Driver and receiver path, V_{CM} = 1000 V, see 图 9-4		100		kV/µs
Driver						
$\|V_{OD}\|$	Differential output voltage magnitude	Unloaded bus, V_{DD} = 3 V to 3.6 V with MODE=GND2, or 4.5 V to 5.5 V with MODE= V_{ISOOUT}	1.5		V_{ISOIN}	V
		R_L = 60 Ω, – 7 V ≤ V_{TEST} ≤ 12 V (see 图 9-1), V_{DD} = 3 V to 3.6 V, MODE = GND2	1.5		V_{ISOIN}	
		R_L = 100 Ω (see 图 9-2) (RS-422 load), V_{DD} = 3 V to 3.6 V, MODE = GND2	2		V_{ISOIN}	
		R_L = 54 Ω (see 图 9-2) (RS-485 load), V_{DD} = 3 V to 3.6 V, MODE = GND2	1.5		V_{ISOIN}	
$\|V_{OD}\|$	Differential output voltage magnitude	R_L = 54 Ω, V_{DD} = 4.5 V to 5.5 V, MODE = V_{ISOOUT} , see 图 9-2	2.1		V_{ISOIN}	V
$\|V_{OD}\|$	Differential output voltage magnitude	R_L = 100 Ω (see 图 9-2) (RS-422 load), V_{DD} = 4.5 V to 5.5 V, MODE = V_{ISOOUT}	2.1		V_{ISOIN}	V
$\|V_{OD}\|$	Differential output voltage magnitude	R_L = 60 Ω, – 7 V ≤ V_{TEST} ≤ 12 V (see 图 9-1), VDD = 4.5 V to 5.5V, MODE = V_{ISOOUT}	2.1		V_{ISOIN}	V
$\Delta\|V_{OD}\|$	Change in differential output voltage between the two states	R_L = 54 Ω or 100 Ω (see 图 9-2)	– 200		200	mV
V_{OC}	Common-mode output voltage	R_L = 54 Ω or 100 Ω (see 图 9-2)	1	0.5 × V_{ISOIN}	3	V
$\Delta V_{OC(SS)}$	Change in steady-state common-mode output voltage between the two states	R_L = 54 Ω or 100 Ω (see 图 9-2)	– 200		200	mV
$V_{OC(PP)}$	Peak-to-peak common mode output voltage	R_L = 54 Ω or 100 Ω, V_{ISOIN}=V_{ISOOUT}=3.3V, see 图 9-2		400		mV
I_{OS}	Short-circuit output current	V_{DE} = V_{IO}, V_D=V_{IO} or GND1, – 7 V ≤ Y or Z ≤ 12 V, or Y shorted to Z, see 图 9-10		180		mA

Over recommended operating conditions, typical values are at V_{DD} = V_{IO} = 3.3 V and T_A =25°C, GND1 = GNDIO, GND2 = GISOIN (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_I	Input current , D, DE	V_D, V_{DE} at 0 V or V_{IO}	–25		25	µA
Receiver						
I_{I1}	Bus input current	V_{DE} = 0 V, V_{ISOIN} = 0 V or 3.3 V or 5V, ISOW1412 or ISOW1432, V_A or V_B = –7 V to 12 V, other input at 0 V	–100		125	µA
V_{TH+}	Positive-going input-threshold voltage	–7 V ≤ V_{CM} ≤ 12 V	See(1)	–78	–20	mV
V_{TH-}	Negative-going input-threshold voltage	–7 V ≤ V_{CM} ≤ 12 V	–200	–141	See(1)	mV
V_{hys}	Input hysteresis (V_{TH+} – V_{TH-})	–7 V ≤ V_{CM} ≤ 12 V	40	63		mV
V_{OH}	Output high voltage on R pin	V_{IO} = 5 V ± 10%, I_{OH} = –4 mA, V_{ID} ≥ 200 mV	V_{IO} – 0.4			V
		V_{IO} = 3.3 V ± 10%, I_{OH} = –2 mA, V_{ID} ≥ 200 mV	V_{IO} – 0.3			
		V_{IO} = 2.5 V ± 10% , I_{OH} = –1 mA, V_{ID} ≥ 200 mV	V_{IO} – 0.2			
		V_{IO} = 1.8 V ± 5%, I_{OH} = –1 mA, V_{ID} ≥ 200 mV	V_{IO} – 0.2			
V_{OL}	Output low voltage on R pin	V_{IO} = 5 V ± 10%, I_{OL} = 4 mA, V_{ID} ≤ –200 mV			0.4	V
		V_{IO} = 3.3 V ± 10%, I_{OL} = 2 mA, V_{ID} ≤ –200 mV			0.3	
		V_{IO} = 2.5 V ± 10% , I_{OL} = 1 mA, V_{ID} ≤ –200 mV			0.2	
		V_{IO} = 1.8 V ± 5%, I_{OL} = 1 mA, V_{ID} ≤ –200 mV			0.2	
I_{OZ}	Output high-impedance current on R pin	V_R = 0 V or V_{IO}, $V_{\overline{RE}}$ = V_{IO}	–1		1	µA
$I_{I(RE)}$	Input current on $\overline{RE}$ pin	$V_{\overline{RE}}$ at 0 V or V_{IO}	–25		25	µA

(1) The V_{TH+} voltage is specified to be greater than the V_{TH-} voltage by at least the V_{hys} voltage under any specific conditions.

8.9 Supply Current Characteristics at V_{ISOOUT} = 3.3 V

over recommended operating conditions, V_{DD} = V_{IO} = 3 to 5.5 V, MODE=GND2, GND1 = GNDIO, GND2 = GISOIN (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Power converter disabled						
I_{DD}	Power converter supply current	EN=GND1, D, DE, $\overline{RE}$ floating		0.23	0.45	mA
I_{IO}	Logic supply current	EN=GND1, D, DE, $\overline{RE}$ floating		0.24	0.55	mA
Power converter supply current: Driver enabled, receiver disabled						
I_{DD}	Power converter supply current	V_{DE} = V_{IO}, $V_{\overline{RE}}$ = V_{IO}, bus load = 120 Ω, V_D= V_{IO}, V_{DD} = 5 V ± 10%, A and B floating		56	77	mA
		V_{DE} = V_{IO}, $V_{\overline{RE}}$ = V_{IO}, bus load = 120 Ω, V_D= V_{IO}, V_{DD} = 3.3 V ± 10%, A and B floating		69	109	mA
I_{DD}	Power converter supply current, ISOW1412	V_{DE} = V_{IO}, $V_{\overline{RE}}$ = V_{IO}, bus load = 120 Ω || 50 pF, D = 500-kbps square wave 50% duty, V_{DD} = 5 V ± 10%		62	86	mA
		V_{DE} = V_{IO}, $V_{\overline{RE}}$ = V_{IO}, bus load = 100 Ω || 50 pF, D = 500-kbps square wave 50% duty, V_{DD} = 5 V ± 10%		69	88	mA
		V_{DE} = V_{IO}, $V_{\overline{RE}}$ = V_{IO}, bus load = 54 Ω || 50 pF, D = 500-kbps square wave 50% duty, V_{DD} = 5 V ± 10%		90	122	mA
		V_{DE} = V_{IO}, $V_{\overline{RE}}$ = V_{IO}, bus load = 120 Ω || 50 pF, D = 500-kbps square wave 50% duty, V_{DD} = 3.3 V ± 10%		76	131	mA
		V_{DE} = V_{IO}, $V_{\overline{RE}}$ = V_{IO}, bus load = 100 Ω || 50 pF, D = 500-kbps square wave 50% duty, V_{DD} = 3.3 V ± 10%		84	131	mA
		V_{DE} = V_{IO}, $V_{\overline{RE}}$ = V_{IO}, bus load = 54 Ω || 50 pF, D = 500-kbps square wave 50% duty, V_{DD} = 3.3 V ± 10%		111	158	mA
I_{DD}	Power converter supply current, ISOW1432	V_{DE} = V_{IO}, $V_{\overline{RE}}$ = V_{IO}, bus load = 120 Ω || 50 pF, D = 12-Mbps square wave 50% duty, V_{DD} = 5 V ± 10%		64	87	mA
		V_{DE} = V_{IO}, $V_{\overline{RE}}$ = V_{IO}, bus load = 100 Ω || 50 pF, D = 12-Mbps square wave 50% duty, V_{DD} = 5 V ± 10%		69	94	mA
		V_{DE} = V_{IO}, $V_{\overline{RE}}$ = V_{IO}, bus load = 54 Ω || 50 pF, D = 12-Mbps square wave 50% duty, V_{DD} = 5 V ± 10%		90	117	mA
		V_{DE}= V_{IO}, $V_{\overline{RE}}$ = V_{IO}, bus load = 120 Ω || 50 pF, D = 12-Mbps square wave 50% duty, V_{DD} = 3.3 V ± 10%		79	129	mA
		V_{DE}= V_{IO}, $V_{\overline{RE}}$ = V_{IO}, bus load = 100 Ω || 50 pF, D = 12-Mbps square wave 50% duty, V_{DD} = 3.3 V ± 10%		84	135	mA
		V_{DE} = V_{IO}, $V_{\overline{RE}}$ = V_{IO}, bus load = 54 Ω || 50 pF, D = 12-Mbps square wave 50% duty, V_{DD} = 3.3 V ± 10%		113	156	mA
Power converter supply current: Driver disabled, receiver enabled						
I_{DD}	Power converter supply current, ISOW1412	V_{DE} = V_{GND1}, $V_{\overline{RE}}$= V_{GND1}, Y and Z bus loaded and unloaded, A-B = square wave 500-kbps 50% duty V_D= V_{GND1}, V_{DD} = 5 V ± 10%, C_L on R = 15 pF		16	28	mA
		V_{DE} = V_{GND1}, $V_{\overline{RE}}$= V_{GND1}, Y and Z bus loaded and unloaded, A-B = square wave 500-kbps 50% duty V_D= V_{GND1}, V_{DD} = 3.3 V ± 10%, C_L on R = 15 pF		18	30	
I_{DD}	Power converter supply current, ISOW1432	V_{DE} = V_{GND1}, $V_{\overline{RE}}$= V_{GND1}, Y and Z bus loaded and unloaded, A-B = square wave 12-Mbps 50% duty V_D= V_{GND1}, V_{DD} = 5 V ± 10%, C_L on R = 15 pF		15	24	mA
		V_{DE} = V_{GND1}, $V_{\overline{RE}}$= V_{GND1}, Y and Z bus loaded and unloaded, A-B = square wave 12-Mbps 50% duty V_D= V_{GND1}, V_{DD} = 3.3 V ± 10%, C_L on R = 15 pF		17	27	
Power converter supply current: Driver enabled, receiver enabled						

over recommended operating conditions, V_{DD} = V_{IO} = 3 to 5.5 V, MODE=GND2, GND1 = GNDIO, GND2 = GISOIN (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{DD}	Power converter supply current, ISOW1412	V_{DE} = V_{IO}, $V_{\overline{RE}}$= V_{GND1}, Y and Z bus load = 120 Ω || 50 pF, loopback(1), D = 500-kbps 50% duty, V_{DD} = 5 V ± 10%, C_L on R = 15 pF		63	102	mA
		V_{DE} = V_{IO}, $V_{\overline{RE}}$= V_{GND1}, Y and Z bus load = 120 Ω || 50 pF, loopback(1), D = 500-kbps 50% duty, V_{DD} = 3.3 V ± 10%, C_L on R = 15 pF		77	129	
I_{DD}	Power converter supply current, ISOW1432	V_{DE} = V_{IO}, $V_{\overline{RE}}$= V_{GND1}, Y and Z bus load = 120 Ω || 50 pF, loopback(1), D = 12-Mbps 50% duty, V_{DD} = 5 V ± 10%, C_L on R = 15 pF		66	91	mA
		V_{DE} = V_{IO}, $V_{\overline{RE}}$= V_{GND1}, Y and Z bus load = 120 Ω || 50 pF, loopback(1), D = 12-Mbps 50% duty, V_{DD} = 3.3 V ± 10%, C_L on R = 15 pF		84	136	
Logic supply current: Driver disabled, receiver disabled						
I_{IO}	Logic supply current	V_{DE} = V_{GND1}, $V_{\overline{RE}}$ = V_{IO} , V_D = V_{IO}, V_{IO}= 3.3 V ± 10%		3.2	6.0	mA
Logic supply current: Driver enabled, Receiver enabled, static						
I_{IO}	Logic supply current	V_{DE} = V_{IO}, $V_{\overline{RE}}$= V_{GND1}, V_D = V_{IO}, loopback(1), V_{IO}= 3.3 V ± 10%		4	6.8	mA
Logic supply current: Driver enabled, receiver enabled, dynamic						
I_{IO}	Logic supply current, ISOW1412	V_{DE} = V_{IO}, $V_{\overline{RE}}$= V_{GND1}, D = 500-kbps 50% duty square wave, loopback(1), V_{IO} = 3.3 V ± 10%		4.6	7.2	mA
I_{IO}	Logic supply current, ISOW1432	V_{DE} = V_{IO}, $V_{\overline{RE}}$ = V_{GND1} , D = 12-Mbps 50% duty square wave, loopback(1), V_{IO} = 3.3 V ± 10%		4.6	7.2	mA

(1) The output of the driver is connected to the input of a receiverin a loopback mode.

8.10 Supply Current Characteristics at V_{ISOOUT} = 5 V

over recommended operating conditions, V_{DD} = V_{IO} = 4.5 V to 5.5 V, MODE=V_{ISOOUT} , GND1 = GNDIO, GND2 = GISOIN (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Power converter disabled						
I_{DD}	Power converter supply current	EN=GND1, D, DE, $\overline{RE}$ floating		0.23	0.45	mA
I_{IO}	Logic supply current	EN=GND1, D, DE, $\overline{RE}$ floating		0.24	0.55	mA
Power converter supply current: Driver enabled, receiver disabled						
I_{DD}	Power converter supply current	V_{DE} = V_{IO}, $V_{\overline{RE}}$ = V_{IO}, bus load = 120 Ω , V_D= V_{IO}, V_{DD} = 5 V ± 10%, A and B floating		97	160	mA
I_{DD}	Power converter supply current, ISOW1412	V_{DE} = V_{IO}, $V_{\overline{RE}}$ = V_{IO}, bus load = 120 Ω || 50 pF, D = 500-kbps square wave 50% duty, V_{DD} = 5 V ± 10%		123	205	mA
		V_{DE} = V_{IO}, $V_{\overline{RE}}$ = V_{IO}, bus load = 54 Ω || 50 pF, D = 500-kbps square wave 50% duty, V_{DD} = 5 V ± 10%		175	292	mA
I_{DD}	Power converter supply current, ISOW1432	V_{DE} = V_{IO}, $V_{\overline{RE}}$ = V_{IO}, bus load = 120 Ω || 50 pF, D = 12-Mbps square wave 50% duty, V_{DD} = 5 V ± 10%		77	108	mA
		V_{DE} = V_{IO}, $V_{\overline{RE}}$ = V_{IO}, bus load = 54 Ω || 50 pF, D = 12-Mbps square wave 50% duty, V_{DD} = 5 V ± 10%		164	214	mA
Power converter supply current: Driver disabled, receiver enabled						
I_{DD}	Power converter supply current	V_{DE}= V_{GND1}, $V_{\overline{RE}}$= V_{GND1}, Y and Z bus loaded and unloaded, A-B = square wave 500-kbps 50% duty V_D= V_{IO}, V_{DD}= 5 V ± 10%, C_L on R = 15 pF		17	31	mA
I_{DD}	Power converter supply current	V_{DE}= V_{GND1}, $V_{\overline{RE}}$= V_{GND1}, Y and Z bus loaded and unloaded, A-B = square wave 12-Mbps 50% duty (ISOW1432) V_D= V_{IO}, V_{DD}= 5 V ± 10%, C_L on R = 15 pF		19	26	mA
Power converter supply current: Driver enabled, receiver enabled						
I_{DD}	Power converter supply current, ISOW1412	V_{DE} = V_{IO}, $V_{\overline{RE}}$= V_{GND1}, Y and Z bus load = 120 Ω || 50 pF, loopback(1), D = 500-kbps 50% duty, V_{DD} = 5 V ± 10%, C_L on R = 15 pF		123	207	mA
I_{DD}	Power converter supply current, ISOW1432	V_{DE} = V_{IO}, $V_{\overline{RE}}$= V_{GND1}, Y and Z bus load = 120 Ω || 50 pF, loopback(1), D = 12-Mbps 50% duty, V_{DD} = 5 V ± 10%, C_L on R = 15 pF		112	135	mA

(1) The output of the driver is connected to the input of a receiverin a loopback mode.

8.11 Switching Characteristics at V_{ISOOUT} = 3.3 V

Min / Max specifications are over recommended operating conditions, typical values are at V_{DD} = V_{IO} = 3.3 V, MODE=GND2 (V_{ISOOUT}= 3.3V), GND1 = GNDIO, GND2 = GISOIN, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Driver: 500-kbps device (ISOW1412)						
t_r, t_f	Differential output rise time and fall time	R_L = 54 Ω, C_L = 50 pF, see 图 9-3	190	300	600	ns
t_{PHL}, t_{PLH}	Propagation delay	R_L = 54 Ω, C_L = 50 pF, see 图 9-3		450	610	ns
PWD	Pulse width distortion(1), $\lvert t_{PHL} - t_{PLH} \rvert$	R_L = 54 Ω, C_L = 50 pF, see 图 9-3		3	40	ns
t_{PHZ}, t_{PLZ}	Disable time	See 图 9-5 and 图 9-6		56	200	ns
t_{PZH}, t_{PZL}	Enable time	See 图 9-5 and 图 9-6		280	600	ns
Receiver: 500-kbps device (ISOW1412)						
t_r, t_f	Output rise time and fall time	C_L = 15 pF, see 图 9-7			4	ns
t_{PHL}, t_{PLH}	Propagation delay	C_L = 15 pF, see 图 9-7		60	135	ns
PWD	Pulse width distortion(1), $\lvert t_{PHL} - t_{PLH} \rvert$	C_L = 15 pF, see 图 9-7		2	15	ns
t_{PHZ}, t_{PLZ}	Disable time	See 图 9-8 and 图 9-9		9	30	ns
t_{PZH}, t_{PZL}	Enable time	See 图 9-8 and 图 9-9		8	30	ns
Driver: 12-Mbps device (ISOW1432)						
t_r, t_f	Differential output rise time and fall time	R_L = 54 Ω, C_L = 50 pF, see 图 9-3	6	15	25	ns
t_{PHL}	Propagation delay	R_L = 54 Ω, C_L = 50 pF, see 图 9-3		49	125	ns
t_{PLH}	Propagation delay	R_L = 54 Ω, C_L = 50 pF, see 图 9-3		49	125	ns
t_{PHL}, t_{PLH}	Propagation delay	R_L = 54 Ω, C_L = 50 pF, see 图 9-3		52	125	ns
PWD	Pulse width distortion(1), $\lvert t_{PHL} - t_{PLH} \rvert$	R_L = 54 Ω, C_L = 50 pF, see 图 9-3		1	10	ns
t_{PHZ}	Disable time	See 图 9-5 and 图 9-6		35	125	ns
t_{PLZ}	Disable time	See 图 9-5 and 图 9-6		35	125	ns
t_{PHZ}, t_{PLZ}	Disable time	See 图 9-5 and 图 9-6		36	125	ns
t_{PZH}	Enable time	See 图 9-5 and 图 9-6		46	150	ns
t_{PZL}	Enable time	See 图 9-5 and 图 9-6		36	150	ns
t_{PZH}, t_{PZL}	Enable time	See 图 9-5 and 图 9-6		48	150	ns

Min / Max specifications are over recommended operating conditions, typical values are at V_{DD} = V_{IO} = 3.3 V, MODE=GND2 (V_{ISOOUT}= 3.3V), GND1 = GNDIO, GND2 = GISOIN, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Receiver: 12-Mbps device (ISOW1432)						
t_r, t_f	Output rise time and fall time	C_L = 15 pF, see 图 9-7			4	ns
t_{PHL}	Propagation delay	C_L = 15 pF, see 图 9-7		59	120	ns
t_{PLH}	Propagation delay	C_L = 15 pF, see 图 9-7		59	120	ns
t_{PHL}, t_{PLH}	Propagation delay	C_L = 15 pF, see 图 9-7		42	120	ns
PWD	Pulse width distortion(1), $\lvert t_{PHL} - t_{PLH} \rvert$	C_L = 15 pF, see 图 9-7		1.7	10	ns
t_{PHZ}	Disable time	See 图 9-8 and 图 9-9		7	30	ns
t_{PLZ}	Disable time	See 图 9-8 and 图 9-9		6	30	ns
t_{PHZ}, t_{PLZ}	Disable time	See 图 9-8 and 图 9-9		9	30	ns
t_{PZH}	Enable time	See 图 9-8 and 图 9-9		6	30	ns
t_{PZL}	Enable time	See 图 9-8 and 图 9-9		5	30	ns
t_{PZH}, t_{PZL}	Enable time	See 图 9-8 and 图 9-9		8	30	ns
GPIO channel						
t_{PHL}, t_{PLH}	Propagation delay time	See 图 9-11		227	347	ns
PWD	Pulse width distortion, $\lvert t_{PHL} - t_{PLH} \rvert$			20	110	ns
t_r	Output signal rise time			1	4	ns
t_f	Output signal fall time			1	4	ns

(1) Also known as pulse skew.

8.12 Switching Characteristics at V_{ISOOUT} = 5 V

Min / Max specifications are over recommended operating conditions, typical values are at V_{DD} = V_{IO} = 5 V, MODE=V_{ISOOUT} (V_{ISOOUT}= 5 V), GND1 = GNDIO, GND2 = GISOIN, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Driver: 500-kbps device (ISOW1412)						
t_r, t_f	Differential output rise time and fall time	R_L = 54 Ω, C_L = 50 pF, see 图 9-3	200	300	600	ns
t_{PHL}, t_{PLH}	Propagation delay	R_L = 54 Ω, C_L = 50 pF, see 图 9-3		400	610	ns
PWD	Pulse width distortion(1), $\lvert t_{PHL} - t_{PLH} \rvert$	R_L = 54 Ω, C_L = 50 pF, see 图 9-3		2	40	ns
t_{PHZ}, t_{PLZ}	Disable time	See 图 9-5 and 图 9-6		30	200	ns
t_{PZH}, t_{PZL}	Enable time	See 图 9-5 and 图 9-6		115	600	ns
Receiver: 500-kbps device (ISOW1412)						
t_r, t_f	Output rise time and fall time	C_L = 15 pF, see 图 9-7			4	ns
t_{PHL}, t_{PLH}	Propagation delay	C_L = 15 pF, see 图 9-7		49	135	ns
PWD	Pulse width distortion(1), $\lvert t_{PHL} - t_{PLH} \rvert$	C_L = 15 pF, see 图 9-7		2	20	ns
t_{PHZ}, t_{PLZ}	Disable time	See 图 9-8 and 图 9-9		8	30	ns
t_{PZH}, t_{PZL}	Enable time	See 图 9-8 and 图 9-9		7	30	ns
Driver: 12-Mbps device (ISOW1432)						
t_r, t_f	Differential output rise time and fall time	R_L = 54 Ω, C_L = 50 pF, see 图 9-3	7	15	25	ns
t_{PHL}	Propagation delay	R_L = 54 Ω, C_L = 50 pF, see 图 9-3		40	125	ns
t_{PLH}	Propagation delay	R_L = 54 Ω, C_L = 50 pF, see 图 9-3		40	125	ns
t_{PHL}, t_{PLH}	Propagation delay	R_L = 54 Ω, C_L = 50 pF, see 图 9-3		40	125	ns
PWD	Pulse width distortion(1), $\lvert t_{PHL} - t_{PLH} \rvert$	R_L = 54 Ω, C_L = 50 pF, see 图 9-3		2	10	ns
t_{PHZ}	Disable time	See 图 9-5 and 图 9-6		30	125	ns
t_{PLZ}	Disable time	See 图 9-5 and 图 9-6		30	125	ns
t_{PHZ}, t_{PLZ}	Disable time	See 图 9-5 and 图 9-6		28	125	ns
t_{PZH}	Enable time	See 图 9-5 and 图 9-6		34	150	ns
t_{PZL}	Enable time	See 图 9-5 and 图 9-6		25	150	ns
t_{PZH}, t_{PZL}	Enable time	See 图 9-5 and 图 9-6		33	150	ns
Receiver: 12-Mbps device (ISOW1432)						
t_r, t_f	Output rise time and fall time	C_L = 15 pF, see 图 9-7			6	ns
t_{PHL}	Propagation delay	C_L = 15 pF, see 图 9-7		55	120	ns
t_{PLH}	Propagation delay	C_L = 15 pF, see 图 9-7		55	120	ns
t_{PHL}, t_{PLH}	Propagation delay	C_L = 15 pF, see 图 9-7		52	120	ns
PWD	Pulse width distortion(1), $\lvert t_{PHL} - t_{PLH} \rvert$	C_L = 15 pF, see 图 9-7		2.5	10	ns
t_{PHZ}	Disable time	See 图 9-8 and 图 9-9		5	30	ns
t_{PLZ}	Disable time	See 图 9-8 and 图 9-9		5	30	ns
t_{PHZ}, t_{PLZ}	Disable time	See 图 9-8 and 图 9-9		8	30	ns
t_{PZH}	Enable time	See 图 9-8 and 图 9-9		4	30	ns
t_{PZL}	Enable time	See 图 9-8 and 图 9-9		4	30	ns
t_{PZH}, t_{PZL}	Enable time	See 图 9-8 and 图 9-9		7	30	ns
GPIO channel						

Min / Max specifications are over recommended operating conditions, typical values are at V_{DD} = V_{IO} = 5 V, MODE=V_{ISOOUT} (V_{ISOOUT}= 5 V), GND1 = GNDIO, GND2 = GISOIN, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PHL}, t_{PLH}	Propagation delay time	See 图 9-11		227	347	ns
PWD	Pulse width distortion, $\|t_{PHL} - t_{PLH}\|$			20	110	ns
t_r	Output signal rise time			2.2	4	ns
t_f	Output signal fall time			2.2	4	ns

(1) Also known as pulse skew.

8.13 Insulation Characteristics Curves

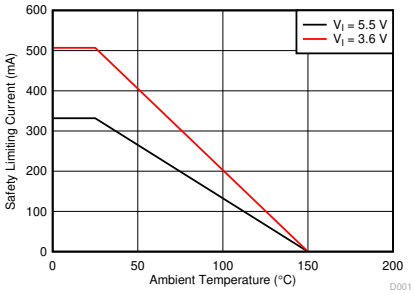


图 8-1. Thermal Derating Curve for Limiting Current per VDE

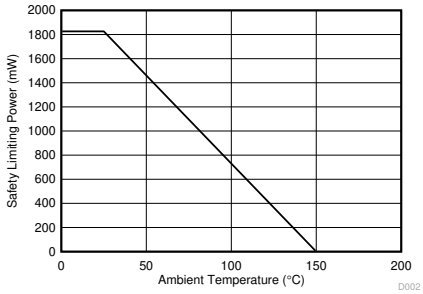
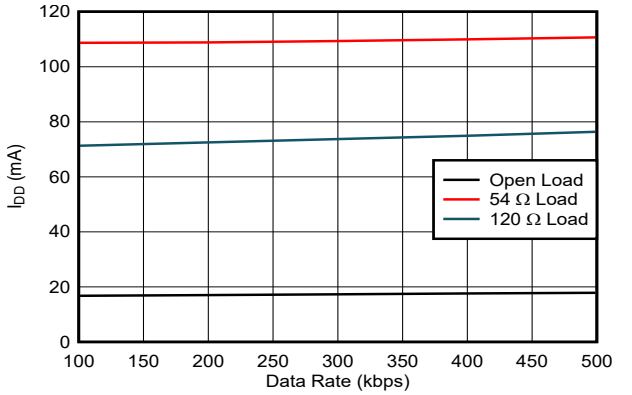


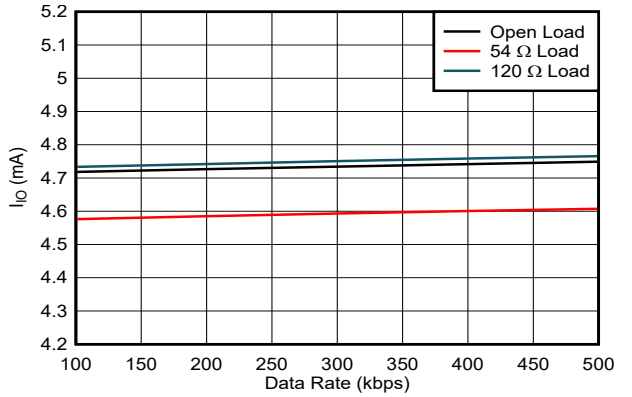
图 8-2. Thermal Derating Curve for Limiting Power per VDE

8.14 Typical Characteristics



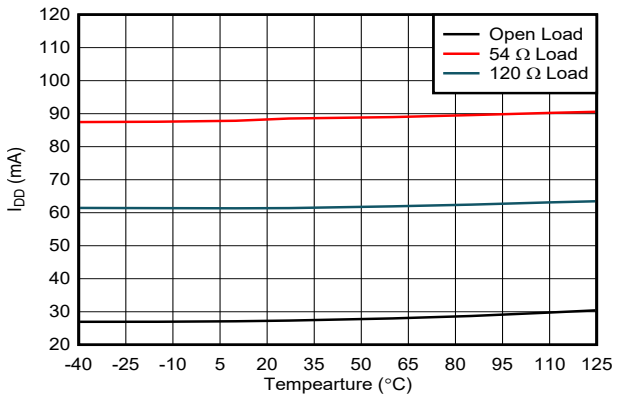
MODE = GND2 V_{DD} = 3.3 V $\overline{RE}$ = GND1
T_A = 25°C DE = V_{IO}

图 8-3. ISOW1412 V_{DD} Supply Current vs. Data Rate - RS485 Mode



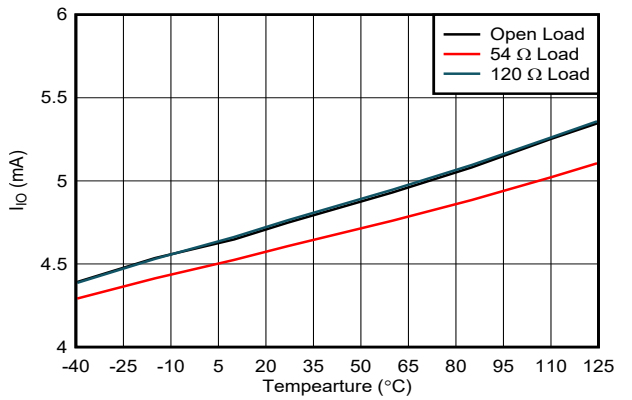
MODE = GND2 V_{DD} = 3.3 V $\overline{RE}$ = GND1
T_A = 25°C DE = V_{IO}

图 8-4. ISOW1412 VIO Supply Current vs. Data Rate - RS485 Mode



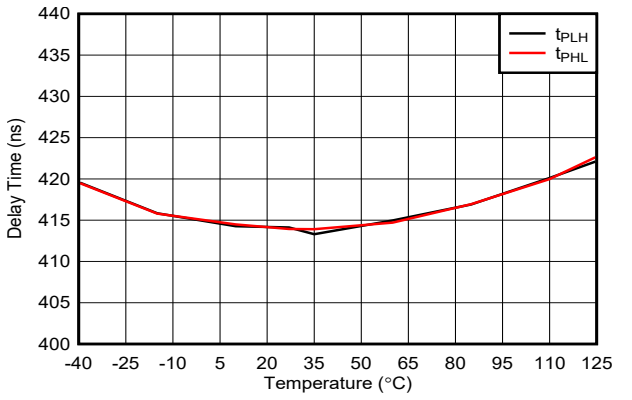
MODE = GND2 V_{DD} = 3.3 V $\overline{RE}$ = GND1
DE = V_{IO}

图 8-5. ISOW1412 VDD Current vs. Temperature - RS485 Mode



MODE = GND2 V_{DD} = 3.3 V $\overline{RE}$ = GND1
DE = V_{IO}

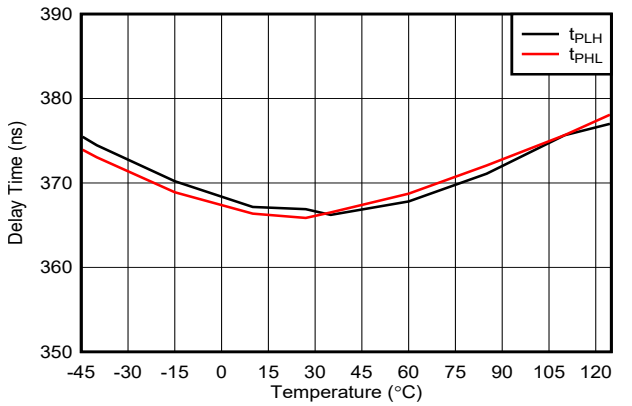
图 8-6. ISOW1412 VIO Current vs. Temperature - RS485 Mode



MODE = GND2 V_{DD} = 3.3 V LOAD = 54 Ω || 50pF

DE = V_{IO}

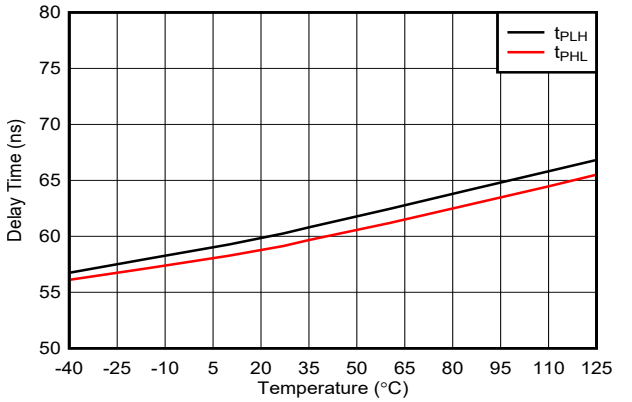
图 8-7. ISOW1412 Driver Propagation Delay vs. Temperature - RS485 Mode



MODE = V_{ISOOUT} V_{DD} = 5 V LOAD = 54 Ω || 50pF

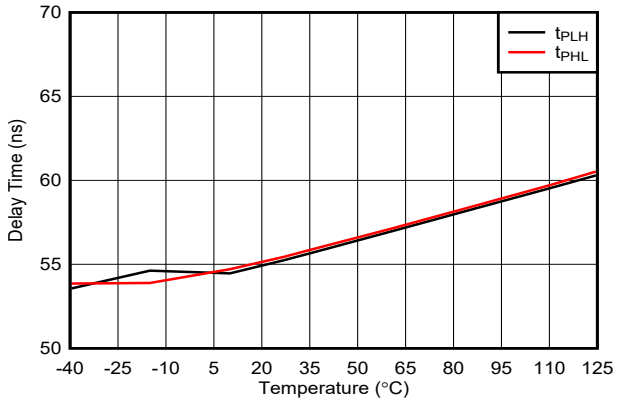
DE = V_{IO}

图 8-8. ISOW1412 Driver Propagation Delay vs. Temperature - Profibus Mode



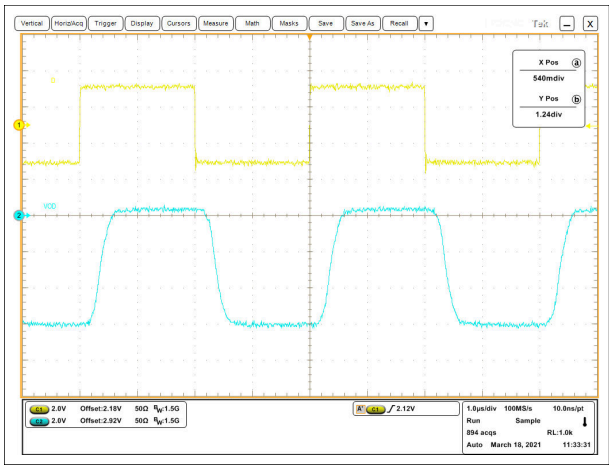
MODE = GND2 V_{DD} = 3.3 V $\overline{RE}$ = GND1 LOAD = 54 Ω || 50pF

图 8-9. ISOW1412 Receiver Propagation Delay vs. Temperature - RS485 Mode



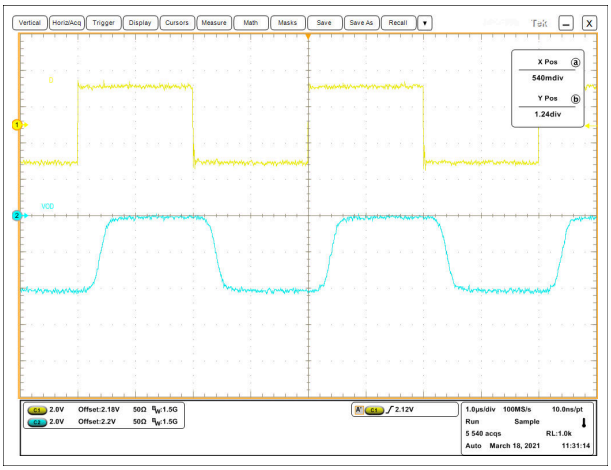
MODE = V_{ISOOUT} V_{DD} = 5 V $\overline{RE}$ = GND1 LOAD = 54 Ω || 50pF

图 8-10. ISOW1412 Receiver Propagation Delay vs. Temperature - Profibus Mode



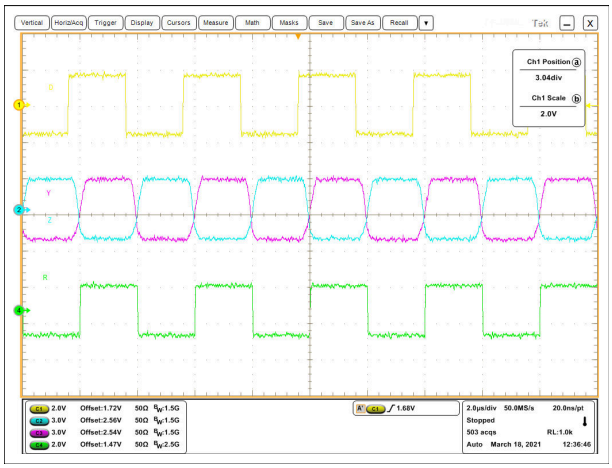
MODE = GND2
LOAD = 54 Ω || 50pF
V_{DD} = 3.3 V
T_A = 25°C
DE = V_{IO}

图 8-11. ISOW1412 Driver Propagation Delay - Profibus Mode



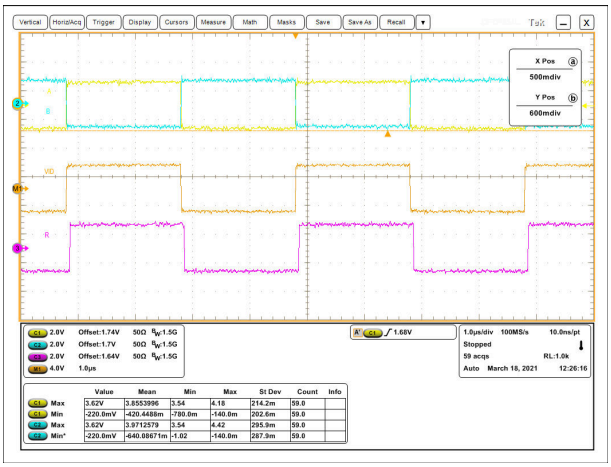
MODE = V_{ISOOUT}
LOAD = 54 Ω || 50pF
V_{DD} = 5 V
T_A = 25°C
DE = V_{IO}

图 8-12. ISOW1412 Driver Propagation Delay - RS485 Mode



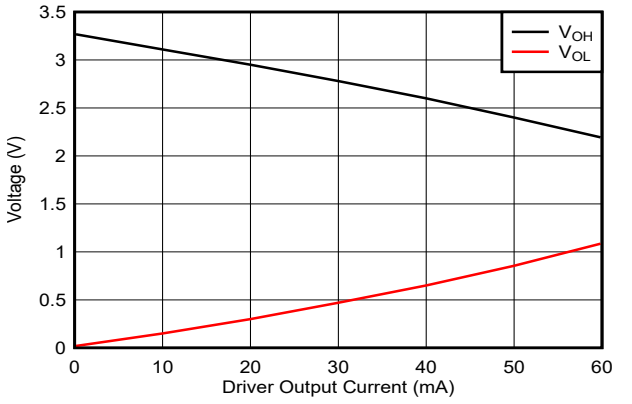
MODE = GND2
LOAD = 54 Ω || 50pF
V_{DD} = 3.3 V
T_A = 25°C
$\overline{RE}$ = GND1

图 8-13. ISOW1412 Receiver Propagation Delay - Profibus Mode



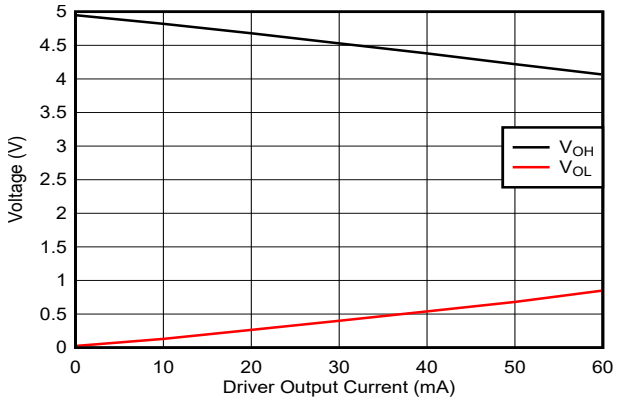
MODE = V_{ISOOUT}
LOAD = 54 Ω || 50pF
V_{DD} = 5 V
T_A = 25°C
$\overline{RE}$ = GND1

图 8-14. Receiver Propagation Delay - RS485 Mode



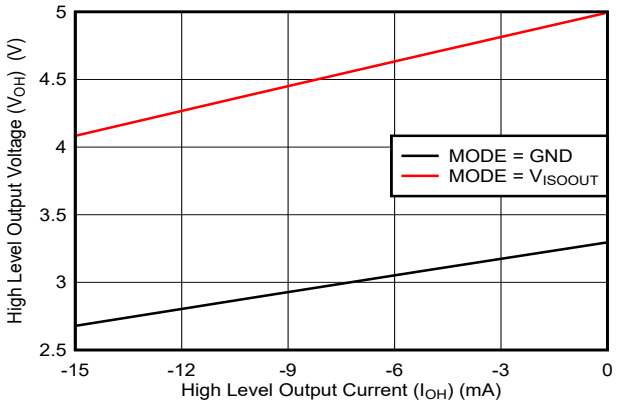
MODE = GND2 V_{DD} = 3.3 V DE = V_{IO}
LOAD = 54 Ω T_A = 25°C

图 8-15. ISOW1412 Driver output voltage vs. Driver output current - RS485 Mode



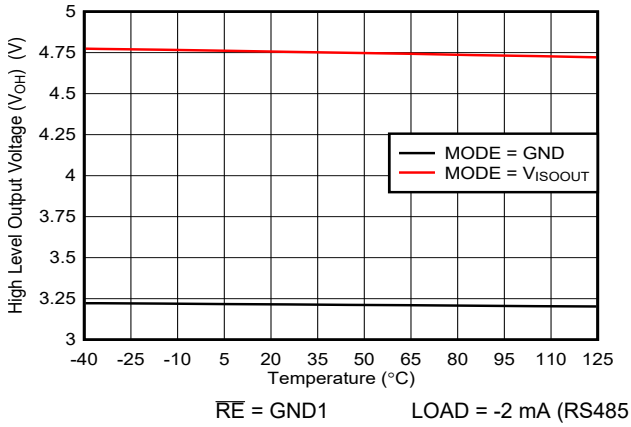
MODE = V_{ISOOUT} V_{DD} = 5 V DE = V_{IO}
LOAD = 54 Ω T_A = 25°C

图 8-16. ISOW1412 Driver output voltage vs. Driver output current - Profibus Mode



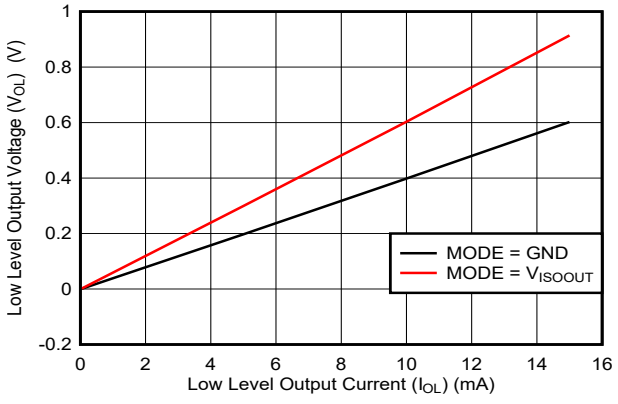
$\overline{RE}$ = GND1 Load = 54 Ω T_A = 25°C

图 8-17. ISOW1412 Receiver Buffer High Level output voltage vs. High Level output current - RS485 & Profibus Mode



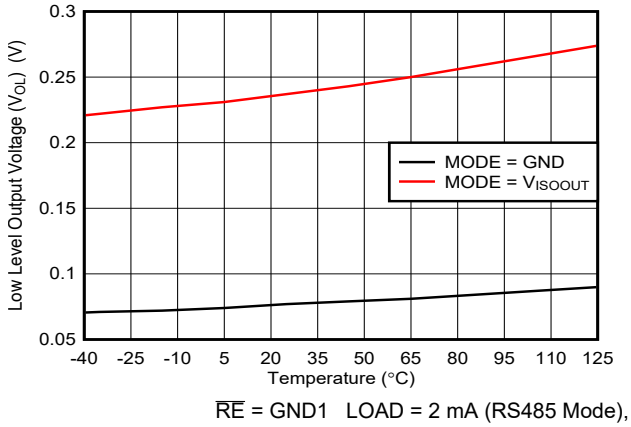
$\overline{RE}$ = GND1 LOAD = -2 mA (RS485 Mode), -4mA (Profibus Mode)

图 8-18. ISOW1412 Receiver Buffer High Level output voltage vs. Temperature - RS485 & Profibus Mode



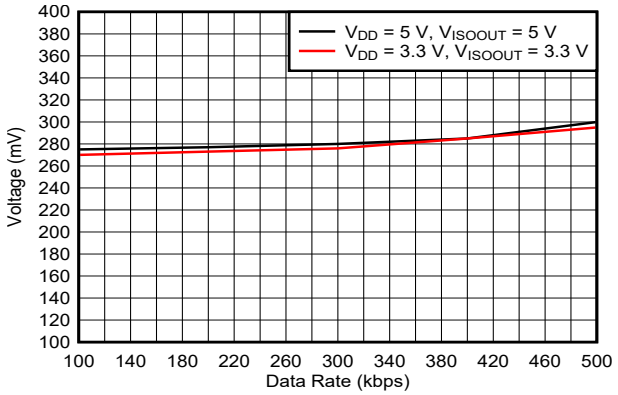
$\overline{RE}$ = GND1 LOAD = 54 Ω T_A = 25°C

图 8-19. ISOW1412 Receiver Buffer Low Level output voltage vs. Low Level output current - RS485 & Profibus Mode



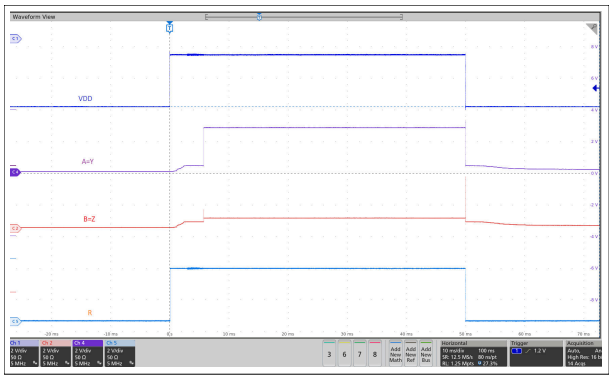
$\overline{RE}$ = GND1 LOAD = 2 mA (RS485 Mode), 4mA (Profibus Mode)

图 8-20. ISOW1412 Receiver Buffer Low Level output voltage vs. Temperature - RS485 & Profibus Mode



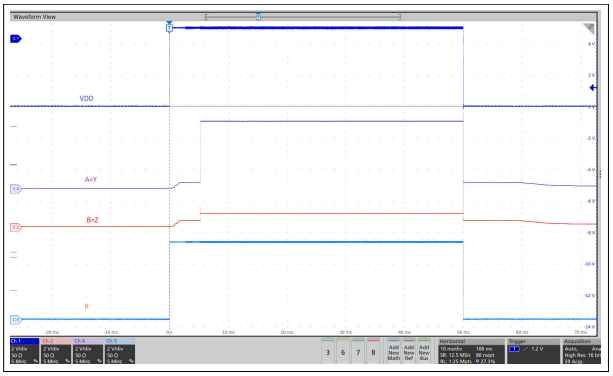
For PWD ⩽±5% T_A = 25°C

图 8-21. ISOW1412 Receiver VID vs. Data Rate - RS485 & Profibus Mode



MODE = GND2 D = V_{IO} DE = V_{IO}
$\overline{RE}$ = GND1 T_A = 25°C LOAD = 54 Ω || 50pF

图 8-22. Glitch-free Power up/down- RS485 Mode



MODE = V_{ISOOUT} D = V_{IO} DE = V_{IO}
T_A = 25°C LOAD = 54 Ω || 50pF

图 8-23. Glitch-free Power up/down- Profibus Mode

9 Parameter Measurement Information

In this section, GND1 = GNDIO, GND2 = GISOIN unless otherwise noted.

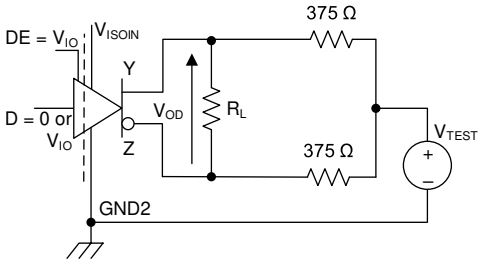
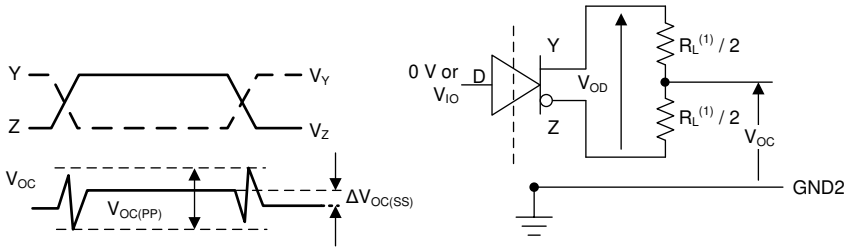
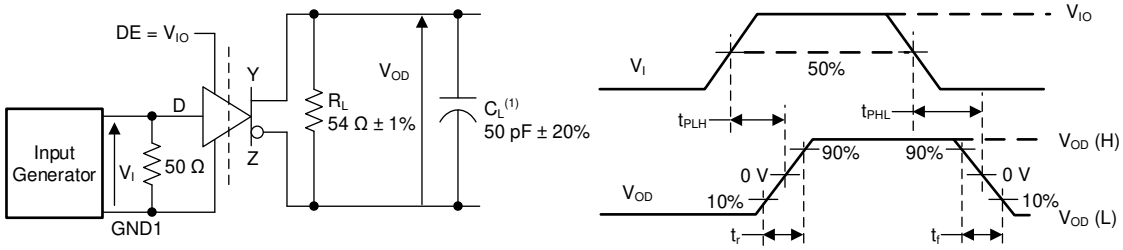


图 9-1. Driver Voltages



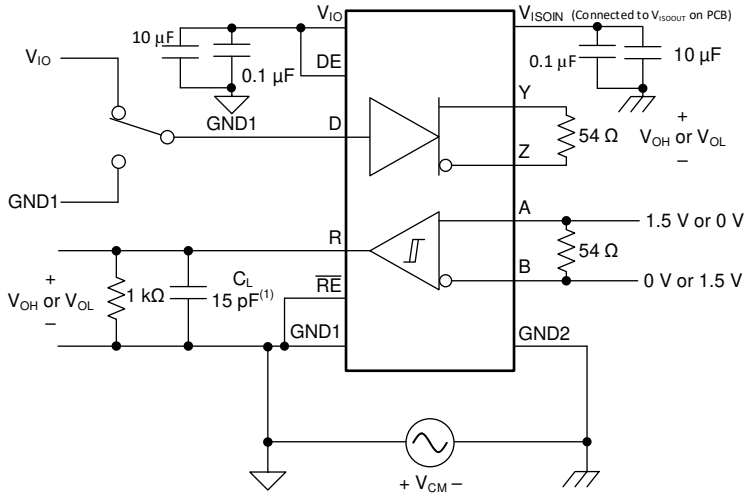
A. R_L = 100 Ω for RS-422, R_L = 54 Ω for RS-485

图 9-2. Driver Voltages



A. C_L includes fixture and instrumentation capacitance

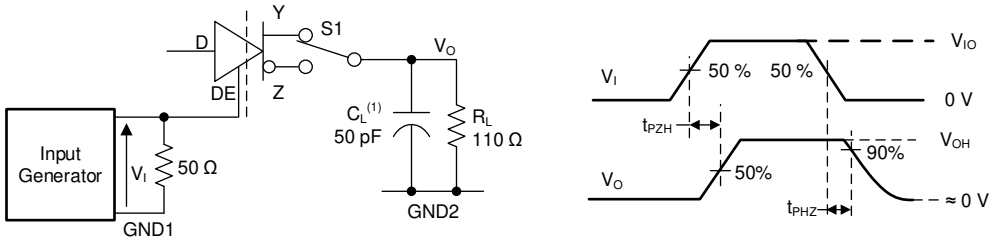
图 9-3. Driver Switching Specifications



A. Includes probe and fixture capacitance

B. Pass-fail criteria: Device is tested in both half-duplex and full-duplex conditions. Both the signal path and power path should be in specification compliant region during the application of CMTI pulse. This means no bit flips on R, and both V_{ISOOUT} and Driver V_{OD} should be within specifications mentioned in electrical characterisitcs table.

图 9-4. Common Mode Transient Immunity (CMTI)—Full Duplex



A. C_L includes fixture and instrumentation capacitance

图 9-5. Driver Enable and Disable Times

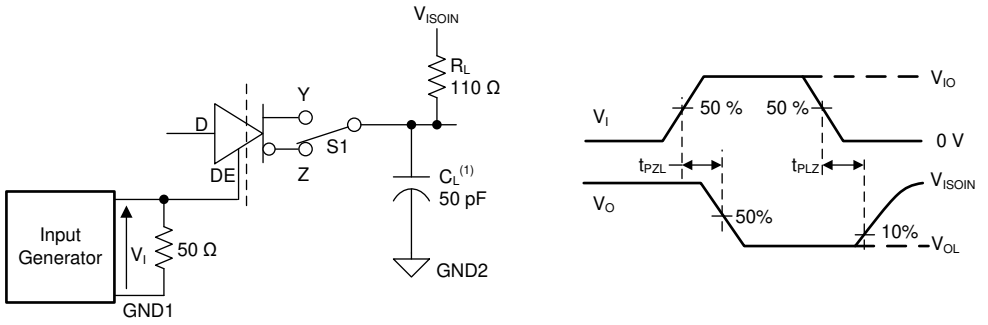
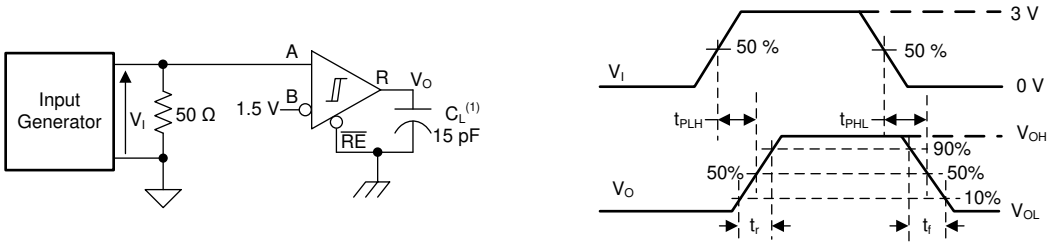


图 9-6. Driver Enable and Disable Times



A. C_L includes fixture and instrumentation capacitance

图 9-7. Receiver Switching Specifications

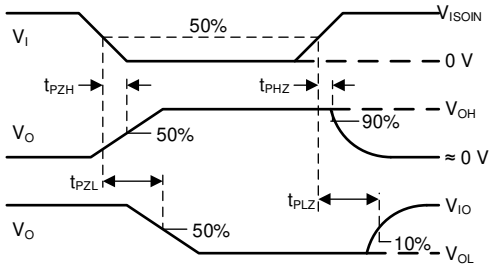


图 9-8. Receiver Enable and Disable Times

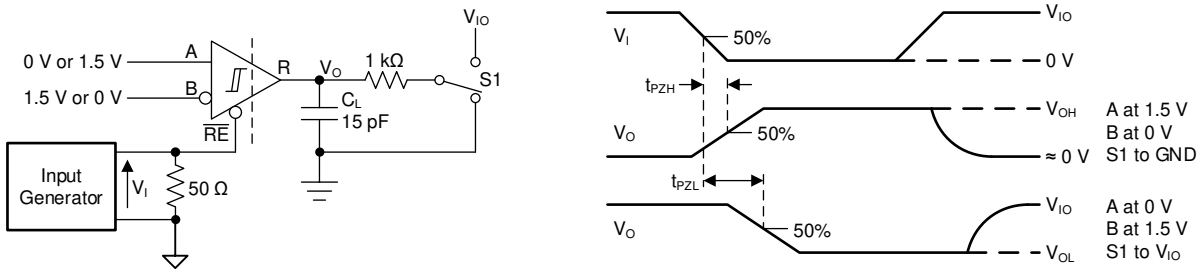
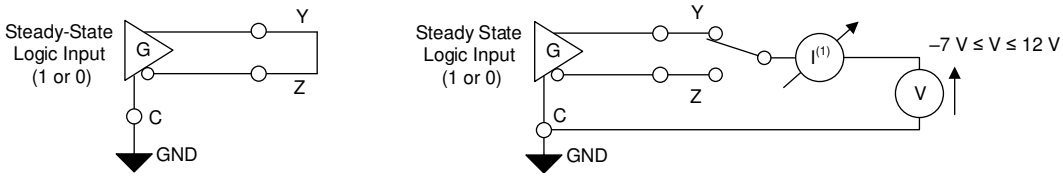
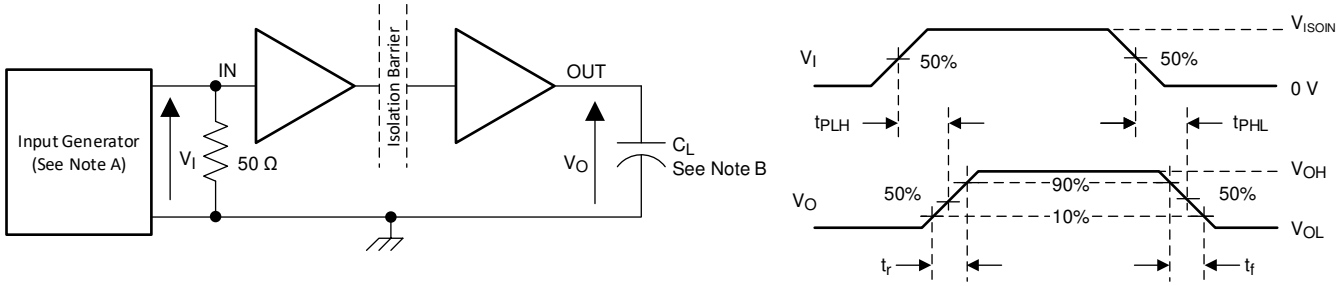


图 9-9. Receiver Enable and Disable Times



A. The driver should not sustain any damage with this configuration

图 9-10. Short-Circuit Current Limiting



The input pulse is supplied by a generator having the following characteristics: PRR ⩽ 50 kHz, 50% duty cycle, t_r ⩽ 3 ns, t_f ⩽ 3 ns, Z_O = 50 Ω. At the input, 50-Ω resistor is required to terminate the input generator signal. The resistor is not required in the actual application. C_L = 15 pF and includes instrumentation and fixture capacitance within ±20%.

图 9-11. GPIO Channel: Switching Characteristics Test Circuit and Voltage Waveforms

10 Detailed Description

10.1 Overview

The ISOW14x2 family of devices has signal isolation channels, power isolation with integrated transformer and RS-485 transceiver all integrated in one package. ISOW1412 supports maximum signaling rate up to 500 kbps, while ISOW1432 is designed for 12 Mbps maximum data rate. Figure 10-1 shows functional block diagram of ISOW14x2 family of devices.

10.2 Power Isolation

The integrated isolated DC-DC converter uses advanced circuit and on-chip layout techniques to reduce radiated emissions and achieve up to 46% typical efficiency. The integrated transformer uses thin film polymer as the insulation barrier. Output voltage of power converter can be controlled to 3.3 V or 5 V using MODE pin. In case bus communication is not needed, the DC-DC converter can be switched off using EN (enable) pin to save power. The output voltage, V_{ISOOUT}, is monitored and feedback information is conveyed to the primary side through a dedicated isolation channel. The duty cycle of the primary switching stage is adjusted accordingly. The fast feedback control loop of the power converter ensures low overshoots and undershoots during load transients. Undervoltage lockout (UVLO) with hysteresis is integrated on the V_{IO}, V_{DD} and V_{ISOOUT} supplies which ensures robust fails-safe system performance under noisy conditions. An integrated soft-start mechanism ensures controlled inrush current and avoids any overshoot on the output during power up.

10.3 Signal Isolation

The integrated signal isolation channels employ an ON-OFF keying (OOK) modulation scheme to transmit the digital data across a silicon-dioxide based isolation barrier. The transmitter sends a high frequency carrier across the barrier to represent one state and sends no signal to represent the other state. The receiver demodulates the signal after signal conditioning and produces the output through a buffer stage. The signal-isolation channels incorporate advanced circuit techniques to maximize the CMTI performance and minimize the radiated emissions from the high frequency carrier and IO buffer switching. 图 10-2 shows a functional block diagram of a typical signal isolation channel.

In order to keep any noise coupling from power converter away from signal path, power supplies on side1 for power converter (V_{DD}) and signal path(V_{IO}) are kept separate. Similarly on side2, power converter output (V_{ISOOUT}) needs to be connected to power supply for RS-485 (V_{ISOIN}) externally on PCB. For more details, refer to Layout guidelines section.

10.4 RS-485

In a typical RS-485 network, multiple nodes may be connected on the bus and the distance of communicating nodes can be as far as 4000-5000 feet. While communicating at such large distances, usual common mode of non-isolated RS-485 transceiver is not sufficient. ISOW14x2 has integrated isolation barrier with upto 1500 Vpk working voltage rating. Isolation breaks the ground loop between the communicating nodes and allows for data transfer in the presence of large ground potential differences. These devices have a higher typical differential output voltage (V_{OD}) than traditional transceivers for better noise immunity. A minimum differential output voltage of 2.1 V is specified when V_{ISOIN} is configured for 5 V supply which meets the requirements for PROFIBUS applications.

The ISOW14x2 family of devices is suitable for applications that have limited board space and require more integration. Only external bypass capacitors are needed to fully realize an isolated RS-485 port. This family of devices is also suitable for very-high voltage applications, where power transformers for discrete isolated supply meeting the required isolation specifications are bulky and expensive. Though the device family is full-duplex, it can also be used for half-duplex applications by connecting driver output (Y , Z) to receiver input (A , B) on PCB- this helps to reduce cabling costs. For more details, refer to Application Information.

10.5 Functional Block Diagram

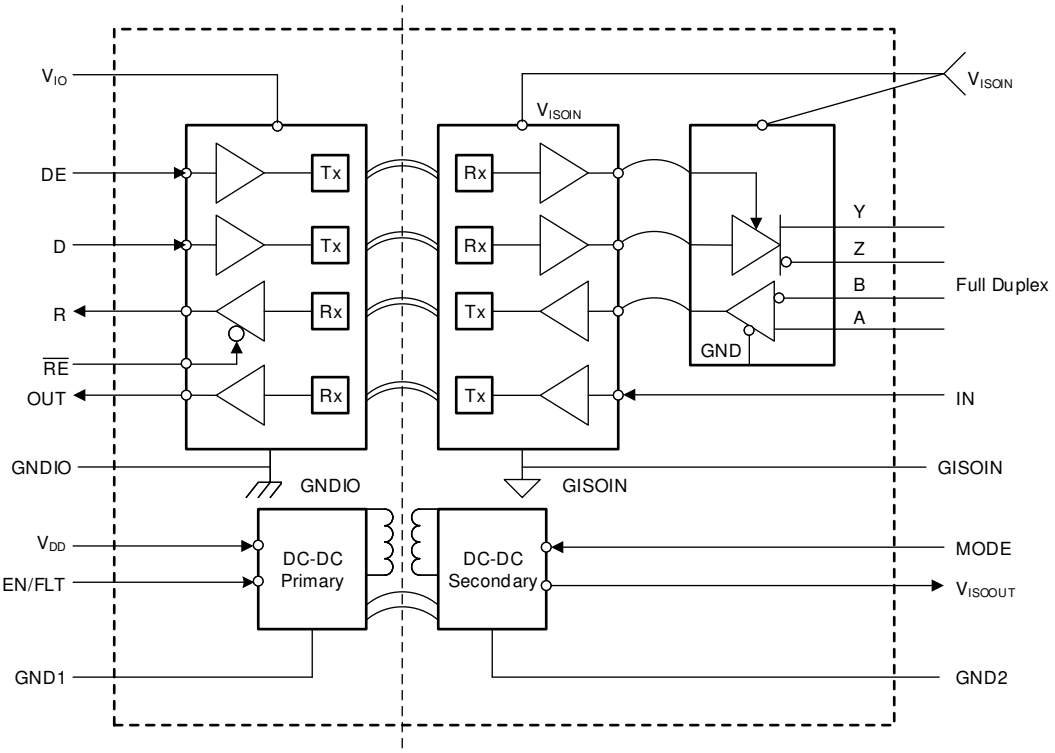


图 10-1. Block Diagram

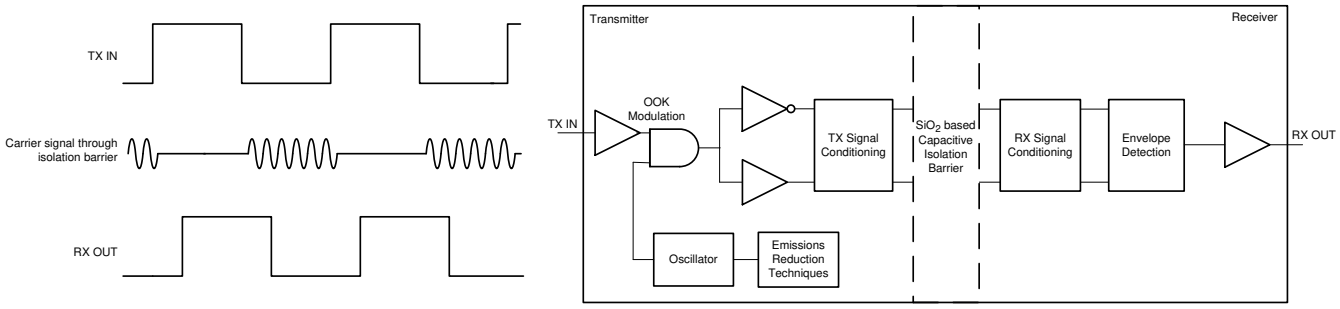


图 10-2. Signal Isolation channel

10.6 Feature Description

10.6.1 Power-Up and Power-Down Behavior

The ISOW14x2 family of devices has built-in under-voltage lockout (UVLO) on all supplies (V_{DD}, V_{IO} and V_{ISOOUT}) with positive-going and negative-going thresholds and hysteresis. Both the power converter supply (V_{DD}) and Logic supply (V_{IO}) need to be present for the device to work. If either of them is below its UVLO, both the signal path and the power converter are disabled.

Assuming V_{IO} is above its UVLO+, when the V_{DD} voltage crosses the positive-going UVLO threshold during power-up, the DC-DC converter initializes and the power converter duty cycle is increased in a controlled manner. This soft-start scheme limits primary peak currents drawn from the V_{DD} supply and charges the V_{ISOOUT} output in a controlled manner, avoiding overshoots. RS-485 driver output is in high impedance state in this duration. When the UVLO positive-going threshold is crossed on the secondary side V_{ISOOUT} pin, the feedback channel starts providing feedback to the primary controller. The regulation loop takes over and RS-485 drive output, Received data output R and general purpose logic output OUT take their respective states defined by the inputs to the device i.e. Driver enable(DE), Driver data to be transmitted D, Receiver enable $\overline{RE}$ and general

purpose logic input IN respectively. Designers should consider a sufficient time margin (typically 5 ms with 10-µF load capacitance) to allow this power up sequence before any usable system functionality.

When either of V_{DD} or V_{IO} is lost, the primary side DC-DC controller turns off when the UVLO lower threshold is reached. The V_{ISOOUT} capacitor then discharges depending on the isolation channels and RS-485 load.

10.6.2 Protection Features

The ISOW14x2 family of devices has multiple protection features to create a robust system level solution.

- The first feature is an Enable/Fault protection feature. This EN/FLT pin can be used as either an input pin to enable or disable the integrated DC-DC power converter or as an output pin which works as an alert signal if the power converter is not operating properly. In the /Fault use case, a fault is reported if V_{DD} > 7 V, V_{DD} < 2.5 V, or if the junction temperature >170°C. When a fault is detected, this pin will go low, disabling the DC-DC converter to prevent any damage.

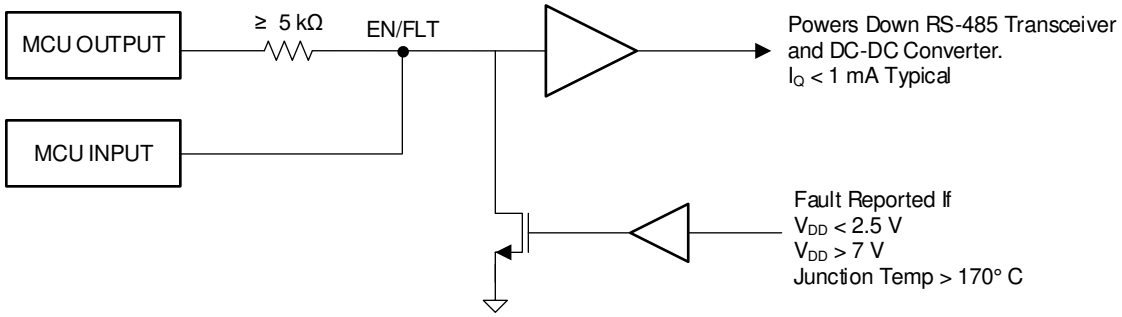


图 10-3. EN Fault Pin Diagram

- An over-voltage clamp feature is present on V_{ISOOUT} which will clamp the voltage at 6 V at Profibus mode (MODE = V_{ISOOUT}) or 4V at RS485 mode (MODE = GND2), if there is an increase in voltage seen. For device reliability, it is recommended that V_{ISOOUT} stays lower than the over-clamp voltage for device reliability.
- Over-Voltage Lock Out (OVLO) on VDD will occur when a voltage higher than 7 V on VDD is seen. At OVLO, the device will go into a low power state and the EN/FLT pin will go low.
- These devices are protected against output overload and short circuit. In cases of overload or short on power converter output V_{ISOOUT}, maximum duty cycle of power converter is limited. In cases of driver bus short circuit due to the external power supply cable shorting to the bus cable, or due to bus contention, short circuit current protection on RS-485 chip restricts the bus current to ±250 mA maximum.
- Thermal protection is also integrated to help prevent the device from getting damaged under such scenarios. An increase in the die temperature is monitored and the device is disabled when the die temperature becomes 165℃ (typical), thus disabling the short condition. The device is re-enabled when the junction temperature becomes 155℃ (typical). If an overload or output short-circuit condition prevails, this protection cycle is repeated. Care should be taken in the system design to prevent repeated or prolonged exposure to bus shorts as this exposes the device to high junction temperatures for extreme amounts of time affecting device reliability.

10.6.3 Failsafe Receiver

The differential receiver of the ISOW14x2 devices has failsafe protection from invalid bus states caused by:

- Open bus conditions such as a broken cable or a disconnected connector
- Shorted bus conditions such as insulation breakdown of a cable that shorts the twisted-pair
- Idle bus conditions that occur when no driver on the bus is actively driving.

The differential input of the RS-485 receiver is 0 in any of these conditions for a terminated transmission line. The receiver outputs a failsafe logic-high state on R pin so that the output of the receiver is determinate. The

receiver thresholds are offset in the receiver design so that the indeterminate range does not include a 0 V differential. See Receiver functional table for more details.

10.6.4 Glitch-Free Power Up and Power Down

Communication on the bus that already exist between a master node and slave node in an RS-485 network must not be disturbed when a new node is swapped in or out of the network. No glitches on the bus should occur when the device is:

- Hot plugged into the network in an unpowered state
- Hot plugged into the network in a powered state and disabled state
- Powered up or powered down in a disabled state when already connected to the bus

The ISOW14x2 devices meet above criteria and do not cause any false data toggling on the bus when powered up or powered down in a disabled state with supply ramp rates >= 50 us.

10.7 Device Functional Modes

表 10-1 lists the supply configuration for these devices:

表 10-1. Supply configuration Function Table

INPUTS				OUTPUT
V_{DD} (1)	V_{IO}	EN/FLT	MODE	V_{ISOOUT} (3)
< $V_{DD(UVLO+)}$	>$V_{IO(UVLO+)}$	H or Open	X	OFF
>$V_{DD(UVLO+)}$	<$V_{IO(UVLO+)}$		X	Invalid Operation
5 V	1.71 V to 5.5 V		High(shorted to V_{ISOOUT})	5 V
5 V or 3.3 V	1.71 V to 5.5 V		Low(shorted to GND2) or floating (2)	3.3 V
3.3 V	1.71 V to 5.5 V		High(shorted to V_{ISOOUT})	Invalid Operation
X	X	L	X	OFF

(1) V_{DD}= 3.3 V, MODE shorted to V_{ISOOUT}(essentially V_{ISOOUT} = 5 V) is an invalid operation
(2) The MODE pin has a weak pulldown internally. Therefore for V_{ISOOUT} = 3.3 V, the MODE pin should be strongly connected to the GND2 pin in noisy system scenarios.
(3) V_{ISOOUT} shorted to V_{ISOIN} on PCB. GND2 and GISOIN pins are shorted to each other and EN=High

表 10-2 shows the driver functional modes:

表 10-2. Driver Functional Table

INPUTS					OUTPUTS(3)	
V_{DD} (1)	V_{IO}	EN/FLT	D	DE	Y, A	Z, B
PU	PU	H or Open	H	H	H	L
			L	H	L	H
			X	L	Hi-Z	Hi-Z
			X	Open	Hi-Z	Hi-Z
			Open	H	H	L
		L	X	X	Hi-Z	Hi-Z
PD	PU	X	X	X	Hi-Z	Hi-Z
PU	PD(2)	X	X	X	Invalid Operation	

(1) PU=Powered up, PD=Powered down; H=high level; L=Low level; X=Irrelevant; Hi-Z=High impedance state
(2) A strongly driven input signal on D, DE or RE can weakly power the floating V_{IO} through an internal protection diode and cause an undetermined output.
(3) V_{ISOOUT} shorted to V_{ISOIN} on PCB and both GND2 pins are shorted to each other and EN=High

When the driver enable pin, DE, is logic high, the differential outputs, Y and Z, follow the logic states at data input, D. A logic high at the D input causes the Y output to go high and the Z output to go low. Therefore the differential output voltage defined by Equation 1 is positive.

$$V_{OD} = V_Y - V_Z \quad (1)$$

A logic low at the D input causes the Z output to go high and the Y output to go low. Therefore the differential output voltage defined by Equation 1 is negative. A logic low at the DE input causes both outputs to go to the high-impedance (Hi-Z) state. The logic state at the D pin is irrelevant when the DE input is logic low. The DE pin has an internal pulldown resistor to ground. The driver is disabled (bus outputs are in the Hi-Z) by default when the DE pin is left open. The D pin has an internal pullup resistor. The Y output goes high and the Z output goes low when the D pin is left open while the driver enabled.

表 10-3 shows the receiver functional modes:

表 10-3. Receiver Functional Table

INPUTS					OUTPUT
V_{DD} (1)	V_{IO}	EN/FLT	Differential Input $V_{ID} = V_A - V_B$	$\overline{RE}$	R (3)
PU	PU	H or Open	$V_{ID} > V_{IT+}$	L	H
			$V_{IT-} < V_{ID} < V_{IT+}$	L	Indeterminate
			$V_{ID} < V_{IT-}$	L	L
			X	H	Hi-Z
			X	Open	Hi-Z
			Open, Short, Idle	L	H
		L	X	X	H
PD	PU	X	X	X	Hi-Z
PU	PD(2)	H or Open	X	X	Invalid Operation
		L	X	X	

(1) PU=Powered up, PD=Powered down; H=high level; L=Low level; X=Irrelevant; Hi-Z=High impedance state
(2) A strongly driven input signal on D, DE or $\overline{RE}$ can weakly power the floating VIO through an internal protection diode and cause an undetermined output.
(3) V_{ISOOUT} shorted to V_{ISOIN} on PCB and both GND2 pins are shorted to each other and EN/FLT=High

The receiver is enabled when the receiver enable pin, $\overline{RE}$, is logic low. The receiver output, R, goes high when the differential input voltage defined by Equation 2 is greater than the positive input threshold, V_{TH+}.

$$V_{ID} = V_A - V_B \quad (2)$$

The receiver output, R, goes low when the differential input voltage defined by Equation 2 is less than the negative input threshold, V_{TH-}. If the V_{ID} voltage is between the V_{TH+} and V_{TH-} thresholds, the output is indeterminate. The receiver output is in the Hi-Z state and the magnitude and polarity of V_{ID} are irrelevant when the $\overline{RE}$ pin is logic high or left open. The internal biasing of the receiver inputs causes the output to go to a failsafe-high when the transceiver is disconnected from the bus (open-circuit), the bus lines are shorted to one another (short-circuit), or the bus is not actively driven (idle bus).

Other device feature functional states in shown in 表 10-4 and 表 10-5 below:

表 10-4. DC-DC Converter Enable/Disable

INPUTS			OUTPUT
V_{DD}	V_{IO}	EN/FLT	V_{ISOOUT}
PU	PU	H or Open	3.3 V or 5 V depending on MODE pin setting
PU	PU	L	OFF

表 10-5. General Purpose Logic Input/Output

INPUTS				OUTPUT	Comments
V_{DD} (1) (2)	V_{IO}	EN/FLT	IN	OUT	
PU	PU	H or Open	H	H	Output channel assumes logic state governed by IN
			L	L	
			Open	L	Default state
		L	X	Hi-Z	Device is in disabled state when either of VDD or VIO is missing
PD	PU	X	X	Hi-Z	
PU	PD	X	X	Invalid Operation	

(1) PU = Powered Up; PD = Powered Down; H = Logic High; L= Logic Low; X = Irrelevant, Hi-Z = High Impedance (OFF) state
(2) V_{ISOOUT} shorted to V_{ISOIN} on PCB. GISOIN and GND2 pins are shorted to each other and EN/FLT=High

10.8 Device I/O Schematics

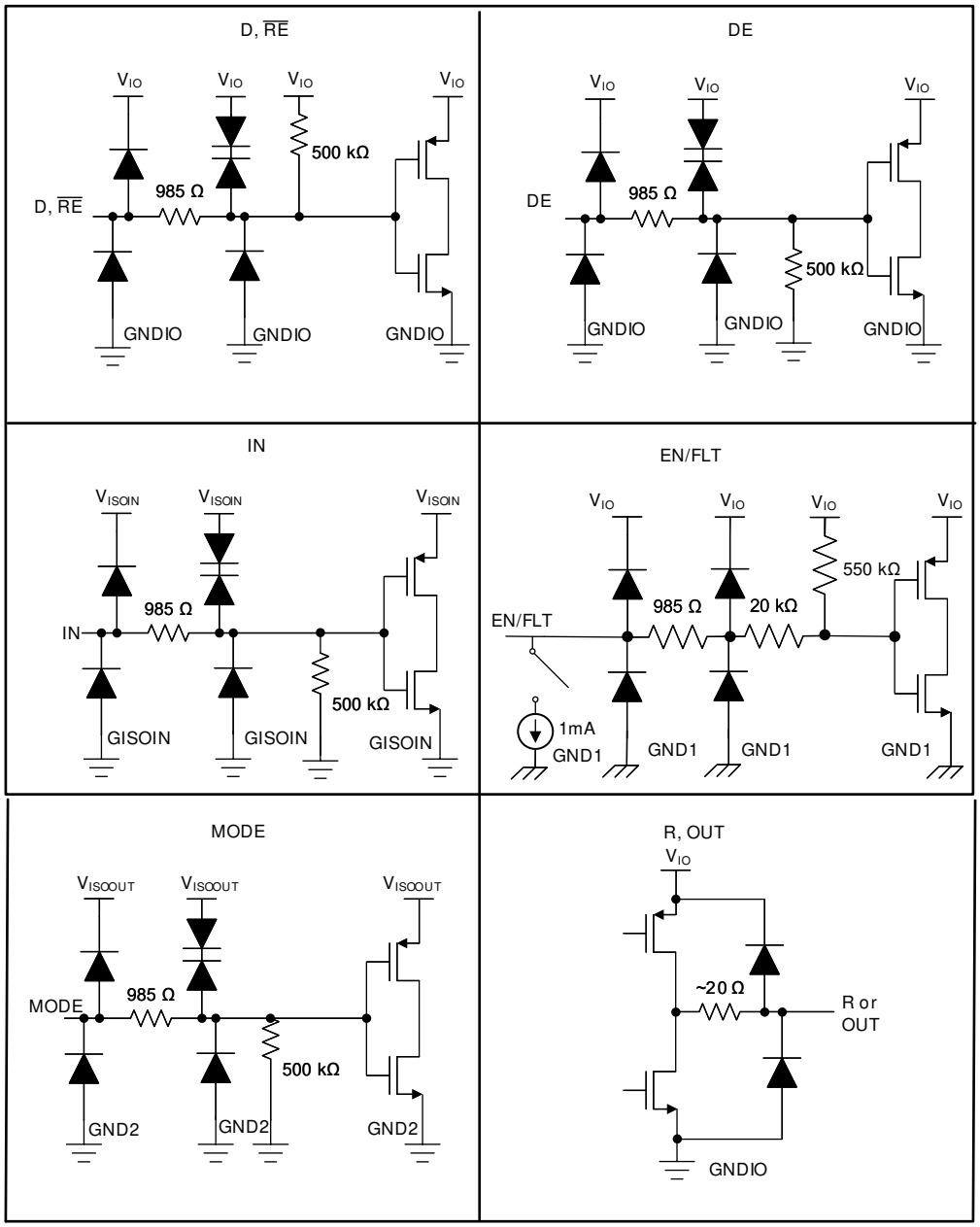


图 10-4. Device I/O schematics

11 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI’s customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

11.1 Application Information

The ISOW14x2 devices are designed for bidirectional data transfer on multipoint RS-485 networks. An RS-485 bus has multiple transceivers that connect in parallel to a bus cable. Both cable ends are terminated with a termination resistor, R_T, to remove line reflections. The value of R_T matches the characteristic impedance, Z_0, of the cable. This method, known as parallel termination, lets higher data rates be used over a longer cable length.

Full-duplex implementation shown in Figure 9-1 requires two signal pairs (four wires). Full-duplex implementation lets each node to transmit data on one pair while simultaneously receiving data on the other pair.

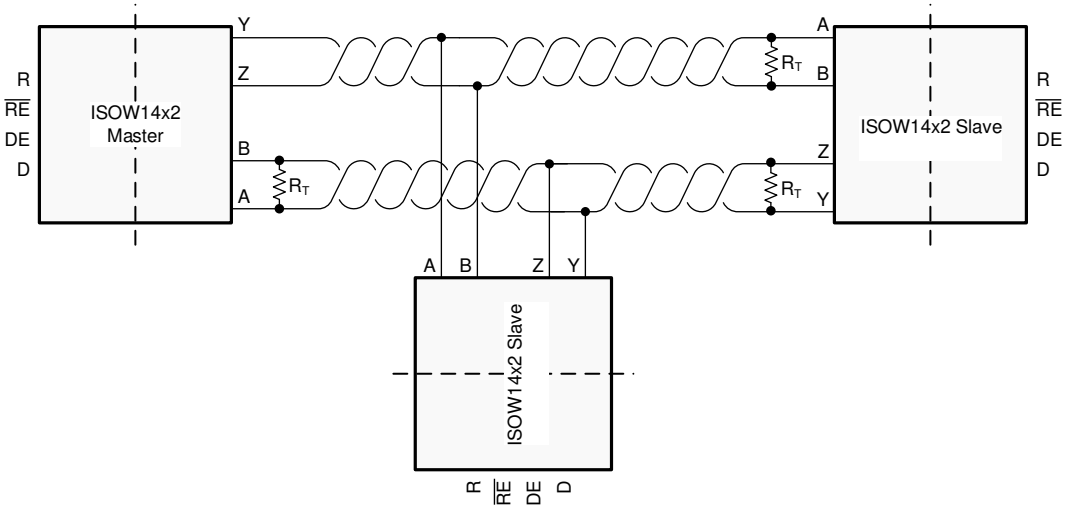


图 11-1. Typical RS-485 network with Full-duplex Isolated transceivers

Figure 9-2 below, shows ISOW14x2 devices used in half duplex configuration. Driver outputs Y and Z are shorted to A and B respectively. This reduces overall cabling requirements. Also DE/RE are shorted to each other, and at a time, any node acts as either a driver or a receiver. Split termination is also shown in this configuration which helps to boost network immunity in noisy environments by providing common-mode noise filtering and also reduces radiated emissions by providing low impedance path to earth to the bus common mode excursions.

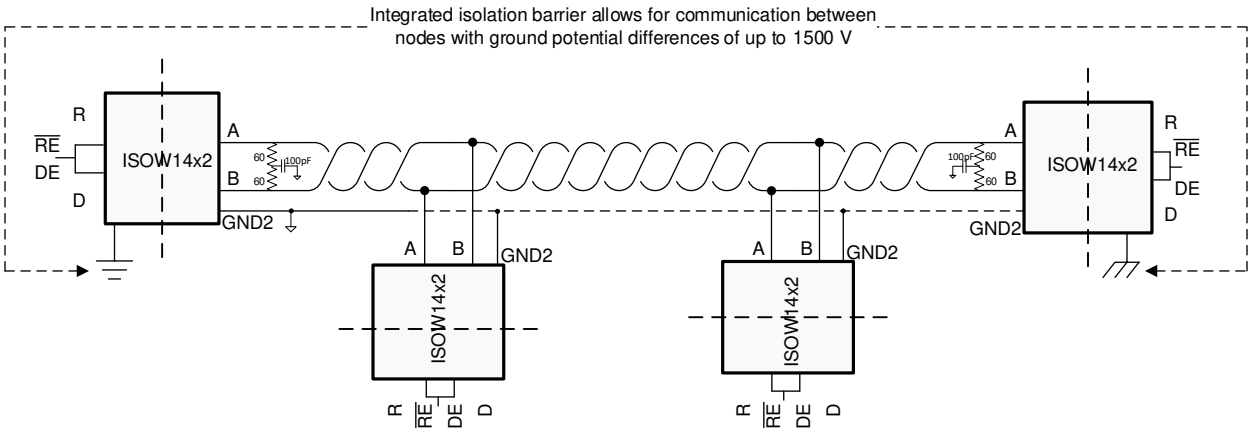
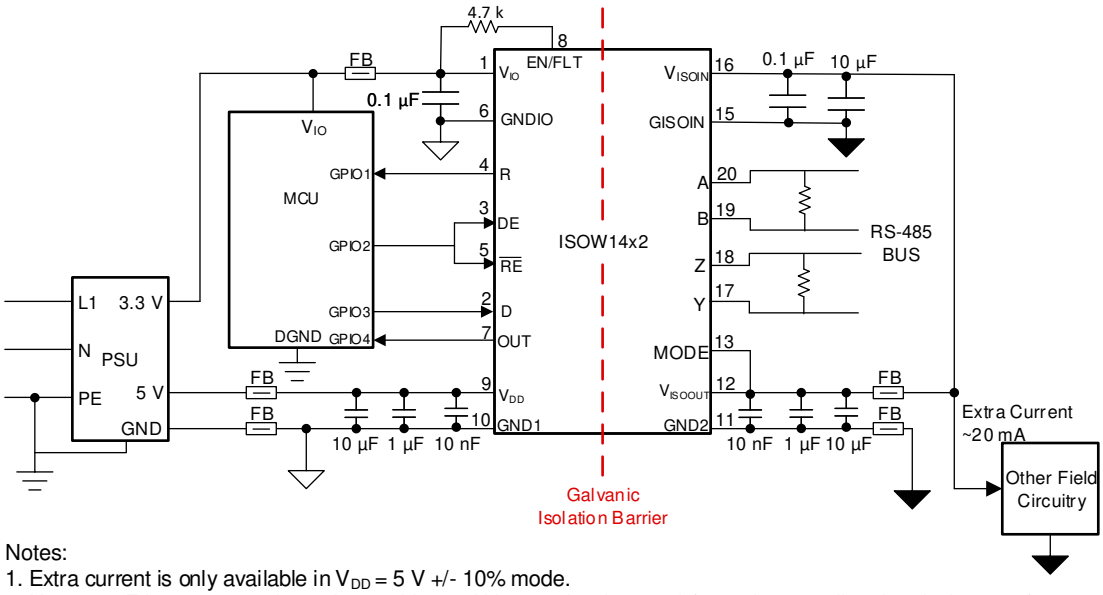


图 11-2. Typical RS-485 Network With Half-Duplex Isolated Transceivers

11.2 Typical Application



Notes:
1. Extra current is only available in V_{DD} = 5 V +/- 10% mode.
2. Keep 10 nF bypass capacitors close to V_{DD} and V_{ISOOUT} pins (< 1 mm) for optimum radiated emissions performance.
3. GND1 and GNDIO must be shorted directly. GND2 and GISOIN must be shorted directly, or through ferrite beads.

图 11-3. Application circuit for ISOW14x2

11.2.1 Design Requirements

Unlike an optocoupler-based solution, which requires several external components to improve performance, provide bias, or limit current, the ISOW14x2 devices only require external bypass capacitors to operate as shown in above application diagram. Because of high peak currents flowing through V_{DD} and V_{ISOOUT} supplies, bulk capacitance of minimum 10 µF is recommended on both pins. Higher values of bulk capacitors will attenuate noise and ripple further, enhancing performance.

11.2.2 Detailed Design Procedure

The RS-485 bus is a robust electrical interface suitable for long-distance communications. The RS-485 interface can be used in a wide range of applications with varying requirements of distance of communication, data rate, and number of nodes.

11.2.2.1 Data Rate, Bus Length and Bus Loading

The RS-485 standard has typical curves similar to those shown in Figure 11-4. These curves show the inverse relationship between signaling rate and cable length. If the data rate of the payload between two nodes is lower, the cable length between the nodes can be longer. Use below Figure as a guideline for cable selection, data rate, cable length and subsequent jitter budgeting.

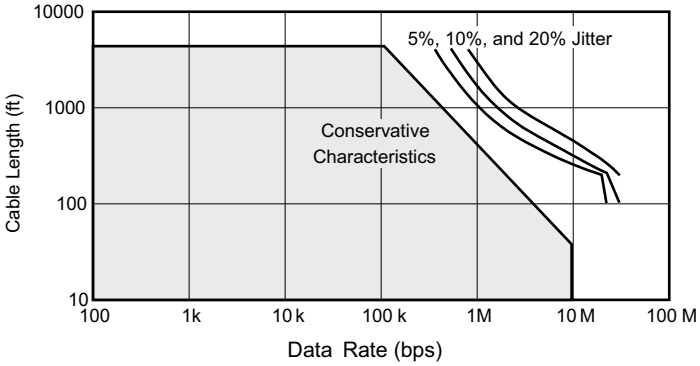


图 11-4. Cable length vs Data rate characteristics

The current supplied by the driver must supply into a load because the output of the driver depends on this current. Add transceivers to the bus to increase the total bus loading. The RS-485 standard specifies a hypothetical term of a unit load (UL) to estimate the maximum number of possible bus loads. The UL represents a load impedance of approximately 12 kΩ. Standard-compliant drivers must be able to drive 32 of these ULs. The ISOW14x2 devices have 1/8 UL impedance transceiver and can connect up to 256 nodes to the bus.

11.2.2.2 Stub Length

In an RS-485 network, the distance between the transceiver inputs and the cable trunk is known as the stub. The stub should be as short as possible when a node is connected to the bus. Stubs are a non-terminated piece of bus line that can introduce reflections of varying phase as the length of the stub increases. The electrical length, or round-trip delay, of a stub should be less than one-tenth of the rise time of the driver as a general guideline. Therefore, the maximum physical stub length (L(STUB)) is calculated as shown in Equation 3.

$$L(STUB) \leqslant 0.1 \times tr \times v \times c \tag{3}$$

where:

- tr is the 10/90 rise time of the driver.
- c is the speed of light (3 × 108 m/s).
- v is the signal velocity of the cable or trace as a factor of c.

11.2.2.3 Insulation Lifetime

Insulation lifetime projection data is collected by using industry-standard Time Dependent Dielectric Breakdown (TDDB) test method. In this test, all pins on each side of the barrier are tied together creating a two-terminal device and high voltage applied between the two sides as shown in below TDDB test setup. The insulation breakdown data is collected at various high voltages switching at 60 Hz over temperature. For reinforced insulation, VDE standard requires the use of TDDB projection line with failure rate of less than 1 part per million (ppm). Even though the expected minimum insulation lifetime is 20 years at the specified working isolation voltage, VDE reinforced certification requires additional safety margin of 20% for working voltage and 87.5% for lifetime which translates into minimum required insulation lifetime of 37.5 years at a working voltage that's 20% higher than the specified value.

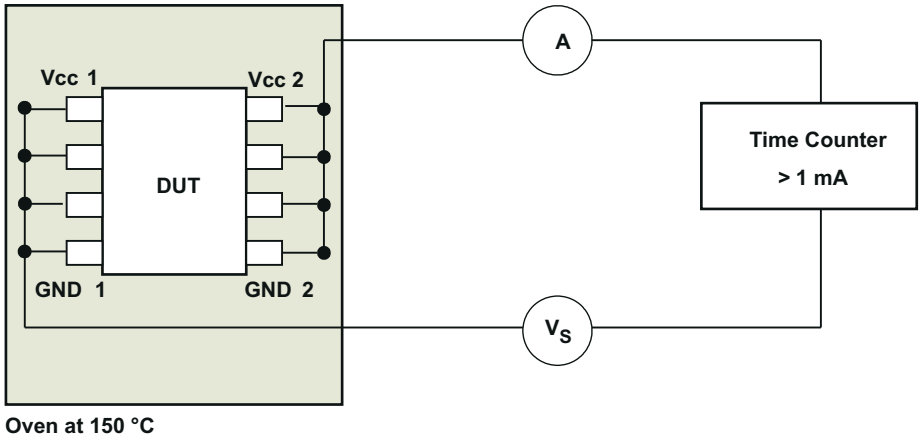


图 11-5. Test Setup for Insulation Lifetime Measurement

The insulation lifetime projection data shows the intrinsic capability of the isolation barrier to withstand high voltage stress over its lifetime. Based on the TDDB data, the intrinsic capability of the insulation is 1000 V_{RMS} with a lifetime of 1184 years.

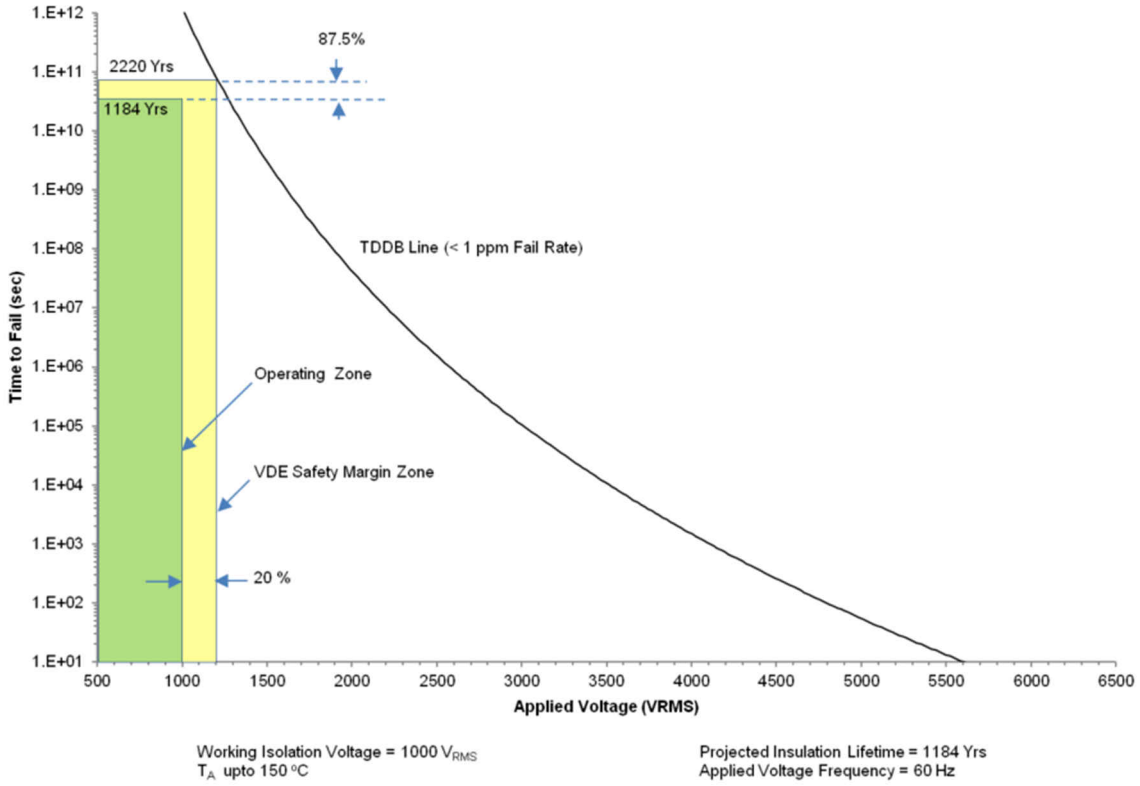


图 11-6. Insulation Lifetime Projection Data

12 Power Supply Recommendations

To make sure that operation is reliable at all data rates and supply voltages, adequate decoupling capacitors must be located as close to supply pins as possible. Power converter input V_{DD} and output V_{ISOOUT} supply pins should have high frequency ceramic capacitors 10 nF and bulk capacitors 10 μF atleast close to the pins. Signal path supply pins, V_{IO} and V_{ISOIN}, should have 100 nF or higher value ceramic bypass capacitors close to device pins. ISOW1412 can consume typical peak pulse currents of upto 250 mA under fully loaded conditions

for short durations (10s of µs) from the power source that is powering V_{DD} of ISOW1412. Please make sure the current limit of upstream power device is at least 300 mA typical.

13 Layout

13.1 Layout Guidelines

Figure 11-1 shows the recommended placement and routing of device bypass capacitors. Below guidelines must be followed to achieve low emissions design:

1. High frequency bypass capacitors 10 nF must be placed close to V_{DD} and V_{ISOOUT} pins, less than 1 mm distance away from device pins. This is very essential for optimised radiated emissions performance. Ensure that these capacitors are 0402 size so that they offer least inductance (ESL).
2. Bulk capacitors of atleast 10 µF must be placed on power converter input (V_{DD}) and output (V_{ISOOUT}) supply pins.
3. Traces on V_{DD} and GND1 must be symmetric till bypass capacitors. Similarly traces on V_{ISOOUT} and GND2 must be symmetric.
4. Place two 0402 size Ferrite beads (Part number: BLM15EX331SN1) on power supply pins, one between V_{ISOOUT} and V_{ISOIN} and the other between GND2 (11) and GISOIN(15), as shown in example PCB layout, so that any high frequency noise from power converter output sees a high impedance before it goes to other components on PCB.
5. Do not have any metal traces or ground pour within 4 mm of power converter output terminals V_{ISOOUT} (pin12) and GND2 (pin11). MODE pin is also in V_{ISOOUT} domain and should be shorted to either pin 11 or pin 12 for output voltage selection.
6. Common mode choke or ferrite beads on bus terminals (Y/Z/A/B) can minimise any high frequency noise that can couple of RS-485 bus cable which can act as antenna and amplify that noise. This will improve Radiated emissions performance on a system level.
7. Following the layout guidelines of EVM as much as possible is highly recommended for a low radiated emissions design. EVM Link is available in Related Documentation.

13.2 Layout Example

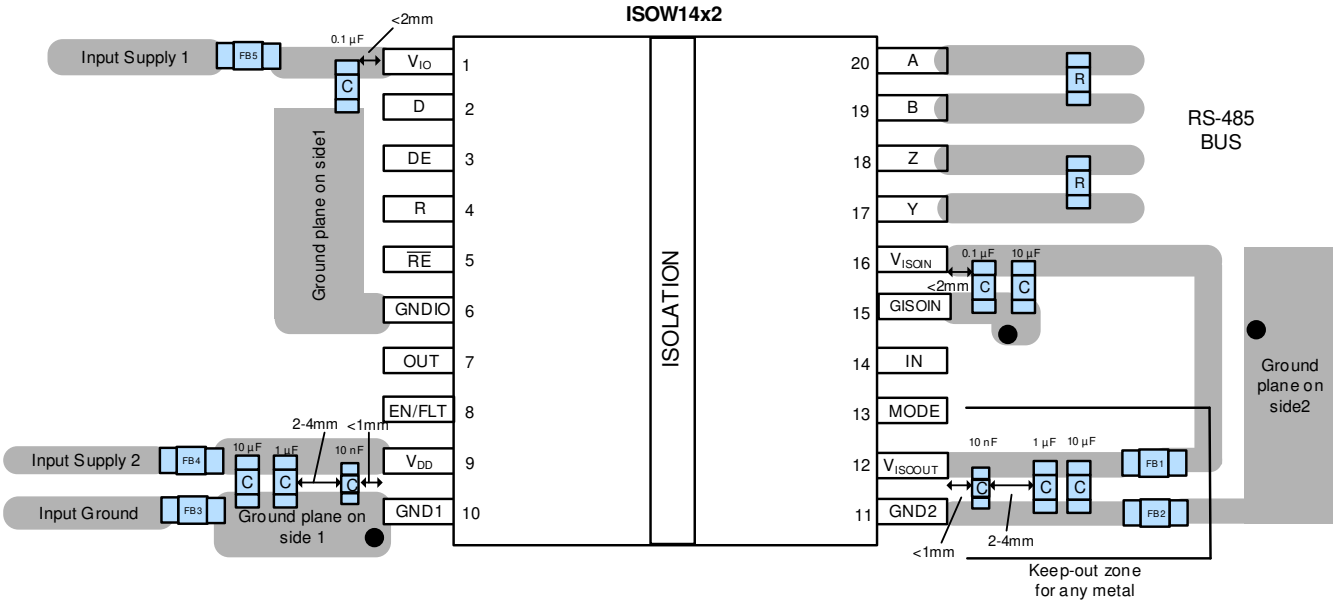


图 13-1. Layout example

14 Device and Documentation Support

14.1 Documentation Support

14.1.1 Related Documentation

For related documentation see the following:

- Texas Instruments, *Digital Isolator Design Guide*
- Texas Instruments, *Isolation Glossary*
- **ISOW1412DFM** Evaluation board

14.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

14.3 支持资源

TI E2E™ 支持论坛是工程师的重要参考资料，可直接从专家获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题可获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的《使用条款》。

14.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.
所有商标均为其各自所有者的财产。

14.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

14.6 术语表

TI 术语表　　本术语表列出并解释了术语、首字母缩略词和定义。

15 Mechanical, Packaging, and Orderable Information

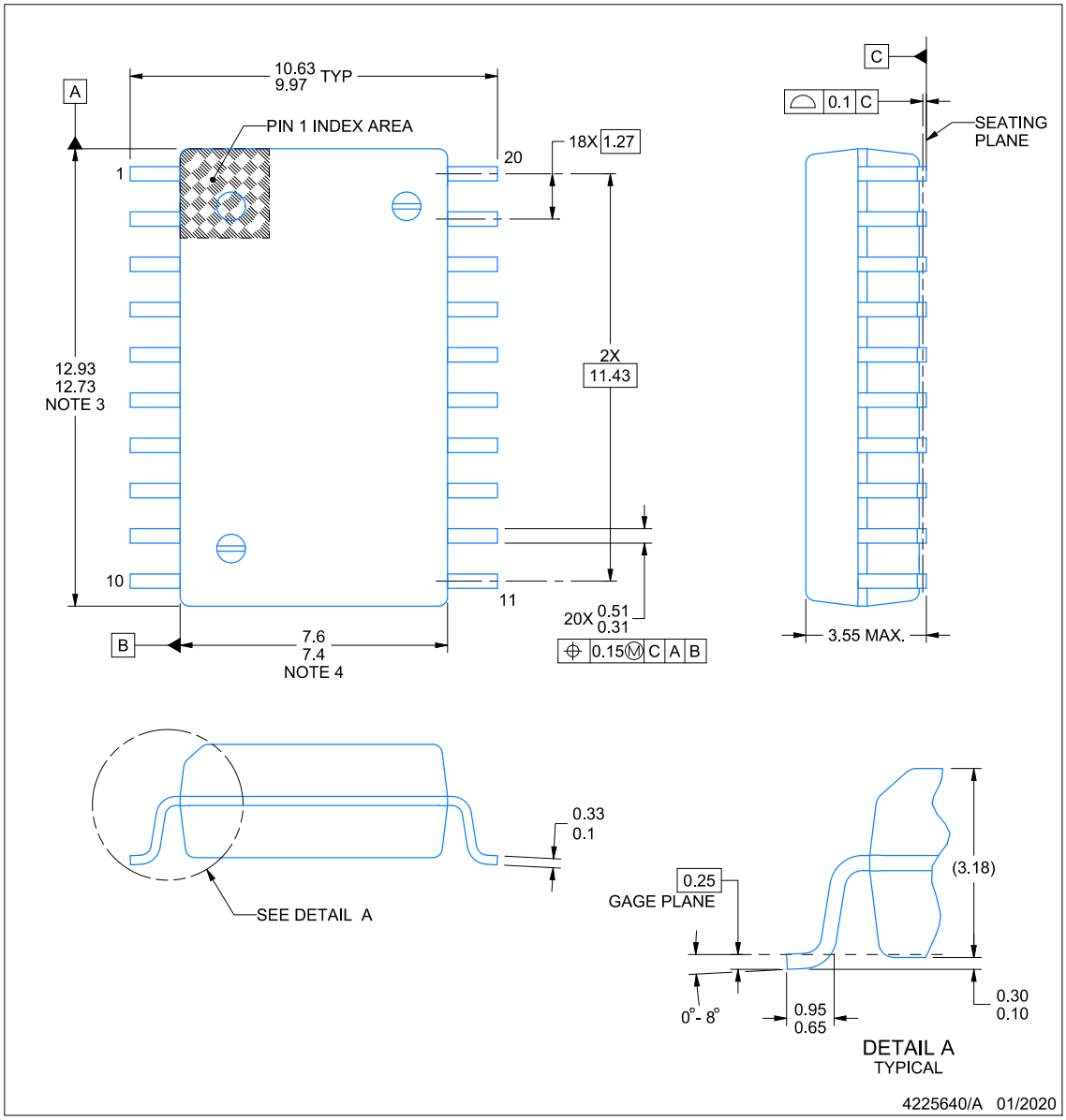
The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGE OUTLINE

DFM0020A

SOIC - 3.55 mm max height

SMALL OUTLINE PACKAGE



NOTES:

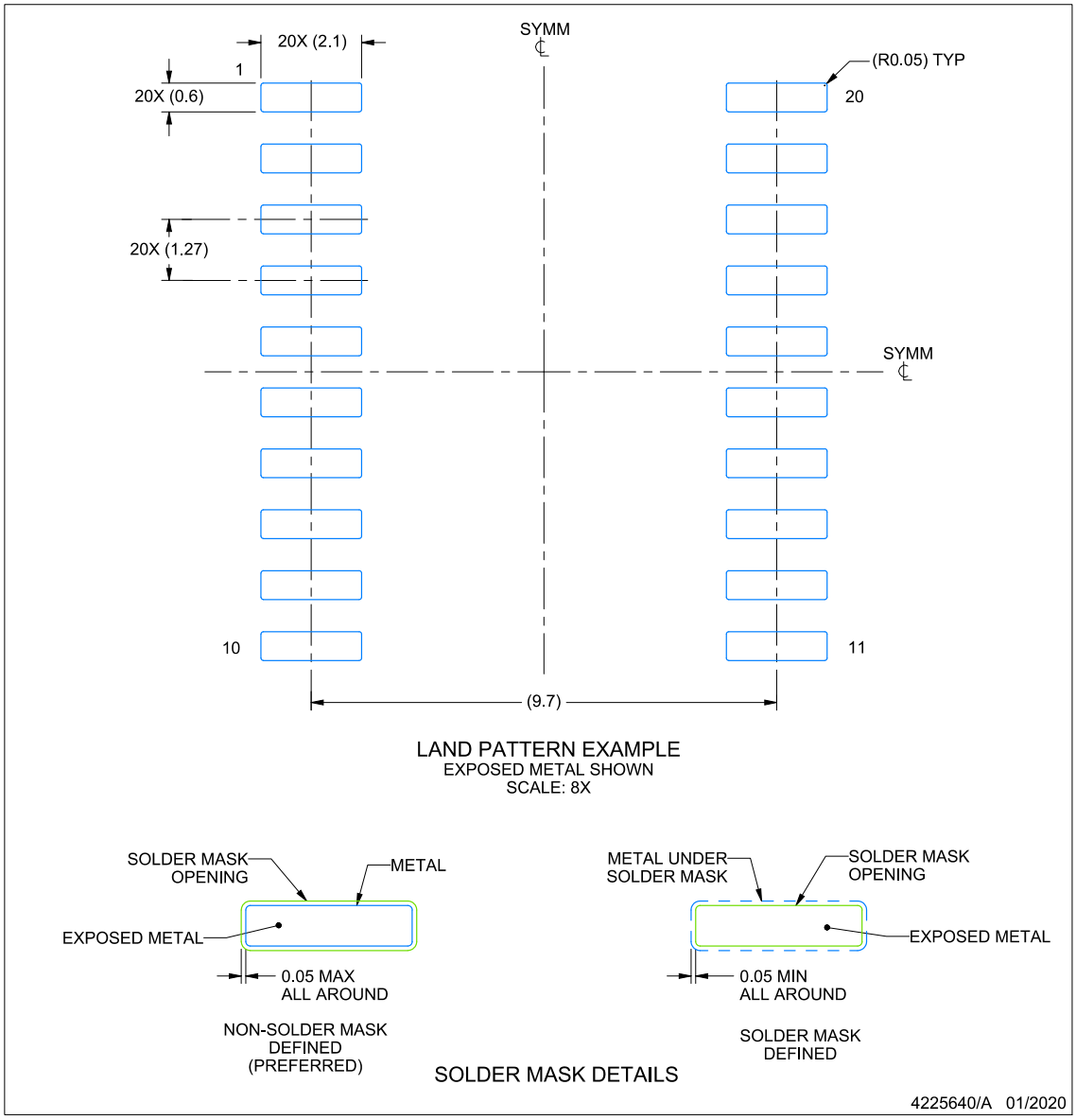
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Ref. JEDEC registration MS-013

EXAMPLE BOARD LAYOUT

DFM0020A

SOIC - 3.55 mm max height

SMALL OUTLINE PACKAGE



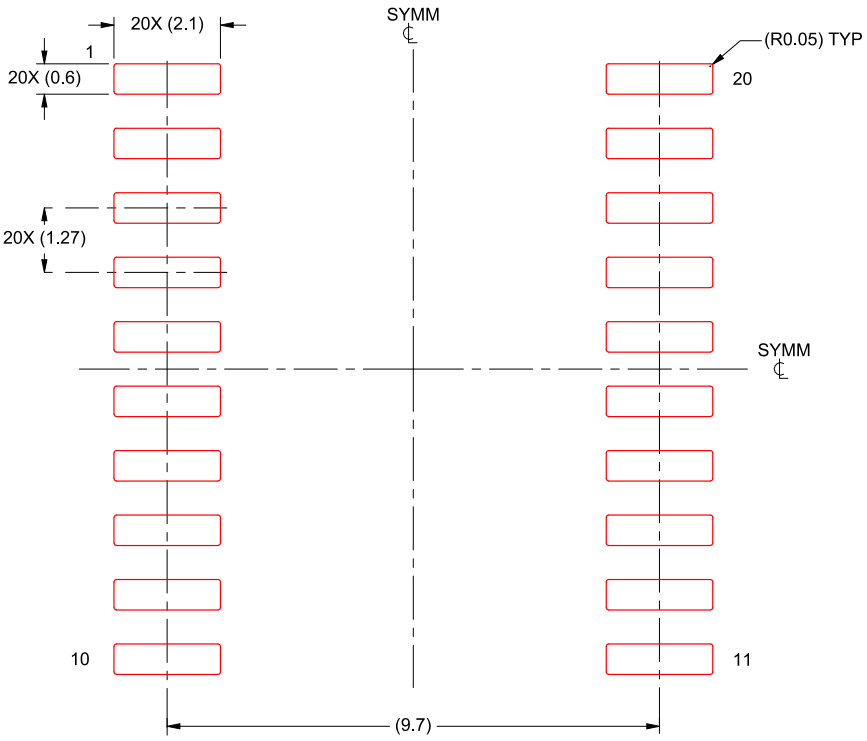
NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DFM0020A — **SOIC - 3.55 mm max height**

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 8X

4225640/A 01/2020

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
ISOW1412BDFMR	ACTIVE	SOIC	DFM	20	850	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 125	ISOW1412	Samples
ISOW1412DFMR	ACTIVE	SOIC	DFM	20	850	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 125	ISOW1412	Samples
ISOW1432BDFMR	ACTIVE	SOIC	DFM	20	850	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 125	ISOW1432	Samples
ISOW1432DFMR	ACTIVE	SOIC	DFM	20	850	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 125	ISOW1432	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

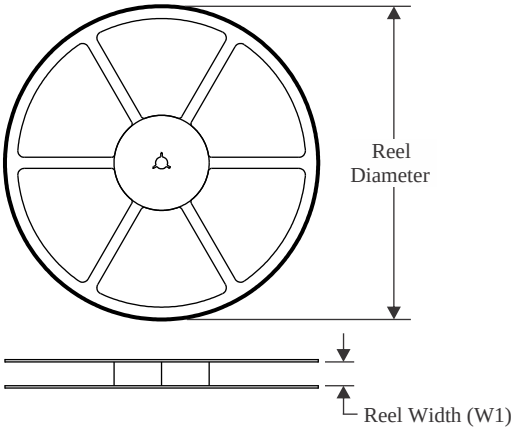
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals.
TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

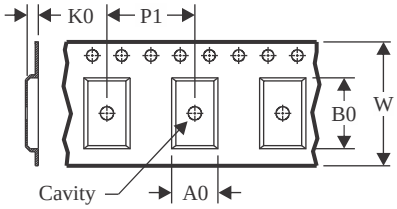
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

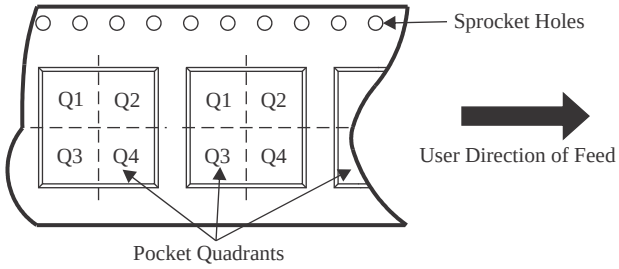


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

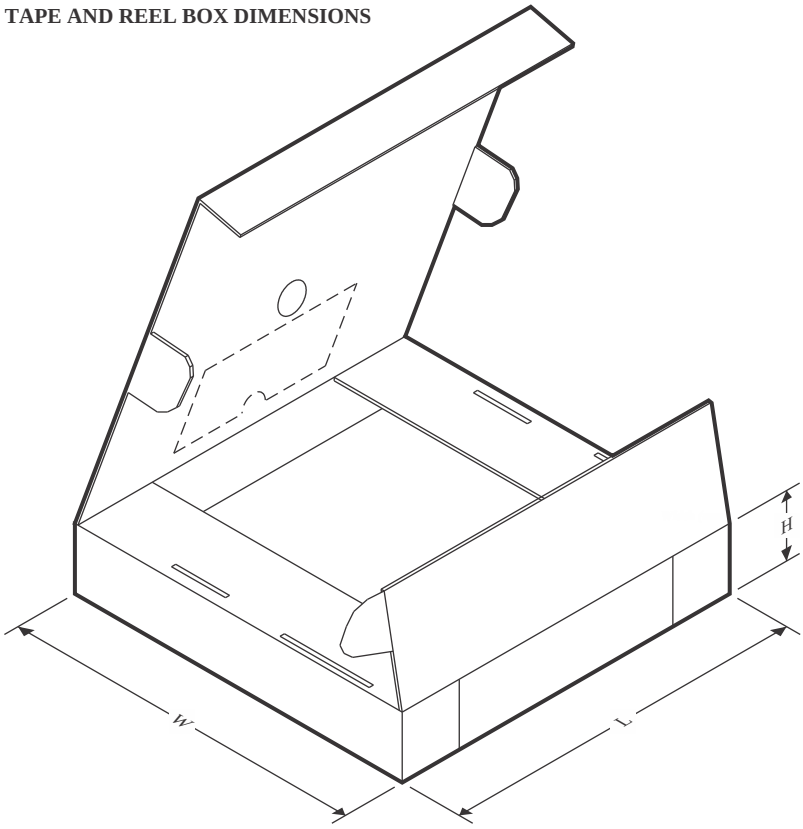
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ISOW1412BDFMR	SOIC	DFM	20	850	330.0	24.4	10.85	13.4	4.0	16.0	24.0	Q1
ISOW1412DFMR	SOIC	DFM	20	850	330.0	24.4	10.85	13.4	4.0	16.0	24.0	Q1
ISOW1432BDFMR	SOIC	DFM	20	850	330.0	24.4	10.85	13.4	4.0	16.0	24.0	Q1
ISOW1432DFMR	SOIC	DFM	20	850	330.0	24.4	10.85	13.4	4.0	16.0	24.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

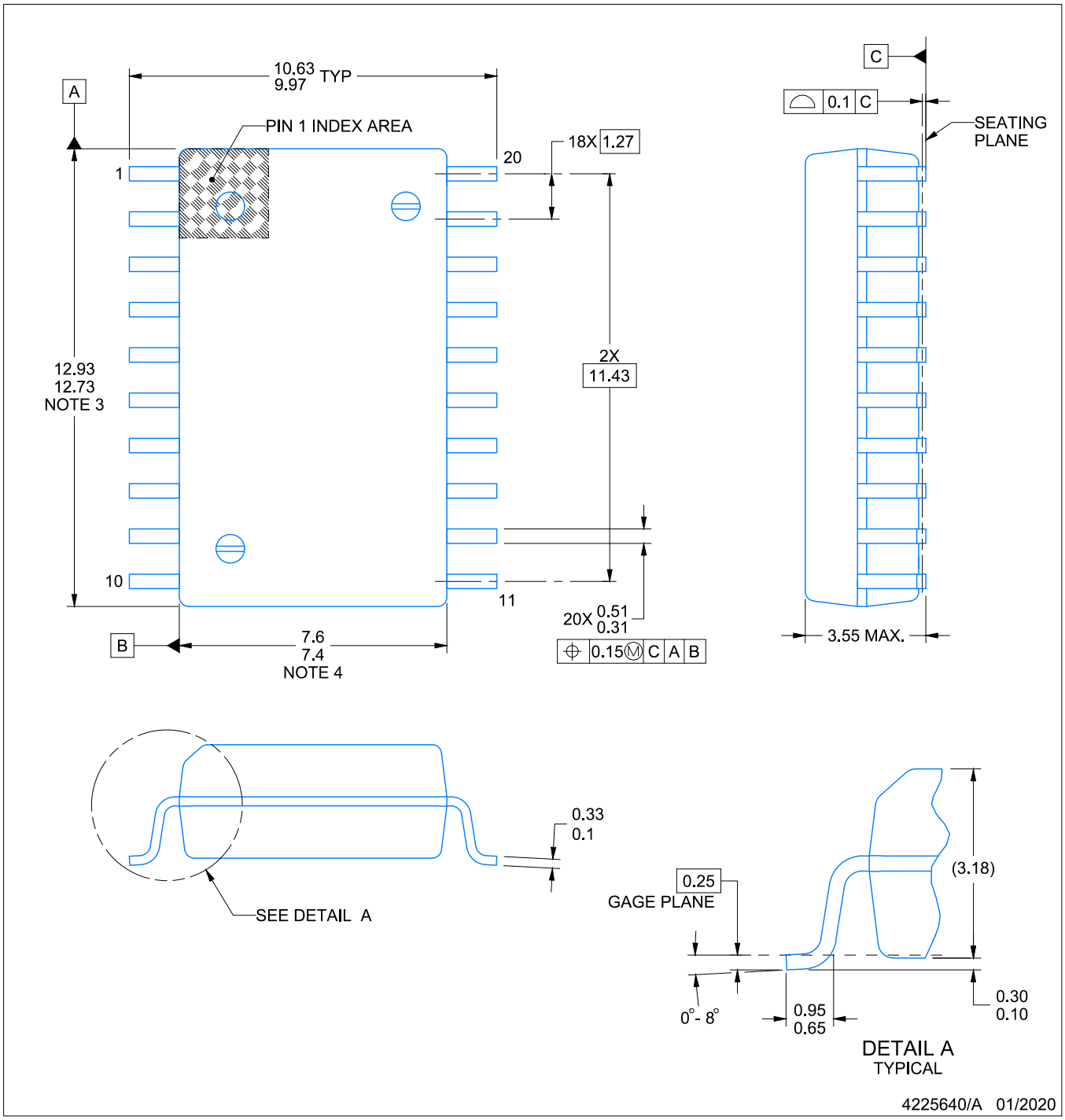
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ISOW1412BDFMR	SOIC	DFM	20	850	350.0	350.0	43.0
ISOW1412DFMR	SOIC	DFM	20	850	350.0	350.0	43.0
ISOW1432BDFMR	SOIC	DFM	20	850	350.0	350.0	43.0
ISOW1432DFMR	SOIC	DFM	20	850	350.0	350.0	43.0

PACKAGE OUTLINE

DFM0020A

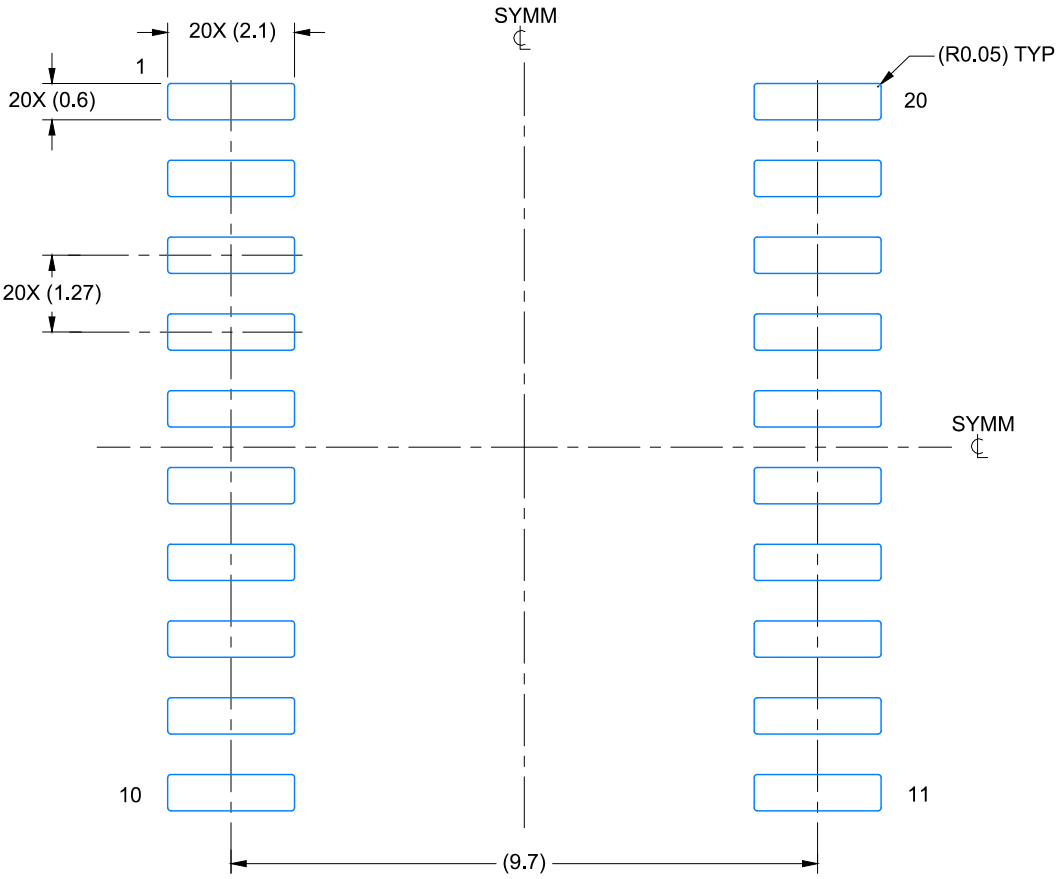
SOIC - 3.55 mm max height

SMALL OUTLINE PACKAGE

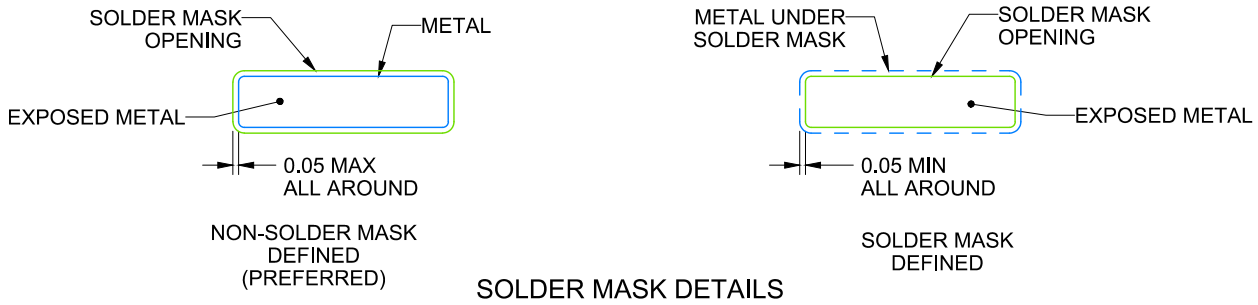


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Ref. JEDEC registration MS-013



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 8X

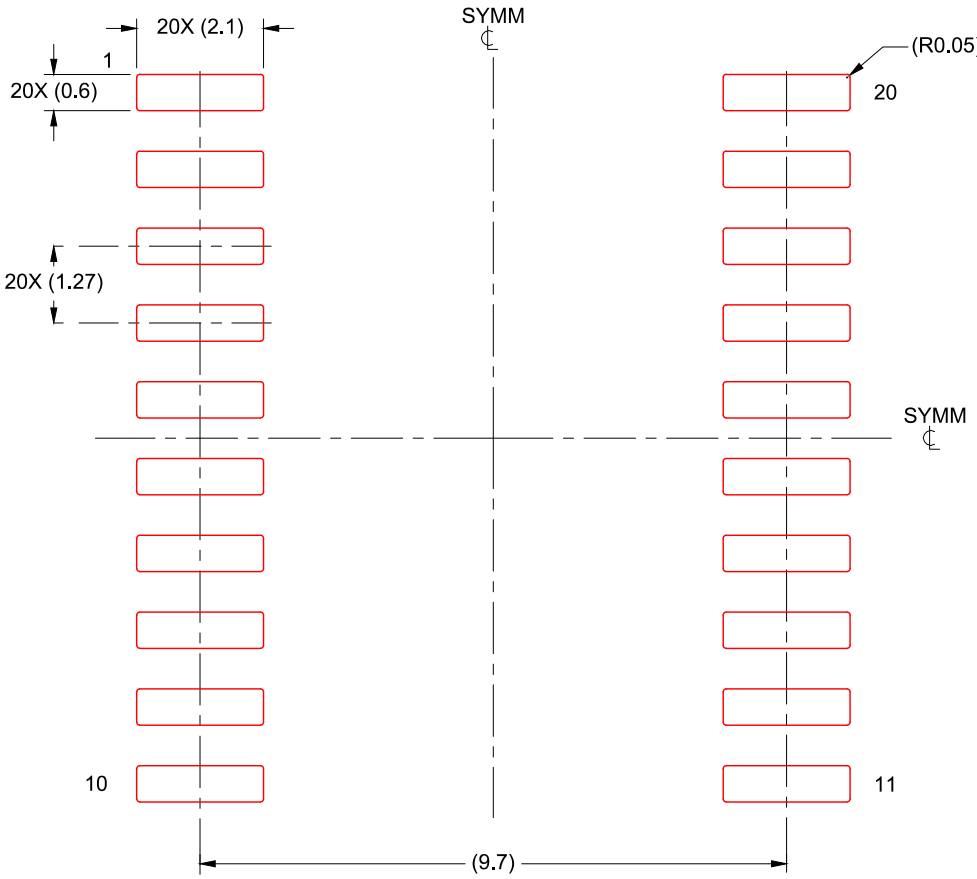


SOLDER MASK DETAILS

4225640/A 01/2020

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 8X

4225640/A 01/2020

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

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