# LM2101 具有 8V UVLO 的 107V、0.5A、0.8A 半桥驱动器

## 1 特性

- 可驱动两个采用半桥配置的 N 沟道 MOSFET
- 8-V GVDD 上的典型欠压锁定
- BST 上的最大绝对电压为 107V
- SH 上的 –19.5V 绝对最大负瞬态电压处理
- 0.5A/0.8A 峰值拉电流/灌电流
- 115ns 典型传播延迟

## 2 应用

- 无刷直流 (BLDC) 电机
- 永磁同步电机 (PMSM)
- 无线真空吸尘器
- 无线园艺工具和电动工具
- 电动自行车和电动踏板车
- 电池测试设备
- 离线不间断电源 (UPS)
- 通用 MOSFET 或 IGBT 驱动器

## 3 说明

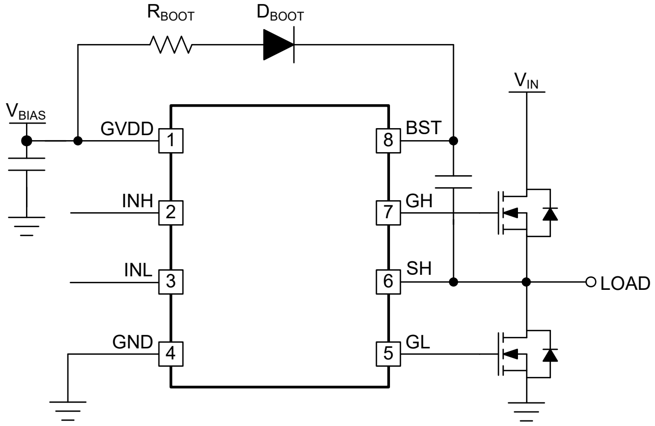
LM2101 是一款紧凑型高压栅极驱动器，专为驱动采用同步降压或半桥配置的高侧和低侧 N 沟道 MOSFET 而设计。

SH 引脚具有–1V 直流和 –19.5V 瞬态负电压处理能力，可提升高噪声应用中的系统稳健性。该器件采用小型热增强型 8 引脚 WSON 封装，可将驱动器放置在更靠近电机相位的位置，从而改善 PCB 布局。 LM2101 还采用与业界通用引脚排列兼容的 8 引脚 SOIC 封装。在低侧和高侧电源轨上均提供欠压锁定 (UVLO) 功能，以在上电和断电期间提供保护。

**器件信息**

| 器件型号 | 封装(1) | 封装尺寸（标称值） |
|---|---|---|
| LM2101 | D（SOIC，8） | 4.90mm × 3.91mm |
|  | DSG（WSON，8） | 2.00mm × 2.00mm |

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。



简化版应用示意图

## Table of Contents

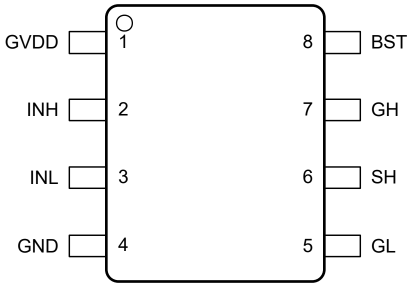
---

## 4 Revision History

注：以前版本的页码可能与当前版本的页码不同

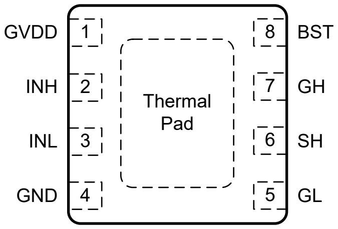
| **Changes from Revision * (February 2023) to Revision A (September 2023)** | **Page** |
|---|---|
| • 将“产品预发布”和“预告信息”更改为“量产数据” | 1 |

# 5 Pin Configuration and Functions



Not to scale

图 5-1. D Package, 8-Pin SOIC (Top View)



Not to scale

图 5-2. DSG Package, 8-Pin WSON (Top View)

表 5-1. Pin Functions

| PIN | | | DESCRIPTION |
|---|---|---|---|
| **NO.**[1] | **NAME** | **TYPE**[2] | |
| 1 | GVDD | P | Gate driver positive supply rail. Locally decouple to ground using low ESR and ESL capacitor located as close to IC as possible. |
| 2 | INH | I | High-side control input. The INH input is compatible with TTL and CMOS input thresholds. Unused INH input must be tied to ground and not left open. |
| 3 | INL | I | Low-side control input. The INL input is compatible with TTL and CMOS input thresholds. Unused INL input must be tied to ground and not left open. |
| 4 | GND | G | Ground. All signals are referenced to this ground. |
| 5 | GL | O | Low-side gate driver output. Connect to the gate of the low-side MOSFET or one end of external gate resistor, when used. |
| 6 | SH | P | High-side source connection. Connect to the negative terminal of the bootstrap capacitor and to the source of the high-side MOSFET. |
| 7 | GH | O | High-side gate driver output. Connect to the gate of the high-side MOSFET or one end of external gate resistor, when used. |
| 8 | BST | P | High-side gate driver positive supply rail. Connect the positive terminal of the bootstrap capacitor to BST and the negative terminal of the bootstrap capacitor to SH. The bootstrap capacitor must be placed as close to IC as possible. |

(1) For 8-pin WSON package, TI recommends that the exposed pad on the bottom of the package be soldered to ground plane on the PCB and the ground plane must extend out from underneath the package to improve heat dissipation.
(2) G = Ground, I = Input, O = Output, and P = Power

# 6 Specifications

## 6.1 Absolute Maximum Ratings

Over operating junction temperature range and all voltages are with respect to GND (unless otherwise noted).(1)

| | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| $V_{GVDD}$ | Low-side supply voltage | | –0.3 | 19.5 | V |
| $V_{BST}$ to $V_{SH}$ | High-side supply voltage | | –0.3 | 19.5 | V |
| $V_{INL}$, $V_{INH}$ | Input voltages on INL and INH | | –0.3 | 19.5 | V |
| $V_{GL}$ | Output voltage on GL | | –0.3 | GVDD + 0.3 | V |
| $V_{GH}$ | Output voltage on GH | | $V_{SH}$– 0.3 | $V_{BST}$ + 0.3 | V |
| $V_{SH}$ | Voltage on SH | DC | –1 | 95 | V |
| | | Repetitive pulse < 100 ns(2) | -19.5 | 95 | |
| $V_{BST}$ | Voltage on BST | | $V_{SH}$ | 107 | V |
| $T_J$ | Junction temperature | | –40 | 125 | °C |
| $T_{stg}$ | Storage temperature | Storage temperature | –65 | 150 | °C |

(1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. *Absolute Maximum Ratings* do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If used outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

(2) Values are verified by characterization and are not production tested.

## 6.2 ESD Ratings

| | | | VALUE | UNIT |
|---|---|---|---|---|
| $V_{(ESD)}$ | Electrostatic discharge | Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1) | ±1000 | V |
| | | Charged-device model (CDM), per JEDEC specification JESD22-C101(2) | ±250 | |

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

## 6.3 Recommended Operating Conditions

Over operating junction temperature range and all voltages are with respect to GND (unless otherwise noted).

| | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|
| $V_{GVDD}$ | Supply voltage | 9 | 12 | 18 | V |
| $V_{INL}$, $V_{INH}$ | Input voltage range | 0 | | $V_{GVDD}$ + 0.3 | V |
| $V_{BST}$ | Voltage on BST | $V_{SH}$ + 9 | | 105 | V |
| $V_{SH}$ | Voltage on SH (DC) | –1 | | $V_{BST} – V_{GVDD}$ | V |
| $V_{SH}$ | Voltage on SH (repetitive pulse < 100 ns)(1) | –18 | | $V_{BST} – V_{GVDD}$ | V |
| $SR_{SH}$ | Voltage slew rate on SH | | | 50 | V/ns |
| $T_J$ | Operating junction temperature | –40 | | 125 | °C |

(1) Values are verified by characterization and are not production tested.

## 6.4 Thermal Information

| THERMAL METRIC(1) | | LM2101 | LM2101 | UNIT |
|---|---|---|---|---|
| | | D (SOIC) | DSG (WSON) | |
| | | 8 PINS | 8 PINS | |
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance | 133.2 | 78.2 | °C/W |
| $R_{\theta JC(top)}$ | Junction-to-case (top) thermal resistance | 75.2 | 97.7 | °C/W |
| $R_{\theta JB}$ | Junction-to-board thermal resistance | 76.7 | 44.6 | °C/W |
| $\Psi_{JT}$ | Junction-to-top characterization parameter | 25.5 | 4.6 | °C/W |

## 6.4 Thermal Information （续）

| THERMAL METRIC[1] | | LM2101<br>D (SOIC)<br>8 PINS | LM2101<br>DSG (WSON)<br>8 PINS | UNIT |
|---|---|---|---|---|
| $\Psi_{JB}$ | Junction-to-board characterization parameter | 75.9 | 44.6 | °C/W |
| $R_{\theta JC(bot)}$ | Junction-to-case (bottom) thermal resistance | N/A | 9.9 | °C/W |

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report, SPRA953.

## 6.5 Electrical Characteristics

$V_{GVDD}$ = $V_{BST}$ = 12 V, GND = $V_{SH}$ = 0 V, No Load on GL or GH, $T_J$ = 25°C (unless otherwise noted).

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **SUPPLY CURRENTS** | | | | | | |
| $I_{GVDD}$ | GVDD quiescent current | $V_{INL}$ = $V_{INH}$ = 0 V | | 430 | | µA |
| $I_{DDO}$ | GVDD operating current | f = 50 kHz, $C_{LOAD}$ = 0 | | 0.56 | | mA |
| $I_{BST}$ | Total BST quiescent current | $V_{INL}$ = $V_{INH}$ = 0 V, VDD = 12 V | | 150 | | uA |
| $I_{BSTO}$ | Total BST operating current | f = 50 kHz, $C_{LOAD}$ = 0 | | 0.16 | | mA |
| $I_{BSTS}$ | BST to GND quiescent current | $V_{SH}$ = $V_{BST}$ = 95 V, GVDD = 12 V | | 33.3 | | µA |
| $I_{BSTSO}$ | BST to GND operating current | f = 50 kHz, $C_{LOAD}$ = 0 | | 0.07 | | mA |
| **INPUT** | | | | | | |
| $V_{HIT}$ | Input voltage high threshold | -40°C to 125°C | | 1.45 | 2 | V |
| $V_{LIT}$ | Input voltage low threshold | -40°C to 125°C | 0.8 | 1.3 | | V |
| $V_{IHYS}$ | Input voltage hysteresis | | | 0.15 | | V |
| $R_{IN}$ | Input pulldown resistance | $V_{IN}$ = 3 V | | 200 | | kΩ |
| **UNDERVOLTAGE PROTECTION (UVLO)** | | | | | | |
| $V_{GVDDR}$ | GVDD rising threshold | $V_{GVDDR}$ = $V_{GVDD}$ - GND, -40°C to 125°C | | 8.15 | 8.75 | V |
| $V_{GVDDF}$ | GVDD falling threshold | $V_{GVDDF}$ = $V_{GVDD}$ - GND, -40°C to 125°C | 6.75 | 7.7 | | V |
| $V_{DDHYS}$ | GVDD threshold hysteresis | | | 0.45 | | V |
| $V_{BSTR}$ | VBST rising threshold | $V_{BSTR}$ = $V_{BST}$ - $V_{SH,}$ -40°C to 125°C | | 7.6 | 8.5 | V |
| $V_{BSTF}$ | VBST falling threshold | $V_{BSTR}$ = $V_{BST}$ - $V_{SH,}$ -40°C to 125°C | 6.25 | 7.15 | | V |
| $V_{BSTHYS}$ | VBST threshold hysteresis | | | 0.45 | | V |
| **LO GATE DRIVER** | | | | | | |
| $V_{GL\_L}$ | Low level output voltage | $I_{GL}$ = 100 mA, $V_{GL\_L}$ = $V_{GL}$ – GND | | 0.25 | | V |
| $V_{GL\_H}$ | High level output voltage | $I_{GL}$ = -100 mA, $V_{GL\_H}$ = $V_{GVDD}$ – $V_{GL}$ | | 0.8 | | V |
| | Peak pullup current[1] | $V_{GL}$ = 0V | | 0.5 | | A |
| | Peak pulldown current[1] | $V_{GL}$ = 12V | | 0.8 | | A |
| **HO GATE DRIVER** | | | | | | |
| $V_{GH\_L}$ | Low level output voltage | $I_{GH}$ = 100 mA, $V_{GH\_L}$ = $V_{GH}$ – $V_{SH}$ | | 0.25 | | V |
| $V_{GH\_H}$ | High level output voltage | $I_{GH}$ = –100 mA, $V_{GH\_H}$ = $V_{BST}$ – $V_{GH}$ | | 0.8 | | V |
| | Peak pullup current[1] | $V_{GH}$ = 0V | | 0.5 | | A |
| | Peak pulldown current[1] | $V_{GH}$ = 12V | | 0.8 | | A |

(1) Parameter not tested in production.

## 6.6 Switching Characteristics

$V_{GVDD}$ = $V_{BST}$ = 12 V, GND = $V_{SH}$ = 0 V, No Load on GL or GH, $T_J$ = 25°C (unless otherwise noted).

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **PROPAGATION DELAYS** | | | | | | |
| $t_{DLFF}$ | VINL falling to VGL falling | $V_{INH}$ = $V_{INL}$ = 0-3 V, $C_{LOAD}$ = 0 pF. Time from 50% of the input to 90% of the output. | | 115 | | ns |

## 6.6 Switching Characteristics（续）

$V_{GVDD}$ = $V_{BST}$ = 12 V, GND = $V_{SH}$ = 0 V, No Load on GL or GH, $T_J$ = 25°C (unless otherwise noted).

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $t_{DHFF}$ | VINH falling to VGH falling | $V_{INH}$ = $V_{IN L}$= 0-3 V, $C_{LOAD}$ = 0 pF. Time from 50% of the input to 90% of the output. | | 115 | | ns |
| $t_{DLRR}$ | VINL rising to VGL rising | $V_{INH}$ = $V_{INL}$ = 0-3 V, $C_{LOAD}$ = 0 pF. Time from 50% of the input to 10% of the output. | | 115 | | ns |
| $t_{DHRR}$ | VINH rising to VGH rising | $V_{INH}$ = $V_{INL}$ = 0-3 V, $C_{LOAD}$ = 0 pF. Time from 50% of the input to 10% of the output. | | 115 | | ns |
| **DELAY MATCHING** | | | | | | |
| $t_{MON}$ | Delay from GL on to GH off | INL ON, INH OFF, $V_{INH}$ = $V_{INL}$ = 0-3 V | | | 30 | ns |
| $t_{MOFF}$ | Delay from GL off to GH on | INL OFF, INH ON, $V_{INH}$ = $V_{INL}$ = 0-3 V | | | 30 | ns |
| **OUTPUT RISE AND FALL TIME** | | | | | | |
| $t_{R\_GL}$ | GL | $C_{LOAD}$ = 1000 pF, $V_{INH}$ = $V_{INL}$ = 0-3 V | | 28 | | ns |
| $t_{R\_GH}$ | GH | $C_{LOAD}$ = 1000 pF, $V_{INH}$ = $V_{INL}$ = 0-3 V | | 28 | | ns |
| $t_{F\_GL}$ | GL | $C_{LOAD}$ = 1000 pF, $V_{INH}$ = $V_{INL}$ = 0-3 V | | 18 | | ns |
| $t_{F\_GH}$ | GH | $C_{LOAD}$ = 1000 pF, $V_{INH}$ = $V_{INL}$ = 0-3 V | | 18 | | ns |

## 6.7 Timing Diagrams

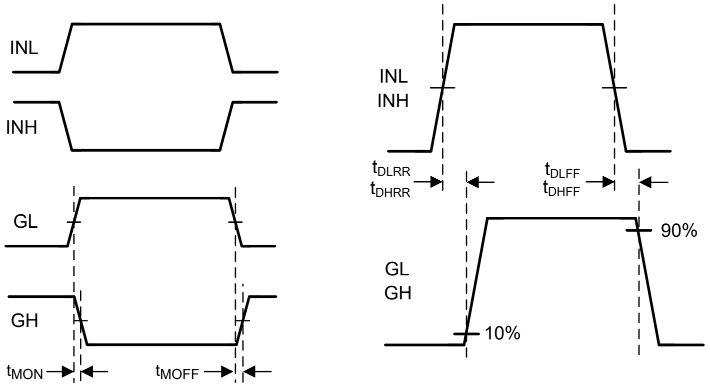


图 6-1. Timing Definition Diagram

## 6.8 Typical Characteristics

Unless otherwise specified, $V_{GVDD}$ = $V_{BST}$ = 12 V, GND = $V_{SH}$ = 0 V, No Load on GL or GH, $T_J$ = 25°C.

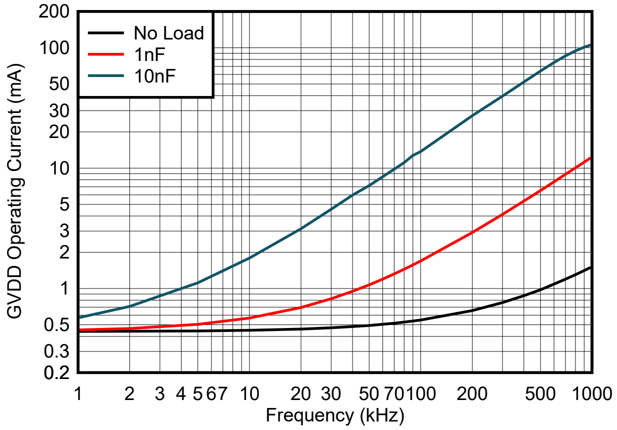


**图 6-2. GVDD Operating Current vs Frequency**

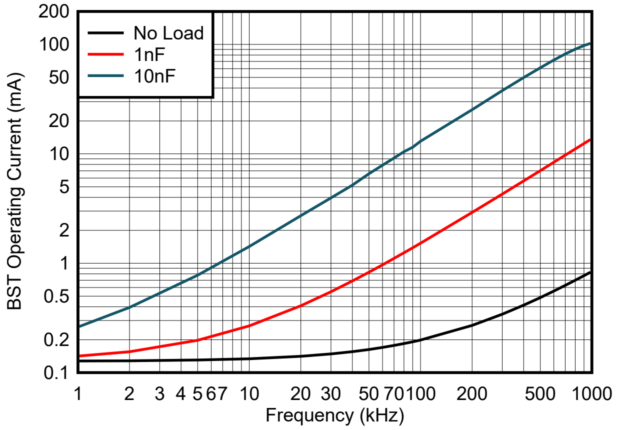


**图 6-3. BST Operating Current vs Frequency**

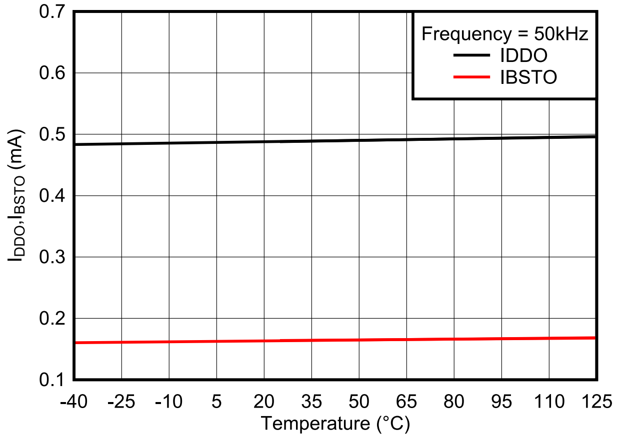


**图 6-4. Operating Currents vs Temperature**

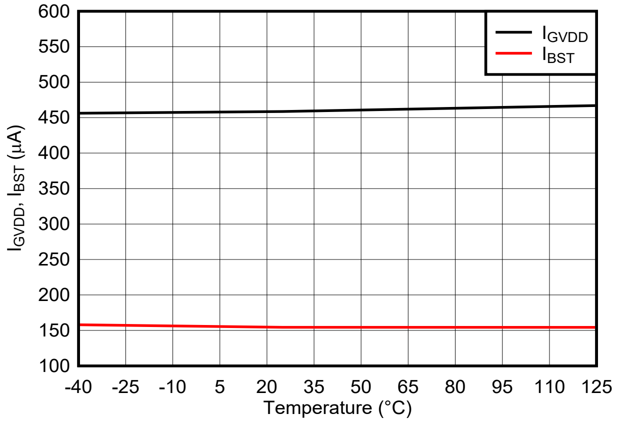


**图 6-5. Quiescent Currents vs Temperature**

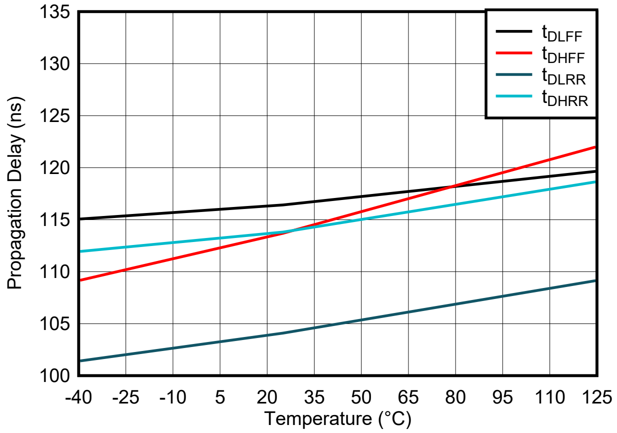


**图 6-6. Propagation Delays vs Temperature**

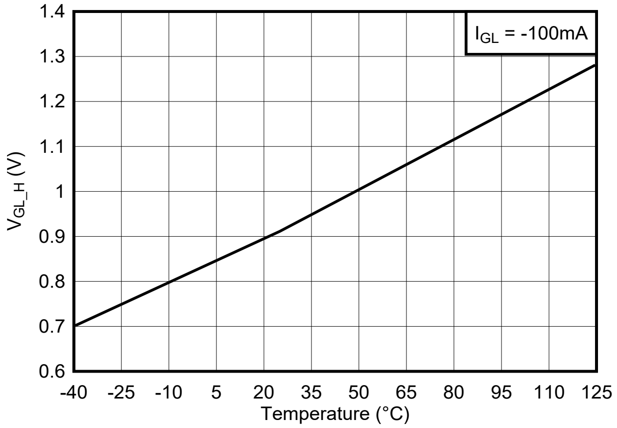


**图 6-7. GL Output High Voltage vs Temperature**

## 6.8 Typical Characteristics (continued)

Unless otherwise specified, $V_{GVDD} = V_{BST} = 12$ V, GND = $V_{SH} = 0$ V, No Load on GL or GH, $T_J = 25$°C.

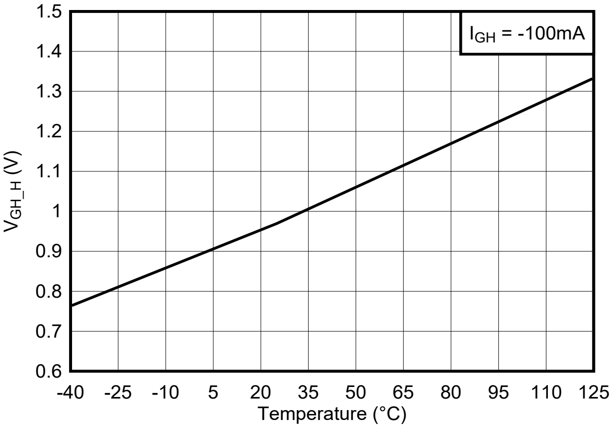


**图 6-8. GH Output High Voltage vs Temperature**

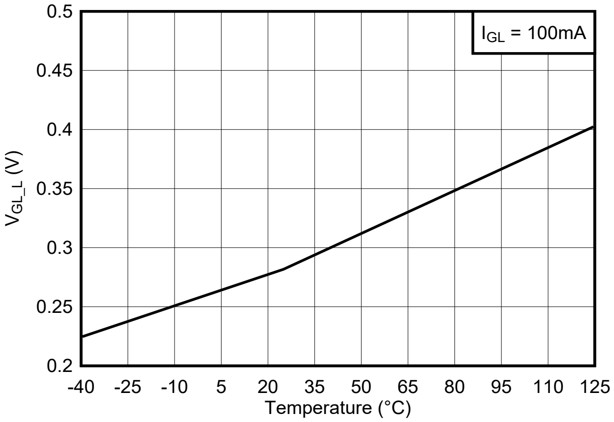


**图 6-9. GL Output Low Voltage vs Temperature**

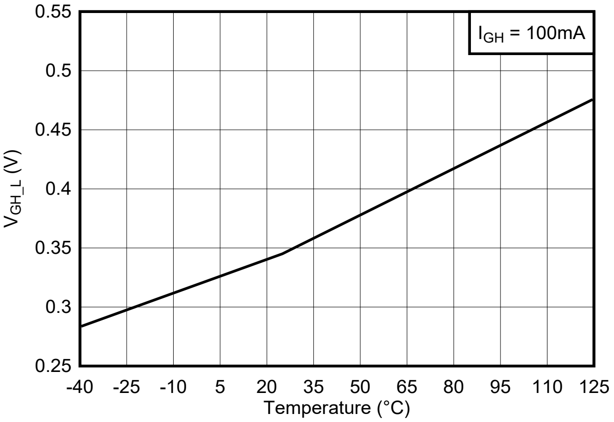


**图 6-10. GH Output Low Voltage vs Temperature**

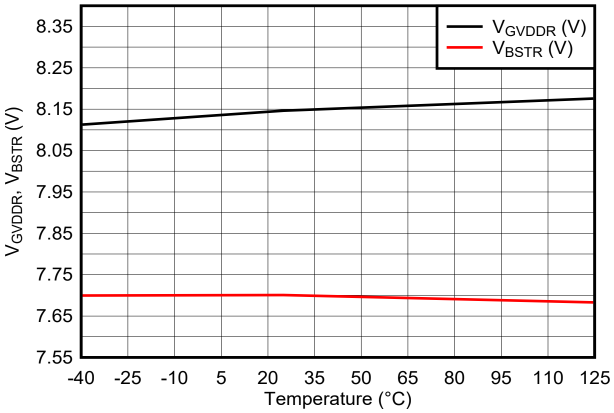


**图 6-11. GVDD and BST UVLO Thresholds vs Temperature**

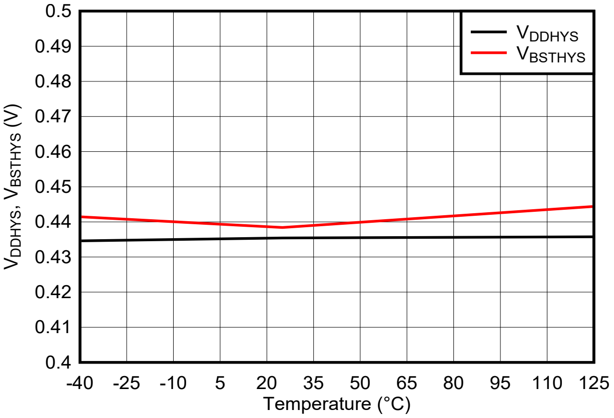


**图 6-12. GVDD and BST UVLO Hysteresis vs Temperature**

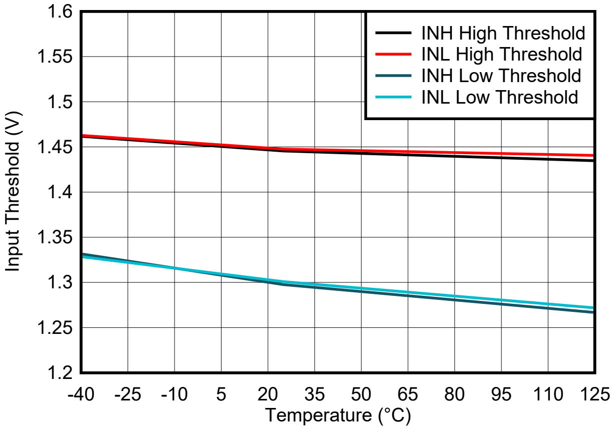


**图 6-13. Input Voltage Thresholds vs Temperature**

## 6.8 Typical Characteristics (continued)

Unless otherwise specified, $V_{GVDD}$ = $V_{BST}$ = 12 V, GND = $V_{SH}$ = 0 V, No Load on GL or GH, $T_J$ = 25°C.

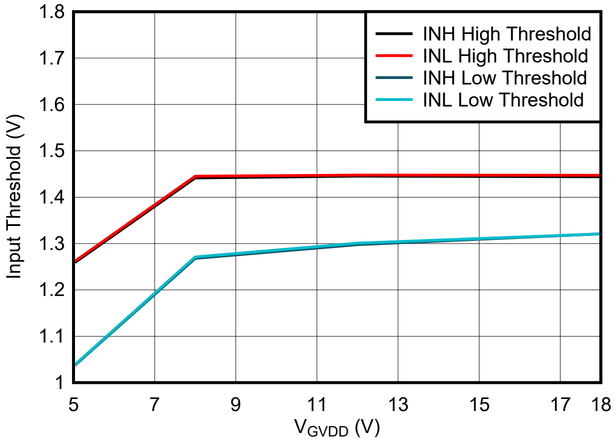


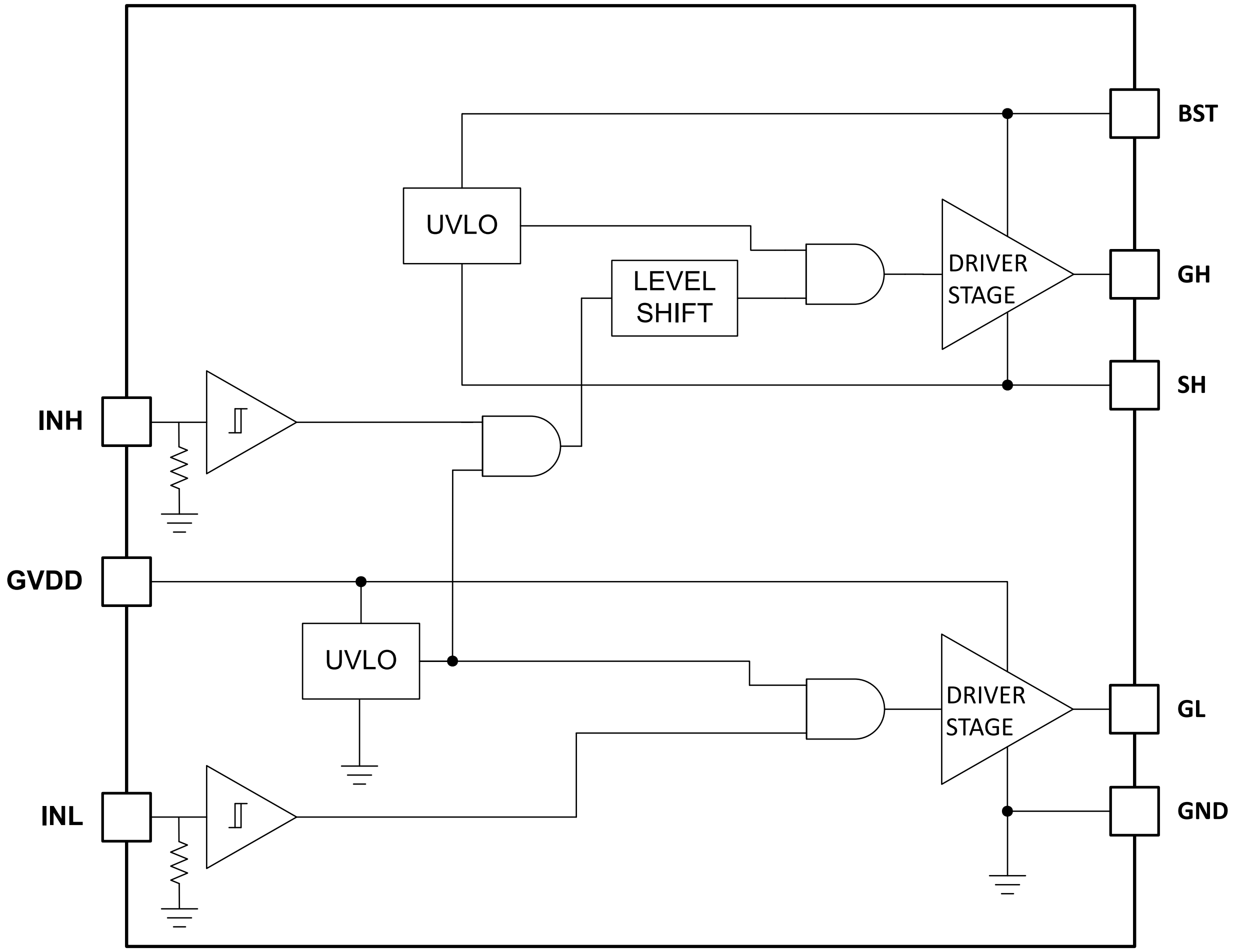
**图 6-14. Input Voltage Thresholds vs Supply Voltage**

# 7 Detailed Description

## 7.1 Overview

The LM2101 is a high-voltage gate driver designed to drive both the high-side and the low-side N-channel FETs in a synchronous buck or a half-bridge configuration. The two outputs are independently controlled with two TTL-compatible input signals. The device can also work with CMOS type control signals at its inputs as long as the signals meet the turn-on and turn-off threshold specifications of the LM2101. The floating high-side driver is capable of working with a recommended BST voltage up to 105 V. A robust level shifter operates at high speed while consuming low power and providing clean level transitions from the control logic to the high-side gate driver. Undervoltage lockout (UVLO) is provided on both the low-side and the high-side power rails.

## 7.2 功能方框图



## 7.3 Feature Description

### 7.3.1 Start-Up and UVLO

Both the high-side and the low-side driver stages include UVLO protection circuitry which monitors the supply voltage ($V_{GVDD}$) and the bootstrap capacitor voltage ($V_{BST\text{-}SH}$). The UVLO circuit inhibits each output until sufficient supply voltage is available to turn on the external MOSFETs, and the built-in UVLO hysteresis prevents chattering during supply voltage variations. When the supply voltage is applied to the GVDD pin of the device, both outputs are held low until $V_{GVDD}$ exceeds the UVLO threshold, typically 8 V. Any UVLO condition on the bootstrap capacitor ($V_{BST–SH}$) disables only the high-side output (GH).

表 7-1. GVDD UVLO Logic Operation

| CONDITION ($V_{BST- SH} > V_{BSTR}$) | INH | INL | GH | GL |
|---|---|---|---|---|
| $V_{GVDD}$ – GND < $V_{GVDDR}$ during device start-up | H | L | L | L |
| | L | H | L | L |
| | H | H | L | L |
| | L | L | L | L |
| $V_{GVDD}$ – GND < $V_{GVDDR}$ – $V_{DDHYS}$ after device start-up | H | L | L | L |
| | L | H | L | L |
| | H | H | L | L |
| | L | L | L | L |

表 7-2. BST UVLO Logic Operation

| CONDITION ($V_{GVDD} > V_{GVDDR}$) | INH | INL | GH | GL |
|---|---|---|---|---|
| $V_{BST\text{-}SH} < V_{BSTR}$ during device start-up | H | L | L | L |
| | L | H | L | H |
| | H | H | L | H |
| | L | L | L | L |
| $V_{BST\text{-}SH} < V_{BSTR} – V_{BSTHYS}$ after device start-up | H | L | L | L |
| | L | H | L | H |
| | H | H | L | H |
| | L | L | L | L |

### 7.3.2 Input Stages

The INL and INH inputs operate independent of each other. There is no fixed time de-glitch filter implemented at the inputs and therefore propagation delay and delay matching are not sacrificed. In other words, there is no built-in dead time. If the dead time between two outputs is desired then that shall be programmed through the microcontroller. A small filter at each of the inputs of the driver further improves system robustness in noise-prone applications. The inputs have internal pulldown resistors with typical value of 200 kΩ. Thus, when the inputs are floating, the outputs are held low.

### 7.3.3 Level Shift

The level shift circuit is the interface from the high-side input, which is a GND referenced signal, to the high-side driver stage, which is referenced to the switch node (SH). The level shift allows control of the GH output which is referenced to the SH pin and provides excellent delay matching with the low-side driver.

### 7.3.4 Output Stages

The output stages are the interface to the power MOSFETs in the power train. High slew rate, low resistance, and high peak current capability of both outputs allow for efficient switching of the power MOSFETs. The low-side output stage is referenced to GND and the high-side is referenced to SH.

### 7.3.5 SH Transient Voltages Below Ground

In most applications, the body diode of the external low-side power MOSFET clamps the SH node to ground. In some situations, board capacitance and inductance can cause the SH node to transiently swing several volts below ground, before the body diode of the external low-side MOSFET clamps this swing. The SH pin in the LM2101 is allowed to swing below ground as long as specifications are not violated and conditions mentioned in this section are followed.

SH must always be at a lower potential than GH. Pulling GH more negative than specified conditions can activate parasitic transistors which may result in excessive current flow from the BST supply. This may result in damage to the device. The same relationship is true with GL and GND. If necessary, a Schottky diode can be placed externally between GH and SH or GL and GND to protect the device from this type of transient. The diode must be placed as close to the device pins as possible in order to be effective.

Low ESR bypass capacitors from BST to SH and from GVDD to GND are essential for proper operation of the gate driver device. The capacitor should be located at the leads of the device to minimize series inductance. The peak currents from GL and GH can be quite large. Any series inductance with the bypass capacitor causes voltage ringing at the leads of the device which must be avoided for reliable operation.

## 7.4 Device Functional Modes

The device operates in normal mode and UVLO mode. See 节 7.3.1 for more information on UVLO operation mode. In normal mode, when the $V_{GVDD}$ and $V_{BST-SH}$ are above UVLO threshold, the output stage is dependent on the states of the INH and INL pins. The outputs GH and GL will be low if input state is floating.

**表 7-3. Input/Output Logic in Normal Mode of Operation**

| INH | INL | GH(1) | GL(2) |
|---|---|---|---|
| L | L | L | L |
| L | H | L | H |
| H | L | H | L |
| H | H | H | H |
| Floating | Floating | L | L |

(1) GH is measured with respect to SH.
(2) GL is measured with respect to GND.

# 8 Application and Implementation

---

**备注**

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

---

## 8.1 Application Information

To operate power MOSFETs at high switching frequencies and to reduce associated switching losses, a powerful gate driver is employed between the PWM output of controller and the gates of the power semiconductor devices. Also, gate drivers are indispensable when it is impossible for the PWM controller to directly drive the gates of the switching devices. With the advent of digital power, this situation is often encountered because the PWM signal from the digital controller is often a 3.3-V logic signal which cannot effectively turn on a power switch. Level-shift circuitry is needed to boost the 3.3-V signal to the gate-drive voltage (such as 12 V) to fully turn on the power device and minimize conduction losses. Traditional buffer drive circuits based on NPN and PNP bipolar transistors in totem-pole arrangement prove inadequate with digital power because they lack level-shifting capability. Gate drivers effectively combine both the level-shifting and buffer-drive functions. Gate drivers can also minimize the effect of high-frequency switching noise by being placed physically close to the power switch. Additionally, gate drivers can drive gate-drive transformers and control floating power-device gates, reducing the controller's power dissipation and thermal stress by moving the gate-charge power losses into the driver.

## 8.2 Typical Application

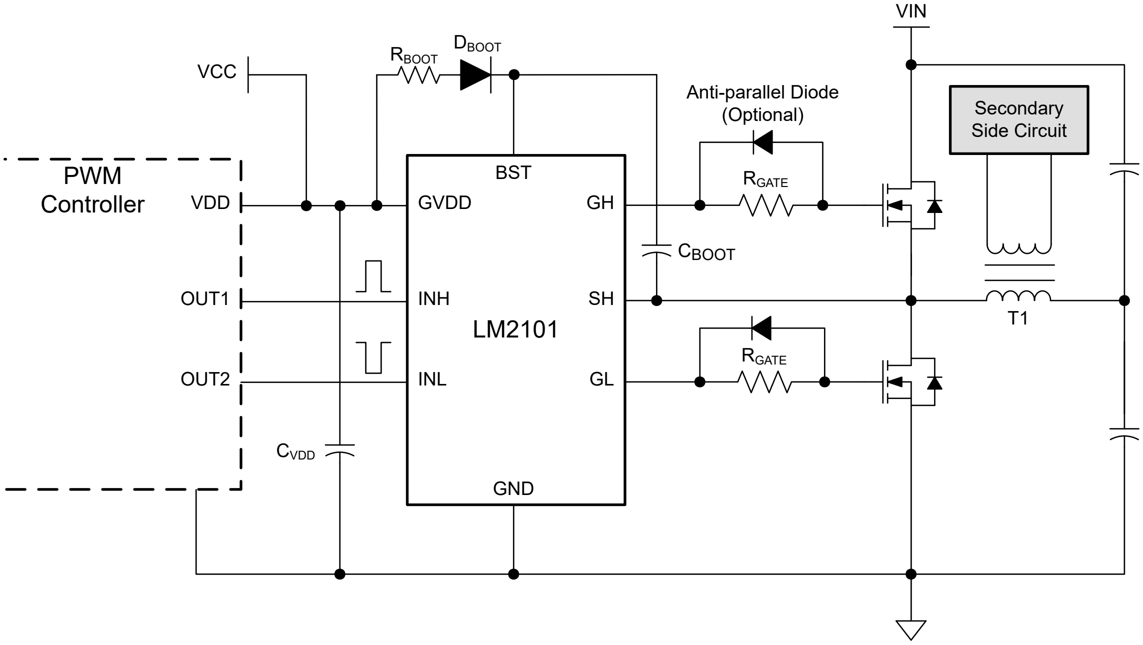


图 8-1. LM2101 Driving MOSFETs in a Half-Bridge Converter

### 8.2.1 Design Requirements

表 8-1 lists the design parameters of the LM2101.

**表 8-1. Design Example**

| PARAMETER | VALUE |
|---|---|
| Gate Driver | LM2101 |
| MOSFET | CSD19534KCS |
| $V_{DD}$ | 12 V |
| $Q_G$ | 17 nC |
| $f_{SW}$ | 50 kHz |

### 8.2.2 Detailed Design Procedure

#### *8.2.2.1 Select External Bootstrap Diode and Its Series Resistor*

An external bootstrap diode between GVDD pin and BST pin is required to allow the bootstrap capacitor to be charged from GVDD pin every cycle when the low-side MOSFET turns on. The charging of the capacitor involves high-peak currents, and therefore, transient power dissipation in the bootstrap diode may be significant. The reverse recovery time of the bootstrap diode must be very small to achieve a reduction in reverse recovery losses. Both the diode conduction losses and reverse recovery losses contribute to the total losses in the gate driver and must be considered in calculation the gate driver's power dissipation.

In order to minimize losses associated with the reverse recovery properties of the diode and ground noise bouncing, a fast recovery diode or Schottky diode with low forward voltage drop and low junction capacitance is recommended. Using Schottky diodes reduce the risk associated with charge supplied back to the gate driver supply from the bootstrap capacitor and minimize leakage current. When the SH pin (switch node) is pulled to a higher voltage, the diode must be able reverse bias fast enough to block any charges from the bootstrap capacitor to the GVDD supply. This bootstrap diode should be carefully chosen such that it is capable of handling the peak transient currents during start-up, and such that its voltage rating is higher than the system DC-link voltage with enough margins.

A bootstrap resistor $R_{BOOT}$ in series with the bootstrap diode is recommended to reduce the inrush current in $D_{BOOT}$ and limit the ramp up slew rate of voltage of $V_{BST\text{-}SH}$ during each switching cycle, especially when the SH pin has excessive negative transient voltage. $R_{BOOT}$ recommended value is between 2 Ω and 10 Ω depending on diode selection. A current limiting resistor of 2.2 Ω is selected to limit inrush current of bootstrap diode, and the estimated peak current on the $D_{Boot}$ is shown in 方程式 1.

$$I_{Dboot(pk)} = \frac{V_{GVDD} - V_{DH}}{R_{BOOT}} = \frac{12V - 1V}{2.2\Omega} = 5A \quad (1)$$

where

- $V_{DH}$ is the bootstrap diode forward voltage drop

#### *8.2.2.2 Select Bootstrap and GVDD Capacitor*

The bootstrap capacitor must maintain the $V_{BST\text{-}SH}$ voltage above the UVLO threshold for normal operation. Calculate the maximum allowable drop across the bootstrap capacitor with 方程式 2.

$$\Delta V_{BST} = V_{GVDD} - V_{DH} - V_{BSTL} = 12V - 1V - 8.05V = 2.95V \quad (2)$$

where

- $V_{GVDD}$ = Supply voltage of the gate drive IC
- $V_{DH}$ = Bootstrap diode forward voltage drop
- $V_{BSTL}$ = BST falling threshold ($V_{BSTR(max)}$ - $V_{BSTHYS}$)

Then, the total charge needed per switching cycle is estimated by 方程式 3.

$$Q_{TOTAL} = Q_G + I_{BSTS} \times \frac{D_{MAX}}{f_{SW}} + \frac{I_{BST}}{f_{SW}} = 17nC + 33.3\mu A \times \frac{0.95}{50kHz} + \frac{150\mu A}{50kHz} = 20nC \quad (3)$$

where

- $Q_G$ = Total MOSFET gate charge
- $I_{BSTS}$ = BST to VSS leakage current
- $D_{Max}$ = Converter maximum duty cycle
- $I_{BST}$ = BST quiescent current

Next, use 方程式 4 to estimate the minimum bootstrap capacitor value.

$$C_{BOOT\ (MIN)} = \frac{Q_{TOTAL}}{\Delta V_{BST}} = \frac{20nC}{2.95V} = 6.8nF \quad (4)$$

In practice, the value of the $C_{Boot}$ capacitor must be greater than calculated to allow for situations where the power stage may skip pulse due to load transients. 方程式 5 can be used to estimate the recommended bootstrap capacitance based on the maximum bootstrap voltage ripple desired for a specific application.

$$C_{BOOT} > \frac{Q_{TOTAL}}{\Delta V_{BST\_RIPPLE}} \quad (5)$$

where

- $\Delta V_{BST\_RIPPLE}$ = Maximum allowable voltage drop across the bypass capacitor based on system requirements

TI recommends having enough margins and to place the bootstrap capacitor as close to the BST and SH pins as possible.

$$C_{BOOT} = 100\ nF \quad (6)$$

As a general rule, the local $V_{GVDD}$ bypass capacitor must be 10 times greater than the value of $C_{BOOT}$, as shown in 方程式 7.

$$C_{GVDD} = 1\ \mu F \quad (7)$$

The bootstrap and bias capacitors must be ceramic types with X7R dielectric. The voltage rating must be twice that of the maximum $V_{GVDD}$ considering capacitance tolerances once the devices have a DC bias voltage across them and to ensure long-term reliability.

#### *8.2.2.3 Select External Gate Driver Resistor*

The external gate driver resistor, $R_{GATE}$, is sized to reduce ringing caused by parasitic inductances and capacitances and also to limit the current coming out of the gate driver.

The peak GH pullup current is calculated in 方程式 8.

$$I_{GHH} = \frac{V_{GVDD} - V_{DH}}{R_{GHH} + R_{GATE} + R_{GFET\_INT}} \quad (8)$$

where

- $I_{GHH}$ = GH Peak pullup current
- $V_{DH}$ = Bootstrap diode forward voltage drop
- $R_{GHH}$ = Gate driver internal GH pullup resistance, estimated from the testing conditions, that is $R_{GHH}$ = $V_{GH\_H}$ / $I_{GH}$
- $R_{GATE}$ = External gate drive resistance
- $R_{GFET\_INT}$ = MOSFET internal gate resistance, provided by transistor data sheet

Similarly, the peak GH pulldown current is shown in 方程式 9.

$$I_{GHL} = \frac{V_{GVDD} - V_{DH}}{R_{GHL} + R_{GATE} + R_{GFET\_INT}} \quad (9)$$

where

- $R_{GHL}$ is the GH pulldown resistance

The peak GL pullup current is shown in 方程式 10.

$$I_{GLH} = \frac{V_{GVDD}}{R_{GLH} + R_{GATE} + R_{GFET\_INT}} \quad (10)$$

where

- $R_{GLH}$ is the GL pullup resistance

The peak GL pulldown current is shown in 方程式 11.

$$I_{GLL} = \frac{V_{GVDD}}{R_{GLL} + R_{GATE} + R_{GFET\_INT}} \quad (11)$$

where

- $R_{GLL}$ is the GL pulldown resistance

For some scenarios, if the applications require fast turnoff, an anti-paralleled diode on $R_{Gate}$ could be used to bypass the external gate drive resistor and speed up turnoff transition.

#### *8.2.2.4 Estimate the Driver Power Loss*

The total driver IC power dissipation can be estimated through the following components.

1. Static power losses, $P_{QC}$, due to quiescent currents $I_{GVDD}$ and $I_{BST}$ is shown in 方程式 12.

   $$P_{QC} = V_{GVDD} \times I_{GVDD} + (V_{GVDD} - V_F) \times I_{BST} = 12V \times 0.43mA + (12V - 1V) \times 0.15mA = 6.8mW \quad (12)$$

2. Level-shifter losses, $P_{IBSTS}$, due high-side leakage current $I_{BSTS}$ is shown in 方程式 13.

   $$P_{IBSTS} = V_{BST} \times I_{BSTS} \times D = 72V \times 0.033mA \times 0.95 = 2.26mW \quad (13)$$

   where

   - D is the high-side switch duty cycle

3. Dynamic losses, $P_{QG1\&2}$, due to the FETs gate charge $Q_G$ as shown in 方程式 14.

   $$P_{QG1\&2} = 2 \times V_{GVDD} \times Q_G \times f_{SW} \times \frac{R_{GD\_R}}{R_{GD\_R} + R_{GATE} + R_{GFET\_INT}} = 2 \times 12V \times 17nC \times 50kHz \times \frac{5.25\Omega}{5.25\Omega + 4.7\Omega + 2.2\Omega} = 8.8mW \quad (14)$$

   where

   - $Q_G$ = Total FETs gate charge
   - $f_{SW}$ = Switching frequency
   - $R_{GD\_R}$ = Average value of pullup and pulldown resistor
   - $R_{GATE}$ = External gate drive resistor
   - $R_{GFET\_INT}$ = Internal FETs gate resistor

4. Level-shifter dynamic losses, $P_{LS}$, during high-side switching due to required level-shifter charge on each switching cycle. For this example it is assumed that value of parasitic charge $Q_P$ is 2.5 nC, as shown in 方程式 15.

   $$P_{LS} = V_{BST} \times Q_P \times f_{SW} = 72V \times 2.5nC \times 50kHz = 9mW \quad (15)$$

In this example, the sum of all the losses is 27 mW as a total gate driver loss. For gate drivers that include bootstrap diode, one should also estimate losses in the bootstrap diode. Diode forward conduction loss is computed as product of average forward voltage drop and average forward current.

方程式 16 estimates the maximum allowable power loss of the device for a given ambient temperature.

$$P_{MAX} = \frac{T_J - T_A}{R_{\theta JA}} \tag{16}$$

where

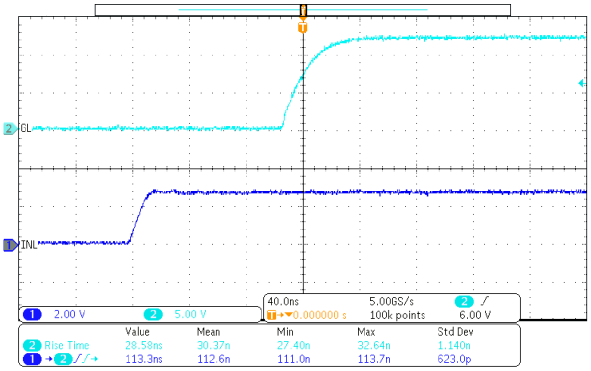
- $P_{MAX}$ = Maximum allowed power dissipation in the gate driver device
- $T_J$ = Junction temperature
- $T_A$ = Ambient temperature
- $R_{\theta JA}$ = Junction-to-ambient thermal resistance

The thermal metrics for the driver package is summarized in the *Thermal Information* table of the data sheet. For detailed information regarding the thermal information table, refer to the Texas Instruments application note entitled *Semiconductor and IC Package Thermal Metrics*.

### 8.2.3 Application Curves

图 8-2 and 图 8-3 show the rise times and turn-on propagation delays for the low side driver and the high side driver respectively. Likewise, 图 8-4 and 图 8-5 show the fall times and turn-off propagation delays. Each channel (INH, INL, GH, and GL) is labeled and displayed on the left hand of the waveforms.

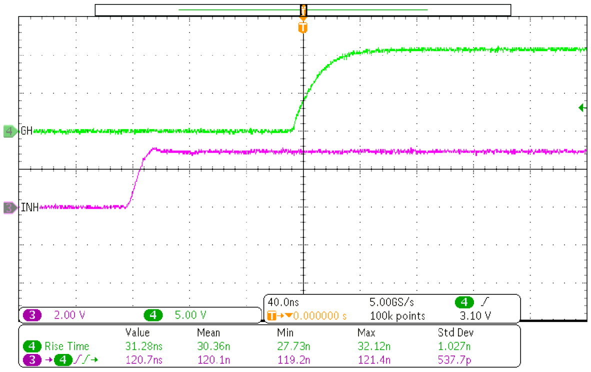
The testing condition: load capacitance is 1 nF, gate resistor is 4 Ω, $V_{DD}$ = 12 V, $f_{SW}$ = 50 kHz.



| | Value | Mean | Min | Max | Std Dev |
|---|---|---|---|---|---|
| 2 Rise Time | 28.58ns | 30.37n | 27.40n | 32.64n | 1.140n |
| 1 → 2 ∕∕→ | 113.3ns | 112.6n | 111.0n | 113.7n | 623.0p |

$C_L$ = 1 nF   $R_G$ = 4 Ω | $V_{GVDD}$ = 12 V   $f_{SW}$ = 50 kHz

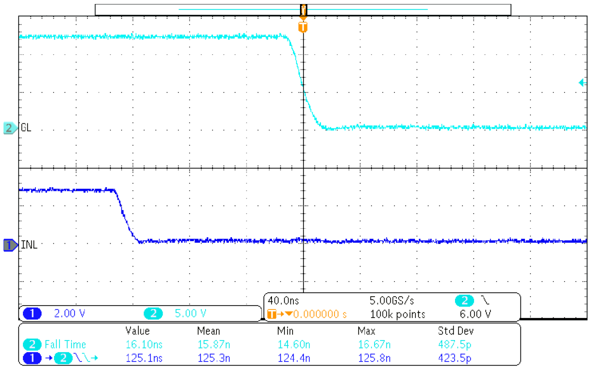
**图 8-2. GL Rise Time and INL to GL Turn-on Propagation Delay**



| | Value | Mean | Min | Max | Std Dev |
|---|---|---|---|---|---|
| 4 Rise Time | 31.28ns | 30.36n | 27.73n | 32.12n | 1.027n |
| 3 → 4 ∕∕→ | 120.7ns | 120.1n | 119.2n | 121.4n | 537.7p |

$C_L$ = 1 nF   $R_G$ = 4 Ω | $V_{GVDD}$ = 12 V   $f_{SW}$ = 50 kHz

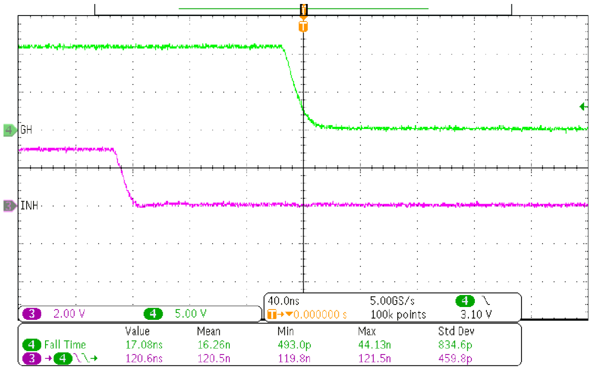
**图 8-3. GH Rise Time and INH to GH Turn-on Propagation Delay**



| | Value | Mean | Min | Max | Std Dev |
|---|---|---|---|---|---|
| 2 Fall Time | 16.10ns | 15.87n | 14.60n | 16.67n | 487.5p |
| 1 → 2 ╲╲→ | 125.1ns | 125.3n | 124.4n | 125.8n | 423.5p |

$C_L$ = 1 nF   $R_G$ = 4 Ω | $V_{DD}$ = 12 V   $f_{SW}$ = 50 kHz

**图 8-4. GL Fall Time and INL to GL Turn-off Propagation Delay**



| | Value | Mean | Min | Max | Std Dev |
|---|---|---|---|---|---|
| 4 Fall Time | 17.08ns | 16.26n | 493.0p | 44.13n | 834.6p |
| 3 → 4 ╲╲→ | 120.6ns | 120.5n | 119.8n | 121.5n | 459.8p |

$C_L$ = 1 nF   $R_G$ = 4 Ω | $V_{DD}$ = 12 V   $f_{SW}$ = 50 kHz

**图 8-5. GH Fall Time and INH to GH Turn-off Propagation Delay**

## 9 Power Supply Recommendations

The recommended bias supply voltage range for LM2101 is from 9 V to 18 V. The lower end of this range is governed by the internal undervoltage lockout (UVLO) protection feature of the $V_{GVDD}$ supply circuit blocks. The upper end of this range is driven by the 18-V recommended maximum voltage rating of the GVDD pin. It is recommened that the voltage on GVDD pin is lower than the maximum recommended voltage to account for transient voltage spikes.

The UVLO protection feature also involves a hysteresis function. This means that once the device is operating in normal mode, if the $V_{GVDD}$ voltage drops, the device continues to operate in normal mode as long as the voltage drop does not exceed the hysteresis specification, $V_{DDHYS}$. If the voltage drop is more than hysteresis specification, the device shuts down. Therefore, while operating at or near the 9-V range, the voltage ripple on the auxiliary power supply output must be smaller than the hysteresis specification of LM2101 to avoid triggering device-shutdown.

A local bypass capacitor must be placed between the GVDD and GND pins and this capacitor must be located as close to the device as possible. A low-ESR, ceramic surface mount capacitor is recommended. TI recommends using 2 capacitors across GVDD and GND: a low capacitance ceramic surface-mount capacitor for high-frequency filtering placed very close to GVDD and GND pins, and another high capacitance value surface-mount capacitor for IC bias requirements. In a similar manner, the current pulses delivered by the GH pin are sourced from the BST pin. Therefore, a local decoupling capacitor is recommended between the BST and SH pins.

# 10 Layout

## 10.1 Layout Guidelines

Optimum performance of half-bridge gate drivers cannot be achieved without taking due considerations during circuit board layout. The following points are emphasized:

1. Low-ESR and low-ESL capacitors must be connected close to the IC between GVDD and GND pins and between BST and SH pins to support high peak currents being drawn from GVDD and BST during the turn-on of the external MOSFETs.
2. To prevent large voltage transients at the drain of the top MOSFET, a low-ESR electrolytic capacitor and a good-quality ceramic capacitor must be connected between the MOSFET drain and ground (GND).
3. To avoid large negative transients on the switch node (SH) pin, the parasitic inductances between the source of the top MOSFET and the drain of the bottom MOSFET (synchronous rectifier) must be minimized.
4. Grounding considerations:
    - The first priority in designing grounding connections is to confine the high peak currents that charge and discharge the MOSFET gates to a minimal physical area. This will decrease the loop inductance and minimize noise issues on the gate terminals of the MOSFETs. The gate driver must be placed as close as possible to the MOSFETs.
    - The second consideration is the high current path that includes the bootstrap capacitor, the bootstrap diode, the local ground referenced bypass capacitor, and the low-side MOSFET body diode. The bootstrap capacitor is recharged on a cycle-by-cycle basis through the bootstrap diode from the ground referenced GVDD bypass capacitor. The recharging occurs in a short time interval and involves high peak current. Minimizing this loop length and area on the circuit board is important to ensure reliable operation.

## 10.2 Layout Example

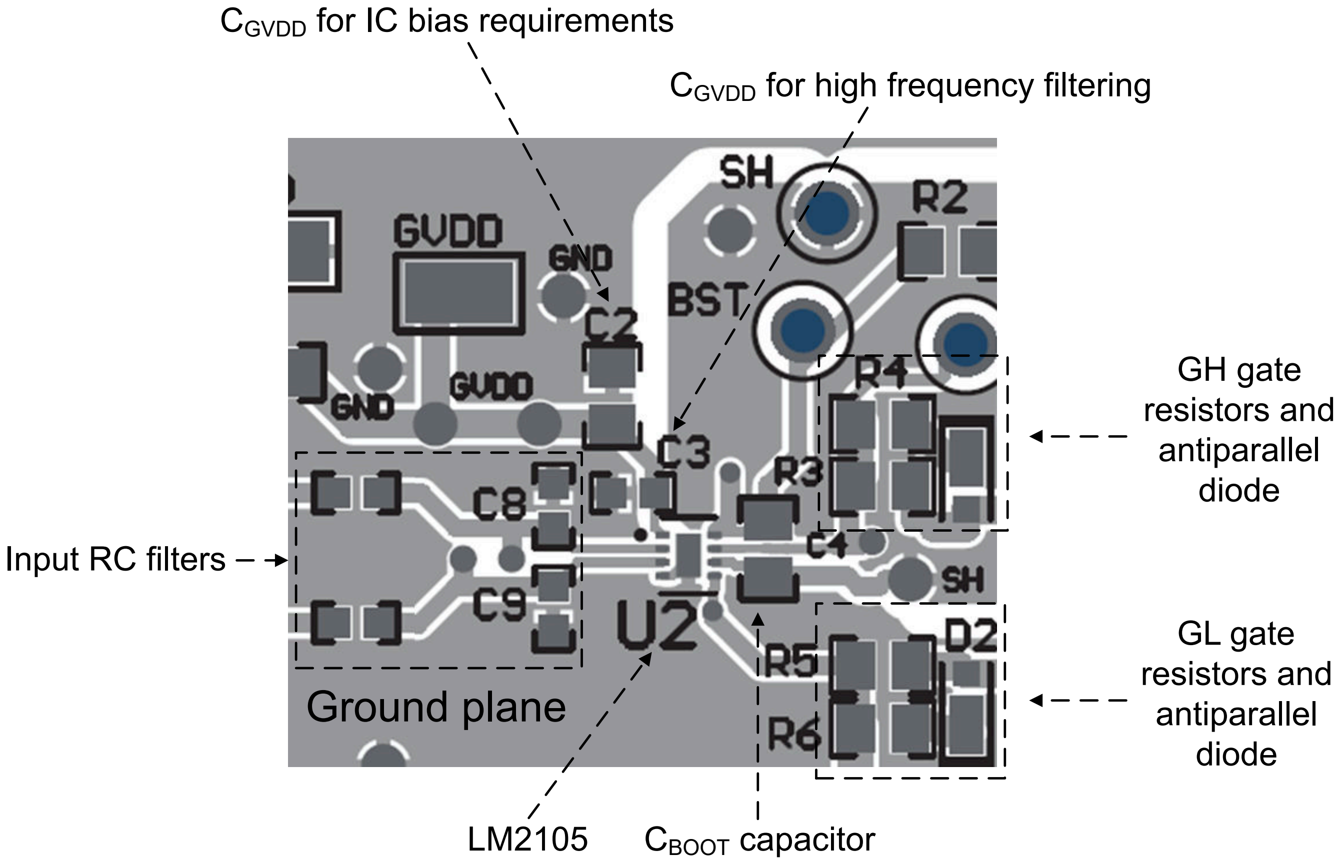


图 10-1. Layout Example

# 11 Device and Documentation Support

## 11.1 Device Support

### 11.1.1 第三方产品免责声明

TI 发布的与第三方产品或服务有关的信息，不能构成与此类产品或服务或保修的适用性有关的认可，不能构成此类产品或服务单独或与任何 TI 产品或服务一起的表示或认可。

## 11.2 Documentation Support

### 11.2.1 Related Documentation

For related documentation see the following:

- *Semiconductor and IC Packaging Thermal Metrics*, SPRA953

## 11.3 接收文档更新通知

要接收文档更新通知，请导航至 ti.com 上的器件产品文件夹。点击*订阅更新* 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

## 11.4 支持资源

TI E2E™ 支持论坛是工程师的重要参考资料，可直接从专家获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题可获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的《使用条款》。

## 11.5 Trademarks

TI E2E™ is a trademark of Texas Instruments.
所有商标均为其各自所有者的财产。

## 11.6 静电放电警告

静电放电 (ESD) 会损坏这个集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

## 11.7 术语表

| | |
|---|---|
| TI 术语表 | 本术语表列出并解释了术语、首字母缩略词和定义。 |

# 12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

# 重要声明和免责声明

邮寄地址：Texas Instruments, Post Office Box 655303, Dallas, Texas 75265