

## 适用于开关稳压器的 LM3478Q-Q1 高效率、低侧 N 沟道控制器

### 1 特性

- LM3478Q-Q1 符合 AEC-Q100 标准且采用汽车级工艺流程制造
- 8 引线 VSSOP-8
- 具备 1A 峰值电流能力的内部推挽驱动器
- 电流限制和热关断
- 通过电容器和电阻器优化的频率补偿
- 内部软启动
- 电流模式运行
- 带有迟滞功能的欠压闭锁
- 使用 LM3478 并借助 [WEBENCH 电源设计器](#) 创建定制设计方案

### 2 应用

- 分布式电源系统
- 电池充电器
- 离线电源
- 电信电源
- 汽车电源系统
- 2.97V 至 40V 的宽电源电压范围
- 100kHz 到 1MHz 的可调节时钟频率范围
- $\pm 2.5\%$  (过热保护) 内部基准
- 10 $\mu$ A 关断电流 (过热保护)

### 3 说明

LM3478Q-Q1 是适用于开关稳压器的多功能低侧 N 沟道 MOSFET 控制器。它适用于需要低侧 MOSFET 的拓扑，如升压、反激、SEPIC 等。此外，LM3478Q-Q1 还能够以极高的开关频率运行，以缩小总体解决方案规模。LM3478Q-Q1 的开关频率可通过单个外部电阻器调整为介于 100kHz 和 1MHz 之间的任意值。除了逐周期电流限制外，电流模式控制还可以提供出色的带宽和瞬态响应。可以使用单个外部电阻器对输出电流进行编程。

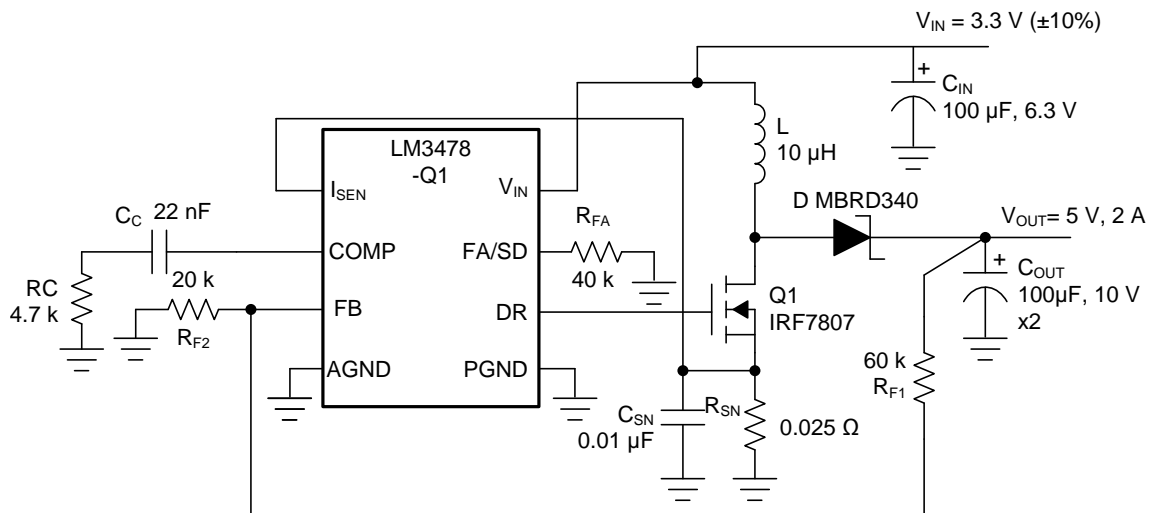
LM3478Q-Q1 内置热关断、短路保护、过压保护等特性。节能关断模式可以将总电源电流降低至 5 $\mu$ A 并允许进行电源定序。内部软启动会在启动时限制浪涌电流。

#### 器件信息(1)

| 器件型号       | 封装        | 封装尺寸 (标称值)      |
|------------|-----------|-----------------|
| LM3478Q-Q1 | VSSOP (8) | 3.00mm x 3.00mm |

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。

#### 典型的高效升压转换器



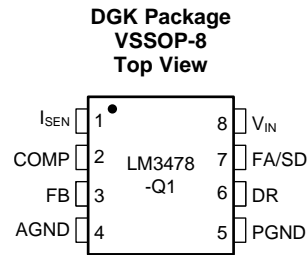
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## 4 修订历史记录

| 日期         | 修订版本 | 说明  |
|------------|------|---|
| 2018 年 4 月 | *    | LM3478Q-Q1 初始发行版（文献编号 SNVSAX8）请参阅 LM3478 器件（文献编号 SNVS085），了解商用级器件修订历史记录 |

## 5 Pin Configuration and Functions



### Pin Functions

| PIN              |     | I/O | DESCRIPTION  |
|------------------|-----|-----|--|
| NAME             | NO. |     |  |
| I <sub>SEN</sub> | 1   | I   | Current sense input pin. Voltage generated across an external sense resistor is fed into this pin.   |
| COMP             | 2   | I   | Compensation pin. A resistor, capacitor combination connected to this pin provides compensation for the control loop.  |
| FB               | 3   | I   | Feedback pin. The output voltage should be adjusted using a resistor divider to provide 1.26 V at this pin.  |
| AGND             | 4   | G   | Analog ground pin.   |
| PGND             | 5   | G   | Power ground pin.  |
| DR               | 6   | O   | Drive pin. The gate of the external MOSFET should be connected to this pin.  |
| FA/SD            | 7   | I   | Frequency adjust and Shutdown pin. A resistor connected to this pin sets the oscillator frequency. A high level on this pin for longer than 30 $\mu$ s will turn the device off. The device will then draw less than 10 $\mu$ A from the supply. |
| V <sub>IN</sub>  | 8   | P   | Power Supply Input pin.  |

## 6 Specifications

### 6.1 Absolute Maximum Ratings

 over operating free-air temperature (unless otherwise noted) <sup>(1)</sup>

|                                    |                     | MIN                | MAX             | UNIT |
|------------------------------------|---------------------|--------------------|-----------------|------|
| Input Voltage                      |                     |                    | 45              | V    |
| FB Pin Voltage                     |                     | $-0.4 < V$         | $V_{FB} < 7$    | V    |
| FA/SD Pin Voltage                  |                     | $-0.4 < V_{FA/SD}$ | $V_{FA/SD} < 7$ | V    |
| Peak Driver Output Current (<10µs) |                     |                    | 1               | A    |
| Power Dissipation                  |                     | Internally Limited |                 |      |
| Junction Temperature               |                     |                    | +150            | °C   |
| Lead Temperature                   | Vapor Phase (60 s)  |                    | 215             | °C   |
|                                    | Infrared (15 s)     |                    | 260             | °C   |
| DR Pin Voltage                     |                     | $-0.4 \leq VDR$    | $VDR \leq 8$    | V    |
| I <sub>SEN</sub> Pin Voltage       |                     |                    | 500             | mV   |
| T <sub>stg</sub>                   | Storage temperature | -65                | 150             | °C   |

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

### 6.2 ESD Ratings - LM3478Q-Q1

|                    |                         |   | VALUE                        | UNIT |      |
|--------------------|-------------------------|---|------------------------------|------|------|
| V <sub>(ESD)</sub> | Electrostatic discharge | Human body model (HBM), per AEC Q100-002 <sup>(1)</sup> | ±2000                        | V    |      |
|                    |                         | Charged device model (CDM), per AEC Q100-011            | Other pins                   |      | ±750 |
|                    |                         |   | Corner pins (1, 4, 5, and 8) |      | ±750 |

(1) AEC Q100-002 indicates HBM stressing is done in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

### 6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

|                            | MIN                | NOM | MAX              | UNIT |
|----------------------------|--------------------|-----|------------------|------|
| Supply Voltage             | $2.97 \leq V_{IN}$ |     | $V_{IN} \leq 40$ | V    |
| Junction Temperature Range | $-40 \leq T_J$     |     | $T_J \leq +125$  | °C   |
| Switching Frequency        | $100 \leq F_{SW}$  |     | $F_{SW} \leq 1$  | MHz  |

## 6.4 Thermal Information

| THERMAL METRIC <sup>(1)</sup> |  | LM3478Q-Q1 | UNIT |
|-------------------------------|--|------------|------|
|                               |  | DGK        |      |
|                               |  | 8 PINS     |      |
| R <sub>θJA</sub>              | Junction-to-ambient thermal resistance       | 157.2      | °C/W |
| R <sub>θJC(top)</sub>         | Junction-to-case (top) thermal resistance    | 49.9       | °C/W |
| R <sub>θJB</sub>              | Junction-to-board thermal resistance         | 77.1       | °C/W |
| ψ <sub>JT</sub>               | Junction-to-top characterization parameter   | 4.7        | °C/W |
| ψ <sub>JB</sub>               | Junction-to-board characterization parameter | 75.8       | °C/W |
| R <sub>θJC(bot)</sub>         | Junction-to-case (bottom) thermal resistance | N/A        | °C/W |

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, [SPRA953](#).

## 6.5 Electrical Characteristics

Unless otherwise specified, V<sub>IN</sub> = 12V, R<sub>FA</sub> = 40kΩ, T<sub>J</sub> = 25°C

| PARAMETER             | TEST CONDITIONS                            | MIN   | TYP    | MAX   | UNIT            |     |     |    |
|-----------------------|--|---|--------|-------|-----------------|-----|-----|----|
| V <sub>FB</sub>       | Feedback Voltage                           | V <sub>COMP</sub> = 1.4V, 2.97 ≤ V <sub>IN</sub> ≤ 40V  | 1.2416 | 1.26  | 1.2843          | V   |     |    |
|                       |  | V <sub>COMP</sub> = 1.4V, 2.97 ≤ V <sub>IN</sub> ≤ 40V, -40°C ≤ T <sub>J</sub> ≤ 125°C        | 1.228  |       | 1.292           |     |     |    |
| ΔV <sub>LINE</sub>    | Feedback Voltage Line Regulation           | 2.97 ≤ V <sub>IN</sub> ≤ 40V  |        | 0.001 | %/V             |     |     |    |
| ΔV <sub>LOAD</sub>    | Output Voltage Load Regulation             | I <sub>EAO</sub> Source/Sink  |        |       | ±0.5            | %/A |     |    |
| V <sub>UVLO</sub>     | Input Undervoltage Lock-out                |   |        |       | 2.85            | V   |     |    |
|                       |  | -40°C ≤ T <sub>J</sub> ≤ 125°C  |        |       | 2.97            |     |     |    |
| V <sub>UV(HYS)</sub>  | Input Undervoltage Lock-out Hysteresis     |   |        |       | 170             | mV  |     |    |
|                       |  | -40°C ≤ T <sub>J</sub> ≤ 125°C  |        |       | 210             |     |     |    |
| F <sub>nom</sub>      | Nominal Switching Frequency                | R <sub>FA</sub> = 40KΩ  |        |       | 400             | kHz |     |    |
|                       |  | R <sub>FA</sub> = 40KΩ, -40°C ≤ T <sub>J</sub> ≤ 125°C  |        |       | 440             |     |     |    |
| R <sub>DS1 (ON)</sub> | Driver Switch On Resistance (top)          | I <sub>DR</sub> = 0.2A, V <sub>IN</sub> = 5V  |        |       | 16              | Ω   |     |    |
| R <sub>DS2 (ON)</sub> | Driver Switch On Resistance (bottom)       | I <sub>DR</sub> = 0.2A  |        |       | 4.5             |     |     |    |
| V <sub>DR (max)</sub> | Maximum Drive Voltage Swing <sup>(1)</sup> | V <sub>IN</sub> < 7.2V  |        |       | V <sub>IN</sub> | V   |     |    |
|                       |  | V <sub>IN</sub> ≥ 7.2V  |        |       | 7.2             |     |     |    |
| D <sub>max</sub>      | Maximum Duty Cycle <sup>(2)</sup>          |   |        |       | 100%            |     |     |    |
| T <sub>min (on)</sub> | Minimum On Time                            |   |        |       | 325             | ns  |     |    |
|                       |  | -40°C ≤ T <sub>J</sub> ≤ 125°C  |        |       | 210             |     | 600 |    |
| I <sub>SUPPLY</sub>   | Supply Current (non-switching)             | See <sup>(3)</sup>  |        |       | 2.7             | mA  |     |    |
|                       |  | See <sup>(3)</sup> , -40°C ≤ T <sub>J</sub> ≤ 125°C   |        |       | 3.3             |     |     |    |
| I <sub>Q</sub>        | Quiescent Current in Shutdown Mode         | V <sub>FA/SD</sub> = 5V <sup>(4)</sup> , V <sub>IN</sub> = 5V                                 |        |       | 5               | μA  |     |    |
|                       |  | V <sub>FA/SD</sub> = 5V <sup>(4)</sup> , V <sub>IN</sub> = 5V, -40°C ≤ T <sub>J</sub> ≤ 125°C |        |       | 10              |     |     |    |
| V <sub>SENSE</sub>    | Current Sense Threshold Voltage            | V <sub>IN</sub> = 5V  |        |       | 135             | 156 | 180 | mV |
|                       |  | V <sub>IN</sub> = 5V, -40°C ≤ T <sub>J</sub> ≤ 125°C  |        |       | 125             | 190 |     |    |
| V <sub>SC</sub>       | Short-Circuit Current Limit Sense Voltage  | V <sub>IN</sub> = 5V  |        |       | 343             |     | mV  |    |
|                       |  | V <sub>IN</sub> = 5V, -40°C ≤ T <sub>J</sub> ≤ 125°C  |        |       | 250             | 415 |     |    |

(1) The voltage on the drive pin, V<sub>DR</sub> is equal to the input voltage when input voltage is less than 7.2 V. V<sub>DR</sub> is equal to 7.2 V when the input voltage is greater than or equal to 7.2 V.

(2) The limits for the maximum duty cycle can not be specified since the part does not permit less than 100% maximum duty cycle operation.

(3) For this test, the FA/SD pin is pulled to ground using a 40-K resistor.

(4) For this test, the FA/SD pin is pulled to 5 V using a 40-K resistor.

**Electrical Characteristics (continued)**

 Unless otherwise specified,  $V_{IN} = 12V$ ,  $R_{FA} = 40k\Omega$ ,  $T_J = 25^\circ C$ 

| PARAMETER      |  | TEST CONDITIONS  | MIN  | TYP  | MAX  | UNIT       |
|----------------|--|--|------|------|------|------------|
| $V_{SL}$       | Internal Compensation Ramp Voltage   | $V_{IN} = 5V$  |      | 92   |      | mV         |
|                |  | $V_{IN} = 5V, -40^\circ C \leq T_J \leq 125^\circ C$   | 52   |      | 132  |            |
| $V_{SL}$ ratio | $V_{SL}/V_{SENSE}$   |  | 0.30 | 0.49 | 0.70 |            |
| $V_{OVP}$      | Output Over-voltage Protection (with respect to feedback voltage) <sup>(5)</sup> | $V_{COMP} = 1.4V$  | 32   | 50   |      | mV         |
|                |  | $V_{COMP} = 1.4V, -40^\circ C \leq T_J \leq 125^\circ C$                                     | 25   |      |      |            |
|                |  | VSSOP Package  |      |      | 78   |            |
|                |  | VSSOP Package, $-40^\circ C \leq T_J \leq 125^\circ C$                                       |      |      | 85   |            |
| $V_{OVP(HYS)}$ | Output Over-Voltage Protection Hysteresis <sup>(5)</sup>                         | $V_{COMP} = 1.4V$  |      | 60   |      | mV         |
|                |  | $V_{COMP} = 1.4V, -40^\circ C \leq T_J \leq 125^\circ C$                                     | 20   |      | 110  |            |
| $G_m$          | Error Amplifier Transconductance   | $V_{COMP} = 1.4V, I_{EAO} = 100\mu A$ (Source/Sink)  | 600  | 800  | 1000 | $\mu S$    |
|                |  | $V_{COMP} = 1.4V, I_{EAO} = 100\mu A$ (Source/Sink), $-40^\circ C \leq T_J \leq 125^\circ C$ | 365  |      | 1265 |            |
| $A_{VOL}$      | Error Amplifier Voltage Gain   | $V_{COMP} = 1.4V, I_{EAO} = 100\mu A$ (Source/Sink)  |      | 38   |      | V/V        |
|                |  | $V_{COMP} = 1.4V, I_{EAO} = 100\mu A$ (Source/Sink), $-40^\circ C \leq T_J \leq 125^\circ C$ | 26   |      | 44   |            |
| $I_{EAO}$      | Error Amplifier Output Current (Source/ Sink)                                    | Source, $V_{COMP} = 1.4V, V_{FB} = 0V$   | 80   | 110  | 140  | $\mu A$    |
|                |  | Source, $V_{COMP} = 1.4V, V_{FB} = 0V, -40^\circ C \leq T_J \leq 125^\circ C$                | 50   |      | 180  |            |
|                |  | Sink, $V_{COMP} = 1.4V, V_{FB} = 1.4V$   | -100 | -140 | -180 | $\mu A$    |
|                |  | Sink, $V_{COMP} = 1.4V, V_{FB} = 1.4V, -40^\circ C \leq T_J \leq 125^\circ C$                | -85  |      | -185 |            |
| $V_{EAO}$      | Error Amplifier Output Voltage Swing   | Upper Limit, $V_{FB} = 0V$ , COMP Pin = Floating   |      | 2.2  |      | V          |
|                |  | Upper Limit, $V_{FB} = 0V$ , COMP Pin = Floating, $-40^\circ C \leq T_J \leq 125^\circ C$    | 1.8  |      | 2.4  |            |
|                |  | Lower Limit, $V_{FB} = 1.4V$   |      | 0.56 |      | V          |
|                |  | Lower Limit, $V_{FB} = 1.4V, -40^\circ C \leq T_J \leq 125^\circ C$                          | 0.2  |      | 1.0  |            |
| $T_{SS}$       | Internal Soft-Start Delay  | $V_{FB} = 1.2V, V_{COMP} = \text{Floating}$  |      | 4    |      | ms         |
| $T_r$          | Drive Pin Rise Time  | $C_{gs} = 3000pf, V_{DR} = 0$ to 3V  |      | 25   |      | ns         |
| $T_f$          | Drive Pin Fall Time  | $C_{gs} = 3000pf, V_{DR} = 0$ to 3V  |      | 25   |      | ns         |
| $V_{SD}$       | Shutdown threshold <sup>(6)</sup>  | Output = High  |      | 1.27 |      | V          |
|                |  | Output = High, $-40^\circ C \leq T_J \leq 125^\circ C$                                       |      |      | 1.4  |            |
|                |  | Output = Low   |      | 0.65 |      | V          |
|                |  | Output = Low, $-40^\circ C \leq T_J \leq 125^\circ C$  |      |      | 0.3  |            |
| $I_{SD}$       | Shutdown Pin Current   | $V_{SD} = 5V$  |      | -1   |      | $\mu A$    |
|                |  | $V_{SD} = 0V$  |      | +1   |      |            |
| $I_{FB}$       | Feedback Pin Current   |  |      | 15   |      | nA         |
| $T_{SD}$       | Thermal Shutdown   |  |      | 165  |      | $^\circ C$ |
| $T_{sh}$       | Thermal Shutdown Hysteresis  |  |      | 10   |      | $^\circ C$ |

(5) The over-voltage protection is specified with respect to the feedback voltage. This is because the over-voltage protection tracks the feedback voltage. The overvoltage protection threshold is given by adding the feedback voltage,  $V_{FB}$  to the over-voltage protection specification.

(6) The FA/SD pin should be pulled to  $V_{IN}$  through a resistor to turn the regulator off. The voltage on the FA/SD pin must be above the maximum limit for Output = High to keep the regulator off and must be below the limit for Output = Low to keep the regulator on.

### 6.6 Typical Characteristics

Unless otherwise specified,  $V_{IN} = 12V$ ,  $T_J = 25^\circ C$ .

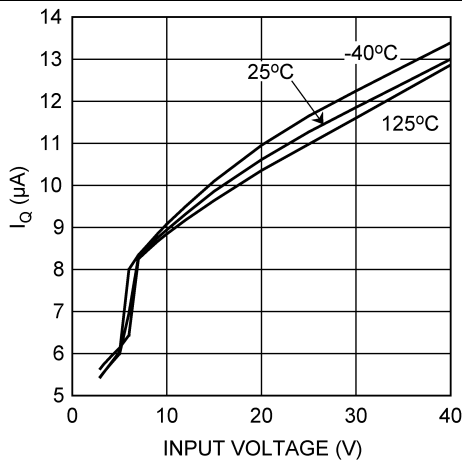


Figure 1.  $I_Q$  vs Input Voltage (Shutdown)

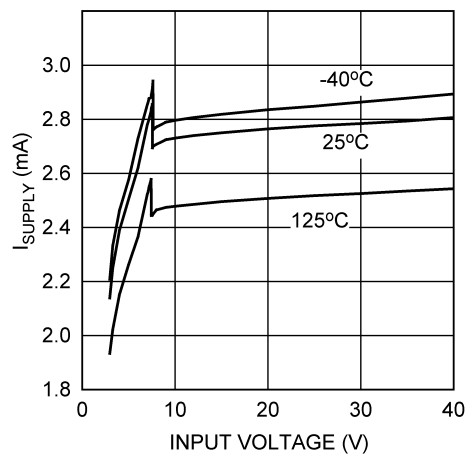


Figure 2.  $I_{Supply}$  vs Input Voltage (Non-Switching)

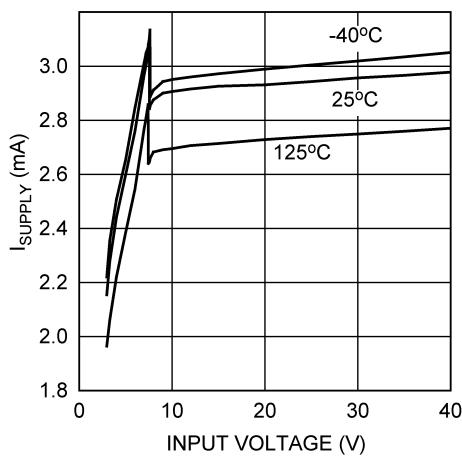


Figure 3.  $I_{Supply}$  vs  $V_{IN}$  (Switching)

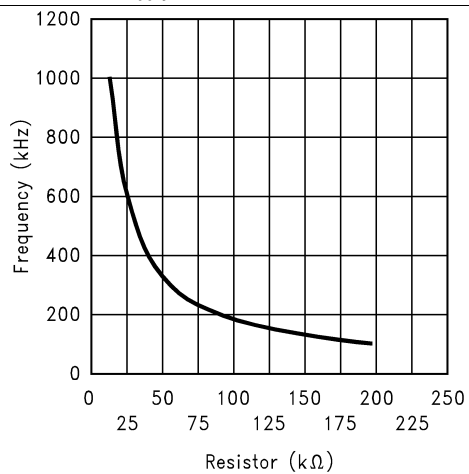


Figure 4. Switching Frequency vs  $R_{FA}$

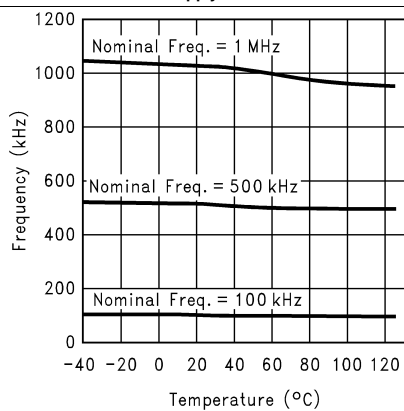


Figure 5. Frequency vs Temperature

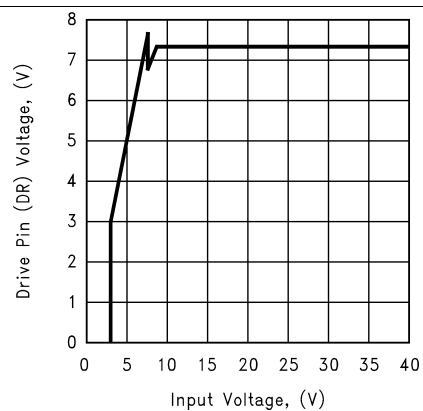
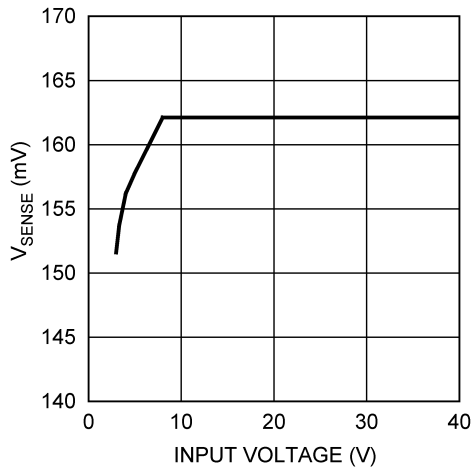


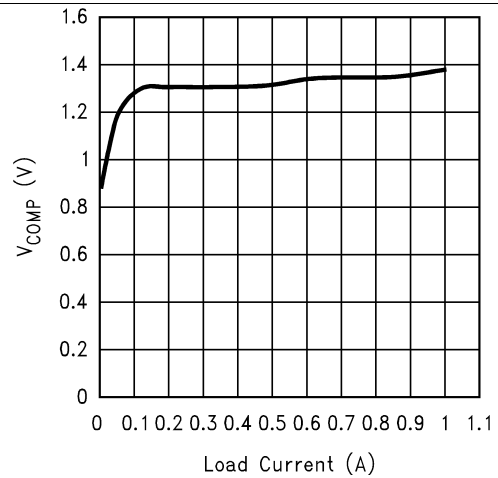
Figure 6. Drive Voltage vs Input Voltage

## Typical Characteristics (continued)

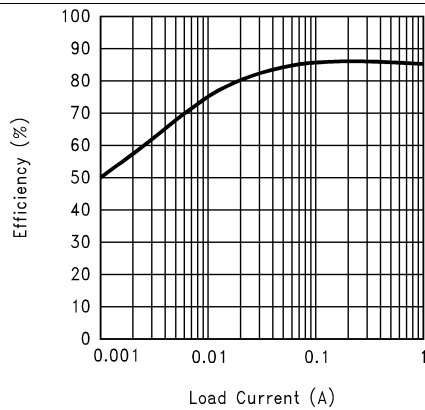
Unless otherwise specified,  $V_{IN} = 12V$ ,  $T_J = 25^\circ C$ .



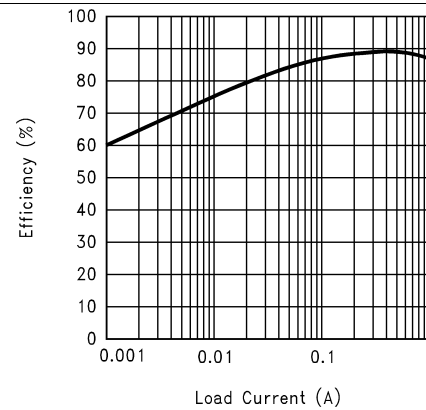
**Figure 7. Current Sense Threshold vs Input Voltage**



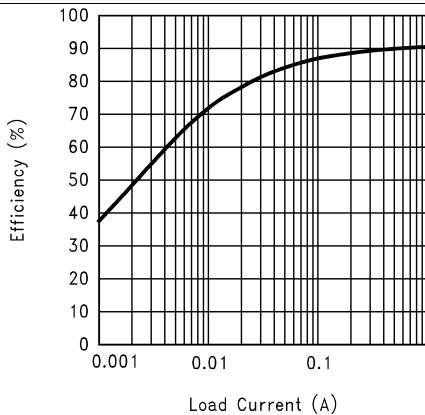
**Figure 8. COMP Pin Voltage vs Load Current**



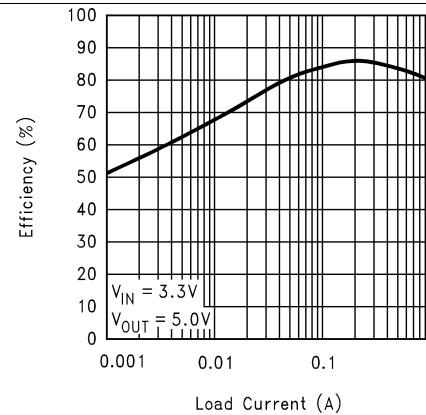
**Figure 9. Efficiency vs Load Current (3.3-V Input and 12-V Output)**



**Figure 10. Efficiency vs Load Current (5-V Input and 12-V Output)**



**Figure 11. Efficiency vs Load Current (9-V Input and 12-V Output)**



**Figure 12. Efficiency vs Load Current (3.3-V Input and 5-V Output)**



Typical Characteristics (continued)

Unless otherwise specified,  $V_{IN} = 12V$ ,  $T_J = 25^\circ C$ .

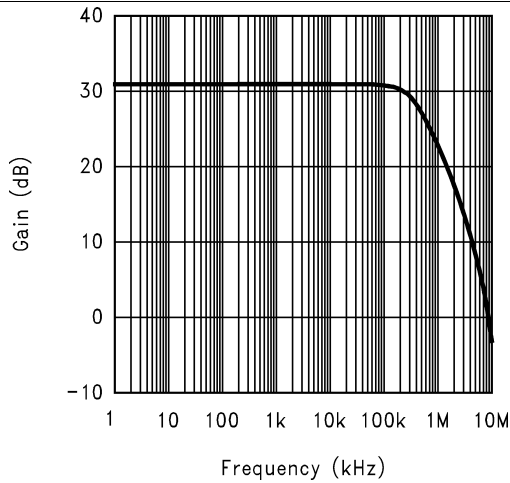


Figure 13. Error Amplifier Gain

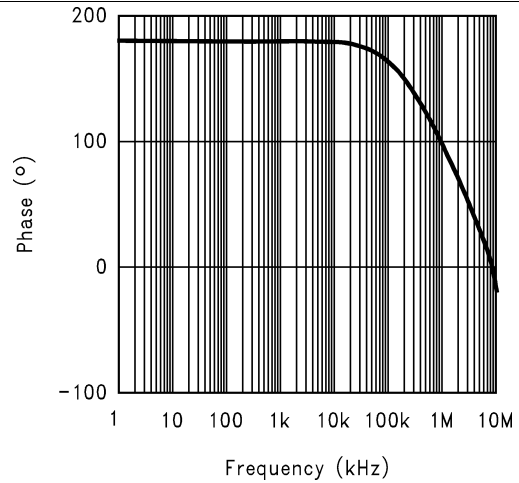


Figure 14. Error Amplifier Phase

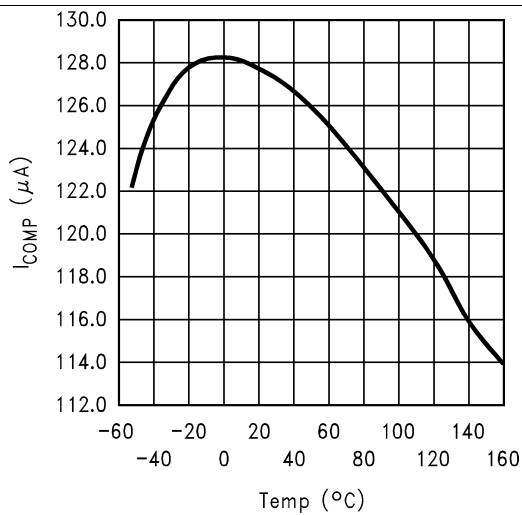


Figure 15. COMP Pin Source Current vs Temperature

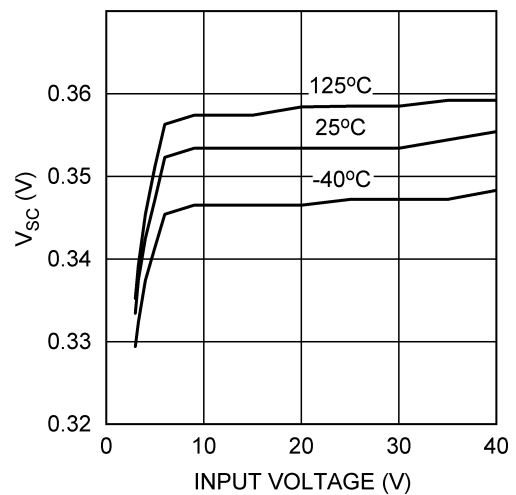


Figure 16. Short Circuit Sense Voltage vs Input Voltage

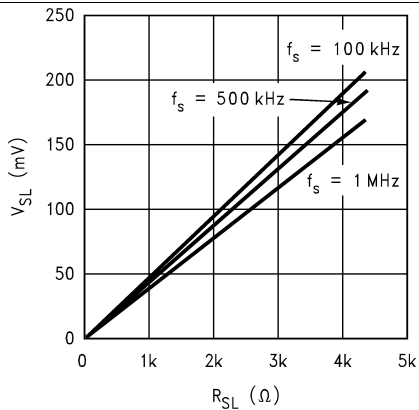


Figure 17. Compensation Ramp vs Compensation Resistor

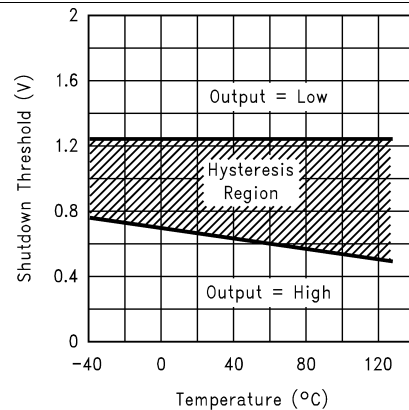
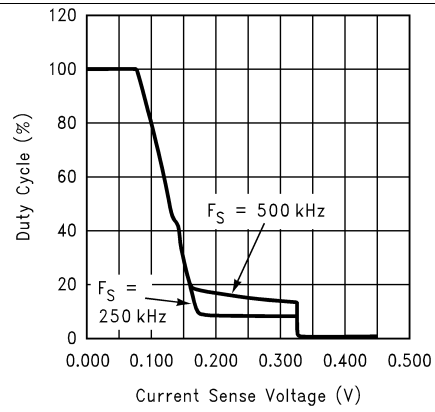


Figure 18. Shutdown Threshold Hysteresis vs Temperature

**Typical Characteristics (continued)**

Unless otherwise specified,  $V_{IN} = 12V$ ,  $T_J = 25^\circ C$ .



**Figure 19. Duty Cycle vs Current Sense Voltage**

## 7 Detailed Description

### 7.1 Overview

The LM3478Q-Q1 device uses a fixed frequency, Pulse Width Modulated (PWM) current mode control architecture. The [Functional Block Diagram](#) shows the basic functionality. In a typical application circuit, the peak current through the external MOSFET is sensed through an external sense resistor. The voltage across this resistor is fed into the  $I_{SEN}$  pin. This voltage is fed into the positive input of the PWM comparator. The output voltage is also sensed through an external feedback resistor divider network and fed into the error amplifier negative input (feedback pin, FB). The output of the error amplifier (COMP pin) is added to the slope compensation ramp and fed into the negative input of the PWM comparator. At the start of any switching cycle, the oscillator sets the RS latch using the switch logic block. This forces a high signal on the DR pin (gate of the external MOSFET) and the external MOSFET turns on. When the voltage on the positive input of the PWM comparator exceeds the negative input, the RS latch is reset and the external MOSFET turns off.

The voltage sensed across the sense resistor generally contains spurious noise spikes, as shown in [Figure 20](#). These spikes can force the PWM comparator to reset the RS latch prematurely. To prevent these spikes from resetting the latch, a blank-out circuit inside the IC prevents the PWM comparator from resetting the latch for a short duration after the latch is set. This duration is about 325 ns and is called the blanking interval and is specified as minimum on-time in the Electrical Characteristics section. Under extremely light-load or no-load conditions, the energy delivered to the output capacitor when the external MOSFET is on during the blanking interval is more than what is delivered to the load. An over-voltage comparator inside the LM3478Q-Q1 prevents the output voltage from rising under these conditions. The over-voltage comparator senses the feedback (FB pin) voltage and resets the RS latch. The latch remains in reset state until the output decays to the nominal value.

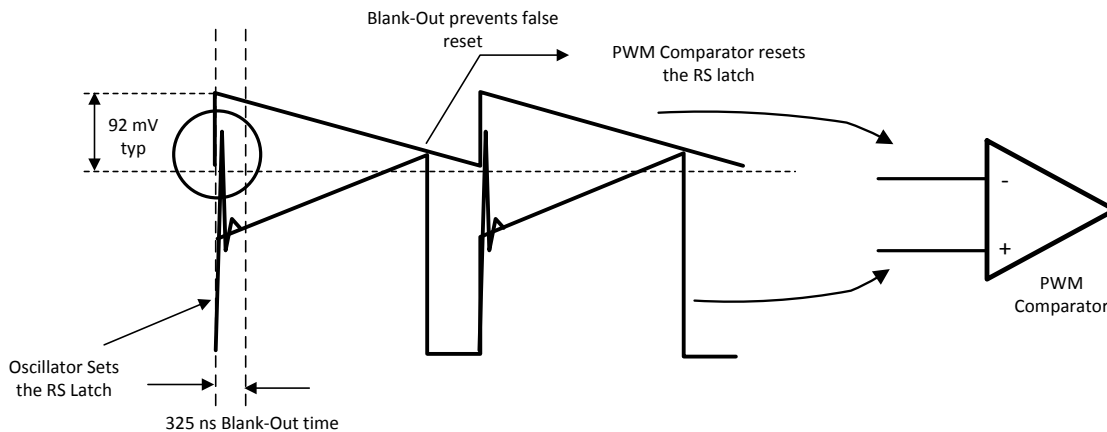
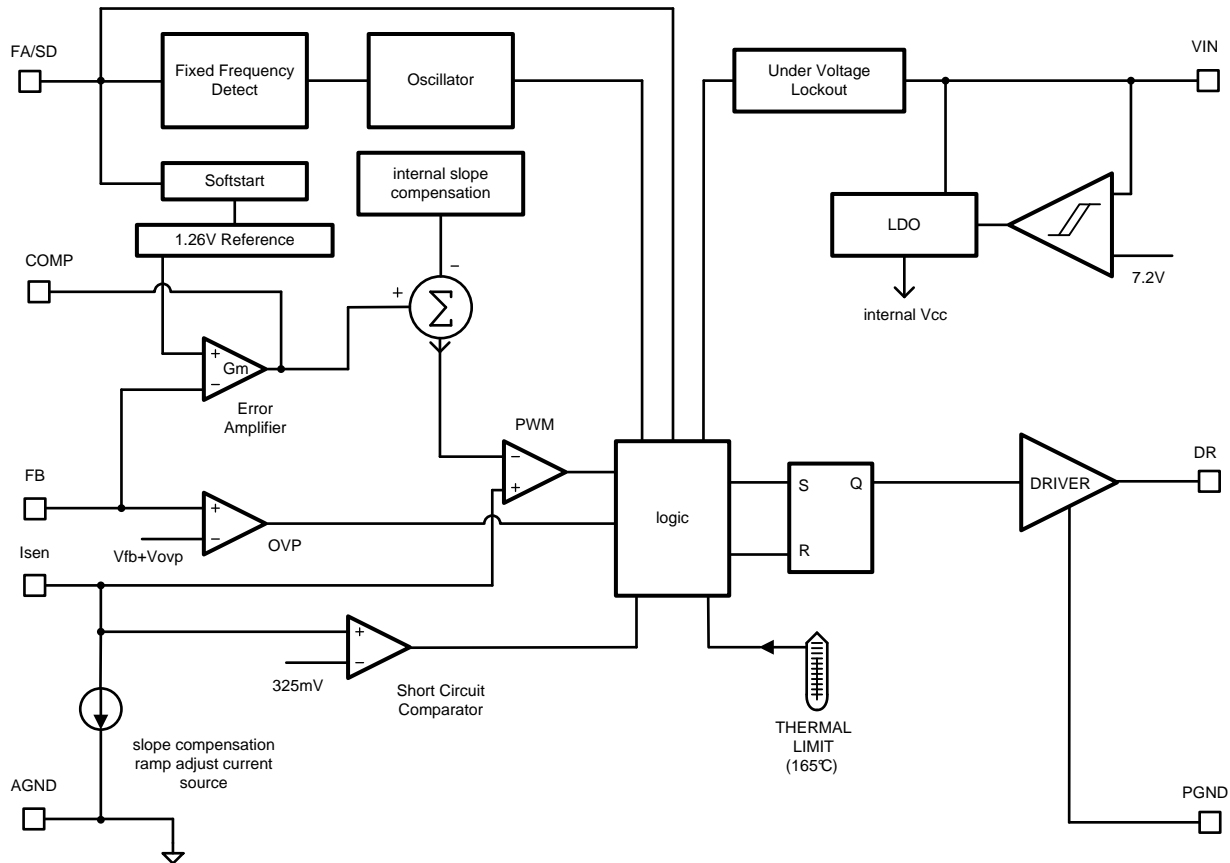


Figure 20. Basic Operation of the PWM Comparator

## 7.2 Functional Block Diagram



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## 7.3 Feature Description

### 7.3.1 Overvoltage Protection

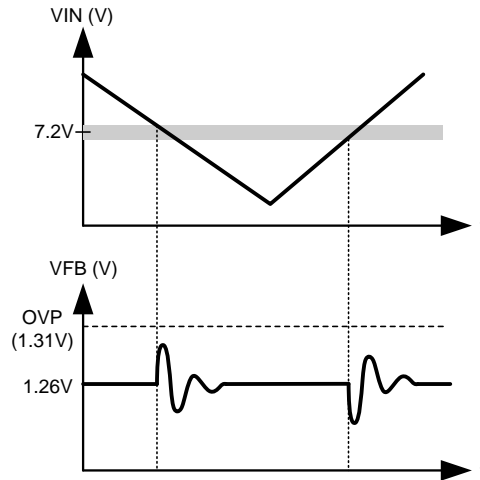
The LM3478Q-Q1 has over voltage protection (OVP) for the output voltage. OVP is sensed at the feedback pin (pin 3). If at anytime the voltage at the feedback pin rises to  $V_{FB} + V_{OVP}$ , OVP is triggered. See [Electrical Characteristics](#) section for limits on  $V_{FB}$  and  $V_{OVP}$ .

OVP will cause the drive pin to go low, forcing the power MOSFET off. With the MOSFET off, the output voltage will drop. The LM3478Q-Q1 begins switching again when the feedback voltage reaches  $V_{FB} + (V_{OVP} - V_{OVP(HYS)})$ . See [Electrical Characteristics](#) for limits on  $V_{OVP(HYS)}$ .

OVP can be triggered if the unregulated input voltage crosses 7.2 V, the output voltage will react as shown in [Figure 21](#). The internal bias of the LM3478Q-Q1 comes from either the internal LDO as shown in the block diagram or the voltage at the  $V_{in}$  pin is used directly. At  $V_{in}$  voltages lower than 7.2 V the internal IC bias is the  $V_{in}$  voltage and at voltages above 7.2V the internal LDO of the LM3478Q-Q1 provides the bias. At the switch over threshold at 7.2 V a sudden small change in bias voltage is seen by all the internal blocks of the LM3478Q-Q1. The control voltage shifts because of the bias change, the PWM comparator tries to keep regulation. To the PWM comparator, the scenario is identical to a step change in the load current, so the response at the output voltage is the same as would be observed in a step load change. Hence, the output voltage overshoot here can also trigger OVP. The LM3478Q-Q1 will regulate in hysteretic mode for several cycles, or may not recover and simply stay in hysteretic mode until the load current drops or  $V_{in}$  is not crossing the 7.2 V threshold anymore. Note that the output is still regulated in hysteretic mode.

### Feature Description (continued)

Depending on the requirements of the application, there is some influence one has over this effect. The threshold of 7.2 V can be shifted to higher voltages by adding a resistor in series with  $V_{IN}$ . In case  $V_{IN}$  is right at the threshold of 7.2 V, the threshold could cross over and over due to some slight ripple on  $V_{IN}$ . To minimize the effect on the output voltage one can filter the  $V_{IN}$  pin with an RC filter.



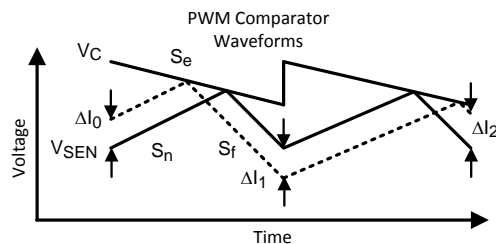
**Figure 21. The Feedback Voltage Experiences an Oscillation if the Input Voltage crosses the 7.2-V Internal Bias Threshold**

### 7.3.2 Slope Compensation Ramp

The LM3478Q-Q1 uses a current mode control scheme. The main advantages of current mode control are inherent cycle-by-cycle current limit for the switch and simpler control loop characteristics. It is also easy to parallel power stages using current mode control since current sharing is automatic. However, current mode control has an inherent instability for duty cycles greater than 50%, as shown in [Figure 22](#).

A small increase in the load current causes the switch current to increase by  $\Delta I_0$ . The effect of this load change is  $\Delta I_1$ .

The two solid waveforms shown are the waveforms compared at the internal pulse width modulator, used to generate the MOSFET drive signal. The top waveform with the slope  $S_e$  is the internally generated control waveform  $V_C$ . The bottom waveform with slopes  $S_n$  and  $S_f$  is the sensed inductor current waveform  $V_{SEN}$ .



**Figure 22. Sub-Harmonic Oscillation for  $D > 0.5$  and Compensation Ramp to Avoid Sub-Harmonic Oscillation**

Sub-harmonic Oscillation can be easily understood as a geometric problem. If the control signal does not have slope, the slope representing the inductor current ramps up until the control signal is reached and then slopes down again. If the duty cycle is above 50%, any perturbation will not converge but diverge from cycle to cycle and causes sub-harmonic oscillation.

It is apparent that the difference in the inductor current from one cycle to the next is a function of  $S_n$ ,  $S_f$  and  $S_e$  as shown in [Equation 1](#).

**Feature Description (continued)**

$$\Delta I_n = \frac{S_f - S_e}{S_n + S_e} \Delta I_{n-1} \tag{1}$$

Hence, if the quantity  $(S_f - S_e)/(S_n + S_e)$  is greater than 1, the inductor current diverges and sub-harmonic oscillation results. This counts for all current mode topologies. The LM3478Q-Q1 has some internal slope compensation  $V_{SL}$  which is enough for many applications above 50% duty cycle to avoid sub-harmonic oscillation .

For boost applications, the slopes  $S_e$ ,  $S_f$  and  $S_n$  can be calculated with [Equation 2](#), [Equation 3](#), and [Equation 4](#).

$$S_e = V_{SL} \times f_s \tag{2}$$

$$S_f = R_{sen} \times (V_{OUT} - V_{IN})/L \tag{3}$$

$$S_n = V_{IN} \times R_{sen}/L \tag{4}$$

When  $S_e$  increases, then the factor that determines if sub-harmonic oscillation will occur decreases. When the duty cycle is greater than 50%, and the inductance becomes less, the factor increases.

For more flexibility, slope compensation can be increased by adding one external resistor,  $R_{SL}$ , in the  $I_{SEN}$ 's path. [Figure 23](#) shows the setup. The externally generated slope compensation is then added to the internal slope compensation of the LM3478Q-Q1. When using external slope compensation, the formula for  $S_e$  becomes:

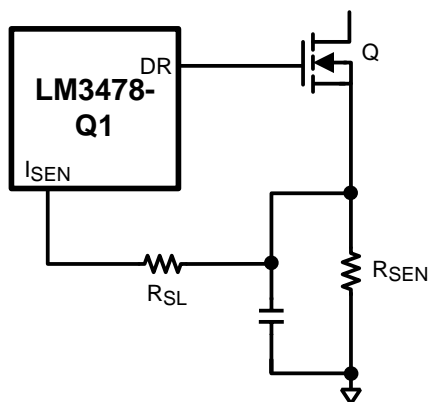
$$S_e = (V_{SL} + (K \times R_{SL})) \times f_s \tag{5}$$

A typical value for factor K is 40  $\mu A$ .

The factor changes with switching frequency. [Figure 24](#) is used to determine the factor K for individual applications and [Equation 6](#) gives the factor K.

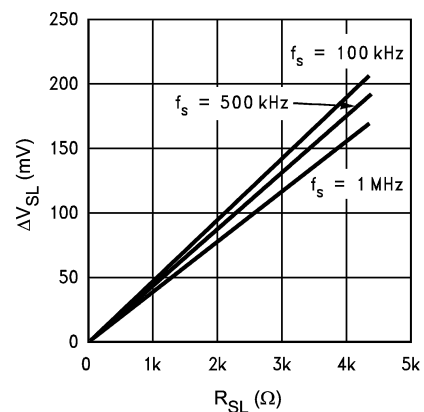
$$K = \Delta V_{SL} / R_{SL} \tag{6}$$

It is a good design practice to only add as much slope compensation as needed to avoid sub-harmonic oscillation. Additional slope compensation minimizes the influence of the sensed current in the control loop. With very large slope compensation the control loop characteristics are similar to a voltage mode regulator which compares the error voltage to a saw tooth waveform rather than the inductor current.



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**Figure 23. Adding External Slope Compensation**



**Figure 24. External Slope Compensation  $\Delta V_{SL}$  vs  $R_{SL}$**

## Feature Description (continued)

### 7.3.3 Frequency Adjust/Shutdown

The switching frequency of the LM3478Q-Q1 can be adjusted between 100 kHz and 1 MHz using a single external resistor. This resistor must be connected between FA/SD pin and ground, as shown in Figure 25. To determine the value of the resistor required for a desired switching frequency, refer to *Typical Characteristics* or use Equation 7:

$$R_{FA} = 4.503 \times 10^{11} \times f_S^{-1.26} \quad (7)$$

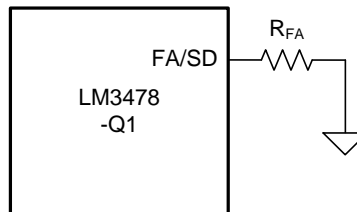


Figure 25. Frequency Adjust

The FA/SD pin also functions as a shutdown pin. If a high signal (>1.35 V) appears on the FA/SD pin, the LM3478Q-Q1 stops switching and goes into a low current mode. The total supply current of the IC reduces to less than 10 μA under these conditions. Figure 26 shows implementation of the shutdown function when operating in frequency adjust mode. In this mode a high signal for more than 30 us shuts down the IC. However, the voltage on the FA/SD pin should be always less than the absolute maximum of 7 V to avoid any damage to the device.

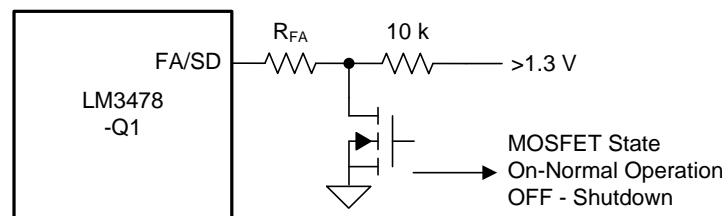


Figure 26. Shutdown Operation in Frequency Adjust Mode

### 7.3.4 Short-Circuit Protection

When the voltage across the sense resistor measured on the I<sub>SEN</sub> pin exceeds 343 mV, short circuit current limit protection gets activated. A comparator inside the LM3478Q-Q1 reduces the switching frequency by a factor of 5 and maintains this condition until the short is removed. In normal operation the sensed current will trigger the power MOSFET to turn off. During the blanking interval the PWM comparator will not react to an over current so that this additional 343 mV current limit threshold is implemented to protect the device in a short circuit or severe overload condition.

## 7.4 Device Functional Modes

The device is set to run as soon as the input voltage crosses above the UVLO set point and at a frequency set according to the FA/SD pin pull-down resistor. If the FA/SD pin is pulled high, the LM3478Q-Q1 enters shut-down mode.

## 8 Application and Implementation

### NOTE

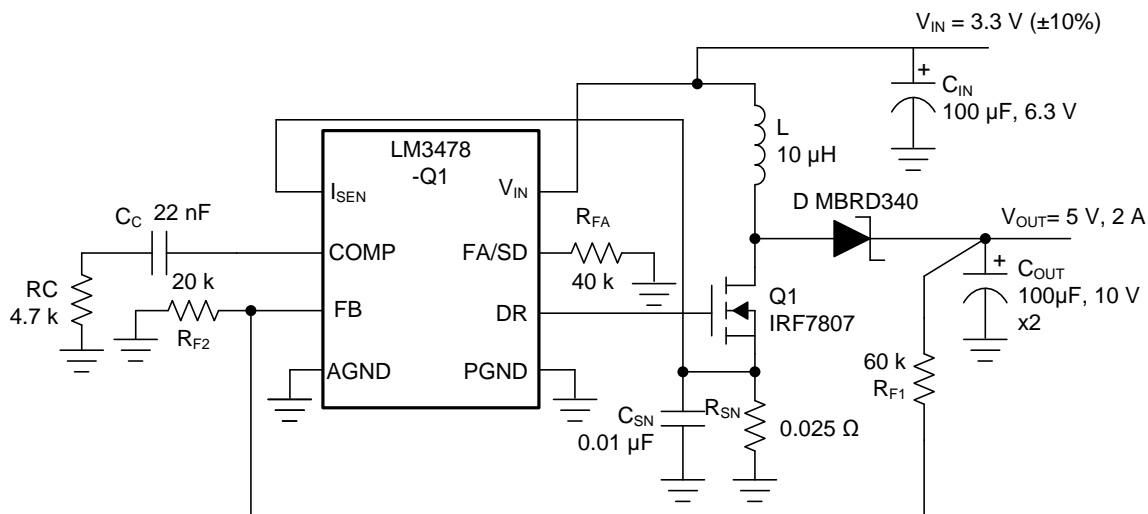
Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

### 8.1 Application Information

The LM3478Q-Q1 may be operated in either the continuous conduction mode (CCM) or the discontinuous current conduction mode (DCM). The following applications are designed for the CCM operation. This mode of operation has higher efficiency and usually lower EMI characteristics than the DCM.

### 8.2 Typical Applications

#### 8.2.1 Typical High Efficiency Step-Up (Boost) Converter



**Figure 27. Typical High Efficiency Step-Up (Boost) Converter Schematic**

The boost converter converts a low input voltage into a higher output voltage. The basic configuration for a boost converter is shown in [Figure 28](#). In the CCM (when the inductor current never reaches zero at steady state), the boost regulator operates in two states. In the first state of operation, MOSFET Q is turned on and energy is stored in the inductor. During this state, diode D is reverse biased and load current is supplied by the output capacitor,  $C_{OUT}$ .

In the second state, MOSFET Q is off and the diode is forward biased. The energy stored in the inductor is transferred to the load and the output capacitor. The ratio of the switch on time to the total period is the duty cycle D as shown in [Equation 8](#).

$$D = 1 - (V_{in} / V_{out}) \quad (8)$$

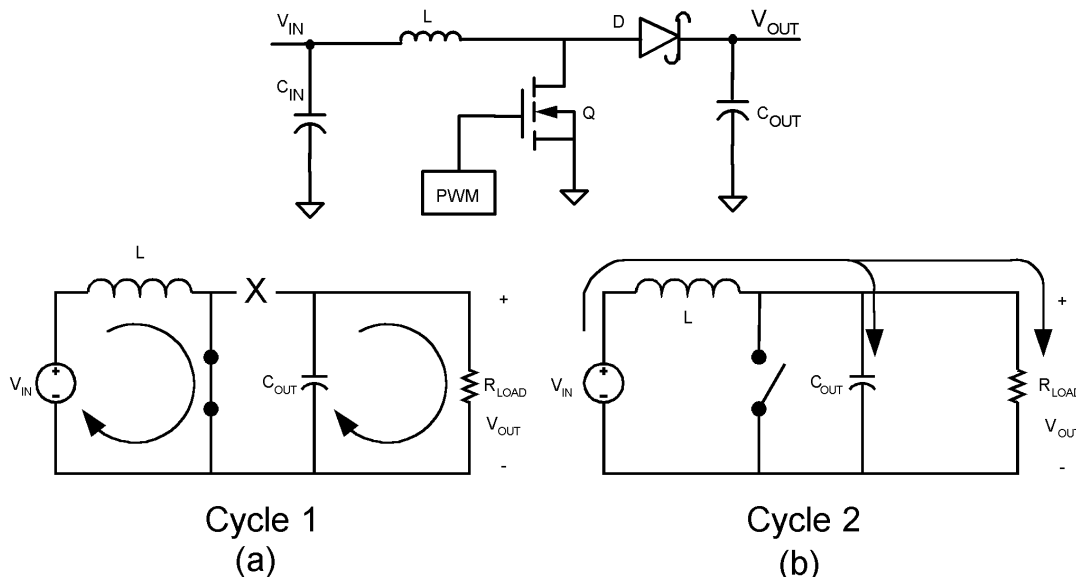
Including the voltage drop across the MOSFET and the diode the definition for the duty cycle is shown in [Equation 9](#).

$$D = 1 - ((V_{in} - V_q) / (V_{out} + V_d)) \quad (9)$$

$V_d$  is the forward voltage drop of the diode and  $V_q$  is the voltage drop across the MOSFET when it is on.



## Typical Applications (continued)



- A. First Cycle Operation
- B. Second Cycle of Operation

**Figure 28. Simplified Boost Converter**

### 8.2.1.1 Design Requirements

To properly size the components for the application, the designer needs the following parameters: input voltage range, output voltage, output current range, and required switching frequency. These four main parameters affect the choices of component available to achieve a proper system behavior.

For the power supply, the input impedance of the supply rail should be low enough that the input current transient does not drop below the UVLO value. The factors determining the choice of inductor used should be the average inductor current, and the inductor current ripple. If the switching frequency is set high, the converter can be operated with very small inductor values. The maximum current that can be delivered to the load is set by the sense resistor, RSEN. Current limit occurs when the voltage generated across the sense resistor equals the current sense threshold voltage, VSENSE. Also, a resistor RSL adds additional slope compensation, if required.

The following sections describe the design requirements for a typical LM3478Q-Q1 boost application.

### 8.2.1.2 Detailed Design Procedure

#### 8.2.1.2.1 Custom Design with WEBENCH Tools

[Click here](#) to create a custom design using the LM3478Q-Q1 device with the WEBENCH® Power Designer.

1. Start by entering your  $V_{IN}$ ,  $V_{OUT}$  and  $I_{OUT}$  requirements.
2. Optimize your design for key parameters like efficiency, footprint and cost using the optimizer dial and compare this design with other possible solutions from Texas Instruments.
3. WEBENCH Power Designer provides you with a customized schematic along with a list of materials with real time pricing and component availability.
4. In most cases, you will also be able to:
  - Run electrical simulations to see important waveforms and circuit performance,
  - Run thermal simulations to understand the thermal performance of your board,
  - Export your customized schematic and layout into popular CAD formats,
  - Print PDF reports for the design, and share your design with colleagues.

## Typical Applications (continued)

- Get more information about WEBENCH tools at [www.ti.com/webench](http://www.ti.com/webench).

### 8.2.1.2.2 Power Inductor Selection

The inductor is one of the two energy storage elements in a boost converter. [Figure 29](#) shows how the inductor current varies during a switching cycle. The current through an inductor is quantified using [Equation 10](#), which shows the relationship of  $L$ ,  $I_L$  and  $V_L$ .

$$V_L(t) = L \frac{di_L(t)}{dt} \quad (10)$$

The important quantities in determining a proper inductance value are  $I_L$  (the average inductor current) and  $\Delta I_L$  (the inductor current ripple). If  $\Delta I_L$  is larger than  $I_L$ , the inductor current will drop to zero for a portion of the cycle and the converter will operate in the DCM. All the analysis in this datasheet assumes operation in the CCM. To operate in the CCM, the following condition must be met by using [Equation 11](#).

$$L > \frac{D(1-D)V_{in}}{2I_{OUT}f_s} \quad (11)$$

Choose the minimum  $I_{OUT}$  to determine the minimum inductance value. A common choice is to set  $\Delta I_L$  to 30% of  $I_L$ . Choosing an appropriate core size for the inductor involves calculating the average and peak currents expected through the inductor. Use [Equation 12](#), [Equation 13](#), and [Equation 14](#) to the peak inductor current in a boost converter.

$$I_{LPEAK} = \text{Average } I_{L(max)} + \Delta I_{L(max)} \quad (12)$$

$$\text{Average } I_{L(max)} = I_{out} / (1-D) \quad (13)$$

$$\Delta I_{L(max)} = D \times V_{in} / (2 \times f_s \times L) \quad (14)$$

An inductor size with ratings higher than these values has to be selected. If the inductor is not properly rated, saturation will occur and may cause the circuit to malfunction.

The LM3478Q-Q1 can be set to switch at very high frequencies. When the switching frequency is high, the converter can be operated with very small inductor values. The LM3478Q-Q1 senses the peak current through the switch which is the same as the peak inductor current as calculated in the previous equation.

Typical Applications (continued)

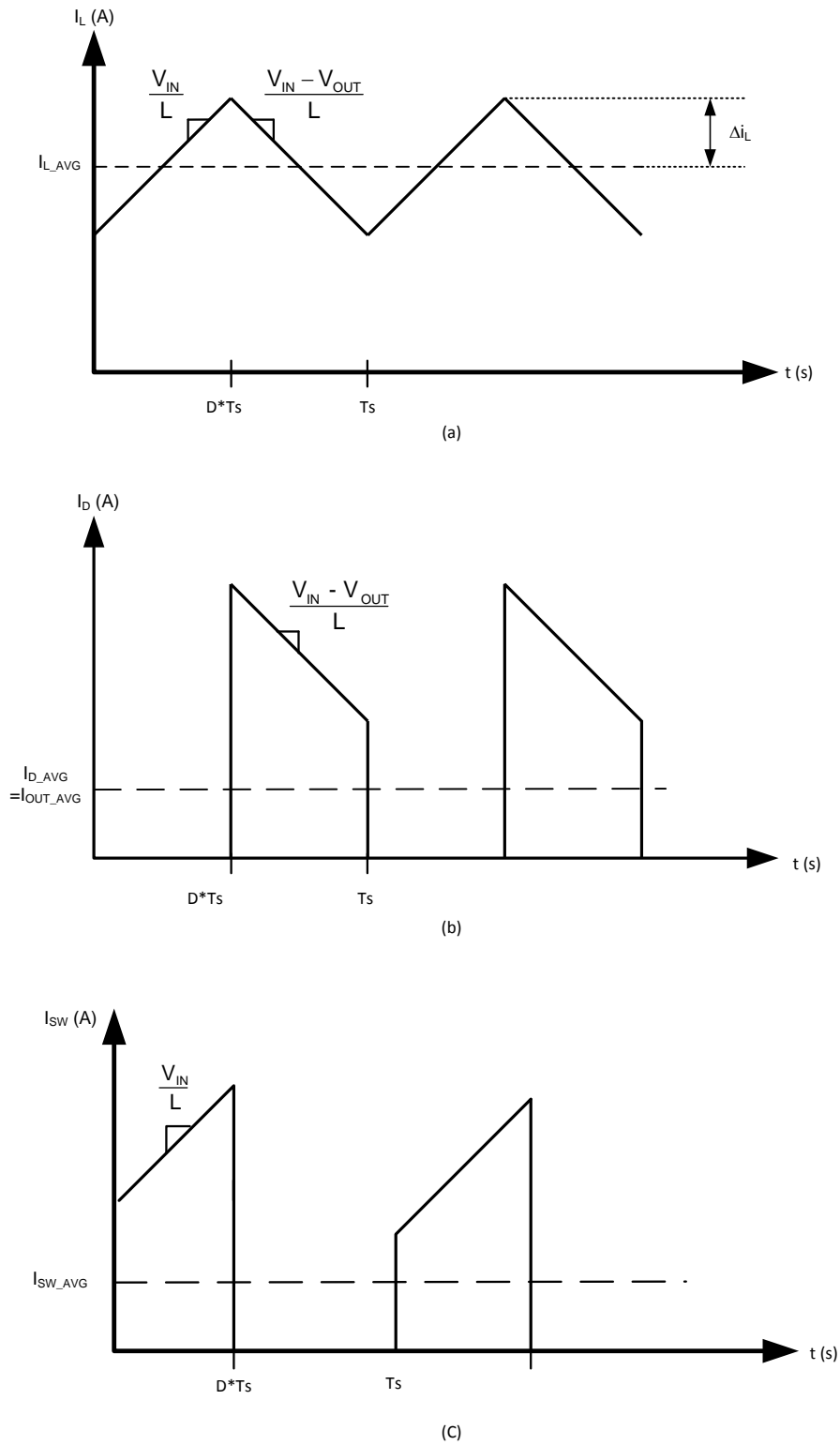


Figure 29. Inductor Current and Diode Current

## Typical Applications (continued)

### 8.2.1.2.3 Programming the Output Voltage

The output voltage can be programmed using a resistor divider between the output and the FB pin. The resistors are selected such that the voltage at the FB pin is 1.26 V. Pick  $R_{F1}$  (the resistor between the output voltage and the feedback pin) and  $R_{F2}$  (the resistor between the feedback pin and ground) can be selected using the following equation,

$$R_{F2} = (1.26 \text{ V} \times R_{F1}) / (V_{\text{out}} - 1.26 \text{ V}) \quad (15)$$

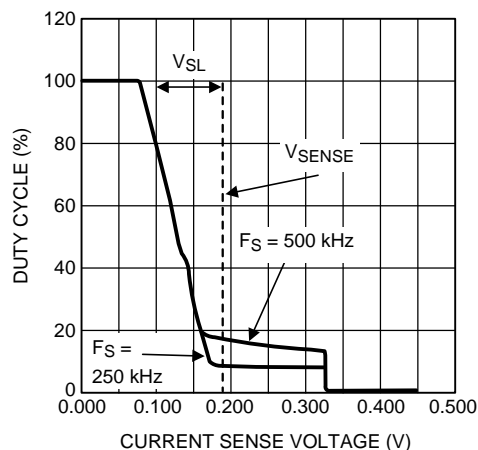
A 100-pF capacitor may be connected between the feedback and ground pins to reduce noise.

### 8.2.1.2.4 Setting the Current Limit

The maximum amount of current that can be delivered to the load is set by the sense resistor,  $R_{\text{SEN}}$ . Current limit occurs when the voltage that is generated across the sense resistor equals the current sense threshold voltage,  $V_{\text{SENSE}}$ . When this threshold is reached, the switch will be turned off until the next cycle. Limits for  $V_{\text{SENSE}}$  are specified in the electrical characteristics section.  $V_{\text{SENSE}}$  represents the maximum value of the internal control signal  $V_{\text{CS}}$  as shown in Figure 30. This control signal, however, is not a constant value and changes over the course of a period as a result of the internal compensation ramp ( $V_{\text{SL}}$ ). Therefore the current limit threshold will also change. The actual current limit threshold is a function of the sense voltage ( $V_{\text{SENSE}}$ ) and the internal compensation ramp:

$$R_{\text{SEN}} \times \text{ISW}_{\text{LIMIT}} = V_{\text{CS}_{\text{MAX}}} = V_{\text{SENSE}} - (D \times V_{\text{SL}}) \quad (16)$$

Where  $\text{ISW}_{\text{LIMIT}}$  is the peak switch current limit, defined by Equation 17.



**Figure 30. Current Sense Voltage vs Duty Cycle**

Figure 30 shows how  $V_{\text{CS}}$  (and current limit threshold voltage) change with duty cycle. The curve is equivalent to the internal compensation ramp slope ( $S_e$ ) and is bounded at low duty cycle by  $V_{\text{SENSE}}$ , shown as a dotted line. As duty cycle increases, the control voltage is reduced as  $V_{\text{SL}}$  ramps up. The graph also shows the short circuit current limit threshold of 343 mV (typical) during the 325 ns (typical) blanking time. For higher frequencies this fixed blanking time obviously occupies more duty cycle, percentage wise. Since current limit threshold varies with duty cycle, the use Equation 17 to select  $R_{\text{SEN}}$  and set the desired current limit threshold:

$$R_{\text{SEN}} = \frac{V_{\text{SENSE}} - (D \times V_{\text{SL}})}{\text{ISW}_{\text{LIMIT}}} \quad (17)$$

The numerator of Equation 17 is  $V_{\text{CS}}$ , and  $\text{ISW}_{\text{LIMIT}}$  using Equation 18.

$$\text{ISW}_{\text{LIMIT}} = \left[ \frac{I_{\text{OUT}}}{(1-D)} + \frac{(D \times V_{\text{IN}})}{(2 \times f_{\text{S}} \times L)} \right] \quad (18)$$

## Typical Applications (continued)

To avoid false triggering, the current limit value should have some margin above the maximum operating value, typically 120%. Values for both  $V_{SENSE}$  and  $V_{SL}$  are specified in [Electrical Characteristics](#). However, calculating with the limits of these two specs could result in an unrealistically wide current limit or  $R_{SEN}$  range. Therefore, [Equation 19](#) is recommended, using the  $V_{SL}$  ratio value given in [Electrical Characteristics](#).

$$R_{SEN} = \frac{V_{SENSE} - (D \times V_{SENSE} \times V_{SLratio})}{ISW_{LIMIT}} \quad (19)$$

$R_{SEN}$  is part of the current mode control loop and has some influence on control loop stability. Therefore, once the current limit threshold is set, loop stability must be verified. As described in the slope compensation section, [Equation 20](#) must hold true for a current mode converter to be stable.

$$S_f - S_e < S_n + S_e \quad (20)$$

To verify that this equation holds true, use [Equation 21](#).

$$R_{SEN} < \frac{2 \times V_{SL} \times f_s \times L}{V_o - (2 \times V_{IN})} \quad (21)$$

If the selected  $R_{SEN}$  is greater than this value, additional slope compensation must be added to ensure stability, as described in the section below.

### 8.2.1.2.5 Current Limit with External Slope Compensation

$R_{SL}$  is used to add additional slope compensation when required. It is not necessary in most designs and  $R_{SL}$  should be no larger than necessary. Select  $R_{SL}$  according to [Equation 22](#).

$$R_{SL} > \frac{\frac{R_{SEN} \times (V_o - 2V_{IN})}{2 \times f_s \times L} - V_{SL}}{40 \mu A} \quad (22)$$

Where  $R_{SEN}$  is the selected value based on current limit. With  $R_{SL}$  installed, the control signal includes additional external slope to stabilize the loop, which will also have an effect on the current limit threshold. Therefore, the current limit threshold must be re-verified, as illustrated in [Equation 23](#), [Equation 24](#), and [Equation 25](#) below.

$$V_{CS} = V_{SENSE} - (D \times (V_{SL} + \Delta V_{SL})) \quad (23)$$

Where  $\Delta V_{SL}$  is the additional slope compensation generated as discussed in the slope compensation ramp section and calculated using [Equation 24](#).

$$\Delta V_{SL} = 40 \mu A \times R_{SL} \quad (24)$$

This changes the equation for current limit (or  $R_{SEN}$ ) as shown in [Equation 25](#).

$$ISW_{LIMIT} = \frac{V_{SENSE} - (D \times (V_{SL} + \Delta V_{SL}))}{R_{SEN}} \quad (25)$$

The  $R_{SEN}$  and  $R_{SL}$  values may have to be calculated iteratively in order to achieve both the desired current limit and stable operation. In some designs  $R_{SL}$  can also help to filter noise on the  $I_{SEN}$  pin.

If the inductor is selected such that ripple current is the recommended 30% value, and the current limit threshold is 120% of the maximum peak, a simpler method can be used to determine  $R_{SEN}$ . [Equation 26](#) below will provide optimum stability without  $R_{SL}$ , provided that the above 2 conditions are met.

$$R_{SEN} = \frac{V_{SENSE}}{ISW_{LIMIT} + \left( \frac{V_o - V_i}{L \times f_s} \right) \times D} \quad (26)$$

### 8.2.1.2.6 Power Diode Selection

Observation of the boost converter circuit shows that the average current through the diode is the average load current, and the peak current through the diode is the peak current through the inductor. The diode should be rated to handle more than its peak current. The peak diode current can be calculated using [Equation 27](#).

$$I_{D(Peak)} = I_{OUT} / (1-D) + \Delta I_L \quad (27)$$

## Typical Applications (continued)

Thermally the diode must be able to handle the maximum average current delivered to the output. The peak reverse voltage for boost converters is equal to the regulated output voltage. The diode must be capable of handling this voltage. To improve efficiency, a low forward drop schottky diode is recommended.

### 8.2.1.2.7 Power MOSFET Selection

The drive pin of the LM3478Q-Q1 must be connected to the gate of an external MOSFET. The drive pin (DR) voltage depends on the input voltage (see [Typical Characteristics](#)). In most applications, a logic level MOSFET can be used. For very low input voltages, a sub logic level MOSFET should be used. The selected MOSFET has a great influence on the system efficiency. The critical parameters for selecting a MOSFET are:

1. Minimum threshold voltage,  $V_{TH(MIN)}$
2. On-resistance,  $R_{DS(ON)}$
3. Total gate charge,  $Q_g$
4. Reverse transfer capacitance,  $C_{RSS}$
5. Maximum drain to source voltage,  $V_{DS(MAX)}$

The off-state voltage of the MOSFET is approximately equal to the output voltage.  $V_{ds(max)}$  must be greater than the output voltage. The power losses in the MOSFET can be categorized into conduction losses and switching losses.  $R_{DS(ON)}$  is needed to estimate the conduction losses,  $P_{cond}$ :

$$P_{cond} = I^2 \times R_{DS(ON)} \times D \quad (28)$$

The temperature effect on the  $R_{DS(ON)}$  usually is quite significant. Assume 30% increase at hot.

For the current  $I$  in [Equation 28](#) the average inductor current may be used.

Especially at high switching frequencies the switching losses may be the largest portion of the total losses.

The switching losses are very difficult to calculate due to changing parasitics of a given MOSFET in operation. Often the individual MOSFET's data sheet does not give enough information to yield a useful result. [Equation 29](#) and [Equation 30](#) give a rough idea how the switching losses are calculated:

$$P_{SW} = \frac{I_{Lmax} \times V_{out}}{2} \times f_{SW} \times (t_{LH} + t_{HL}) \quad (29)$$

$$t_{LH} = \left( Q_{gd} + \frac{Q_{gs}}{2} \right) \times \frac{R_{drOn}}{V_{dr} - V_{gsTh}} \quad (30)$$

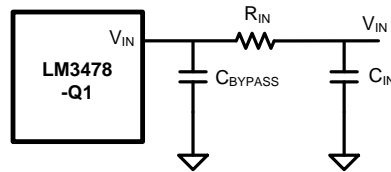
### 8.2.1.2.8 Input Capacitor Selection

Due to the presence of an inductor at the input of a boost converter, the input current waveform is continuous and triangular as shown in [Figure 29](#). The inductor ensures that the input capacitor sees fairly low ripple currents. However, as the input capacitor gets smaller, the input ripple goes up. The RMS current in the input capacitor is given using [Equation 31](#).

$$I_{CIN(RMS)} = \Delta i_L / \sqrt{3} = \frac{1}{2\sqrt{3}} \left( \frac{V_{OUT} - V_{IN}}{V_{OUT} L f_s} \right) \times V_{in} \quad (31)$$

The input capacitor should be capable of handling the RMS current. Although the input capacitor is not as critical in a boost application, low values can cause impedance interactions. Therefore a good quality capacitor should be chosen in the range of 10  $\mu F$  to 20  $\mu F$ . If a value lower than 10  $\mu F$  is used, then problems with impedance interactions or switching noise can affect the LM3478Q-Q1. To improve performance, especially with  $V_{in}$  below 8 volts, it is recommended to use a 20 Ohm resistor at the input to provide an RC filter. The resistor is placed in series with the VIN pin with only a bypass capacitor attached to the VIN pin directly (see [Figure 31](#)). A 0.1- $\mu F$  or 1- $\mu F$  ceramic capacitor is necessary in this configuration. The bulk input capacitor and inductor will connect on the other side of the resistor at the input power supply.

Typical Applications (continued)



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Figure 31. Reducing IC Input Noise

8.2.1.2.9 Output Capacitor Selection

The output capacitor in a boost converter provides all the output current when the inductor is charging. As a result it sees very large ripple currents. The output capacitor should be capable of handling the maximum RMS current. Equation 32 shows the RMS current in the output capacitor.

$$I_{\text{COUT(RMS)}} = \sqrt{(1-D) \left[ I_{\text{OUT}}^2 \frac{D}{(1-D)^2} + \frac{\Delta i_L^2}{3} \right]} \tag{32}$$

Where

$$\Delta i_L = \frac{DV_{\text{IN}}}{2Lf_s} \tag{33}$$

The ESR and ESL of the capacitor directly control the output ripple. Use capacitors with low ESR and ESL at the output for high efficiency and low ripple voltage. Surface mount tantalums, surface mount polymer electrolytic, polymer tantalum, or multi-layer ceramic capacitors are recommended at the output.

For applications that require very low output voltage ripple, a second stage LC filter often is a good solution. Most of the time it is lower cost to use a small second inductor in the power path and an additional final output capacitor than to reduce the output voltage ripple by purely increasing the output capacitor without an additional LC filter.

8.2.1.2.10 Compensation

For detailed explanation on how to select the right compensation components to attach to the compensation pin for a boost topology, please see AN-1286 Compensation For The LM3748 Boost Controller SNVA067.

8.2.1.3 Application Curves

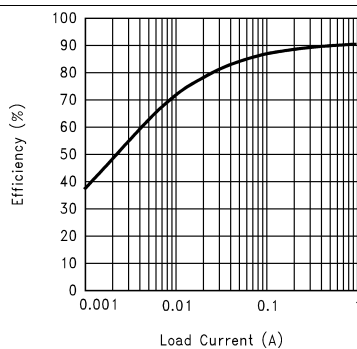


Figure 32. Efficiency vs Load Current (9-V In and 12-V Out)

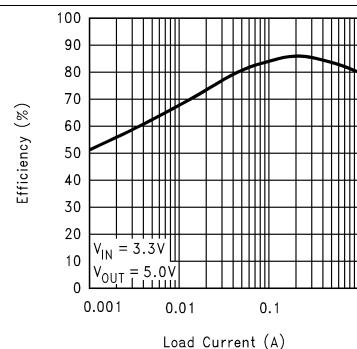
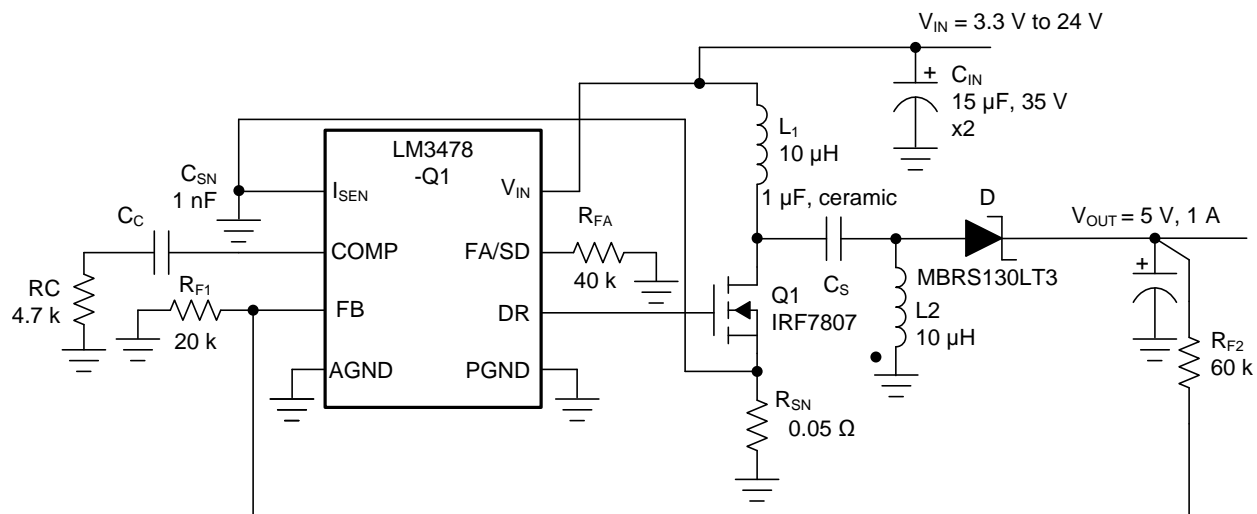


Figure 33. Efficiency vs Load Current (3.3-V In and 5-V Out)

## Typical Applications (continued)

### 8.2.2 Typical SEPIC Converter



**Figure 34. Typical SEPIC Converter**

Since the LM3478Q-Q1 controls a low-side N-Channel MOSFET, it can also be used in SEPIC (Single Ended Primary Inductance Converter) applications. An example of a SEPIC using the LM3478Q-Q1 is shown in [Figure 34](#). Note that the output voltage can be higher or lower than the input voltage. The SEPIC uses two inductors to step-up or step-down the input voltage. The inductors L1 and L2 can be two discrete inductors or two windings of a coupled inductor since equal voltages are applied across the inductor throughout the switching cycle. Using two discrete inductors allows use of catalog magnetics, as opposed to a custom inductor. The input ripple can be reduced along with size by using the coupled windings for L1 and L2.

Due to the presence of the inductor L1 at the input, the SEPIC inherits all the benefits of a boost converter. One main advantage of a SEPIC over a boost converter is the inherent input to output isolation. The capacitor C<sub>S</sub> isolates the input from the output and provides protection against a shorted or malfunctioning load. Hence, the SEPIC is useful for replacing boost circuits when true shutdown is required. This means that the output voltage falls to 0V when the switch is turned off. In a boost converter, the output can only fall to the input voltage minus a diode drop.

The duty cycle of a SEPIC is given using [Equation 34](#).

$$D = \frac{V_{OUT} + V_{DIODE}}{V_{OUT} + V_{IN} - V_Q + V_{DIODE}} \quad (34)$$

In [Equation 34](#),  $V_Q$  is the on-state voltage of the MOSFET, Q, and  $V_{DIODE}$  is the forward voltage drop of the diode.

#### 8.2.2.1 Design Requirements

To properly size the components for the application, the designer needs the following parameters: input voltage range, output voltage, output current range, and required switching frequency. These four main parameters affect the choices of component available to achieve a proper system behavior.

For the power supply, the input impedance of the supply rail should be low enough that the input current transient does not drop below the UVLO value. The factors determining the choice of inductor used should be the average inductor current, and the inductor current ripple. If the switching frequency is set high, the converter can be operated with very small inductor values. The maximum current that can be delivered to the load is set by the sense resistor, R<sub>SEN</sub>. Current limit occurs when the voltage generated across the sense resistor equals the current sense threshold voltage, V<sub>SENSE</sub>. Also, a resistor R<sub>SL</sub> adds additional slope compensation, if required.

The following sections describe the design requirements for a typical LM3478Q-Q1 boost application.



## Typical Applications (continued)

### 8.2.2.2 Detailed Design Procedure

#### 8.2.2.2.1 Power MOSFET Selection

As in a boost converter, parameters governing the selection of the MOSFET are the minimum threshold voltage,  $V_{TH(MIN)}$ , the on-resistance,  $R_{DS(ON)}$ , the total gate charge,  $Q_g$ , the reverse transfer capacitance,  $C_{RSS}$ , and the maximum drain to source voltage,  $V_{DS(MAX)}$ . The peak switch voltage in a SEPIC is given using [Equation 35](#).

$$V_{SW(PEAK)} = V_{IN} + V_{OUT} + V_{DIODE} \quad (35)$$

The selected MOSFET should satisfy the condition:

$$V_{DS(MAX)} > V_{SW(PEAK)} \quad (36)$$

The peak switch current is given using [Equation 37](#).

$$I_{SW(PEAK)} = I_{L1(AVG)} + I_{OUT} + \frac{\Delta I_{L1} + \Delta I_{L2}}{2} \quad (37)$$

The RMS current through the switch is given using [Equation 38](#).

$$I_{SWRMS} = \sqrt{\left[ I_{SWPEAK}^2 - I_{SWPEAK} (\Delta I_{L1} + \Delta I_{L2}) + \frac{(\Delta I_{L1} + \Delta I_{L2})^2}{3} \right] D} \quad (38)$$

#### 8.2.2.2.2 Power Diode Selection

The Power diode must be selected to handle the peak current and the peak reverse voltage. In a SEPIC, the diode peak current is the same as the switch peak current. The off-state voltage or peak reverse voltage of the diode is  $V_{IN} + V_{OUT}$ . Similar to the boost converter, the average diode current is equal to the output current. Schottky diodes are recommended.

#### 8.2.2.2.3 Selection of Inductors L1 and L2

Proper selection of inductors L1 and L2 to maintain continuous current conduction mode requires calculations of the following parameters.

Average current in the inductors can be calculated using [Equation 39](#).

$$I_{L1AVE} = \frac{D I_{OUT}}{1-D} \quad (39)$$

$$I_{L2AVE} = I_{OUT} \quad (40)$$

Peak to peak ripple current, to calculate core loss if necessary using [Equation 41](#) and [Equation 42](#).

$$\Delta I_{L1} = \frac{(V_{IN} - V_Q) D}{(L1) f_s} \quad (41)$$

$$\Delta I_{L2} = \frac{(V_{IN} - V_Q) D}{(L2) f_s} \quad (42)$$

Maintaining the condition  $I_L > \Delta I_L / 2$  to ensure continuous current conduction yields [Equation 43](#) and [Equation 44](#).

$$L1 > \frac{(V_{IN} - V_Q)(1-D)}{2 I_{OUT} f_s} \quad (43)$$

$$L2 > \frac{(V_{IN} - V_Q) D}{2 I_{OUT} f_s} \quad (44)$$

Peak current in the inductor, use [Equation 45](#) and [Equation 46](#) to ensure the inductor does not saturate.

$$I_{L1PK} = \frac{D I_{OUT}}{1-D} + \frac{\Delta I_{L1}}{2} \quad (45)$$

## Typical Applications (continued)

$$I_{L2PK} = I_{OUT} + \frac{\Delta I_{L2}}{2} \quad (46)$$

$I_{L1PK}$  must be lower than the maximum current rating set by the current sense resistor.

The value of L1 can be increased above the minimum recommended to reduce input ripple and output ripple. However, once  $D_{IL1}$  is less than 20% of  $I_{L1AVE}$ , the benefit to output ripple is minimal.

By increasing the value of L2 above the minimum recommended,  $\Delta I_{L2}$  can be reduced, which in turn will reduce the output ripple voltage:

$$\Delta V_{OUT} = \left( \frac{I_{OUT}}{1-D} + \frac{\Delta I_{L2}}{2} \right) ESR \quad (47)$$

where ESR is the effective series resistance of the output capacitor.

If L1 and L2 are wound on the same core, then  $L1 = L2 = L$ . All of the previous equations will hold true if the inductance is replaced by 2L.

### 8.2.2.2.4 Sense Resistor Selection

The peak current through the switch,  $I_{SW(PEAK)}$  can be adjusted using the current sense resistor,  $R_{SEN}$ , to provide a certain output current. Resistor  $R_{SEN}$  can be selected using [Equation 48](#)

$$R_{SEN} = \frac{V_{SENSE} - D(V_{SL} + \Delta V_{SL})}{I_{SWPEAK}} \quad (48)$$

### 8.2.2.2.5 Sepic Capacitor Selection

The selection of the SEPIC capacitor, CS, depends on the RMS current. The RMS current of the SEPIC capacitor is given by [Equation 49](#).

$$I_{CSRMS} = \sqrt{I_{SWRMS}^2 + (I_{L1PK}^2 - I_{L1PK}\Delta I_{L1} + \Delta I_{L1}^2)(1-D)} \quad (49)$$

The SEPIC capacitor must be rated for a large ACrms current relative to the output power. This property makes the SEPIC much better suited to lower power applications where the RMS current through the capacitor is relatively small (relative to capacitor technology). The voltage rating of the SEPIC capacitor must be greater than the maximum input voltage. There is an energy balance between CS and L1, which can be used to determine the value of the capacitor. [Equation 50](#) shows the basic energy balance.

$$\frac{1}{2} C_S \Delta V_S^2 = \frac{1}{2} L_1 \Delta I_{L1}^2 \quad (50)$$

where

$$\Delta V_S = \left( \frac{V_{OUT}}{V_{OUT} + V_{IN} - V_Q + V_{DIODE}} \right) \frac{I_{OUT}}{f_S C_S} \quad (51)$$

is the ripple voltage across the SEPIC capacitor, and

$$\Delta I_{L1} = \frac{(V_{IN} - V_Q) D}{L_1 f_S} \quad (52)$$

is the ripple current through the inductor L1. The energy balance equation can be solved using [Equation 53](#) to provide a minimum value for  $C_S$ .

$$C_S \geq L_1 \frac{I_{OUT}^2}{(V_{IN} - V_Q)^2} \quad (53)$$

## Typical Applications (continued)

### 8.2.2.2.6 Input Capacitor Selection

Similar to a boost converter, the SEPIC has an inductor at the input. Hence, the input current waveform is continuous and triangular. The inductor ensures that the input capacitor sees fairly low ripple currents. However, as the input capacitor gets smaller, the input ripple goes up. The RMS current in the input capacitor is given using Equation 54.

$$I_{CIN(RMS)} = \Delta I_{L1} / \sqrt{12} = \frac{D}{2\sqrt{3}} \left( \frac{V_{IN} - V_O}{L_1 f_s} \right) \tag{54}$$

The input capacitor should be capable of handling the RMS current. Although the input capacitor is not as critical in a boost application, low values can cause impedance interactions. Therefore a good quality capacitor should be chosen in the range of 10µF to 20µF. If a value lower than 10 µF is used, then problems with impedance interactions or switching noise can affect the LM3478Q-Q1. To improve performance, especially with  $V_{IN}$  below 8 volts, TI recommends that the user uses a 20Ω resistor at the input to provide a RC filter. The resistor is placed in series with the  $V_{IN}$  pin with only a bypass capacitor attached to the  $V_{IN}$  pin directly (see Figure 31). A 0.1-µF or 1-µF ceramic capacitor is necessary in this configuration. The bulk input capacitor and inductor will connect on the other side of the resistor with the input power supply.

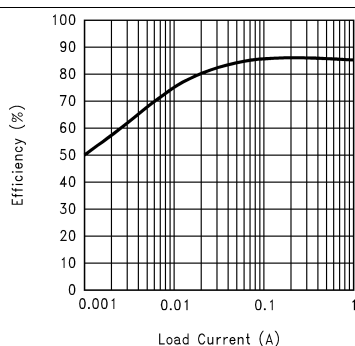
### 8.2.2.2.7 Output Capacitor Selection

The output capacitor of the SEPIC sees very large ripple currents (similar to the output capacitor of a boost converter). The RMS current through the output capacitor is given using Equation 55.

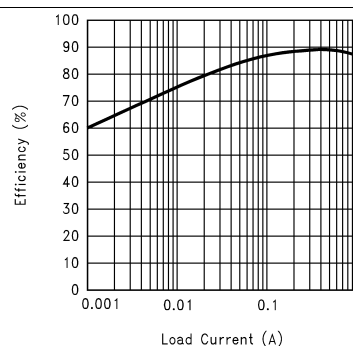
$$I_{RMS} = \sqrt{\left[ I_{SWPK}^2 - I_{SWPK} (\Delta I_{L1} + \Delta I_{L2}) + \frac{(\Delta I_{L1} + \Delta I_{L2})^2}{3} \right] (1-D) - I_{OUT}^2} \tag{55}$$

The ESR and ESL of the output capacitor directly control the output ripple. Use low capacitors with low ESR and ESL at the output for high efficiency and low ripple voltage. Surface mount tantalums, surface mount polymer electrolytic and polymer tantalum, Sanyo-OSCON, or multi-layer ceramic capacitors are recommended at the output for low ripple.

### 8.2.2.3 Application Curves



**Figure 35. Efficiency vs Load Current (3.3-V In and 12-V Out)**



**Figure 36. Efficiency vs Load Current (5-V In and 12-V Out)**

## 9 Power Supply Recommendations

The LM3478Q-Q1 is designed to operate from various DC power supply including a car battery. If so, VIN input should be protected from reversal voltage and voltage dump over 40 volts. The impedance of the input supply rail should be low enough that the input current transient does not cause drop below VIN UVLO level. If the input supply is connected by using long wires, additional bulk capacitance may be required in addition to normal input capacitor.

## 10 Layout

### 10.1 Layout Guidelines

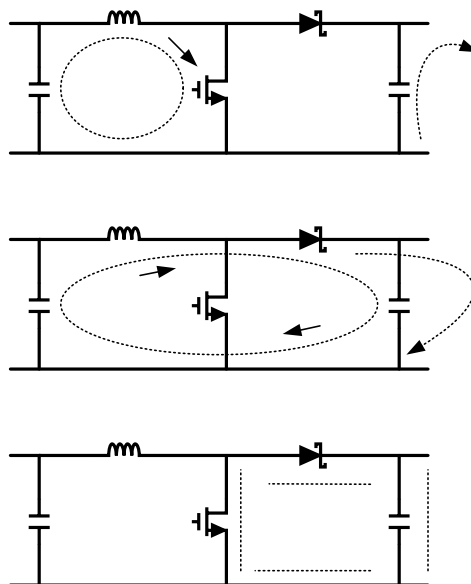
Good board layout is critical for switching controllers. First the ground plane area must be sufficient for thermal dissipation purposes and second, appropriate guidelines must be followed to reduce the effects of switching noise. Switching converters are very fast switching devices. In such devices, the rapid increase of input current combined with the parasitic trace inductance generates unwanted  $Ldi/dt$  noise spikes. The magnitude of this noise tends to increase as the output current increases. This parasitic spike noise may turn into electromagnetic interference (EMI), and can also cause problems in device performance. Therefore, care must be taken in layout to minimize the effect of this switching noise. The current sensing circuit in current mode devices can be easily affected by switching noise. This noise can cause duty cycle jittering which leads to increased spectral noise. Although the LM3478Q-Q1 has 325 ns blanking time at the beginning of every cycle to ignore this noise, some noise may remain after the blanking time.

The most important layout rule is to keep the AC current loops as small as possible. [Figure 37](#) shows the current flow of a boost converter. The top schematic shows a dotted line which represents the current flow during on-state and the middle schematic shows the current flow during off-state. The bottom schematic shows the currents we refer to as AC currents. They are the most critical ones since current is changing in very short time periods. The dotted lined traces of the bottom schematic are the ones to make as short as possible.

The PGND and AGND pins have to be connected to the same ground very close to the IC. To avoid ground loop currents, attach all the grounds of the system only at one point.

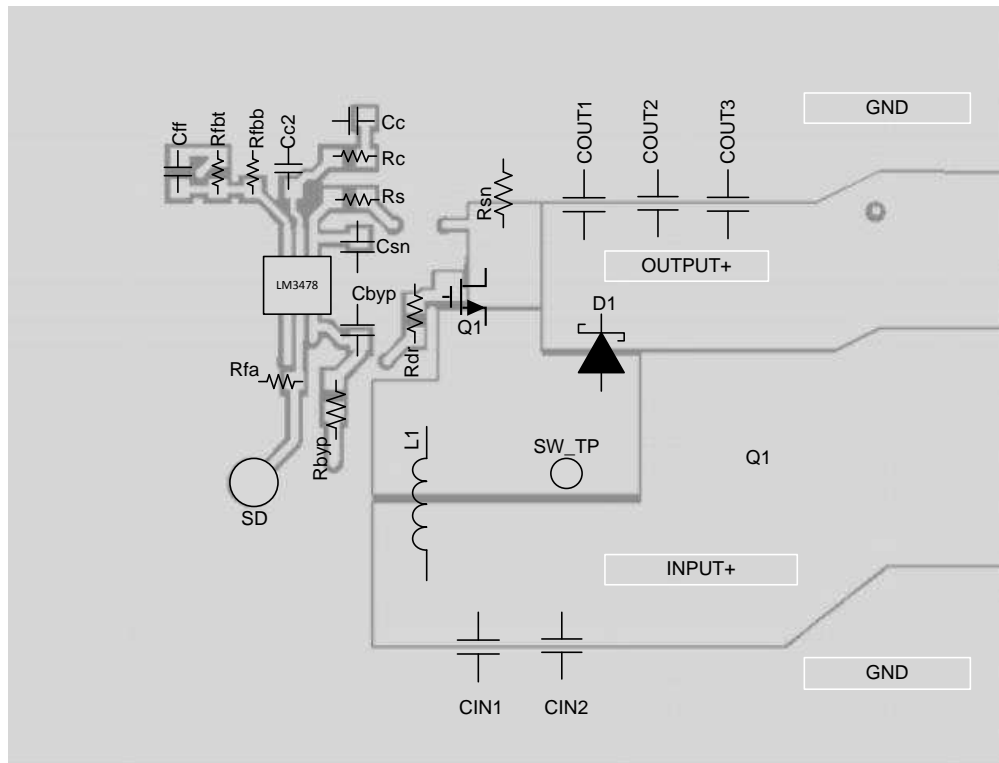
A ceramic input capacitor should be connected as close as possible to the Vin pin and grounded close to the GND pin.

For more information about layout in switch mode power supplies please refer to *AN-1229 Simple Switcher PCB Layout Guidelines*, [SNVA054](#).



**Figure 37. Current Flow in a Boost Application**

## 10.2 Layout Example



See evaluation modules for more detailed examples.

**Figure 38. Typical Layout for a Boost Converter**

## 11 器件和文档支持

### 11.1 使用 WEBENCH 工具创建定制设计

请[单击此处](#)，使用 LM3478Q-Q1 器件并借助 WEBENCH®电源设计器创建定制设计。

1. 首先，输入您的输入电压、输出电压和输出电流要求。
2. 使用优化器拨盘优化效率、封装和成本等关键设计参数并将您的设计与德州仪器 (TI) 的其他可行解决方案进行比较。
3. WEBENCH 电源设计器提供一份定制原理图以及罗列实时价格和组件供货情况的物料清单。
4. 在大多数情况下，您还可以：
  - 运行电气仿真，观察重要波形以及电路性能；
  - 运行热性能仿真，了解电路板热性能；
  - 将定制原理图和布局方案导出至常用 CAD 格式，
  - 打印设计方案的 PDF 报告并与同事共享。
5. 请访问 [www.ti.com.cn/webench](http://www.ti.com.cn/webench)，获取有关 WEBENCH 工具的详细信息。

### 11.2 接收文档更新通知

要接收文档更新通知，请导航至 [TI.com.cn](http://TI.com.cn) 上的器件产品文件夹。单击右上角的 *通知我* 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查阅已修订文档中包含的修订历史记录。

### 11.3 文档支持

使用 [LM3478](#) 并借助 WEBENCH 电源设计器创建定制设计。

#### 11.3.1 相关文档

请参阅如下相关文档：

- [AN-1286 LM3748 升压控制器的补偿 SNVA067](#)
- [AN-1229 Simple Switcher PCB 布局指南 SNVA054](#)

### 11.4 商标

WEBENCH is a registered trademark of Texas Instruments.  
All other trademarks are the property of their respective owners.

### 11.5 静电放电警告



这些装置包含有限的内置 ESD 保护。存储或装卸时，应将导线一起截短或将装置放置于导电泡棉中，以防止 MOS 门极遭受静电损伤。

### 11.6 术语表

[SLYZ022](#) — TI 术语表。

这份术语表列出并解释术语、缩写和定义。

## 12 机械、封装和可订购信息

以下页面包含机械、封装和可订购信息。这些信息是指定器件的最新可用数据。数据如有变更，恕不另行通知，且不会对此文档进行修订。如需获取此数据表的浏览器版本，请参阅左侧的导航栏。

**PACKAGING INFORMATION**

| Orderable Device | Status<br>(1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan<br>(2) | Lead finish/<br>Ball material<br>(6) | MSL Peak Temp<br>(3) | Op Temp (°C) | Device Marking<br>(4/5) | Samples                 |
|------------------|---------------|--------------|-----------------|------|-------------|-----------------|--------------------------------------|----------------------|--------------|-------------------------|-------------------------|
| LM3478QMM/NOPB   | ACTIVE        | VSSOP        | DGK             | 8    | 1000        | RoHS & Green    | NIPDAU   SN                          | Level-1-260C-UNLIM   | -40 to 125   | SSFB                    | <a href="#">Samples</a> |
| LM3478QMMX/NOPB  | ACTIVE        | VSSOP        | DGK             | 8    | 3500        | RoHS & Green    | NIPDAU   SN                          | Level-1-260C-UNLIM   | -40 to 125   | SSFB                    | <a href="#">Samples</a> |

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

| Device          | Package Type | Package Drawing | Pins | SPQ  | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|-----------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| LM3478QMM/NOPB  | VSSOP        | DGK             | 8    | 1000 | 178.0              | 12.4               | 5.3     | 3.4     | 1.4     | 8.0     | 12.0   | Q1            |
| LM3478QMMX/NOPB | VSSOP        | DGK             | 8    | 3500 | 330.0              | 12.4               | 5.3     | 3.4     | 1.4     | 8.0     | 12.0   | Q1            |

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

| Device          | Package Type | Package Drawing | Pins | SPQ  | Length (mm) | Width (mm) | Height (mm) |
|-----------------|--------------|-----------------|------|------|-------------|------------|-------------|
| LM3478QMM/NOPB  | VSSOP        | DGK             | 8    | 1000 | 208.0       | 191.0      | 35.0        |
| LM3478QMMX/NOPB | VSSOP        | DGK             | 8    | 3500 | 367.0       | 367.0      | 35.0        |

# DGK0008A



# PACKAGE OUTLINE

VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



4214862/A 04/2023

**NOTES:**

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1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.

# EXAMPLE BOARD LAYOUT

DGK0008A

™ VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 15X



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NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.

# EXAMPLE STENCIL DESIGN

DGK0008A

<sup>TM</sup> VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
SCALE: 15X

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NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

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