LM5118-Q1 宽电压范围降压/升压控制器

1 特性

- 符合 AEC-Q100 的汽车应用 标准
  - 器件温度 1 级：-40°C 至 +125°C 的环境运行温度范围
  - 器件 HBM ESD 分类等级 2
  - 器件组件充电模式 (CDM) ESD 分类等级 C6
- 3V 至 75V 的超宽输入电压范围
- 仿真峰值电流模式控制
- 在降压和升压模式之间平滑转换
- 开关频率最高可通过编程设定为 500kHz
- 振荡器同步功能
- 内部高电压偏置稳压器
- 集成了高侧和低侧栅极驱动器
- 可编程软启动时间
- 超低关断电流
- 使能输入宽带宽误差放大器
- 1.5% 反馈基准精度
- 热关断
- 封装：20 引脚 HTSSOP（裸露焊盘）
- 结合使用 LM5118-Q1 和 WEBENCH® 电源设计器创建定制设计

2 应用

- 车用信息娱乐
- 汽车启动和停止系统
- 工业降压/升压电源

3 说明

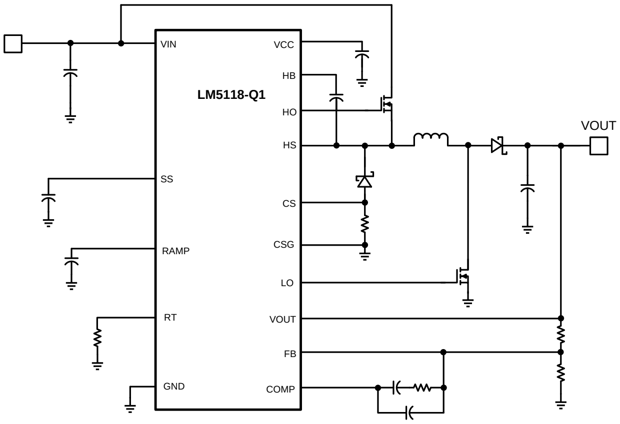
LM5118-Q1 宽电压范围降压/升压开关稳压控制器 具有 使用最少外部组件实现高性能且具成本效益的降压/升压稳压器所需的所有功能。当输入电压低于或高于输出电压时，降压/升压拓扑可使输出电压保持稳定，因此，这款器件非常适合汽车 应用。当输入电压比调节后的输出电压足够大时，LM5118-Q1 将作为降压稳压器运行，然后随着输入电压接近输出电压逐渐过渡到相应的降压/升压模式。这种双模式方法可在宽输入电压范围内保持稳压，并且在降压模式下提供最佳的转换效率，同时在模式转换期间提供无干扰的输出。该控制器易于使用，其中包含适用于高侧降压 MOSFET 和低侧升压 MOSFET 的驱动器。此稳压器控制方法基于采用仿真电流斜坡的电流模式控制。仿真电流模式控制可降低脉冲宽调制电路的噪声敏感度，以便可靠地控制高输入电压 应用中所需的极小占空比。额外保护 功能 包括电流限制、热关断和使能输入。该器件采用功耗增强型 20 引脚 HTSSOP 封装，并且配有利于散热的裸露芯片连接焊盘。

器件信息(1)

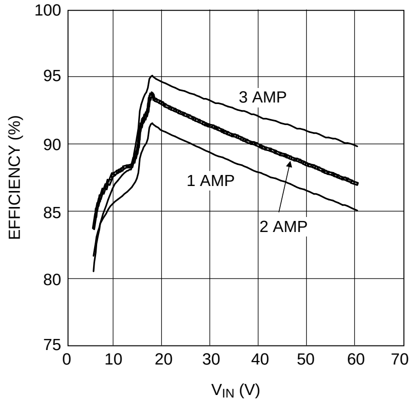
器件型号	封装	封装尺寸（标称值）
LM5118-Q1	HTSSOP (20)	6.50mm x 4.40mm

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。

简化电路原理图



效率与输入电压和输出电流（输出电压 = 12V）



English Data Sheet: SNVSAX9

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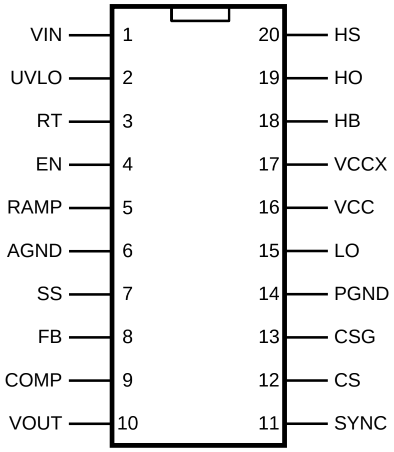
4 修订历史记录

注：之前版本的页码可能与当前版本有所不同。

日期	修订版本	说明
2017 年 6 月	*	初始发行版。将 SNVS566 中的汽车器件移到了单独的产品说明书中

5 Pin Configuration and Functions

PWP Package
20-Pin HTSSOP
(Top View)



Pin Descriptions

PIN		TYPE[1]	DESCRIPTION
NO.	NAME		
1	VIN	P/I	Input supply voltage.
2	UVLO	I	If the UVLO pin is below 1.23 V, the regulator will be in standby mode (VCC regulator running, switching regulator disabled). When the UVLO pin exceeds 1.23 V, the regulator enters the normal operating mode. An external voltage divider can be used to set an undervoltage shutdown threshold. A fixed 5-µA current is sourced out of the UVLO pin. If a current limit condition exists for 256 consecutive switching cycles, an internal switch pulls the UVLO pin to ground and then releases.
3	RT	I	The internal oscillator frequency is set with a single resistor between this pin and the AGND pin. The recommended frequency range is 50 kHz to 500 kHz.
4	EN	I	If the EN pin is below 0.5 V, the regulator will be in a low power state drawing less than 10 µA from VIN. EN must be raised above 3 V for normal operation.
5	RAMP	I	Ramp control signal. An external capacitor connected between this pin and the AGND pin sets the ramp slope used for emulated current mode control.
6	AGND	G	Analog ground.
7	SS	I	Soft Start. An external capacitor and an internal 10-µA current source set the rise time of the error amp reference. The SS pin is held low when VCC is less than the VCC undervoltage threshold (< 3.7 V), when the UVLO pin is low (< 1.23 V), when EN is low (< 0.5 V) or when thermal shutdown is active.
8	FB	I	Feedback signal from the regulated output. Connect to the inverting input of the internal error amplifier.
9	COMP	O	Output of the internal error amplifier. The loop compensation network should be connected between COMP and the FB pin.
10	VOUT	I	Output voltage monitor for emulated current mode control. Connect this pin directly to the regulated output.
11	SYNC	I	Sync input for switching regulator synchronization to an external clock.
12	CS	I	Current sense input. Connect to the diode side of the current sense resistor.
13	CSG	I	Current sense ground input. Connect to the ground side of the current sense resistor.
14	PGND	G	Power Ground.
15	LO	O	Boost MOSFET gate drive output. Connect to the gate of the external boost MOSFET.
16	VCC	P/I/O	Output of the bias regulator. Locally decouple to PGND using a low ESR/ESL capacitor located as close to the controller as possible.
17	VCCX	P/I	Optional input for an externally supplied bias supply. If the voltage at the VCCX pin is greater than 3.9 V, the internal VCC regulator is disabled and the VCC pin is internally connected to VCCX pin supply. If VCCX is not used, connect to AGND.

---

(1) G = Ground, I = Input, O = Output, P = Power

Pin Descriptions (continued)

PIN		TYPE[1]	DESCRIPTION
NO.	NAME		
18	HB	I	High-side gate driver supply used in bootstrap operation. The bootstrap capacitor supplies current to charge the high-side MOSFET gate. This capacitor should be placed as close to the controller as possible and connected between HB and HS.
19	HO	O	Buck MOSFET gate drive output. Connect to the gate of the high-side buck MOSFET through a short, low inductance path.
20	HS	I	Buck MOSFET source pin. Connect to the source terminal of the high-side buck MOSFET and the bootstrap capacitor.
—	EP	—	Solder to the ground plane under the IC to aid in heat dissipation.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free air temperature range (unless otherwise noted)(1)

	MIN	MAX	UNIT
VIN, EN, VOUT to GND	–0.3	76	V
VCC, LO, VCCX, UVLO to GND	–0.3	15	V
HB to HS	–0.3	15	V
HO to HS	–0.3	HB + 0.3	V
HS to GND	–4	76	V
CSG, CS to GND	–0.3	0.3	V
RAMP, SS, COMP, FB, SYNC, RT to GND	–0.3	7	V
Junction temperature	–40	150	°C
Storage temperature, T_{stg}	–55	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002(1)	±2000	V
		Charged-device model (CDM), per AEC Q100-011	±1000	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.3 Recommended Operating Conditions

over operating free air temperature range (unless otherwise noted)(1)

	MIN	MAX	UNIT
VIN (2)	3	75	V
VCC, VCCX	4.75	14	V
Junction temperature	–40	+125	°C

(1) The *Recommended Operating Conditions* indicate conditions for which the device is intended to be functional, but does not ensure specific performance limits. For specifications and test conditions see *Electrical Characteristics*.
(2) 5-V VIN is required to initially start the controller.

6.4 Thermal Information

THERMAL METRIC(1)		LM5118-Q1 PWP (HTSSOP) 20 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	40	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	4	°C/W

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report.

6.5 Electrical Characteristics

Unless otherwise specified, the following conditions apply: VIN = 48 V, VCCX = 0 V, EN = 5 V, RT = 29.11 kΩ, No load on LO and HO. Typical values apply for T_J = 25°C; minimum and maximum values apply over the full junction temperature range for operation, −40°C to +125°C.(1)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
VIN SUPPLY						
I_{BIAS}	VIN operating current	VCCX = 0 V		4.5	5.5	mA
I_{BIASX}	VIN operating current	VCCX = 5 V		1	1.85	mA
I_{STDBY}	VIN shutdown current	EN = 0 V		1	10	µA
VCC REGULATOR						
$V_{CC(REG)}$	VCC regulation	VCCX = 0 V	6.8	7	7.2	V
$V_{CC(REG)}$	VCC regulation	VCCX = 0 V, VIN = 6 V	5	5.25	5.5	V
	VCC sourcing current limit	VCC = 0	21	35		mA
	VCCX switch threshold	VCCX rising	3.68	3.85	4.02	V
	VCCX switch hysteresis			0.2		V
	VCCX switch RDS(ON)	ICCX = 10 mA		5	12	Ω
	VCCX switch leakage	VCCX = 0 V		0.5	1	µA
	VCCCX pulldown resistance	VCCX = 3 V		70		kΩ
	VCC undervoltage lockout voltage	VCC rising	3.52	3.7	3.86	V
	VCC undervoltage hysteresis			0.21		V
	HB DC bias current	HB-HS = 15 V		205	260	µA
	VC LDO mode turnoff			10		V
EN INPUT						
$V_{IL\ max}$	EN input low threshold				0.5	V
$V_{IH\ min}$	EN input high threshold		3			V
	EN input bias current	VEN = 3 V	–1		1	µA
	EN input bias current	VEN = 0.5 V	–1		1	µA
	EN input bias current	VEN = 75 V		50		µA
UVLO THRESHOLDS						
	UVLO standby threshold	UVLO rising	1.191	1.231	1.271	V
	UVLO threshold hysteresis			0.105		V
	UVLO pullup current source	UVLO = 0 V		5		µA
	UVLO pulldown $R_{DS(ON)}$			100	200	Ω
SOFT START						
	SS current source	SS = 0V	7.5	10.5	13.5	µA
	SS to FB offset	FB = 1.23 V		150		mV
	SS output low voltage	Sinking 100 µA, UVLO = 0 V		7		mV
ERROR AMPLIFIER						
V_{REF}	FB reference voltage	Measured at FB pin, FB = COMP	1.212	1.23	1.248	V
	FB input bias current	FB = 2 V		20	200	nA
	COMP sink/source current		3			mA
A_{OL}	DC gain			80		dB
f_{BW}	Unity bain bandwidth			3		MHz

(1) Minimum and maximum limits are 100% production tested at 25°C. Limits over the operating temperature range are ensured through correlation using Statistical Quality Control (SQC) methods. Limits are used to calculate Average Outgoing Quality Level (AOQL).

Electrical Characteristics (continued)

Unless otherwise specified, the following conditions apply: VIN = 48 V, VCCX = 0 V, EN = 5 V, RT = 29.11 kΩ, No load on LO and HO. Typical values apply for T_J = 25°C; minimum and maximum values apply over the full junction temperature range for operation, −40°C to +125°C.(1)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
PWM COMPARATORS						
$t_{HO(OFF)}$	Forced HO off-time		305	400	495	ns
$T_{ON(MIN)}$	Minimum HO on-time			70		ns
	COMP to comparator offset			200		mV
OSCILLATOR (RT PIN)						
f_{SW1}	Frequency 1	RT = 29.11 kΩ	178	200	224	kHz
f_{SW2}	Frequency 2	RT = 9.525 kΩ	450	515	575	kHz
SYNC						
	Sync threshold falling			1.3		V
CURRENT LIMIT						
$V_{CS(TH)}$	Cycle-by-cycle sense voltage threshold (CS-CSG)	RAMP = 0 buck mode	–103	–125	–147	mV
$V_{CS(THX)}$	Cycle-by-cycle sense voltage threshold (CS-CSG)	RAMP = 0 buck-boost mode	–218	–255	–300	mV
	CS bias current	CS = 0 V		45	60	µA
	CSG bias current	CSG = 0 V		45	60	µA
	Current limit fault timer			256		cycles
RAMP GENERATOR						
I_{R1}	RAMP current 1	VIN = 60 V, VOUT = 10 V	245	305	365	µA
I_{R2}	RAMP current 2	VIN = 12 V, VOUT = 12 V	95	115	135	µA
I_{R3}	RAMP current 3	VIN = 5 V, VOUT = 12 V	65	80	95	µA
	VOUT bias current	VOUT = 48 V		245		µA
LOW-SIDE (LO) GATE DRIVER						
V_{OLL}	LO low-state output voltage	I_{LO} = 100 mA		0.14	0.23	V
V_{OHL}	LO high-state output voltage	I_{LO} = -100 mA $V_{OHL} = V_{CC}\text{-}V_{LO}$		0.25		V
	LO rise time	C-load = 1 nF, VCC = 8 V		16		ns
	LO fall time	C-load = 1 nF, VCC = 8 V		14		ns
I_{OHL}	Peak LO source current	V_{LO} = 0 V, VCC = 8 V		2.2		A
I_{OLL}	Peak LO sink current	V_{LO} = VCC = 8 V		2.7		A
HIGH-SIDE (HO) GATE DRIVER						
V_{OLH}	HO low-state output voltage	I_{HO} = 100 mA		0.135	0.21	V
V_{OHH}	HO high-state output voltage	I_{HO} = -100 mA, $V_{OHH} = V_{HB}\text{-}V_{OH}$		0.25		V
	HO rise time	C-load = 1 nF, VCC = 8 V		14		ns
	HO fall time	C-load = 1 nF, VCC = 8 V		12		ns
I_{OHH}	Peak HO source current	V_{HO} = 0V, VCC = 8 V		2.2		A
I_{OLH}	Peak HO sink current	V_{HO} = VCC = 8 V		3.5		A
	HB-HS undervoltage lockout			3		V

Electrical Characteristics (continued)

Unless otherwise specified, the following conditions apply: VIN = 48 V, VCCX = 0 V, EN = 5 V, RT = 29.11 kΩ, No load on LO and HO. Typical values apply for T_J = 25°C; minimum and maximum values apply over the full junction temperature range for operation, −40°C to +125°C.(1)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
BUCK-BOOST CHARACTERISTICS						
	Buck-boost mode	Buck duty cycle (2)	69%	75%	80%	
THERMAL						
T_{SD}	Thermal shutdown temperature			165		°C
	Thermal shutdown hysteresis			25		°C

(2) When the duty cycle exceeds 75%, the LM5118-Q1 controller gradually phases into the Buck-Boost mode.

6.6 Typical Characteristics

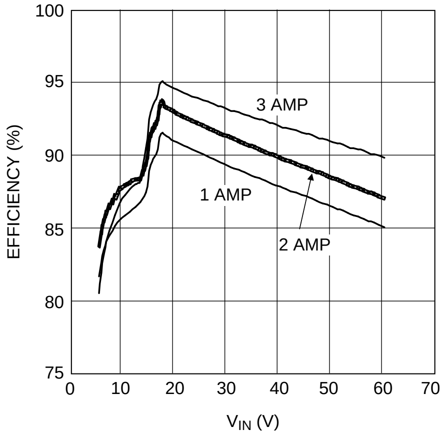


Figure 1. Efficiency vs VIN and IOUT, VOUT = 12 V

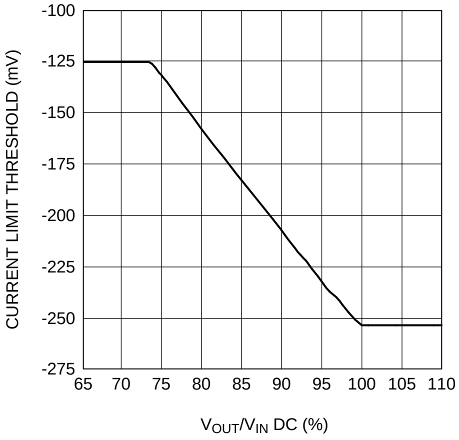


Figure 2. Current Limit Threshold vs VOUT/VIN VOUT = 12 V

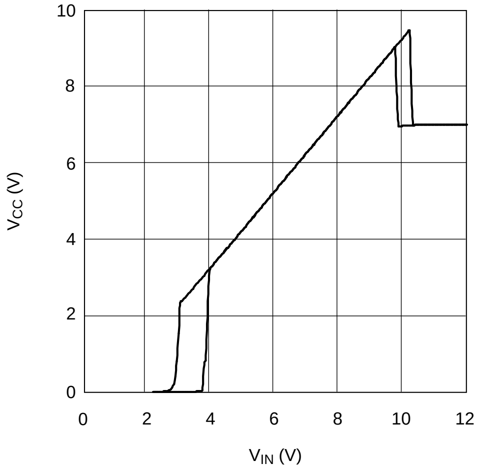


Figure 3. VCC vs VIN

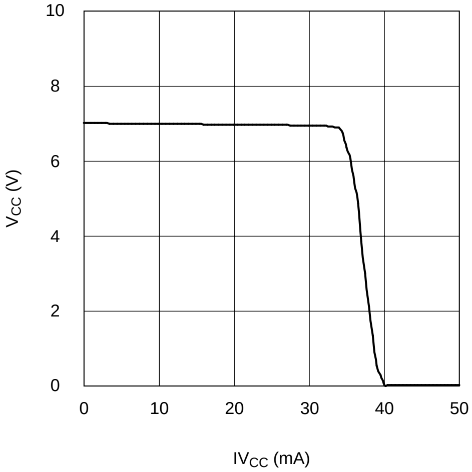


Figure 4. VCC vs IVCC

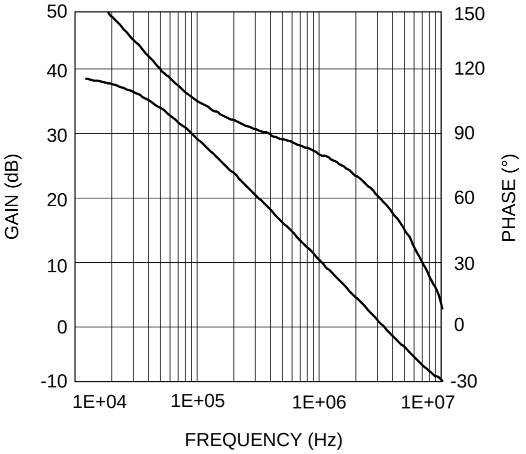


Figure 5. Error Amplifier Gain/Phase

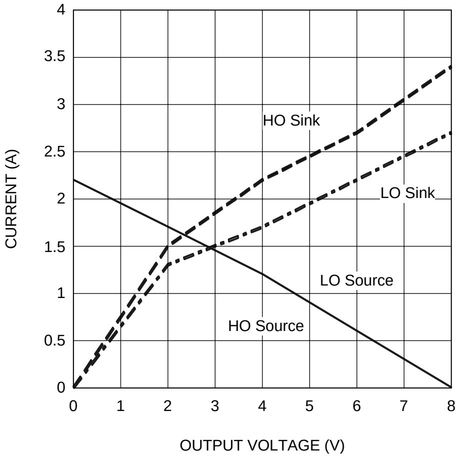


Figure 6. LO and HO Peak Gate Current vs Output Voltage VCC = 8 V

Typical Characteristics (continued)

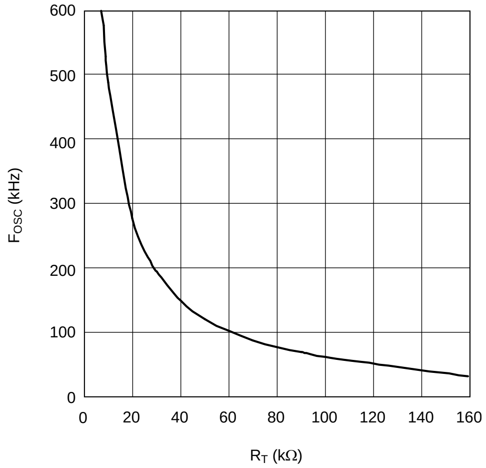


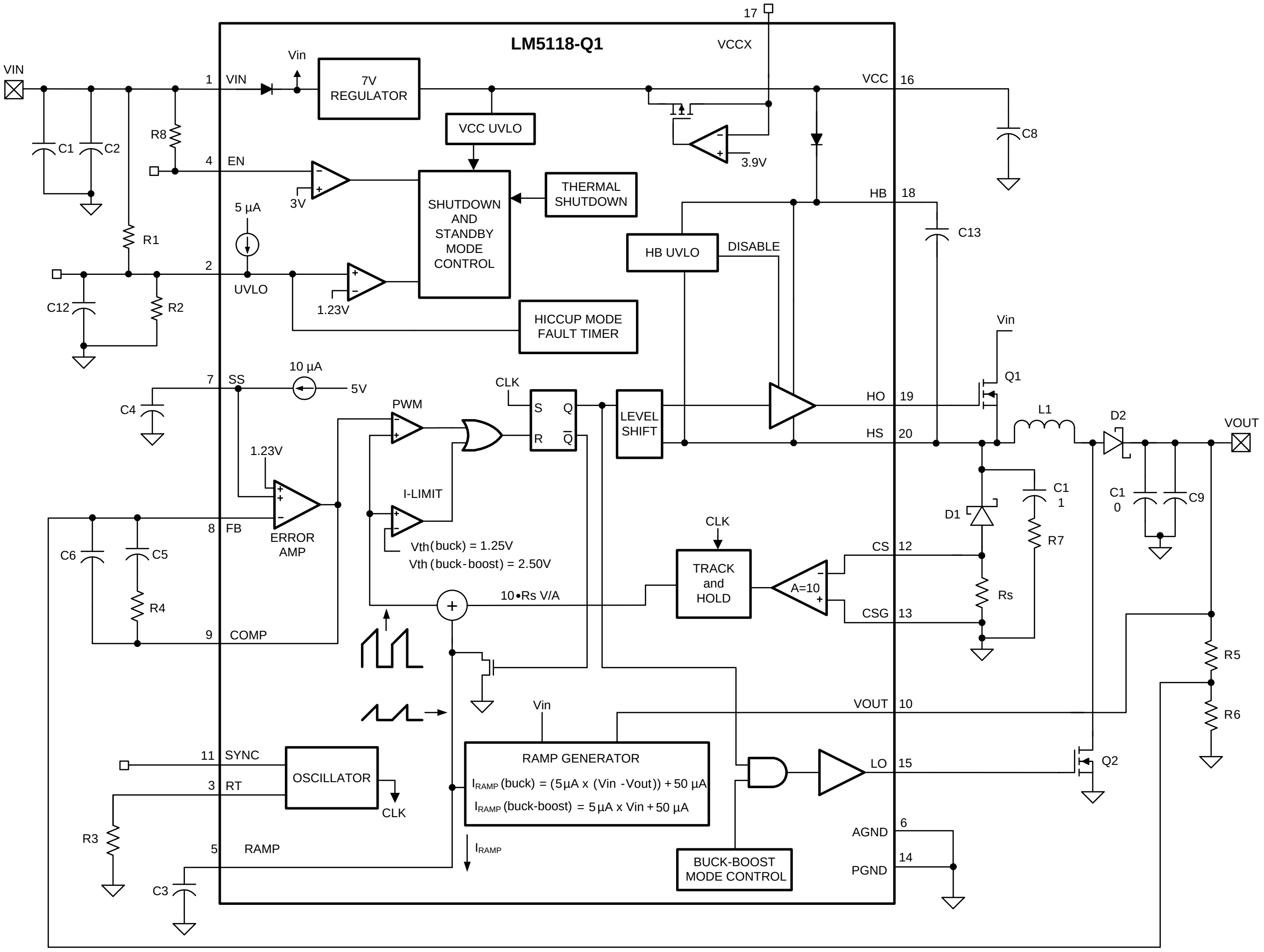
Figure 7. Oscillator Frequency vs RT

7 Detailed Description

7.1 Overview

The LM5118-Q1 high voltage switching regulator features all of the functions necessary to implement an efficient high voltage buck or buck-boost regulator using a minimum of external components. The regulator switches smoothly from buck to buck-boost operation as the input voltage approaches the output voltage, allowing operation with the input greater than or less than the output voltage. This easy to use regulator integrates high-side and low-side MOSFET drivers capable of supplying peak currents of 2 A. The regulator control method is based on current mode control using an emulated current ramp. Peak current mode control provides inherent line feed-forward, cycle-by-cycle current limiting and ease of loop compensation. The use of an emulated control ramp reduces noise sensitivity of the pulse-width modulation circuit, allowing reliable processing of very small duty cycles necessary in high input voltage applications. The operating frequency is user programmable from 50 kHz to 500 kHz. An oscillator synchronization pin allows multiple LM5118-Q1 regulators to self synchronize or be synchronized to an external clock. Fault protection features include current limiting, thermal shutdown, and remote shutdown capability. An undervoltage lockout input allows regulator shutdown when the input voltage is below a user selected threshold, and a low state at the enable pin will put the regulator into an extremely low current shutdown state. The device is available in the HTSSOP-20EP package featuring an exposed pad to aid in thermal dissipation.

7.2 Functional Block Diagram



7.3 Feature Description

A buck-boost regulator can maintain regulation for input voltages either higher or lower than the output voltage. The challenge is that buck-boost power converters are not as efficient as buck regulators. The LM5118-Q1 has been designed as a dual-mode controller whereby the power converter acts as a buck regulator while the input voltage is above the output. As the input voltage approaches the output voltage, a gradual transition to the buck-boost mode occurs. The dual-mode approach maintains regulation over a wide range of input voltages, while maintaining the optimal conversion efficiency in the normal buck mode. The gradual transition between modes eliminates disturbances at the output during transitions. Figure 8 shows the basic operation of the LM5118-Q1 regulator in the buck mode. In buck mode, transistor Q1 is active and Q2 is disabled. The inductor current ramps in proportion to the VIN – VOUT voltage difference when Q1 is active and ramps down through the recirculating diode D1 when Q1 is off. The first order buck mode transfer function is VOUT/VIN = D, where D is the duty cycle of the buck switch, Q1.

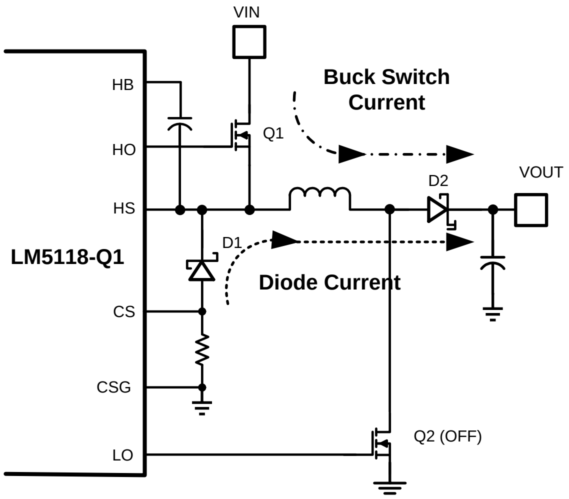


Figure 8. Buck Mode Operation

Feature Description (continued)

Figure 9 shows the basic operation of buck-boost mode. In buck-boost mode both Q1 and Q2 are active for the same time interval each cycle. The inductor current ramps up (proportional to VIN) when Q1 and Q2 are active and ramps down through the recirculating diode during the off time. The first order buck-boost transfer function is VOUT/VIN = D/(1-D), where D is the duty cycle of Q1 and Q2.

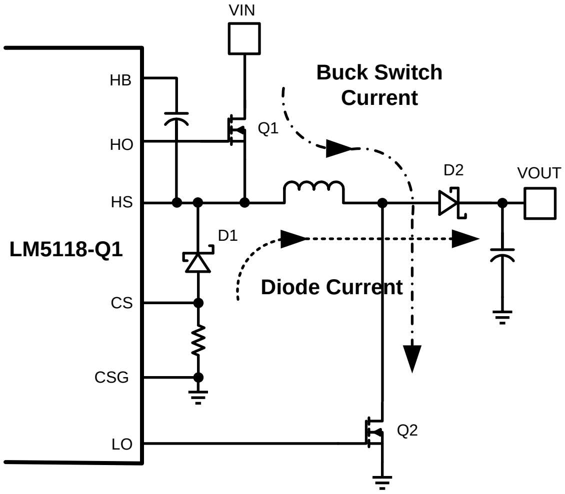


Figure 9. Buck-Boost Mode Operation

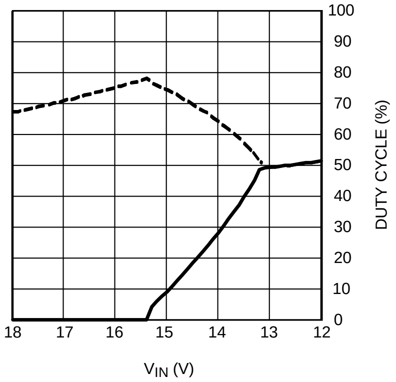


Figure 10. Mode Dependence on Duty Cycle (VOUT = 12 V)

7.3.1 UVLO

An undervoltage lockout pin is provided to disable the regulator when the input is below the desired operating range. If the UVLO pin is below 1.13 V, the regulator enters a standby mode with the outputs disabled, but with VCC regulator operating. If the UVLO input exceeds 1.23 V, the regulator will resume normal operation. A voltage divider from the input to ground can be used to set a VIN threshold to disable the regulator in brownout conditions or for low input faults.

Feature Description (continued)

If a current limit fault exists for more than 256 clock cycles, the regulator will enter a *hiccup* mode of current limiting and the UVLO pin will be pulled low by an internal switch. This switch turns off when the UVLO pin approaches ground potential allowing the UVLO pin to rise. A capacitor connected to the UVLO pin will delay the return to a normal operating level and thereby set the off-time of the hiccup mode fault protection. An internal 5-µA pullup current pulls the UVLO pin to a high state to ensure normal operation when the VIN UVLO function is not required and the pin is left floating.

7.3.2 Oscillator and Sync Capability

The LM5118-Q1 oscillator frequency is set by a single external resistor connected between the RT pin and the AGND pin. The R_T resistor should be located very close to the device and connected directly to the pins of the IC. To set a desired oscillator frequency (f), the necessary value for the R_T resistor can be calculated from Equation 1:

$$R_T = \frac{6.4 \times 10^9}{f} - 3.02 \times 10^3 \tag{1}$$

The SYNC pin can be used to synchronize the internal oscillator to an external clock. The external clock must be of higher frequency than the free-running frequency set by the R_T resistor. A clock circuit with an open-drain output is the recommended interface from the external clock to the SYNC pin. The clock pulse duration should be greater than 15 ns.

Multiple LM5118-Q1 devices can be synchronized together simply by connecting the SYNC pins together as in Figure 11. In this configuration, all of the devices are synchronized to the highest frequency device. Figure 12 shows the SYNC input and output features of the LM5118-Q1. The internal oscillator circuit drives the SYNC pin with a strong pull down or weak pullup inverter. When the SYNC pin is pulled low, either by the internal oscillator or an external clock, the ramp cycle of the oscillator is terminated and forced 400 ns off-time is initiated before a new oscillator cycle begins. If the SYNC pins of several LM5118-Q1 IC’s are connected together, the IC with the highest internal clock frequency will pull all the connected SYNC pins low and terminate the oscillator ramp cycles of the other ICs. The LM5118-Q1 with the highest programmed clock frequency will serve as the master and control the switching frequency of all the devices with lower oscillator frequencies.

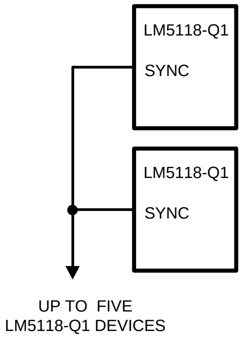


Figure 11. Sync From Multiple Devices

Feature Description (continued)

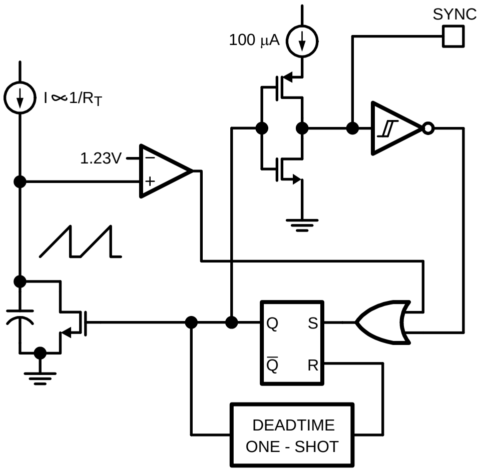


Figure 12. Simplified Oscillator and Block Diagram With Sync I/O Circuit

7.3.3 Error Amplifier and PWM Comparator

The internal high gain error amplifier generates an error signal proportional to the difference between the regulated output voltage and an internal precision reference (1.23 V). The output of the error amplifier is connected to the COMP pin. Loop compensation components, typically a type II network shown in are connected between the COMP and FB pins. This network creates a low frequency pole, a zero, and a noise reducing high frequency pole. The PWM comparator compares the emulated current sense signal from the RAMP generator to the error amplifier output voltage at the COMP pin. The same error amplifier is used for operation in buck and buck-boost mode.

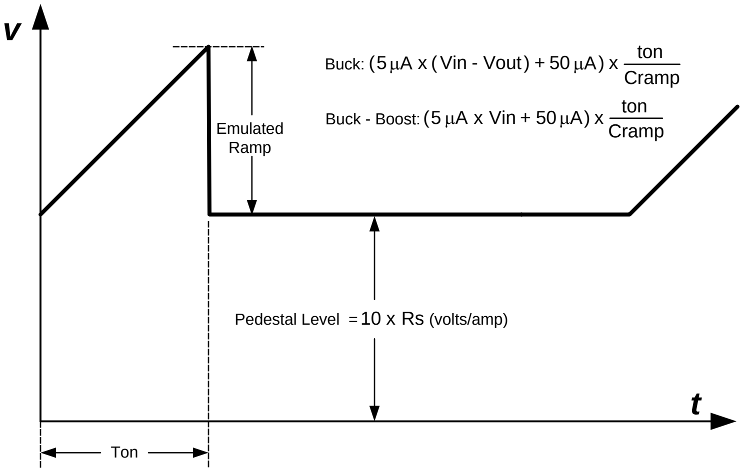


Figure 13. Composition of Emulated Current Signal

Feature Description (continued)

7.3.4 Ramp Generator

The ramp signal of a pulse-width modulator with current mode control is typically derived directly from the buck switch drain current. This switch current corresponds to the positive slope portion of the inductor current signal. Using this signal for the PWM ramp simplifies the control loop transfer function to a single pole response and provides inherent input voltage feed-forward compensation. The disadvantage of using the buck switch current signal for PWM control is the large leading edge spike due to circuit parasitics. The leading edge spike must be filtered or blanked to avoid early termination of the PWM pulse. Also, the current measurement may introduce significant propagation delays. The filtering, blanking time and propagation delay limit the minimal achievable pulse width. In applications where the input voltage may be relatively large in comparison to the output voltage, controlling a small pulse width is necessary for regulation. The LM5118-Q1 uses a unique ramp generator which does not actually measure the buck switch current but instead creates a signal representing or emulating the inductor current. The emulated ramp provides signal to the PWM comparator that is free of leading edge spikes and measurement or filtering delays. The current reconstruction is comprised of two elements, a sample-and-hold pedestal level and a ramp capacitor which is charged by a controlled current source. Refer to Figure 13 for details.

The sample-and-hold pedestal level is derived from a measurement of the recirculating current through a current sense resistor in series with the recirculating diode of the buck regulator stage. A small value current sensing resistor is required between the recirculating diode anode and ground. The CS and CSG pins should be Kelvin connected directly to the sense resistor. The voltage level across the sense resistor is sampled and held just prior to the onset of the next conduction interval of the buck switch. The current sensing and sample-and-hold provide the DC level of the reconstructed current signal. The sample and hold of the recirculating diode current is valid for both buck and buck-boost modes. The positive slope inductor current ramp is emulated by an external capacitor connected from the RAMP pin to the AGND and an internal voltage controlled current source. In buck mode, the ramp current source that emulates the inductor current is a function of the VIN and VOUT voltages per Equation 2:

$$I_{RAMP}\text{ (buck)} = \frac{5\ \mu A}{V} \times (VIN - VOUT) + 50\ \mu A \tag{2}$$

In buck-boost mode, the ramp current source is a function of the input voltage VIN, per Equation 3:

$$I_{RAMP}\text{ (buck - boost)} = \frac{5\ \mu A}{V} \times VIN + 50\ \mu A \tag{3}$$

Proper selection of the RAMP capacitor (C_{RAMP}) depends upon the value of the output inductor (L) and the current sense resistor (R_S). For proper current emulation, the sample and hold pedestal value and the ramp amplitude must have the same relative relationship to the actual inductor current. That is:

$$R_S \times A = \frac{g_m \times L}{C_{RAMP}}$$

$$C_{RAMP} = \frac{g_m \times L}{A \times R_S}$$

where

- g_m is the ramp generator transconductance (5 µA/V)
- A is the current sense amplifier gain (10V/V) (4)

The ramp capacitor should be located very close to the device and connected directly to the RAMP and AGND pins.

Feature Description (continued)

The relationship between the average inductor current and the pedestal value of the sampled inductor current can cause instability in certain operating conditions. This instability is known as sub-harmonic oscillation, which occurs when the inductor ripple current does not return to its initial value by the start of the next switching cycle. Sub-harmonic oscillation is normally characterized by observing alternating wide and narrow pulses at the switch node. Adding a fixed slope voltage ramp (slope compensation) to the current sense signal prevents this oscillation. The 50 µA of offset current provided from the emulated current source adds enough slope compensation to the ramp signal for output voltages less than or equal to 12 V. For higher output voltages, additional slope compensation may be required. In such applications, the ramp capacitor can be decreased from the nominal calculated value to increase the ramp slope compensation.

The pedestal current sample is obtained from the current sense resistor (Rs) connected to the CS and CSG pins. It is sometimes helpful to adjust the internal current sense amplifier gain (A) to a lower value in order to obtain the higher current limit threshold. Adding a pair of external resistors RG in a series with CS and CSG as in Figure 14 reduces the current sense amplifier gain A according to Equation 5:

$$A = \frac{10k}{1k + R_G} \tag{5}$$

7.3.5 Current Limit

In the buck mode the average inductor current is equal to the output current (IOUT). In buck-boost mode the average inductor current is approximately equal to:

$$\text{Iout x} \left(1 + \frac{\text{VOUT}}{\text{VIN}}\right) \tag{6}$$

Consequently, the inductor current in buck-boost mode is much larger especially when VOUT is large relative to VIN. The LM5118-Q1 provides a current monitoring scheme to protect the circuit from possible over-current conditions. When set correctly, the emulated current sense signal is proportional to the buck switch current with a scale factor determined by the current sense resistor. The emulated ramp signal is applied to the current limit comparator. If the peak of the emulated ramp signal exceeds 1.25 V when operating in the buck mode, the PWM cycle is immediately terminated (cycle-by-cycle current limiting). In buck-boost mode the current limit threshold is increased to 2.50 V to allow higher peak inductor current. To further protect the external switches during prolonged overload conditions, an internal counter detects consecutive cycles of current limiting. If the counter detects 256 consecutive current limited PWM cycles, the LM5118-Q1 enters a low power dissipation hiccup mode. In the hiccup mode, the output drivers are disabled, the UVLO pin is momentarily pulled low, and the soft-start capacitor is discharged. The regulator is restarted with a normal soft-start sequence once the UVLO pin charges back to 1.23 V. The hiccup mode off-time can be programmed by an external capacitor connected from UVLO pin to ground. This hiccup cycle will repeat until the output overload condition is removed.

In applications with low output inductance and high input voltage, the switch current may overshoot due to the propagation delay of the current limit comparator and control circuitry. If an overshoot should occur, the sample-and-hold circuit will detect the excess recirculating diode current. If the sample-and-hold pedestal level exceeds the internal current limit threshold, the buck switch will be disabled and will skip PWM cycles until the inductor current has decayed below the current limit threshold. This approach prevents current runaway conditions due to propagation delays or inductor saturation since the inductor current is forced to decay before the buck switch is turned on again.

Feature Description (continued)

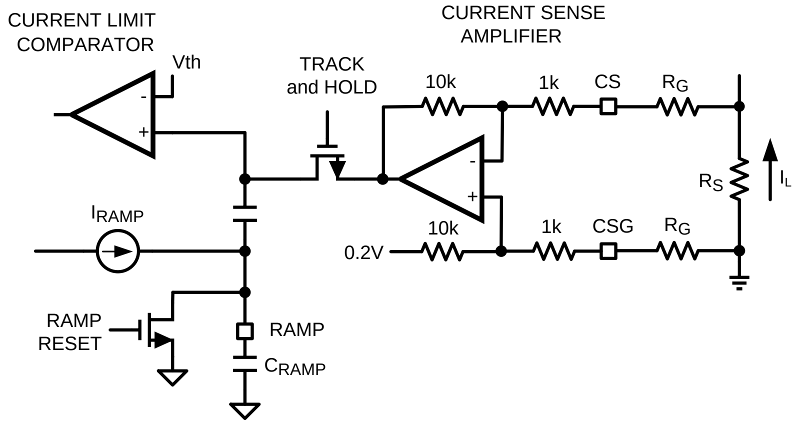


Figure 14. Current Limit and Ramp Circuit

7.3.6 Maximum Duty Cycle

Each conduction cycle of the buck switch is followed by a forced minimum off-time of 400 ns to allow sufficient time for the recirculating diode current to be sampled. This forced off-time limits the maximum duty cycle of the controller. The actual maximum duty cycle will vary with the operating frequency as follows:

$$D_{MAX} = 1 - f \times 400 \times 10^{-9}$$

where

- f is the oscillator frequency in Hz (7)

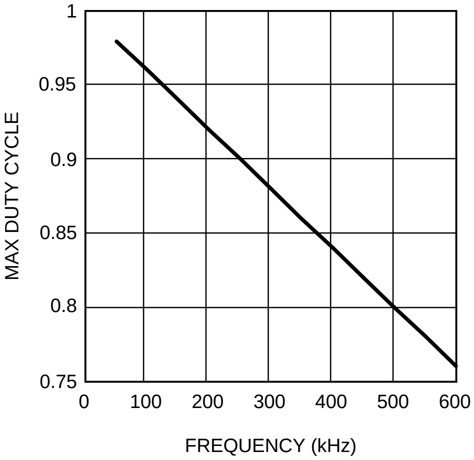


Figure 15. Maximum Duty Cycle vs Frequency

Limiting the maximum duty cycle will limit the maximum boost ratio (VOUT/VIN) while operating in buck-boost mode. For example, from Figure 15, at an operating frequency of 500 kHz, D_{MAX} is 80%. Using the buck-boost transfer function.

$$D = \frac{Vout}{Vin + Vout} \tag{8}$$

With D = 80%, solving for VOUT results in:

$$VOUT = 4 \times VIN \tag{9}$$

Feature Description (continued)

With a minimum input voltage of 5 V, the maximum possible output voltage is 20 V at f = 500 kHz. The buck-boost step-up ratio can be increased by reducing the operating frequency which increases the maximum duty cycle.

7.3.7 Soft Start

The soft-start feature allows the regulator to gradually reach the initial steady-state operating point, thus reducing start-up stresses and surges. The internal 10-µA soft-start current source gradually charges an external soft-start capacitor connected to the SS pin. The SS pin is connected to the positive input of the internal error amplifier. The error amplifier controls the pulse-width modulator such that the FB pin approximately equals the SS pin as the SS capacitor is charged. Once the SS pin voltage exceeds the internal 1.23-V reference voltage, the error amp is controlled by the reference instead of the SS pin. The SS pin voltage is clamped by an internal amplifier at a level of 150 mV above the FB pin voltage. This feature provides a soft-start controlled recovery in the event a severe overload pulls the output voltage (and FB pin) well below normal regulation but does not persist for 256 clock cycles.

Various sequencing and tracking schemes can be implemented using external circuits that limit or clamp the voltage level of the SS pin. The SS pin acts as a non-inverting input to the error amplifier anytime SS voltage is less than the 1.23-V reference. In the event a fault is detected (overtemperature, VCC undervoltage, hiccup current limit), the soft-start capacitor will be discharged. When the fault condition is no longer present, a new soft-start sequence will begin.

7.3.8 HO Output

The LM5118-Q1 contains a high-side, high-current gate driver and associated high voltage level shift. This gate driver circuit works in conjunction with an internal diode and an external bootstrap capacitor. A 0.1-µF ceramic capacitor, connected with short traces between the HB pin and HS pin is recommended for most circuit configurations. The size of the bootstrap capacitor depends on the gate charge of the external FET. During the off time of the buck switch, the HS pin voltage is approximately –0.5 V and the bootstrap capacitor is charged from VCC through the internal bootstrap diode. When operating with a high PWM duty cycle, the buck switch will be forced off each cycle for 400 ns to ensure that the bootstrap capacitor is recharged.

7.3.9 Thermal Protection

Internal Thermal Shutdown circuitry is provided to protect the integrated circuit in the event the maximum junction temperature is exceeded. When activated, typically at 165°C, the controller is forced into a low power reset state, disabling the output driver and the bias regulator. This protection is provided to prevent catastrophic failures from accidental device overheating.

7.4 Device Functional Modes

Figure 10 shows how duty cycle effects the operational mode and is useful for reference in the following discussions. Initially, only the buck switch is active and the buck duty cycle increases to maintain output regulation as VIN decreases. When VIN is approximately equal to 15.5 V, the boost switch begins to operate with a low duty cycle. If VIN continues to fall, the boost switch duty cycle increases and the buck switch duty cycle decreases until they become equal at VIN = 13.2 V.

7.4.1 Buck Mode Operation: VIN > VOUT

The LM5118-Q1 buck-boost regulator operates as a conventional buck regulator with emulated current mode control while VIN is greater than VOUT and the buck mode duty cycle is less than 75%. In buck mode, the LO gate drive output to the boost switch remains low.

Device Functional Modes (continued)

7.4.2 Buck-Boost Mode Operation: VIN ≅ VOUT

When VIN decreases relative to VOUT, the duty cycle of the buck switch will increase to maintain regulation. Once the duty cycle reaches 75%, the boost switch starts to operate with a very small duty cycle. As VIN is further decreased, the boost switch duty cycle increases until it is the same as the buck switch. As VIN is further decreased below VOUT, the buck and boost switch operate together with the same duty cycle and the regulator is in full buck-boost mode. This feature allows the regulator to transition smoothly from buck to buck-boost mode. Note that the regulator can be designed to operate with VIN less than 4 V, but VIN must be at least 5 V Figure 16 presents a timing illustration of the gradual transition from buck to buck-boost mode when the input voltage ramps downward over a few switching cycles.

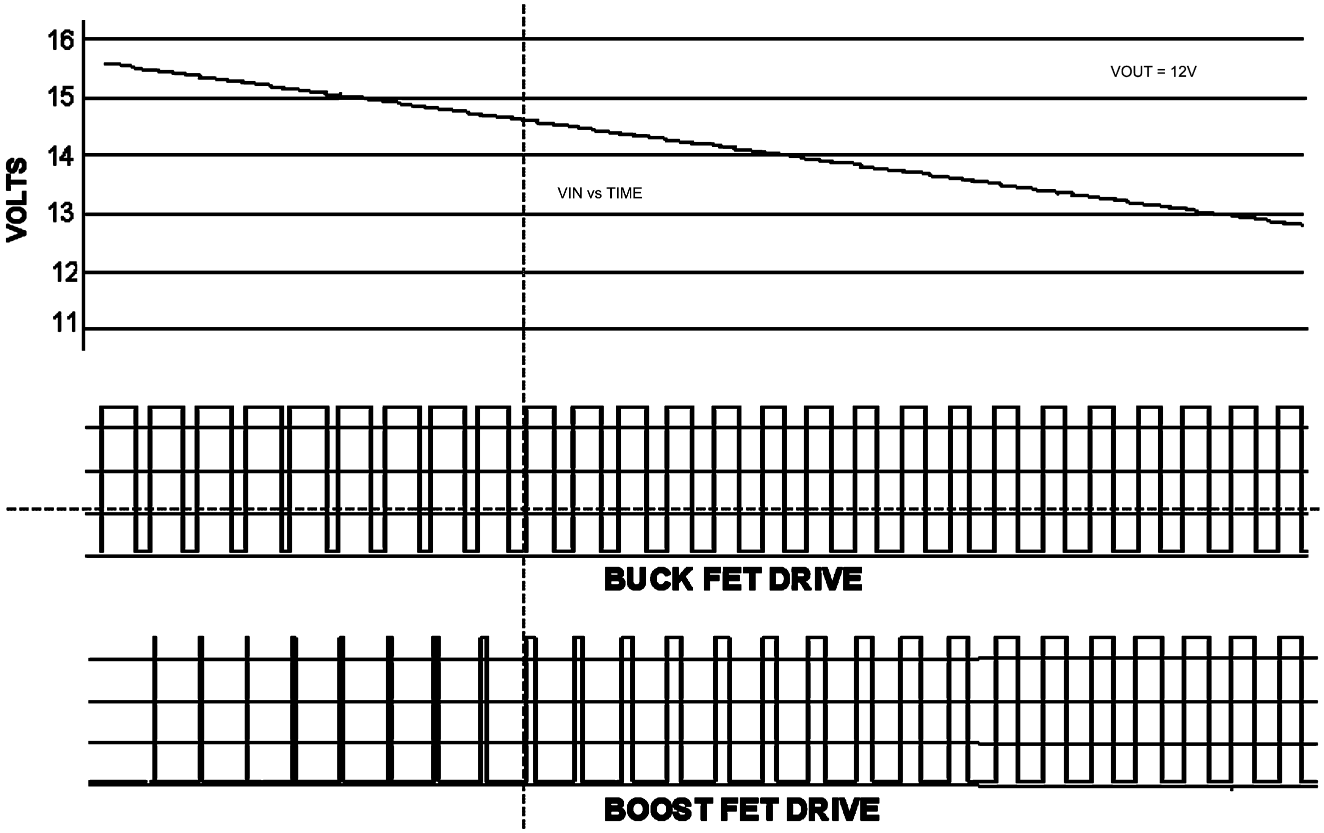


Figure 16. Buck (HO) and Boost (LO) Switch Duty Cycle vs. Time, Illustrating Gradual Mode Change With Decreasing Input Voltage

7.4.3 High Voltage Start-Up Regulator

The LM5118-Q1 contains a dual-mode, high voltage linear regulator that provides the VCC bias supply for the PWM controller and the MOSFET gate driver. The VIN input pin can be connected directly to input voltages as high as 75 V. For input voltages below 10 V, an internal low dropout switch connects VCC directly to VIN. In this supply range, VCC is approximately equal to VIN. For VIN voltages greater than 10 V, the low dropout switch is disabled and the VCC regulator is enabled to maintain VCC at approximately 7 V. A wide operating range of 4 V to 75 V (with a start-up requirement of at least 5 V) is achieved through the use of this dual mode regulator.

The output of the VCC regulator is current limited to 35 mA, typical. Upon power up, the regulator sources current into the capacitor connected to the VCC pin. When the voltage at the VCC pin exceeds the VCC undervoltage threshold of 3.7 V and the UVLO input pin voltage is greater than 1.23 V, the gate driver outputs are enabled and a soft-start sequence begins. The gate driver outputs remain enabled until VCC falls below 3.5 V or the voltage at the UVLO pin falls below 1.13 V.

Device Functional Modes (continued)

In many applications, the regulated output voltage or an auxiliary supply voltage can be applied to the VCCX pin to reduce the IC power dissipation. For output voltages between 4 V and 15 V, VOUT can be connected directly to VCCX. When the voltage at the VCCX pin is greater than 3.85 V, the internal VCC regulator is disabled and an internal switch connects VCCX to VCC, reducing the internal power dissipation.

In high voltage applications, take extrac care to ensure the VIN pin voltage does not exceed the absolute maximum voltage rating of 76 V. During line or load transients, voltage ringing on the VIN line that exceeds the absolute maximum rating can damage the IC. Both careful PCB layout and the use of quality bypass capacitors located close to the VIN and GND pins are essential.

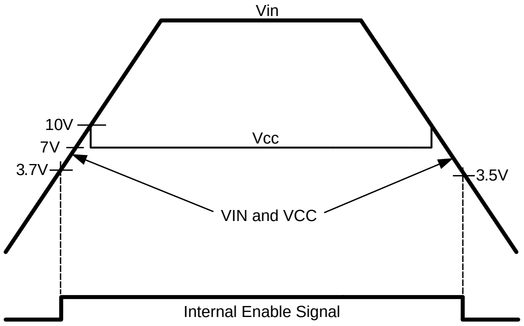


Figure 17. VIN and VCC Sequencing

7.4.4 Enable

The LM5118-Q1 contains an enable function which provides a very low input current shutdown mode. If the EN pin is pulled below 0.5 V, the regulator enters shutdown mode, drawing less than 10 µA from the VIN pin. Raising the EN input above 3 V returns the regulator to normal operation. The EN pin can be tied directly to the VIN pin if this function is not needed. It must not be left floating. A 1-MΩ pullup resistor to VIN can be used to interface with an open-collector or open-drain control signal.

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The LM5118-Q1 high voltage switching regulator features all of the functions necessary to implement an efficient high voltage buck or buck-boost regulator using a minimum of external components. A buck-boost regulator can maintain regulation for input voltages either higher or lower than the output voltage.

8.2 Typical Application

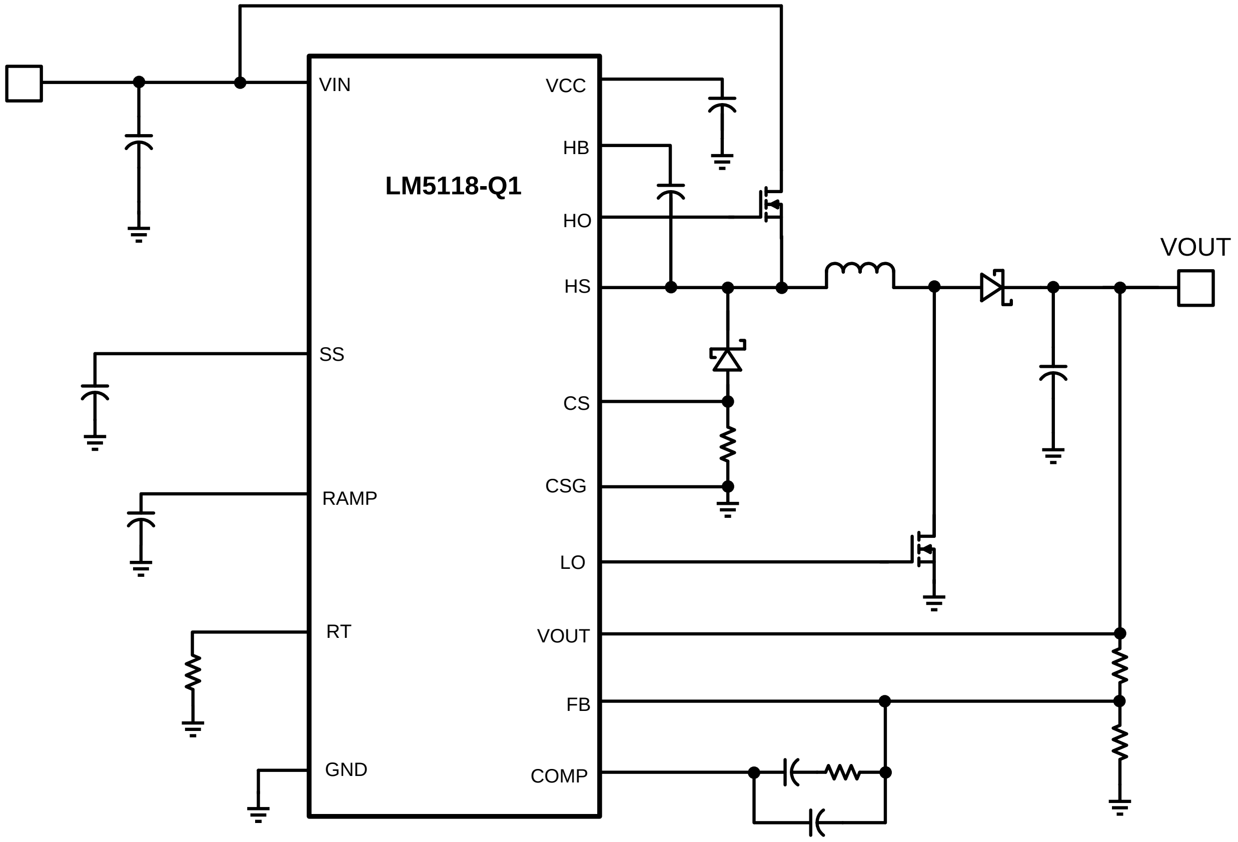


Figure 18. Simplified Application Schematic

Typical Application (continued)

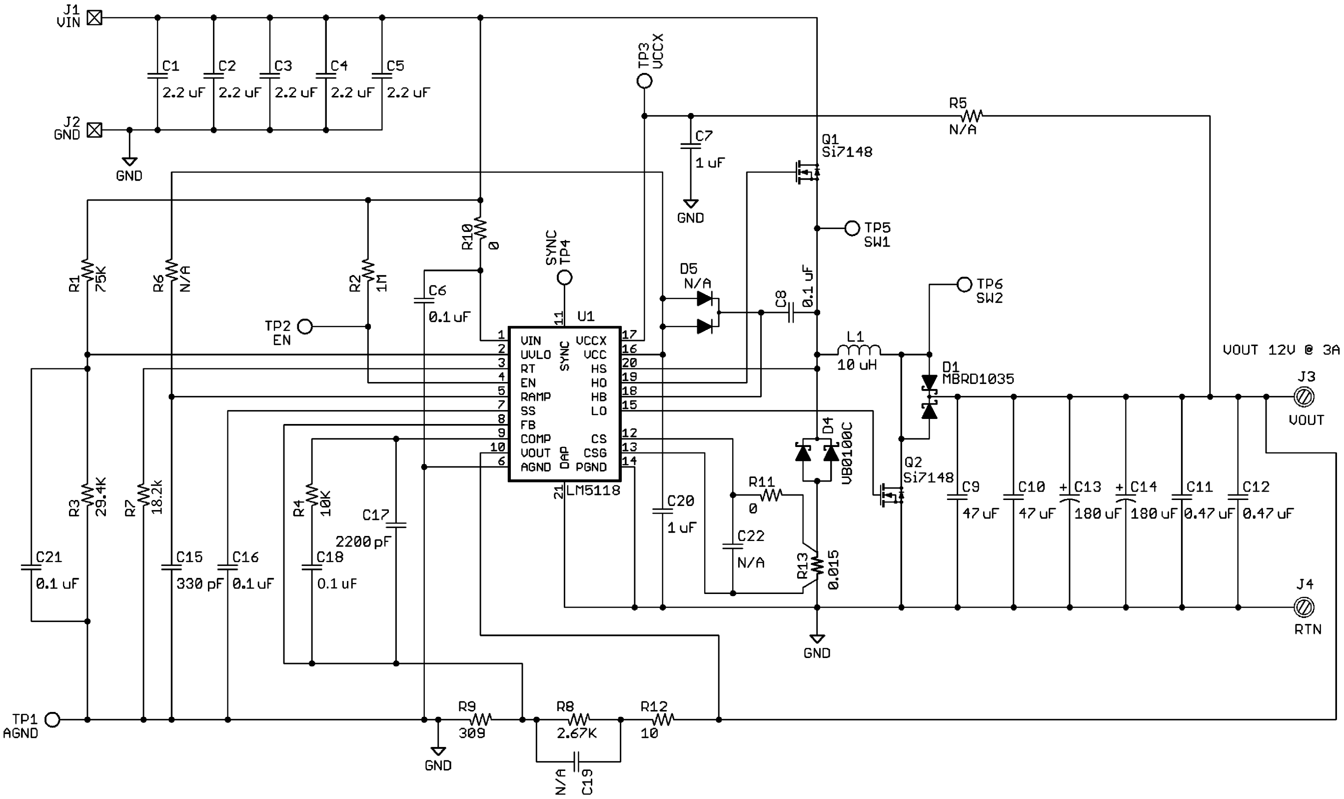


Figure 19. 12-V, 3-A Typical Application Schematic

Typical Application (continued)

8.2.1 Design Requirements

The procedure for calculating the external components is illustrated with the following design example. The designations used in the design example correlate to the Figure 19. The design specifications are:

- VOUT = 12 V
- VIN = 5 V to 42 V
- f = 300 kHz
- Minimum load current (CCM operation) = 600 mA
- Maximum load current = 3 A

8.2.2 Detailed Design Procedure

8.2.2.1 Custom Design With WEBENCH® Tools

Click here to create a custom design using the LM5118-Q1 device with the WEBENCH® Power Designer.

1. Start by entering the input voltage (V_{IN}), output voltage (V_{OUT}), and output current (I_{OUT}) requirements.
2. Optimize the design for key parameters such as efficiency, footprint, and cost using the optimizer dial.
3. Compare the generated design with other possible solutions from Texas Instruments.

The WEBENCH Power Designer provides a customized schematic along with a list of materials with real-time pricing and component availability.

In most cases, these actions are available:

- Run electrical simulations to see important waveforms and circuit performance
- Run thermal simulations to understand board thermal performance
- Export customized schematic and layout into popular CAD formats
- Print PDF reports for the design, and share the design with colleagues

Get more information about WEBENCH tools at www.ti.com/WEBENCH.

8.2.2.2 R7 = R_T

RT sets the oscillator switching frequency. Generally speaking, higher operating frequency applications will use smaller components, but have higher switching losses. An operating frequency of 300 kHz was selected for this example as a reasonable compromise for both component size and efficiency. The value of R_T can be calculated as follows:

$$R_T = \frac{6.4 \times 10^9}{f} - 3.02 \times 10^3 \tag{10}$$

therefore, R7 = 18.3 kΩ

Typical Application (continued)

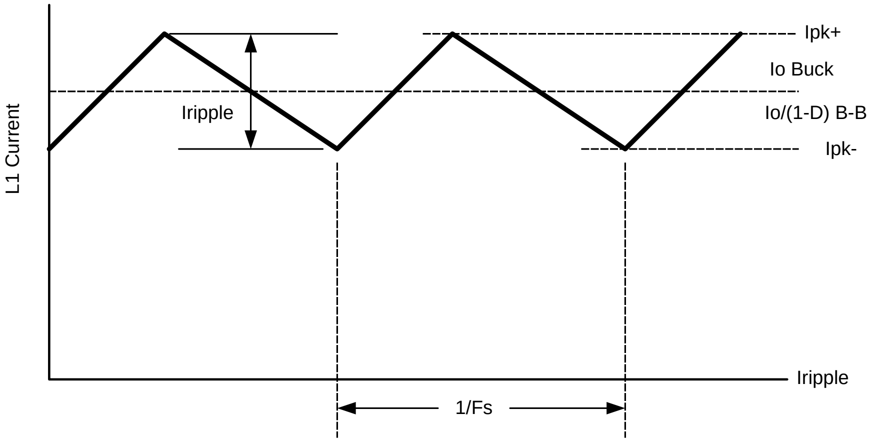


Figure 20. Inductor Current Waveform

Typical Application (continued)

8.2.2.3 Inductor Selection, L1

The inductor value is determined based upon the operating frequency, load current, ripple current and the input and output voltages. Refer to Figure 20 for details.

To keep the circuit in continuous conduction mode (CCM), the maximum ripple current I_{RIPPLE} should be less than twice the minimum load current. For the specified minimum load of 0.6 A, The maximum ripple current is 1.2 Ap-p. Also, the minimum value of L must be calculated both for a buck and buck-boost configurations. The final value of inductance will generally be a compromise between the two modes. It is desirable to have a larger value inductor for buck mode, but the saturation current rating for the inductor must be large for buck-boost mode, resulting in a physically large inductor. Additionally, large value inductors present buck-boost mode loop compensation challenges which will be discussed in the Error Amplifier Configuration section. For the design example, the inductor values in both modes are calculated as:

$$L1 = \frac{V_{OUT}(V_{IN(MAX)} - V_{OUT})}{V_{IN(MAX)} \times f \times I_{RIPPLE}} \text{ Buck Mode}$$

$$L1 = \frac{V_{IN(MIN)}(V_{OUT})}{(V_{OUT} + V_{IN(MIN)}) \times f \times I_{RIPPLE}} \text{ Buck-Boost Mode} \quad (11)$$

where

- V_{OUT} is the output voltage
- $V_{IN(MAX)}$ is the maximum input voltage
- f is the switching frequency
- I_{RIPPLE} is the selected inductor peak to peak ripple current (1.2 A selected for this example)
- $V_{IN(MIN)}$ is the minimum input voltage
- (12)

The resulting inductor values are:

- L1 = 28 µH, Buck Mode
- L1 = 9.8 µH Buck-Boost mode

A 10-µH inductor was selected which is a compromise between these values, while favoring the buck-boost mode. As illustrated in the compensation section below, the inductor value should be as low as possible to move the buck-boost right-half-plane zero to a higher frequency. The ripple current is then rechecked with the selected inductor value using Equation 11 and Equation 12,

$I_{RIPPLE(BUCK)} = 3.36$ A (13)

$I_{RIPPLE(BUCK\text{-}BOOST)} = 1.17$ A (14)

Because the inductor selected is lower than calculated for the Buck mode, the minimum load current for CCM in buck mode is 1.68 A at maximum VIN.

With a 10-µH inductor, the worst case peak inductor currents can be estimated for each case, assuming a 20% inductor value tolerance and assuming 80% efficiency of the converter.

$$I_{1(PEAK)} = \frac{I_{OUT}}{\eta} + \frac{I_{RIPPLE(BUCK)}}{2(1 - L_{TOL})}$$

$$I_{2(PEAK)} = \frac{I_{OUT}(V_{OUT} + V_{IN(MIN)})}{\eta \times V_{IN(MIN)}} + \frac{I_{RIPPLE(BUCK\text{-}BOOST)}}{2(1 - L_{TOL})} \quad (15)$$

where

- η is efficiency
- L_{TOL} is the inductor tolerance (16)

Typical Application (continued)

For this example, Equation 15 and Equation 16 yield:

$$I_{1(PEAK)} = 5.62\ \text{A} \tag{17}$$

$$I_{2(PEAK)} = 13.4\ \text{A} \tag{18}$$

An acceptable current limit setting would be 6.7 A for buck mode because the LM5118-Q1 automatically doubles the current limit threshold in buck-boost mode. The selected inductor must have a saturation current rating at least as high as the buck-boost mode cycle-by-cycle current limit threshold, in this case at least 13.5 A. A 10-µH, 15-A inductor was chosen for this application.

8.2.2.4 R13 = R_{SENSE}

To select the current sense resistor, begin by calculating the minimum K values for each mode using Equation 19 and Equation 20. K represents the slope compensation of the controller and is different for each mode, K_{BUCK} and $K_{BUCK\text{-}BOOST}$.

$$K_{BUCK} \geq 1 + \frac{10}{V_{IN(MAX)} - V_{OUT}} \tag{19}$$

$$K_{BUCK-BOOST} \geq 1 + \frac{10}{V_{IN(MIN)}} \tag{20}$$

- K_{BUCK} = 1.16
- $K_{BUCK\text{-}BOOST}$ = 3

Use Equation 21 and Equation 22 to calculate RSENSE for each mode of operation. A design margin, M, should be selected between 10%-30% to allow for component tolerances. For this design M was selected to be 10%.

$$R13_{(BUCK)} = \frac{1.25(1-M)}{10 \cdot \left(\frac{I_{OUT}}{\eta} + \frac{I_{RIPPLE(BUCK)}}{2}\right) \cdot K_{BUCK}} \tag{21}$$

$$R13_{(BUCK\text{-}BOOST)} = \frac{2.5 \cdot (1-M)}{10 \cdot \left(\frac{V_{IN(MIN)} + V_{OUT}}{V_{IN(MIN)}} \cdot \frac{I_{OUT}}{\eta} + \frac{I_{RIPPLE(BUCK\text{-}BOOST)}}{2}\right) \cdot K_{BUCK\text{-}BOOST}} \tag{22}$$

- $R13_{(BUCK)}$ = 19.75 mΩ
- $R13_{(BUCK\text{-}BOOST)}$ = 15.5 mΩ

An R_{SENSE} value of no more than 15.5 mΩ must be used to ensure the required maximum output current in the buck-boost mode. A standard value of 15 mΩ was selected for this design.

8.2.2.5 C15 = C_{RAMP}

With the inductor value selected, the value of C3 necessary for the emulation ramp circuit is:

$$C15 = C_{RAMP} = \frac{L \times 10^{-6}}{2 \times R_{SENSE}} \tag{23}$$

With the inductance value (L1) selected as 10 µH, the calculated value for C_{RAMP} is 333 pF. A standard value of 330 pF was selected.

Typical Application (continued)

8.2.2.6 Inductor Current Limit Calculation

The current limit for each mode can be calculated using Equation 24 and Equation 26. If the peak current limit is less than the calculated inductor peak current the R13 and C15 need to be recalculated. This can be done by increasing the previous K values or M and reiterating the calculations.

$$I_{LIMIT(BUCK)} = \frac{1.25 - \frac{50 \times 10^{-6} \times V_{OUT}}{C15 \times f \times V_{IN(MAX)}}}{10 \times R13} \quad (24)$$

$$I_{LIMIT(BUCK)} = 7.795\text{ A} \quad (25)$$

$$I_{LIMIT(BUCK\text{-}BOOST)} = \frac{2.5 - \frac{50 \times 10^{-6} \times V_{OUT}}{C15 \times f \times (V_{IN(MIN)} + V_{OUT})}}{10 \times R13} \quad (26)$$

$$I_{LIMIT(BUCK\text{-}BOOST)} = 14.29\text{ A} \quad (27)$$

8.2.2.7 C9 - C12 = Output Capacitors

In buck-boost mode, the output capacitors C9 - C12 must supply the entire output current during the switch on-time. For this reason, the output capacitors are chosen for operation in buck-boost mode, the demands being much less in buck operation. Both bulk capacitance and ESR must be considered to ensure a given output ripple voltage. Buck-boost mode capacitance can be estimated from:

$$C_{MIN} = \frac{I_{OUT} \times D_{MAX}}{f \times \Delta V_{OUT}} \text{ with } D_{MAX} = \frac{V_{OUT}}{V_{IN(MIN)} + V_{OUT}} \quad (28)$$

ESR requirements can be estimated from:

$$ESR_{MAX} = \frac{\Delta V_{OUT}}{\frac{V_{OUT} + V_{IN(MIN)}}{V_{IN(MIN)}} \cdot I_{OUT} + \frac{I_{RIPPLE(BUCK\text{-}BOOST)}}{2}} \quad (29)$$

For this example, with a ΔVOUT (output ripple) of 50 mV:

$$C_{MIN} = 141\ \mu F \quad (30)$$

$$ESR_{MAX} = 4.6\ m\Omega \quad (31)$$

If hold-up times are a consideration, the values of the input and output capacitors must be increased appropriately. Note that it is usually advantageous to use multiple capacitors in parallel to achieve the ESR value required. Also, it is good practice to put a .1-µF to .47-µF ceramic capacitor directly on the output pins of the supply to reduce high-frequency noise. Ceramic capacitors have good ESR characteristics, and are a good choice for input and output capacitors. It should be noted that the effective capacitance of ceramic capacitors decreases with dc bias. For larger bulk values of capacitance, a low ESR electrolytic is usually used. However, electrolytic capacitors have poor tolerance, especially over temperature, and the selected value should be selected larger than the calculated value to allow for temperature variation. Allowing for component tolerances, the following values of COUT were chosen for this design example:

Two 180-µF Oscon electrolytic capacitors for bulk capacitance

Two 47-µF ceramic capacitors to reduce ESR

Two 0.47-µF ceramic capacitors to reduce spikes at the output.

Typical Application (continued)

8.2.2.8 D1

Reverse recovery currents degrade performance and decrease efficiency. For these reasons, a Schottky diode of appropriate ratings should be used for D1. The voltage rating of the boost diode should be equal to V_{OUT} plus some margin. D1 conducts continually in buck mode and only when the buck switch is off in Buck-Boost mode.

8.2.2.9 D4

A Schottky type recirculating diode is required for all LM5118-Q1 applications. The near ideal reverse recovery characteristics and low forward voltage drop are particularly important diode characteristics for high input voltage and low output voltage applications. The reverse recovery characteristic determines how long the current surge lasts each cycle when the buck switch is turned on. The reverse recovery characteristics of Schottky diodes minimize the peak instantaneous power in the buck switch during the turnon transition. The reverse breakdown rating of the diode should be selected for the maximum VIN plus some safety margin.

The forward voltage drop has a significant impact on the conversion efficiency, especially for applications with a low output voltage. *Rated* current for diodes vary widely from various manufacturers. For the LM5118-Q1 this current is user selectable through the current sense resistor value. Assuming a worst case 0.6-V drop across the diode, the maximum diode power dissipation can be high. The diode should have a voltage rating of VIN and a current rating of IOUT. A conservative design would at least double the advertised diode rating since specifications between manufacturers vary. For the reference design a 100-V, 10-A Schottky in a D2PAK package was selected.

8.2.2.10 C1 - C5 = Input Capacitor

A typical regulator supply voltage has a large source impedance at the switching frequency. Good-quality input capacitors are necessary to limit the ripple voltage at the VIN pin while supplying most of the switch current during the buck switch on-time. When the buck switch turns on, the current into the buck switch steps from zero to the lower peak of the inductor current waveform, then ramps up to the peak value, and then drops to the zero at turnoff. The RMS current rating of the input capacitors depends on which mode of operation is most critical.

$$I_{RMS(BUCK)} = I_{OUT}\sqrt{D(1 - D)} \tag{32}$$

This value is a maximum at 50% duty cycle which corresponds to VIN = 24 V.

$$I_{RMS(BUCK\text{-}BOOST)} = \frac{I_{OUT}}{1 - D}\sqrt{D(1 - D)} \tag{33}$$

Checking both modes of operation we find:

- $I_{RMS(BUCK)} = 1.5$ A
- $I_{RMS(BUCK\text{-}BOOST)} = 4.7$ A

Therefore C1-C5 should be sized to handle 4.7 A of ripple current. Quality ceramic capacitors with a low ESR should be selected. To allow for capacitor tolerances, five 2.2-µF, 100-V ceramic capacitors will be used. If step input voltage transients are expected near the maximum rating of the LM5118-Q1, a careful evaluation of the ringing and possible spikes at the device VIN pin should be completed. An additional damping network or input voltage clamp may be required in these cases.

8.2.2.11 C20

The capacitor at the VCC pin provides noise filtering and stability for the VCC regulator. The recommended value of C20 should be no smaller than 0.1 µF, and should be a good-quality, low-ESR, ceramic capacitor. A value of 1 µF was selected for this design. C20 should be 10 x C8.

If operating without VCCX, then

$$f_{OSC} \times (Q_C\text{Buck} + \text{Boost}) + I_{LOAD(INTERNAL)} \tag{34}$$

must be less than the VCC current limit.

Typical Application (continued)

8.2.2.12 C8

The bootstrap capacitor between the HB and HS pins supplies the gate current to charge the buck switch gate at turnon. The recommended value of C8 is 0.1 µF to 0.47 µF, and should be a good-quality, low-ESR, ceramic capacitor. A value of 0.1 µF was chosen for this design.

8.2.2.13 C16 = C_{SS}

The capacitor at the SS pin determines the soft-start time, that is, the time for the reference voltage and the output voltage, to reach the final regulated value. The time is determined from:

$$t_{SS} = \frac{\text{C16 x 1.23V}}{10\ \mu\text{A}} \tag{35}$$

and assumes a current limit > Iload + ICout

For this application, a C16 value of 0.1 µF was chosen which corresponds to a soft-start time of about 12 ms.

8.2.2.14 R8, R9

R8 and R9 set the output voltage level, the ratio of these resistors is calculated from:

$$\frac{R8}{R9} = \frac{V_{OUT}}{1.23V} - 1 \tag{36}$$

For a 12-V output, the R8/R9 ratio calculates to 8.76. The resistors should be chosen from standard value resistors and a good starting point is to select resistors within power ratings appropriate for the output voltage. Values of 309 Ω for R9 and 2.67 kΩ for R8 were selected.

8.2.2.15 R1, R3, C21

A voltage divider can be connected to the UVLO pin to set a minimum operating voltage $VIN_{(UVLO)}$ for the regulator. If this feature is required, the easiest approach to select the divider resistor values is to choose a value for R1 between 10 kΩ and 100 kΩ, while observing the minimum value of R1 necessary to allow the UVLO switch to pull the UVLO pin low. This value is:

$R1 \geq 1000 \times V_{IN(MAX)}$

R1 ≥ 75 k in our example

R3 is then calculated from:

$$R3 = 1.23 \text{ x} \left[\frac{R1}{V_{IN(MIN)} + 5\ \mu\text{A x R1} - 1.23}\right] \tag{37}$$

Because $VIN_{(MIN)}$ for our example is 5 V, set $VIN_{(UVLO)}$ to 4.0 V for some margin in component tolerances and input ripple.

R1 = 75 k is chosen since it is a standard value.

R3 = 29.332 k is calculated from Equation 37. The 29.4 k value was used since it is a standard value.

Capacitor C21 provides filtering for the divider and the off-time of the *hiccup* duty cycle during current limit. The voltage at the UVLO pin should never exceed 15 V when using an external set-point divider. It may be necessary to clamp the UVLO pin at high input voltages.

Knowing the desired off time during *hiccup* current limit, the value of C21 is given by:

$$t_{OFF} = \frac{-C21 \cdot R1 \cdot R3}{R1 + R3} \cdot Ln\left[1 - .98 \cdot \frac{R1 + R3}{V_{IN} \cdot R3}\right] \tag{38}$$

Notice that t_{OFF} varies with V_{IN}

In this example, C21 was chosen to be 0.1 µF. This will set the t_{OFF} time to 723 µs with VIN = 12 V.

Typical Application (continued)

8.2.2.16 R2

A 1-M pullup resistor connected from the EN pin to the VIN pin is sufficient to keep enable in a high state if on-off control is not used.

8.2.2.17 Snubber

A snubber network across the buck recirculating diode reduces ringing and spikes at the switching node. Excessive ringing and spikes can cause erratic operation and increase noise at the regulator output. In the limit, spikes beyond the maximum voltage rating of the LM5118-Q1 or the recirculating diode can damage these devices. Selecting the values for the snubber is best accomplished through empirical methods. First, make sure the lead lengths for the snubber connections are very short. Start with a resistor value between 5 and 20 Ω. Increasing the value of the snubber capacitor results in more damping, however the snubber losses increase. Select a minimum value of the capacitor that provides adequate clamping of the diode waveform at maximum load. A snubber may be required for the boost diode as well. The same empirical procedure applies. Snubbers were not necessary in this example.

8.2.2.18 Error Amplifier Configuration

8.2.2.18.1 R4, C18, C17

These components configure the error amplifier gain characteristics to accomplish a stable overall loop gain. One advantage of current mode control is the ability to close the loop with only three feedback components, R4, C18 and C17. The overall loop gain is the product of the modulator gain and the error amplifier gain. The DC modulator gain of the LM5118-Q1 is as follows:

$$\mathrm{DCGain}_{(MOD)} = \frac{R_{LOAD} \times V_{IN}}{10R_S(V_{IN} + 2V_{OUT})} \tag{39}$$

The dominant, low frequency pole of the modulator is determined by the load resistance (R_{LOAD}) and output capacitance (C_{OUT}). The corner frequency of this pole is:

$$f_{P(MOD)} = \frac{1 + D_{MAX}}{2\pi \times R_{LOAD} \times C_{OUT}} \tag{40}$$

For this example, R_{LOAD} = 4 Ω, D_{MAX} = 0.705, and C_{OUT} = 454 µF, therefore:

$$f_{P(MOD)} = 149\ \mathrm{Hz} \tag{41}$$

$$\mathrm{DC\ Gain}_{(MOD)} = 4.598 = 13.25\ \mathrm{dB} \tag{42}$$

Additionally, there is a right-half plane (RHP) zero associated with the modulator. The frequency of the RHP zero is:

$$f_{RHPzero} = \frac{R_{LOAD}\,(1 - D)^2}{2\pi \times L \times D} \tag{43}$$

$$f_{RHPzero} = 7.8\ \mathrm{kHz} \tag{44}$$

The output capacitor ESR produces a zero given by:

$$\mathrm{ESR}_{zero} = \frac{1}{2\pi \times \mathrm{ESR} \times C_{OUT}} \tag{45}$$

$$\mathrm{ESR}_{ZERO} = 76\ \mathrm{kHz} \tag{46}$$

The RHP zero complicates compensation. The best design approach is to reduce the loop gain to cross zero at about 25% of the calculated RHP zero frequency. The Type II error amplifier compensation provided by R4, C18, and C17 places one pole at the origin for high DC gain. The 2nd pole should be located close to the RHP zero. The error amplifier zero (Equation 47) should be placed near the dominate modulator pole. This is a good starting point for compensation. Refer to the on-line LM5118-Q1 Quick-Start calculator for ready to use equations and more details.

Typical Application (continued)

Components R4 and C18 configure the error amplifier as a type II configuration which has a DC pole and a zero at:

$$f_z = \frac{1}{2 \times \pi \times R4 \times C18} \tag{47}$$

C17 introduces an additional pole used to cancel high-frequency switching noise. The error amplifier zero cancels the modulator pole leaving a single pose response at the crossover frequency of the loop gain if the crossover frequency is much lower than the right half plane zero frequency. A single pole response at the crossover frequency yields a very stable loop with 90 degrees of phase margin.

For the design example, a target loop bandwidth (crossover frequency) of 2.0 kHz was selected (about 25% of the right-half-plane zero frequency). The error amplifier zero (fz) should be selected at a frequency near that of the modulator pole and much less than the target crossover frequency. This constrains the product of R4 and C18 for a desired compensation network zero to be less than 2 kHz. Increasing R4, while proportionally decreasing C18 increases the error amp gain. Conversely, decreasing R4 while proportionally increasing C18 decreases the error amp gain. For the design example C18 was selected for 100 nF and R4 was selected to be 10 kΩ. These values set the compensation network zero at 159 Hz. The overall loop gain can be predicted as the sum (in dB) of the modulator gain and the error amp gain.

If a network analyzer is available, the modulator gain can be measured and the error amplifier gain can be configured for the desired loop transfer function. If a network analyzer is not available, the error amplifier compensation components can be designed with the guidelines given. Step load transient tests can be performed to verify acceptable performance. The step load goal is minimal overshoot with a damped response.

Typical Application (continued)

8.2.3 Application Curves

The plots in Figure 21 through Figure 26 show the gain and phase diagrams of the design example. The overall bandwidth is lower in a buck-boost application due the compensation challenges associated with the right-half-plane zero. For a pure buck application, the bandwidth could be much higher. The LM5116 data sheet is a good reference for compensation design of a pure buck mode regulator.

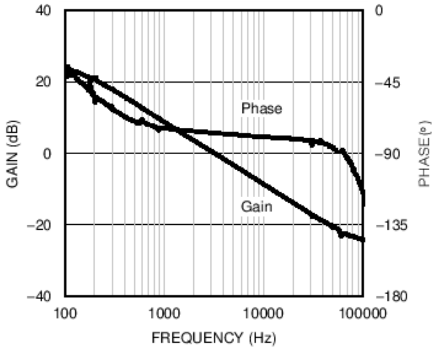


Figure 21. Modulator Gain and Phase - Buck Mode

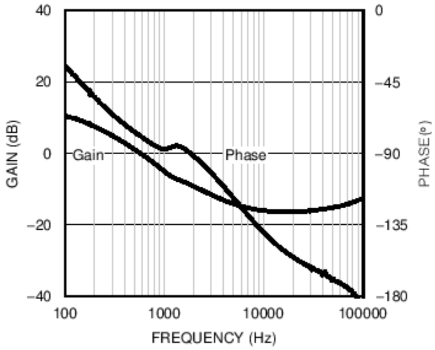


Figure 22. Modulator Gain and Phase - Buck-Boost Mode

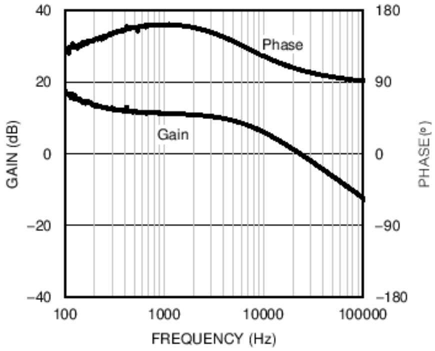


Figure 23. Error Amplifier Gain and Phase - Buck Mode

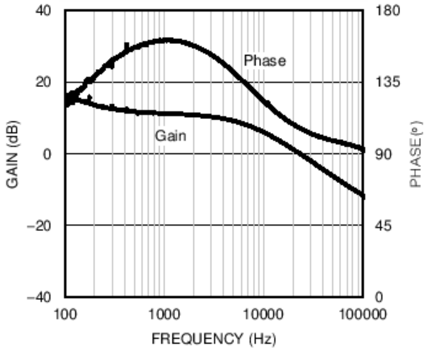


Figure 24. Error Amplifier Gain and Phase - Buck-Boost Mode

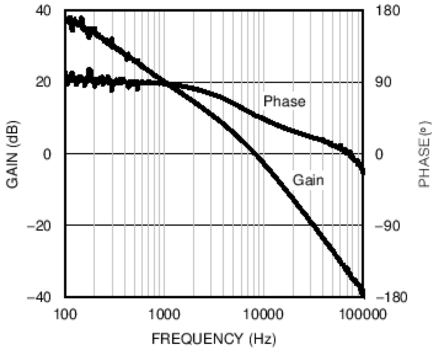


Figure 25. Overall Loop Gain and Phase - Buck Mode

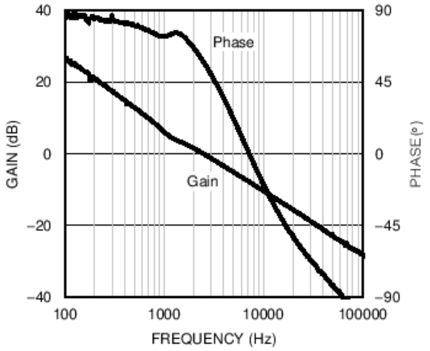


Figure 26. Overall Loop Gain and Phase - Buck Boost Mode

9 Power Supply Recommendations

9.1 Thermal Considerations

The highest power dissipating components are the two power MOSFETs, the recirculating diode, and the output diode. The easiest way to determine the power dissipated in the MOSFETs is to measure the total conversion losses (P_{IN} - P_{OUT}), then subtract the power losses in the Schottky diodes, output inductor and any snubber resistors. An approximation for the recirculating Schottky diode loss is:

$$P = (1 - D) \times I_{OUT} \times V_{FWD}. \tag{48}$$

The boost diode loss is

$$P = I_{OUT} \times V_{FWD}. \tag{49}$$

If a snubber is used, the power loss can be estimated with an oscilloscope by observation of the resistor voltage drop at both turnon and turnoff transitions. The LM5118-Q1 package has an exposed thermal pad to aid power dissipation. Selecting diodes with exposed pads will aid the power dissipation of the diodes as well. When selecting the MOSFETs, pay careful attention to $R_{DS(ON)}$ at high temperature. Also, selecting MOSFETs with low gate charge will result in lower switching losses.

9.2 Bias Power Dissipation Reduction

Buck or Buck-boost regulators operating with high input voltage can dissipate an appreciable amount of power while supplying the required bias current of the IC. The VCC regulator must step-down the input voltage VIN to a nominal VCC level of 7 V. The large voltage drop across the VCC regulator translates into high power dissipation in the VCC regulator. There are several techniques that can significantly reduce this bias regulator power dissipation. Figure 27 and Figure 28 depict two methods to bias the IC, one from the output voltage and one from a separate bias supply. In the first case, the internal VCC regulator is used to initially bias the VCC pin. After the output voltage is established, the VCC pin bias current is supplied through the VCCX pin, which effectively disables the internal VCC regulator. Any voltage greater than 4.0 V can supply VCC bias through the VCCX pin. However, the voltage applied to the VCCX pin should never exceed 15 V. The voltage supplied through VCCX must be large enough to drive the switching MOSFETs into full saturation.

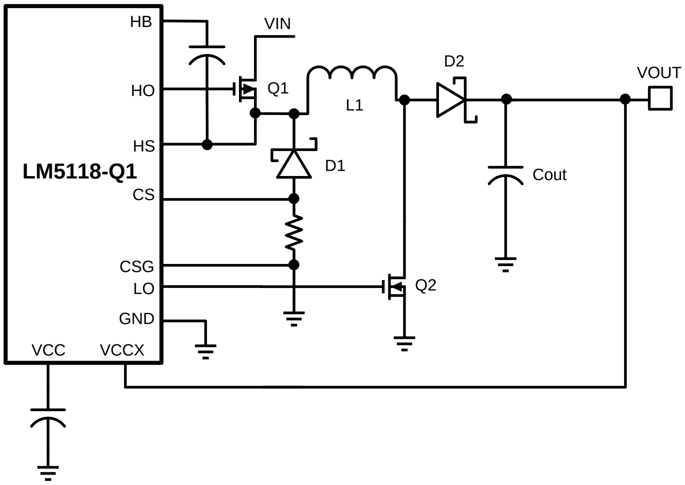


Figure 27. VCC Bias From VOUT 4 V < VOUT < 15 V

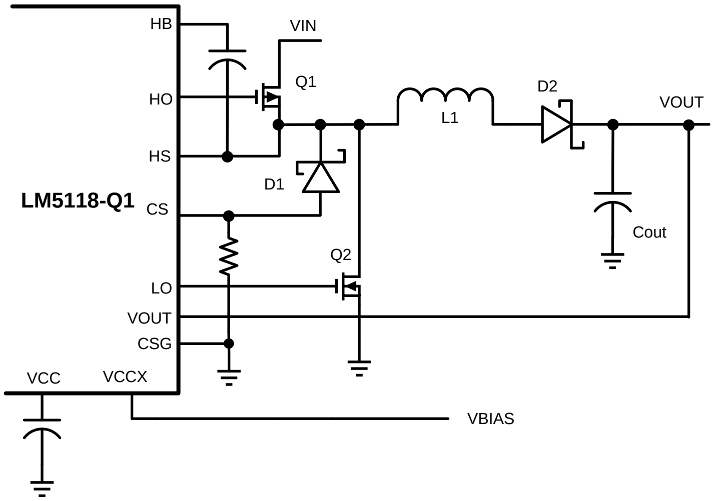


Figure 28. VCC Bias With Additional Bias Supply

Bias Power Dissipation Reduction (continued)

In a buck-boost regulator, there are two loops where currents are switched very fast. The first loop starts from the input capacitors, and then to the buck switch, the inductor, the boost switch then back to the input capacitor. The second loop starts from the inductor, and then to the output diode, the output capacitor, the recirculating diode, and back to the inductor. Minimizing the PCB area of these two loops reduces the stray inductance and minimizes noise and the possibility of erratic operation. A ground plane in the PCB is recommended as a means to connect the input filter capacitors to the output filter capacitors and the PGND pins of the LM5118-Q1. Connect all of the low current ground connections (C_{SS}, R_T, C_{RAMP}) directly to the regulator AGND pin. Connect the AGND and PGND pins together through topside copper area covering the entire underside of the device. Place several vias in this underside copper area to the ground plane of the input capacitors.

10 Layout

10.1 Layout Guidelines

In a buck-boost regulator, there are two loops where currents are switched very fast. The first loop starts from the input capacitors, and then to the buck switch, the inductor, the boost switch then back to the input capacitor. The second loop starts from the inductor, and then to the output diode, the output capacitor, the re-circulating diode, and back to the inductor. Minimizing the PCB area of these two loops reduces the stray inductance and minimizes noise and the possibility of erratic operation. A ground plane in the PCB is recommended as a means to connect the input filter capacitors to the output filter capacitors and the PGND pins of the LM5118-Q1. Connect all of the low current ground connections (C_{SS}, R_T, C_{RAMP}) directly to the regulator AGND pin. Connect the AGND and PGND pins together through topside copper area covering the entire underside of the device. Place several vias in this underside copper area to the ground plane of the input capacitors.

10.2 Layout Example

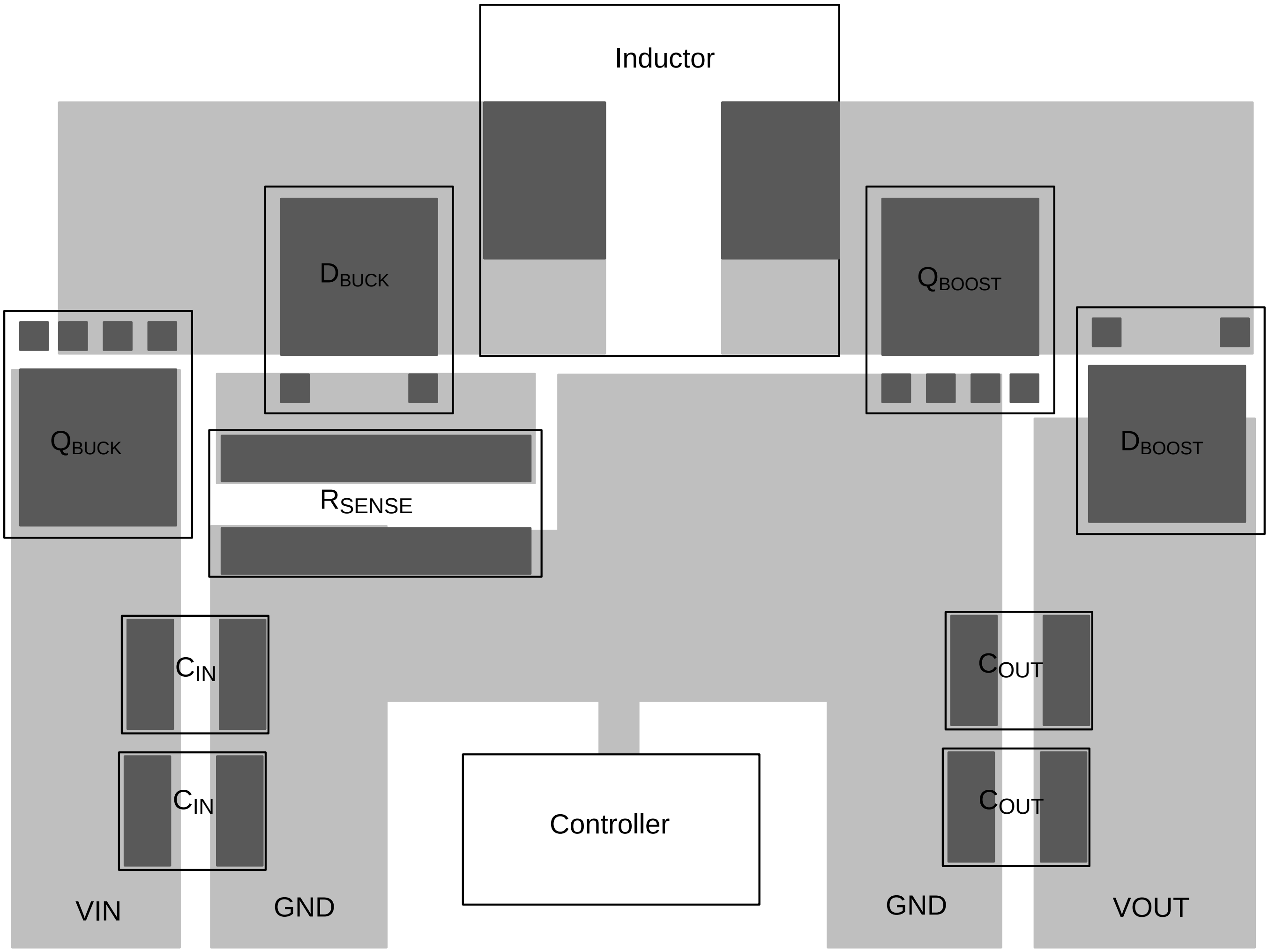


Figure 29. LM5118-Q1 Layout Example

11 器件和文档支持

11.1 器件支持

11.1.1 开发支持

*11.1.1.1 使用 **WEBENCH®** 工具创建定制设计*

请单击此处，结合使用 LM5118-Q1 器件和 WEBENCH® 电源设计器创建定制设计。

1. 在开始阶段键入输出电压 (V_{IN})、输出电压 (V_{OUT}) 和输出电流 (I_{OUT}) 要求。
2. 使用优化器拨盘优化关键设计参数，如效率、封装和成本。
3. 将生成的设计与德州仪器 (TI) 的其他解决方案进行比较。

WEBENCH Power Designer 提供一份定制原理图以及罗列实时价格和组件可用性的物料清单。

在多数情况下，可执行以下操作：

- 运行电气仿真，观察重要波形以及电路性能
- 运行热性能仿真，了解电路板热性能
- 将定制原理图和布局方案导出至常用 CAD 格式
- 打印设计方案的 PDF 报告并与同事共享

有关 WEBENCH 工具的详细信息，请访问 www.ti.com/WEBENCH。

11.2 商标

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All other trademarks are the property of their respective owners.

11.3 静电放电警告

这些装置包含有限的内置 ESD 保护。 存储或装卸时，应将导线一起截短或将装置放置于导电泡棉中，以防止 MOS 门极遭受静电损伤。

11.4 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 机械、封装和可订购信息

以下页面包含机械、封装和可订购信息。这些信息是指定器件的最新可用数据。这些数据如有变更，恕不另行通知和修订此文档。如欲获取此数据表的浏览器版本，请参阅左侧的导航。

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LM5118Q1MH/NOPB	ACTIVE	HTSSOP	PWP	20	73	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	LM5118 Q1MH	Samples
LM5118Q1MHX/NOPB	ACTIVE	HTSSOP	PWP	20	2500	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	LM5118 Q1MH	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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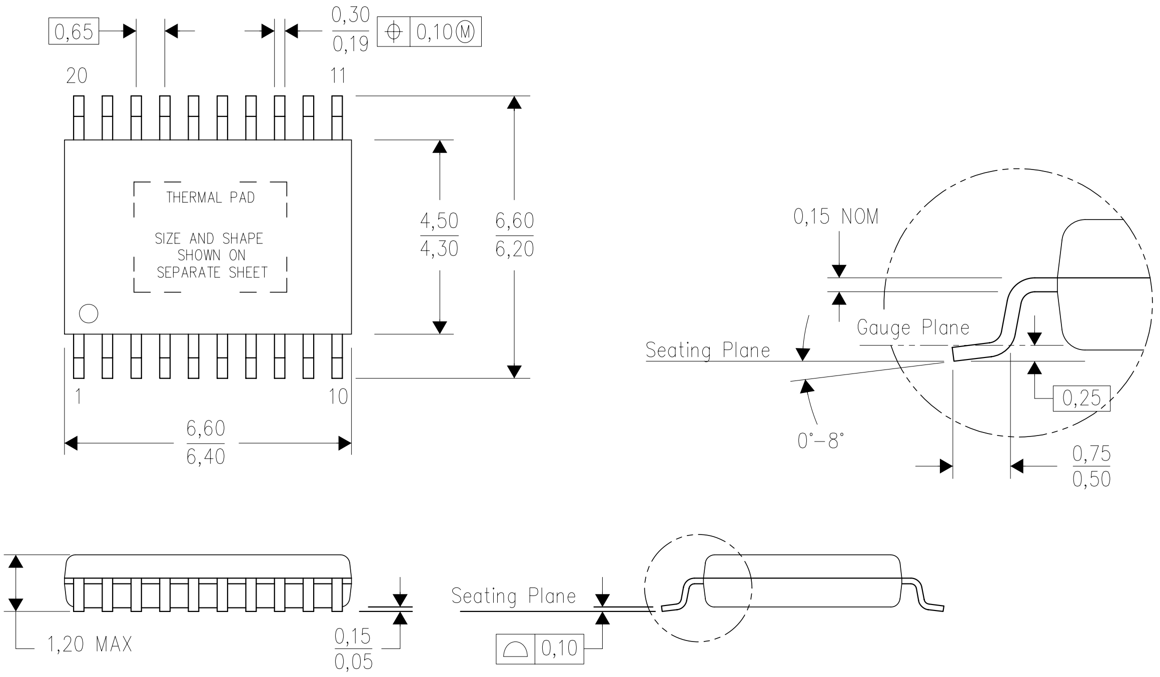
PWP (R–PDSO–G20) PowerPAD™ PLASTIC SMALL OUTLINE



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NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusions. Mold flash and protrusion shall not exceed 0.15 per side.
- D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http://www.ti.com>.
- E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
- E. Falls within JEDEC MO–153

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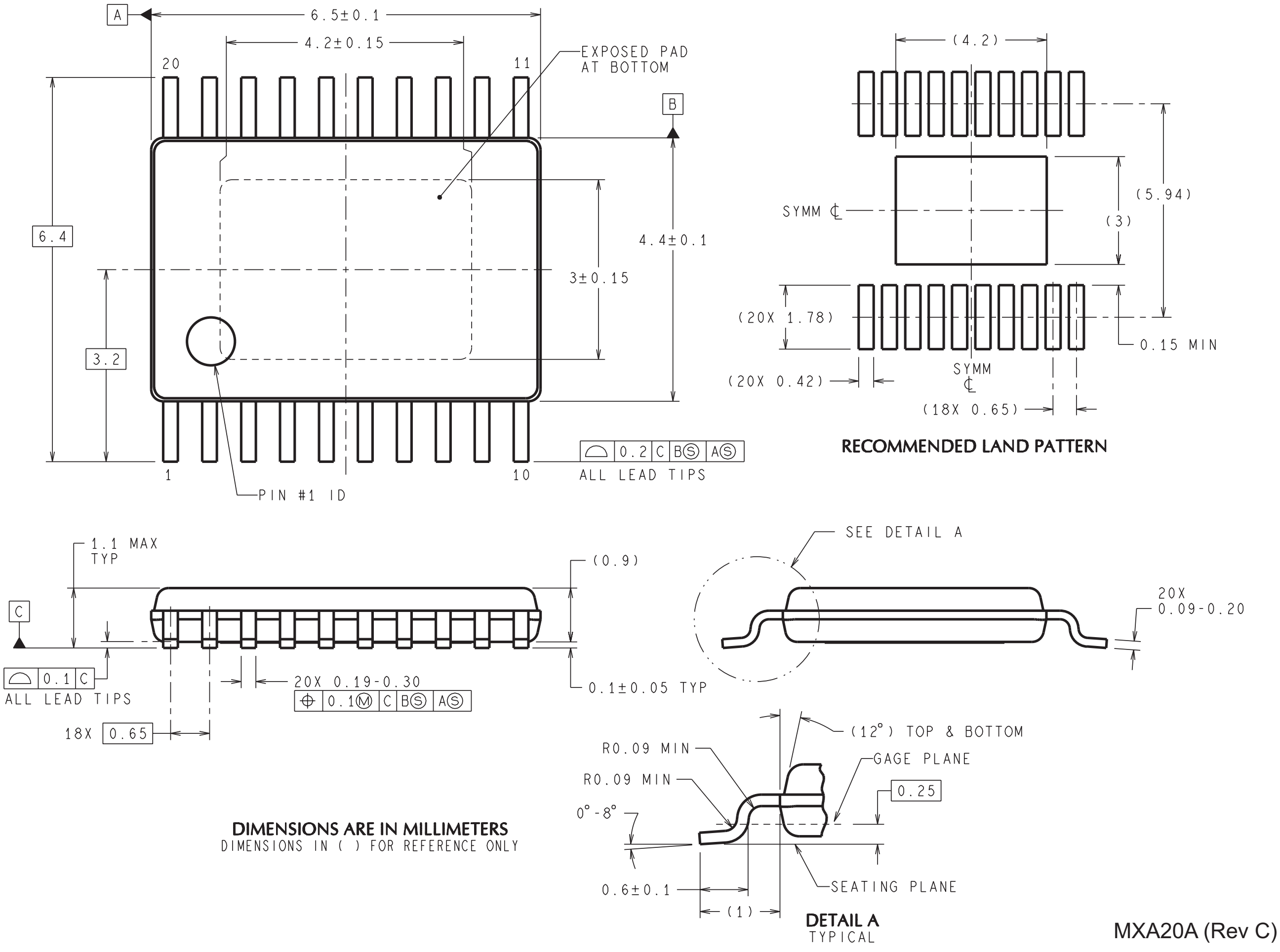
A
6.5±0.1
4.2±0.15
20
11
EXPOSED PAD
AT BOTTOM
B
6.4
4.4±0.1
3±0.15
3.2
1
10
0.2 C B(S) A(S)
ALL LEAD TIPS
PIN #1 ID
(4.2)
SYMM ℄
(5.94)
(3)
(20X 1.78)
0.15 MIN
(20X 0.42)
SYMM
℄
(18X 0.65)
RECOMMENDED LAND PATTERN
1.1 MAX
TYP
(0.9)
C
0.1 C
ALL LEAD TIPS
20X 0.19-0.30
0.1(M) C B(S) A(S)
0.1±0.05 TYP
18X 0.65
SEE DETAIL A
20X
0.09-0.20
(12°) TOP & BOTTOM
R0.09 MIN
GAGE PLANE
R0.09 MIN
0.25
0°-8°
DIMENSIONS ARE IN MILLIMETERS
DIMENSIONS IN ( ) FOR REFERENCE ONLY
SEATING PLANE
0.6±0.1
(1)
DETAIL A
TYPICAL

MXA20A (Rev C)

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