# 具有超低 $I_Q$ 的 LM5166 3V 至 65V 输入、500mA 同步降压转换器

## 1 特性

- 3V 至 65V 宽输入电压范围
- 9.7µA 无负载静态电流
- –40°C 至 150°C 结温范围
- 固定（3.3V、5V）或可调节输出电压选项
- 符合 EN55022/CISPR 22 EMI 标准
- 集成 1Ω P 沟道场效应晶体管 (PFET) 降压开关
  - 支持 100% 占空比，可实现低压降
- 集成 0.5Ω N 沟道场效应晶体管 (NFET) 同步整流器
  - 无需使用外部肖特基二极管
- 可编程峰值电流限制支持：
  - 500mA、300mA 或 200mA 负载
- 可选 PFM 或 COT 模式工作
- 1.223V ±1.2% 内部电压基准
- 开关频率高达 600kHz
- 900µs 内部或外部可调节软启动
- 二极管仿真以及用于在轻负载时确保超高效率的脉冲跳跃模式
- 无环路补偿或自举升压组件
- 具有迟滞功能的精密使能和输入 UVLO
- 开漏电源正常指示器
- 具有迟滞功能的热关断保护
- 与 LM5165 引脚对引脚兼容
- 10 引脚 3mm × 3mm VSON 封装
- 使用 WEBENCH® 电源设计器创建定制稳压器设计

## 2 应用

- 工厂和楼宇自动化
- 汽车和电池供电 应用
- 高电压 LDO 替代产品
- 低功耗偏置电源

## 3 说明

LM5166 是一款易于使用的紧凑型 3V 至 65V、超低 $I_Q$ 同步降压转换器，可在宽输入电压和负载电流范围内提供高效率。该器件集成有高侧和低侧功率金属氧化物半导体场效应晶体管 (MOSFET)，可提供高达 500mA 的输出电流，输出电压有固定式（3.3V 或 5V）和可调节式两种可供选择。该转换器设计旨在简化实现方案，同时优化目标应用的性能。脉频调制 (PFM) 模式可确保在轻负载条件下获得最优效率，恒定导通时间 (COT) 控制可实现近似恒定的工作频率。这两种控制方案都不需要环路补偿，同时还能够针对较高的降压转换比实现出色的线路和负载瞬态响应以及短暂的脉宽调制 (PWM) 导通时间。

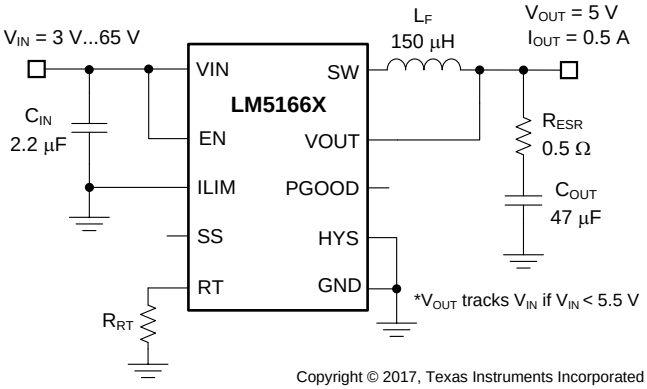
高侧 P 沟道 MOSFET 能够以 100% 占空比工作以确保最低压差电压，而且不需要使用自举电容器进行栅极驱动。另外，还可以调节电流限制设定值来优化电感器选择，从而满足特定的负载电流要求。可选和可调节启动时序选项包括最短延迟（无软启动）、内部固定值 (900µs) 以及可使用电容器进行外部编程的软启动。可以使用开漏 PGOOD 指示器进行定序、故障报告和输出电压监视。LM5166 采用引脚间距为 0.5mm 的 10 引脚 VSON 封装。

**器件信息(1)**

| 器件型号 | 输出 | 封装 |
|---|---|---|
| LM5166 | 可调节 | VSON (10) |
| LM5166X | 5V 固定 | |
| LM5166Y | 3.3V 固定 | |

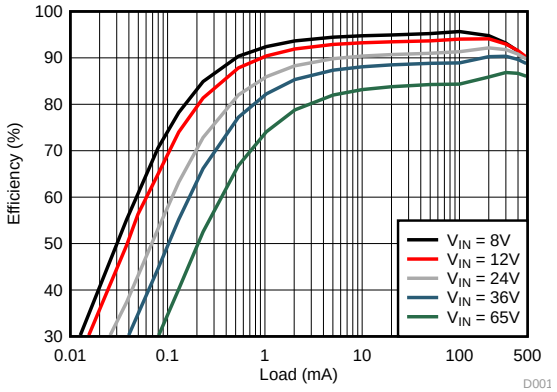
(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。

**典型 COT 模式应用**






**典型 COT 模式应用效率**



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## 4 修订历史记录

**Changes from Revision A (December 2016) to Revision B** **Page**

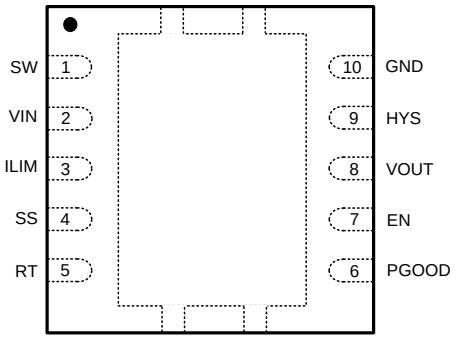
- 根据最新 TI 文档和翻译标准更新了数据表文本 ..... 1
- 更改了 WEBENCH 列表项的语言；在数据表中添加了有关 WEBENCH 的其他内容和链接 ..... 1
- 在数据表中添加了 LM5166X 和 LM5166Y 输出版本 ..... 1
- 将*器件信息* 表中的“封装尺寸（标称值）”列替换成了“输出版本” ..... 1
- 将*典型 COT 模式应用* 电路更改成了固定 5V 输出 ..... 1
- Changed the EN absolute maximum voltage from ($V_{VIN}$ + 0.3 V) to 68 V ..... 4
- Deleted note 5 under the *Absolute Maximum Ratings* table ..... 4
- Changed the EN max operating voltage from $V_{VIN}$ to 65 V ..... 4
- Removed note 2 under the *Recommended Operating Conditions* ..... 4
- Changed the $I_{FB}$ maximum from: 100 nA to: 25 nA ..... 5
- Added 图 13 and 图 14 ..... 8
- Modified the *Functional Block Diagram* graphic ..... 14
- Changed $R_{DSON1}$ to $R_{DSON2}$ in 公式 3 ..... 17
- Updated 公式 12 ..... 19
- Added a link to TI Design TIDA-01395 to the *Typical Applications* section ..... 26
- Changed Design 3 to a 3.3-V fixed output, LM5166Y ..... 35
- Added a new part number to $C_{IN}$ ref description ..... 35
- Added a new part number to $L_F$ ref description ..... 38
- Added the *Design 5: 12-V, 300-mA COT Converter Operating from 24-V or 48-V Input* section to *Typical Applications* ..... 41
- Changed the *PCB Layout* and *PCB Layout Guidelines* section names to *Layout* and *Layout Guidelines* ..... 44
- 向*文档支持* 部分添加了内容 ..... 47

**Changes from Original (December 2016) to Revision A** **Page**

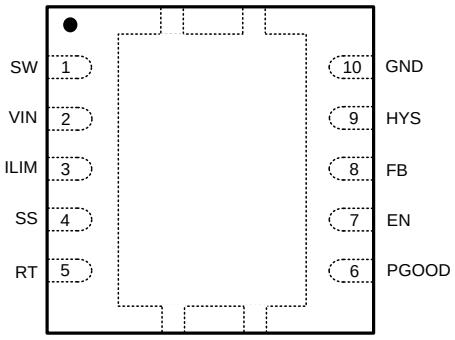
- 将数据表状态从“产品预览”更改成了“生产数据” ..... 1

# 5 Pin Configuration and Functions

**LM5166X and LM5166Y Fixed Output DRC Package**
**10-Pin VSON**
**Top View**




**LM5166 Adjustable Output DRC Package**
**10-Pin VSON**
**Top View**




**Pin Functions**

| PIN | | I/O(1) | DESCRIPTION |
|---|---|---|---|
| NO. | NAME | | |
| 1 | SW | P | Switching node that is internally connected to the drain of the PFET buck switch (high side) and the drain of the NFET synchronous rectifier (low side). Connect to the buck inductor. |
| 2 | VIN | P | Regulator supply input pin to high-side power MOSFET and internal bias rail LDO. Connect to input supply and input filter capacitor $C_{IN}$. The path from the VIN pin to the input capacitor must be as short as possible. |
| 3 | ILIM | I | Programming pin for current limit. Connecting the appropriate resistance from the ILIM pin to GND selects one of the three current limit options. The available current limit options are detailed in 表 3. |
| 4 | SS | I | Programming pin for the soft-start delay. If a 100-kΩ resistor is connected from the SS pin to GND, the internal soft-start circuit is disabled and the FB comparator reference steps immediately from zero to full value when the regulator is enabled by the EN input. If the SS pin is left open, the internal soft-start circuit ramps the FB reference from zero to full value in 900 µs. If a capacitor is connected from the SS pin to GND, the soft-start time can be set longer than 900 µs. |
| 5 | RT | I | Mode select and on-time programming pin for Constant On-Time control. Connect a resistor from the RT pin to GND to program the on-time and hence switching frequency. Short RT to GND to select PFM (pulse frequency modulation) operation. |
| 6 | PGOOD | O | Power Good output flag pin. PGOOD is connected to the drain of an NFET that holds the pin low when either FB or VOUT is not in regulation. Use a 10-kΩ to 100-kΩ pullup resistor to system voltage rail or VOUT (no higher than 12 V). |
| 7 | EN | I | Input pin of the precision enable / UVLO comparator. The regulator is enabled when the EN pin voltage is greater than 1.22 V. |
| 8 | VOUT or FB | I | Feedback input to the voltage regulation loop for the LM5166 Adjustable Output version, or a VOUT pin connects the internal feedback resistor divider to the regulator output voltage for the fixed 3.3-V or 5-V options. The FB pin connects the internal feedback comparator to an external resistor divider for the adjustable voltage option, and the reference for the FB pin comparator is 1.223 V. |
| 9 | HYS | O | Drain of internal NFET that is turned off when the EN input is greater than the EN pin threshold. External resistors from HYS to EN and GND program the input UVLO threshold and hysteresis. |
| 10 | GND | G | Regulator ground return. |
| — | PAD | P | Connect to GND pin and system ground on PCB. Path to $C_{IN}$ must be as short as possible. |

(1) P = Power, G = Ground, I = Input, O = Output.

# 6 Specifications

## 6.1 Absolute Maximum Ratings

Over the recommended operating junction temperature range of –40°C to 150°C (unless otherwise noted).[1][2]

| | | MIN | MAX | UNIT |
|---|---|---|---|---|
| VIN, EN to GND | | –0.3 | 68 | V |
| SW to GND | | –0.7 | $V_{VIN}$ + 0.3 | V |
| | 20-ns transient | –3 | | |
| PGOOD, VOUT[3] to GND | | –0.3 | 16 | V |
| HYS to GND | | –0.3 | 7 | V |
| ILIM, SS, RT, FB[4] to GND | | –0.3 | 3.6 | V |
| Maximum junction temperature, $T_J$ | | –40 | 150 | °C |
| Storage temperature, $T_{stg}$ | | –55 | 150 | °C |

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/Distributors for availability and specifications.
(3) Fixed output setting.
(4) Adjustable output setting.

## 6.2 ESD Ratings

| | | | VALUE | UNIT |
|---|---|---|---|---|
| $V_{(ESD)}$ | Electrostatic discharge | Human body model (HBM), per ANSI/ESDA/JEDEC JS-001[1] | ±2000 | V |
| | | Charged device model (CDM), per JEDEC specification JESD22-C101[2] | ±1000 | |

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

## 6.3 Recommended Operating Conditions

Over the recommended operating junction temperature range of –40°C to 150°C (unless otherwise noted).[1]

| | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|
| Input voltages | VIN | 3 | | 65 | V |
| | EN | –0.3 | | 65 | |
| | PGOOD | –0.3 | | 12 | |
| | HYS | –0.3 | | 5.5 | |
| Output current | $I_{OUT}$ | 0 | | 500 | mA |
| Temperature | Operating junction temperature | –40 | | 150 | °C |

(1) Operating Ratings are conditions under which the device is intended to be functional. For specifications and test conditions, see *Electrical Characteristics*.

## 6.4 Thermal Information

| THERMAL METRIC[1] | | LM5166 DRC (VSON) 10 PINS | UNIT |
|---|---|---|---|
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance | 49.1 | °C/W |
| $R_{\theta JC(top)}$ | Junction-to-case (top) thermal resistance | 57.2 | °C/W |
| $R_{\theta JB}$ | Junction-to-board thermal resistance | 26.6 | °C/W |
| $\psi_{JT}$ | Junction-to-top characterization parameter | 0.8 | °C/W |
| $\psi_{JB}$ | Junction-to-board characterization parameter | 23.8 | °C/W |
| $R_{\theta JC(bot)}$ | Junction-to-case (bottom) thermal resistance | 4.8 | °C/W |

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

## 6.5 Electrical Characteristics

Typical values correspond to $T_J$ = 25°C. Minimum and maximum limits are based on $T_J$ = –40°C to +125°C. $V_{IN}$ = 12 V (unless otherwise noted).(1)(2)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $I_{Q-SD}$ | VIN DC supply current, shutdown | $V_{EN}$ = 0 V, $T_J$ = 25°C | | 4 | 6 | µA |
| $I_{Q-SLEEP}$ | VIN DC supply current, no load | $V_{FB}$ = 1.5 V, $T_J$ = 25°C | | 9.7 | 15 | µA |
| $I_{Q-SLEEP-VINMAX}$ | VIN DC supply current, no load | $V_{FB}$ = 1.5 V, $V_{VIN}$ = 65 V, $T_J$ = 25°C | | 10 | 15 | µA |
| $I_{Q-ACTIVE-PFM}$ | VIN DC supply current, active | PFM mode, $R_{RT}$ = 0 Ω, $R_{SS}$ = 100 kΩ | | 205 | | µA |
| $I_{Q-ACTIVE-COT}$ | VIN DC supply current, active | COT mode, $R_{RT}$ = $R_{SS}$ = 100 kΩ | | 320 | | µA |
| **POWER SWITCHES** | | | | | | |
| $R_{DSON1}$ | High-side MOSFET $R_{DS(on)}$ | $I_{SW}$ = –100 mA | | 0.93 | | Ω |
| $R_{DSON2}$ | Low-side MOSFET $R_{DS(on)}$ | $I_{SW}$ = 100 mA | | 0.48 | | Ω |
| **CURRENT LIMITING** | | | | | | |
| $I_{HS\_LIM1}$ | High-side peak current limit threshold | See 表 3 | 1125 | 1250 | 1375 | mA |
| $I_{HS\_LIM2}$ | | | 675 | 750 | 825 | |
| $I_{HS\_LIM3}$ | | | 440 | 500 | 560 | |
| $I_{LS\_LIM1}$ | Low-side valley current limit threshold | See 表 3 | | 415 | | mA |
| $I_{LS\_LIM2}$ | | | | 315 | | |
| **REGULATION COMPARATOR** | | | | | | |
| $V_{VOUT5}$ | VOUT 5-V DC setpoint | LM5166X | 4.9 | 5.0 | 5.1 | V |
| $V_{VOUT3.3}$ | VOUT 3.3-V DC setpoint | LM5166Y | 3.23 | 3.3 | 3.37 | V |
| $I_{VOUT}$ | VOUT pin input current | $V_{VOUT}$ = 5 V, LM5166X | | 7 | | µA |
| | | $V_{VOUT}$ = 3.3 V, LM5166Y | | 3.8 | | |
| $V_{FB1}$ | Lower FB regulation threshold (PFM and COT) | Adjustable VOUT version | 1.208 | 1.223 | 1.238 | V |
| $V_{FB2}$ | Upper FB regulation threshold (PFM) | | 1.218 | 1.233 | 1.248 | V |
| $I_{FB}$ | FB pin input bias current | $V_{FB}$ = 1 V | | | 25 | nA |
| $FB_{HYS-PFM}$ | FB comparator PFM hysteresis | PFM mode | | 10 | | mV |
| $FB_{HYS-COT}$ | FB comparator dropout hysteresis | COT mode | | 4 | | mV |
| $FB_{LINE-REG}$ | FB threshold variation over line | $V_{VIN}$ = 3 V to 65 V | | 0.005 | | %/V |
| $VOUT_{LINE-REG}$ | VOUT threshold variation over line | LM5166X, $V_{VIN}$ = 6 V to 65 V<br>LM5166Y, $V_{VIN}$ = 4.5 V to 65 V | | 0.005 | | %/V |
| **POWER GOOD** | | | | | | |
| $UVT_{RISING}$ | PGOOD comparator | $V_{FB}$ rising relative to $V_{FB1}$ threshold | | 94% | | |
| $UVT_{FALLING}$ | | $V_{FB}$ falling relative to $V_{FB1}$ threshold | | 87% | | |
| $R_{PGOOD}$ | PGOOD on-resistance | $V_{FB}$ = 1 V | | 80 | 200 | Ω |
| $V_{INMIN-PGOOD}$ | Minimum required VIN for valid PGOOD | $V_{VIN}$ falling<br>$I_{PGOOD}$ = 0.1 mA, $V_{PGOOD}$ < 0.5 V | | 1.2 | 1.65 | V |
| $I_{PGOOD}$ | PGOOD off-state leakage | $V_{FB}$ = 1.2 V, $V_{PGOOD}$ = 5.5 V | | 10 | 100 | nA |
| **ENABLE / UVLO** | | | | | | |
| $V_{IN-ON}$ | Turnon threshold | $V_{VIN}$ rising | 2.60 | 2.75 | 2.95 | V |
| $V_{IN-OFF}$ | Turnoff threshold | $V_{VIN}$ falling | 2.35 | 2.45 | 2.60 | V |
| $V_{EN-ON}$ | EN turnon threshold | $V_{EN}$ rising | 1.163 | 1.22 | 1.276 | V |
| $V_{EN-OFF}$ | EN turnoff threshold | $V_{EN}$ falling | 1.109 | 1.144 | 1.178 | V |

(1) All hot and cold limits are specified by correlating the electrical characteristics to process and temperature variations and applying statistical process control.
(2) The junction temperature ($T_J$ in °C) is calculated from the ambient temperature ($T_A$ in °C) and power dissipation ($P_D$ in Watts) as follows: $T_J = T_A + (P_D \bullet \theta_{JA})$ where $\theta_{JA}$ (in °C/W) is the package thermal impedance provided in *Thermal Information*.

## Electrical Characteristics (continued)

Typical values correspond to $T_J$ = 25°C. Minimum and maximum limits are based on $T_J$ = –40°C to +125°C. $V_{IN}$ = 12 V (unless otherwise noted).[1][2]

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $V_{EN-HYS}$ | EN hysteresis | | | 76 | | mV |
| $V_{EN-SD}$ | EN shutdown threshold | $V_{EN}$ falling | 0.3 | 0.6 | | V |
| $R_{HYS}$ | HYS on-resistance | $V_{EN}$ = 1 V | | 80 | 200 | Ω |
| $I_{HYS}$ | HYS off-state leakage | $V_{EN}$ = 1.5 V, $V_{HYS}$ = 5.5 V | | 10 | 100 | nA |
| **SOFT-START** | | | | | | |
| $I_{SS}$ | Soft-start charging current | $V_{SS}$ = 1 V | | 10 | | µA |
| $T_{SS-INT}$ | Soft-start rise time | SS floating | | 900 | | µs |
| **THERMAL SHUTDOWN** | | | | | | |
| $T_{J-SD}$ | Thermal shutdown threshold | | | 170 | | °C |
| $T_{J-SD-HYS}$ | Thermal shutdown hysteresis | | | 10 | | °C |

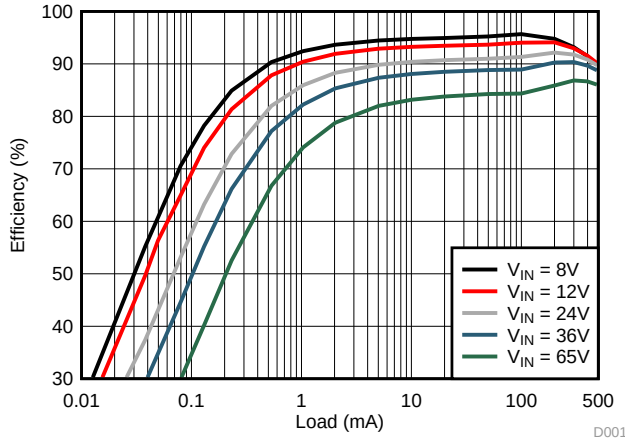
## 6.6 Switching Characteristics

Over operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $T_{ON-MIN}$ | Minimum on-time | | | 180 | | ns |
| $T_{ON1}$ | On-time | 16 kΩ from RT to GND | | 280 | | ns |
| $T_{ON2}$ | On-time | 75 kΩ from RT to GND | | 1150 | | ns |

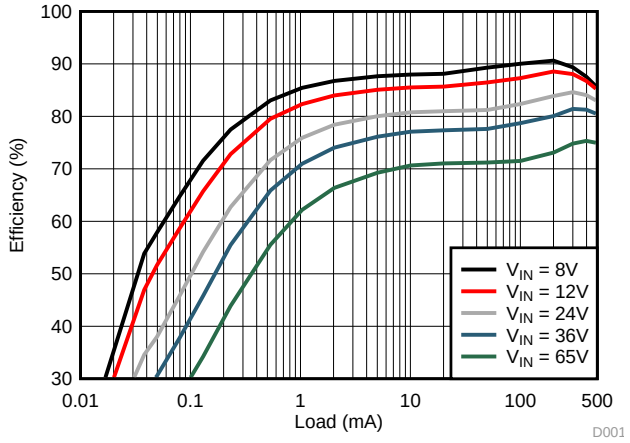
## 6.7 Typical Characteristics

Unless otherwise specified, $V_{IN}$ = 12 V, $V_{OUT}$ = 5 V. Please refer to Typical Applications for circuit designs.



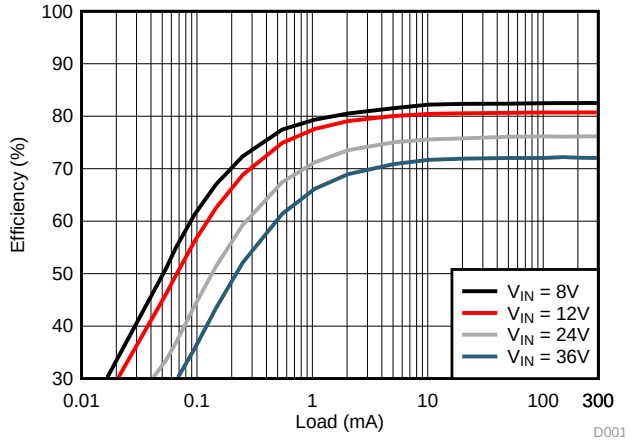

See schematic, 图 52 | $L_F$ = 150 µH | $C_{OUT}$ = 47 µF | $F_{SW(nom)}$ = 100 kHz | $R_{RT}$ = 309 kΩ

**图 1. Converter Efficiency: 5 V, 500 mA, COT**



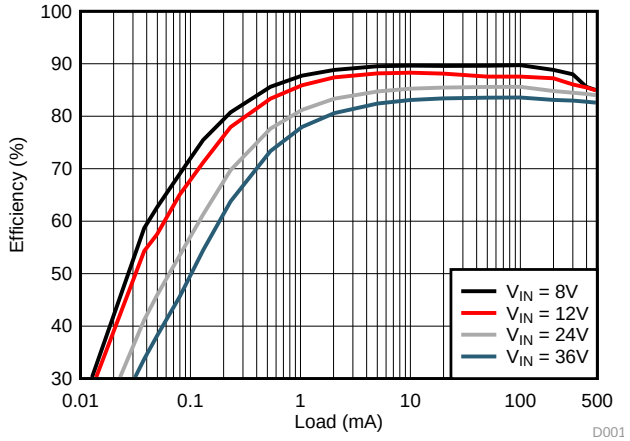

See schematic, 图 63 | $L_F$ = 47 µH | $C_{OUT}$ = 47 µF | $F_{SW(nom)}$ = 200 kHz | $R_{RT}$ = 100 kΩ

**图 2. Converter Efficiency: 3.3 V, 500 mA, COT**




See schematic, 图 70 | $L_F$ = 4.7 µH | $C_{OUT}$ = 47 µF | $F_{SW(nom)}$ = 600 kHz | $R_{RT}$ = 0 Ω

**图 3. Converter Efficiency: 3.3 V, 300 mA, PFM**




See schematic, 图 77 | $L_F$ = 22 µH | $C_{OUT}$ = 200 µF | $F_{SW(nom)}$ = 100 kHz | $R_{RT}$ = 0 Ω

**图 4. Converter Efficiency: 5 V, 500 mA, PFM**

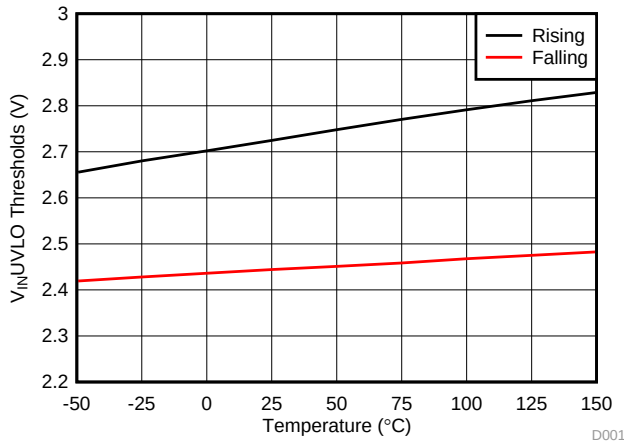



**图 5. Internal $V_{IN}$ UVLO Voltage vs Temperature**

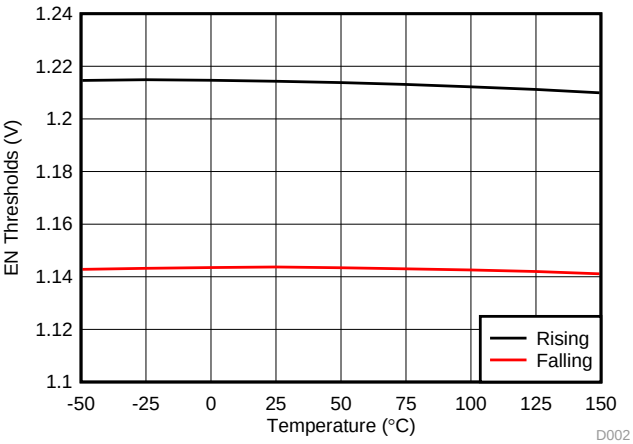



**图 6. Enable Threshold Voltage vs Temperature**

## Typical Characteristics (接下页)

Unless otherwise specified, $V_{IN}$ = 12 V, $V_{OUT}$ = 5 V. Please refer to Typical Applications for circuit designs.

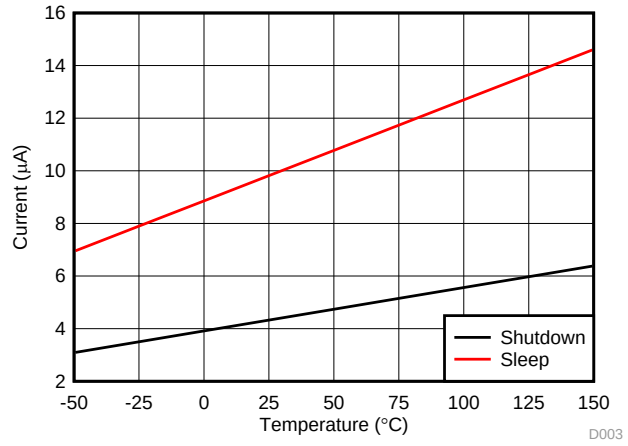



**图 7. $V_{IN}$ Sleep and Shutdown Supply Current vs Temperature**

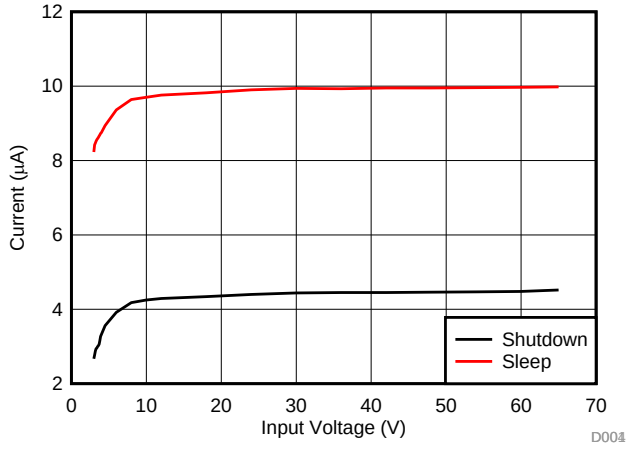
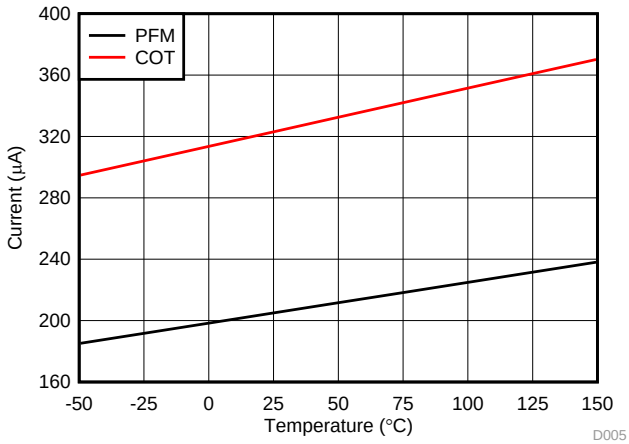
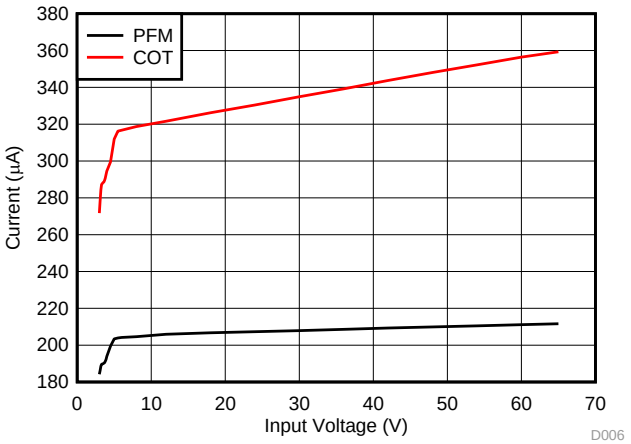



**图 8. $V_{IN}$ Sleep and Shutdown Supply Current vs Input Voltage**



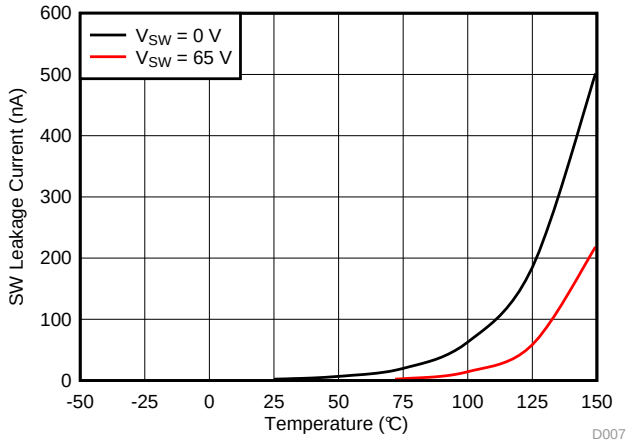

$R_{RT}$ = 100 kΩ

**图 9. $V_{IN}$ Active Mode Supply Current vs Temperature**




$R_{RT}$ = 100 kΩ

**图 10. $V_{IN}$ Active Mode Supply Current vs Input Voltage**




$V_{VIN}$ = 65 V

**图 11. SW Pin Leakage Current vs Temperature**

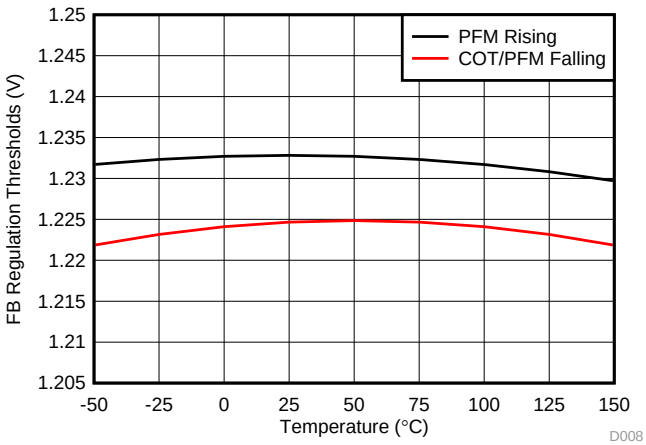
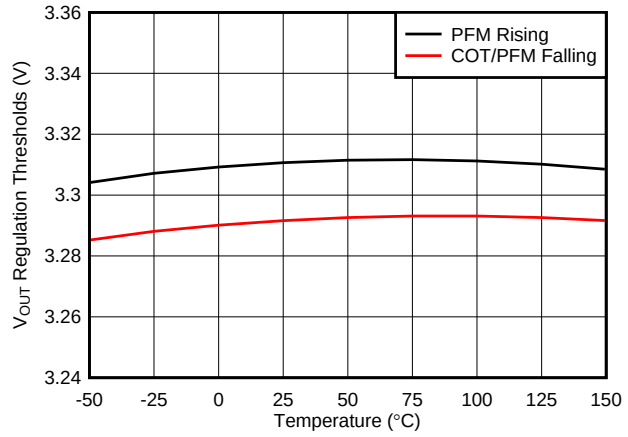



**图 12. Feedback Comparator Threshold Voltage vs Temperature**

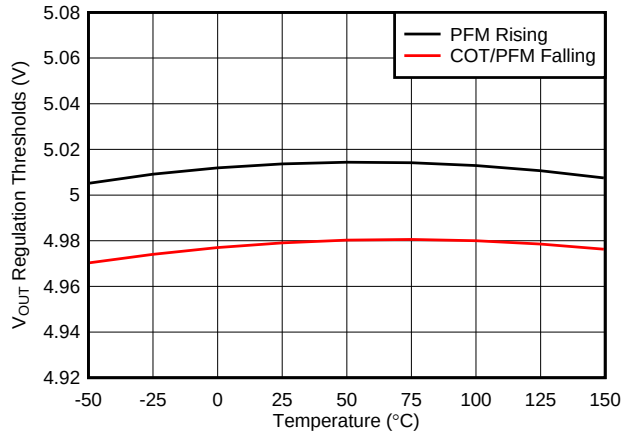
## Typical Characteristics (接下页)

Unless otherwise specified, $V_{IN}$ = 12 V, $V_{OUT}$ = 5 V. Please refer to Typical Applications for circuit designs.




LM5166Y

**图 13. VOUT Regulation Thresholds vs Temperature**




LM5166X

**图 14. VOUT Regulation Thresholds vs Temperature**

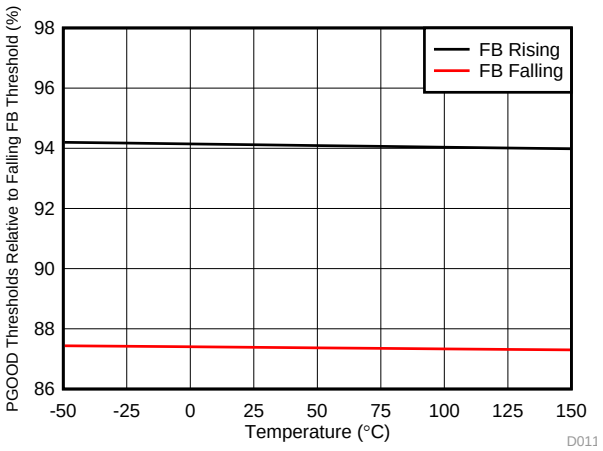



**图 15. PGOOD Thresholds vs Temperature**

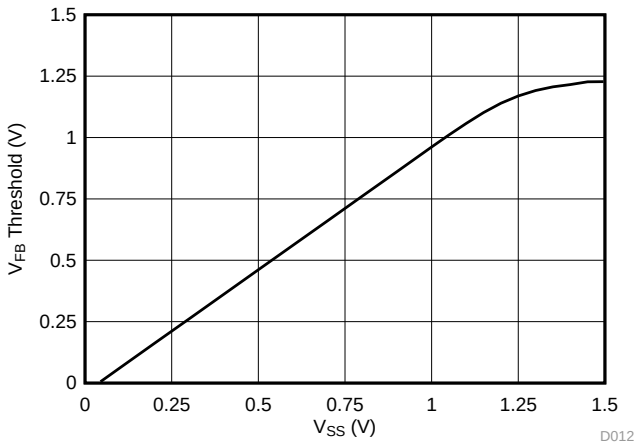



**图 16. Feedback Voltage vs Soft-Start Voltage**

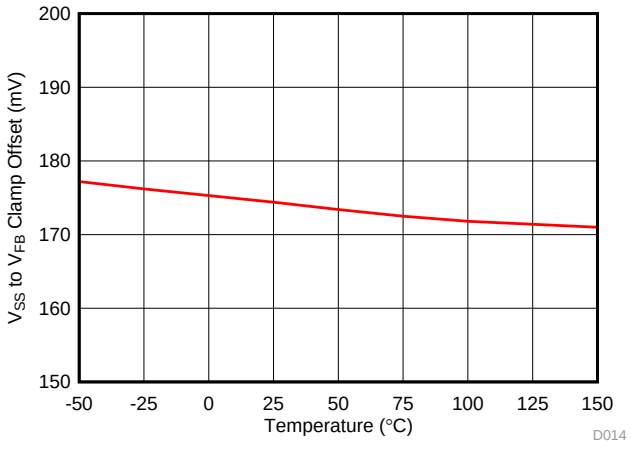



**图 17. Soft-Start to Feedback Clamp Offset vs Temperature**

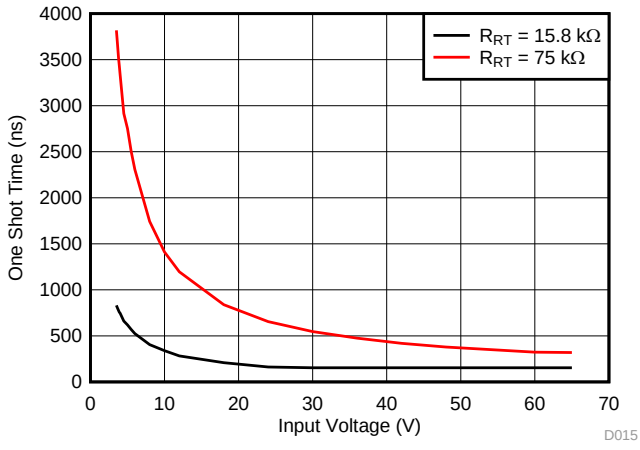



**图 18. COT One-Shot Timer $T_{ON}$ vs Input Voltage**

## Typical Characteristics (接下页)

Unless otherwise specified, $V_{IN}$ = 12 V, $V_{OUT}$ = 5 V. Please refer to Typical Applications for circuit designs.

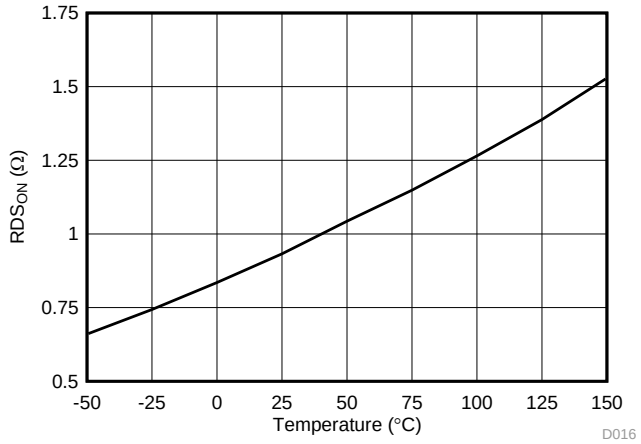



**图 19. High-Side MOSFET On-State Resistance vs Temperature**

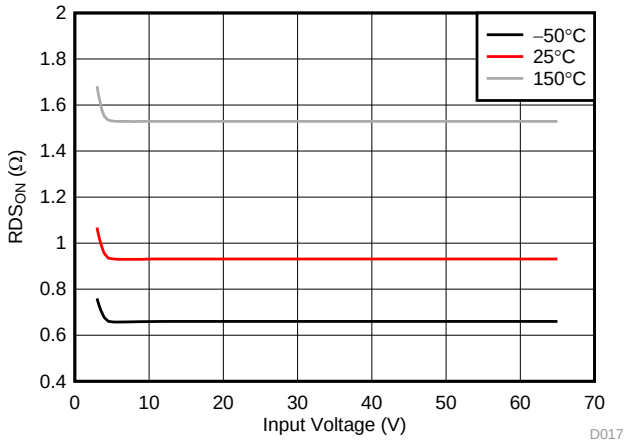



**图 20. High-Side MOSFET On-State Resistance vs Input Voltage**

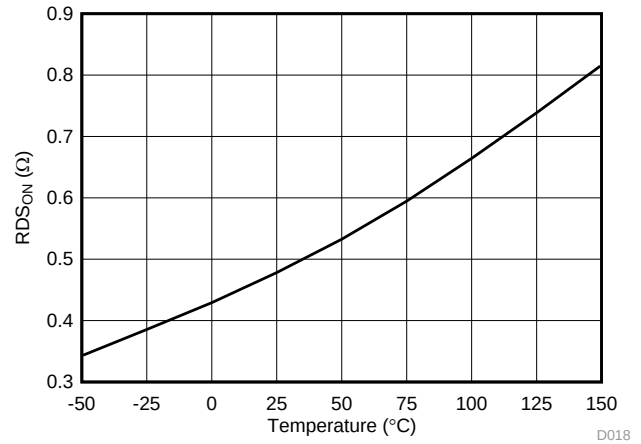



**图 21. Low-Side MOSFET On-State Resistance vs Temperature**

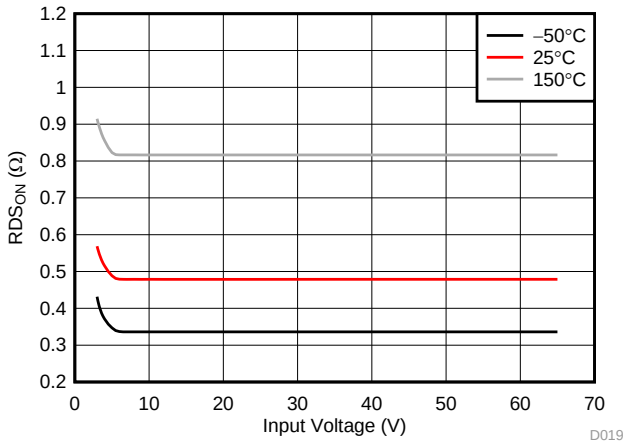



**图 22. Low-Side MOSFET On-State Resistance vs Input Voltage**

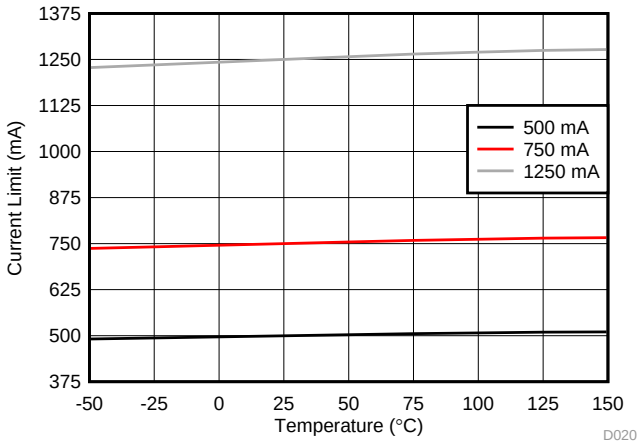



**图 23. High-Side Peak Current Limit vs Temperature**

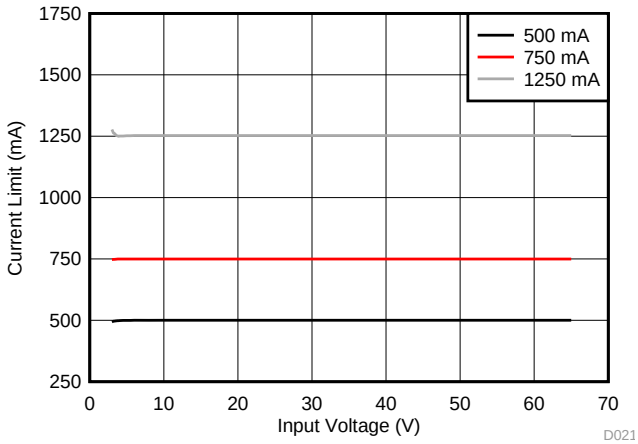



**图 24. High-Side Peak Current Limit vs Input Voltage**

## Typical Characteristics (接下页)

Unless otherwise specified, $V_{IN}$ = 12 V, $V_{OUT}$ = 5 V. Please refer to Typical Applications for circuit designs.

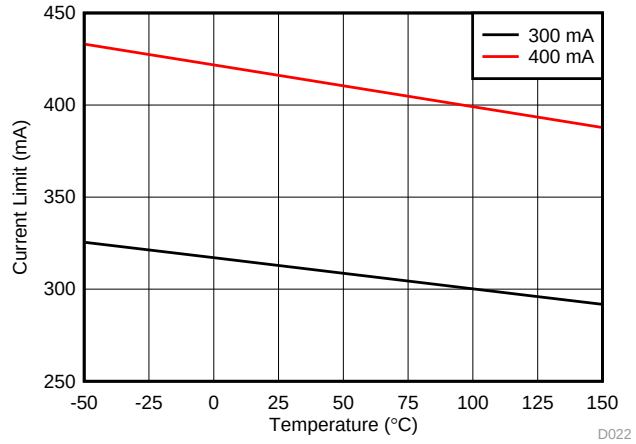



图 25. Low-Side Valley Current Limit vs Temperature

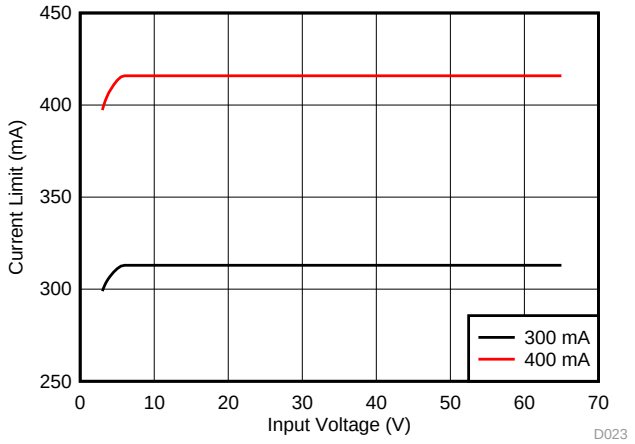



图 26. Low-Side Valley Current Limit vs Input Voltage

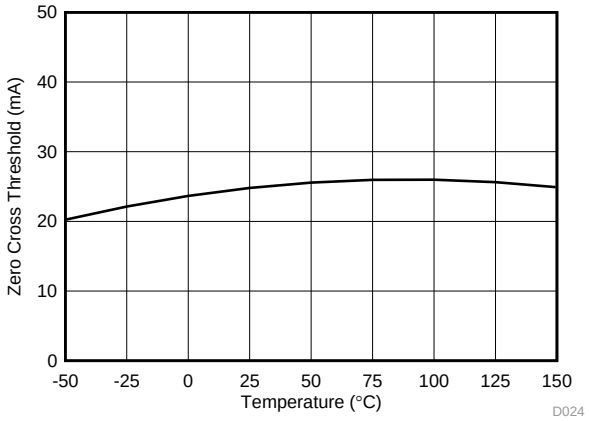



图 27. Zero-Cross Current Threshold vs Temperature

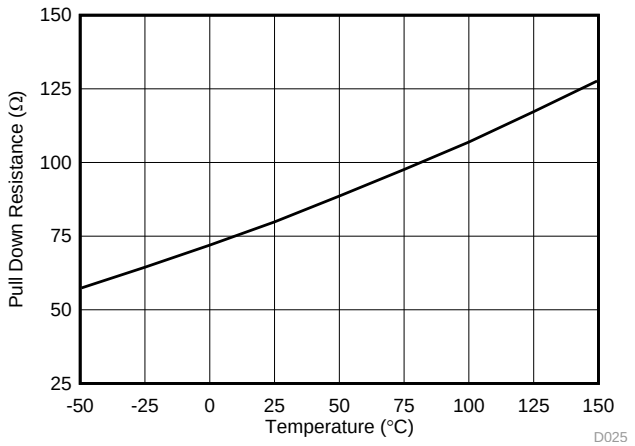
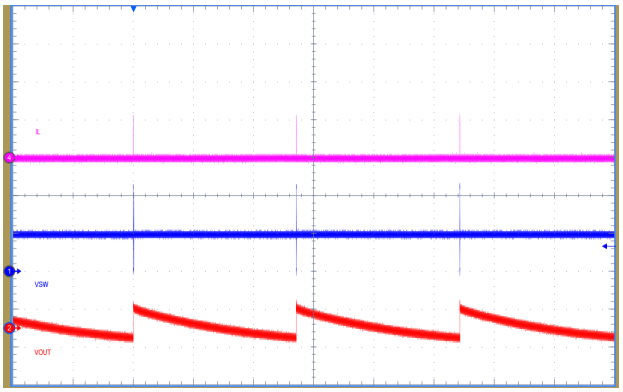
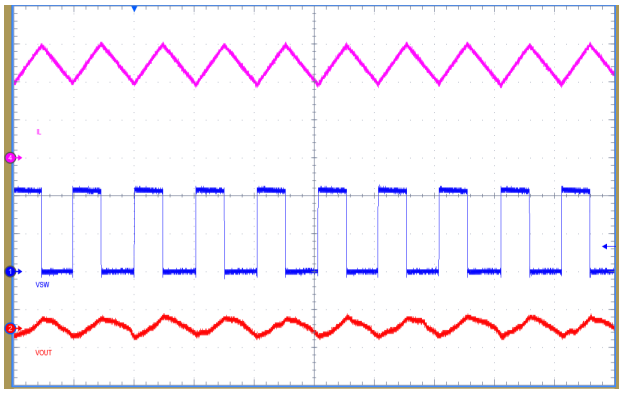



图 28. PGOOD and HYS Pulldown $R_{DS(on)}$ vs Temperature



Time Scale: 20 ms/Div
CH1: $V_{SW}$, 5 V/Div
CH2: $V_{OUT}$, 50 mV/Div
CH4: $I_L$, 200 mA/Div

图 29. No-Load Switching Waveforms, COT, Type 2

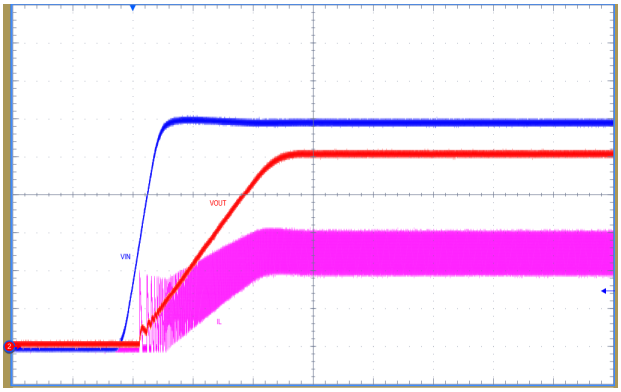


Time Scale: 10 µs/Div
CH1: $V_{SW}$, 5 V/Div
CH2: $V_{OUT}$, 50 mV/Div
CH4: $I_L$, 200 mA/Div

图 30. Full Load Switching Waveforms, COT, Type 2

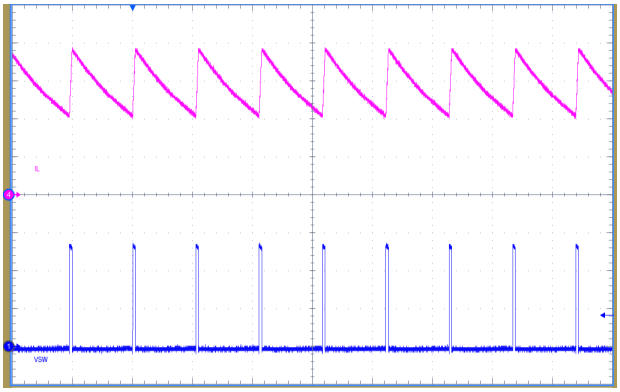
## Typical Characteristics (接下页)

Unless otherwise specified, $V_{IN}$ = 12 V, $V_{OUT}$ = 5 V. Please refer to Typical Applications for circuit designs.



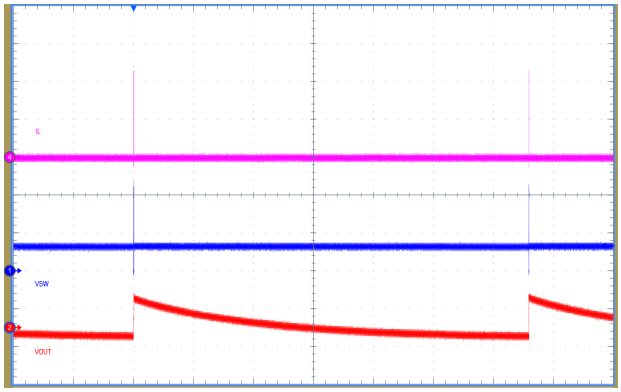
Time Scale: 2 ms/Div
CH1: $V_{IN}$, 2 V/Div
CH2: $V_{OUT}$, 1 V/Div
CH4: $I_L$, 200 mA/Div

**图 31. Full-Load Start-Up, COT, Type 2**



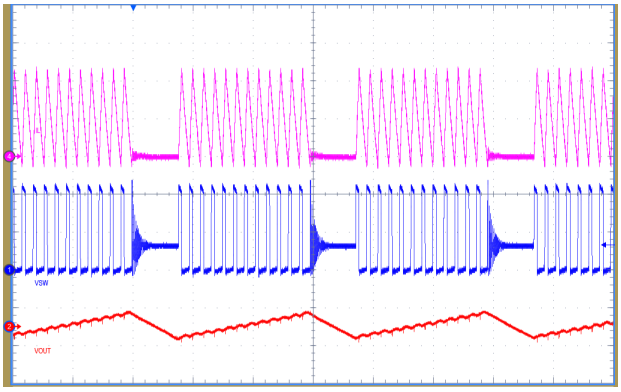
Time Scale: 100 µs/Div
CH1: $V_{SW}$, 4 V/Div
CH4: $I_L$, 200 mA/Div

**图 32. Short Circuit, COT, Type 2**



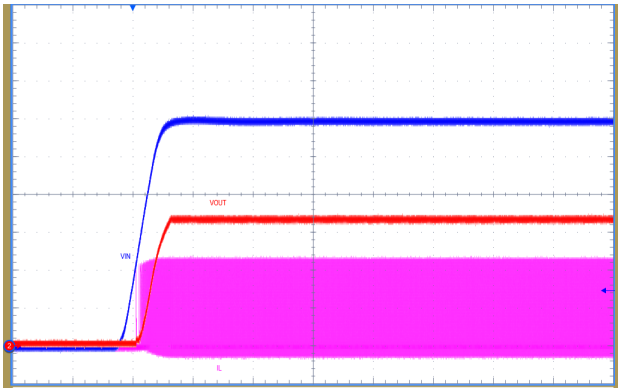
Time Scale: 20 ms/Div
CH1: $V_{SW}$, 5 V/Div
CH2: $V_{OUT}$, 50 mV/Div
CH4: $I_L$, 400 mA/Div

**图 33. No-Load Switching Waveforms PFM Mode, $I_{LIM}$ = 750 mA**



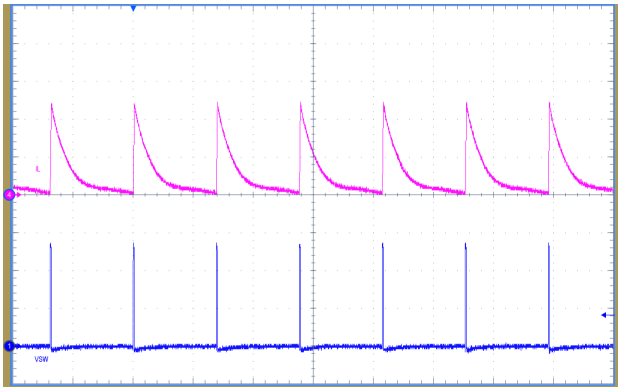
Time Scale: 10 µs/Div
CH1: $V_{SW}$, 5 V/Div
CH2: $V_{OUT}$, 100 mV/Div
CH4: $I_L$, 400 mA/Div

**图 34. Full-Load Switching Waveforms PFM Mode, $I_{LIM}$ = 750 mA**



Time Scale: 2 ms/Div
CH1: $V_{IN}$, 2 V/Div
CH2: $V_{OUT}$, 1 V/Div
CH4: $I_L$, 400 mA/Div

**图 35. Full-Load Start-Up, PFM, $I_{LIM}$ = 750 mA**

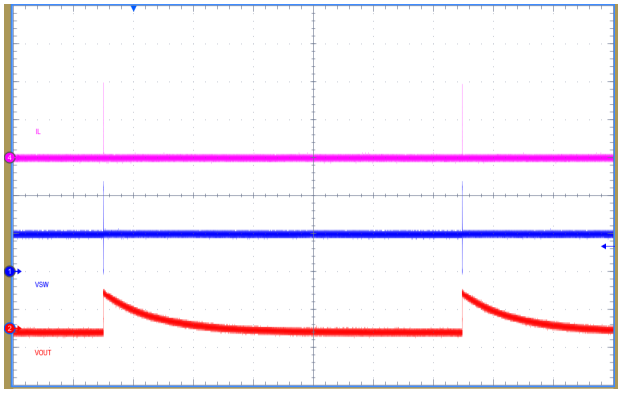


Time Scale: 20 µs/Div
CH1: $V_{SW}$, 4 V/Div
CH4: $I_L$, 400 mA/Div

**图 36. Short Circuit, PFM, $I_{LIM}$ = 750 mA**

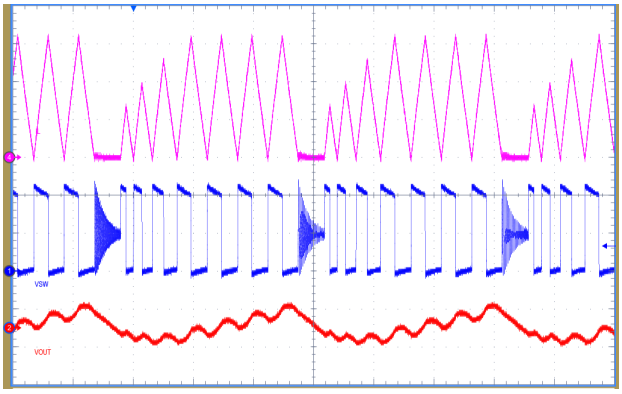
## Typical Characteristics (接下页)

Unless otherwise specified, $V_{IN}$ = 12 V, $V_{OUT}$ = 5 V. Please refer to Typical Applications for circuit designs.




Time Scale: 50 ms/Div
CH1: $V_{SW}$, 5 V/Div
CH2: $V_{OUT}$, 50 mV/Div
CH4: $I_L$, 400 mA/Div

**图 37. No-Load Switching Waveforms**
**PFM Mode, $I_{LIM}$ = 1.25 A, Modulated**




Time Scale: 20 µs/Div
CH1: $V_{SW}$, 5 V/Div
CH2: $V_{OUT}$, 100 mV/Div
CH4: $I_L$, 400 mA/Div

**图 38. Full-Load Switching Waveforms**
**PFM Mode, $I_{LIM}$ = 1.25 A, Modulated**

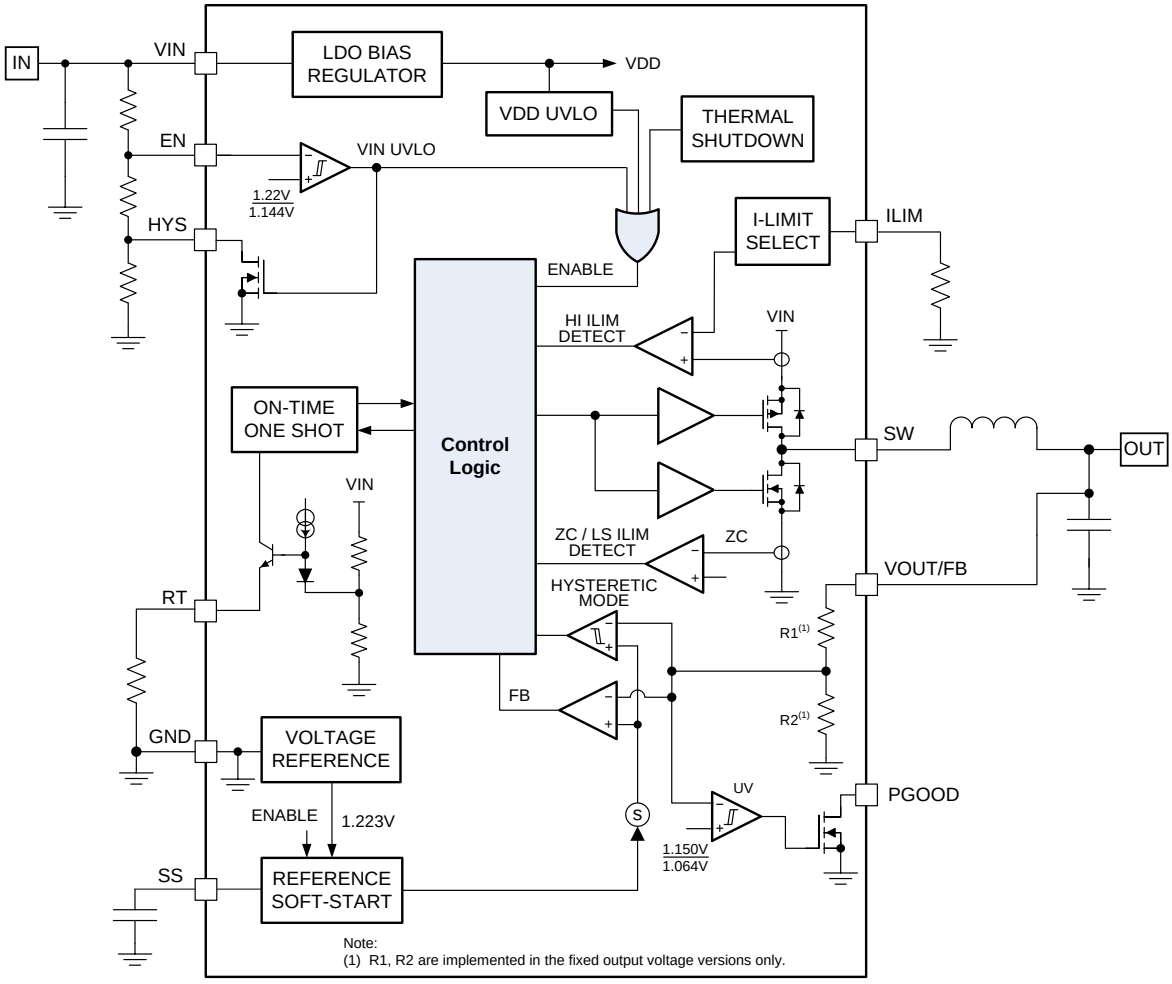
# 7 Detailed Description

## 7.1 Overview

The LM5166 regulator is an easy-to-use synchronous buck DC-DC converter that operates from a supply voltage ranging from 3 V to 65 V. The device is intended for step-down conversions from 5-V, 12-V, 24-V, and 48-V unregulated, semi-regulated, and fully-regulated supply rails. With integrated high-side and low-side power MOSFETs, the LM5166 delivers up to 500-mA DC load current with exceptional efficiency and ultra-low input quiescent current in a very small solution size. Designed for simple implementation, a choice of operating modes offers flexibility to optimize its usage according to the target application. Fixed-frequency, constant on-time (COT) operation with discontinuous conduction mode (DCM) at light loads is ideal for low-noise, high current, fast transient load requirements. Alternatively, pulse frequency modulation (PFM) mode, complemented by an adjustable current limit, achieves ultra-high light-load efficiency performance. Control loop compensation is not required with either operating mode, which reduces design time and external component count.

The LM5166 incorporates other features for comprehensive system requirements, including an open-drain Power Good circuit for power-rail sequencing and fault reporting, internally-fixed or externally-adjustable soft start, monotonic start-up into prebiased loads, precision enable with customizable hysteresis for programmable line undervoltage lockout (UVLO), and thermal shutdown with automatic recovery. These features enable a flexible and easy-to-use platform for a wide range of applications. The pin arrangement is designed for simple and optimized PCB *Layout*, requiring only a few external components.

## 7.2 Functional Block Diagram



## 7.3 Feature Description

### 7.3.1 Integrated Power MOSFETs

The LM5166 is a step-down buck converter with integrated high-side PMOS buck switch and low-side NMOS synchronous switch. During the high-side MOSFET on-time, the SW voltage $V_{SW}$ swings up to approximately $V_{IN}$, and the inductor current increases with slope $(V_{IN} – V_{OUT})/L_F$. When the high-side MOSFET is turned off by the control logic, the low-side MOSFET turns on after a fixed dead time. Inductor current flows through the low-side MOSFET with slope $–V_{OUT}/L_F$. Duty cycle D is defined as $T_{ON}/T_{SW}$, where $T_{ON}$ is the high-side MOSFET conduction time and $T_{SW}$ is the switching period.

### 7.3.2 Selectable PFM or COT Mode Converter Operation

Depending on how the RT pin is connected, the LM5166 operates in PFM or COT mode. With the RT pin tied to GND, the device operates in PFM mode. An $R_{RT}$ resistor connected between the RT and GND pins enables COT control and sets the desired switching frequency as defined by 公式 4. 图 39 and 图 40 show converter schematics for PFM and COT modes of operation.

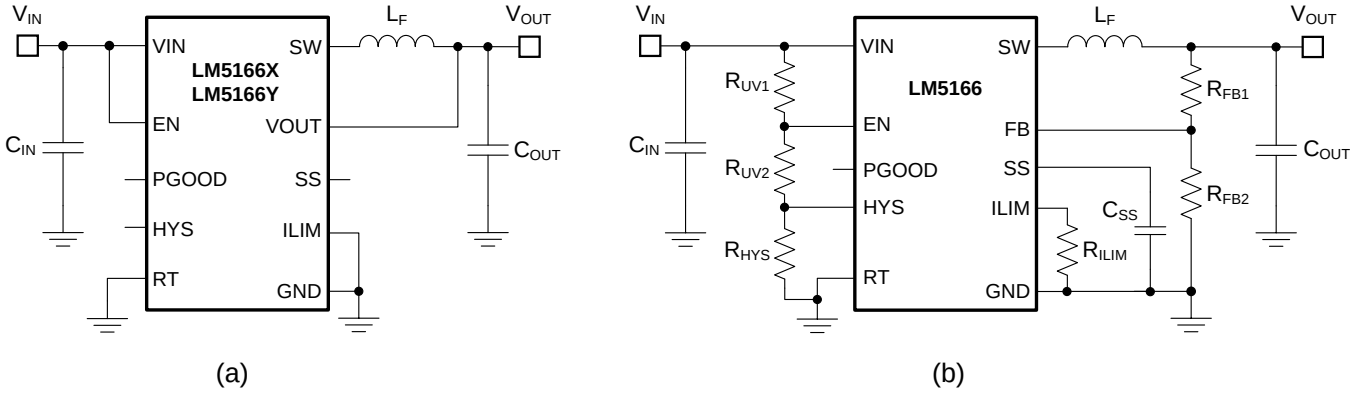



**图 39. PFM Mode Converter Schematics: (a) Fixed Output Voltage of 5 V or 3.3 V, (b) Adjustable Output Voltage With Programmable Soft Start, Current Limit, and UVLO**

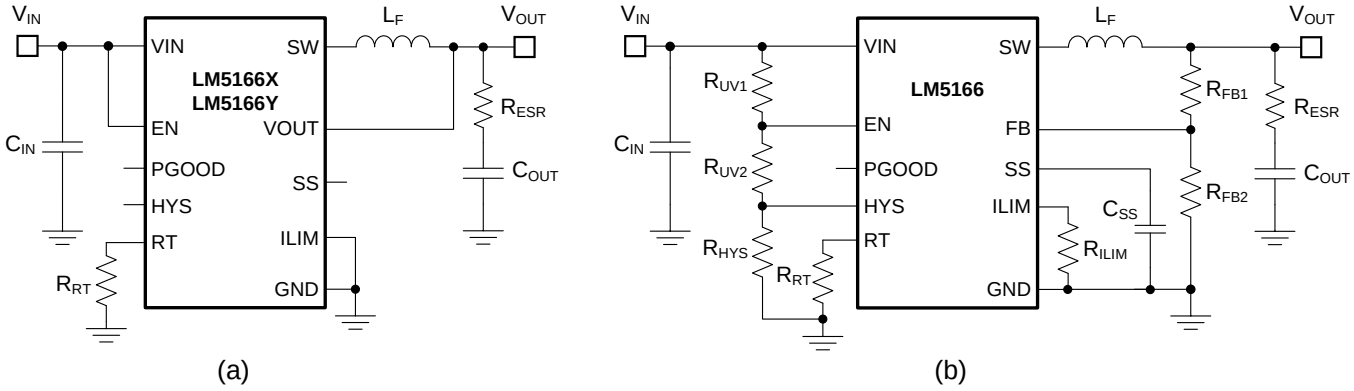



**图 40. COT Mode Converter Schematics: (a) Fixed Output Voltage of 5 V or 3.3 V, (b) Adjustable Output Voltage With Programmable Soft Start, Current Limit, and UVLO**

## Feature Description (接下页)

### 7.3.2.1 PFM Mode Operation

In PFM mode, the LM5166 behaves as a hysteretic voltage regulator operating in boundary conduction mode. The output voltage is regulated between upper and lower threshold levels according to the PFM feedback comparator hysteresis of 10 mV. 图 41 shows the relevant output voltage and inductor current waveforms. The LM5166 provides the required switching pulses to recharge the output capacitor to the upper threshold, followed by a sleep period where most of the internal circuits are disabled. The load current is supported by the output capacitor during this time, and the LM5166 current consumption reduces to 9.7 µA. The sleep period duration depends on load current and output capacitance.

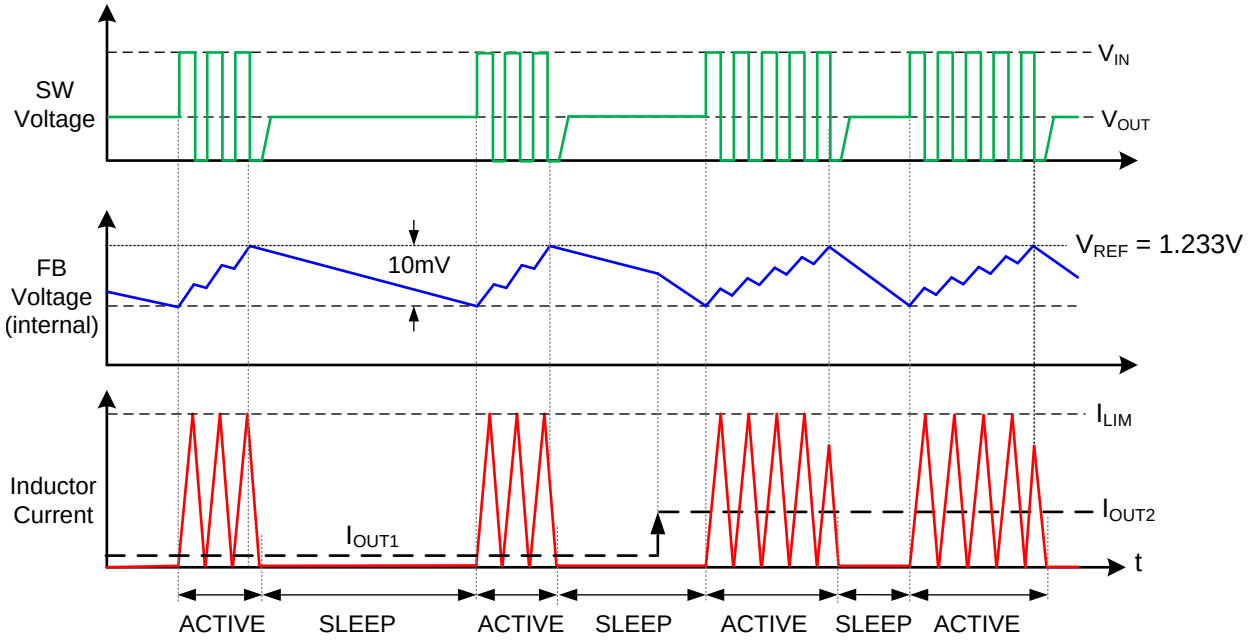



**图 41. PFM Mode Output Voltage and Inductor Current Representative Waveforms**

When operating in PFM mode at given input and output voltages, the chosen filter inductance dictates the PFM pulse frequency as

$$F_{SW(PFM)} = \frac{V_{OUT}}{L_F \cdot I_{PK(PFM)}} \cdot \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \quad (1)$$

where

- $I_{PK(PFM)}$ is one of the programmable levels for peak current limit. See Adjustable Current Limit for more detail.

One of the supported ILIM settings enables a function that modulates the peak current threshold levels during the first three switching cycles of each active period as illustrated in 图 42. This function improves efficiency under most application conditions at the expense of slightly degraded load transient response.

## Feature Description (接下页)

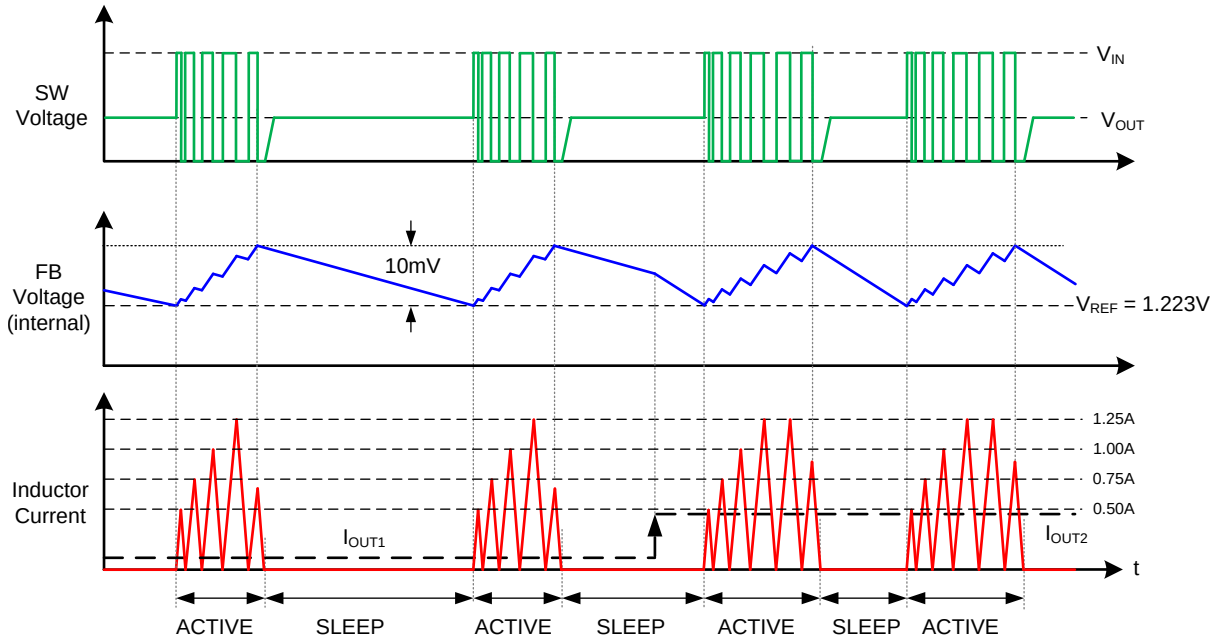



**图 42. PFM Mode With Modulated $I_{LIM}$, Output Voltage and Inductor Current Representative Waveforms**

As expected, the choice of mode and switching frequency represents a compromise between conversion efficiency, quiescent current, and passive component size. Lower switching frequency implies reduced switching losses (including gate charge losses, transition losses, and so forth) and higher overall efficiency. Higher switching frequency, on the other hand, implies smaller LC output filter and hence, a more compact design. Lower inductance also helps transient response and reduces the inductor DCR conduction loss. The ideal switching frequency in a given application is a tradeoff and thus is determined on a case-by-case basis. It relates to the input voltage, output voltage, most frequent load current level(s), external component choices, and circuit size requirement. At light loads, the PFM converter has a relatively longer sleep time interval and thus operates at lower input quiescent current levels.

### *7.3.2.2 COT Mode Operation*

In COT mode, the LM5166-based converter turns on the high-side MOSFET with constant on-time that adapts to $V_{IN}$, as defined by 公式 2, to operate with nearly fixed switching frequency when in continuous conduction mode (CCM). The high-side MOSFET turns on when the feedback voltage ($V_{FB}$) falls below the reference voltage. The regulator control loop maintains a constant output voltage by adjusting the PWM off-time as defined with 公式 3. For stable operation, the feedback voltage must decrease monotonically in phase with the inductor current during the off-time as explained in *Ripple Generation Methods*.

$$t_{ON}[ns] = \frac{175 \cdot R_{RT}[k\Omega]}{V_{IN}} \quad (2)$$

$$t_{OFF} = \frac{L_F \cdot \Delta I_{L(nom)}}{V_{OUT} + (R_{DCR} + R_{DSON2}) \cdot I_{OUT}} \quad (3)$$

Diode emulation mode (DEM) prevents negative inductor current, and pulse skipping maintains high efficiency at light load currents by decreasing the effective switching frequency. The COT-controlled LM5166 waveforms in CCM and DEM are shown in 图 43.

## Feature Description (接下页)

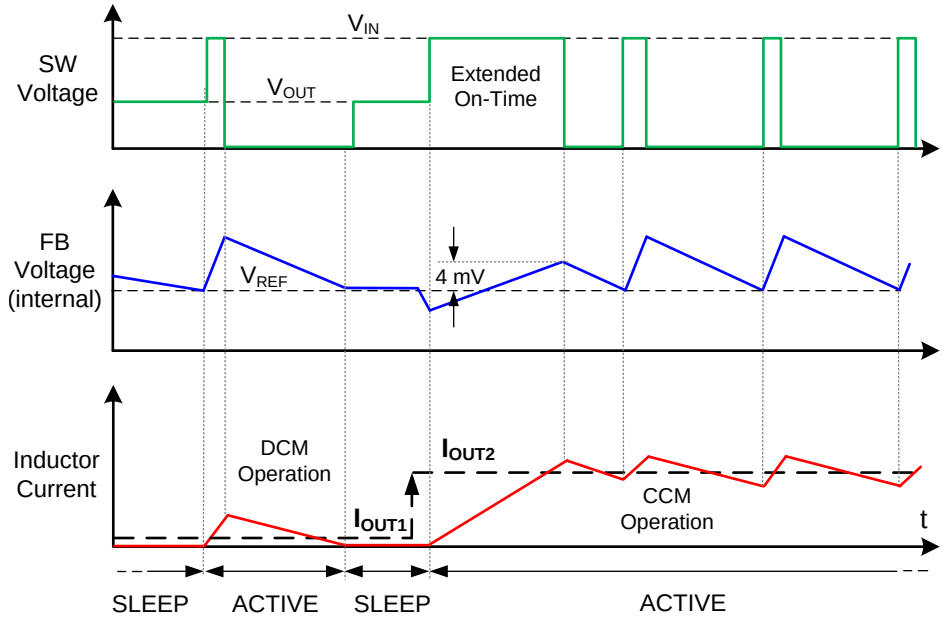



**图 43. COT Mode Feedback Voltage and Inductor Current Representative Waveforms**

The required on-time adjust resistance for a particular frequency (in CCM) is given in 公式 4 and tabulated in 表 1. The maximum programmable on-time is 15 µs.

$$R_{RT}[k\Omega] = \frac{V_{OUT}[V]}{F_{SW}[kHz]} \cdot \frac{10^4}{1.75} \quad (4)$$

**表 1. On-Time Adjust Resistance (E96 EIA Values) for Various Switching Frequencies and Output Voltages(1)**

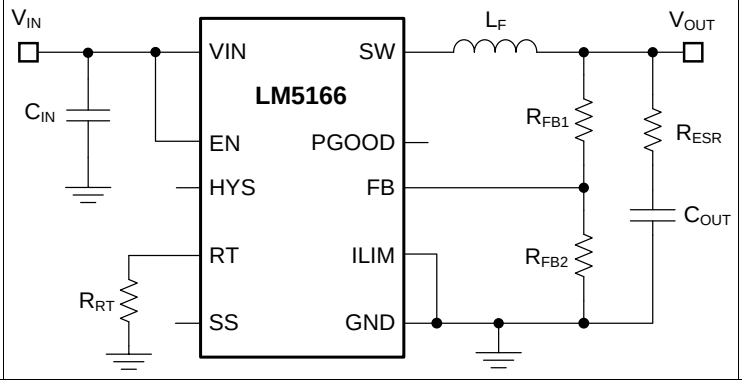
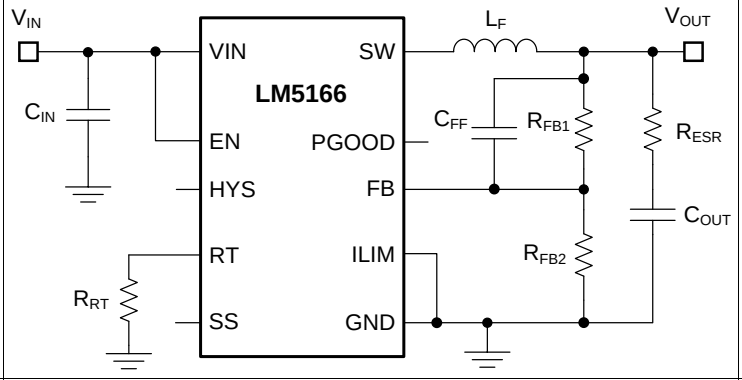
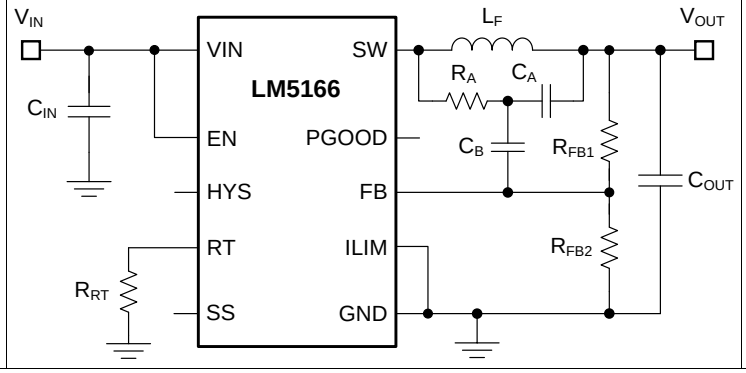
| $F_{SW}$ (kHz) | $R_{RT}$ (kΩ) | | | |
|---|---|---|---|---|
| | $V_{OUT}$ = 1.8 V | $V_{OUT}$ = 3.3 V | $V_{OUT}$ = 5 V | $V_{OUT}$ = 12 V |
| 100 | 102 | 187 | 287 | 681 |
| 200 | 51.1 | 95.3 | 143 | 340 |
| 300 | 34 | 63.4 | 95.3 | 226 |
| 400 | 25.5 | 47.5 | 71.5 | 169 |
| 500 | 20.5 | 37.4 | 57.6 | 137 |
| 600 | 16.9 | 31.6 | 47.5 | 115 |

(1) For a more precise adjustment of the switching frequency consider 公式 2 and 公式 3. The *LM5166 Quickstart Calculatorl* estimates and plots the switching frequency as a function of load current.

#### 7.3.2.2.1 Ripple Generation Methods

In the Constant-On-Time (COT) control scheme, the on-time is terminated by a one-shot, and the off-time is terminated by the feedback voltage ($V_{FB}$) falling below the reference voltage ($V_{FB1}$). Therefore, for stable operation, the feedback voltage must decrease monotonically in phase with the inductor current during the off-time. Furthermore, this change in feedback voltage ($V_{FB}$) during the off-time must be large enough to dominate any noise present at the feedback node.

**表 2. Ripple Generation Methods**

| TYPE | SCHEMATIC | CALCULATION |
|---|---|---|
| **Type 1**<br>Lowest Cost |  | $R_{ESR} \geq \frac{20mV \cdot V_{OUT}}{V_{FB1} \cdot \Delta I_{L(nom)}}$ (5)<br>$R_{ESR} \geq \frac{V_{OUT}}{2 \cdot V_{IN} \cdot F_{SW} \cdot C_{OUT}}$ (6) |
| **Type 2**<br>Reduced Ripple |  | $R_{ESR} \geq \frac{20mV}{\Delta I_{L(nom)}}$ (7)<br>$R_{ESR} \geq \frac{V_{OUT}}{2 \cdot V_{IN} \cdot F_{SW} \cdot C_{OUT}}$ (8)<br>$C_{FF} \geq \frac{1}{2\pi \cdot F_{SW} \cdot (R_{FB1} \parallel R_{FB2})}$ (9) |
| **Type 3**[(1)]<br>Lowest Ripple |  | $C_A \geq \frac{10}{F_{SW} \cdot (R_{FB1} \parallel R_{FB2})}$ (10)<br>$R_A C_A \leq \frac{(V_{IN\text{-}nom} - V_{OUT}) \cdot T_{ON\,(@V_{IN\text{-}nom})}}{20mV}$ (11)<br>$C_B \geq \frac{T_{TR-Settling}}{3 \cdot R_{FB1}}$ (12) |

(1) Lin, Min and others, "Frequency Domain Analysis of Fixed On-Time With Bottom Detection Control for Buck Converter," IEEE IECON 2010, pp. 481–485.

表 2 presents three different methods for generating appropriate voltage ripple at the feedback node. Type 1 ripple generation method uses a single resistor, designated $R_{ESR}$, in series with the output capacitor. The generated voltage ripple has two components:

- Capacitive ripple caused by the inductor ripple current charging and discharging the output capacitor.
- Resistive ripple caused by the inductor ripple current flowing in the output capacitor ESR and series resistance $R_{ESR}$.

The capacitive ripple component is out of phase with the inductor current. As a result, the capacitive ripple does not decrease monotonically during the off-time. The resistive ripple component is in phase with the inductor current and decreases monotonically during the off-time. The resistive ripple must exceed the capacitive ripple at the output ($V_{OUT}$) for stable operation. If this condition is not satisfied, unstable switching behavior is observed in COT converters, with multiple on-time bursts in close succession followed by a long off-time. 公式 5 and 公式 6 define the value of the $R_{ESR}$ resistor that ensures the required amplitude and phase of the ripple at the feedback node.

Type-2 ripple generation method uses a $C_{FF}$ capacitor in addition to the $R_{ESR}$ resistor. As the output voltage ripple is directly AC-coupled by $C_{FF}$ to the feedback node, the $R_{ESR}$ value and ultimately the output voltage ripple are reduced by a factor of $V_{OUT}$ / $V_{FB1}$.

Type-3 ripple generation method uses an RC network consisting of $R_A$ and $C_A$, and the switch node (SW) voltage to generate a triangular ramp. This triangular ramp is then AC-coupled into the feedback node (FB) with capacitor $C_B$. Because this circuit does not use the output voltage ripple, it is suited for applications where low output voltage ripple is critical. Application note *AN-1481 Controlling Output Ripple & Achieving ESR Independence in Constant On-Time Regulator Designs* provides additional details on this topic.

#### 7.3.2.2.2 COT Mode Light-Load Operation

Diode emulation mode (DEM) operation occurs when the low-side MOSFET switches off as the inductor valley current reaches zero. Here, the load current is less than half of the peak-to-peak inductor current ripple in CCM. Turning off the low-side MOSFET at zero current reduces switching loss, and preventing negative current conduction reduces conduction loss. In DEM, the duration that both high-side and low-side MOSFETs remain off progressively increases as load current decreases.

### 7.3.3 Low Dropout Operation and 100% Duty Cycle Mode

Using $R_{DSON1}$ and $R_{DSON2}$ for the high-side and low-side MOSFET on-state resistances, respectively, and $R_{DCR}$ for the inductor DC resistance, the duty cycle in COT (CCM) or PFM mode is given by 公式 13.

$$D = \frac{V_{OUT} + \left(R_{DSON2} + R_{DCR}\right) \cdot I_{OUT}}{V_{IN} - \left(R_{DSON1} - R_{DSON2}\right) \cdot I_{OUT}} \approx \frac{V_{OUT}}{V_{IN}} \tag{13}$$

The LM5166 provides a low input voltage to output voltage dropout by engaging the high-side MOSFET at 100% duty cycle. In COT operation, the extended on-time mode seamlessly increases the duty cycle during low dropout conditions or load-step transients. The buck switch on-time extends based on the requirement that the FB voltage exceeds the internal 4-mV FB comparator hysteresis during any COT mode on-time. The on-time (and duty cycle) are extended as needed at low input voltage conditions until the FB voltage reaches the upper threshold. 100% duty cycle operation is eventually reached as the input voltage decreases to a level near the output voltage setpoint. Very low dropout voltages can be achieved with 100% duty cycle and a low DCR inductor.

Note that PFM mode operation provides a natural transition to 100% duty cycle if needed during low input voltage conditions. If the input-to-output voltage difference is very low, the inductor current increases to a level determined by the load and may not reach the peak current threshold required to turn off the buck switch.

Use 公式 14 to calculate the minimum input voltage to maintain output regulation at 100% duty cycle.

$$V_{IN(min)} = V_{OUT} + I_{OUT} \cdot \left(R_{DSON1} + R_{DCR}\right) \tag{14}$$

### 7.3.4 Adjustable Output Voltage (FB)

Three voltage feedback settings are available. The fixed 3.3-V and 5-V versions include internal feedback resistors that sense the output directly through the VOUT pin, and the adjustable voltage option senses the output through an external resistor divider connected from the output to the FB pin.

The LM5166 voltage regulation loop regulates the output voltage by maintaining the FB voltage equal to the internal reference voltage ($V_{FB1}$). A resistor divider programs the ratio from output voltage $V_{OUT}$ to FB. For a target $V_{OUT}$ setpoint, calculate $R_{FB2}$ based on the selected $R_{FB1}$ by 公式 15.

$$R_{FB2} = \frac{1.223V}{V_{OUT} - 1.223V} \cdot R_{FB1} \tag{15}$$

$R_{FB1}$ in the range of 100 kΩ to 1 MΩ is recommended for most applications. A larger $R_{FB1}$ consumes less DC current, which is necessary if light-load efficiency is critical. However, $R_{FB1}$ larger than 1 MΩ is not recommended as the feedback path becomes more susceptible to noise. Larger feedback resistances generally require more careful feedback path PCB layout. It is important to route the feedback trace away from the noisy area of the PCB. For more PCB layout recommendations, see *Layout*.

### 7.3.5 Adjustable Current Limit

The LM5166 protects the system from overload conditions using cycle-by-cycle current limiting of the peak inductor current. The current sensed in the high-side MOSFET is compared to the current limit threshold set by the ILIM pin (see 表 3). Current is sensed after a 120-ns leading-edge blanking time following the high-side MOSFET turnon. The propagation delay of the current limit comparator is 80 ns, typical.

**表 3. Current Limit Thresholds**

| MODE OF OPERATION | $R_{ILIM}$ (kΩ) | TYPICAL $I_{HS\_LIM}$ (mA) | TYPICAL $I_{LS\_LIM}$ (mA) | $I_{OUT(max)}$ (mA) |
|---|---|---|---|---|
| COT Mode | 0 | 750 | 415 | 500 |
| | ≥ 100 (1) | 500 | 315 | 300 |
| PFM Mode | 0 | 1250 | N/A | 500 |
| | 24.9 | 1250 (2) | N/A | 500 |
| | 56.2 | 750 | N/A | 300 |
| | ≥ 100 (1) | 500 | N/A | 200 |

(1) For this current limit threshold selection, the ILIM pin may also be left open instead of using a 100-kΩ or greater resistor.
(2) This $I_{LIM}$ setting enables a function that modulates the $I_{LIM}$ levels during the first three switching cycles as illustrated in 图 42.

Note that in PFM mode, the inductor current ramps from zero to the chosen peak threshold every switching cycle. Consequently, the maximum output current is equal to half the peak inductor current. The output current capability in COT mode is higher and equal to the peak current threshold minus one-half the inductor ripple current. The ripple current is determined by the input and output voltages and the chosen inductance and switching frequency.

### 7.3.6 Precision Enable (EN) and Hysteresis (HYS)

The precision EN input supports adjustable input undervoltage lockout (UVLO) with hysteresis programmed independently through the HYS pin for application specific power-up and power-down requirements. EN connects to the input of a comparator with 76-mV hysteresis. The reference input of the comparator is connected to a 1.22-V bandgap reference. An external logic signal can be used to drive EN input to toggle the output on and off for system sequencing or protection. The simplest way to enable operation is to connect EN directly to VIN. This allows self-start-up of the LM5166 when $V_{IN}$ is within its valid operating range.

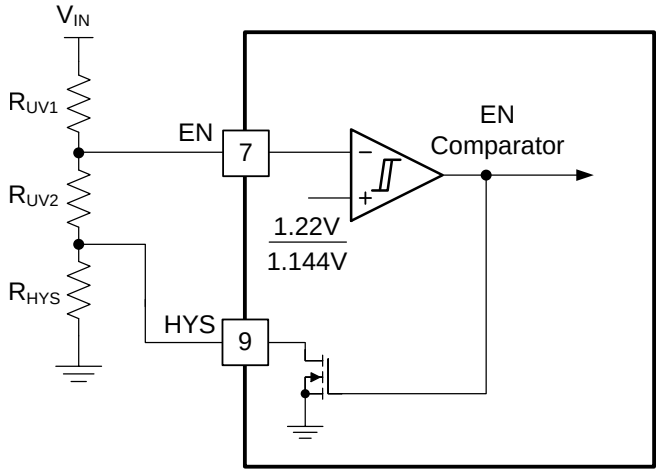



**图 44. Input Voltage UVLO Using EN and HYS**

However, many applications benefit from using a resistor divider $R_{UV1}$ and $R_{UV2}$ as shown in 图 44 to establish a precision UVLO level. Adding $R_{HYS}$ and the connection to the HYS pin increases the voltage hysteresis as needed.

The input UVLO voltages are calculated using 公式 16 and 公式 17.

$$V_{IN(on)} = 1.22V \cdot \left(1 + \frac{R_{UV1}}{R_{UV2}}\right) \quad (16)$$

$$V_{IN(off)} = 1.144V \cdot \left(1 + \frac{R_{UV1}}{R_{UV2} + R_{HYS}}\right) \quad (17)$$

The LM5166 enters a low $I_Q$ shutdown mode when EN is pulled below an NPN transistor base-emitter voltage drop (approximately 0.6 V at room temperature). If EN is below this hard shutdown threshold, the internal LDO regulator powers off and the internal bias supply rail collapses, turning off the bias currents of the LM5166.

### 7.3.7 Power Good (PGOOD)

The LM5166 has a built-in PGOOD flag to indicate whether the output voltage is within a regulation window. The PGOOD signal can be used for start-up sequencing of downstream converters, as shown in 图 45, or fault protection. PGOOD is an open-drain output that requires a pullup resistor to a DC supply (12 V maximum). Typical range of pullup resistance is 10 kΩ to 100 kΩ. If necessary, use a resistor divider to decrease the PGOOD pin voltage from a higher pullup rail.

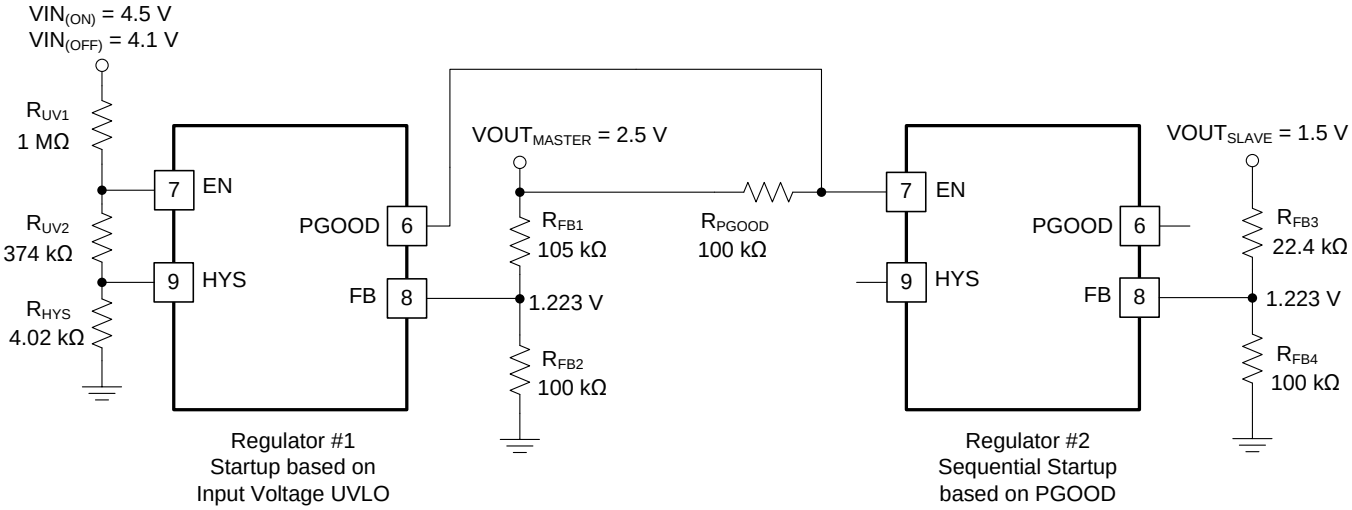



**图 45. Master-Slave Sequencing Implementation Using PGOOD and EN**

When the FB voltage exceeds 94% of the internal reference $V_{FB1}$, the PGOOD switch turns off and PGOOD will be pulled high. If the FB voltage falls below 87% of $V_{FB1}$, the PGOOD switch turns on, and PGOOD pulls low to indicate *power bad*. The rising edge of PGOOD has a built-in noise filter delay of 5 µs.

### 7.3.8 Configurable Soft Start (SS)

The LM5166 has a flexible and easy-to-use start-up control through the SS pin. A soft-start feature prevents inrush current impacting the LM5166 and its supply when power is first applied. Soft start is achieved by slowly ramping up the target regulation voltage when the device is enabled or powered up. Selectable and adjustable soft-start timing options include minimum delay (no soft-start), 900-µs internally fixed soft-start, and an externally-adjustable soft start.

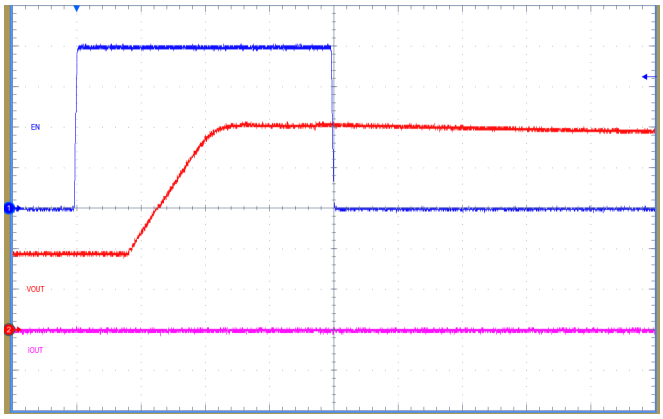
The simplest way to use the LM5166 is to leave the SS pin open circuit for a 900-µs soft-start time. The LM5166 will employ the internal soft-start control ramp and start-up to the regulated output voltage. In applications with a large amount of output capacitors, higher $V_{OUT}$, or other special requirements, extend the soft-start time by connecting an external capacitor $C_{SS}$ from SS to GND. Longer soft-start time further reduces the supply current needed to charge the output capacitors. An internal current source ($I_{SS}$ = 10 µA) charges $C_{SS}$ and generates a ramp to control the ramp rate of the output voltage. For a desired soft-start time $t_{SS}$, the $C_{SS}$ capacitance is:

$$C_{SS}\left[nF\right] = 8.1 \cdot t_{SS}\left[ms\right] \quad (18)$$

$C_{SS}$ is discharged by an internal 80-Ω FET when $V_{OUT}$ is shutdown by EN, UVLO, or thermal shutdown.

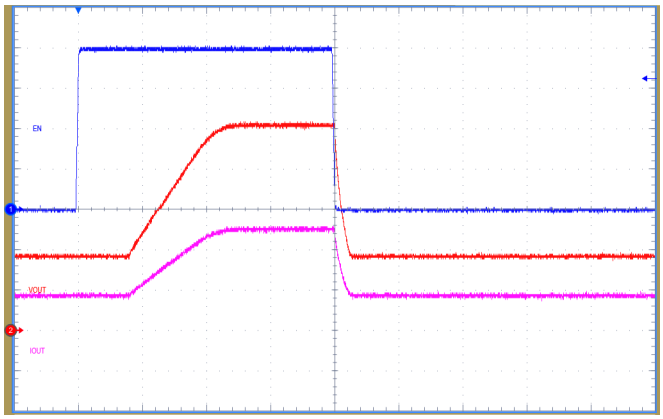
It is desirable in some applications for the output voltage to reach its nominal setpoint in the shortest possible time. Connecting a 100-kΩ resistor from SS to GND disables the soft-start circuit of the LM5166, and the LM5166 operates in current limit during start-up to rapidly charge the output capacitance.

Diode emulation mode (DEM) of the LM5166 prevents negative inductor current enabling monotonic start-up under prebiased output conditions. With a prebiased output voltage, the LM5166 waits until the soft-start ramp allows regulation above the prebiased voltage and then follows the soft-start ramp to the regulation setpoint as shown in 图 46 and 图 47.




Time Scale: 2 ms/Div
CH1: $V_{EN}$, 1 V/Div
CH2: $V_{OUT}$, 1 V/Div
CH4: $I_{OUT}$, 200 mA/Div

**图 46. ENABLE On and Off; $V_{OUT}$ Prebiased to 1.8 V 图 52 Circuit, $V_{IN}$ = 24 V, No Load**




Time Scale: 2 ms/Div
CH1: $V_{EN}$, 5 V/Div
CH2: $V_{OUT}$, 1 V/Div
CH4: $I_{OUT}$, 200 mA/Div

**图 47. ENABLE On and Off; $V_{OUT}$ Prebiased to 1.8 V 图 52 Circuit, $V_{IN}$ = 24 V, 500 mA Load**

### 7.3.9 Short-Circuit Operation

The LM5166 features a clamping circuit that clamps the SS voltage about 175 mV above the FB voltage (see 图 48 and 图 49). The circuit is enabled in COT mode and only works when an external soft-start capacitor is connected.

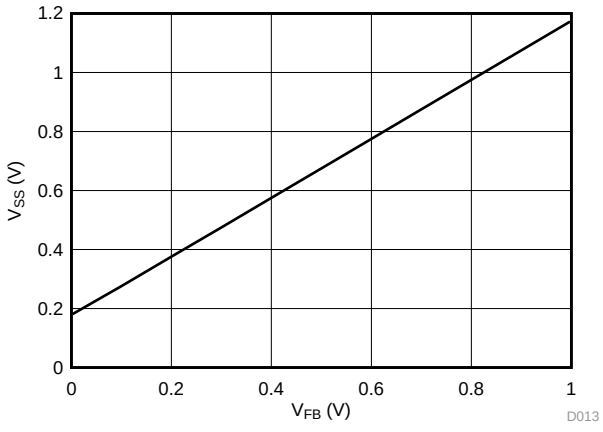



**图 48. Soft-Start (SS) Voltage vs Feedback (FB) Voltage**

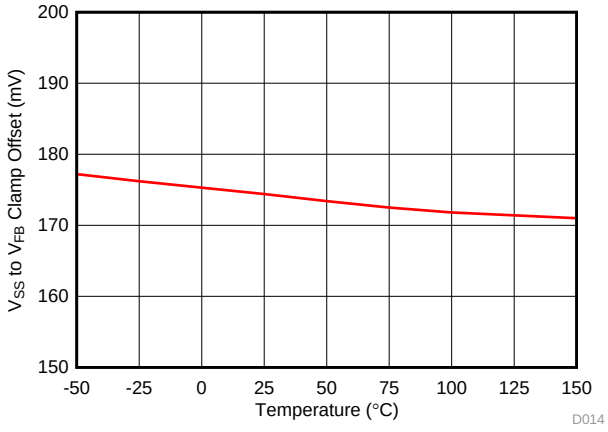



**图 49. Soft-Start to Feedback Clamp Offset vs Temperature**

In case of an overload event such as an output short circuit, the clamping circuit discharges the soft-start capacitor. When the short is removed, the FB voltage quickly rises until it reaches the level of the SS pin. Then, the recovery continues under the soft-start capacitor control. 图 50 and 图 51 show short-circuit entry and recovery waveforms.

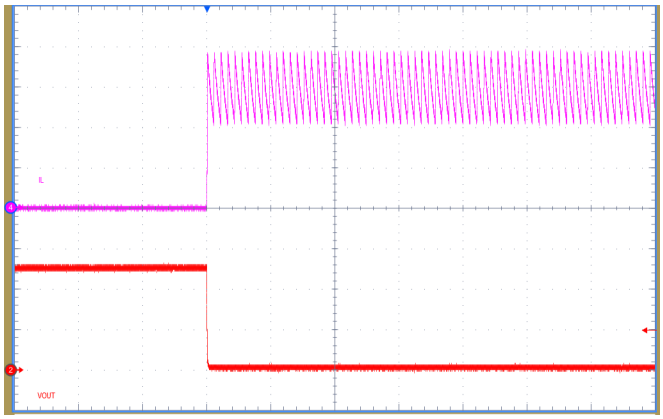



**图 50. Short-Circuit Entry (图 52 Circuit)**

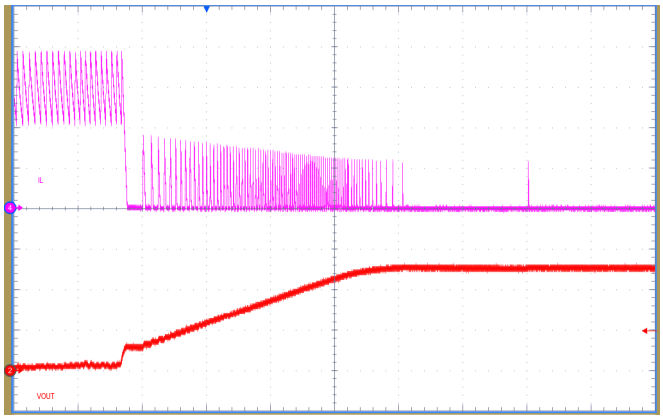



**图 51. Short-Circuit Recovery (图 52 Circuit)**

### 7.3.10 Thermal Shutdown

Thermal shutdown is a built-in self protection to limit junction temperature and prevent damage related to overheating. Thermal shutdown turns off the device when the junction temperature exceeds 170°C typically to prevent further power dissipation and temperature rise. Junction temperature decreases during thermal shutdown, and the LM5166 restarts when the junction temperature falls to 160°C.

## 7.4 Device Functional Modes

### 7.4.1 Shutdown Mode

The EN pin provides ON / OFF control for the LM5166. When $V_{EN}$ is below 0.3 V, the device is in shutdown mode. Both the internal LDO and the switching regulator are off. The quiescent current in shutdown mode drops to 4 µA (typical) at $V_{IN}$ = 12 V. The LM5166 also includes undervoltage protection of the internal bias LDO. If the internal bias supply voltage is below the UV threshold level, the switching regulator remains off.

### 7.4.2 Standby Mode

The internal bias LDO has a lower enable threshold than the switching regulator. When $V_{EN}$ is above 0.6 V and below the precision enable threshold (1.22 V typically), the internal LDO is on and regulating. The precision enable circuitry is turned on if the LDO output is above the bias rail UV threshold. The switching action and output voltage regulation are disabled in the standby mode.

### 7.4.3 Active Mode – COT

The LM5166 is in active mode when $V_{EN}$ is above the precision enable threshold and the internal bias rail is above its UV threshold level. In COT active mode, the LM5166 operates in one of three modes depending on the load current:

1. CCM with fixed switching frequency when the load current is more than half of the peak-to-peak inductor current ripple;
2. Pulse skipping and diode emulation mode when load current is less than half of the peak-to-peak inductor current ripple of CCM operation;
3. Extended on-time mode when $V_{IN}$ is nearly equal to $V_{OUT}$ (dropout) and during load step transients.

### 7.4.4 Sleep Mode – COT

The LM5166 is in COT sleep mode when $V_{EN}$ and $V_{IN}$ are above their relevant threshold levels, FB has exceeded its upper hysteresis level, and the output capacitor is sourcing the load current. In COT sleep mode, the LM5166 operates with very low quiescent current (9.7 µA typical). There is a 2-µs wake-up delay from sleep to active modes.

### 7.4.5 Active Mode – PFM

The LM5166 is in PFM active mode when $V_{EN}$ and $V_{IN}$ are above their relevant thresholds, FB has fallen below the lower hysteresis level, and boundary conduction mode switching is recharging the output capacitor to the upper hysteresis level.

### 7.4.6 Sleep Mode – PFM

The LM5166 is in PFM sleep mode when $V_{EN}$ and $V_{IN}$ are above their relevant threshold levels, FB has exceeded the upper hysteresis level, and the output capacitor is sourcing the load current. In PFM sleep mode, the LM5166 operates with very low quiescent current (9.7 µA typical). There is a 2-µs wake-up delay from sleep to active modes.

# 8 Applications and Implementation

**注**

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

## 8.1 Application Information

The LM5166 only requires a few external components to convert from a wide range of supply voltages to a fixed output voltage. To expedite and streamline the process of designing a LM5166-based converter, a comprehensive *LM5166 Quickstart Calculator* is available for download to assist the designer with component selection for a given application. WEBENCH® online software is also available to generate complete designs, leveraging iterative design procedures and access to comprehensive component databases. The following sections discuss the design procedure for both COT and PFM converters using specific circuit design examples.

The LM5166 integrates several optional features to meet system design requirements, including precision enable, UVLO, programmable soft start, programmable switching frequency in COT mode, adjustable current limit, and PGOOD indicator. Each application incorporates these features as needed for a more comprehensive design. The application circuits detailed below show LM5166 configuration options suitable for several application use cases. Please see the *LM5166EVM-C50A* and *LM5166EVM-C33A* EVM user's guides for more detail.

## 8.2 Typical Applications

TIDesigns

For step-by-step design procedure, circuit schematics, bill of materials, PCB files, simulation and test results of an LM5166-powered implementation, refer to *24-V AC Power Stage with Wide $V_{IN}$ Converter and Battery Gauge for Smart Thermostat* reference design.

### 8.2.1 Design 1: Wide $V_{IN}$, Low $I_Q$, High-Efficiency COT Converter Rated at 5 V, 500 mA

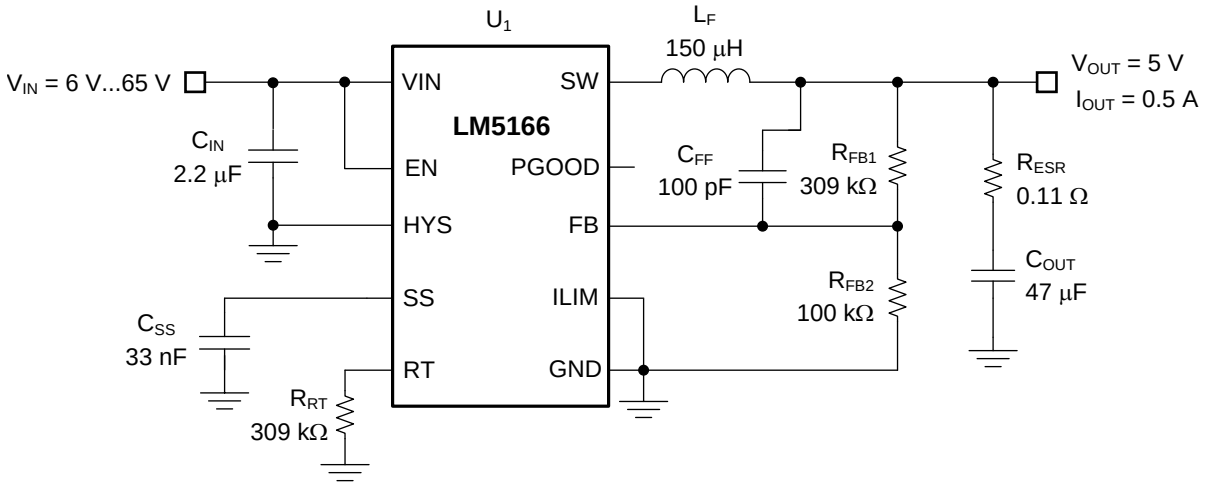





**图 52. Schematic for Design 1 With $V_{IN(nom)}$ = 24 V, $V_{OUT}$ = 5 V, $I_{OUT(max)}$ = 500 mA, $F_{SW(nom)}$ = 100 kHz**

#### *8.2.1.1 Design Requirements*

The target efficiency is 90% for loads above 10 mA based on a nominal input voltage of 24 V and an output voltage of 5 V. The required input voltage range is 6 V to 65 V. The LM5166 is chosen to deliver a 5-V output voltage. The switching frequency is set at 100 kHz. The output voltage soft-start time is 4 ms. The required components are listed in 表 4.

**表 4. List of Components for Design 1(1)**

| COUNT | REF DES | DESCRIPTION | PART NUMBER | MFR |
|---|---|---|---|---|
| 1 | $C_{IN}$ | Capacitor, Ceramic, 2.2 µF, 100 V, X7R, 10%, 1210 | GRM32ER72A225KA35L | Murata |
| 1 | $C_{OUT}$ | Capacitor, Ceramic, 47 µF, 10 V, X7R, 10%, 1210 | GRM32ER71A476KE15L | Murata |
| 1 | $C_{SS}$ | Capacitor, Ceramic, 33 nF, 16 V, X7R, 10%, 0402 | Std | Std |
| 1 | $C_{FF}$ | Capacitor, Ceramic, 100 pF, 50 V, X7R, 10%, 0402 | Std | Std |
| 1 | $L_F$ | Inductor, 150 µH, 0.240 Ω typ, 1.4 A Isat, 5 mm max | 7447714151 | Würth |
| | | Inductor, 150 µH, 0.285 Ω typ, 1.12 A Isat, 5.1 mm max | CDRH105RNP-151NC | Sumida |
| 1 | $R_{RT}$ | Resistor, Chip, 309 kΩ, 1/16W, 1%, 0402 | Std | Std |
| 1 | $R_{FB1}$ | Resistor, Chip, 309 kΩ, 1/16W, 1%, 0402 | Std | Std |
| 1 | $R_{ESR}$ | Resistor, Chip, 0.11 Ω, 1/16W, 1%, 0402 | Std | Std |
| 1 | $R_{FB2}$ | Resistor, Chip, 100 kΩ, 1/16W, 1%, 0402 | Std | Std |
| 1 | $U_1$ | LM5166, Synchronous Buck Converter, VSON-10, ADJ | LM5166DRCR | TI |

(1) See *第三方产品免责声明*.

### *8.2.1.2 Detailed Design Procedure*

#### 8.2.1.2.1 Custom Design With WEBENCH® Tools

Click here to create a custom design using the LM5166 device with the WEBENCH® Power Designer.

1. Start by entering the input voltage ($V_{IN}$), output voltage ($V_{OUT}$), and output current ($I_{OUT}$) requirements.
2. Optimize the design for key parameters such as efficiency, footprint, and cost using the optimizer dial.
3. Compare the generated design with other possible solutions from Texas Instruments.

The WEBENCH Power Designer provides a customized schematic along with a list of materials with real-time pricing and component availability.

In most cases, these actions are available:

- Run electrical simulations to see important waveforms and circuit performance
- Run thermal simulations to understand board thermal performance
- Export customized schematic and layout into popular CAD formats
- Print PDF reports for the design, and share the design with colleagues

Get more information about WEBENCH tools at www.ti.com/WEBENCH.

#### 8.2.1.2.2 Feedback Resistors – $R_{FB1}$, $R_{FB2}$

While the 5-V fixed output version of the LM5166 is suitable here, the adjustable version is chosen to provide the user with the option to trim or margin the output voltage if needed. The feedback resistor divider network comprises the upper feedback resistor $R_{FB1}$ and lower feedback resistor $R_{FB2}$. Select $R_{FB1}$ of 309 kΩ to minimize quiescent current and improve light-load efficiency in this application. With the desired output voltage setpoint of 5 V and $V_{FB}$ = 1.223 V, calculate the resistance of $R_{FB2}$ using 公式 15 as 100.1 kΩ. Choose the closest available standard value of 100 kΩ for $R_{FB2}$. See *Adjustable Output Voltage (FB)* for more details.

#### 8.2.1.2.3 Switching Frequency – $R_T$

The switching frequency of a COT-configured LM5166 is set by the on-time programming resistor at the RT pin. Using 公式 4, a standard 1% resistor of 309 kΩ gives a switching frequency of 92 kHz. Including the inductor $R_{DCR}$ and $R_{DSON2}$ in the calculation of $t_{OFF}$ (公式 3) gives an adjusted $F_{SW}$ of 101 kHz at 500 mA. The *LM5166 Quickstart Calculator* estimates and plots the switching frequency as a function of load current.

Note that at very low duty cycles, the minimum controllable on-time of the high-side MOSFET, $T_{ON(min)}$, of 180 ns may affect choice of switching frequency. In CCM, $T_{ON(min)}$ limits the voltage conversion step-down ratio for a given switching frequency. The minimum controllable duty cycle is given by 公式 19.

$$D_{MIN} = T_{ON(min)} \cdot F_{SW} \quad (19)$$

Given a fixed $T_{ON(min)}$, it follows that higher switching frequency implies a larger minimum controllable duty cycle. Ultimately, the choice of switching frequency for a given output voltage affects the available input voltage range, solution size, and efficiency. The maximum supply voltage for a given $T_{ON(min)}$ before switching frequency reduction occurs is given by 公式 20.

$$V_{IN(max)} = \frac{V_{OUT}}{T_{ON(min)} \cdot F_{SW}} \tag{20}$$

#### 8.2.1.2.4 Filter Inductance – $L_F$

The inductor ripple current (assuming CCM operation) and peak inductor current are given respectively by 公式 21 and 公式 22.

$$\Delta I_L = \frac{V_{OUT}}{F_{SW} \cdot L_F} \cdot \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \tag{21}$$

$$I_{L(peak)} = I_{OUT(max)} + \frac{\Delta I_L}{2} \tag{22}$$

For most applications, choose the inductance such that the inductor ripple current, $\Delta I_L$, is between 30% and 60% of the rated load current at nominal input voltage. Calculate the inductance using 公式 23.

$$L_F = \frac{V_{OUT}}{F_{SW} \cdot \Delta I_{L(nom)}} \cdot \left(1 - \frac{V_{OUT}}{V_{IN(nom)}}\right) \tag{23}$$

Choosing a 150-µH inductor in this design results in 295-mA peak-to-peak ripple current at nominal input voltage of 24 V, equivalent to 59% of the 500-mA rated load current. The peak inductor current at maximum input voltage of 65 V is 675 mA, which is sufficiently below the LM5166 peak current limit of 750 mA.

Check the inductor datasheet to ensure that the inductor saturation current is well above the current limit setting of a particular design. Ferrite designs have low core loss and are preferred at high switching frequencies, so design goals can then concentrate on copper loss and preventing saturation. However, ferrite core materials exhibit a hard saturation characteristic – the inductance collapses abruptly when the saturation current is exceeded. This results in an abrupt increase in inductor ripple current, higher output voltage ripple, not to mention reduced efficiency and compromised reliability. Note that inductor saturation current generally decreases as the core temperature increases.

#### 8.2.1.2.5 Output Capacitors – $C_{OUT}$

Select the output capacitor to limit the capacitive voltage ripple at the converter output. This is the sinusoidal ripple voltage that arises from the triangular ripple current flowing in the capacitor. Select an output capacitance using 公式 24 to limit the capacitive voltage ripple component to 0.5% of the output voltage.

$$C_{OUT} \geq \frac{\Delta I_{L(nom)}}{8 \cdot F_{SW} \cdot \Delta V_{OUT}} \tag{24}$$

Substituting $\Delta I_{L(nom)}$ of 295 mA and $\Delta V_{OUT}$ of 25 mV gives $C_{OUT}$ greater than 16 µF. Mindful of the voltage coefficient of ceramic capacitors, select a 47-µF, 10-V capacitor with a high-quality dielectric.

#### 8.2.1.2.6 Ripple Generation Network – $R_{ESR}$, $C_{FF}$

For this design, the Type 2 ripple generation method is selected as it offers a good balance between cost and output voltage ripple. For other methods, see *Ripple Generation Methods*.

Select a series resistor, $R_{ESR}$, such that sufficient ripple in phase with the inductor current ripple appears at the feedback node, FB, using 公式 7 and 公式 8. Select a feedforward capacitor, $C_{FF}$, using 公式 9.

With $\Delta I_{L(nom)}$ of 295 mA at the nominal input voltage of 24 V, the required $R_{ESR}$ is 0.11 Ω. The required feedforward capacitance, $C_{FF}$, is 100 pF. Calculate the total output voltage ripple in CCM using 公式 25.

$$\Delta V_{OUT} = \Delta I_{L(nom)} \cdot \sqrt{R_{ESR}^2 + \left(\frac{1}{8 \cdot F_{SW} \cdot C_{OUT}}\right)^2} \tag{25}$$

#### 8.2.1.2.7 Input Capacitor – $C_{IN}$

An input capacitor is necessary to limit the input ripple voltage while providing switching-frequency AC current to the buck power stage. To minimize the parasitic inductance in the switching loop, position the input capacitors as close as possible to the VIN and GND pins of the LM5166. The input capacitors conduct a trapezoidal-wave current of peak-to-peak amplitude equal to the output current. It follows that the resultant capacitive component of AC ripple voltage is a triangular waveform. Together with the ESR-related ripple component, the peak-to-peak input ripple voltage amplitude is given by 公式 26.

$$\Delta V_{IN} = \frac{I_{OUT} \cdot D \cdot (1-D)}{F_{SW} \cdot C_{IN}} + I_{OUT} \cdot R_{ESR} \tag{26}$$

The input capacitance required for a particular load current, based on an input voltage ripple specification of $\Delta V_{IN}$, is given by 公式 27.

$$C_{IN} \geq \frac{I_{OUT} \cdot D \cdot (1-D)}{F_{SW} \cdot (\Delta V_{IN} - I_{OUT} \cdot R_{ESR})} \tag{27}$$

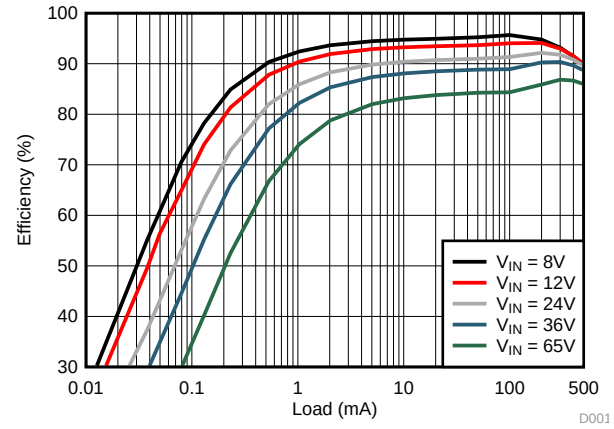
The recommended high-frequency input capacitance is 2.2 µF or higher and should be a high-quality ceramic component with sufficient voltage rating. Based on the voltage coefficient of ceramic capacitors, choose a voltage rating of twice the maximum input voltage. Additionally, some bulk capacitance is required if the LM5166 circuit is not located within approximately 5 cm from the input voltage source. This capacitor provides damping to the resonance associated with parasitic inductance of the supply lines and high-Q ceramics.

#### 8.2.1.2.8 Soft-Start Capacitor – $C_{SS}$

Connect an external soft-start capacitor for a specific soft-start time. In this example, select a soft-start capacitance of 33 nF based on 公式 18 to achieve a soft-start time of 4 ms.

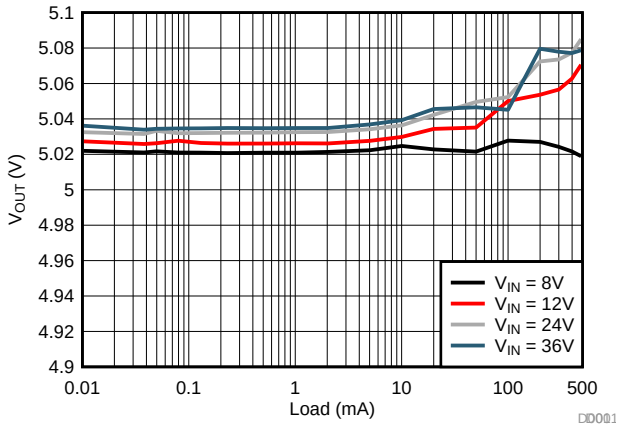
#### 8.2.1.2.9 Application Curves

Unless otherwise stated, application performance curves were taken at $T_A$ = 25°C.



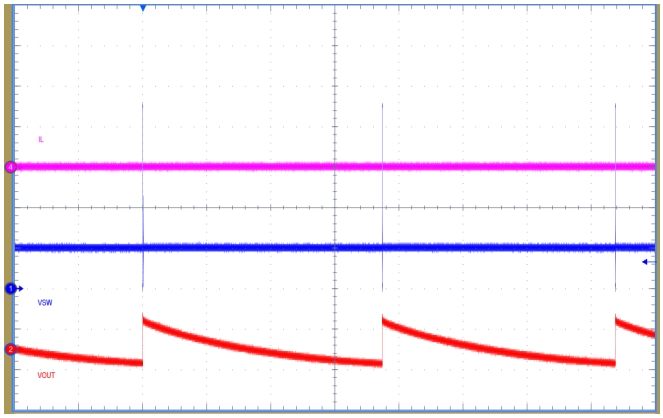

$L_F$ = 150 µH
$C_{OUT}$ = 47 µF
$F_{SW(nom)}$ = 100 kHz
$R_{RT}$ = 309 kΩ

**图 53. Converter Efficiency**



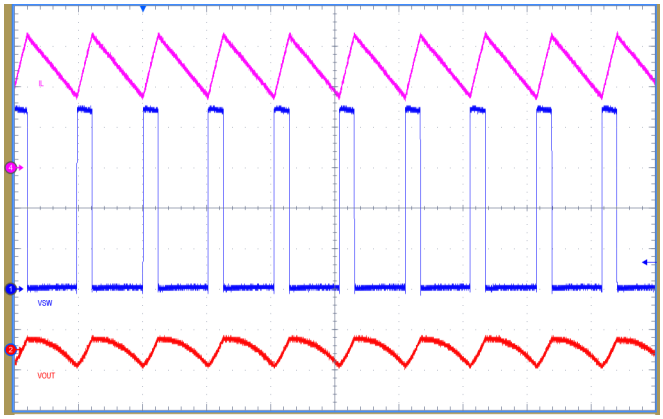

$L_F$ = 150 µH
$C_{OUT}$ = 47 µF
$F_{SW(nom)}$ = 100 kHz
$R_{RT}$ = 309 kΩ

**图 54. Converter Regulation**



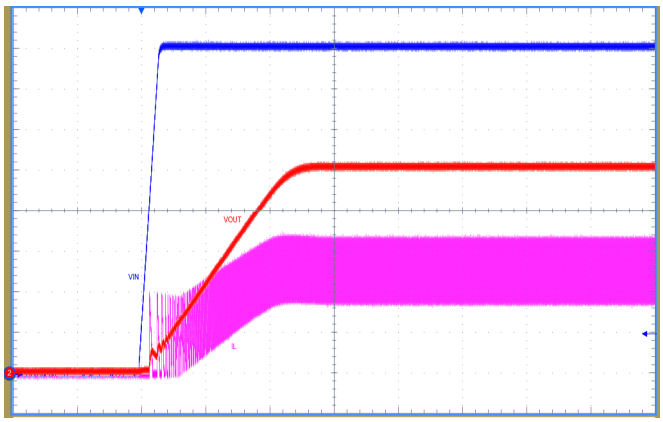

Time Scale: 20 ms/Div
CH1: $V_{SW}$, 5 V/Div
CH2: $V_{OUT}$, 50 mV/Div
CH4: $I_L$, 200 mA/Div

**图 55. No-Load Switching Waveforms, $V_{IN}$ = 24 V**



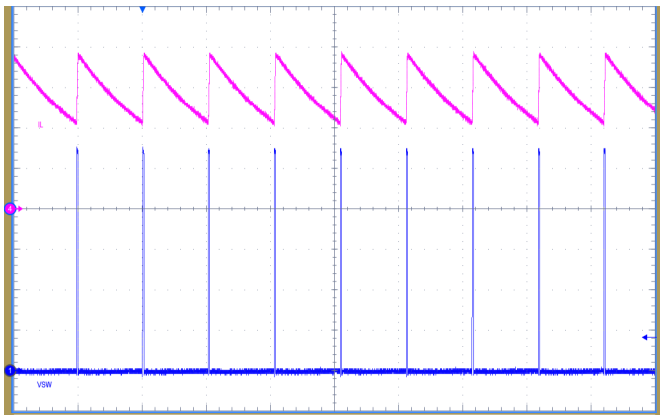

Time Scale: 10 µs/Div
CH1: $V_{SW}$, 5 V/Div
CH2: $V_{OUT}$, 50 mV/Div
CH4: $I_L$, 200 mA/Div

**图 56. Full-Load Switching Waveforms, $V_{IN}$ = 24 V**



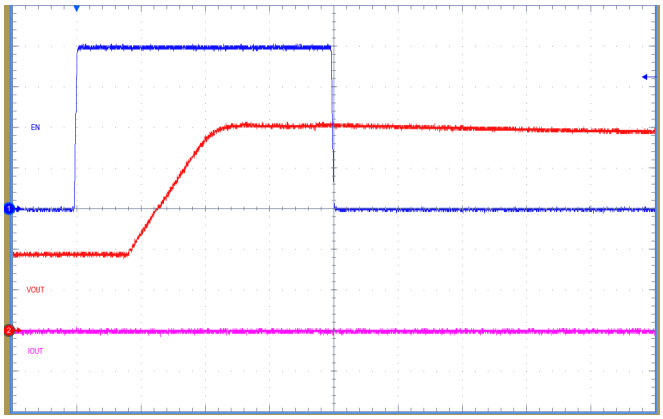

Time Scale: 2 ms/Div
CH1: $V_{IN}$, 3 V/Div
CH2: $V_{OUT}$, 1 V/Div
CH4: $I_L$, 200 mA/Div

**图 57. Full-Load Start-Up, $V_{IN}$ = 24 V**



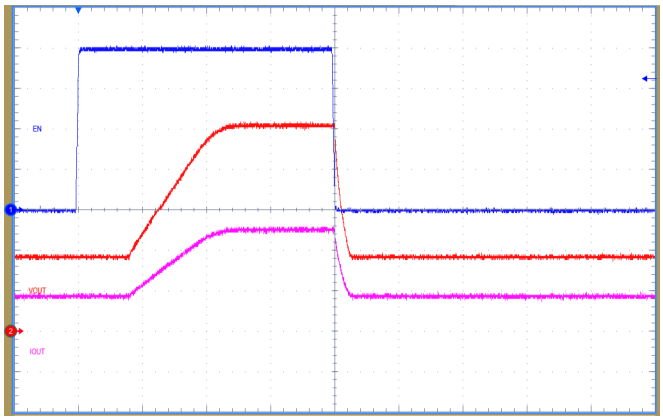

Time Scale: 100 µs/Div
CH1: $V_{SW}$, 4 V/Div
CH4: $I_L$, 200 mA/Div

**图 58. Short Circuit, $V_{IN}$ = 24 V**



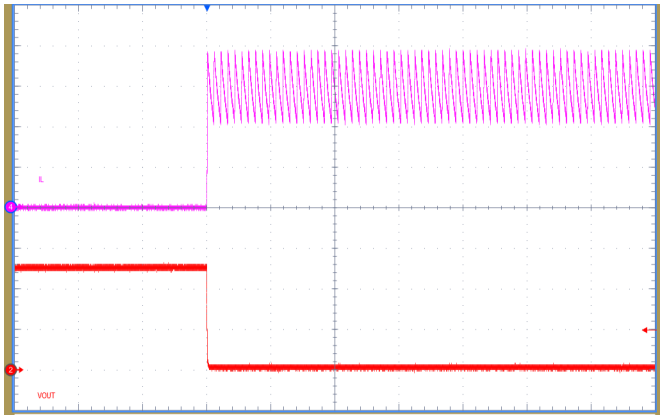

Time Scale: 2 ms/Div
CH1: $V_{EN}$, 1 V/Div
CH2: $V_{OUT}$, 1 V/Div
CH4: $I_{OUT}$, 200 mA/Div

**图 59. ENABLE On and Off; $V_{OUT}$ Prebiased to 1.8 V $V_{IN}$ = 24 V, No Load**



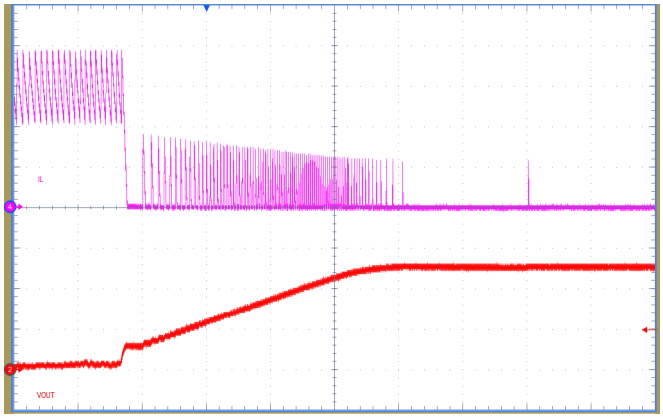

Time Scale: 2 ms/Div
CH1: $V_{EN}$, 5 V/Div
CH2: $V_{OUT}$, 1 V/Div
CH4: $I_{OUT}$, 200 mA/Div

**图 60. ENABLE On and Off; $V_{OUT}$ Prebiased to 1.8 V $V_{IN}$ = 24 V, 500 mA Load**




Time Scale: 1 ms/Div
CH2: $V_{OUT}$, 2 V/Div
CH4: $I_L$, 200 mA/Div

**图 61. Short-Circuit Entry**




Time Scale: 1 ms/Div
CH2: $V_{OUT}$, 2 V/Div
CH4: $I_L$, 200 mA/Div

**图 62. Short-Circuit Recovery**

### 8.2.2 Design 2: Wide $V_{IN}$, Low $I_Q$ COT Converter Rated at 3.3 V, 500 mA

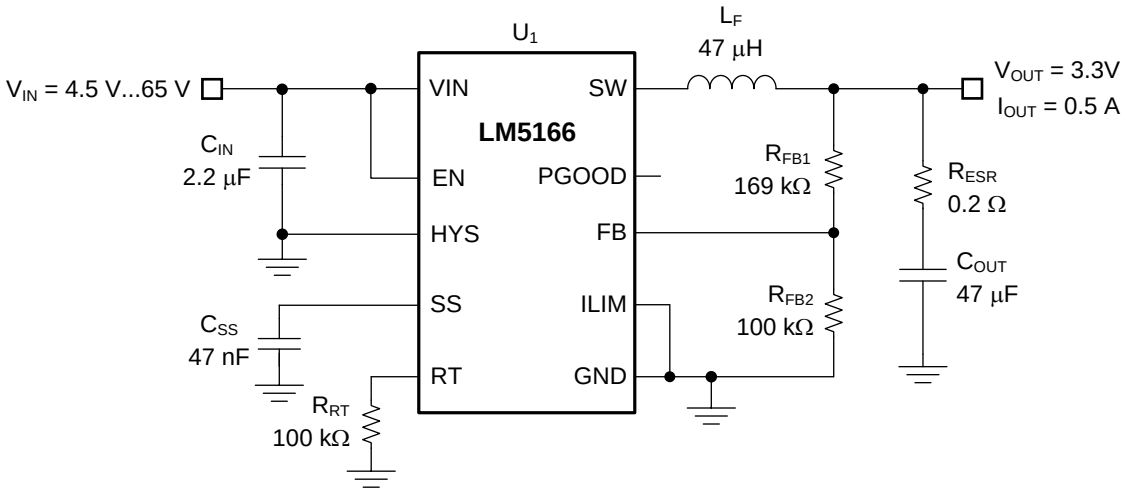





**图 63. Schematic for Design 2 With $V_{IN(nom)}$ = 12 V, $V_{OUT}$ = 3.3 V, $I_{OUT(max)}$ = 500 mA, $F_{SW(nom)}$ = 200 kHz**

#### *8.2.2.1 Design Requirements*

The target efficiency is 85% for loads above 10 mA based on a nominal input voltage of 12 V and an output voltage of 3.3 V. The required input voltage range is 4.5 V to 65 V. The LM5166 is chosen to deliver a 3.3-V output voltage. The switching frequency is set at 200 kHz. The output voltage soft-start time is 4 ms. The required components are listed in 表 5.

**表 5. List of Components for Design 2(1)**

| COUNT | REF DES | DESCRIPTION | PART NUMBER | MFR |
|---|---|---|---|---|
| 1 | $C_{IN}$ | Capacitor, Ceramic, 2.2 µF, 100 V, X7R, 10%, 1210 | GRM32ER72A225KA35L | Murata |
| 1 | $C_{OUT}$ | Capacitor, Ceramic, 47 µF, 10 V, X7R, 10%, 1210 | GRM32ER71A476KE15L | Murata |
| 1 | $C_{SS}$ | Capacitor, Ceramic, 47 nF, 16 V, X7R, 10%, 0402 | Std | Std |
| 1 | $L_F$ | Inductor, 47 µH, 0.245 Ω max, 1.2 A Isat, 3.5 mm max | LPS6235-473MR | Coilcraft |
| | | Inductor, 47 µH, 0.315 Ω typ, 1.3 A Isat, 2.8 mm max | 74404063470 | Würth |
| 1 | $R_{RT}$ | Resistor, Chip, 100 kΩ, 1/16W, 1%, 0402 | Std | Std |
| 1 | $R_{FB1}$ | Resistor, Chip, 169 kΩ, 1/16W, 1%, 0402 | Std | Std |
| 1 | $R_{ESR}$ | Resistor, Chip, 0.2 Ω, 1/16W, 1%, 0402 | Std | Std |
| 1 | $R_{FB2}$ | Resistor, Chip, 100 kΩ, 1/16W, 1%, 0402 | Std | Std |
| 1 | $U_1$ | LM5166, Synchronous Buck Converter, VSON-10, ADJ | LM5166DRCR | TI |

(1) See *第三方产品免责声明*.

#### *8.2.2.2 Detailed Design Procedure*

##### 8.2.2.2.1 Feedback Resistors – $R_{FB1}$, $R_{FB2}$

The output voltage of the LM5166 is externally adjustable using a resistor divider network. The divider network comprises the upper feedback resistor $R_{FB1}$ and lower feedback resistor $R_{FB2}$. Select $R_{FB1}$ of 169 kΩ to minimize quiescent current and improve light-load efficiency in this application. With the desired output voltage setpoint of 3.3 V and $V_{FB}$ = 1.223 V, calculate the resistance of $R_{FB2}$ using 公式 15 as 100.1 kΩ. Choose the closest available standard value of 100 kΩ for $R_{FB2}$. See *Adjustable Output Voltage (FB)* for more detail.

#### 8.2.2.2.2 Switching Frequency – $R_T$

The switching frequency of a COT-configured LM5166 is set by the on-time programming resistor at the RT pin. Using 公式 4, a standard 1% resistor of 100 kΩ gives a switching frequency of 190 kHz. Including the inductor $R_{DCR}$ and $R_{DSON2}$ in the calculation of $t_{OFF}$ (公式 3) gives an adjusted $F_{SW}$ of 215 kHz at 500 mA. The *LM5166 Quick-Start Design Tool* estimates and plots the switching frequency as a function of load current.

Note that at very low duty cycles, the minimum controllable on-time of the high-side MOSFET, $T_{ON(min)}$, of 180 ns may affect choice of switching frequency. In CCM, $T_{ON(min)}$ limits the voltage conversion step-down ratio for a given switching frequency. The minimum controllable duty cycle is given by 公式 19.

Given a fixed $T_{ON(min)}$, it follows that higher switching frequency implies a larger minimum controllable duty cycle. Ultimately, the choice of switching frequency for a given output voltage affects the available input voltage range, solution size, and efficiency. The maximum supply voltage for a given $T_{ON(min)}$ before switching frequency reduction occurs is given by 公式 20.

#### 8.2.2.2.3 Filter Inductance – $L_F$

The inductor ripple current (assuming CCM operation) and peak inductor current are given respectively by 公式 21 and 公式 22. For most applications, choose an inductance such that the inductor ripple current, $\Delta I_L$, is between 30% and 60% of the rated load current at nominal input voltage. Calculate the inductance using 公式 23.

Choosing a 47-µH inductor in this design results in 275-mA peak-to-peak ripple current at nominal input voltage of 12 V, equivalent to 55% of the 500-mA rated load current. The peak inductor current at maximum input voltage of 65 V is 694 mA, which is sufficiently below the LM5166 peak current limit of 750 mA.

#### 8.2.2.2.4 Output Capacitors – $C_{OUT}$

Select the output capacitor to limit the capacitive voltage ripple at the converter output. This is the sinusoidal ripple voltage that arises from the triangular ripple current flowing in the capacitor. Select an output capacitance using 公式 24 to limit the capacitive voltage ripple component to 0.5% of the output voltage.

Substituting $\Delta I_{L(nom)}$ of 275 mA and $\Delta V_{OUT}$ of 25 mV gives $C_{OUT}$ greater than 11 µF. Mindful of the voltage coefficient of ceramic capacitors, select a 47-µF, 10-V capacitor with a high-quality dielectric.

#### 8.2.2.2.5 Ripple Generation Network – $R_{ESR}$

For this design, the Type 1 ripple generation method is selected as it only requires a single external component. For other schemes, see *Ripple Generation Methods*.

Select a series resistor, $R_{ESR}$, using 公式 5 and 公式 6 such that sufficient ripple in phase with the SW node voltage appears at the feedback node, FB. With $\Delta I_{L(nom)}$ of 275 mA at the nominal input voltage of 12 V, the required $R_{ESR}$ is 0.2 Ω. Calculate the total output voltage ripple in CCM using 公式 25.

#### 8.2.2.2.6 Input Capacitor – $C_{IN}$

An input capacitor is necessary to limit the input ripple voltage while providing switching-frequency AC current to the buck power stage. To minimize the parasitic inductance in the switching loop, position the input capacitors as close as possible to the VIN and GND pins of the LM5166. The input capacitors conduct a trapezoidal-wave current of peak-to-peak amplitude equal to the output current. It follows that the resultant capacitive component of AC ripple voltage is a triangular waveform. Together with the ESR-related ripple component, the peak-to-peak input ripple voltage amplitude is given by 公式 26. The input capacitance required for a particular load current, based on an input voltage ripple specification of $\Delta V_{IN}$, is given by 公式 27.

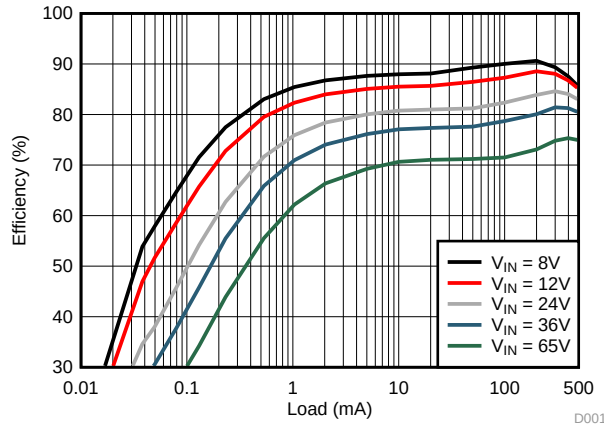
The recommended high-frequency capacitance is 2.2 µF or higher and should be a high-quality ceramic with sufficient voltage rating. Based on the voltage coefficient of ceramic capacitors, choose a voltage rating of twice the maximum input voltage. Additionally, some bulk capacitance is required if the LM5166 circuit is not located within approximately 5 cm from the input voltage source. This capacitor provides damping to the resonance associated with parasitic inductance of the supply lines and high-Q ceramics.

#### 8.2.2.2.7 Soft-Start Capacitor – $C_{SS}$

Connect an external soft-start capacitor for a specific soft-start time. In this example, select a soft-start capacitance of 47 nF based on 公式 18 to achieve a soft-start time of 6 ms.

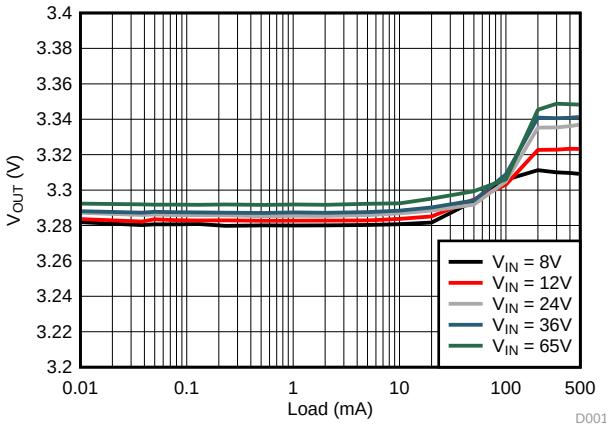
#### 8.2.2.2.8 Application Curves

Unless otherwise stated, application curves were taken at $T_A$ = 25°C.



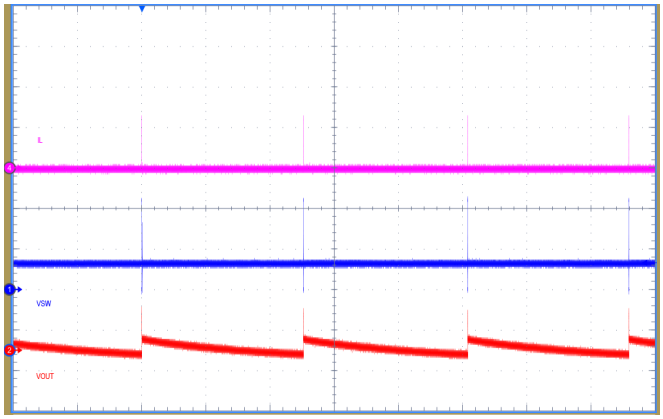

$L_F$ = 47 µH
$C_{OUT}$ = 47 µF
$F_{SW(nom)}$ = 200 kHz
$R_{RT}$ = 100 kΩ

**图 64. Converter Efficiency**



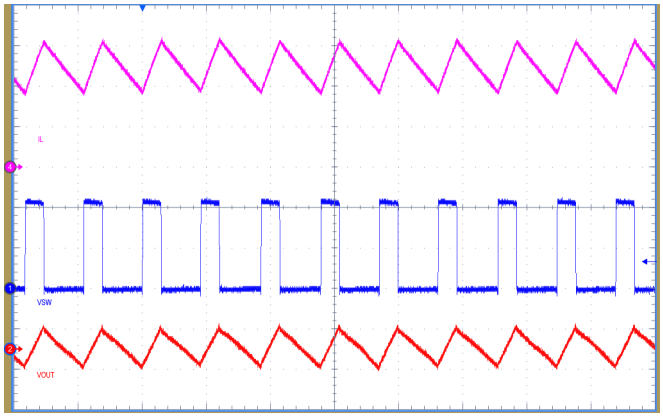

$L_F$ = 47 µH
$C_{OUT}$ = 47 µF
$F_{SW(nom)}$ = 200 kHz
$R_{RT}$ = 100 kΩ

**图 65. Converter Regulation**



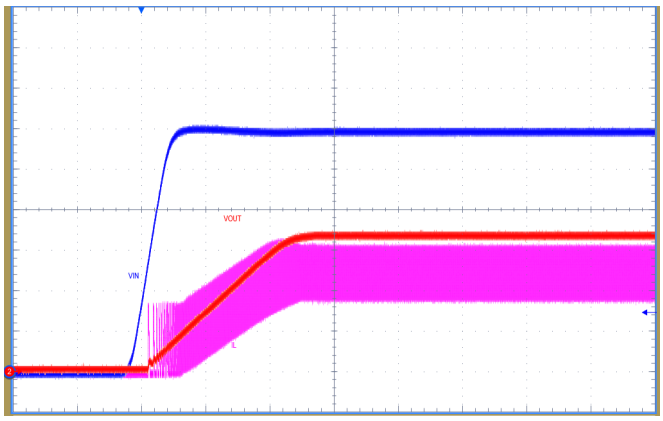
Time Scale: 20 ms/Div
CH1: $V_{SW}$, 5 V/Div
CH2: $V_{OUT}$, 50 mV/Div
CH4: $I_L$, 200 mA/Div

**图 66. No-Load Switching Waveforms**



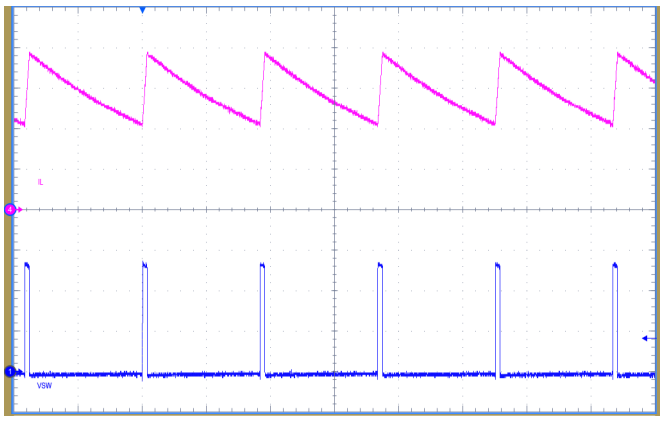
Time Scale: 5 µs/Div
CH1: $V_{SW}$, 5 V/Div
CH2: $V_{OUT}$, 50 mV/Div
CH4: $I_L$, 200 mA/Div

**图 67. Full-Load Switching Waveforms**



Time Scale: 2 ms/Div
CH1: $V_{IN}$, 2 V/Div
CH2: $V_{OUT}$, 1 V/Div
CH4: $I_L$, 200 mA/Div

**图 68. Full-Load Start-Up**



Time Scale: 100 µs/Div
CH1: $V_{SW}$, 4 V/Div
CH4: $I_L$, 200 mA/Div

**图 69. Short Circuit**

### 8.2.3 Design 3: High-Density PFM Converter Rated at 3.3 V, 0.3 A

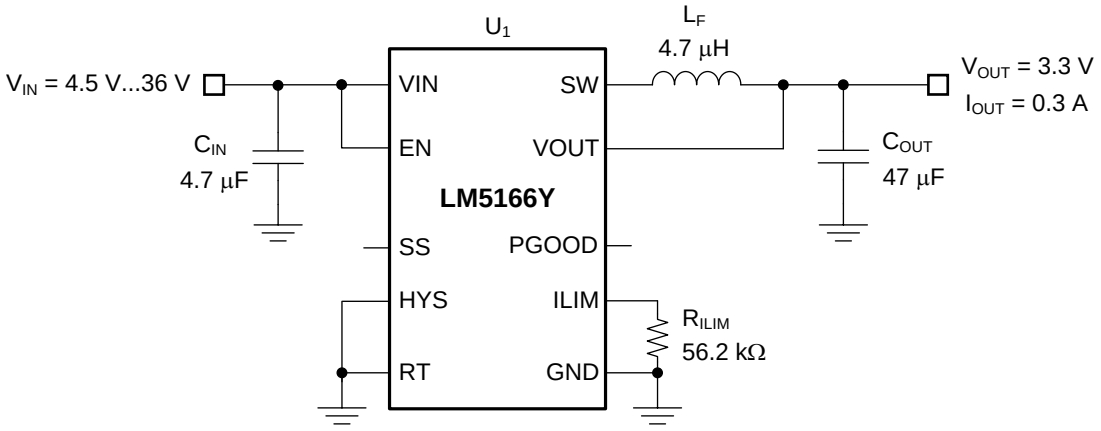





**图 70. Schematic for Design 3 With $V_{IN(nom)}$ = 24 V, $V_{OUT}$ = 3.3 V, $I_{OUT(max)}$ = 0.3 A, $F_{SW(nom)}$ = 600 kHz**

#### *8.2.3.1 Design Requirements*

The target efficiency is 75% for loads above 10 mA based on a nominal input voltage of 24 V, an output voltage of 3.3 V, with the emphasis on small solution size. The required input voltage range is 4.5 V to 36 V. The LM5166 has an internally-set soft-start time of 900 µs and an adjustable peak current limit threshold. The required components are listed in 表 6.

**表 6. List of Components for Design 3(1)**

| COUNT | REF DES | DESCRIPTION | PART NUMBER | MFR |
|---|---|---|---|---|
| 1 | $C_{IN}$ | Capacitor, Ceramic, 4.7 µF, 50 V, X7R, 10%, 1206 | GRM31CR71H475MA12L | Murata |
| | | | 885012208094 | Würth |
| 1 | $C_{OUT}$ | Capacitor, Ceramic, 47 µF, 6.3 V, X5R, 10%, 1206 | GRM31CR60J476KE19 | Murata |
| 1 | $L_F$ | Inductor, 4.7 µH, 0.18 Ω typ, 2.2 A Isat, 1.2 mm max | TFM252012ALMA4R7TMAA | TDK |
| | | Inductor, 4.7 µH, 0.3 Ω typ, 2.1 A Isat, 1.2 mm max | Würth | Würth |
| 1 | $R_{ILIM}$ | Resistor, Chip, 56.2 kΩ, 1/16W, 1%, 0402 | Std | Std |
| 1 | $U_1$ | LM5166Y, Synchronous Buck Converter, VSON-10, 3.3-V Fixed | LM5166YDRCR | TI |

(1) See *第三方产品免责声明*.

#### *8.2.3.2 Detailed Design Procedure*

##### 8.2.3.2.1 Peak Current Limit Setting – $R_{ILIM}$

Install a 56.2-kΩ resistor from ILIM to GND to select a 750-mA peak current limit threshold setting to meet the rated output current of 300 mA in PFM. See *Adjustable Current Limit* for more detail.

##### 8.2.3.2.2 Switching Frequency – $L_F$

Tie RT to GND to select PFM mode of operation. The inductor, input voltage, output voltage and peak current determine the pulse switching frequency of a PFM-configured LM5166. For a given input voltage, output voltage and peak current, the inductance of $L_F$ sets the switching frequency when the output is in regulation. Use 公式 28 to select an inductance of 4.7 µH based on the target PFM converter switching frequency of 600 kHz at 24-V input.

$$L_F = \frac{V_{OUT}}{F_{SW(PFM)} \cdot I_{PK(PFM)}} \cdot \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \quad (28)$$

$I_{PK(PFM)}$ in this example is the peak current limit setting of 750 mA plus the inductor current overshoot resulting from the 80-ns peak current comparator delay, $t_{ILIM\_delay}$. An additional constraint on the inductance is the 180-ns minimum on-time of the high-side MOSFET. Therefore, to keep the inductor current well controlled, choose an inductance that is larger than $L_{F(min)}$ using 公式 29 where $V_{IN(max)}$ is the maximum input supply voltage for the application, $t_{ILIM\_delay}$ is 80 ns, $t_{ON(min)}$ is 180 ns, the maximum current limit threshold, $I_{LIM(max)}$, is 825 mA, and the maximum allowed peak inductor current, $I_{L(max)}$, is 1.6 A.

$$L_{F(min)} = Max\left(\frac{V_{IN(max)} \cdot t_{ON(min)}}{I_{L(max)}}, \frac{V_{IN(max)} \cdot t_{ILIM\_delay}}{I_{L(max)} - I_{LIM(max)}}\right) \quad (29)$$

Choose an inductor with saturation current rating above the peak current limit setting, and allow for derating of the saturation current at the highest expected operating temperature.

#### 8.2.3.2.3 Output Capacitors – $C_{OUT}$

The output capacitor, $C_{OUT}$, filters the inductor's ripple current and stores energy to meet the load current requirement when the LM5166 is in sleep mode. The output ripple has a base component of amplitude $V_{OUT}/123$ related to the typical feedback comparator hysteresis in PFM. The wake-up time from sleep to active mode adds a ripple voltage component that is a function of the output current. Approximate the total output ripple by 公式 30.

$$\Delta V_{OUT} = \left(\frac{I_{PK(PFM)}}{2} + I_{OUT}\right) \cdot \frac{1\mu s}{C_{OUT}} + \frac{V_{OUT}}{123} \quad (30)$$

Also, the output capacitance must be large enough to accept the energy stored in the inductor without a large deviation in output voltage. Setting this voltage change equal to 1% of the output voltage results in a $C_{OUT}$ requirement defined with 公式 31.

$$C_{OUT} \geq 50 \cdot L_F \cdot \left(\frac{I_{PK(PFM)}}{V_{OUT}}\right)^2 \quad (31)$$

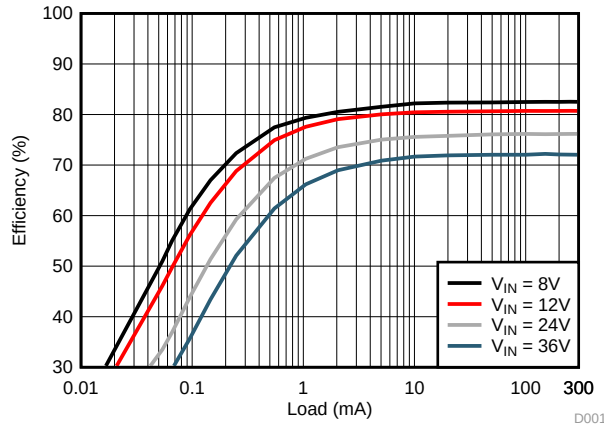
In general, select the capacitance of $C_{OUT}$ to limit the output voltage ripple at full load current, ensuring that it is rated for worst-case RMS ripple current given by $I_{RMS} = I_{PK(PFM)}/2$. In this design example, select a 47-µF, 6.3-V capacitor with a high-quality dielectric.

#### 8.2.3.2.4 Input Capacitor – $C_{IN}$

The input capacitor, $C_{IN}$, filters the triangular current waveform of the high-side MOSFET (see 图 89). To prevent large ripple voltage, use a low-ESR ceramic input capacitor sized for the worst-case RMS ripple current given by $I_{RMS} = I_{OUT}/2$. In this design example, choose a 2.2-µF, 50-V ceramic input capacitor with a high-quality dielectric.

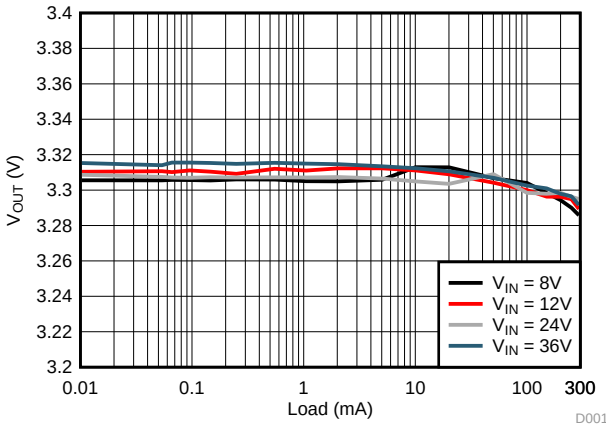
#### 8.2.3.2.5 Application Curves

Unless otherwise stated, application curves were taken at $T_A$ = 25°C.



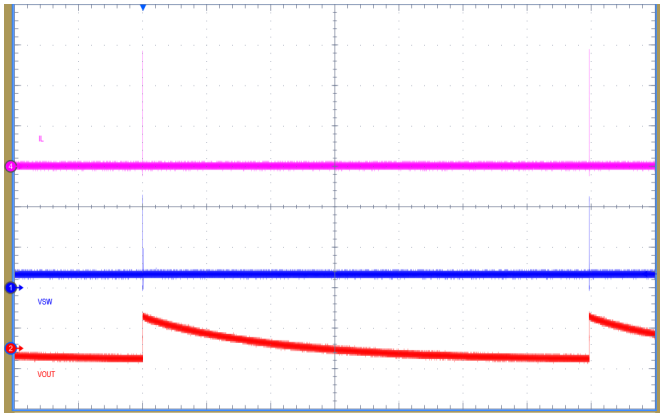

$L_F$ = 4.7 µH
$C_{OUT}$ = 47 µF
$F_{SW(nom)}$ = 600 kHz
$R_{RT}$ = 0 Ω

**图 71. Converter Efficiency**



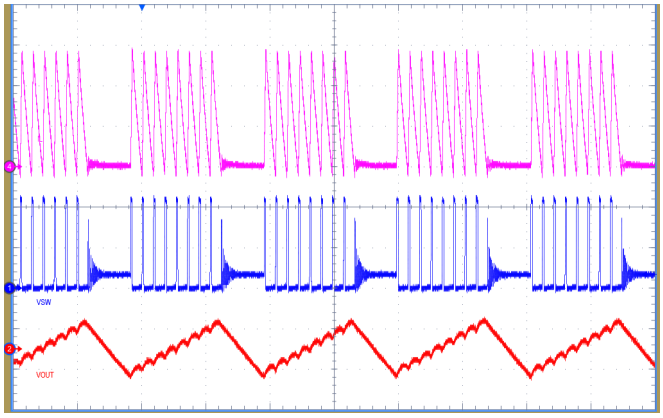

$L_F$ = 4.7 µH
$C_{OUT}$ = 47 µF
$F_{SW(nom)}$ = 600 kHz
$R_{RT}$ = 0 Ω

**图 72. Converter Regulation**



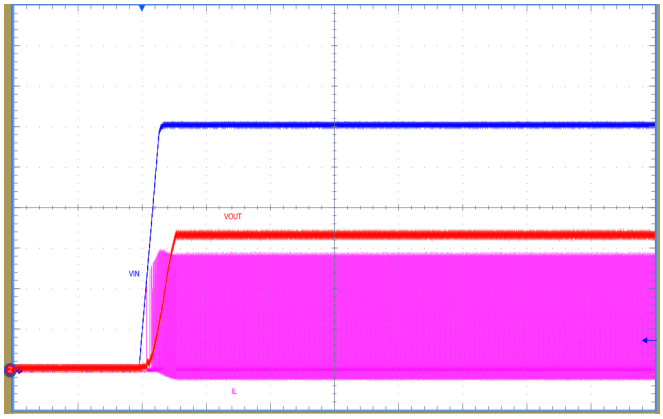

Time Scale: 20 ms/Div
CH1: $V_{SW}$, 10 V/Div
CH2: $V_{OUT}$, 50 mV/Div
CH4: $I_L$, 400 mA/Div

**图 73. No-Load Switching Waveforms, $V_{IN}$ = 24 V**



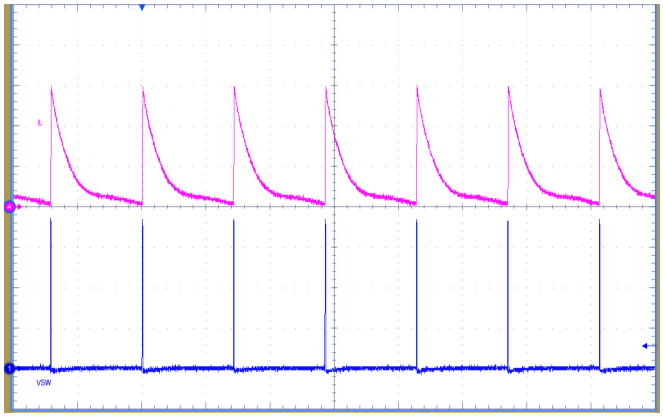

Time Scale: 10 µs/Div
CH1: $V_{SW}$, 10 V/Div
CH2: $V_{OUT}$, 50 mV/Div
CH4: $I_L$, 400 mA/Div

**图 74. Full-Load Switching Waveforms, $V_{IN}$ = 24 V**




Time Scale: 2 ms/Div
CH1: $V_{IN}$, 4 V/Div
CH2: $V_{OUT}$, 1 V/Div
CH4: $I_L$, 400 mA/Div

**图 75. Full-Load Start-Up, $V_{IN}$ = 24 V**




Time Scale: 20 µs/Div
CH1: $V_{SW}$, 6 V/Div
CH4: $I_L$, 400 mA/Div

**图 76. Short Circuit, $V_{IN}$ = 24 V**

### 8.2.4 Design 4: Wide $V_{IN}$, Low $I_Q$ PFM Converter Rated at 5 V, 500 mA

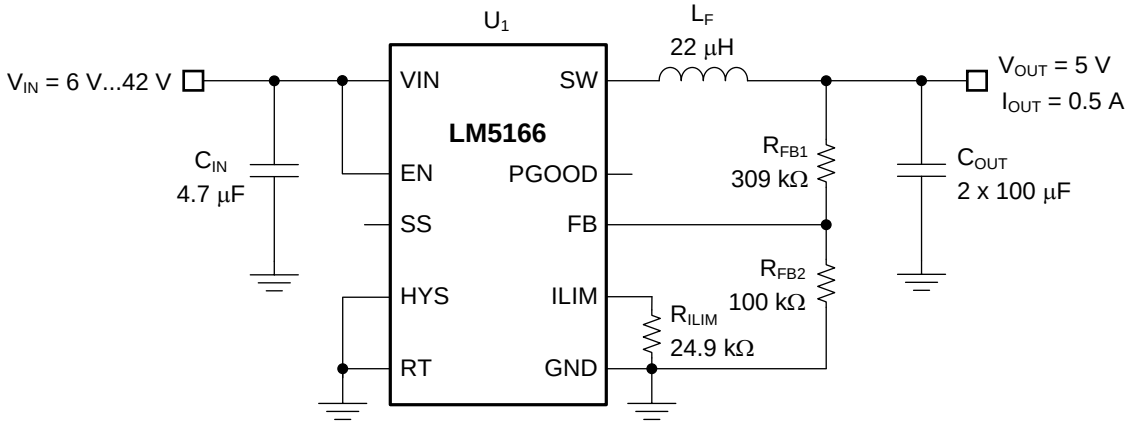





**图 77. Schematic for Design 4 With $V_{IN(nom)}$ = 12 V, $V_{OUT}$ = 5 V, $I_{OUT(max)}$ = 500 mA, $F_{SW(nom)}$ = 100 kHz**

#### *8.2.4.1 Design Requirements*

The target efficiency is 85% for loads above 1 mA based on a nominal input voltage of 12 V, an output voltage of 5 V. The required input voltage range is 6 V to 42 V. The LM5166 has an internally-set soft-start time of 900 µs and an adjustable peak current limit threshold. The required components are listed in 表 7.

**表 7. List of Components for Design 4(1)**

| COUNT | REF DES | DESCRIPTION | PART NUMBER | MFR |
|---|---|---|---|---|
| 1 | $C_{IN}$ | Capacitor, Ceramic, 4.7 µF, 50 V, X7R, 20%, 1206 | GRM31CR71H475MA12L | Murata |
| | | | C3216X7R1H475M160AC | TDK |
| 2 | $C_{OUT}$ | Capacitor, Ceramic, 100 µF, 10 V, X5R, 10%, 1210 | GRM32ER61A107ME20K | Murata |
| 1 | $L_F$ | Inductor, 22 µH, 0.145 Ω max, 1.7 A Isat, 3.5 mm max | LPS6235-223MR | Coilcraft |
| | | Inductor, 22 µH, 0.2 Ω max, 2.3 A Isat, 3 mm max | CMLB063T-220MS | Cyntec |
| 1 | $R_{ILIM}$ | Resistor, Chip, 24.9 kΩ, 1/16W, 1%, 0402 | Std | Std |
| 1 | $R_{FB1}$ | Resistor, Chip, 309 kΩ, 1/16W, 1%, 0402 | Std | Std |
| 1 | $R_{FB2}$ | Resistor, Chip, 100 kΩ, 1/16W, 1%, 0402 | Std | Std |
| 1 | $U_1$ | LM5166, Synchronous Buck Converter, VSON-10, ADJ | LM5166DRCR | TI |

(1) See *第三方产品免责声明*.

#### *8.2.4.2 Detailed Design Procedure*

##### 8.2.4.2.1 Feedback Resistors – $R_{FB1}$, $R_{FB2}$

The output voltage of the LM5166 is externally adjustable using a resistor divider network. The divider network comprises the upper feedback resistor $R_{FB1}$ and lower feedback resistor $R_{FB2}$. Select $R_{FB1}$ of 309 kΩ to minimize quiescent current and improve light-load efficiency in this application. With the desired output voltage setpoint of 5 V and $V_{FB}$ = 1.223 V, calculate the resistance of $R_{FB2}$ using 公式 15 as 99.5 kΩ. Choose the closest available standard value of 100 kΩ for $R_{FB2}$. See *Adjustable Output Voltage (FB)* for more detail.

##### 8.2.4.2.2 Peak Current Limit Setting – $R_{ILIM}$

Install a 24.9-kΩ resistor from ILIM to GND to select a 1.25-A peak current limit threshold setting with modulated ILIM function to meet the rated output current of 500 mA and the efficiency target. See *Adjustable Current Limit* for more detail.

#### 8.2.4.2.3 Switching Frequency – $L_F$

Tie RT to GND to select PFM mode of operation. The inductor, input voltage, output voltage and peak current determine the pulse switching frequency of a PFM-configured LM5166. For a given input voltage, output voltage and peak current, the inductance of $L_F$ sets the switching frequency when the output is in regulation. Use 公式 28 to select an inductance of 22 µH based on the target PFM converter switching frequency of 100 kHz at 12-V input.

$I_{PK(PFM)}$ in this example is the peak current limit setting of 1.25 A plus the inductor current overshoot resulting from the 80-ns peak current comparator delay. An additional constraint on the inductance is the 180-ns minimum on-time of the high-side MOSFET. Therefore, to keep the inductor current well controlled, choose an inductance that is larger than $L_{F(min)}$ using 公式 29.

Choose an inductor with saturation current rating above the peak current limit setting, and allow for derating of the saturation current at the highest expected operating temperature.

#### 8.2.4.2.4 Output Capacitors – $C_{OUT}$

The output capacitor, $C_{OUT}$, filters the ripple current of the inductor and stores energy to meet the load current requirement when the LM5166 is in sleep mode. The output ripple has a base component of amplitude $V_{OUT}/123$ related to the typical feedback comparator hysteresis in PFM. The wake-up time from sleep to active mode adds a ripple voltage component that is a function of the output current. Approximate the total output ripple by 公式 30.

Also, the output capacitance must be large enough to accept the energy stored in the inductor without a large deviation in output voltage. Setting this voltage change equal to 1% of the output voltage results in a $C_{OUT}$ requirement defined with 公式 31.

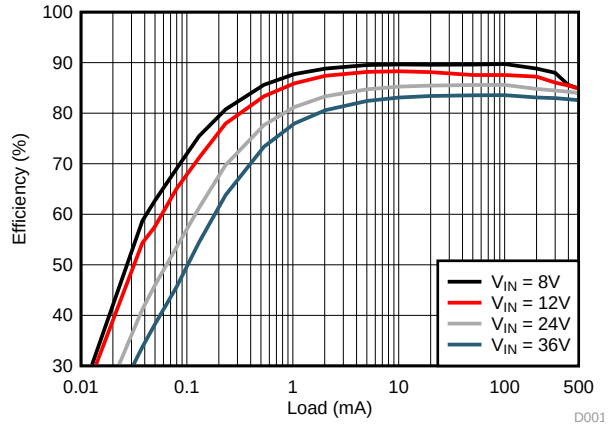
In general, select the capacitance of $C_{OUT}$ to limit the output voltage ripple at full load current, ensuring that it is rated for worst-case RMS ripple current given by $I_{RMS} = I_{PK(PFM)}/2$. In this design example, select two 100-µF, 10-V capacitors with a high-quality dielectric.

#### 8.2.4.2.5 Input Capacitor – $C_{IN}$

The input capacitor, $C_{IN}$, filters the triangular current waveform of the high-side MOSFET (see 图 89). To prevent large ripple voltage, use a low-ESR ceramic input capacitor sized for the worst-case RMS ripple current given by $I_{RMS} = I_{OUT}/2$. In this design example, choose a 4.7-µF, 50-V ceramic input capacitor with a high-quality dielectric.

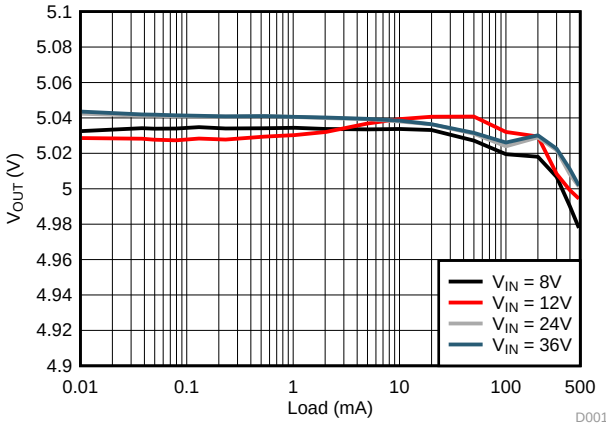
### 8.2.4.3 Application Curves

Unless otherwise stated, application curves were taken at $T_A$ = 25°C.



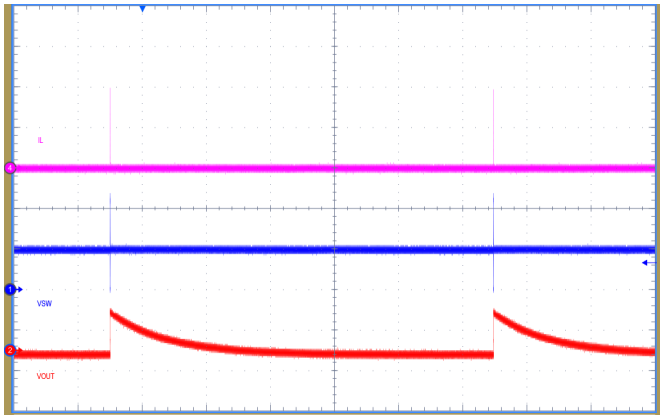

$L_F$ = 22 µH
$C_{OUT}$ = 200 µF
$F_{SW(nom)}$ = 100 kHz
$R_{RT}$ = 0 Ω

**图 78. Converter Efficiency**



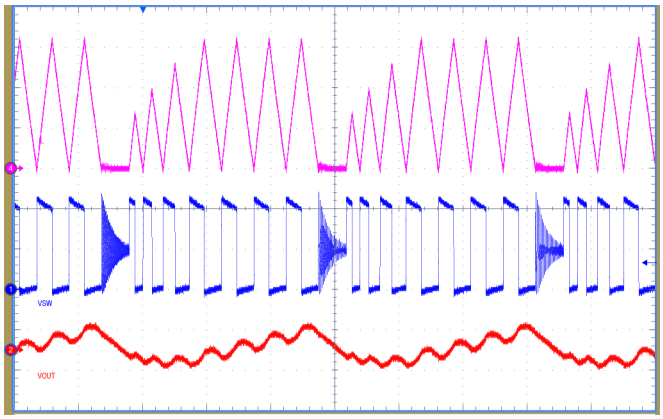

$L_F$ = 22 µH
$C_{OUT}$ = 200 µF
$F_{SW(nom)}$ = 100 kHz
$R_{RT}$ = 0 Ω

**图 79. Converter Regulation**



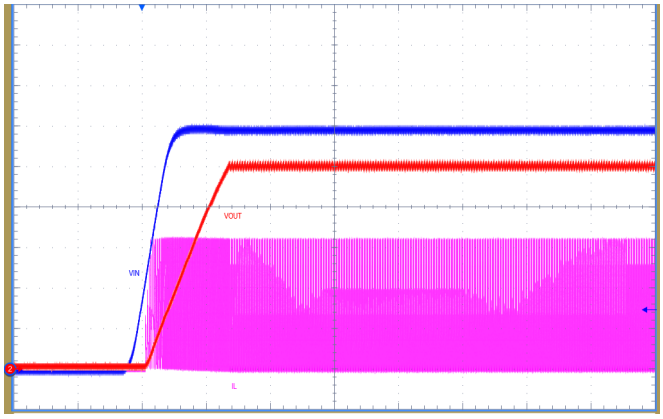
Time Scale: 50 ms/Div
CH1: $V_{SW}$, 5 V/Div
CH2: $V_{OUT}$, 50 mV/Div
CH4: $I_L$, 0.4 A/Div

**图 80. No-Load Switching Waveforms**



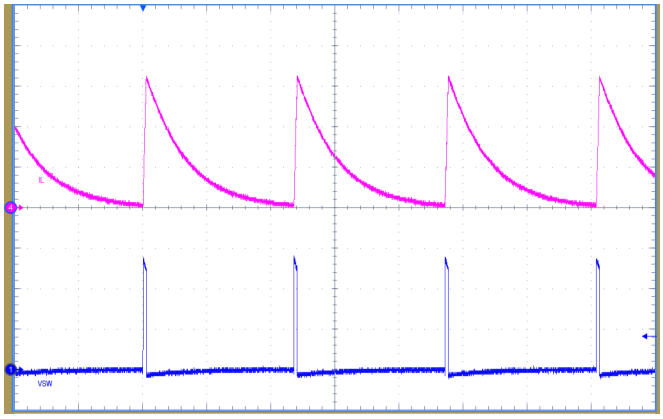
Time Scale: 20 µs/Div
CH1: $V_{SW}$, 5 V/Div
CH2: $V_{OUT}$, 100 mV/Div
CH4: $I_L$, 0.4 A/Div

**图 81. Full-Load Switching Waveforms**



Time Scale: 2 ms/Div
CH1: $V_{IN}$, 2 V/Div
CH2: $V_{OUT}$, 1 V/Div
CH4: $I_L$, 0.4 A/Div

**图 82. Full-Load Start-Up**



Time Scale: 50 µs/Div
CH1: $V_{SW}$, 4 V/Div
CH4: $I_L$, 0.4 A/Div

**图 83. Short Circuit**

### 8.2.5 Design 5: 12-V, 300-mA COT Converter Operating From 24-V or 48-V Input

The schematic diagram of 12-V, 300-mA COT converter is given in 图 84.

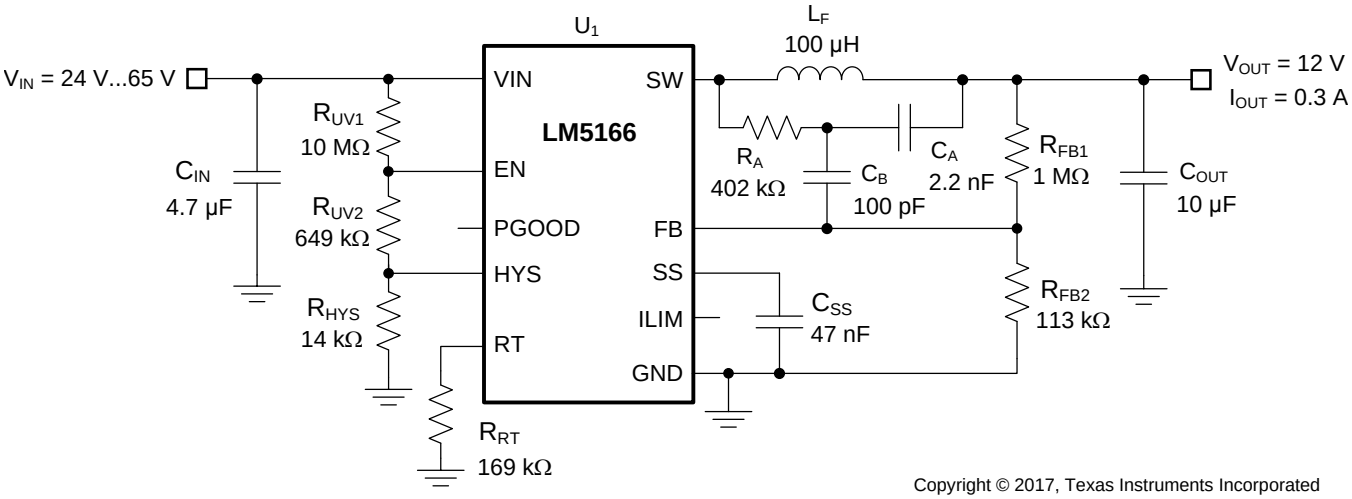



**图 84. Schematic for Design 5 With $V_{OUT}$ = 12 V, $I_{OUT(max)}$ = 300 mA, $F_{SW(nom)}$ = 400 kHz**

#### *8.2.5.1 Design Requirements*

The full-load efficiency specifications are 93% and 89% based on input voltages of 24 V and 48 V, respectively, and an output voltage setpoint of 12 V. The input voltage range is 24 V to 65 V, with UVLO turnon and turnoff at 20 V and 18 V, respectively. The output voltage setpoint is established by feedback resistors, $R_{FB1}$ and $R_{FB2}$. The required components are listed in 表 8.

**表 8. List of Components for Design 5(1)**

| REF DES | QTY | SPECIFICATION | VENDOR | PART NUMBER |
|---|---|---|---|---|
| $C_{IN}$ | 1 | 4.7 µF, 100 V, X7S, 1210 | Murata | GRM31CR71H475MA12L |
| | | 4.7 µF, 80 V, X7R, 1210 | Murata | GRM32ER71K475KE14L |
| $C_{OUT}$ | 1 | 10 µF, 25 V, X7R, 1206 | Murata | GRM31CR71E106MA12L |
| | | | TDK | C3216X7R1E106M |
| | | | Würth | 885012208069 |
| $L_F$ | 1 | 100 µH ±20%, 0.54 A, 375 mΩ maximum DCR, 6 × 6 × 3.5 mm | Coilcraft | LPS6235-104MRC |
| $R_A$ | 1 | 402 kΩ, 1%, 0402 | Std | Std |
| $R_{FB1}$ | 1 | 1 MΩ, 1%, 0402 | Std | Std |
| $R_{FB2}$ | 1 | 113 kΩ, 1%, 0402 | Std | Std |
| $R_{UV1}$ | 1 | 10 MΩ, 1%, 0603 | Std | Std |
| $R_{UV2}$ | 1 | 649 kΩ, 1%, 0402 | Std | Std |
| $R_{HYS}$ | 1 | 14 kΩ, 1%, 0402 | Std | Std |
| $R_{RT}$ | 1 | 169 kΩ, 1%, 0402 | Std | Std |
| $C_A$ | 1 | 2.2 nF, 25 V, X7R, 0402 | Std | Std |
| $C_B$ | 1 | 100 pF, 50 V, NP0, 0402 | Std | Std |
| $C_{SS}$ | 1 | 47 nF, 16 V, X7R, 0402 | Std | Std |
| $U_1$ | 1 | LM5166 Synchronous Buck Converter, VSON-10, 3 mm × 3 mm | TI | LM5166DRCR |

(1) See *第三方产品免责声明*.

### 8.2.5.2 Detailed Design Procedure

The component selection procedure for this design is quite similar to that of COT designs 1 and 2.

#### 8.2.5.2.1 Peak Current Limit Setting – $R_{ILIM}$

Leave the ILIM pin open circuit to select the 500-mA peak current limit setting for a rated output current of 300 mA. See 表 3.

#### 8.2.5.2.2 Switching Frequency – $R_{RT}$

Using 公式 4, select a standard 1% resistor value of 169 kΩ to set a switching frequency of 400 kHz.

#### 8.2.5.2.3 Inductor – $L_F$

Choosing a 100-µH inductor in this design results in 150-mA peak-to-peak ripple current at an input voltage of 24 V, equivalent to 50% of the 300-mA rated load current. A larger ripple current design results in improved light-load efficiency. The peak inductor current at maximum input voltage of 65 V is 424 mA, which is sufficiently below the LM5166 peak current limit of 500 mA. Select an inductor with saturation current rating well above the peak current limit setting, and allow for derating of the saturation current at the highest expected operating temperature.

#### 8.2.5.2.4 Input and Output Capacitors – $C_{IN}$, $C_{OUT}$

Choose a 4.7-µF, 80-V or 100-V ceramic input capacitor with 1210 footprint. Such a capacitor is typically available in X7S or X7R dielectric. Based on 公式 24, select a 10-µF, 25-V ceramic output capacitor with X7R dielectric and 1206 footprint.

#### 8.2.5.2.5 Feedback Resistors – $R_{FB1}$, $R_{FB2}$

Select $R_{FB1}$ of 1 MΩ to minimize quiescent current and improve light-load efficiency in this application. With the desired output voltage setpoint of 12 V and $V_{FB}$ = 1.223 V, calculate the resistance of $R_{FB2}$ using 公式 15 as 113.5 kΩ. Choose the closest available standard value of 113 kΩ for $R_{FB2}$. See *Adjustable Output Voltage (FB)* for more detail.

#### 8.2.5.2.6 Ripple Generation Network – $R_A$, $C_A$, $C_B$

Select the ripple injection circuit components $R_A$ and $C_A$ values using 公式 10 and 公式 11. Choose capacitor $C_B$ using 公式 12 based on a target transient response settling time of 300 µs.

#### 8.2.5.2.7 Undervoltage Lockout Setpoint – $R_{UV1}$, $R_{UV2}$, $R_{HYS}$

Adjust the undervoltage lockout (UVLO) using an externally-connected resistor divider network of $R_{UV1}$, $R_{UV2}$, and $R_{HYS}$. The UVLO has two thresholds, one for power up when the input voltage is rising and one for power down or brownouts when the input voltage is falling. The EN rising threshold for the LM5166 is 1.22 V.

Rearranging 公式 16 and 公式 17, the expressions to calculate $R_{UV2}$ and $R_{HYS}$ are as follows:

$$R_{UV2} = \frac{V_{EN(on)}}{V_{IN(on)} - V_{EN(on)}} \cdot R_{UV1} \tag{32}$$

$$R_{HYS} = \frac{V_{EN(off)}}{V_{IN(off)} - V_{EN(off)}} \cdot R_{UV1} - R_{UV2} \tag{33}$$

Choose $R_{UV1}$ as 10 MΩ to minimize input quiescent current. Given the desired input voltage UVLO thresholds of 20 V and 18 V, calculate the resistance of $R_{UV2}$ and $R_{HYS}$ as 649 kΩ and 14 kΩ, respectively. See *Precision Enable (EN) and Hysteresis (HYS)* for more detail.

#### 8.2.5.2.8 Soft Start – $C_{SS}$

Install a 47-nF capacitor from SS to GND for a soft-start time of 6 ms.

### 8.2.5.3 Application Curves

Unless otherwise stated, application curves were taken at $T_A$ = 25°C.

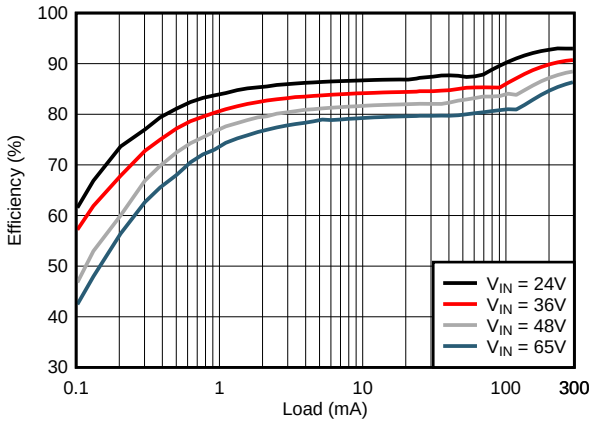
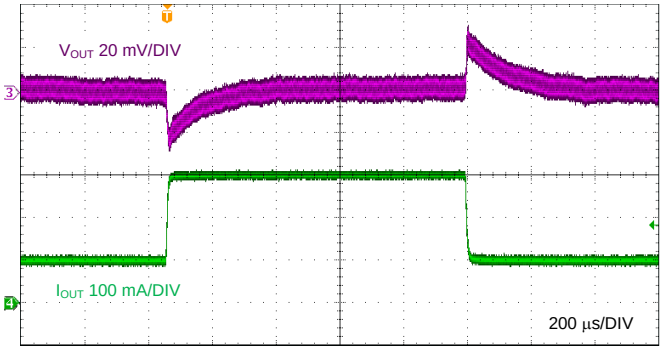
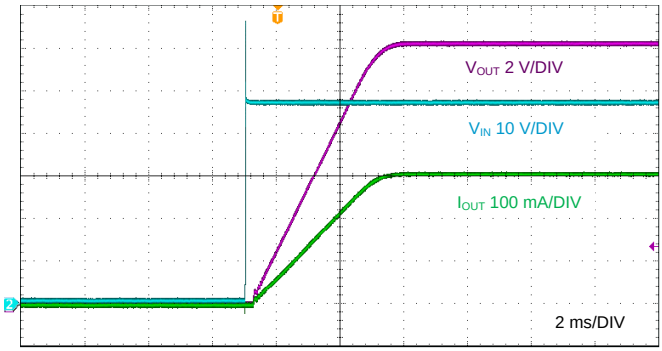



**图 85. Converter Efficiency**



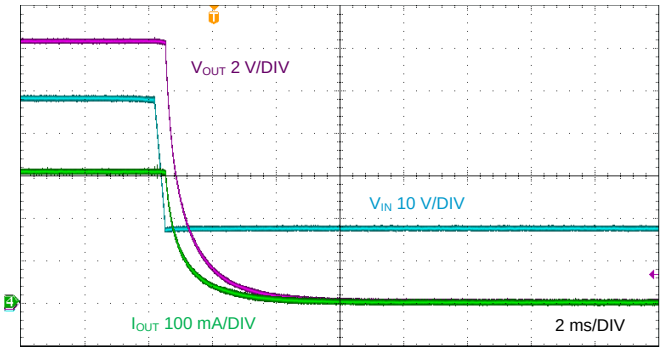

Time Scale: 200 µs/Div
CH3: $V_{OUT}$, 20 mV/Div
CH4: $I_{OUT}$, 0.1 A/Div

**图 86. Load Transient Waveforms, 100 mA to 300 mA**




Time Scale: 2 ms/Div
CH2: $V_{IN}$, 10 V/Div
CH3: $V_{OUT}$, 2 V/Div
CH4: $I_{OUT}$, 0.1 A/Div

**图 87. Start-up Waveforms**




Time Scale: 2 ms/Div
CH2: $V_{IN}$, 10 V/Div
CH3: $V_{OUT}$, 2 V/Div
CH4: $I_L$, 0.1 A/Div

**图 88. Shutdowm Waveforms**

# 9 Power Supply Recommendations

The LM5166 is designed to operate from an input voltage supply range between 3 V and 65 V. This input supply should be able to withstand the maximum input current and maintain a voltage above 3 V. Ensure that the impedance of the input supply rail is low enough that an input current transient does not cause a high enough drop at the LM5166 supply voltage to create a false UVLO fault triggering and system reset. If the input supply is placed more than a few inches from the LM5166 converter, additional bulk capacitance may be required in addition to the ceramic bypass capacitors. A 10-μF electrolytic capacitor is a typical choice for this function, whereby the capacitor ESR provides a level of damping against input filter resonances. A typical ESR of 0.5 Ω provides enough damping for most input circuit configurations.

# 10 Layout

The performance of any switching converter depends as much upon PCB layout as it does the component selection. The following guidelines are provided to assist with designing a PCB with the best power conversion performance, thermal performance, and minimized generation of unwanted EMI.

## 10.1 Layout Guidelines

PCB layout is a critical portion of good power supply design. There are several paths that conduct high slew-rate currents or voltages that can interact with stray inductance or parasitic capacitance to generate noise and EMI or degrade the power supply performance.

1. To help eliminate these problems, bypass the VIN pin to GND with a low-ESR ceramic bypass capacitor with a high-quality dielectric. Place $C_{IN}$ as close as possible to the LM5166 VIN and GND pins. Grounding for both the input and output capacitors should consist of localized top-side planes that connect to the GND pin and GND PAD.
2. Minimize the loop area formed by the input capacitor connections to the VIN and GND pins.
3. Locate the inductor close to the SW pin. Minimize the area of the SW trace or plane to prevent excessive capacitive coupling.
4. Tie the GND pin directly to the power pad under the device and to a heat-sinking PCB ground plane.
5. Use a ground plane in one of the middle layers as noise shielding and heat dissipation path.
6. Have a single-point ground connection to the plane. Route the ground connections for the feedback, soft-start, and enable components to the ground plane. This prevents any switched or load currents from flowing in analog ground traces. If not properly handled, poor grounding results in degraded load regulation or erratic output voltage ripple behavior.
7. Make $V_{IN}$, $V_{OUT}$ and ground bus connections as wide as possible. This reduces any voltage drops on the input or output paths of the converter and maximizes efficiency.
8. Minimize trace length to the FB pin. Place both feedback resistors, $R_{FB1}$ and $R_{FB2}$, close to the FB pin. Place $C_{FF}$ (if needed) directly in parallel with $R_{FB1}$. If output setpoint accuracy at the load is important, connect the $V_{OUT}$ sense at the load. Route the $V_{OUT}$ sense path away from noisy nodes and preferably through a layer on the other side of a shielding layer.
9. The RT pin is sensitive to noise. Thus, locate the $R_{RT}$ resistor as close as possible to the device and route with minimal lengths of trace. The parasitic capacitance from RT to GND must not exceed 20 pF.
10. Provide adequate heat sinking for the LM5166 to keep the junction temperature below 150°C. For operation at full rated load, the top-side ground plane is an important heat-dissipating area. Use an array of heat-sinking vias to connect the exposed pad to the PCB ground plane. If the PCB has multiple copper layers, these thermal vias must also be connected to inner layer heat-spreading ground planes.

### 10.1.1 Compact PCB Layout for EMI Reduction

Radiated EMI generated by high di/dt components relates to pulsing currents in switching converters. The larger area covered by the path of a pulsing current, the more electromagnetic emission is generated. The key to minimizing radiated EMI is to identify the pulsing current path and minimize the area of that path.

The critical switching loop of the buck converter power stage in terms of EMI is denoted in 图 89. The topological architecture of a buck converter means that a particularly high di/dt current path exists in the loop comprising the input capacitor and the integrated MOSFETs of the LM5166, and it becomes mandatory to reduce the parasitic inductance of this loop by minimizing the effective loop area.

## Layout Guidelines (接下页)

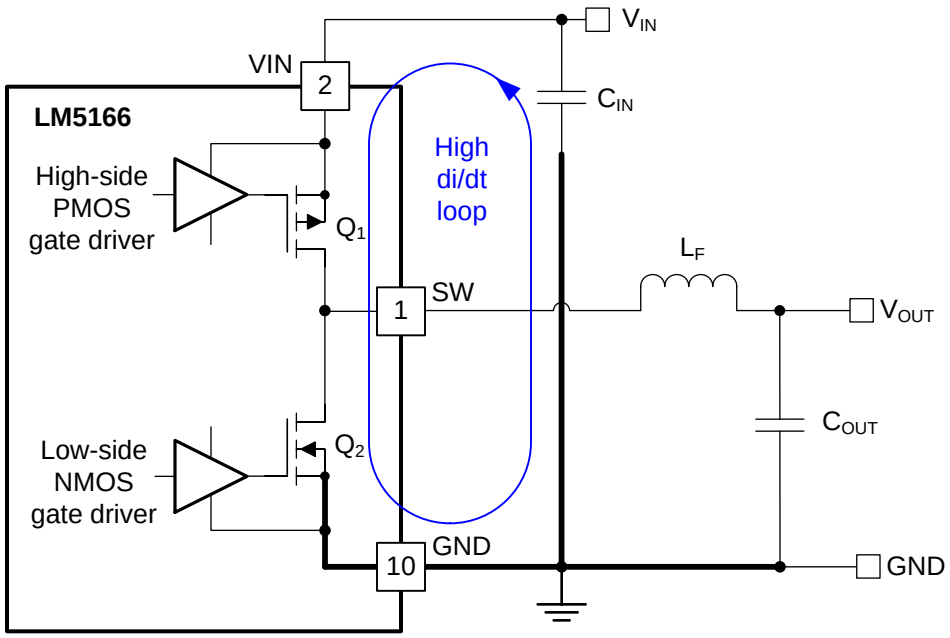



**图 89. DC-DC Buck Converter With Power Stage Circuit Switching Loops**

The input capacitor provides the primary path for the high di/dt components of the high-side MOSFET's current. Placing a ceramic capacitor as close as possible to the VIN and GND pins is the key to EMI reduction. Keep the trace connecting SW to the inductor as short as possible and just wide enough to carry the load current without excessive heating. Use short, thick traces or copper pours (shapes) for current conduction path to minimize parasitic resistance. Place the output capacitor close to the $V_{OUT}$ side of the inductor, and connect the capacitor's return terminal to the GND pin and exposed PAD of the LM5166.

### 10.1.2 Feedback Resistors

For the adjustable output voltage version of the LM5166, reduce noise sensitivity of the output voltage feedback path by placing the resistor divider close to the FB pin, rather than close to the load. This reduces the trace length of FB signal and noise coupling. The FB pin is the input to the feedback comparator, and as such is a high impedance node sensitive to noise. The output node is a low impedance node, so the trace from $V_{OUT}$ to the resistor divider can be long if a short path is not available.

Route the voltage sense trace from the load to the feedback resistor divider, keeping away from the SW node, the inductor and $V_{IN}$ to avoid contaminating the feedback signal with switch noise, while also minimizing the trace length. This is most important when high feedback resistances, greater than 100 kΩ, are used to set the output voltage. Also, route the voltage sense trace on a different layer from the inductor, SW node and $V_{IN}$, such that there is a ground plane that separates the feedback trace from the inductor and SW node copper polygon. This provides further shielding for the voltage feedback path from switching noise sources

## 10.2 Layout Example

图 90 shows an example layout for the PCB top layer of a 4-layer board with essential components placed on the top side. The bottom layer features optional Type 3 ripple generation components ($R_A$ and $C_A$), and $R_{UV1}$, $R_{UV2}$, and $R_{HYS}$ resistors.

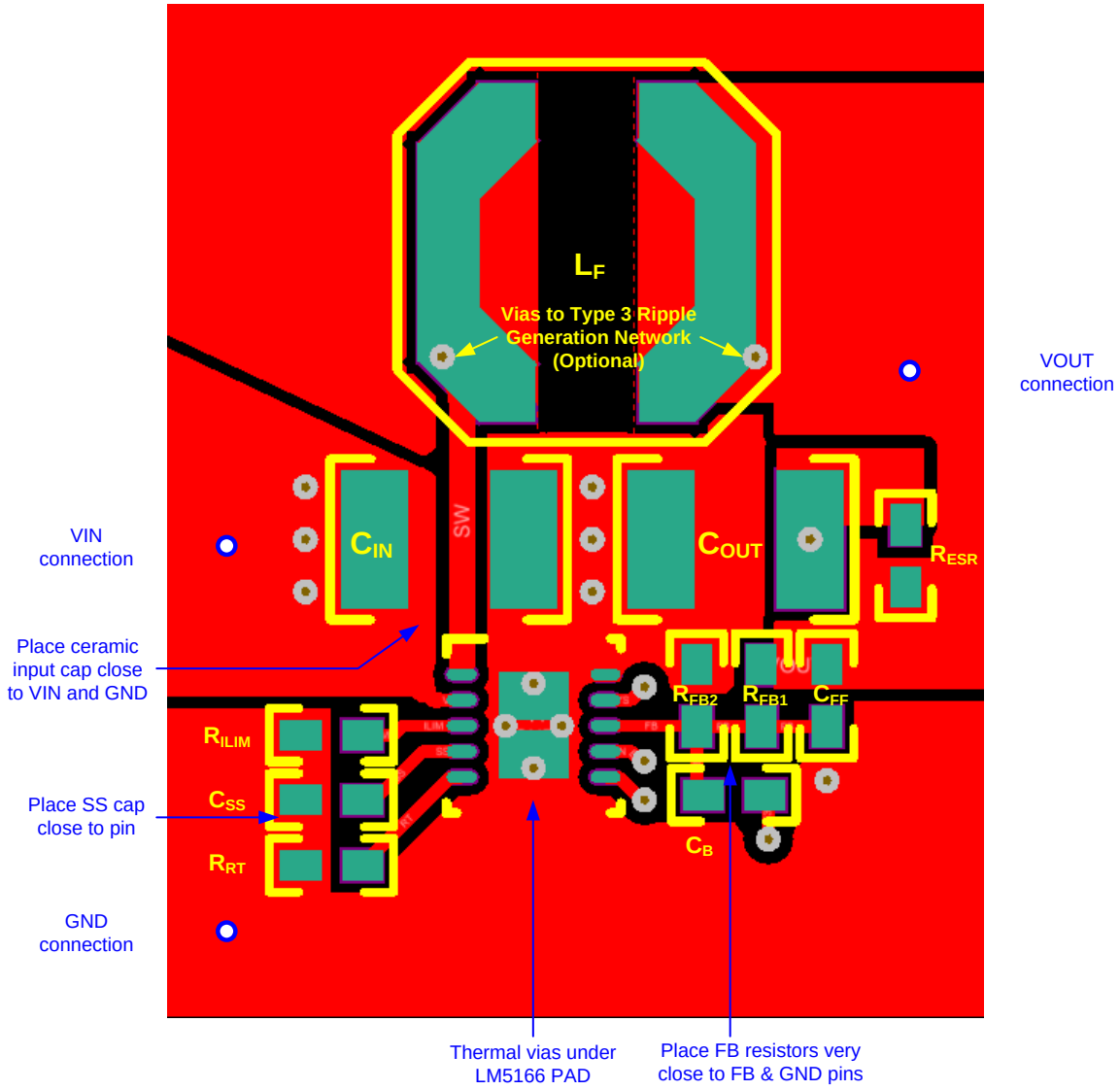



**图 90. LM5166 Single-Sided PCB Layout Example**

# 11 器件和文档支持

## 11.1 器件支持

### 11.1.1 第三方产品免责声明

TI 发布的与第三方产品或服务有关的信息，不能构成与此类产品或服务或保修的适用性有关的认可，不能构成此类产品或服务单独或与任何 TI 产品或服务一起的表示或认可。

### 11.1.2 开发支持

- LM5166 *快速入门计算器*
- LM5166 *仿真模型*
- 如需 TI 的参考设计库，请访问 TIDesigns
- 如需 TI WEBENCH 设计环境，请访问 WEBENCH® 设计中心

### 11.1.3 使用 **WEBENCH®** 工具创建定制设计

请单击此处，使用LM5166 器件并借助 WEBENCH® 电源设计器创建定制设计。

1. 在开始阶段键入输出电压 ($V_{IN}$)、输出电压 ($V_{OUT}$) 和输出电流 ($I_{OUT}$) 要求。
2. 使用优化器拨盘优化关键设计参数，如效率、封装和成本。
3. 将生成的设计与德州仪器 (TI) 的其他解决方案进行比较。

WEBENCH Power Designer 提供一份定制原理图以及罗列实时价格和组件可用性的物料清单。

在多数情况下，可执行以下操作：

- 运行电气仿真，观察重要波形以及电路性能
- 运行热性能仿真，了解电路板热性能
- 将定制原理图和布局方案导出至常用 CAD 格式
- 打印设计方案的 PDF 报告并与同事共享

有关 WEBENCH 工具的详细信息，请访问 www.ti.com/WEBENCH。

## 11.2 文档支持

- *《LM5166EVM-C50A EVM 用户指南》*(SNVU485)
- *《LM5166EVM-C33A EVM 用户指南》*(SNVU544)
- *《低 $I_Q$ 同步降压转换器支持智能场传感器 应用》*(SLYT671)
- *《低 EMI 降压转换器为具有 BLE 连接的多变量传感器发送器供电》*(SLYT693)
- *《为您的 COT 降压转换器选择理想的纹波生成网络》*(SNVA776)
- TI 参考设计：
  - TIDA-01395 *具有宽输入电压转换器和电池量表且适用于智能恒温器的 24V 交流电源级* (TIDUCW0)
  - TIDA-01358 *具有宽输入电压转换器和备用电池且适用于智能恒温器的 24V 交流电源级* (TIDUCE1)
  - TIPD215 *带自适应电源管理、功率低于 1W 的四通道模拟输出模块参考设计* (TIDUCV5)
  - TIDA-00666 *具有低功耗 Bluetooth® 连接且由 4 至 20mA 电流回路供电的场发射器* (TIDUC27)
- Industrial Strength 博客：
  - 为工业应用中的智能传感器发送器 供电
  - Industrial Strength 设计 – 第 1 部分
  - 楼宇自动化趋势：预测性维护
  - 楼宇自动化趋势：用于改善用户舒适度的互联传感器
- 白皮书：
  - *《评估适用于具有成本效益的严苛应用的宽 $V_{IN}$、低 EMI 同步降压 电路》*(SLYY104)
- *《AN-2162：轻松解决直流/直流转换器的传导 EMI 问题》*(SNVA489)
- *《汽车启动仿真器用户指南》*(SLVU984)
- *《使用新的热指标》*(SBVA025)
- *《半导体和 IC 封装热指标》*(SPRA953)

### 11.3 接收文档更新通知

要接收文档更新通知，请导航至德州仪器 TI.com.cn 上的器件产品文件夹。请单击右上角的*通知我* 进行注册，即可收到任意产品信息更改每周摘要。有关更改的详细信息，请查看任意已修订文档中包含的修订历史记录。

### 11.4 社区资源

**下列链接提供到 TI 社区资源的连接。链接的内容由各个分销商“按照原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的 《使用条款》。**

**TI E2E™ 在线社区** ***TI 的工程师对工程师 (E2E) 社区。*** **此社区的创建目的在于促进工程师之间的协作。在 e2e.ti.com 中，您可以咨询问题、分享知识、拓展思路并与同行工程师一道帮助解决问题。**

**设计支持** ***TI 参考设计支持*** **可帮助您快速查找有帮助的 E2E 论坛、设计支持工具以及技术支持的联系信息。**

### 11.5 商标

E2E is a trademark of Texas Instruments.
WEBENCH is a registered trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

### 11.6 静电放电警告

ESD 可能会损坏该集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理措施和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。 精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

### 11.7 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

## 12 机械、封装和可订购信息

以下页面包括机械、封装和可订购信息。这些信息是指定器件的最新可用数据。这些数据发生变化时，我们可能不会另行通知或修订此文档。要获得这份数据表的浏览器版本，请查阅左侧导航栏。

## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead finish/ Ball material (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| LM5166DRCR | ACTIVE | VSON | DRC | 10 | 3000 | RoHS & Green | NIPDAU | Level-2-260C-1 YEAR | -40 to 150 | 5166 | Samples |
| LM5166DRCT | ACTIVE | VSON | DRC | 10 | 250 | RoHS & Green | NIPDAU | Level-2-260C-1 YEAR | -40 to 150 | 5166 | Samples |
| LM5166XDRCR | ACTIVE | VSON | DRC | 10 | 3000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 150 | 5166X | Samples |
| LM5166XDRCT | ACTIVE | VSON | DRC | 10 | 250 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 150 | 5166X | Samples |
| LM5166YDRCR | ACTIVE | VSON | DRC | 10 | 3000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 150 | 5166Y | Samples |
| LM5166YDRCT | ACTIVE | VSON | DRC | 10 | 250 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 150 | 5166Y | Samples |

(1) The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

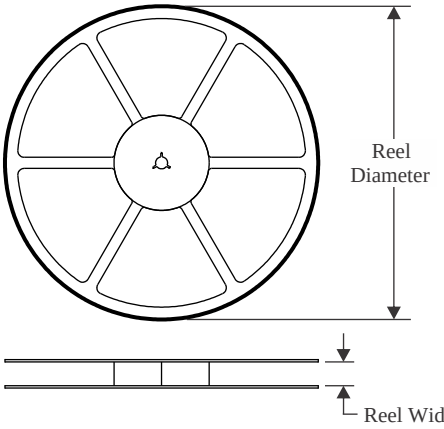
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

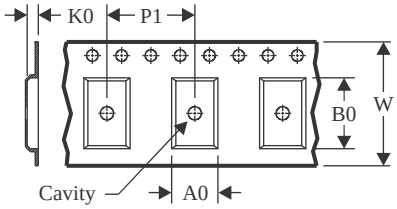
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

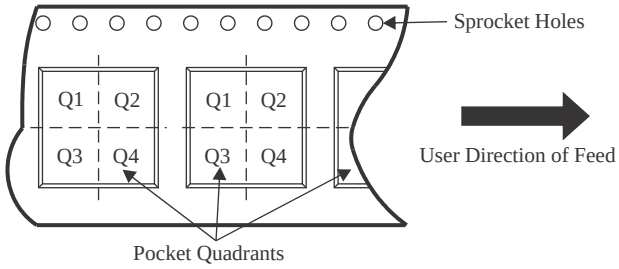



**TAPE DIMENSIONS**




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

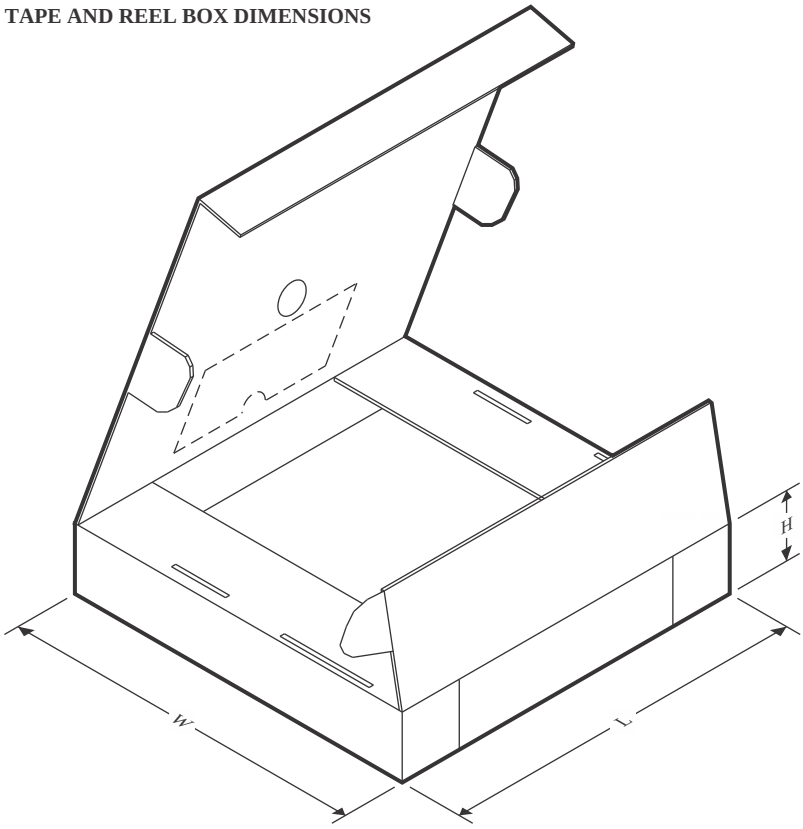
**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| LM5166DRCR | VSON | DRC | 10 | 3000 | 330.0 | 12.4 | 3.3 | 3.3 | 1.1 | 8.0 | 12.0 | Q2 |
| LM5166DRCT | VSON | DRC | 10 | 250 | 180.0 | 12.4 | 3.3 | 3.3 | 1.1 | 8.0 | 12.0 | Q2 |
| LM5166XDRCR | VSON | DRC | 10 | 3000 | 330.0 | 12.4 | 3.3 | 3.3 | 1.1 | 8.0 | 12.0 | Q2 |
| LM5166XDRCT | VSON | DRC | 10 | 250 | 180.0 | 12.4 | 3.3 | 3.3 | 1.1 | 8.0 | 12.0 | Q2 |
| LM5166YDRCR | VSON | DRC | 10 | 3000 | 330.0 | 12.4 | 3.3 | 3.3 | 1.1 | 8.0 | 12.0 | Q2 |
| LM5166YDRCT | VSON | DRC | 10 | 250 | 180.0 | 12.4 | 3.3 | 3.3 | 1.1 | 8.0 | 12.0 | Q2 |

TAPE AND REEL BOX DIMENSIONS




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| LM5166DRCR | VSON | DRC | 10 | 3000 | 346.0 | 346.0 | 33.0 |
| LM5166DRCT | VSON | DRC | 10 | 250 | 210.0 | 185.0 | 35.0 |
| LM5166XDRCR | VSON | DRC | 10 | 3000 | 335.0 | 335.0 | 25.0 |
| LM5166XDRCT | VSON | DRC | 10 | 250 | 182.0 | 182.0 | 20.0 |
| LM5166YDRCR | VSON | DRC | 10 | 3000 | 335.0 | 335.0 | 25.0 |
| LM5166YDRCT | VSON | DRC | 10 | 250 | 182.0 | 182.0 | 20.0 |

# GENERIC PACKAGE VIEW

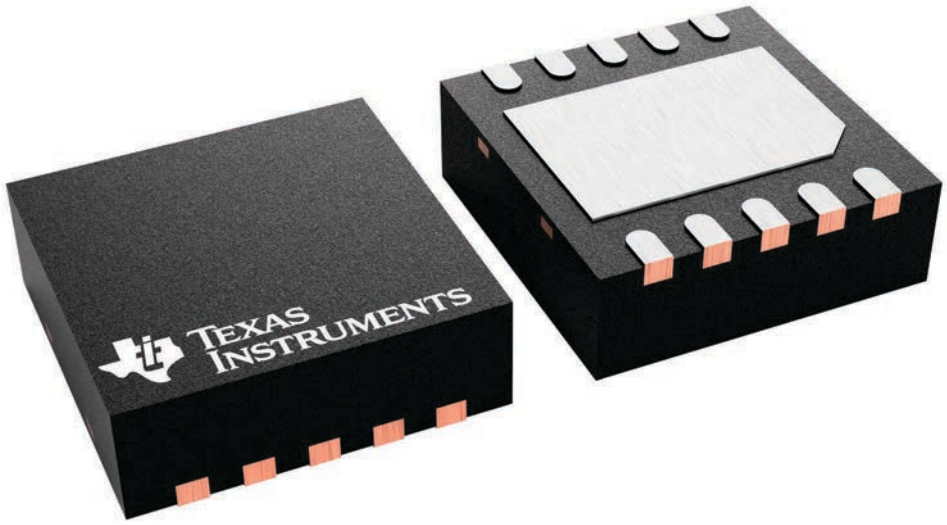
## DRC 10

## VSON - 1 mm max height

**3 x 3, 0.5 mm pitch**

PLASTIC SMALL OUTLINE - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



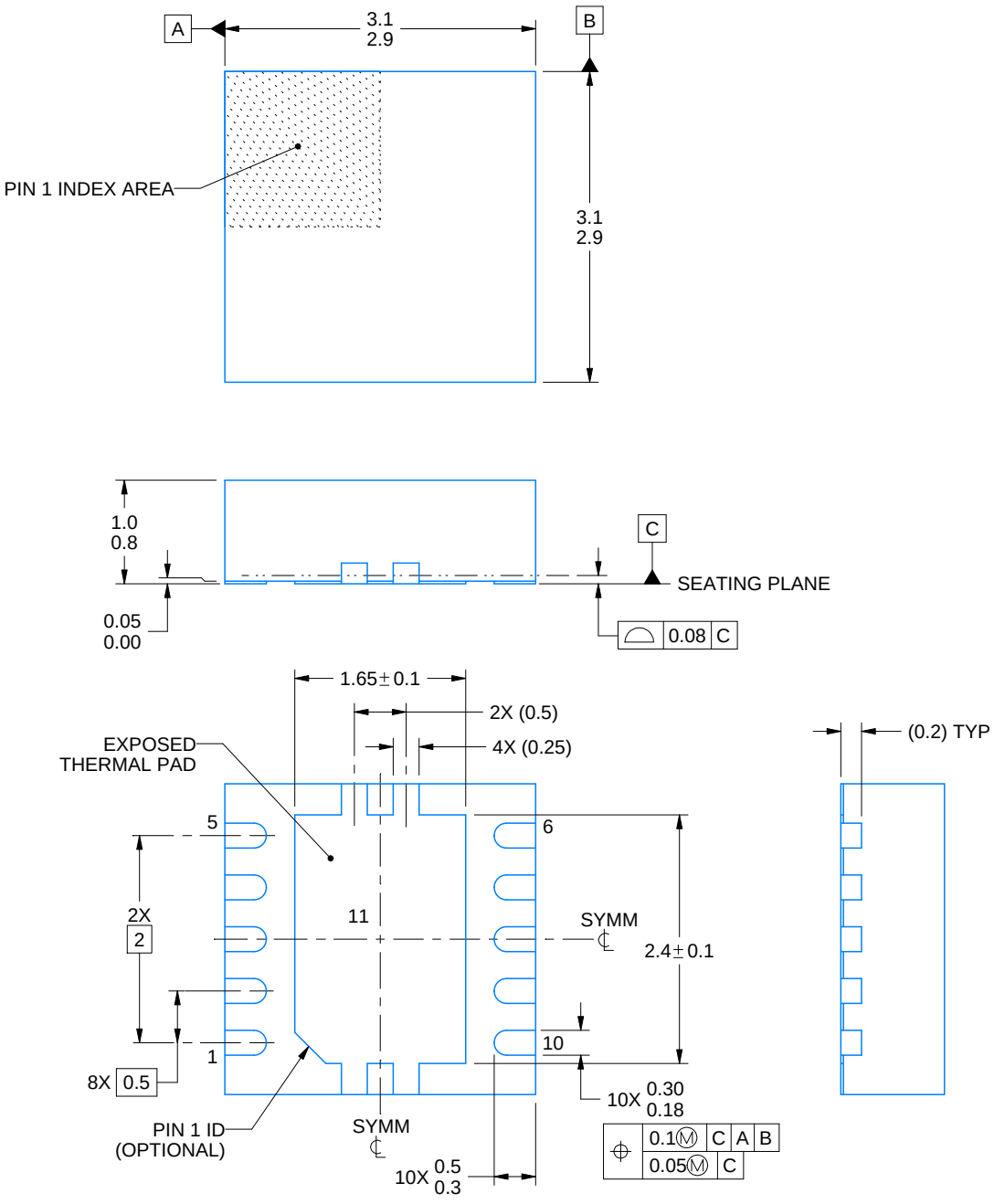

4226193/A

# DRC0010J

# PACKAGE OUTLINE

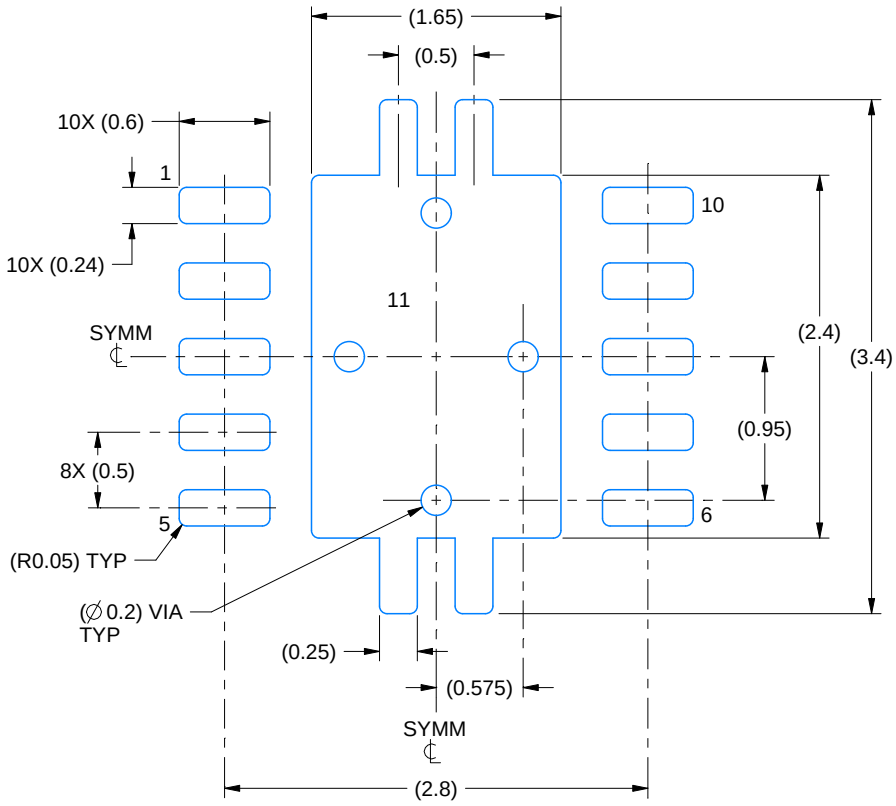
## VSON - 1 mm max height

PLASTIC SMALL OUTLINE - NO LEAD

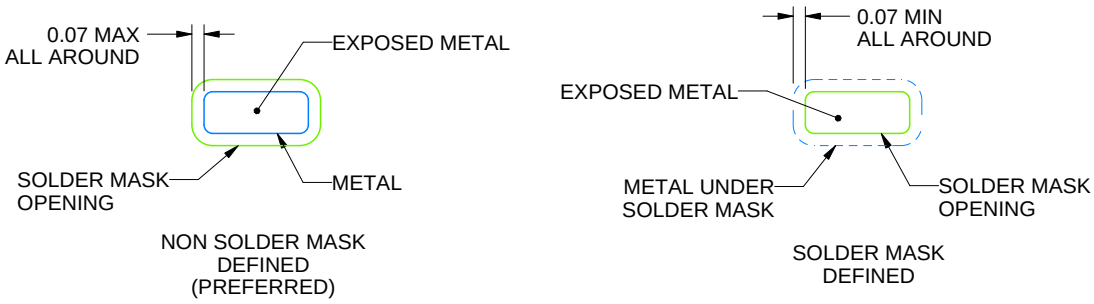



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.




LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:20X




SOLDER MASK DETAILS

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NOTES: (continued)

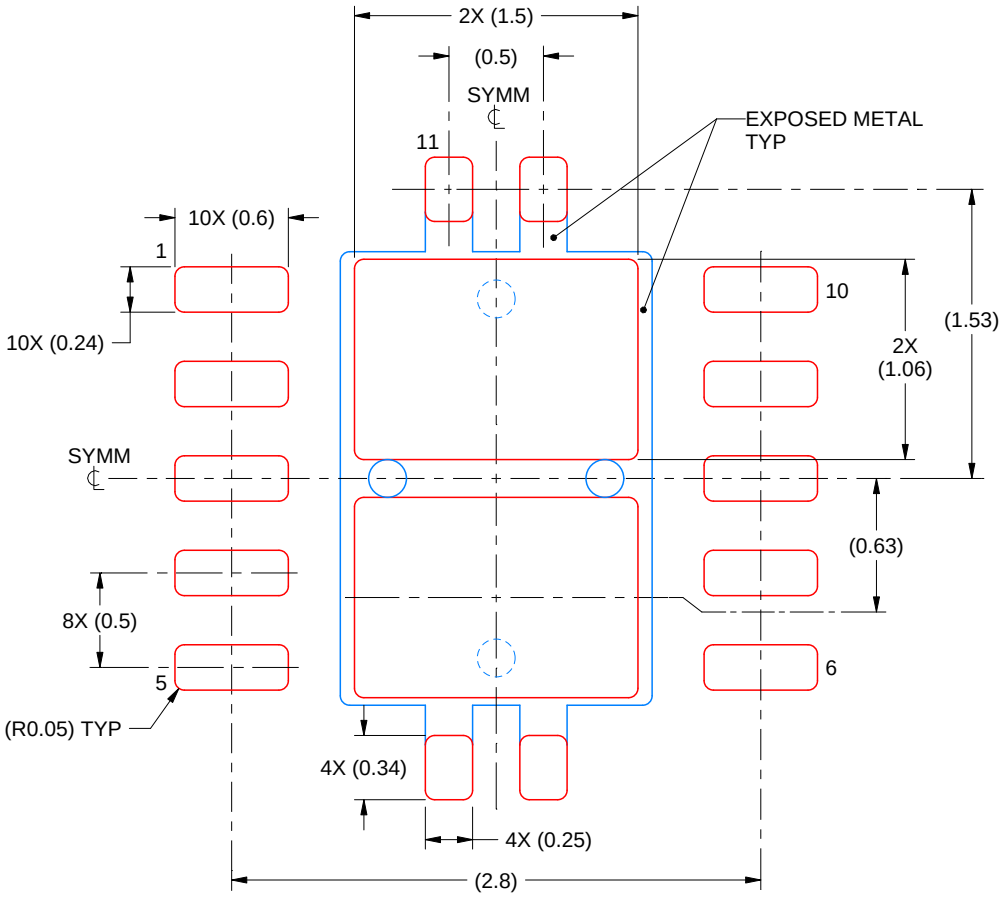
4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

# EXAMPLE STENCIL DESIGN

## DRC0010J

## VSON - 1 mm max height

PLASTIC SMALL OUTLINE - NO LEAD




SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 11:
80% PRINTED SOLDER COVERAGE BY AREA
SCALE:25X

4218878/B 07/2018

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

# 重要声明和免责声明

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