LMH1208 超高清 UHD-SDI 双路输出电缆驱动器

1 特性

- 支持 ST-2082-1 (12G)、ST-2081-1 (6G)、ST-424 (3G)、ST-292 (HD) 和 ST-259 (SD)
- 兼容 DVB-ASI 和 AES10 (MADI)
- 双路差分输出电缆驱动器
- 片上 75Ω 终端和回损补偿网络
- 主机端均衡 100Ω 环回输出
- 75Ω 输出端的可编程压摆率控制
- 75Ω 输出端的可编程预加重和输出振幅
- 100Ω 输出端的可编程去加重功能和输出振幅
- 75Ω 和 100Ω 输出端的极性反转
- 没有输入信号时自动进入省电工作模式
  - 功耗：25mW（典型值）
- 通过 ENABLE 引脚进行断电控制
- 2.5V 单电源
  - 功耗：200mW（典型值）
- 可通过引脚、SPI 或 SMBus 接口进行编程
- 工作温度范围：-40°C 至 +85°C
- 5mm × 5mm 32 引脚 WQFN 封装

2 应用

- SMPTE 兼容串行数字接口
- UHDTV/4K/8K/HDTV/SDTV 视频
- 广播视频路由器、交换机、分配放大器和监视器
- 数字视频处理和编辑

3 说明

LMH1208 器件是一款 12G UHD-SDI 低功耗双路输出电缆驱动器。它支持高达 11.88Gbps 的 SMPTE 视频速率，因此可为 4K/8K 应用实现超高清视频。主机端上额外提供的均衡 100Ω 驱动器输出可用于监控或信号分配用途。

可编程 PCB 输入均衡器提供高频增强功能，以减少 PCB 迹线造成的码间串扰 (ISI)。两个电缆驱动器输出上均集成了 75Ω 终端和回损网络，使得总体系统设计满足严格的 SMPTE 回损要求。

输入信号检测功能可确定电缆驱动器输入端是否具有有效信号。该感应功能可警告用户系统故障并激活省电模式，从而减少电缆驱动器的功耗。LMH1208 提供数据速率高达11.88 Gbps 的可选转换率。输出转换率和振幅可通过引脚、SPI 或 SMBus 控制。

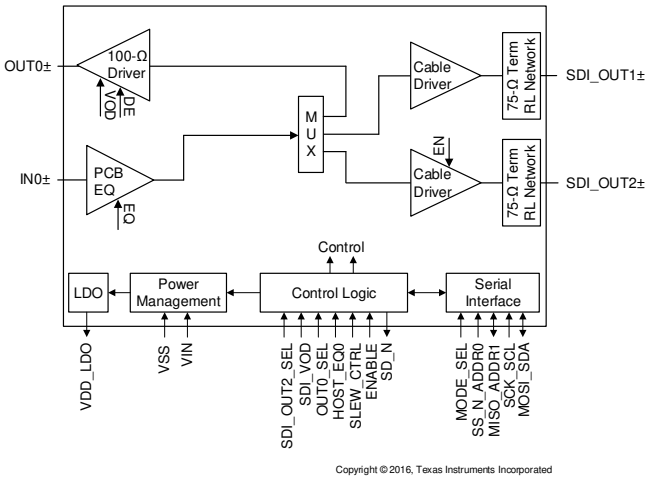
LMH1208 由 2.5V 单电源供电运行。它采用小尺寸 5mm × 5mm 32 引脚 WQFN 封装。LMH1208 与 LMH1228 （带有集成时钟恢复器的 12G 双路电缆驱动器）引脚兼容。

器件信息(1)

器件型号	封装	封装尺寸（标称值）
LMH1208	WQFN (32)	5.00mm × 5.00mm

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。

简化方框图



目录

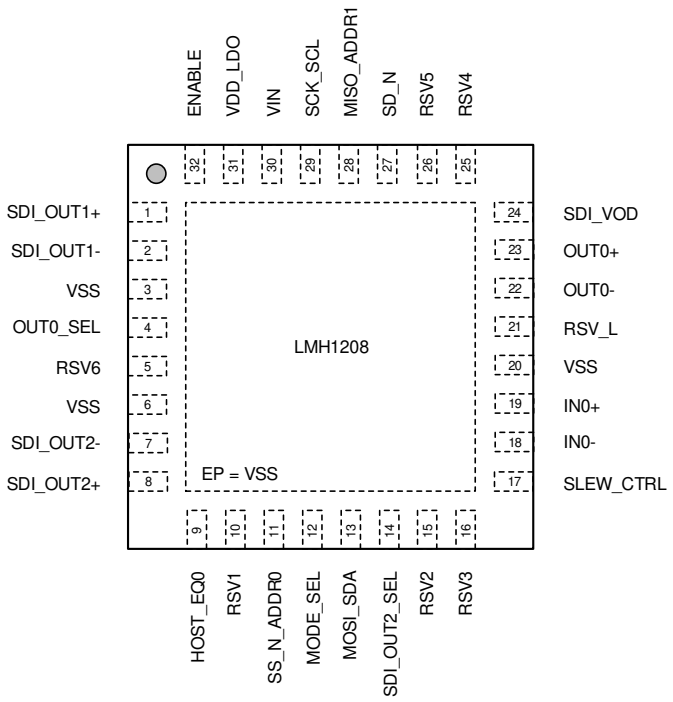
4 修订历史记录

Changes from Revision A (September 2017) to Revision B **Page**

- 首次公开发布 1

5 Pin Configuration and Functions

RTV Package
32-Pin WQFN
Top View



Pin Functions

PIN		I/O(1)	DESCRIPTION
NAME	NO.		
HIGH-SPEED DIFFERENTIAL I/OS			
SDI_OUT1+	1	I/O, Analog	Single-ended complementary outputs with on-chip 75-Ω termination at SDI_OUT1+ and SDI_OUT1–. SDI_OUT1± include integrated return loss networks designed to meet the SMPTE output return loss requirements. Connect SDI_OUT1+ to a BNC through a 4.7-µF, AC-coupling capacitor. SDI_OUT1– should be similarly AC-coupled and terminated with an external 4.7-µF capacitor and 75-Ω resistor to GND.
SDI_OUT1–	2	I/O, Analog	
SDI_OUT2+	8	O, Analog	Single-ended complementary outputs with on-chip 75-Ω termination at SDI_OUT2+ and SDI_OUT2–. SDI_OUT2± include integrated return loss networks designed to meet the SMPTE output return loss requirements. SDI_OUT2± is used as a second cable driver. Connect SDI_OUT2+ to a BNC through a 4.7-µF, AC-coupling capacitor. SDI_OUT2– should be similarly AC-coupled and terminated with an external 4.7-µF capacitor and 75-Ω resistor to GND.
SDI_OUT2–	7	O, Analog	
IN0+	19	I, Analog	Differential inputs from host video processor. On-chip 100-Ω differential termination. Requires external 4.7-µF, AC-coupling capacitors for SMPTE applications.
IN0–	18	I, Analog	
OUT0+	23	O, Analog	Differential outputs to host video processor. On-chip 100-Ω differential termination. Requires external 4.7-µF, AC-coupling capacitors for SMPTE applications.
OUT0–	22	O, Analog	
CONTROL PINS			
OUT0_SEL	4	I, LVCMOS	OUT0_SEL enables the use of the 100-Ω host-side output driver at OUT0±. See Table 2 for details. OUT0_SEL is internally pulled high by default (OUT0 disabled).
HOST_EQ0	9	I, 4-LEVEL	HOST_EQ0 selects the equalizer setting for IN0±. See Table 4 for details.

(1) I = Input, O = Output, I/O = Input or Output, OD = Open Drain, LVCMOS = 2-State Logic, 4-LEVEL = 4-State Logic

Pin Functions (continued)

PIN		I/O[1]	DESCRIPTION
NAME	NO.		
MODE_SEL	12	I, 4-LEVEL	MODE_SEL enables the SPI or SMBus serial control interface. See Table 8 for details.
SDI_OUT2_SEL	14	I, LVCMOS	SDI_OUT2_SEL enables the use of the 75-Ω output driver at SDI_OUT2±. See Table 2 for details. SDI_OUT2_SEL is internally pulled high by default (SDI_OUT2 disabled).
SLEW_CTRL	17	I, 4-LEVEL	SLEW_CTRL selects the edge rate for both cable driver outputs. SLEW_CTRL settings are dependent on the operating SMPTE data rate. SLEW_CTRL also determines the pre-emphasis level applied to both cable driver outputs. See Table 6 and Table 7 for details.
SDI_VOD	24	I, 4-LEVEL	SDI_VOD selects one of four output amplitudes for the cable drivers at SDI_OUT1± and SDI_OUT2±. See Table 5 for details.
SD_N	27	O, LVCMOS, OD	SD_N is the Signal Detect indicator. SD_N is pulled low when signal is detected at IN0±. SD_N is a 3.3-V tolerant, open-drain output. It requires an external resistor to a logic supply. SD_N can be reconfigured to indicate Interrupt (INT_N) through register programming. See *Status Indicators and Interrupts*.
ENABLE	32	I, LVCMOS	A logic-high at ENABLE enables normal operation for the LMH1208. A logic-low at ENABLE places the LMH1208 in Power-Down Mode. ENABLE is internally pulled high by default.
SPI SERIAL CONTROL INTERFACE, MODE_SEL = F (FLOAT)			
SS_N	11	I, LVCMOS	SS_N is the Slave Select. When SS_N is at logic low, it enables SPI access to the LMH1208 slave device. SS_N is a 2.5-V LVCMOS input and is internally pulled high by default.
MOSI	13	I, LVCMOS	MOSI is the SPI serial control data input to the LMH1208 slave device when the SPI bus is enabled. MOSI is a 2.5-V LVCMOS input. An external pullup resistor is recommended.
MISO	28	O, LVCMOS	MISO is the SPI serial control data output from the LMH1208 slave device. MISO is a 2.5-V LVCMOS output.
SCK	29	I, LVCMOS	SCK is the SPI serial input clock to the LMH1208 slave device when the SPI interface is enabled. SCK is a 2.5-V LVCMOS input. An external pullup resistor is recommended.
SMBUS SERIAL CONTROL INTERFACE, MODE_SEL = L (1 KΩ TO VSS)			
ADDR0	11	Strap, 4-LEVEL	ADDR[1:0] are 4-level straps, read into the device at power up. They are used to select one of the 16 supported SMBus addresses when SMBus is enabled. See Table 9 for details.
SDA	13	I/O, LVCMOS, OD	SDA is the SMBus bidirectional data line to or from the LMH1208 slave device when SMBus is enabled. SDA is an open-drain I/O and requires an external pullup resistor to the SMBus termination voltage. SDA is 3.3-V tolerant.
ADDR1	28	Strap, 4-LEVEL	ADDR[1:0] are 4-level straps, read into the device at power up. They are used to select one of the 16 supported SMBus addresses when SMBus is enabled. See Table 9 for details.
SCL	29	I/O, LVCMOS, OD	SCL is the SMBus input clock to the LMH1208 slave device when SMBus is enabled. It is driven by a LVCMOS open-drain driver from the SMBus master. SCL requires an external pullup resistor to the SMBus termination voltage. SCL is 3.3-V tolerant.

Pin Functions (continued)

PIN		I/O[1]	DESCRIPTION
NAME	NO.		
RESERVED			
RSV1 RSV2 RSV3 RSV4 RSV5 RSV6	10 15 16 25 26 5	—	Reserved pins. Do not connect.
POWER			
VSS	3, 6, 20	I, Ground	Ground reference.
RSV_L	21	I, Power	Connect RSV_L to the same 2.5-V ± 5% supply as VIN.
VIN	30	I, Power	VIN is connected to an external 2.5-V ± 5% power supply.
VDD_LDO	31	O, Power	VDD_LDO is the output of the internal 1.8-V LDO regulator. VDD_LDO output requires an external 1-µF and 0.1-µF bypass capacitor to VSS. The internal LDO is designed to power internal circuitry only.
EP	—	I, Ground	EP is the exposed pad at the bottom of the RTV package. The exposed pad should be connected to the VSS plane through a 3 × 3 via array.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

	MIN	MAX	UNIT
Supply voltage (VIN, RSV_L)	–0.5	2.75	V
Input voltage for 4-level pins	–0.5	2.75	V
Input/output voltage for 2-level control pins	–0.5	2.75	V
SMBus input/output voltage (SDA, SCL)	–0.5	4	V
SPI input/output voltage (SS_N, MISO, MOSI, and SCK)	–0.5	2.75	V
High-speed input/output voltage (IN0±, SDI_OUT1±, OUT0±, SDI_OUT2±)	–0.5	2.75	V
Input current (IN0±)	–30	30	mA
Operating junction temperature		125	°C
Storage temperature, T_{stg}	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$ Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	All pins except 13 and 29	±6000	V
		Pins 13 and 29	±5500	
	Charged-device model (CDM), per JEDEC specification JESD22-C101(2)		±1500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 500-V HBM is possible with the necessary precautions.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 250-V CDM is possible with the necessary precautions.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
	Supply voltage	VIN, RSV_L to VSS	2.375	2.5	2.625	V
VDD_{SMBUS}	SMBus: SDA, SCL open-drain termination voltage		2.375		3.6	V
V_{IN0_LAUNCH}	Source differential launch amplitude	Before 5-inch board trace to IN0±	300		850	mVp-p
		Before 20-inch board trace to IN0±	650		1000	
$T_{JUNCTION}$	Operating junction temperature				110	°C
$T_{AMBIENT}$	Ambient temperature		–40	25	85	°C
$NTps_{max}$	Maximum supply noise(1)	50 Hz to 1 MHz, sinusoidal		< 20		mVp-p
		1.1 MHz to 50 MHz, sinusoidal		< 10		

(1) The sum of the DC supply voltage and AC supply noise should not exceed the recommended supply voltage range.

6.4 Thermal Information

THERMAL METRIC(1)		LMH1208 RTV (WQFN) 32 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	32.5	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	15.0	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	6.5	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.2	°C/W
ψ_{JB}	Junction-to-board characterization parameter	6.5	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	1.7	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.5 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER						
PD	Power dissipation Measured with PRBS10, Operating at 11.88 Gbps, VOD = default	SDI_OUT1± enabled SDI_OUT2± disabled OUT0± disabled		200		mW
		SDI_OUT1± enabled SDI_OUT2± disabled OUT0± enabled		250		mW
		SDI_OUT1± enabled SDI_OUT2± enabled OUT0± disabled		340		mW
		SDI_OUT1± enabled SDI_OUT2± enabled OUT0± enabled		385		mW
PD_Z	Power dissipation, Power Save Mode	Power Save Mode, ENABLE = H, no signal applied at IN0±		25		mW
IDD	Current consumption, Measured with PRBS10, Operating at 11.88 Gbps, VOD = default	SDI_OUT1± enabled SDI_OUT2± disabled OUT0± disabled		80	104	mA
		SDI_OUT1± enabled SDI_OUT2± disabled OUT0± enabled		100	125	mA
		SDI_OUT1± enabled SDI_OUT2± enabled OUT0± disabled		136	170	mA
		SDI_OUT1± enabled SDI_OUT2± enabled OUT0± enabled		154	190	mA
IDD_Z	Current consumption, Power Save Mode	Power Save Mode, ENABLE = H, no signal applied at IN0±		10		mA
IDD_{Z_PD}	Current consumption, Power-Down Mode	Power-Down Mode, ENABLE = L, no signal applied at IN0±		10	30	mA
LVCMOS DC SPECIFICATIONS						
V_{IH}	Logic high input voltage	2-level input (SS_N, SCK, MOSI, SDI_OUT2_SEL, OUT0_SEL, ENABLE)	0.72 × VIN		VIN + 0.3	V
		2-level input (SCL, SDA)	0.7 × VIN		3.6	V
V_{IL}	Logic low input voltage	2-level input (SS_N, SCK, MOSI, SDI_OUT2_SEL, OUT0_SEL, ENABLE, SCL, SDA)	0		0.3 × VIN	V
V_{OH}	Logic high output voltage	IOH = –2 mA, (MISO)	0.8 × VIN		VIN	V

Electrical Characteristics (continued)

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OL}	Logic low output voltage	IOL = 2 mA, (MISO)	0		0.2 × VIN	V
		IOL = 3 mA, (SD_N, SDA)			0.4	V
I_{IH}	Input high leakage current (Vinput = VIN)	LVCMOS (SDI_OUT2_SEL, ENABLE)			15	µA
		LVCMOS (OUT0_SEL)			65	µA
		LVCMOS (SD_N)			10	µA
		SPI mode: LVCMOS (SS_N, SCK, MOSI)			15	µA
		SMBus mode: LVCMOS (SCL, SDA)			10	µA
I_{IL}	Input low leakage current (Vinput = GND)	LVCMOS (SDI_OUT2_SEL, ENABLE)	–50			µA
		LVCMOS (OUT0_SEL)	–15			µA
		LVCMOS (SD_N)	–10			µA
		SPI mode: LVCMOS (SCK, MOSI)	–15			µA
		SPI mode: LVCMOS (SS_N)	–50			µA
		SMBus mode: LVCMOS (SCL, SDA)	–10			µA
4-LEVEL LOGIC DC SPECIFICATIONS (APPLY TO ALL 4-LEVEL INPUT CONTROL PINS)						
V_{LVL_H}	LEVEL-H input voltage	Measured voltage at 4-level pin with external 1 kΩ to VIN		VIN		V
V_{LVL_F}	LEVEL-F default voltage	Measured voltage 4-level pin at default		2/3 × VIN		V
V_{LVL_R}	LEVEL-R input voltage	Measured voltage at 4-level pin with external 20 kΩ to VSS		1/3 × VIN		V
V_{LVL_L}	LEVEL-L input voltage	Measured voltage at 4-level pin with external 1 kΩ to VSS		0		V
I_{IH}	Input high leakage current (Vinput = VIN)	4-levels (HOST_EQ0, MODE_SEL, SLEW_CTRL, SDI_VOD)	20	45	80	µA
		SMBus mode: 4-levels (ADDR0, ADDR1)	20	45	80	µA
I_{IL}	Input low leakage current (Vinput = GND)	4-levels (HOST_EQ0, MODE_SEL, SLEW_CTRL, SDI_VOD)	–160	–93	–40	µA
		SMBus mode: 4-levels (ADDR0, ADDR1)	–160	–93	–40	µA
RECEIVER SPECIFICATIONS (IN0±)						
R_{IN0_TERM}	DC input differential termination	Measured across IN0+ to IN0–	80	100	120	Ω
RL_{IN0_SDD11}	Input differential return loss(1)	SDD11, 10 MHz – 2.8 GHz		–22		dB
		SDD11, 2.8 GHz – 6 GHz		–16		dB
		SDD11, 6 GHz – 11.1 GHz		–10		dB
RL_{IN0_SCD11}	Differential to common-mode input conversion(1)	SCD11, 10 MHz to 11.1 GHz		–21		dB
V_{IN0_CM}	DC common-mode voltage	Input common-mode voltage at IN0+ or IN0– to GND		2.06		V
CD_{ON_IN0}	Signal detect (default) Assert ON threshold level for IN0±	11.88 Gbps, EQ and PLL pathological pattern		20		mVp-p
CD_{OFF_IN0}	Signal detect (default) Deassert OFF threshold level for IN0±	11.88 Gbps, EQ and PLL pathological pattern		18		mVp-p
DRIVER OUTPUT (SDI_OUT1+ AND SDI_OUT2+)						
R_{OUT_TERM}	DC output single-ended termination	SDI_OUT1+ and SDI_OUT1–, SDI_OUT2+ and SDI_OUT2– to VIN	63	75	87	Ω

(1) This parameter is measured with the LMH1297EVM (Evaluation board for LMH1208).

Electrical Characteristics (continued)

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
VOD_{CD_OUTP}	Output single-ended output voltage	Measure AC signal at SDI_OUT1+ and SDI_OUT2+, with SDI_OUT1– and SDI_OUT2– AC terminated with 75 Ω SDI_VOD = H		840		mVp-p
		SDI_VOD = F	720	800	880	mVp-p
		SDI_VOD = R		880		mVp-p
		SDI_VOD = L		760		mVp-p
VOD_{CD_OUTN}	Output single-ended output voltage	Measure AC signal at SDI_OUT1– and SDI_OUT2-, with SDI_OUT1+ and SDI_OUT2+ AC terminated with 75 Ω SDI_VOD = H		840		mVp-p
		SDI_VOD = F	720	800	880	mVp-p
		SDI_VOD = R		880		mVp-p
		SDI_VOD = L		760		mVp-p
PRE_{CD_OUTP}	Output pre-emphasis	Output pre-emphasis boost amplitude at SDI_OUT1+ and SDI_OUT2+, programmed to maximum setting through register, measured at SDI_VOD = F		2		dB
PRE_{CD_OUTN}	Output pre-emphasis	Output pre-emphasis boost amplitude at SDI_OUT1– and SDI_OUT2–, programmed to maximum setting through register, measured at SDI_VOD = F		2		dB
$t_{R\_F\_SDI}$	Output rise and fall time (1)	Measured with PRBS10 pattern, default VOD at 20% – 80% amplitude, default pre-emphasis enabled 11.88 Gbps		34	42	ps
		5.94 Gbps		36	43	ps
		2.97 Gbps		59	67	ps
		1.485 Gbps		60	73	ps
		270 Mbps	400	550	700	ps
$t_{R\_F\_DELTA}$	Output rise and fall time mismatch (1)	Measured with PRBS10 pattern, default VOD at 20% – 80% amplitude, default pre-emphasis enabled 11.88 Gbps		3	18	ps
		5.94 Gbps		2.7	12	ps
		2.97 Gbps		0.8	11	ps
		1.485 Gbps		0.8	12	ps
		270 Mbps		72	150	ps
$V_{OVERSHOOT}$	Output overshoot or undershoot	Measured with PRBS10 pattern, default VOD, default pre-emphasis enabled (2) 12G/6G/3G/HD/SD		5%		
V_{DC_OFFSET}	DC offset	12G/6G/3G/HD/SD		±0.2		V
V_{DC_WANDER}	DC wander	12G/6G/3G/HD/SD with EQ pathological pattern		20		mV
RL_{CD_S22}	Output return loss at SDI_OUT1+ and SDI_OUT2+ reference to 75 Ω (1)	S22, 5 MHz to 1.485 GHz		–25		dB
		S22, 1.485 GHz to 3 GHz		–22		dB
		S22, 3 GHz to 6 GHz		–12		dB
		S22, 6 GHz to 12 GHz		–8		dB

(2) $V_{OVERSHOOT}$ overshoot and undershoot maximum measurements are largely affected by the PCB layout and input test pattern. The maximum value specified in *Electrical Characteristics* for $V_{OVERSHOOT}$ is based on bench evaluation across temperature and supply voltages with the LMH1297EVM.

Electrical Characteristics (continued)

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
DRIVER OUTPUT (OUT0±)						
R_{OUT0_TERM}	DC output differential termination	Measured across OUT0+ and OUT0–	80	100	120	Ω
VOD_{OUT0}	Output differential voltage at OUT0±	Measured with 8T pattern HOST_EQ0 = H		410		mVp-p
		HOST_EQ0 = F	485	560	620	mVp-p
		HOST_EQ0 = R		635		mVp-p
		HOST_EQ0 = L		810		mVp-p
VOD_{OUT0_DE}	De-emphasized output differential voltage at OUT0±	Measured with 8T pattern HOST_EQ0 = H		410		mVp-p
		HOST_EQ0 = F		550		mVp-p
		HOST_EQ0 = R		545		mVp-p
		HOST_EQ0 = L		532		mVp-p
t_R/t_F	Output rise and fall time	Measured with 8T Pattern, 20% – 80% amplitude		45		ps
$RL_{OUT0-SDD22}$	Output differential return loss(1)	Measured with the device powered up and outputs a 10-MHz clock signal SDD22, 10 MHz – 2.8 GHz		–24		dB
		SDD22, 2.8 GHz – 6 GHz		–16		dB
		SDD22, 6 GHz – 11.1 GHz		–15		dB
$RL_{OUT0-SCC22}$	Output common-mode return loss(1)	Measured with the device powered up and outputs a 10-MHz clock signal. SCC22, 10 MHz – 4.75 GHz		–12		dB
		SCC22, 4.75 GHz – 11.1 GHz		–9		dB
V_{OUT0_CM}	AC common-mode voltage on OUT0±(1)	Default setting, PRBS31, 11.88 Gbps		8		mV (rms)
OUTPUT JITTER						
$ADDJ_{CD}$	Additive jitter(1)	Measured at SDI_OUT1+ and SDI_OUT2+, OUT0± disabled PRBS10, 12G/6G/3G/HD/SD		0.03		UI

6.6 Recommended SMBus Interface Timing Specifications

over recommended operating supply and temperature ranges unless otherwise specified(1)

PARAMETER		TEST CONDITIONS	MIN	NOM	MAX	UNIT
F_{SCL}	SMBUS SCL frequency		10		400	kHz
T_{BUF}	Bus free time between stop and start condition	See Figure 1.	1.3			µs
$T_{HD:STA}$	Hold time after (repeated) start condition	After this period, the first clock is generated.	0.6			µs
$T_{SU:STA}$	Repeated start condition setup time	See Figure 1.	0.6			µs
$T_{SU:STO}$	Stop condition setup time	See Figure 1.	0.6			µs
$T_{HD:DAT}$	Data hold time	See Figure 1.	0			ns
$T_{SU:DAT}$	Data setup time	See Figure 1.	100			ns
T_{LOW}	Clock low period	See Figure 1.	1.3			µs
T_{HIGH}	Clock high period	See Figure 1.	0.6			µs
T_R	Clock and data rise time	See Figure 1.			300	ns
T_F	Clock and data fall time	See Figure 1.			300	ns
T_{POR}	SMBus ready time after POR	Time from minimum VDDIO to SMBus valid write or read access			50	ms

(1) These parameters support SMBus 2.0 specifications.

6.7 Serial Parallel Interface (SPI) Timing Specifications

over recommended operating supply and temperature ranges unless otherwise specified(1)

PARAMETER		TEST CONDITIONS	MIN	NOM	MAX	UNIT
F_{SCK}	SPI SCK frequency				20	MHz
T_{PH}	SCK pulse width high	See Figure 2 and Figure 3	40			% SCK period
T_{PL}	SCK pulse width low		40			% SCK period
T_{SU}	MOSI setup time	See Figure 2 and Figure 3	4			ns
T_{H}	MOSI hold time		4			ns
T_{SSSU}	SS setup time	See Figure 2 and Figure 3	14			ns
T_{SSH}	SS hold time		4			ns
T_{SSOF}	SS off time		1			µs
T_{ODZ}	MISO driven-to-tristate time	See Figure 2 and Figure 3		20		ns
T_{OZD}	MISO tristate-to-driven time			10		ns
T_{OD}	MISO output delay time			15		ns

(1) Typical SPI load capacitance is 2 pF.

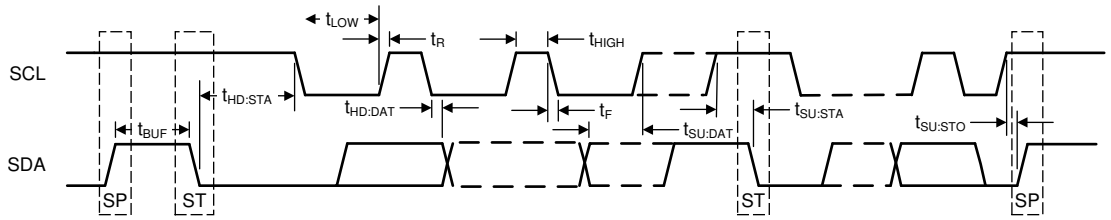


Figure 1. SMBus Timing Parameters

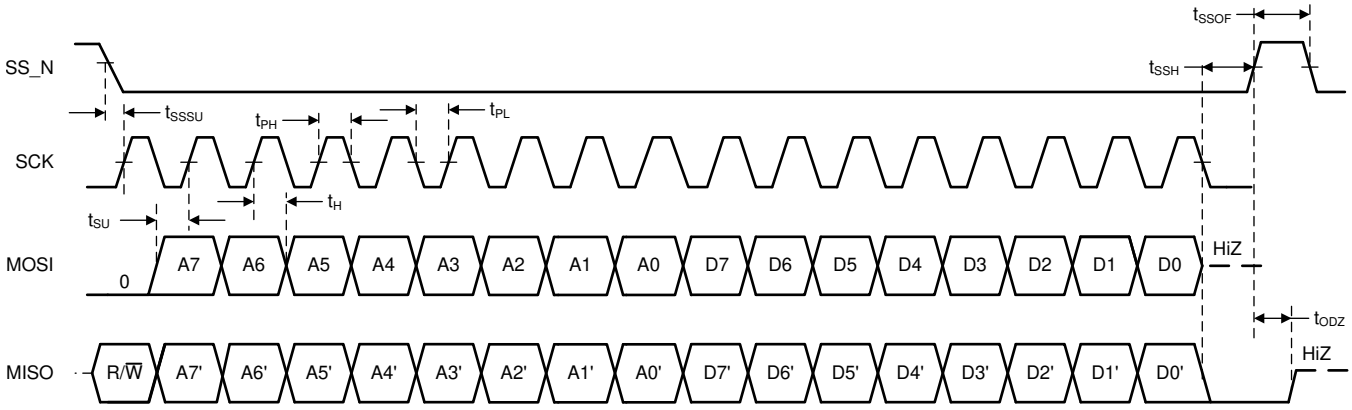


Figure 2. SPI Timing Parameters (Write Operation)

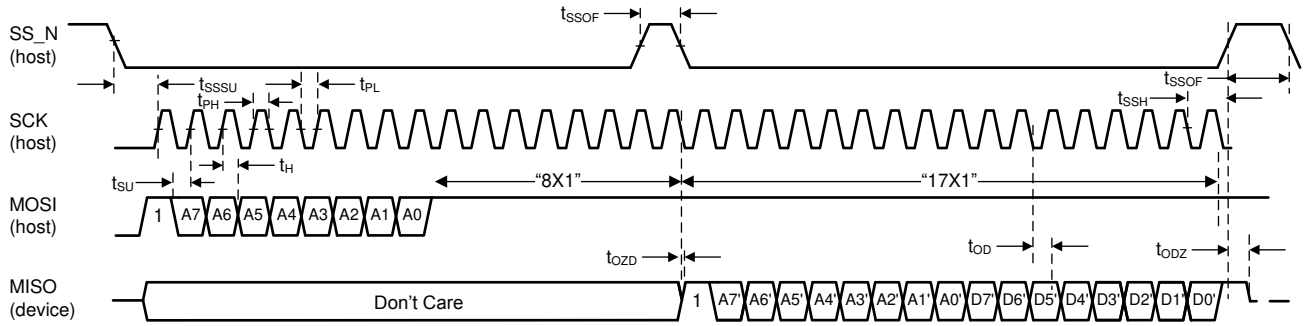


Figure 3. SPI Timing Parameters (Read Operation)

6.8 Typical Characteristics

T_A = 25°C and VIN = RSV_L = 2.5 V (unless otherwise noted)

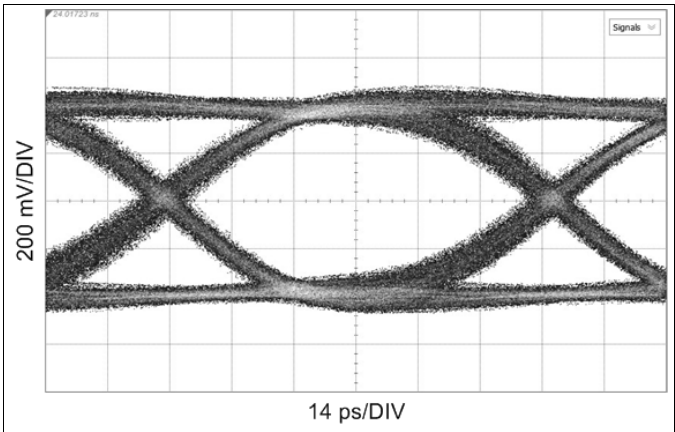


Figure 4. Output at 11.88 Gbps, Measured at SDI_OUT1+, 1-in. FR4 Before IN0±

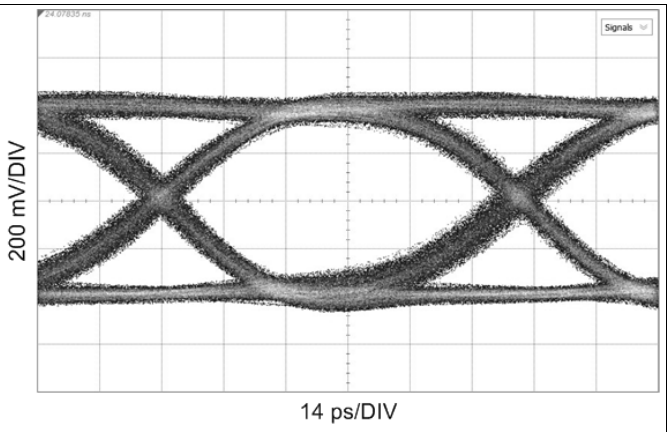


Figure 5. Output at 11.88 Gbps, Measured at SDI_OUT2+, 1-in. FR4 Before IN0±

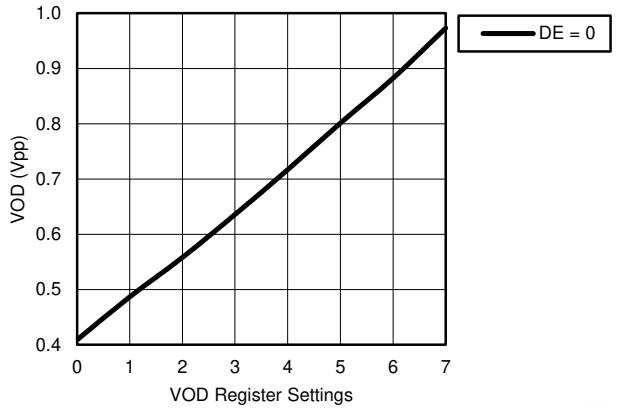


Figure 6. OUT0 VOD vs. OUT0 VOD and DE Register Settings

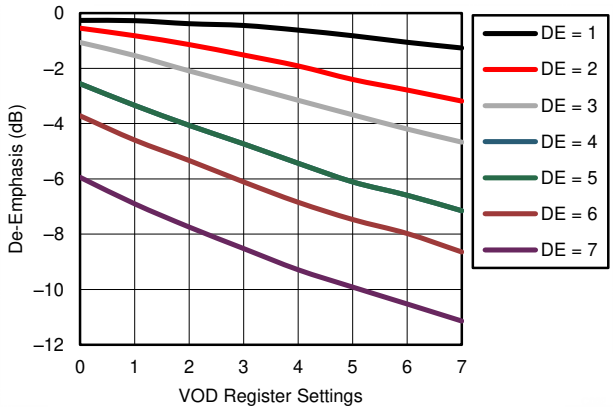
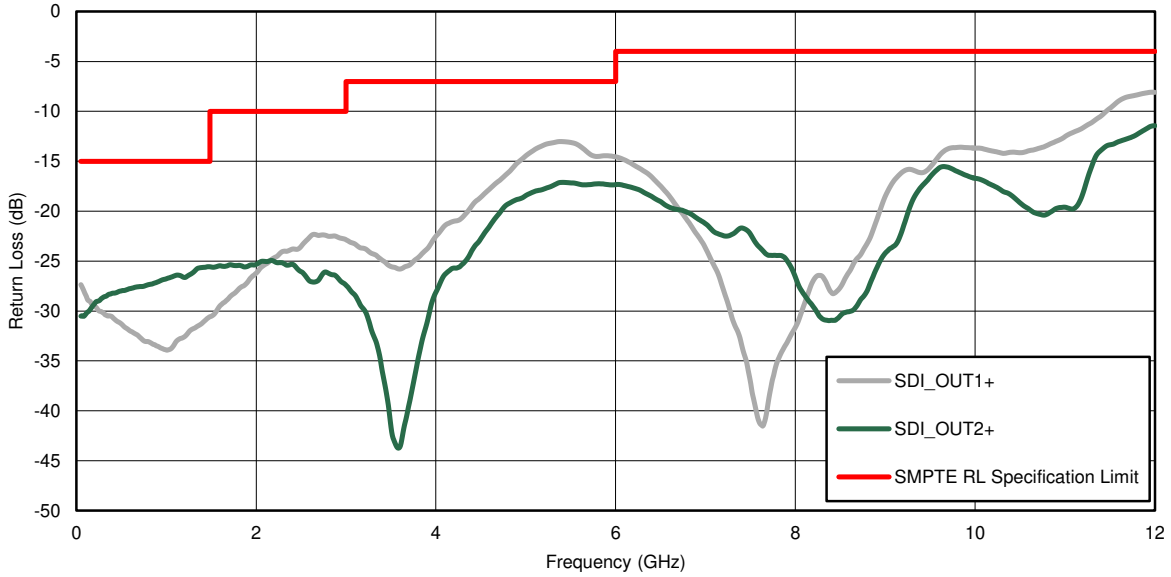


Figure 7. OUT0 De-Emphasis vs. OUT0 VOD and DE Register Settings



Measured with LMH1297EVM

Figure 8. Return Loss (RL) vs Frequency

7 Detailed Description

7.1 Overview

The LMH1208 is a 12G UHD-SDI dual output cable driver. From the host-side input at IN0±, the signal is equalized and routed to 75-Ω cable driver outputs at SDI_OUT1+ and SDI_OUT2+. The 100-Ω driver at OUT0± can be used as a host-side loop-back output for monitoring purposes.

7.2 Functional Block Diagram

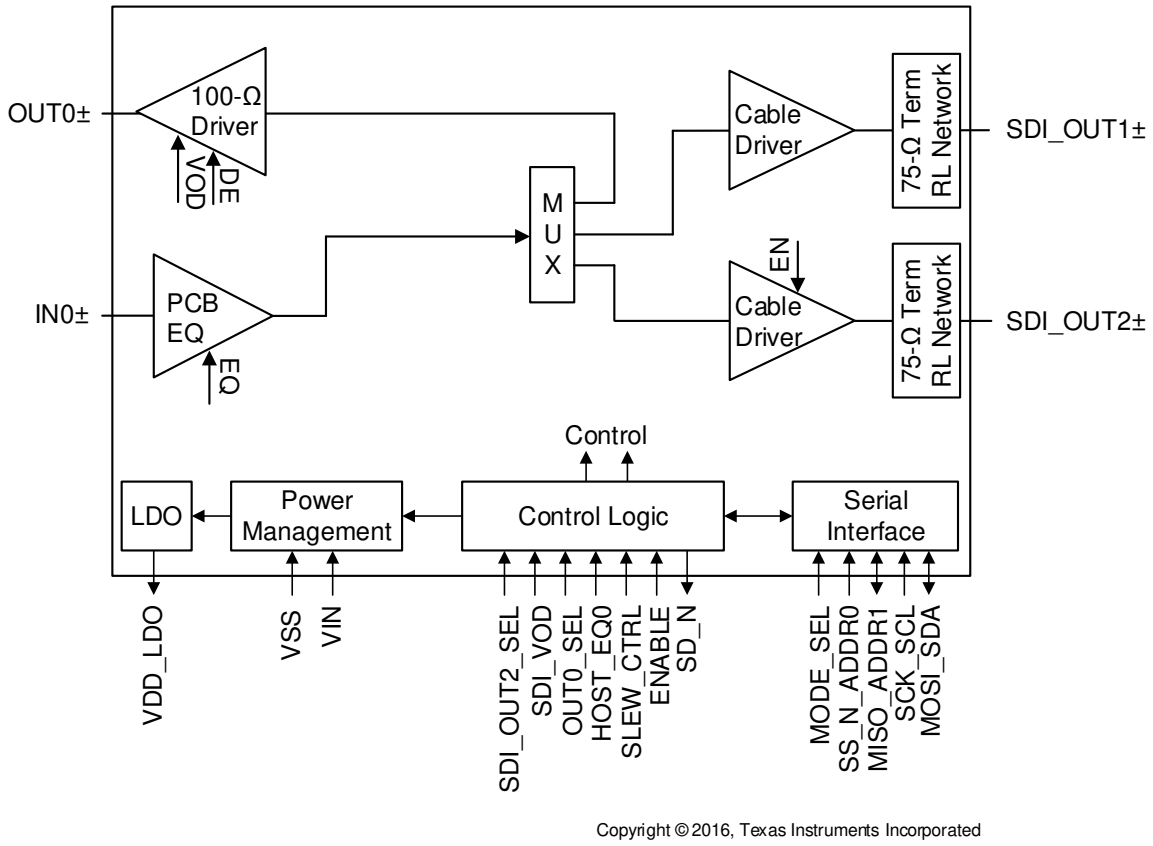


Figure 9. LMH1208 Block Diagram Overview

7.3 Feature Description

The LMH1208 data path consists of several key blocks as shown in the functional block diagram. These key blocks are:

- *4-Level Input Pins and Thresholds*
- *OUT0_SEL and SDI_OUT2_SEL Control*
- *Input Signal Detect*
- *Continuous Time Linear Equalizer (CTLE)*
- *Output Driver Control*
- *Status Indicators and Interrupts*

7.3.1 4-Level Input Pins and Thresholds

The 4-level input configuration pins use a resistor divider to provide four logic states for each control pin. There is an internal 30-kΩ pullup and a 60-kΩ pulldown connected to the control pin that sets the default voltage at 2/3 × VIN. These resistors, together with the external resistor, combine to achieve the desired voltage level. By using the 1-kΩ pulldown, 20-kΩ pulldown, no connect, and 1-kΩ pullup, the optimal voltage levels for each of the four input states are achieved as shown in Table 1.

Table 1. 4-Level Control Pin Settings

LEVEL	SETTING	NOMINAL PIN VOLTAGE
H	Tie 1 kΩ to VIN	VIN
F	Float (leave pin open)	2/3 × VIN
R	Tie 20 kΩ to VSS	1/3 × VIN
L	Tie 1 kΩ to VSS	0

Typical 4-Level Input Thresholds:

- Internal Threshold between L and R = 0.2 × VIN
- Internal Threshold between R and F = 0.5 × VIN
- Internal Threshold between F and H = 0.8 × VIN

7.3.2 OUT0_SEL and SDI_OUT2_SEL Control

The OUT0_SEL and SDI_OUT2_SEL pins select the LMH1208 data-path routes. Table 2 shows all possible signal path combinations and typical use cases for each configuration.

Table 2. LMH1208 Signal Path Combinations

OUT0_SEL	SDI_OUT2_SEL	INPUT	MAIN OUTPUT	LINE SIDE SECONDARY OUTPUT	HOST SIDE LOOP-BACK OUTPUT	TYPICAL APPLICATION
H	H	IN0±	SDI_OUT1±			Single cable driver
H	L	IN0±	SDI_OUT1±	SDI_OUT2±		Dual cable drivers
L	H	IN0±	SDI_OUT1±		OUT0±	Single cable driver with host-side loop-back enabled
L	L	IN0±	SDI_OUT1±	SDI_OUT2±	OUT0±	Dual cable drivers with host-side loop-back enabled

7.3.3 Input Signal Detect

IN0 has a signal detect circuit to monitor the presence or absence of an input signal. When the input signal amplitude for the selected input exceeds the signal detect assert threshold, the LMH1208 operates in normal operation mode.

In the absence of an input signal, the LMH1208 automatically goes into Power Save Mode to conserve power dissipation. When a valid signal is detected, the LMH1208 automatically exits Power Save Mode and returns to the normal operation mode. If the ENABLE pin is pulled low, the LMH1208 is forced into Power-Down Mode. In Power Save Mode, both the signal detect circuit and the serial interface remain active. In Power-Down Mode, only the serial interface remains active.

Users can monitor the status of the signal detect with the SD_N pin or through register programming.

Table 3. Input Signal Detect Modes of Operation

ENABLE	SIGNAL INPUT	OPERATING MODE
H	100-Ω signal input at IN0±	Normal operation Signal Detector at IN0± Serial interface active
H	No signal at IN0±	Power Save Mode Signal Detector at IN0± Serial interface active
L	Input signal ignored	Power-Down Mode Forced device power down Serial interface active

7.3.4 Continuous Time Linear Equalizer (CTLE)

The LMH1208 has a continuous time linear equalizer (CTLE) block for IN0. The CTLE compensates for frequency-dependent loss due to the transmission media prior to the device input. The CTLE accomplishes this by applying variable gain to the input signal, thereby boosting higher frequencies more than lower frequencies. The CTLE block extends the signal bandwidth, restores the signal amplitude, and reduces ISI caused by the transmission medium.

IN0 has an on-chip 100-Ω termination and is designed for AC coupling, requiring a 4.7-µF, AC-coupling capacitor for minimizing base-line wander. The PCB equalizer can compensate up to 20 inches of board trace at data rates up to 11.88 Gbps. There is one adapt mode for IN0: AM0 manual mode. In AM0 manual mode, fixed EQ boost settings are applied through user-programmable control.

The HOST_EQ0 pin determines the IN0 adapt mode and EQ boost level. For normal operation, HOST_EQ0 = F is recommended. HOST_EQ0 pin logic settings are shown in Table 4. These HOST_EQ0 pin settings can be overridden by register control. For more information, refer to the *LMH1228 and LMH1208 Programming Guide* (SNAU206).

Table 4. HOST_EQ0 Pin EQ Settings

HOST_EQ0 (1)	IN0± EQ BOOST	RECOMMENDED BOARD TRACE IN0± (2)
H, F	All Rates: AM0 Manual Mode, EQ=0x00	< 1 inch
R	All Rates: AM0 Manual Mode, EQ=0x80	10-15 inches
L	All Rates: AM0 Manual Mode, EQ=0x90	20 inches

(1) The HOST_EQ0 pin is also used to set OUT0 VOD and de-emphasis values. See *Host-Side 100-Ω Output Driver (OUT0±)* for more information.
(2) Recommended board trace at 11.88 Gbps.

7.3.5 Output Driver Control

7.3.5.1 Line-Side Output Cable Driver (SDI_OUT1+, SDI_OUT2+)

The LMH1208 has two output cable driver (CD) blocks, one for SDI_OUT1 and another for SDI_OUT2. These SDI outputs are designed to drive 75-Ω single-ended coaxial cables at data rates up to 11.88 Gbps. Both SDI_OUT1 and SDI_OUT2 feature an integrated 75-Ω termination and return loss compensation network for meeting stringent SMPTE return loss requirements (see Figure 8). The cable drivers are designed for AC coupling, requiring a 4.7-µF, AC-coupling capacitor for minimizing base-line wander due to the rare-occurring pathological bit pattern.

7.3.5.1.1 Output Amplitude (VOD)

SDI_OUT1 and SDI_OUT2 are designed for transmission across 75-Ω single-ended impedance. The nominal SDI cable driver output amplitude (VOD) is 800 mVp-p single-ended. In the presence of long output cable lengths or crosstalk, the SDI_VOD pin can be used to optimize the cable driver output with respect to the nominal amplitude. Table 5 details VOD settings that can be applied to both SDI_OUT1 and SDI_OUT2. The SDI_VOD pin can be overridden through register control. In addition, the nominal VOD amplitude can be changed by register control. For more information, refer to the *LMH1228 and LMH1208 Programming Guide* (SNAU206).

Table 5. SDI_VOD Settings for Line-Side Output Amplitude

SDI_VOD	DESCRIPTION
H	about +5% of nominal
F	800 mVp-p (nominal)
R	about +10% of nominal
L	about –5% of nominal

7.3.5.1.2 Output Pre-Emphasis

In addition to SDI cable driver VOD control, the LMH1208 can add pre-emphasis on the cable driver output to improve output signal integrity at a UHD (12G, 6G) or HD (3G, 1.5G) input data rate. By default, pre-emphasis is enabled based on the SLEW_CTRL pin setting shown in Table 6.

Table 6. SLEW_CTRL Settings for SDI_OUT1 and SDI_OUT2 Pre-Emphasis

SLEW_CTRL	OUTPUT PRE-EMPHASIS	DATA RATE
H	Enabled	UHD: 11.88 Gbps UHD: 5.94 Gbps
F	Disabled	HD: 2.97 Gbps HD: 1.485 Gbps
R, L	Disabled	SD: 270 Mbps

When enabled, the amount of pre-emphasis applied to cable driver outputs is determined by register control. When disabled, no pre-emphasis is applied. Pre-emphasis control can be overridden for select or all data rates through register control. For more information, refer to the *LMH1228 and LMH1208 Programming Guide* (SNAU206).

7.3.5.1.3 Output Slew Rate

SMPTE specifications require different output driver rise and fall times depending on the operating data rate. To meet these requirements, the output edge rate of SDI_OUT1 and SDI_OUT2 can be configured by the SLEW_CTRL pin. Table 7 shows the recommended SLEW_CTRL pin logic setting and typical edge rate at the cable driver output for each data rate.

Table 7. SLEW_CTRL Settings for SDI_OUT1 and SDI_OUT2 Output Edge Rate

SLEW_CTRL	DATA RATE	CABLE DRIVER OUTPUT EDGE RATE (TYP)
H	11.88 Gbps	34 ps
	5.94 Gbps	36 ps
F	2.97 Gbps	59 ps
	1.485 Gbps	60 ps
R, L	270 Mbps	550 ps

Users can also program the desired edge rate manually through register control. For more information, refer to the *LMH1228 and LMH1208 Programming Guide* (SNAU206).

7.3.5.1.4 Output Polarity Inversion

Polarity inversion is supported on both SDI_OUT1 and SDI_OUT2 outputs through register control.

7.3.5.2 Host-Side 100-Ω Output Driver (OUT0±)

OUT0 is a 100-Ω driver output. OUT0 serves as a host-side loop-back output. OUT0 also supports polarity inversion.

The driver offers users the capability to select higher output amplitude and de-emphasis levels for longer board trace that connects the drivers to their downstream receivers. Driver de-emphasis provides transmitter equalization to reduce the ISI caused by the board trace.

The VOD and de-emphasis levels for OUT0 are set by default to 570 mVp-p and –0.4 dB, and these values are recommended for driving 1-2 inches of board trace from OUT0± at 11.88 Gbps. These settings can be changed through register control if desired. When these parameters are controlled by registers, the VOD and de-emphasis levels can be programmed independently. For more information, refer to the *LMH1228 and LMH1208 Programming Guide* (SNAU206).

7.3.6 Status Indicators and Interrupts

The SD_N pin is a 3.3-V tolerant, active-low, open-drain output. An external resistor to the logic supply is required. The SD_N pin can be configured to indicate input signal detect or an interrupt event.

7.3.6.1 SD_N (Signal Detect)

By default, SD_N indicates a SD_N (signal detect) event, and this pin asserts low after a valid signal is detected by the IN0 signal detect circuit. For more information about how to reconfigure the SD_N pin functionality, refer to the *LMH1228 and LMH1208 Programming Guide* (SNAU206).

7.3.6.2 INT_N (Interrupt)

The SD_N pin can be configured to indicate an INT_N (interrupt) event. When configured as an INT_N output, the pin asserts low when an interrupt occurs, according to the programmed interrupt masks. Two separate masks can be programmed through register control as interrupt sources:

- If there is a loss of signal (LOS) event on IN0 (2 separate masks).

INT_N is a sticky bit, meaning that it will flag after an interrupt occurs and will not clear until read-back. Once the Interrupt Status Register is read, the INT_N pin will assert high again. For more information about how to configure the SD_N pin for INT_N functionality, refer to the *LMH1228 and LMH1208 Programming Guide* (SNAU206).

7.4 Device Functional Modes

The LMH1208 operates in one of two modes: System Management Bus (SMBus) or Serial Peripheral Interface (SPI) mode. To determine the mode of operation, the proper setting must be applied to the MODE_SEL pin at power up, as detailed in Table 8.

Table 8. MODE_SEL Pin Settings

LEVEL	DESCRIPTION
H	Reserved for factory testing – do not use
F	Selects SPI Interface for register access
R	Reserved for factory testing – do not use
L	Selects SMBus Interface for register access

7.4.1 System Management Bus (SMBus) Mode

The SMBus interface can also be used to control the device. If MODE_SEL = Low (1 kΩ to VSS), Pins 13 and 29 are configured as SDA and SCL. Pins 11 and 28 are address straps ADDR0 and ADDR1 during power up. The maximum operating speed supported on the SMBUS pins is 400 kHz.

Table 9. SMBus Device Slave Addresses(1)

ADDR0 (LEVEL)	ADDR1 (LEVEL)	7-BIT SLAVE ADDRESS [HEX]	8-BIT WRITE COMMAND [HEX]
L	L	2D	5A
L	R	2E	5C
L	F	2F	5E
L	H	30	60
R	L	31	62
R	R	32	64
R	F	33	66
R	H	34	68
F	L	35	6A
F	R	36	6C
F	F	37	6E
F	H	38	70
H	L	39	72
H	R	3A	74
H	F	3B	76
H	H	3C	78

(1) The 8-bit write command consists of the 7-bit slave address (Bits 7:1) with 0 appended to the LSB to indicate an SMBus write. For example, if the 7-bit slave address is 0x2D (010 1101'b), the 8-bit write command is 0x5A (0101 1010'b).

7.4.1.1 SMBus Read and Write Transaction

SMBus is a two-wire serial interface through which various system component chips can communicate with the master. Slave devices are identified by having a unique device address. The two-wire serial interface consists of SCL and SDA signals. SCL is a clock output from the master to all of the slave devices on the bus. SDA is a bidirectional data signal between the master and slave devices. The LMH1208 SMBus SCL and SDA signals are open-drain and require external pullup resistors.

Start and Stop:

The master generates Start and Stop patterns at the beginning and end of each transaction.

- Start: High-to-low transition (falling edge) of SDA while SCL is high.
- Start: High-to-low transition (falling edge) of SDA while SCL is high.

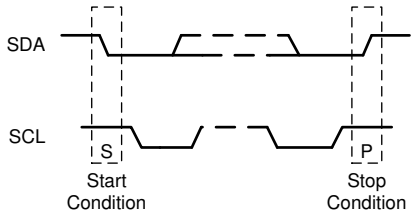


Figure 10. Start and Stop Conditions

The master generates nine clock pulses for each byte transfer. The 9th clock pulse constitutes the ACK cycle. The transmitter releases SDA to allow the receiver to send the ACK signal. An ACK is recorded when the device pulls SDA low, while a NACK is recorded if the line remains high.

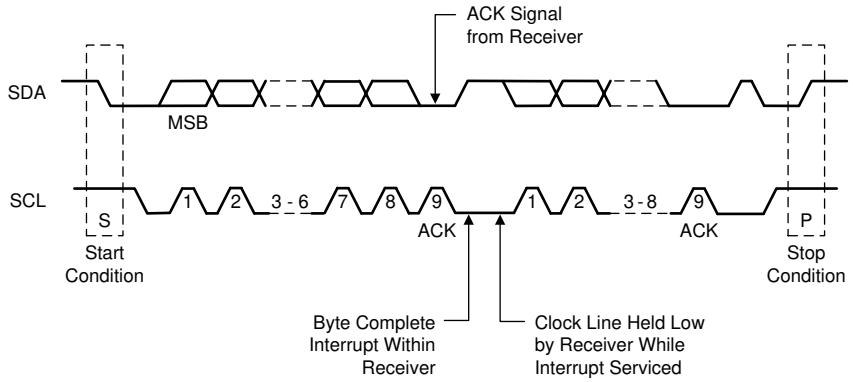


Figure 11. Acknowledge (ACK)

7.4.1.1.1 SMBus Write Operation Format

Writing data to a slave device consists of three parts, as illustrated in Figure 12:

1. The master begins with a start condition followed by the slave device address with the R/$\overline{W}$ bit set to 0’b.
2. After an ACK from the slave device, the 8-bit register word address is written.
3. After an ACK from the slave device, the 8-bit data is written, followed by a stop condition.

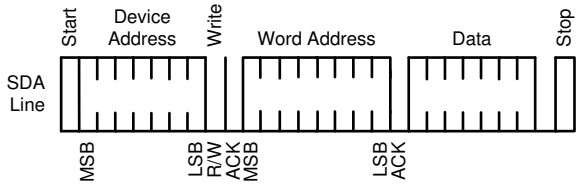


Figure 12. SMBus Write Operation

7.4.1.1.2 SMBus Read Operation Format

SMBus read operation consists of four parts, as illustrated in Figure 13:

1. The master begins with a start condition, followed by the slave device address with the R/$\overline{W}$ bit set to 0'b.
2. After an ACK from the slave device, the 8-bit register word address is written.
3. After an ACK from the slave device, the master initiates a restart condition, followed by the slave address with the R/$\overline{W}$ bit set to 1'b.
4. After an ACK from the slave device, the 8-bit data is read-back. The last ACK is high if there are no more bytes to read, and the last read is followed by a stop condition.

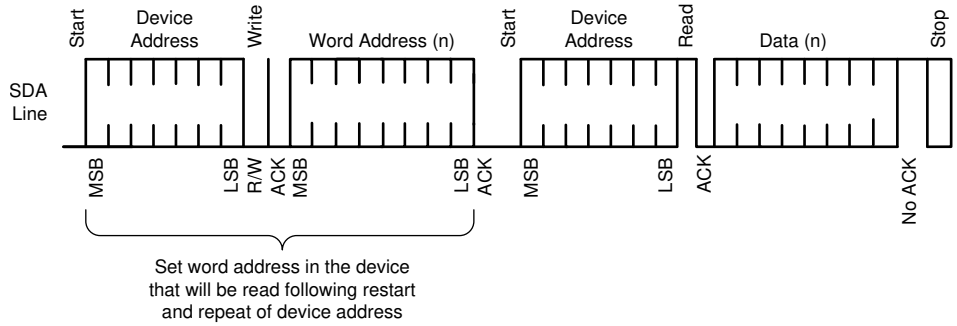


Figure 13. SMBus Read Operation

7.4.2 Serial Peripheral Interface (SPI) Mode

If MODE_SEL = F or H, the LMH1208 is in SPI mode. In SPI mode, the following pins are used for SPI bus communication:

- MOSI (Pin 13): Master Output Slave Input
- MISO (Pin 28): Master Input Slave Output
- SS_N (Pin 11): Slave Select (Active Low)
- SCK (Pin 29): Serial Clock (Input to the LMH1208 Slave Device)

7.4.2.1 SPI Read and Write Transactions

Each SPI transaction to a single device is 17 bits long and is framed by SS_N when asserted low. The MOSI input is ignored, and the MISO output is floated whenever SS_N is deasserted (high).

The bits are shifted in left-to-right. The first bit is R/$\overline{W}$, which is 1'b for *read* and 0'b for *write*. Bits A7-A0 are the 8-bit register address, and bits D7-D0 are the 8-bit read or write data. The previous SPI command, address, and data are shifted out on MISO as the current command, address, and data are shifted in on MOSI. In all SPI transactions, the MISO output signal is enabled asynchronously when SS_N asserts low. The contents of a single MOSI or MISO transaction frame are shown in Figure 14.

Figure 14. 17-Bit Single SPI Transaction Frame

R/W	A7	A6	A5	A4	A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0

7.4.2.2 SPI Write Transaction Format

For SPI writes, the R/W bit is 0'b. SPI write transactions are 17 bits per device, and the command is executed on the rising edge of SS_N. The SPI transaction always starts on the rising edge of the clock.

The signal timing for a SPI Write transaction is shown in Figure 2. The *prime* values on MISO (for example, A7') reflect the contents of the shift register from the previous SPI transaction and are listed as don't care for the current transaction.

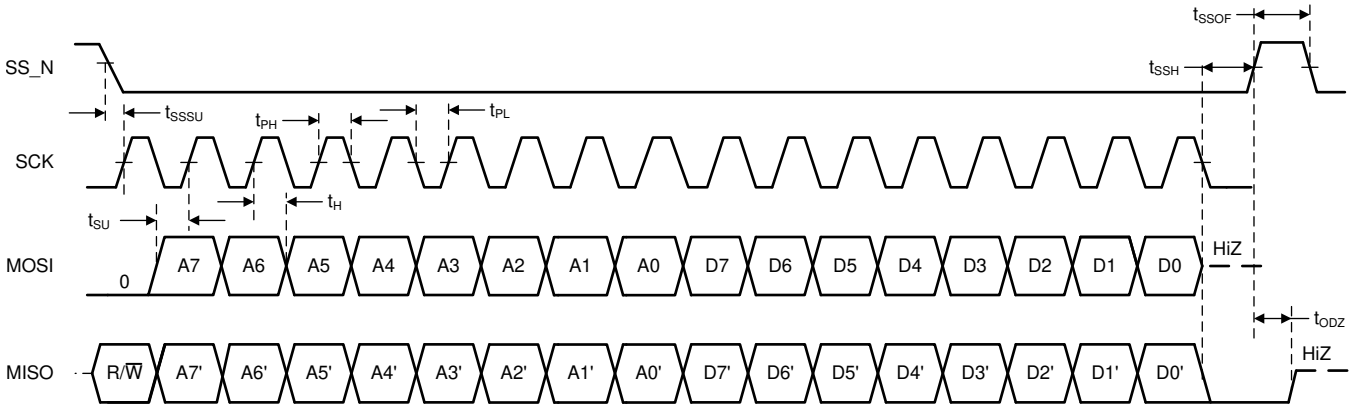


Figure 15. Signal Timing for a SPI Write Transaction

7.4.2.3 SPI Read Transaction Format

A SPI read transaction is 34 bits per device and consists of two 17-bit frames. The first 17-bit read transaction frame shifts in the address to be read, followed by a dummy transaction second frame to shift out 17-bit read data. The R/W bit is 1'b for the read transaction, as shown in Figure 3.

The first 17 bits from the read transaction specifies 1-bit of R/W and 8-bits of address A7-A0 in the first 8 bits. The eight 1's following the address are ignored. The second dummy transaction acts like a read operation on address 0xFF and needs to be ignored. However, the transaction is necessary in order to shift out the read data D7-D0 in the last 8 bits of the MISO output. As with the SPI Write, the *prime* values on MISO during the first 16 clocks are listed as don't care for this portion of the transaction. The values shifted out on MISO during the last 17 clocks reflect the read address and 8-bit read data for the current transaction.

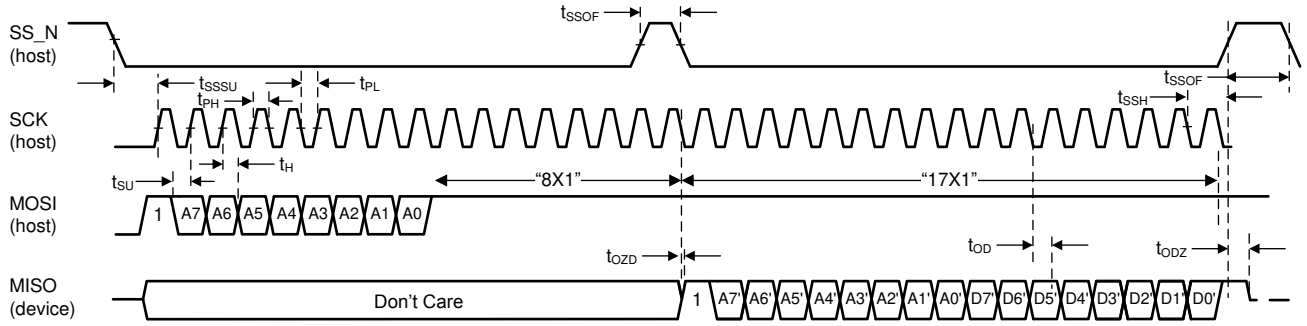


Figure 16. Signal Timing for a SPI Read Transaction

7.4.2.4 SPI Daisy Chain

The LMH1208 supports SPI daisy-chaining among multiple devices, as shown in Figure 17.

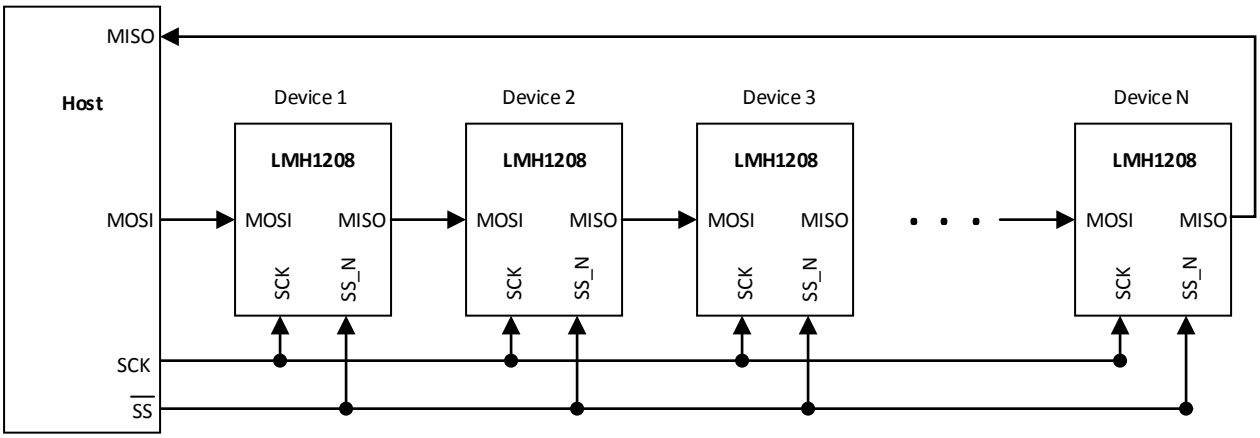


Figure 17. Daisy-Chain Configuration

Each LMH1208 device is directly connected to the SCK and SS_N pins of the host. The first LMH1208 device in the chain is connected to the host's MOSI pin, and the last device in the chain is connected to the host's MISO pin. The MOSI pin of each intermediate LMH1208 device in the chain is connected to the MISO pin of the previous LMH1208 device, thereby creating a serial shift register. In a daisy-chain configuration of N × LMH1208 devices, the host conceptually sees a shift register of length 17 × N for a basic SPI transaction, during which SS_N is asserted low for 17 × N clock cycles.

7.5 Register Maps

The LMH1208 register map is divided into three register pages. These register pages are used to control different aspects of the LMH1208 functionality. A brief summary of the pages is shown below:

1. **Share Register Page:** This page corresponds to global parameters, such as LMH1208 device ID and SD_N status configuration. This is the default page at start-up. Access this page by setting Reg 0xFF[2:0] = 000'b.
2. **CTLE Register Page:** This page corresponds to IN0 PCB CTLE, output mux settings, and output interrupt overrides. Access this page by setting Reg 0xFF[2:0] = 100'b.
3. **Driver Register Page:** This page corresponds to OUT0, SDI_OUT1, and SDI_OUT2 driver output settings. Access this page by setting Reg 0xFF[2:0] = 101'b.

For the complete register map, typical device configurations, and proper register reset sequencing, refer to the *LMH1228 and LMH1208 Programming Guide* (SNAU206).

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

8.1.1 SMPTE Requirements and Specifications

SMPTE specifies several key requirements for the Serial Digital Interface to transport digital video over coaxial cables. Such requirements include return loss, AC coupling, and data rate dependency with rise and fall times.

1. **Return Loss:** This specification details how closely the port resembles 75-Ω impedance across a specified frequency band. The LMH1208 features a built-in 75-Ω return-loss network on SDI_OUT1 and SDI_OUT2 to minimize parasitics and improve overall signal integrity.
2. **AC Coupling:** AC-coupling capacitors are required for transporting uncompressed serial data streams with heavy low-frequency content. The use of 4.7-µF, AC-coupling capacitors is recommended to avoid low-frequency DC wander.
3. **Rise/Fall Time:** Output 75-Ω signals are required to meet certain rise and fall timing depending on the data rate. This improves the eye opening observed for the receiving device. The LMH1208 SDI_OUT1 and SDI_OUT2 cable drivers feature programmable edge rate adjustment to meet SMPTE rise and fall time requirements.

TI recommends placing the LMH1208 as close as possible to the 75-Ω BNC ports to meet SMPTE specifications.

8.1.2 LMH1208 and LMH1228 Compatibility

The LMH1208 is pin-compatible with the LMH1228 (12G UHD-SDI Dual Output Cable Driver with Integrated Reclocker) when LMH1208 RSV_L pin is tied to 2.5 V. This pin compatibility allows users to upgrade easily to the LMH1228. See Figure 18 for details.

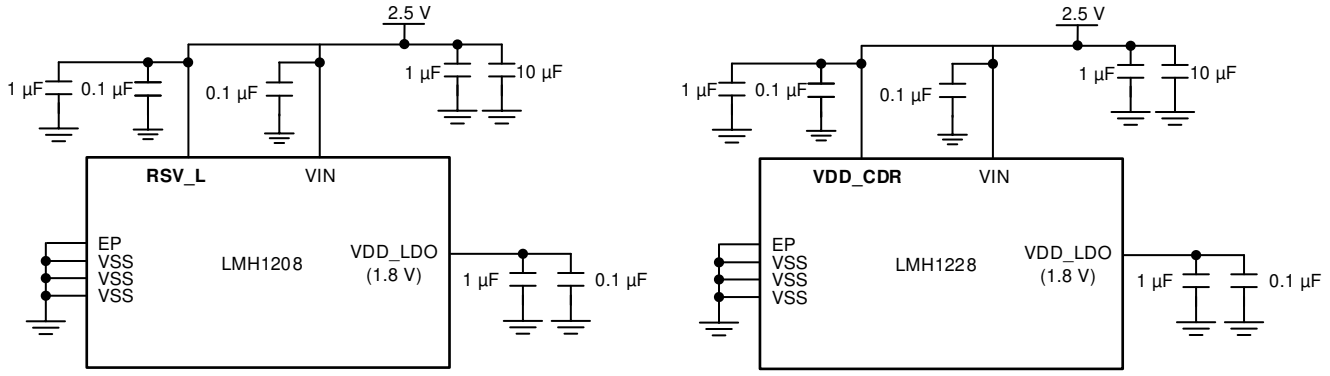


Figure 18. Pin Connections for LMH1208 and LMH1228 Compatibility

8.2 Typical Applications

The LMH1208 is a dual cable driver that supports SDI data rates up to 11.88 Gbps. Figure 19 shows a typical application circuit for the LMH1208.

Specific examples of typical applications for the LMH1208 as a dual cable driver and distribution amplifier are detailed in the following subsections.

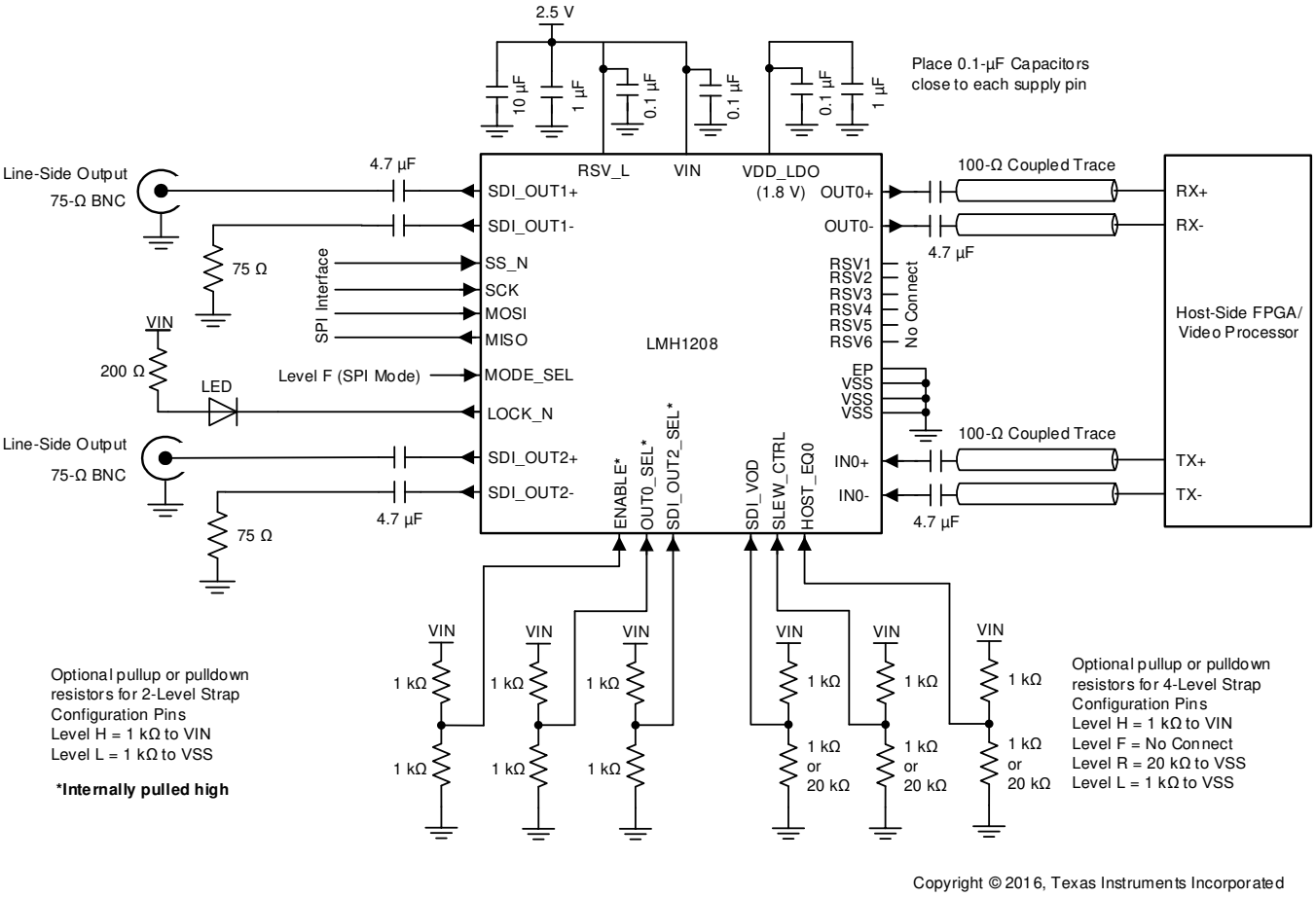


Figure 19. LMH1208 Typical Application Circuit

Typical Applications (continued)

8.2.1 Dual Cable Driver

The LMH1208 can be configured as a dual cable driver to route the same SDI output signal to multiple receivers. In this configuration, the LMH1208 is programmed to equalize 100-Ω SDI input data at IN0 and uses the dual cable drivers at SDI_OUT1 and SDI_OUT2 to drive out the SDI signal.

Figure 20 shows a typical application of an LMH1208 as a dual cable driver output. In this example, the LMH1219 Cable EQ with Integrated Reclocker provides an SDI input to the SDI FPGA. The FPGA then sends post-processed SDI data to the IN0 of the LMH1208, which drives the data on cable driver outputs SDI_OUT1 and SDI_OUT2.

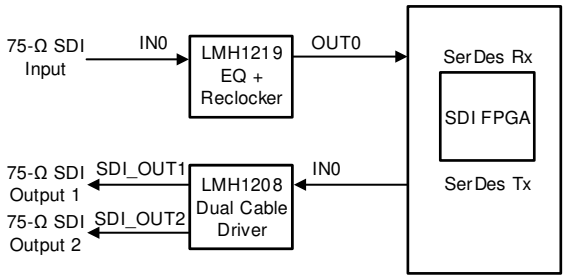


Figure 20. LMH1208 Dual Cable Driver Application

8.2.1.1 Design Requirements

For general LMH1208 design requirements, reference the guidelines in Table 10.

For dual cable driver application-specific requirements, reference the guidelines in Table 11.

Table 10. LMH1208 General Design Requirements

DESIGN PARAMETER	REQUIREMENTS
SDI_OUT1+, SDI_OUT2+ AC-coupling capacitors	4.7-µF capacitors recommended
SDI_OUT1–, SDI_OUT2– AC-coupling capacitors	4.7-µF capacitors recommended, AC terminated with 75 Ω to VSS.
IN0± and OUT0± AC-coupling capacitors	4.7-µF capacitors recommended
Input and output terminations	Input and output terminations provided internally. Do **not** add external terminations.
DC power supply decoupling capacitors	10-µF and 1-µF bulk capacitors; place close to each device. 0.1-µF capacitor; place close to each supply pin.
VDD_LDO decoupling capacitors	1-µF and 0.1-µF capacitors; place as close as possible to the device VDD_LDO pin.
MODE_SEL pin	SPI: Leave MODE_SEL unconnected (Level F) SMBus: Connect 1 kΩ to VSS (Level L)

Table 11. LMH1208 Dual Cable Driver Requirements

DESIGN PARAMETER	REQUIREMENTS
OUT0_SEL pin	1 kΩ to VIN (Level H) to disable the OUT0 loop-back output
SDI_OUT2_SEL pin	1 kΩ to VSS (Level L) to enable SDI_OUT2 as secondary cable output

8.2.1.2 Detailed Design Procedure

The design procedure for dual cable driver applications is as follows:

1. Select a power supply that meets the DC and AC requirements in *Recommended Operating Conditions*.
2. Choose a small 0402 surface mount ceramic capacitor for AC-coupling capacitors to maintain characteristic impedance.
3. Choose a high-quality, 75-Ω BNC connector that is capable of supporting 11.88-Gbps applications. Consult a BNC supplier regarding insertion loss, impedance specifications, and recommended footprint for meeting

SMPTE return loss.

4. Follow detailed high-speed layout recommendations provided in *Layout Guidelines* to ensure optimal signal quality when interconnecting 75-Ω and 100-Ω signals to the LMH1208.
5. Determine whether SPI or SMBus communication is necessary. If the LMH1208 must be programmed with settings other than what is offered by pin control, users must use SPI or SMBus Mode for additional programming.
6. Configure OUT0_SEL and SDI_OUT2_SEL pins according to the desired default use case.
7. Tune the SDI_VOD output amplitude control pin for optimal signal quality depending on the cable length attached at SDI_OUT1+ and SDI_OUT2+. Use register control for more tuning options, if necessary.

8.2.1.3 Application Curves

The LMH1208 performance on SDI_OUT1+ and SDI_OUT2+ was measured with the test setups shown in Figure 21 and Figure 22.

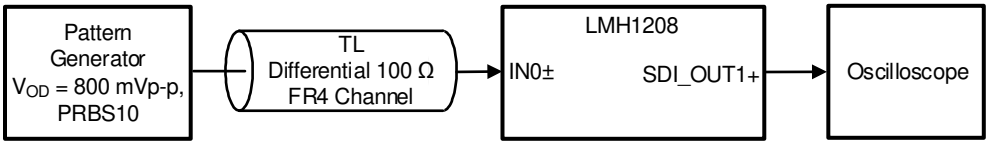


Figure 21. Test Setup for LMH1208 to SDI_OUT1+

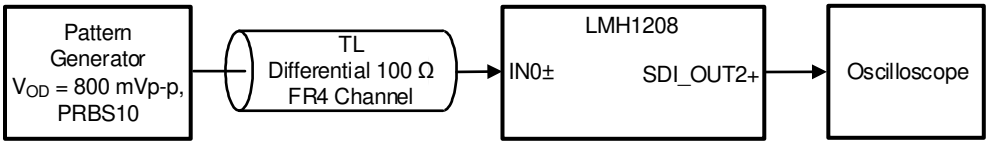
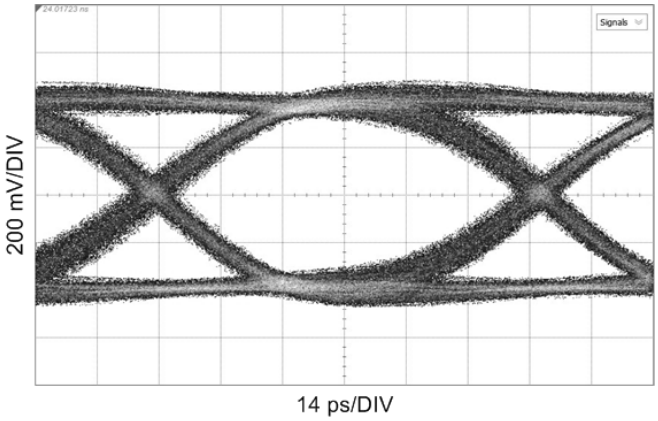


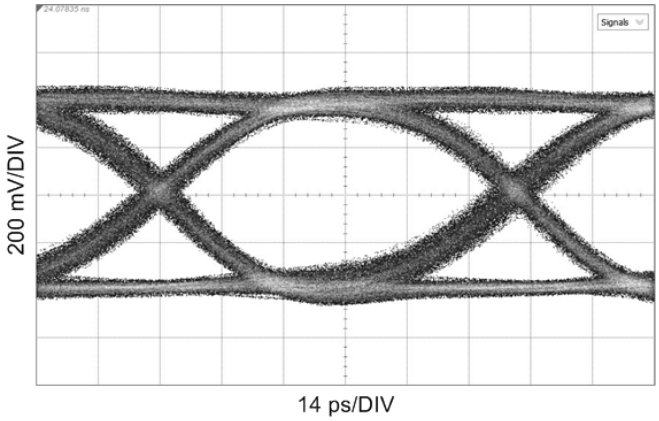
Figure 22. Test Setup for LMH1208 to SDI_OUT2+

The eye diagrams in this subsection show how the LMH1208 improves overall signal integrity in the data path for 100-Ω differential FR4 PCB trace at IN0±.



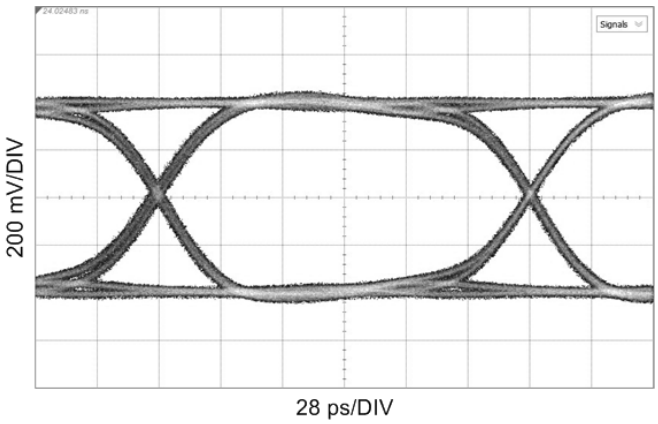
Measured at SDI_OUT1+
HOST_EQ0 = H, SDI_OUT2_SEL = L, SLEW_CTRL = H

Figure 23. 11.88 Gbps, TL = 1" FR4



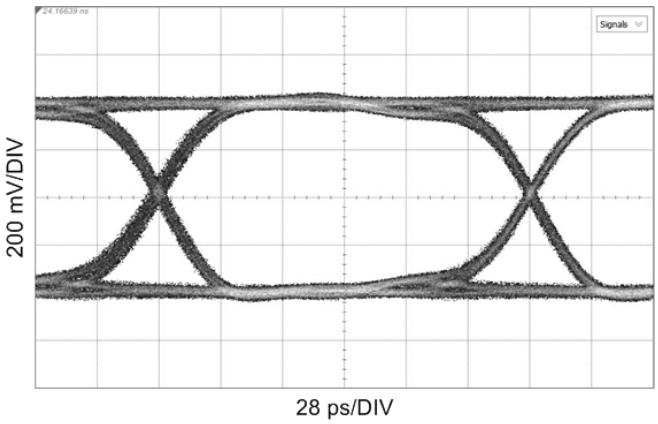
Measured at SDI_OUT2+
HOST_EQ0 = H, SDI_OUT2_SEL = L, SLEW_CTRL = H

Figure 24. 11.88 Gbps, TL = 1" FR4



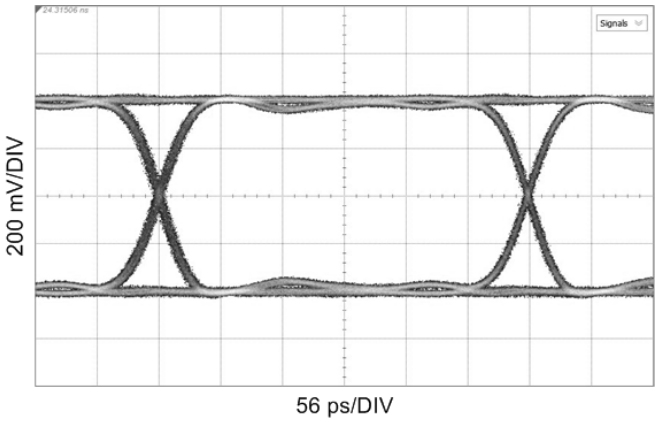
Measured at SDI_OUT1+
HOST_EQ0 = H, SDI_OUT2_SEL = L, SLEW_CTRL = H

Figure 25. 5.94 Gbps, TL = 1" FR4



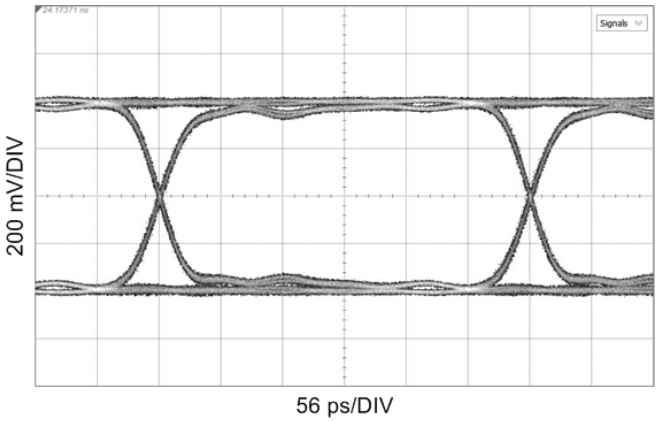
Measured at SDI_OUT2+
HOST_EQ0 = H, SDI_OUT2_SEL = L, SLEW_CTRL = H

Figure 26. 5.94 Gbps, TL = 1" FR4



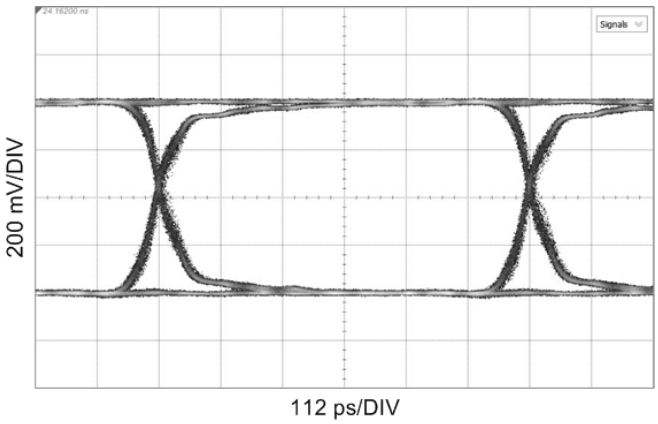
Measured at SDI_OUT1+
HOST_EQ0 = H, SDI_OUT2_SEL = L, SLEW_CTRL = F

Figure 27. 2.97 Gbps, TL = 1" FR4



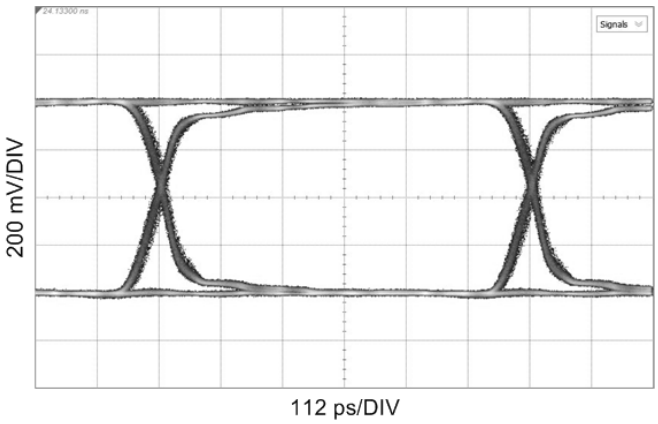
Measured at SDI_OUT2+
HOST_EQ0 = H, SDI_OUT2_SEL = L, SLEW_CTRL = F

Figure 28. 2.97 Gbps, TL = 1" FR4



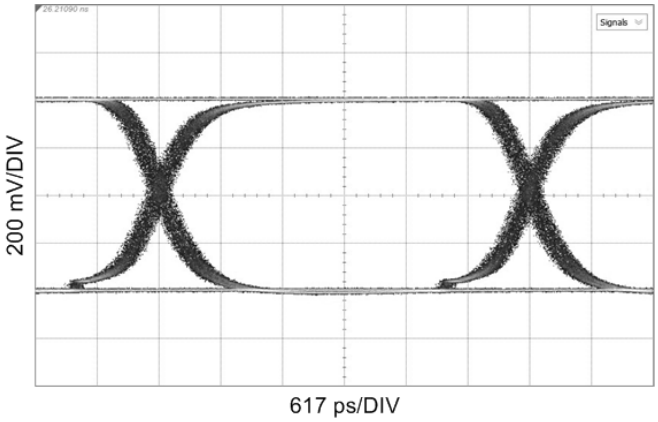
Measured at SDI_OUT1+
HOST_EQ0 = H, SDI_OUT2_SEL = L, SLEW_CTRL = F

Figure 29. 1.485 Gbps, TL = 1" FR4



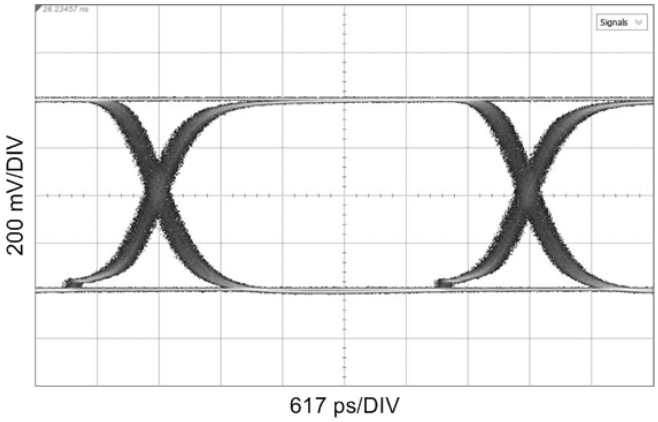
Measured at SDI_OUT2+
HOST_EQ0 = H, SDI_OUT2_SEL = L, SLEW_CTRL = F

Figure 30. 1.485 Gbps, TL = 1" FR4



Measured at SDI_OUT1+
HOST_EQ0 = H, SDI_OUT2_SEL = L, SLEW_CTRL = L

Figure 31. 270 Mbps, TL = 1" FR4



Measured at SDI_OUT2+
HOST_EQ0 = H, SDI_OUT2_SEL = L, SLEW_CTRL = L

Figure 32. 270 Mbps, TL = 1" FR4

8.2.2 Distribution Amplifier

The LMH1208 can be configured as a distribution amplifier to distribute the same SDI input signal to multiple cable driver outputs. In this configuration, the LMH1208 uses the dual cable drivers at SDI_OUT1 and SDI_OUT2 to drive out the SDI signal seen at IN0. Meanwhile, the loop-back output on OUT0 is daisy-chained as a duplicate input to IN0 of the next LMH1208.

Figure 33 shows a typical application where four LMH1208s are used in combination with an LMH1219 Cable EQ with Integrated Reclocker to form a 1:8 distribution amplifier network.

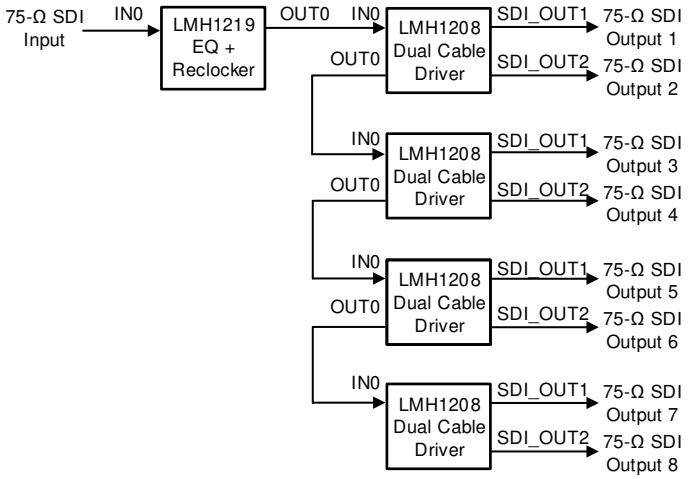


Figure 33. LMH1208 Distribution Amplifier Application

8.2.2.1 Design Requirements

See Table 10 in *Dual Cable Driver Design Requirements* for general LMH1208 design requirements.

For distribution amplifier application-specific requirements, reference the guidelines in Table 12.

Table 12. LMH1208 Distribution Amplifier Requirements

DESIGN PARAMETER	REQUIREMENTS
OUT0_SEL pin	1 kΩ to VSS (Level L) to enable OUT0 as a loop-back output to the next LMH1208 IN0 input
SDI_OUT2_SEL pin	1 kΩ to VSS (Level L) to enable SDI_OUT2 as secondary cable output

8.2.2.2 Detailed Design Procedure

See *Dual Cable Driver Detailed Design Procedure* and follow Steps 1 through 5. Refer to the additional steps below for distribution amplifier applications.

1. Configure OUT0_SEL and SDI_OUT2_SEL pins according to the desired default use case.
2. Tune the output VOD and de-emphasis level for the 100-Ω driver prior to each LMH1208 IN0±. In the distribution amplifier example shown in Figure 33, this step applies to the LMH1219 OUT0± driver and all LMH1208 OUT0± drivers that are daisy-chained to a subsequent LMH1208 IN0±. If OUT0± is located within 1-2 inches of IN0±, then use a lower VOD setting and no de-emphasis. If the OUT0± is located many inches away from IN0±, some VOD gain and de-emphasis may be required at OUT0± for the IN0 CTLE to equalize optimally. Use register control for more tuning options if necessary.
3. Tune the SDI_VOD output amplitude control pin for optimal signal quality depending on the cable length attached at SDI_OUT1+ and SDI_OUT2+ for each LMH1208. Use register control for more tuning options, if necessary.

8.2.2.3 Application Curves

The LMH1208 performance on OUT0± was measured with the test setup shown in Figure 21.

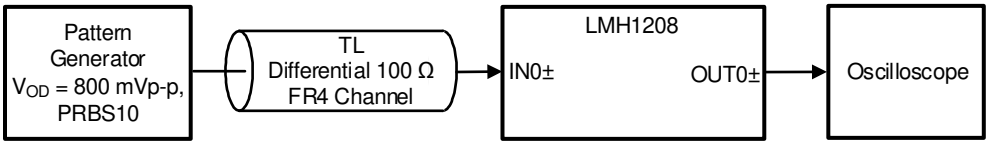
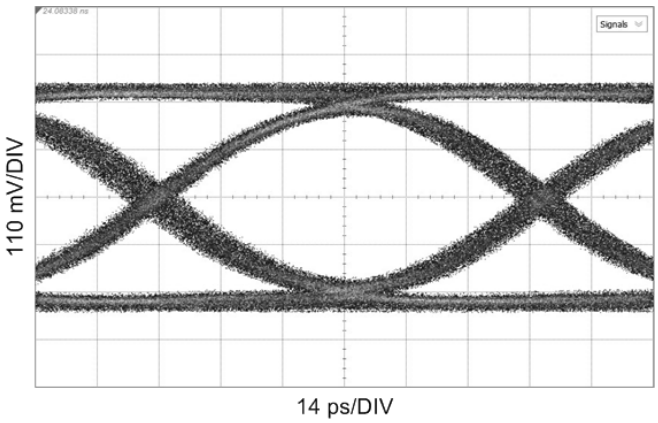


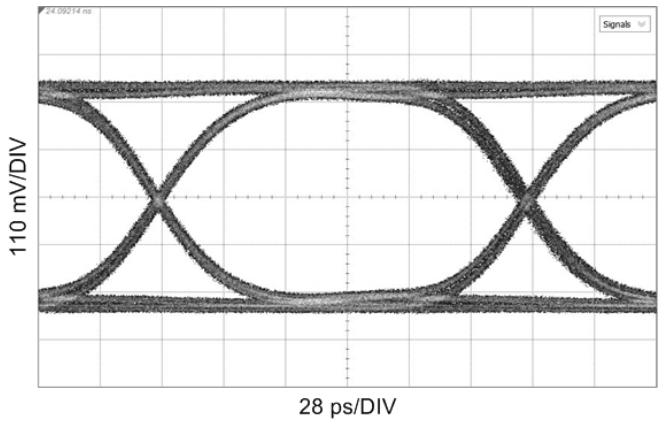
Figure 34. Test Setup for LMH1208 to OUT0±

The eye diagrams in this subsection show how the LMH1208 improves overall signal integrity in the data path for 100-Ω differential FR4 PCB trace at IN0±.



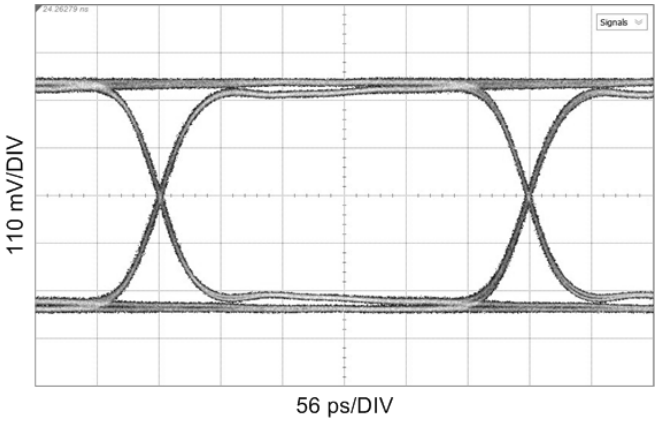
Measured at OUT0±
HOST_EQ0 = H, SDI_OUT2_SEL = L, SLEW_CTRL = H

Figure 35. 11.88 Gbps, TL = 1" FR4



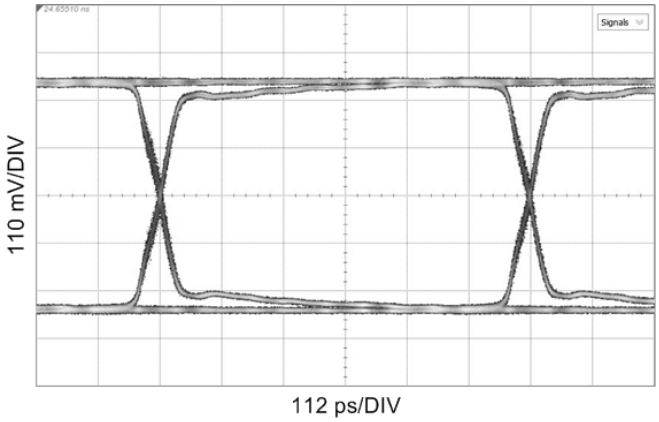
Measured at OUT0±
HOST_EQ0 = H, SDI_OUT2_SEL = L, SLEW_CTRL = H

Figure 36. 5.94 Gbps, TL = 1" FR4



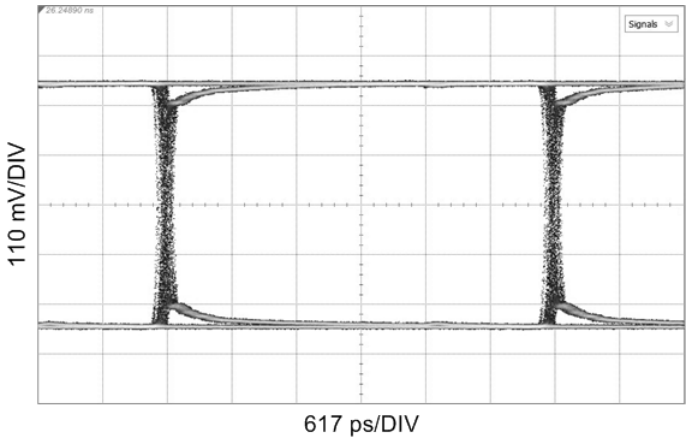
Measured at OUT0±
HOST_EQ0 = H, SDI_OUT2_SEL = L, SLEW_CTRL = F

Figure 37. 2.97 Gbps, TL = 1" FR4



Measured at OUT0±
HOST_EQ0 = H, SDI_OUT2_SEL = L, SLEW_CTRL = F

Figure 38. 1.485 Gbps, TL = 1" FR4



Measured at OUT0±
HOST_EQ0 = H, SDI_OUT2_SEL = L, SLEW_CTRL = L

Figure 39. 270 Mbps, TL = 1" FR4

9 Power Supply Recommendations

The LMH1208 requires decoupling capacitors to ensure a stable power supply. For power supply decoupling, 0.1-μF surface-mount ceramic capacitors must be placed close to each RSV_L, VDD_LDO and VIN supply pin to VSS. Larger bulk capacitors (for example, 10 μF and 1 μF) are recommended for RSV_L and VIN.

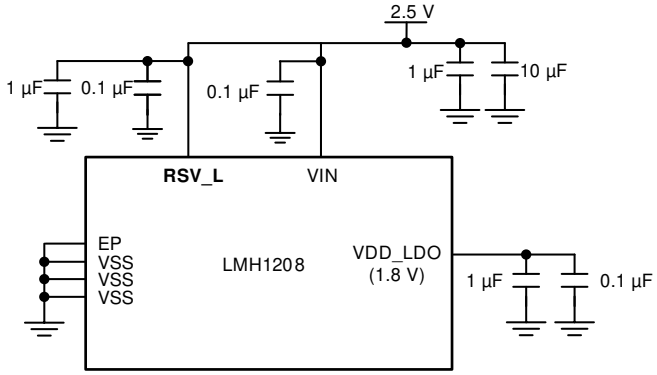


Figure 40. Recommended Power Supply Decoupling

Good supply bypassing requires low inductance capacitors. This can be achieved through an array of multiple small body size surface-mount bypass capacitors to keep low supply impedance. Better results can be achieved through the use of a buried capacitor formed by a VDD and VSS plane separated by 2 to 4 mil dielectric in a printed-circuit board.

10 Layout

10.1 Layout Guidelines

The following guidelines are recommended to optimize the board layout for the LMH1208.

10.1.1 Board Stack-Up and Ground References

- Choose a suitable board stack-up that supports 75-Ω single-ended trace and 100-Ω differential trace routing on the top layer of the board. This is typically done with a Layer-2 ground plane reference for the 100-Ω differential traces and a Layer-3 ground plane reference for the 75-Ω single-end traces.
- Maintain a distance of at least 5 times the trace width between signal trace and ground reference if they are on the same layer. This prevents unwanted changes in the characteristic impedance.
- Maintain a consistent ground plane reference for each high-speed trace from source to end-point. Ground reference discontinuities lead to characteristic impedance mismatch.

10.1.2 High-Speed PCB Trace Routing and Coupling

Observe the following general high-speed recommendations for high-speed trace routing:

- For differential pairs, maintain a uniform width and gap for each differential pair where possible. When traces must diverge (for example, due to AC-coupling capacitors), ensure that the traces branch out or merge uniformly.
- To prevent reflections due to trace routing, ensure that trace bends are at most 45°. Right angle bends should be implemented with at least two 45° corners. Radial bends are ideal.
- Avoid using signal vias. If signal vias must be used, a return path (GND) via must be placed near the signal via to provide a consistent ground reference and minimize impedance discontinuities.
- Avoid via stubs by back-drilling as necessary.

SDI_OUT1± and SDI_OUT2±:

- Use an uncoupled trace with 75-Ω single-ended impedance for signal routing to SDI_OUT1± and SDI_OUT2±.
- The trace width is typically 8 to 10 mils with reference to a Layer-3 ground plane.

IN0± and OUT0±:

- Use coupled traces with 100-Ω differential impedance for signal routing to IN0± and OUT0±.
- The trace width is typically 5 to 8 mils with reference to a Layer-2 ground plane.

10.1.3 Anti-Pads

- Place anti-pads (ground relief) on the power and ground planes directly under the 4.7-µF, AC-coupling capacitor and IC landing pads to minimize parasitic capacitance. The size of the anti-pad and the number of layers to use the anti-pad depend on the board stack-up and can be determined by a 3-dimension electromagnetic simulation tool.

10.1.4 BNC Connector Layout and Routing

- Use a well-designed BNC footprint to ensure the BNC's signal landing pad achieves 75-Ω characteristic impedance. BNC suppliers usually provide recommendations on BNC footprint for best results.
- Keep trace length short between the BNC and SDI_OUT1±. The trace routing for SDI_OUT1+ and SDI_OUT1– should be as symmetrical as possible, with approximately equal lengths and equal loading. The same is true for SDI_OUT2+ and SDI_OUT2–.

10.1.5 Power Supply and Ground Connections

- Connect each supply pin (RSV_L, VIN, VDD_LDO) directly to the power or ground planes with a short via. The via is usually placed tangent to the supply pins' landing pads with the shortest trace possible.
- Power supply decoupling capacitors should be a small physical size (0402 or smaller) and placed close to the supply pins to minimize inductance. The capacitors are commonly placed on the bottom layer and share the ground of the EP (Exposed Pad).

Layout Guidelines (continued)

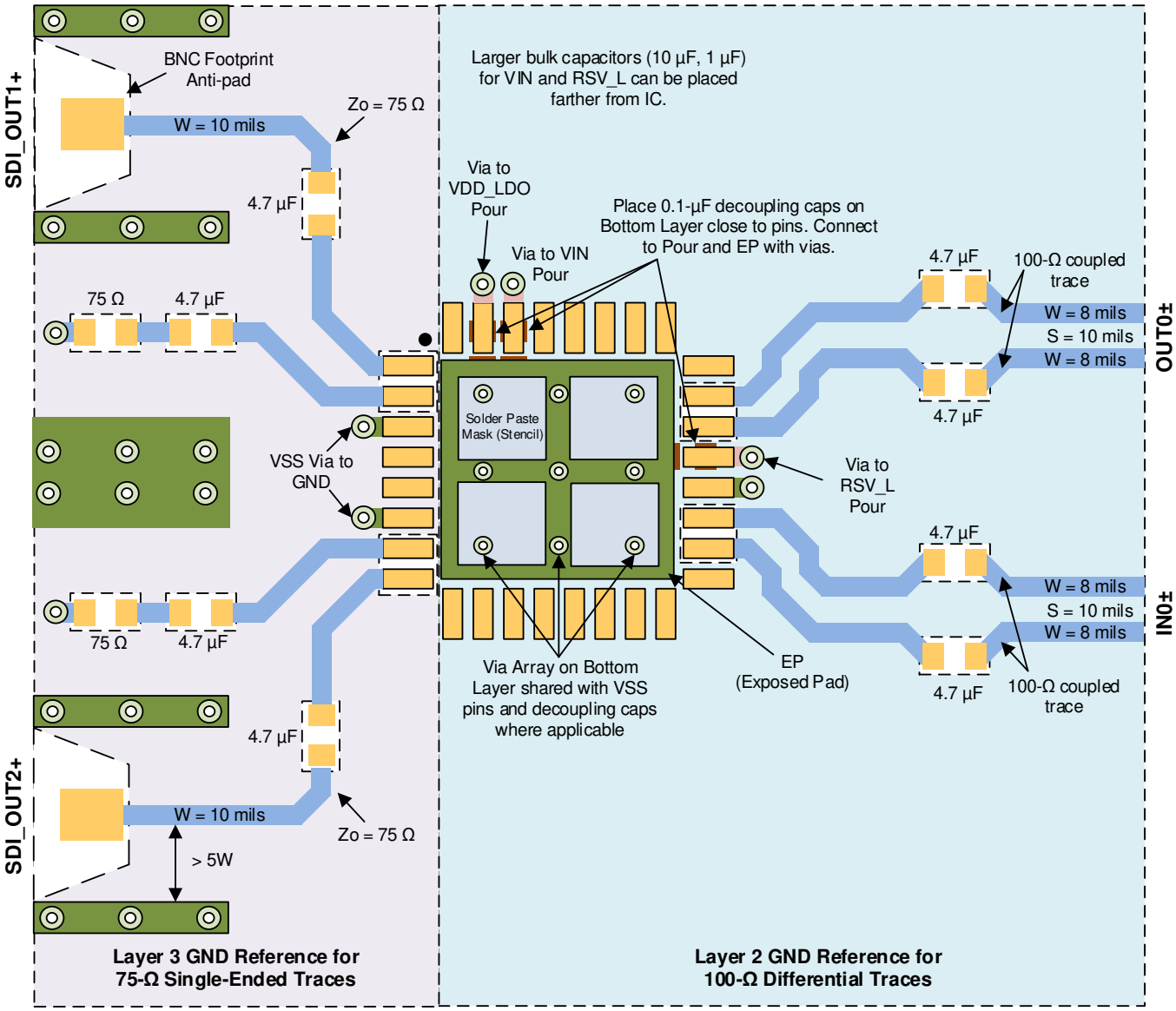
10.1.6 Footprint Recommendations

- Stencil parameters for the EP (Exposed Pad) such as aperture area ratio and the fabrication process have a significant impact on paste deposition. Inspection of the stencil prior to placement of the WQFN package is highly recommended to improve board assembly yields. If the via and aperture openings are not carefully monitored, the solder may flow unevenly through the EP. Stencil parameters for aperture opening and via locations are shown in the RTV package drawing in *机械、封装和可订购信息*.
- The EP of the package must be connected to the ground plane through a 3 × 3 via array. These vias are solder-masked to avoid solder flowing into the plated-through holes during the board manufacturing process. Details about via dimensions are also shown in the RTV package drawing in *机械、封装和可订购信息*.

More information on the WQFN style package is provided in *QFN/SON PCB Attachment Application Report* (SLUA271).

10.2 Layout Example

The example shown in Figure 41 demonstrates the LMH1208 layout guidelines highlighted in *Layout Guidelines*.



Note: All high speed signal traces are assumed to be on Layer 1 (Top Layer).

Figure 41. LMH1208 High-Speed Trace Layout Example

11 器件和文档支持

11.1 文档支持

11.1.1 相关文档

请参阅如下相关文档：

《QFN/SON PCB 连接应用报告》(SLUA271)

11.2 接收文档更新通知

要接收文档更新通知，请导航至 ti.com. 上的器件产品文件夹。单击右上角的*通知我*进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

11.3 社区资源

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

11.4 商标

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

11.5 静电放电警告

ESD 可能会损坏该集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理措施和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。 精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

11.6 出口管制提示

接收方同意：如果美国或其他适用法律限制或禁止将通过本协议的披露方获得的任何产品或技术数据（其中包括软件）（见美国、欧盟和其他出口管理条例之定义）、或者其他适用国家条例限制的任何受管制产品或此项技术的任何直接产品出口或再出口至任何目的地，那么在没有事先获得美国商务部和其他相关政府机构授权的情况下，接收方不得在知情的情况下，以直接或间接的方式将其出口。

11.7 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 机械、封装和可订购信息

以下页面包含机械、封装和可订购信息。这些信息是指定器件的最新可用数据。数据如有变更，恕不另行通知，且不会对此文档进行修订。如欲获取此数据表的浏览器版本，请参阅左侧的导航。

12.1 Package Option Addendum

12.1.1 Packaging Information

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (3)	MSL Peak Temp (4)	Op Temp (°C)	Device Marking (5) (6)
LMH1208RTVR	ACTIVE	WQFN	RTV	32	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	L1208
LMH1208RTVT	ACTIVE	WQFN	RTV	32	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	L1208

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PRE_PROD Unannounced device, not in production, not available for mass market, nor on the web, samples not available.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

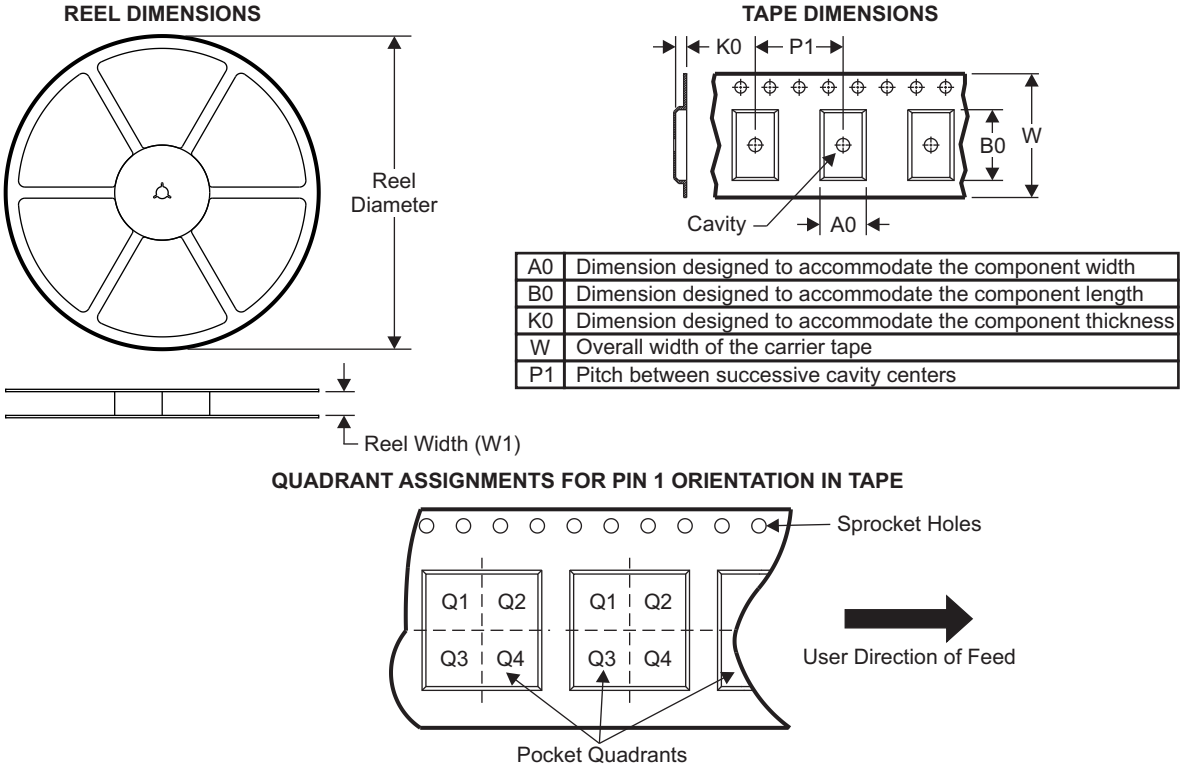
(3) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

(4) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(5) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device

(6) Multiple Device markings will be inside parentheses. Only on Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

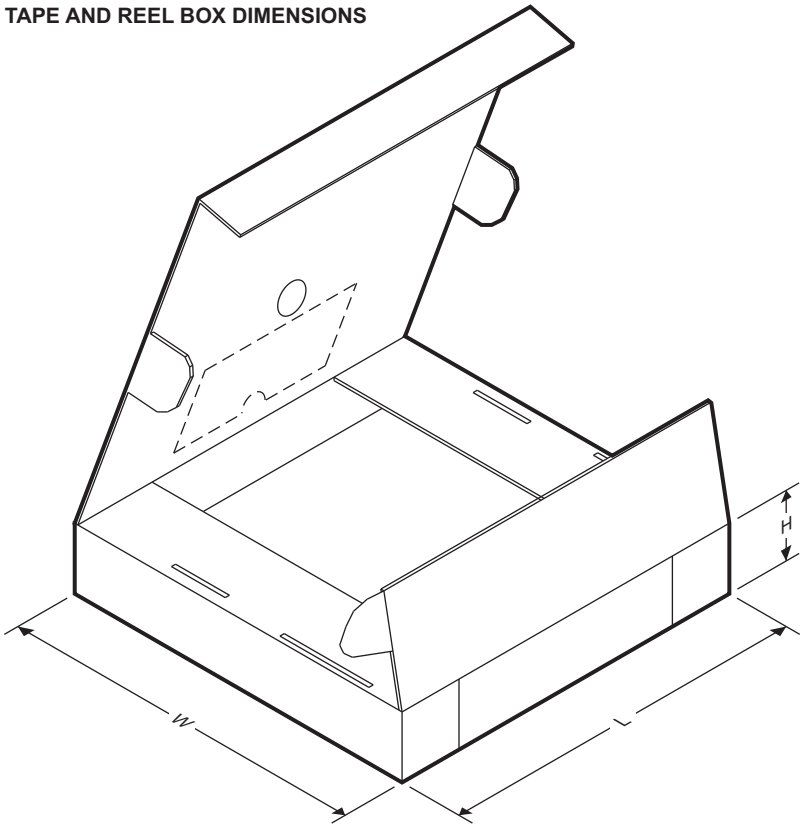
12.1.2 Tape and Reel Information



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LMH1208RTVR	WQFN	RTV	32	1000	178.0	12.4	5.3	5.3	1.1	8.0	12.0	Q2
LMH1208RTVT	WQFN	RTV	32	250	178.0	12.4	5.3	5.3	1.1	8.0	12.0	Q2

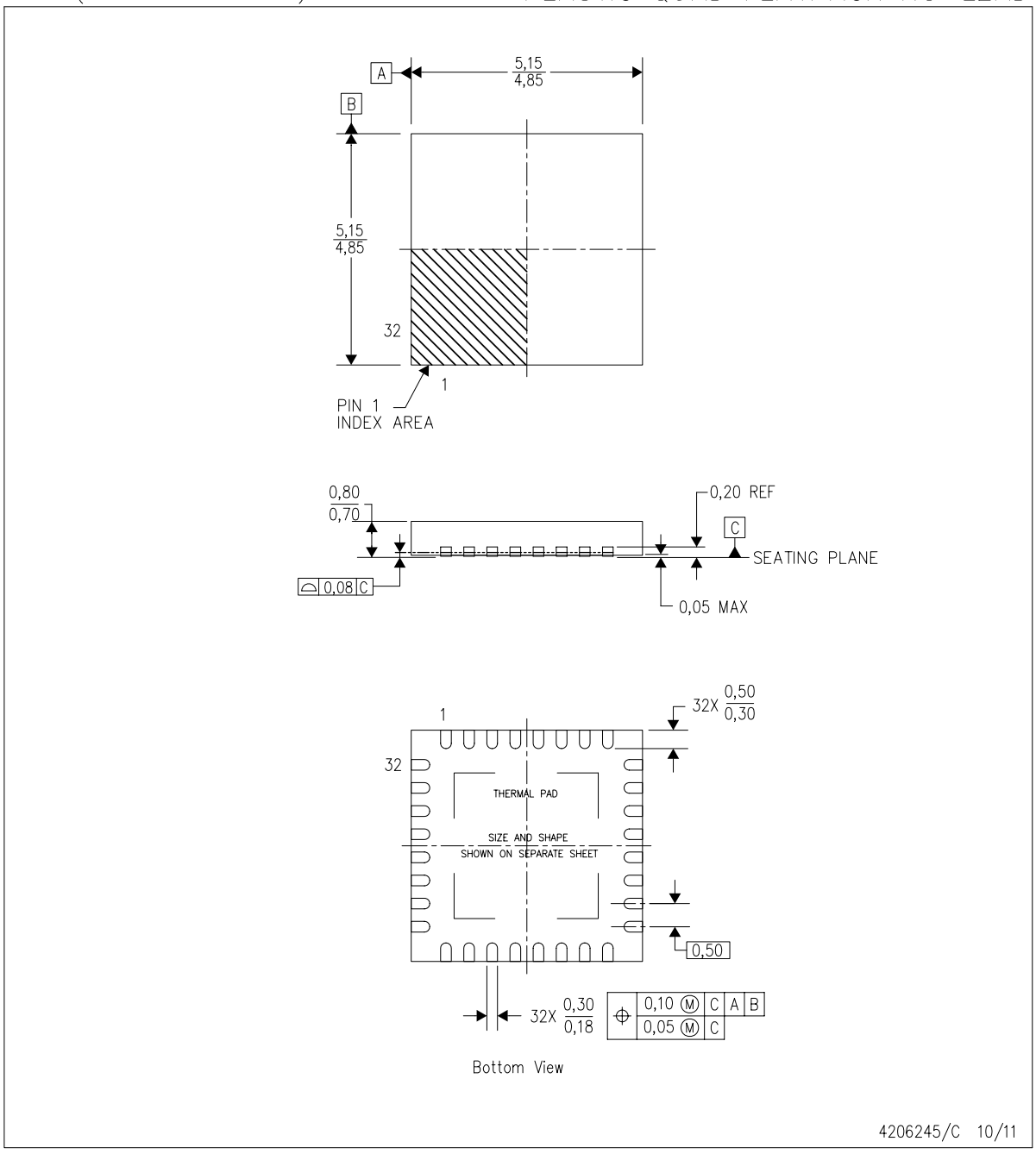
TAPE AND REEL BOX DIMENSIONS



Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LMH1208RTVR	WQFN	RTV	32	1000	210.0	185.0	35.0
LMH1208RTVT	WQFN	RTV	32	250	210.0	185.0	35.0

MECHANICAL DATA

RTV (S–PWQFN–N32) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5–1994.
B. This drawing is subject to change without notice.
C. Quad Flatpack, No–Leads (QFN) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. Falls within JEDEC MO–220.

THERMAL PAD MECHANICAL DATA

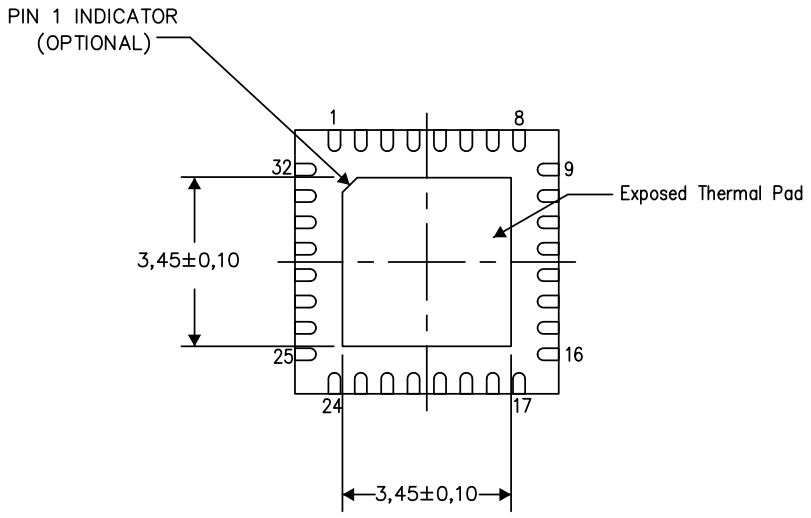
RTV (S–PWQFN–N32) PLASTIC QUAD FLATPACK NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Bottom View

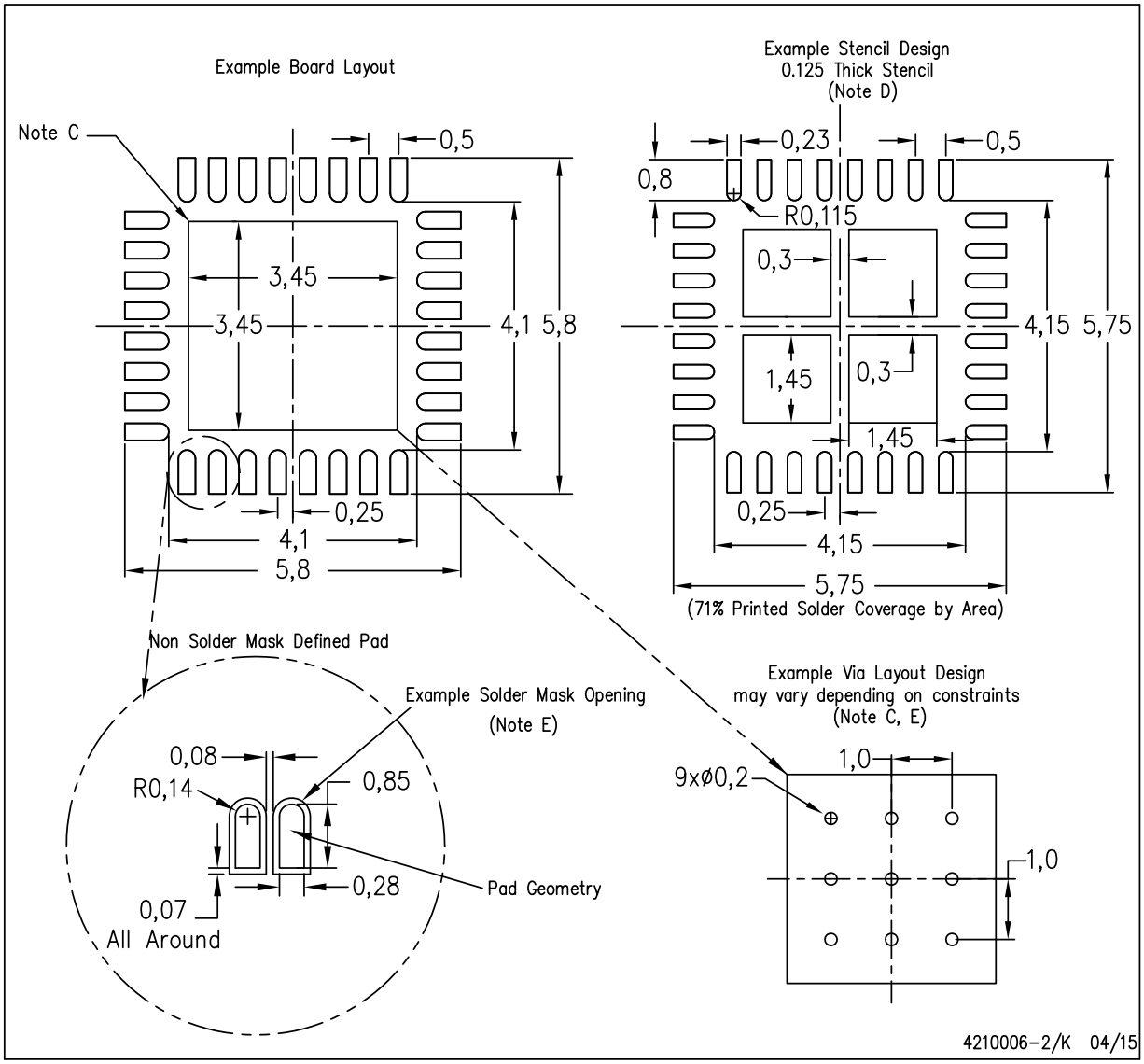
Exposed Thermal Pad Dimensions

4206250–2/Q 05/15

NOTE: All linear dimensions are in millimeters

LAND PATTERN DATA

RTV (S–PWQFN–N32) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack Packages, Texas Instruments Literature No. SCBA017, SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
E. Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting recommendations for vias placed in the thermal pad.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LMH1208RTVR	ACTIVE	WQFN	RTV	32	1000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	L1208	Samples
LMH1208RTVT	ACTIVE	WQFN	RTV	32	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	L1208	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

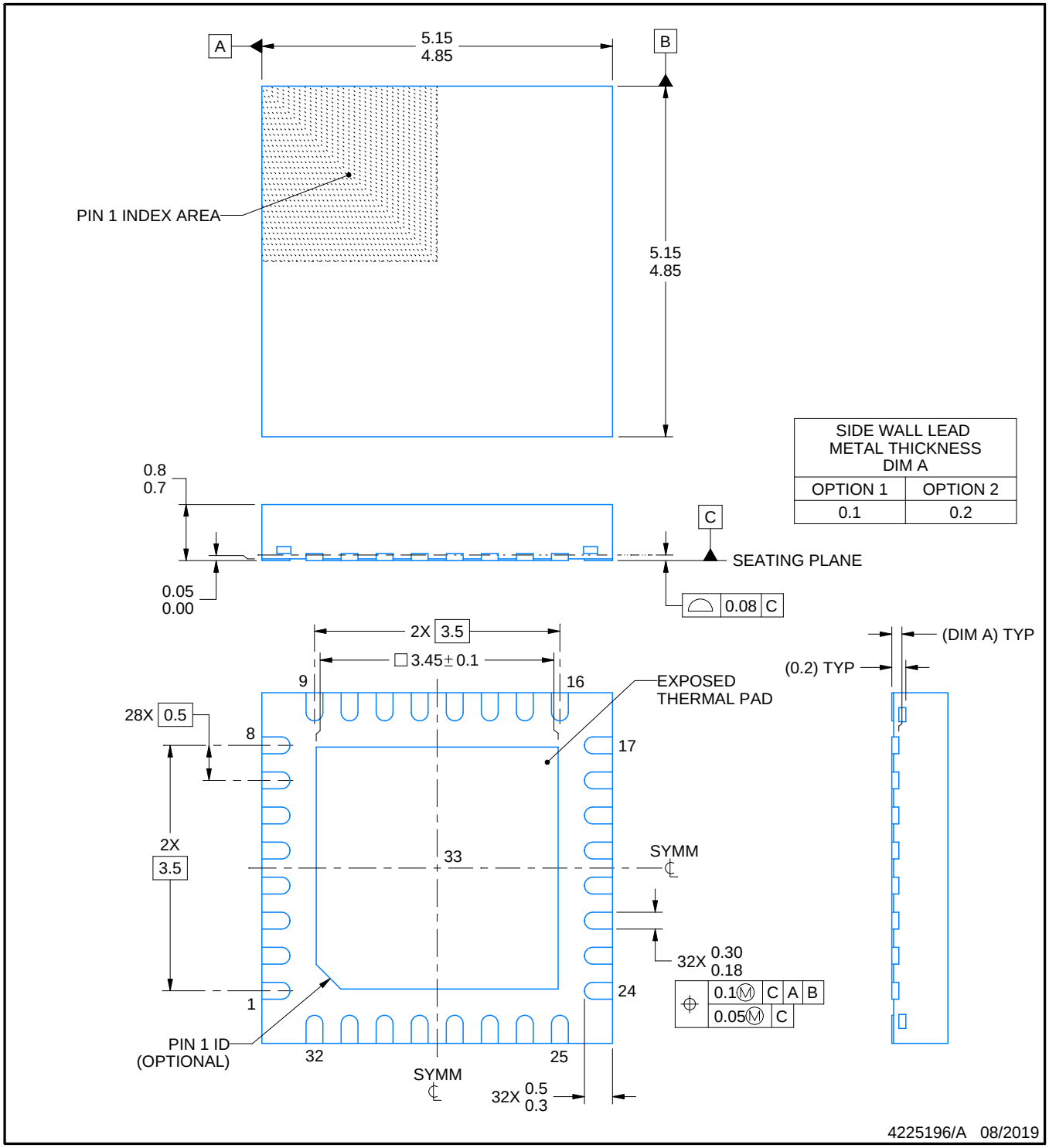
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

RTV0032E

PACKAGE OUTLINE

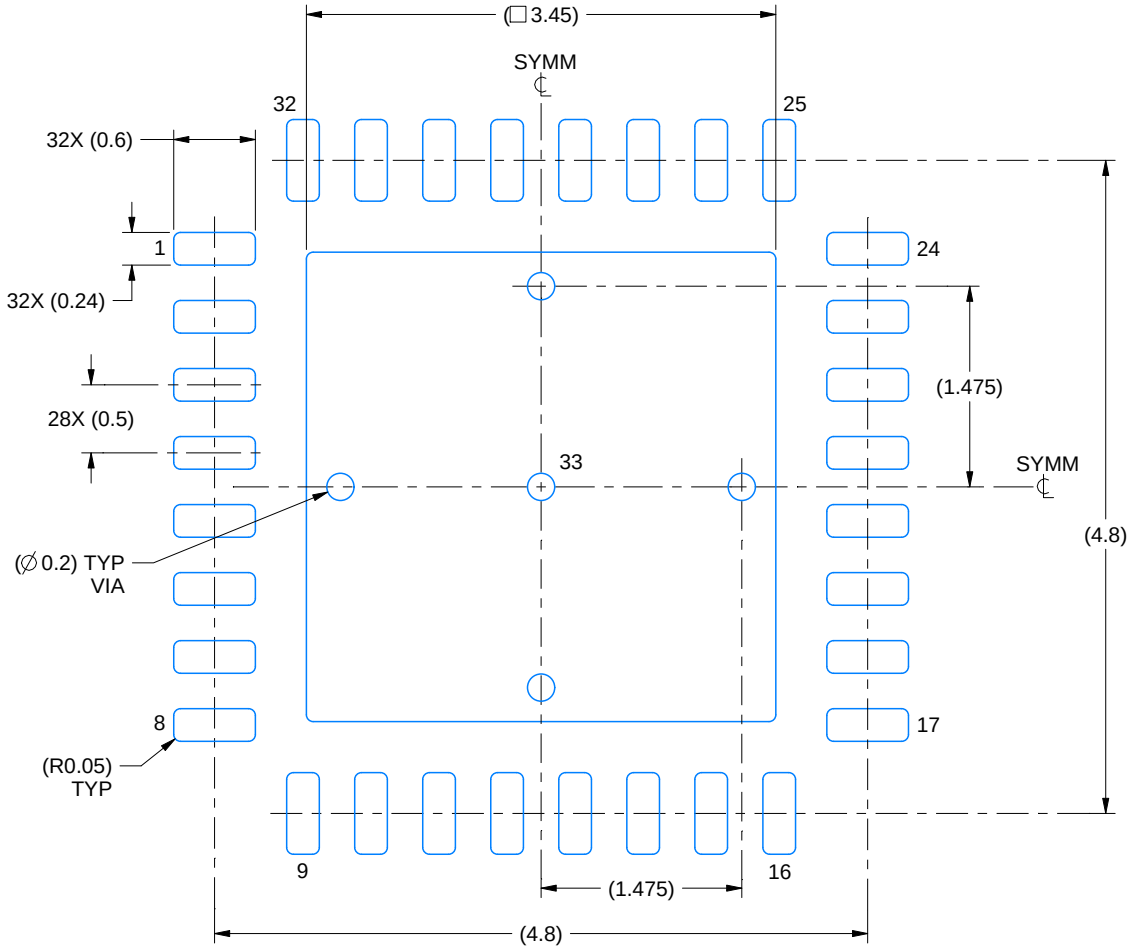
WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

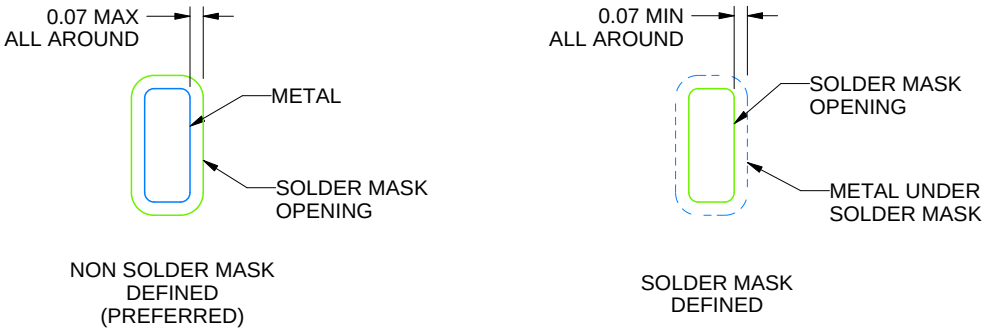


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
SCALE:18X

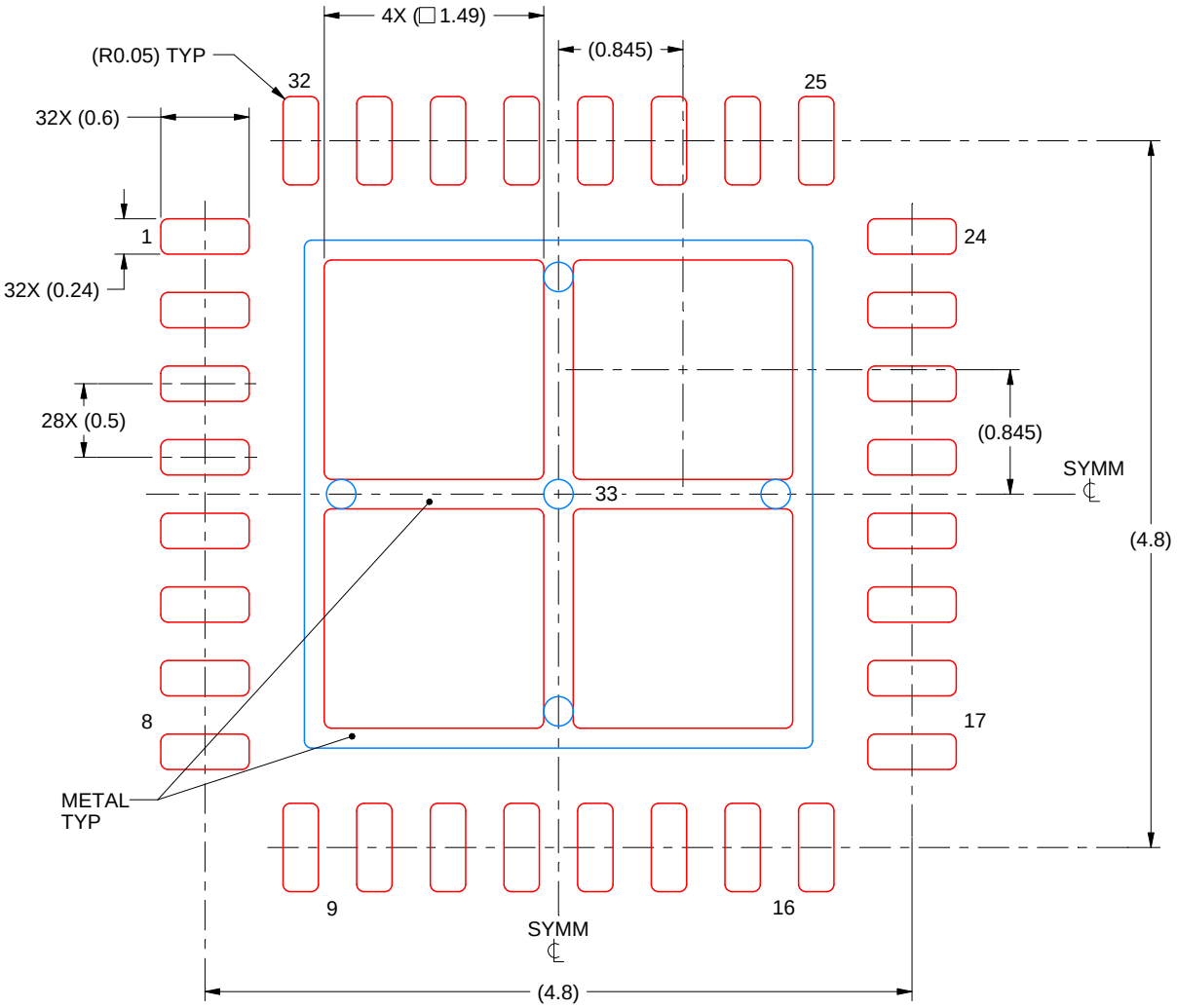


SOLDER MASK DETAILS

4225196/A 08/2019

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 33:
75% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:20X

4225196/A 08/2019

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

重要声明和免责声明

TI“按原样”提供技术和可靠性数据（包括数据表）、设计资源（包括参考设计）、应用或其他设计建议、网络工具、安全信息和其他资源，不保证没有瑕疵且不做出任何明示或暗示的担保，包括但不限于对适销性、某特定用途方面的适用性或不侵犯任何第三方知识产权的暗示担保。

这些资源可供使用 TI 产品进行设计的熟练开发人员使用。您将自行承担以下全部责任：(1) 针对您的应用选择合适的 TI 产品，(2) 设计、验证并测试您的应用，(3) 确保您的应用满足相应标准以及任何其他功能安全、信息安全、监管或其他要求。

这些资源如有变更，恕不另行通知。TI 授权您仅可将这些资源用于研发本资源所述的 TI 产品的应用。严禁对这些资源进行其他复制或展示。您无权使用任何其他 TI 知识产权或任何第三方知识产权。您应全额赔偿因在这些资源的使用中对 TI 及其代表造成的任何索赔、损害、成本、损失和债务，TI 对此概不负责。

TI 提供的产品受 TI 的销售条款或 ti.com 上其他适用条款/TI 产品随附的其他适用条款的约束。TI 提供这些资源并不会扩展或以其他方式更改 TI 针对 TI 产品发布的适用的担保或担保免责声明。

TI 反对并拒绝您可能提出的任何其他或不同的条款。

邮寄地址：Texas Instruments, Post Office Box 655303, Dallas, Texas 75265