

LMS33460 3-V Undervoltage Detector

1 Features

- Ultra-Low Power
- 3-V Detection
- Input Voltage From 0.8 V to 7 V
- Open-Drain Output
- Ultra-Small 5-Pin SC70 Package
- Extended Temperature Range (-40°C to 85°C)
- Ultra-Low Quiescent Current (1 μ A Typical)

2 Applications

- Low Battery Voltage Detectors
- Power Fail Indicators
- Processor Reset Generators
- Battery Backup Controls
- Battery-Operated Equipment
- Hand-Held Instruments
- Undervoltage Detectors

3 Description

The LMS33460 device is an undervoltage detector with a 3-V threshold and extremely low power consumption. The LMS33460 is specifically designed to accurately monitor power supplies. It is especially suited to battery-powered systems where low quiescent current and small size are required. This IC generates an active output whenever the input voltage drops below 3 V.

This part uses a precision on-chip voltage reference and a comparator to measure the input voltage. Built-in hysteresis helps to prevent erratic operation in the presence of noise. The UVD is available in the ultra-miniature 5-pin SC70 package.

Device Information⁽¹⁾

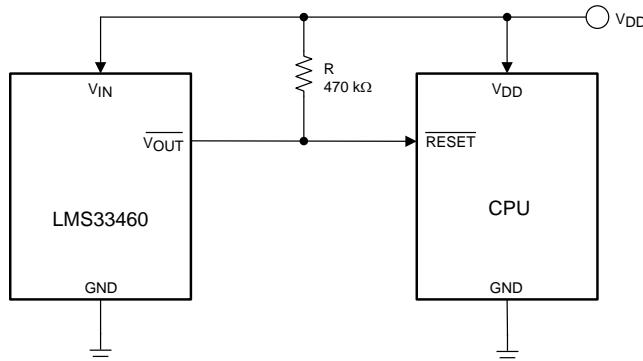
PART NUMBER	PACKAGE	BODY SIZE (NOM)
LMS33460	SC70 (5)	2.00 mm x 1.25 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

SC70 Package



Typical Application



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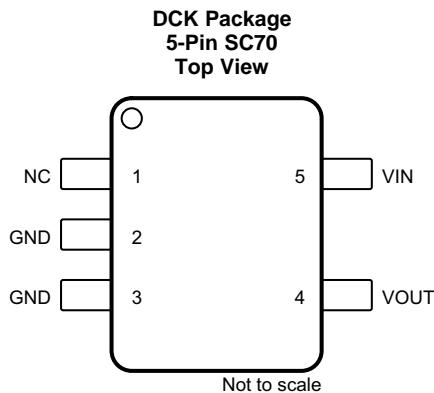
4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision D (April 2013) to Revision E	Page
• Added <i>ESD Ratings</i> table, <i>Feature Description</i> section, <i>Device Functional Modes</i> , <i>Application and Implementation</i> section, <i>Power Supply Recommendations</i> section, <i>Layout</i> section, <i>Device and Documentation Support</i> section, and <i>Mechanical, Packaging, and Orderable Information</i> section	1
• Deleted <i>Ordering Information</i> table; see POA at the end of the data sheet.....	1
• Added <i>Thermal Information</i> table	4
• Changed $R_{\theta,JA}$ value From: 478 To: 275.5	4

Changes from Revision C (April 2013) to Revision D	Page
• Changed layout of National Semiconductor Data Sheet to TI format	1

5 Pin Configuration and Functions



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
GND	2	—	Internally connected to ground. Can be left floating or connected to GND (pin 3).
GND	3	—	Ground
NC	1	—	No connection
VIN	5	I	Input supply
VOUT	4	O	Voltage output

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

		MIN	MAX	UNIT
Input voltage to GND			8	V
Output voltage to GND			8	V
Output continuous output current			30	mA
Vapor phase IR convection reflow			240	°C
Junction temperature, T_J			150	°C
Storage temperature, T_{stg}		-65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

		VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾	± 2500
		Machine model	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

		MIN	MAX	UNIT
T_J	Operating junction temperature	-40	85	°C

6.4 Thermal Information

THERMAL METRIC ⁽¹⁾		LMS33460	UNIT
		DCK (SC70)	
		5 PINS	
R _{θJA}	Junction-to-ambient thermal resistance	275.5	°C/W
R _{θJC(top)}	Junction-to-case (top) thermal resistance	102.5	°C/W
R _{θJB}	Junction-to-board thermal resistance	54	°C/W
Ψ _{JT}	Junction-to-top characterization parameter	2.7	°C/W
Ψ _{JB}	Junction-to-board characterization parameter	53.3	°C/W

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

6.5 Electrical Characteristics

T_J = 25°C (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT	
V _{DET}	V _{IN} falling	2.85	3	3.15	V	
V _{HYS}	V _{IN} rising	0.095	0.155	0.215	V	
I _{IN}	V _{IN} = 2.87 V		1	2.2	µA	
	V _{IN} = 4.7 V		1.2	3.6	µA	
	V _{IN} = 7 V ⁽¹⁾		25	200	µA	
V _{IN(MAX)}	Maximum operating voltage			7	V	
V _{IN(MIN)}	Minimum operating voltage		0.7	1.1	V	
	T _J = -40°C to 85°C		1	1.3		
I _{OUT(LOW)}	Output current low	V _{OUT} = 0.05 V, V _{IN} = 1.1 V	0.01	0.6	mA	
	V _{OUT} = 0.5 V, V _{IN} = 1.5 V		2	11		
t _{PDHL}	Output delay time (output transition high to low)	C _L = 10 pF, R _L = 470 kΩ		130	200	µs
ΔV _{DET} /ΔT	Detect voltage temperature coefficient	T _J = -40°C to 85°C		±120	PPM/°C	

(1) Quiescent current increases substantially above 5.5 V, but is very low in the normal range below 5.5 V.

6.6 Typical Characteristics

$T_A = 25^\circ\text{C}$, $R_L = 470 \text{ k}\Omega$, and $C_L = 10 \text{ pF}$ (unless otherwise noted)

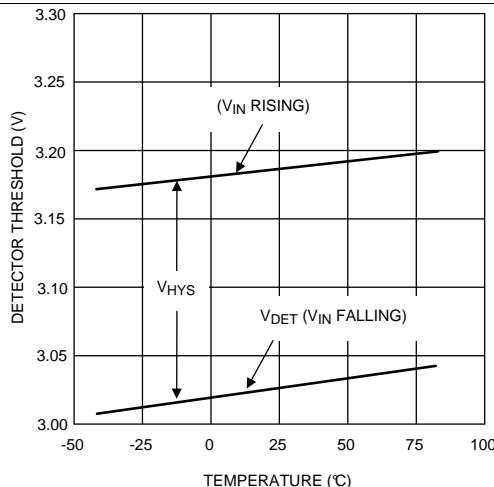


Figure 1. Detector Threshold vs Temperature

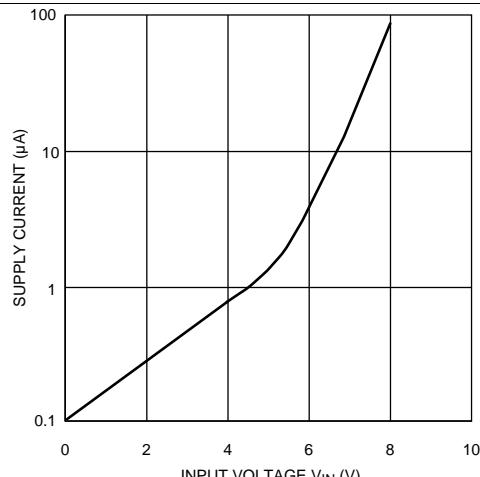


Figure 2. Supply Current vs Input Voltage

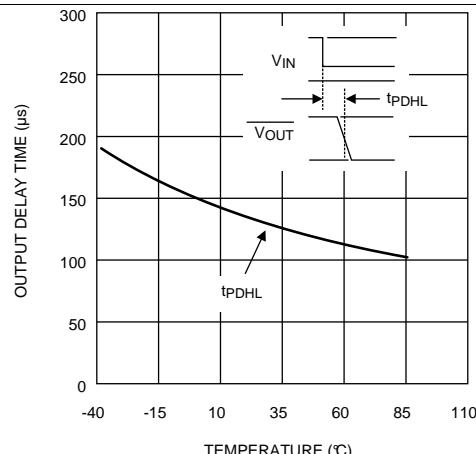


Figure 3. Propagation Delay Time (t_{PDHL}) vs Temperature

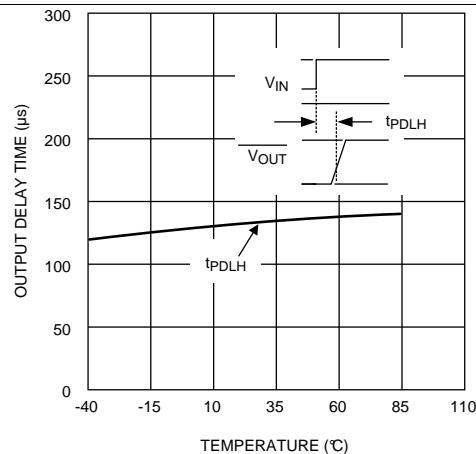


Figure 4. Propagation Delay Time (t_{PDLH}) vs Temperature

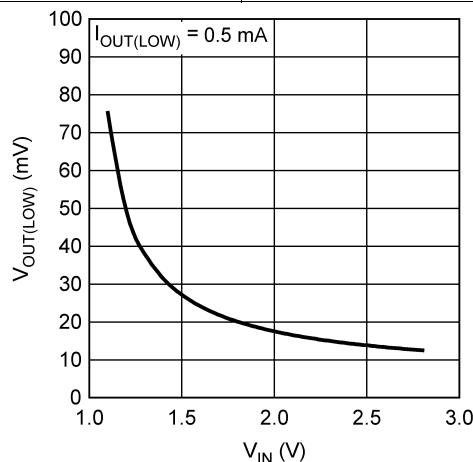


Figure 5. $V_{OUT(LOW)}$ vs V_{IN}

7 Detailed Description

7.1 Overview

The LMS33460 is a micropower undervoltage-sensing circuit with an open-drain output configuration, which requires a pull resistor.

The LMS33460 features a voltage reference, a comparator with precise thresholds and built-in hysteresis to prevent erratic reset operation.

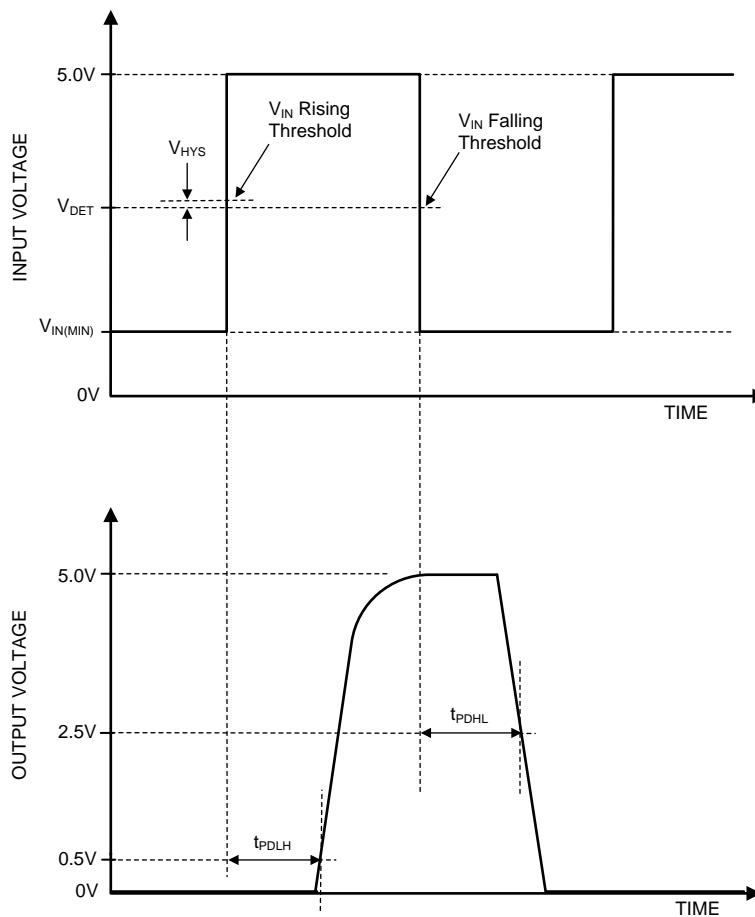
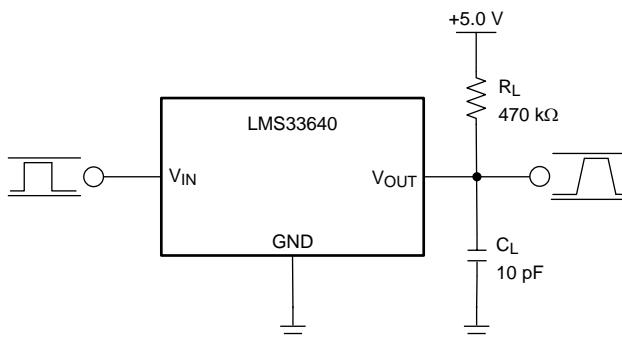


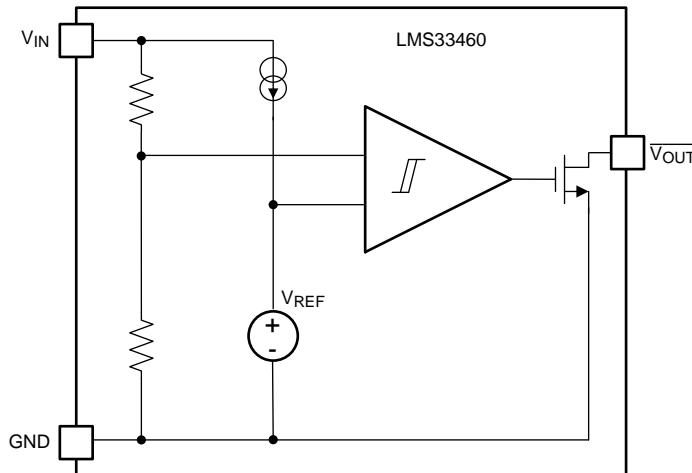
Figure 6. Propagation Delay Timing Diagram



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Figure 7. Propagation Delay Test Circuit

7.2 Functional Block Diagram



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7.3 Feature Description

The input supply (V_{IN}) is the voltage that is being monitored and as it decreases past 3 V, the active-low output (V_{OUT}) transitions to a logic low state. When V_{IN} rises above 3 V plus the built-in hysteresis, V_{OUT} returns to its original state of logic high. The LMS33460 has built-in hysteresis when the input supply is coming back up to help prevent erratic output operation when the input voltage crosses the threshold.

The LMS33460 is useful in a variety of applications that require low voltage detection and is suited for battery-powered systems where low quiescent current and small package size is required. It can also be used as a precision reset circuit for microcontroller applications.

7.4 Device Functional Modes

7.4.1 Start Up

As the input voltage (V_{IN}) ramps up, the output (V_{OUT}) remains logic low until V_{IN} reaches 3.15 V due to the built-in hysteresis (nominally 150 mV). After V_{IN} crosses that threshold, V_{OUT} remains logic high until V_{IN} drops below the 3-V threshold. The hysteresis only applies to the V_{IN} rising threshold.

8 Application and Implementation

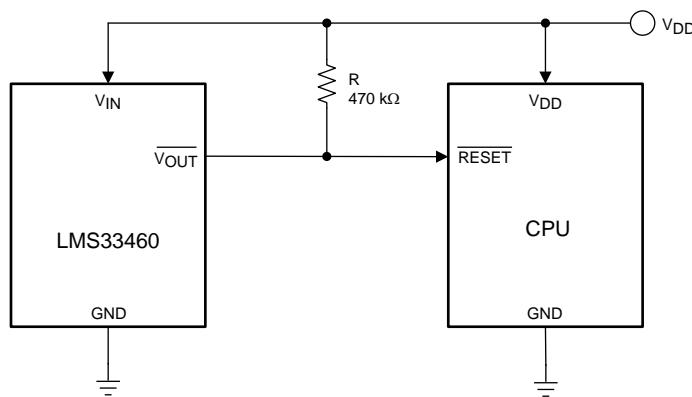
NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

This device is ideal to use in battery-powered or microprocessor based systems and can be used as a low voltage indicator or reset circuit.

8.2 Typical Application



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Figure 8. Typical Application Schematic

8.2.1 Design Requirements

For this design example, use the parameters listed in [Table 1](#) as the input parameters.

Table 1. Design Parameters

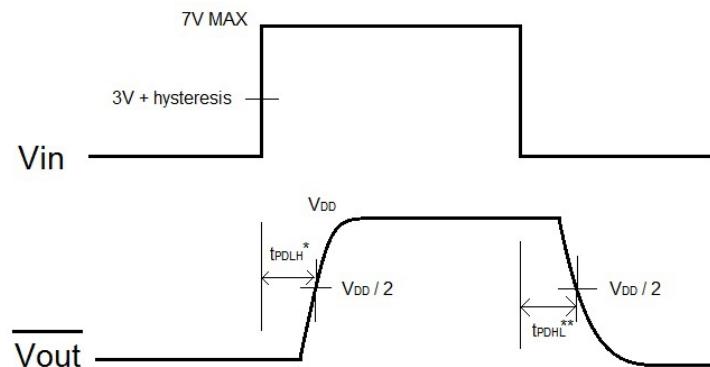
PARAMETER	EXAMPLE VALUE
Input supply voltage maximum	7 V
V_{OUT} maximum	7 V
V_{OUT} minimum	0 V
Pullup resistor	470 kΩ

8.2.2 Detailed Design Procedure

The LMS33460 is a very easy to use low voltage detector. All that required is the input supply voltage and a pullup resistor at the output. TI recommends 470 kΩ for the pullup resistor.

8.2.3 Application Curve

$R_L = 475 \text{ k}\Omega$



* See [Figure 4](#) for tPDLH values

** See [Figure 3](#) for tPDHL values

Figure 9. LMS33460 Turnon

9 Power Supply Recommendations

The input of the LMS33460 is designed to handle up to the recommended supply voltage of 7 V and remain in the recommended input voltage range during operation. No input capacitor is required.

10 Layout

10.1 Layout Guidelines

Place the output pullup resistor, and delay capacitor if used, as close as possible to the IC. Keep traces short between the IC and the components used at the output to ensure the timing delay is as accurate as possible.

10.2 Layout Example

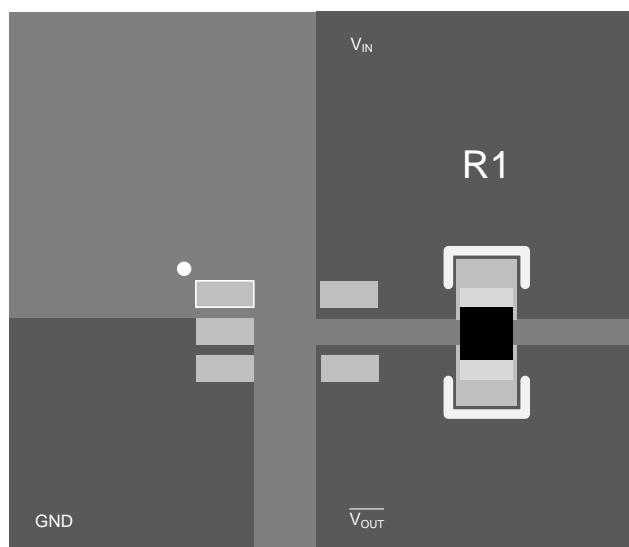


Figure 10. Layout Example Diagram

11 Device and Documentation Support

11.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

TI E2E™ Online Community *TI's Engineer-to-Engineer (E2E) Community*. Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.3 Trademarks

E2E is a trademark of Texas Instruments.

All other trademarks are the property of their respective owners.

11.4 Electrostatic Discharge Caution

 This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

 ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.5 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
LMS33460MG/NOPB	Active	Production	SC70 (DCK) 5	1000 LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	C33
LMS33460MG/NOPB.A	Active	Production	SC70 (DCK) 5	1000 LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	C33

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

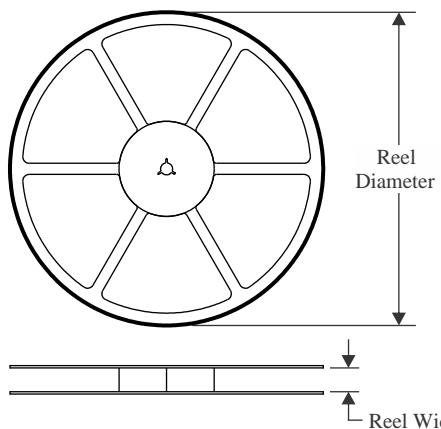
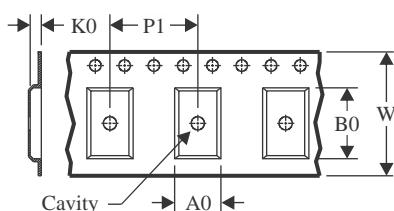
⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

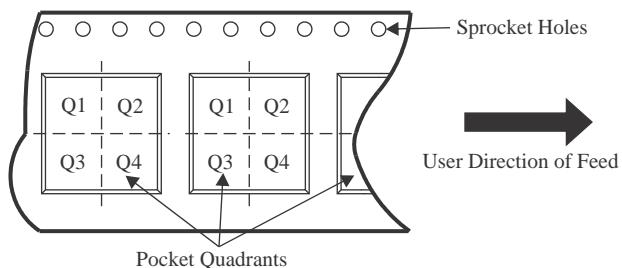
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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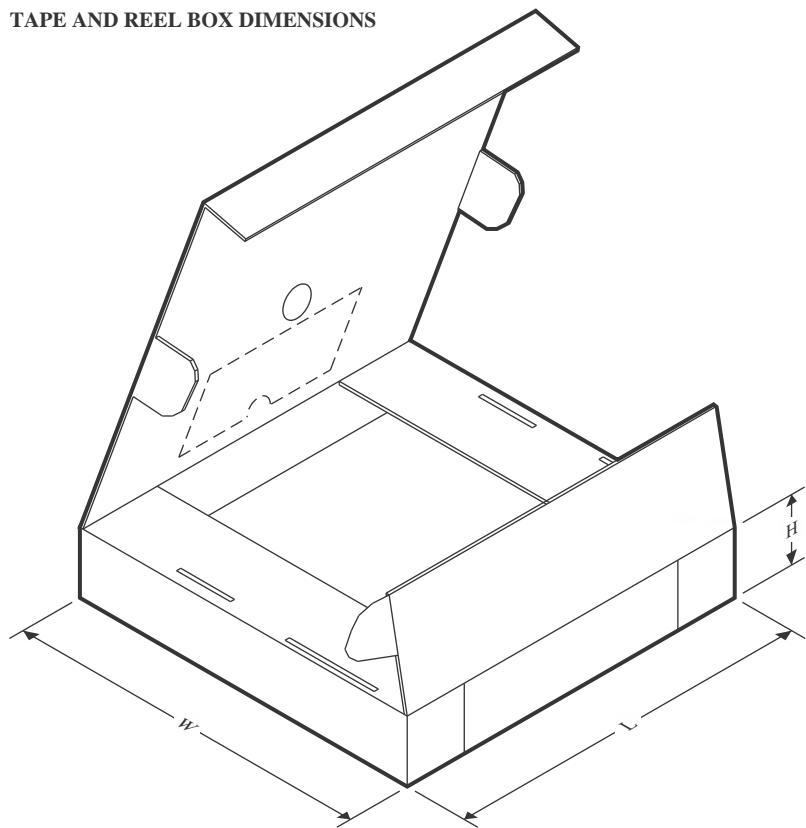
TAPE AND REEL INFORMATION
REEL DIMENSIONS

TAPE DIMENSIONS


A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LMS33460MG/NOPB	SC70	DCK	5	1000	178.0	8.4	2.25	2.45	1.2	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LMS33460MG/NOPB	SC70	DCK	5	1000	208.0	191.0	35.0

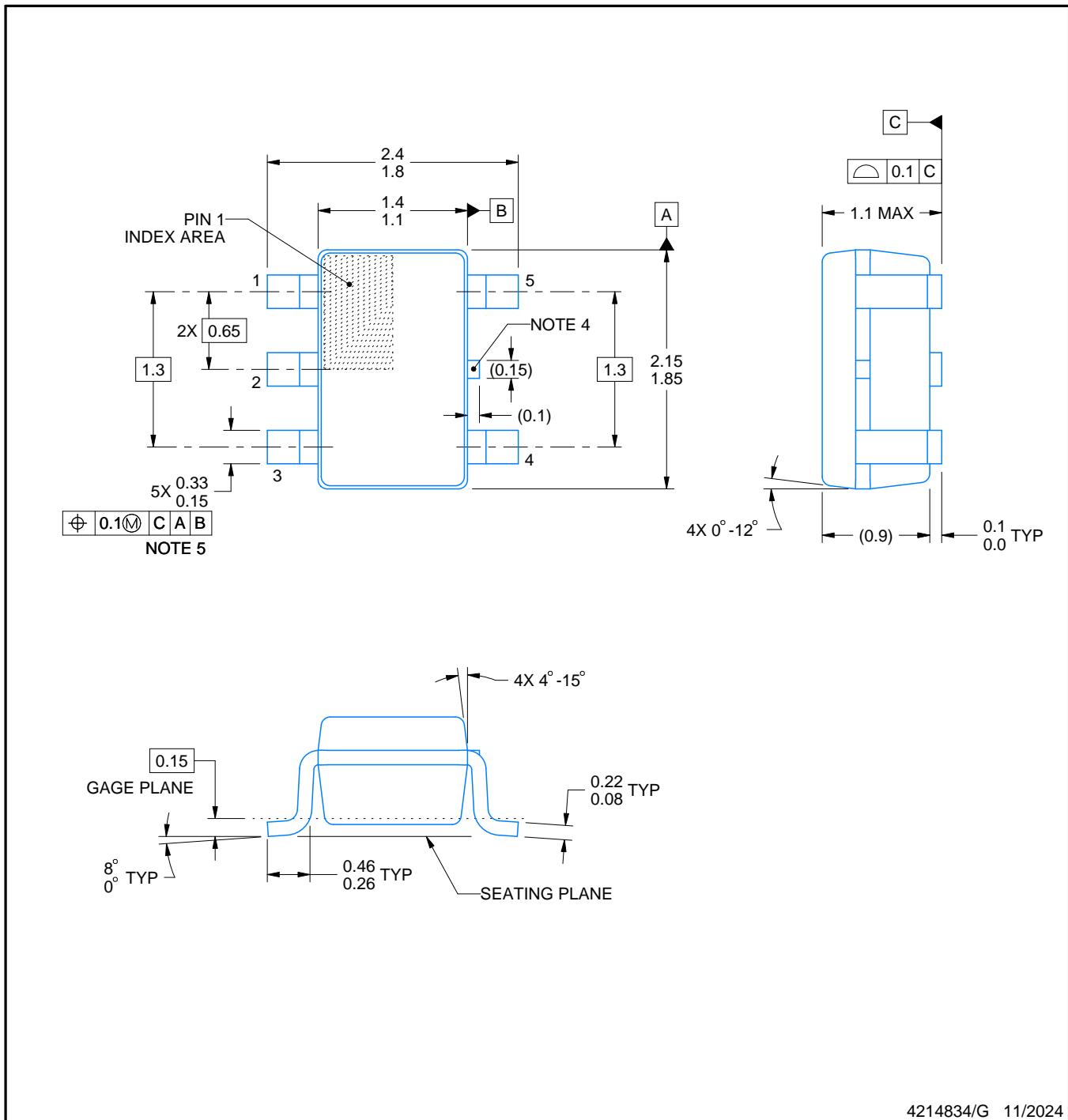
PACKAGE OUTLINE

DCK0005A



SOT - 1.1 max height

SMALL OUTLINE TRANSISTOR



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NOTES:

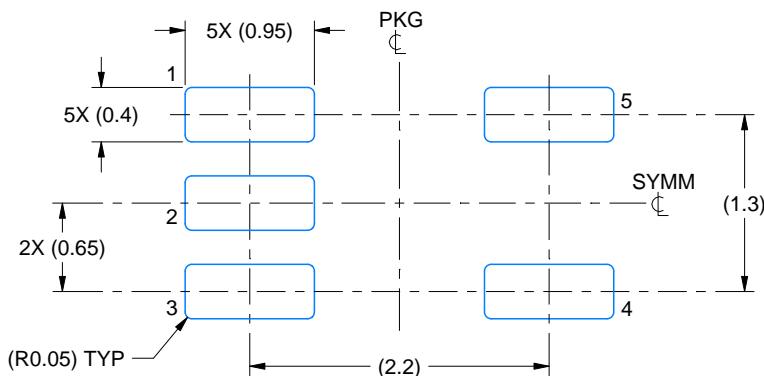
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC MO-203.
4. Support pin may differ or may not be present.
5. Lead width does not comply with JEDEC.
6. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25mm per side

EXAMPLE BOARD LAYOUT

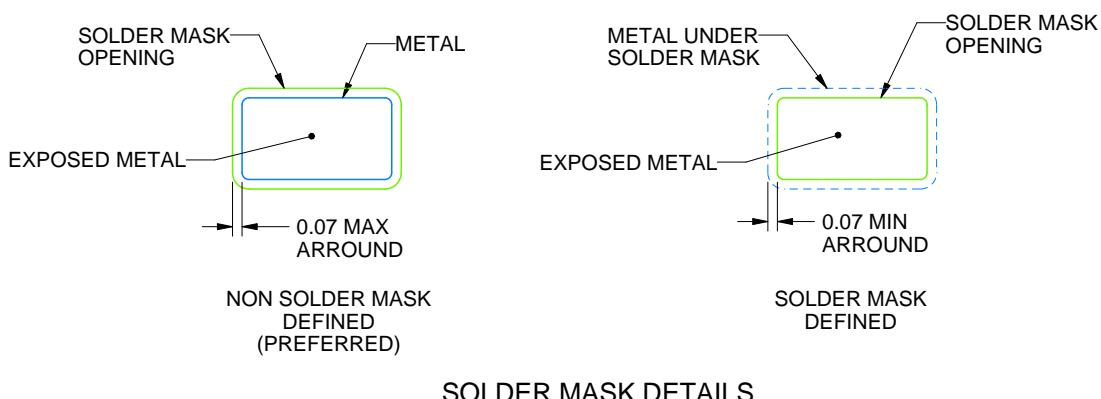
DCK0005A

SOT - 1.1 max height

SMALL OUTLINE TRANSISTOR



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:18X



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NOTES: (continued)

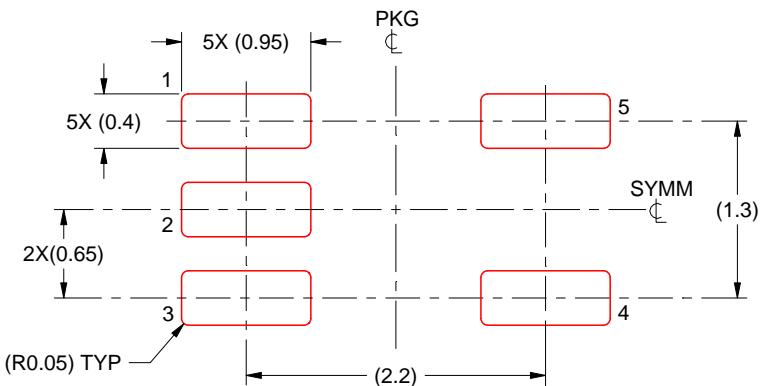
7. Publication IPC-7351 may have alternate designs.
8. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DCK0005A

SOT - 1.1 max height

SMALL OUTLINE TRANSISTOR



SOLDER PASTE EXAMPLE
BASED ON 0.125 THICK STENCIL
SCALE:18X

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NOTES: (continued)

9. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
10. Board assembly site may have different recommendations for stencil design.

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