LMV7275-Q1 具有轨到轨输入的汽车类单路 1.8V 低功耗比较器

1 特性

- 适用于汽车电子 应用
- 具有符合 AEC-Q100 标准的下列结果：
  - 器件温度 3 级：-40°C 至 85°C 的运行环境温度范围
  - 器件人体放电模式 (HBM) 静电放电 (ESD) 分类等级 2
  - 器件组件充电模式 (CDM) ESD 分类等级 C6
- （除非另外注明，否则典型值为 V_S = 1.8V，T_A = 25°C）。
- 由单电源或双电源供电
- 开漏输出
- 超低电源电流：9µA（每通道）
- 低输入偏置电流：10nA
- 低输入偏移电流：200pA
- 低输入偏移电压 (V_{OS})：4mV
- 传播延迟：880ns（20mV 过驱电压）
- 输入共模电压范围：（负电源轨电压 - 0.1V）至（正电源轨电压 + 0.1V）

2 应用

- 可穿戴式设备
- 手机和平板电脑
- 电池供电类电子产品
- 通用低电压 应用

3 说明

LMV7275-Q1 是一款单路轨到轨输入低功耗比较器，额定电源电压包括 1.8V、2.7V 和 5V。每条通道的电源流耗低至 9µA，同时可实现 800ns 的短暂传播延迟。

LMV7275-Q1 采用 SC-70 封装。这类微型封装可显著减小印刷电路板 (PCB) 面积，非常适合低电压、低功耗、对空间要求严格的设计。

LMV7275-Q1 特有 一个开漏输出级，支持线或配置。此外，开漏输出还具备另一项优势，即允许将输出上拉至 5.5V 及以下的任一电压，与 LMV7275-Q1 的电源电压无关。该特性有益于电平转换 应用。

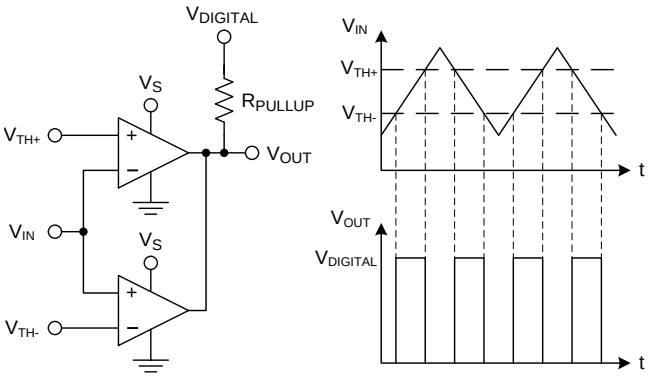
LMV7275-Q1 采用德州仪器 (TI) 先进的亚微米硅栅 BiCMOS 工艺。该器件采用双极输入改善噪声性能，凭借互补金属氧化物半导体 (CMOS) 输出将负输出摆幅降至最低。

器件信息(1)

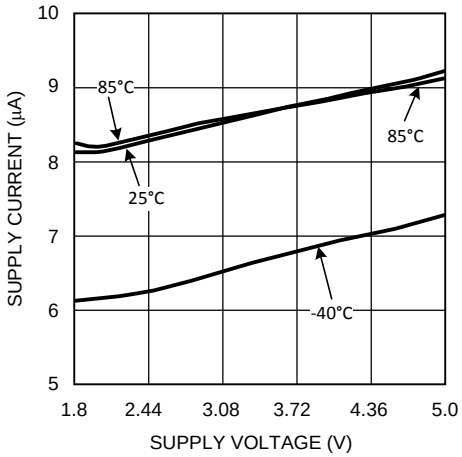
器件型号	封装	封装尺寸（标称值）
LMV7275-Q1	SC70 (5)	1.25mm × 2.00mm

(1) 要了解所有可用封装，请参见数据表末尾的可订购产品附录。

LMV7275-Q1 用作窗口比较器



低电源电流



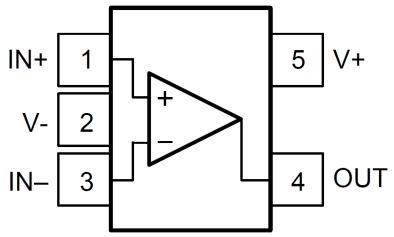
目录

4 修订历史记录

日期	修订版本	注释
2015 年 9 月	*	最初发布版本。

5 Pin Configuration and Functions

DGK Package
5-Pin SC70
Top View



Pin Functions

PIN		I/O	DESCRIPTION
NAME	SC70		
IN+	1	I	Non-Inverting Input
V-	2	P	Negative Supply Voltage
IN-	3	I	Inverting Input
OUT	4	O	Output
V+	5	P	Positive Supply Voltage

6 Specifications

6.1 Absolute Maximum Ratings (1)

	MIN	MAX	UNIT
V_{IN} Differential		±Supply Voltage	V
Supply Voltage (V^+ - V^-)		6	V
Voltage at Input/Output pins	(V^-) − 0.1	(V^+) + 0.1	V
Junction Temperature (2)		150	°C
Storage Temperature, T_{stg}	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The maximum power dissipation is a function of $T_{J(MAX)}$, $R_{\theta JA}$, and T_A. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(MAX)} - T_A)/R_{\theta JA}$. All numbers apply for packages soldered directly into a PCB.

6.2 ESD Ratings LMV7275-Q1

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002 (1)	±2000	V
		Charged-device model (CDM), per AEC Q100-011	±1000	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.3 Recommended Operating Conditions

	MIN	MAX	UNIT
Supply Voltage	1.8	5.5	V
Temperature (1)	–40	85	°C

(1) The maximum power dissipation is a function of $T_{J(MAX)}$, $R_{\theta JA}$, and T_A. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(MAX)} - T_A)/R_{\theta JA}$. All numbers apply for packages soldered directly into a PCB.

6.4 Thermal Information

THERMAL METRIC[1]		LMV7275-Q1 DGK (SC70) 5 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance [2]	273.8	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	106.1	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	54.9	°C/W
ψ_{JT}	Junction-to-top characterization parameter	3.6	°C/W
ψ_{JB}	Junction-to-board characterization parameter	54.1	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.
(2) The maximum power dissipation is a function of $T_{J(MAX)}$, $R_{\theta JA}$, and T_A. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(MAX)} - T_A)/R_{\theta JA}$. All numbers apply for packages soldered directly into a PCB.

6.5 1.8-V Electrical Characteristics

Unless otherwise specified, all limits ensured for T_J = 25°C, V^+ = 1.8 V, V^- = 0 V.

PARAMETER		CONDITION	MIN[1]	TYP[2]	MAX[1]	UNIT
V_{OS}	Input Offset Voltage			0.3	4	mV
		At the temperature extremes			6	
TC V_{OS}	Input Offset Temperature Drift	V_{CM} = 0.9 V [3]		20		uV/°C
I_B	Input Bias Current			10		nA
I_{OS}	Input Offset Current			200		pA
I_S	Supply Current			9	12	µA
		At the temperature extremes			14	
I_{SC}	Output Short Circuit Current	Sinking, V_O = 0.9 V	4	6		mA
V_{OL}	Output Voltage Low	I_O = −0.5 mA		52	100	mV
		I_O = −1.5 mA		166	220	
V_{CM}	Input Common-Mode Voltage Range	CMRR > 45 dB	−0.1		1.9	V
CMRR	Common-Mode Rejection Ratio	0 < V_{CM} < 1.8 V	46	78		dB
PSRR	Power Supply Rejection Ratio	V^+ = 1.8 V to 5 V	55	80		dB
$I_{LEAKAGE}$	Output Leakage Current	V_O = 1.8 V		2		pA

(1) All limits are ensured by testing or statistical analysis.
(2) Typical values represent the most likely parametric norm.
(3) Offset Voltage average drift determined by dividing the change in V_{OS} at temperature extremes into the total temperature change.

6.6 1.8-V AC Electrical Characteristics

Unless otherwise specified, all limits ensured for T_J = 25°C, V^+ = 1.8 V, V^- = 0 V, V_{CM} = 0.5 V, V_O = V^+/2 and R_L > 1 MΩ to V^-.

PARAMETER		CONDITION	MIN[1]	TYP[2]	MAX[1]	UNIT
t_{PHL}	Propagation Delay (High to Low)	Input Overdrive = 20 mV Load = 50 pF//5 kΩ		880		ns
		Input Overdrive = 50 mV Load = 50 pF//5 kΩ		570		ns
t_{PLH}	Propagation Delay (Low to High)	Input Overdrive = 20 mV Load = 50 pF//5 kΩ		1100		ns
		Input Overdrive = 50 mV Load = 50 pF//5 kΩ		800		ns

(1) All limits are ensured by testing or statistical analysis.
(2) Typical values represent the most likely parametric norm.

6.7 2.7-V Electrical Characteristics

Unless otherwise specified, all limits ensured for T_J = 25°C, V^+ = 2.7 V, V^- = 0 V.

PARAMETER		CONDITIONS	MIN(1)	TYP(2)	MAX(1)	UNIT
V_{OS}	Input Offset Voltage			0.3	4	mV
		At the temperature extremes			6	
TC V_{OS}	Input Offset Temperature Drift	V_{CM} = 1.35 V(3)		20		µV/°C
I_B	Input Bias Current			10		nA
I_{OS}	Input offset Current			200		pA
I_S	Supply Current			9	13	µA
		At the temperature extremes			15	
I_{SC}	Output Short Circuit Current	Sinking, V_O = 1.35 V	10	15		mA
V_{OL}	Output Voltage Low	I_O = −0.5 mA		50	70	mV
		I_O = −2 mA		155	220	
V_{CM}	Input Common Voltage Range	CMRR > 45 dB	−0.1		2.8	V
CMRR	Common-Mode Rejection Ratio	0 < V_{CM} < 2.7 V	46	78		dB
PSRR	Power Supply Rejection Ratio	V^+ = 1.8 V to 5 V	55	80		dB
$I_{LEAKAGE}$	Output Leakage Current	V_O = 2.7 V		2		pA

(1) All limits are ensured by testing or statistical analysis.
(2) Typical values represent the most likely parametric norm.
(3) Offset Voltage average drift determined by dividing the change in V_{OS} at temperature extremes into the total temperature change.

6.8 2.7-V AC Electrical Characteristics

Unless otherwise specified, all limits ensured for T_J = 25°C, V^+ = 2.7 V, V^- = 0 V, V_{CM} = 0.5 V, V_O = V^+/2 and R_L > 1 MΩ to V^-.

PARAMETER		CONDITION	MIN(1)	TYP(2)	MAX(1)	UNIT
t_{PHL}	Propagation Delay (High to Low)	Input Overdrive = 20 mV Load = 50 pF//5 kΩ		1200		ns
		Input Overdrive = 50 mV Load = 50 pF//5 kΩ		810		ns
t_{PLH}	Propagation Delay (Low to High)	Input Overdrive = 20 mV Load = 50 pF//5 kΩ		1300		ns
		Input Overdrive = 50 mV Load = 50 pF//5 kΩ		860		ns

(1) All limits are ensured by testing or statistical analysis.
(2) Typical values represent the most likely parametric norm.

6.9 5-V Electrical Characteristics

Unless otherwise specified, all limits ensured for T_J = 25°C, V^+ = 5 V, V^- = 0 V.

PARAMETER		CONDITIONS	MIN(1)	TYP(2)	MAX(1)	UNIT
V_{OS}	Input Offset Voltage			0.3	4	mV
		At the temperature extremes			6	
TC V_{OS}	Input Offset Temperature Drift	V_{CM} = 2.5 V(3)		20		µV/°C
I_B	Input Bias Current			10		nA
I_{OS}	Input Offset Current			200		pA
I_S	Supply Current			10	14	µA
		At the temperature extremes			16	
I_{SC}	Output Short Circuit Current	Sinking, V_O = 2.5 V	18	34		mA
V_{OL}	Output Voltage Low	I_O = −0.5 mA		27	70	mV
		I_O = −4.0 mA		225	315	

(1) All limits are ensured by testing or statistical analysis.
(2) Typical values represent the most likely parametric norm.
(3) Offset Voltage average drift determined by dividing the change in V_{OS} at temperature extremes into the total temperature change.

5-V Electrical Characteristics (continued)

Unless otherwise specified, all limits ensured for T_J = 25°C, V^+ = 5 V, V^- = 0 V.

PARAMETER		CONDITIONS	MIN(1)	TYP(2)	MAX(1)	UNIT
V_{CM}	Input Common Voltage Range	CMRR > 45 dB	−0.1		5.1	V
CMRR	Common-Mode Rejection Ratio	0 < V_{CM} < 5.0 V	46	78		dB
PSRR	Power Supply Rejection Ratio	V^+ = 1.8 V to 5 V	55	80		dB
$I_{LEAKAGE}$	Output Leakage Current	V_O = 5 V		2		pA

6.10 5-V AC Electrical Characteristics

Unless otherwise specified, all limits ensured for T_J = 25°C, V^+ = 5.0 V, V^- = 0 V, V_{CM} = 0.5 V, V_O = V^+/2 and R_L > 1 MΩ to V^-.

PARAMETER		CONDITION	MIN(1)	TYP(2)	MAX(1)	UNIT
t_{PHL}	Propagation Delay (High to Low)	Input Overdrive = 20 mV Load = 50 pF//5 kΩ		2100		ns
		Input Overdrive = 50 mV Load = 50 pF//5 kΩ		1380		ns
t_{PLH}	Propagation Delay (Low to High)	Input Overdrive = 20 mV Load = 50 pF//5 kΩ		1800		ns
		Input Overdrive = 50 mV Load = 50 pF//5 kΩ		1100		ns

(1) All limits are ensured by testing or statistical analysis.
(2) Typical values represent the most likely parametric norm.

6.11 Typical Characteristics

T_A = 25°C, Unless otherwise specified.

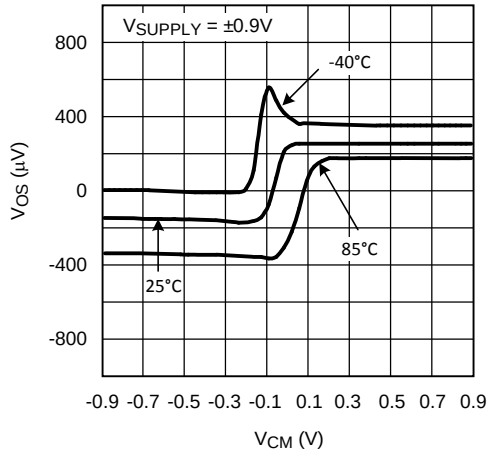


Figure 1. V_{OS} vs. V_{CM}

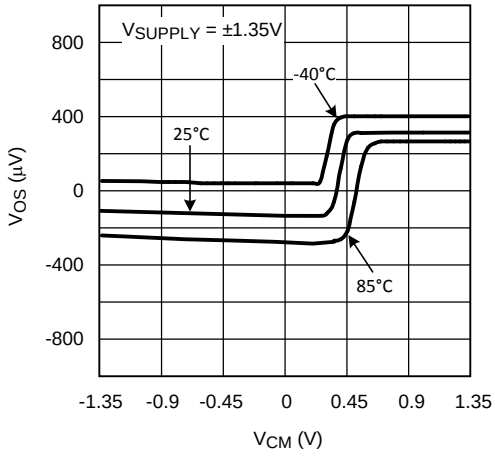


Figure 2. V_{OS} vs. V_{CM}

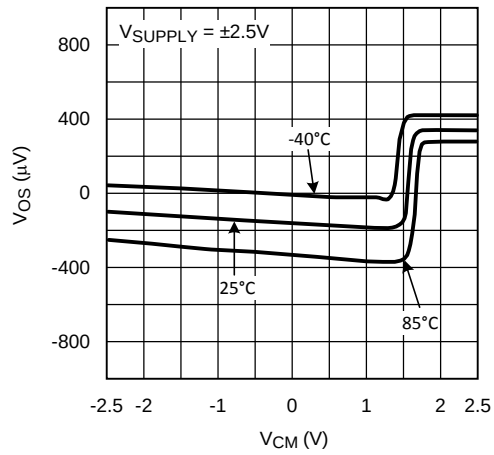


Figure 3. V_{OS} vs. V_{CM}

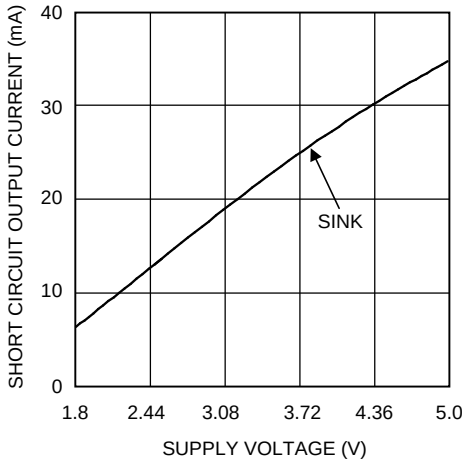


Figure 4. Short Circuit vs. Supply Voltage

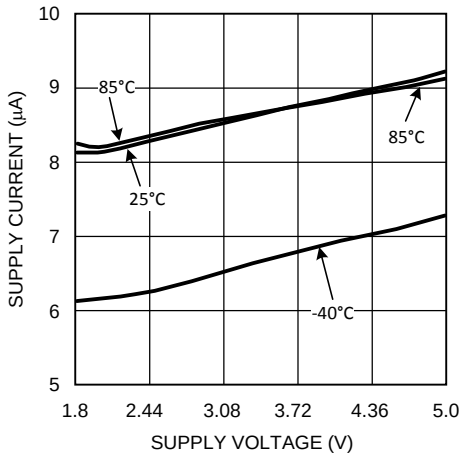


Figure 5. Supply Current vs. Supply Voltage

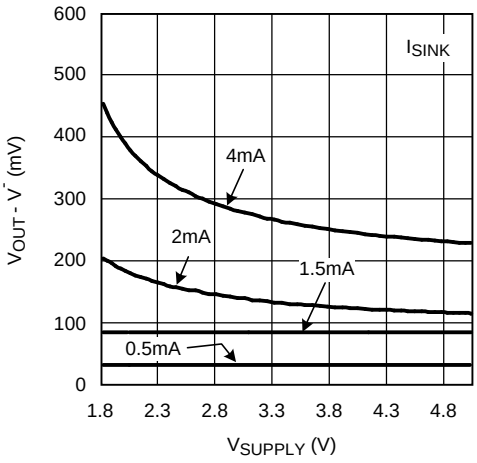


Figure 6. Output Negative Swing vs. V_{SUPPLY}

Typical Characteristics (continued)

T_A = 25°C, Unless otherwise specified.

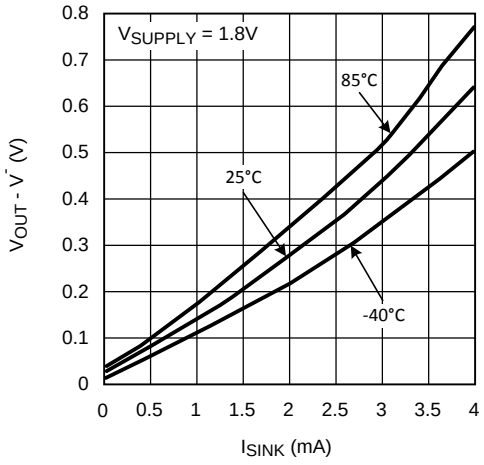


Figure 7. Output Negative Swing vs. I_{SINK}

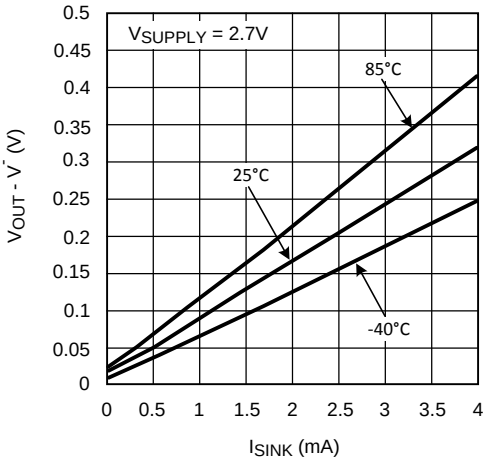


Figure 8. Output Negative Swing vs. I_{SINK}

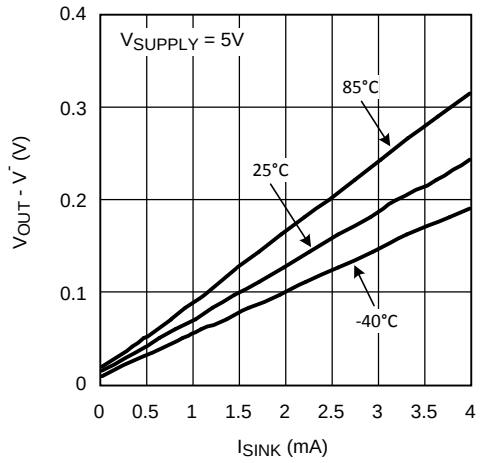


Figure 9. Output Negative Swing vs. I_{SINK}

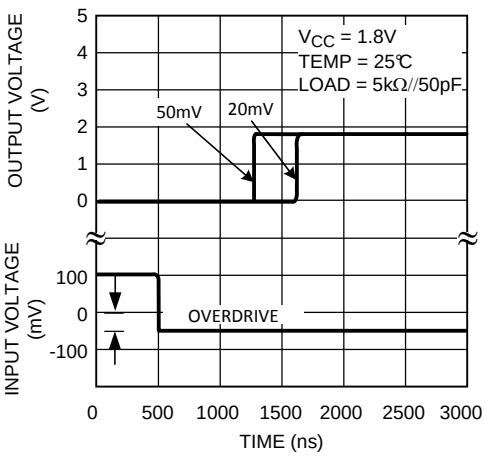


Figure 10. Propagation Delay (t_{PLH})

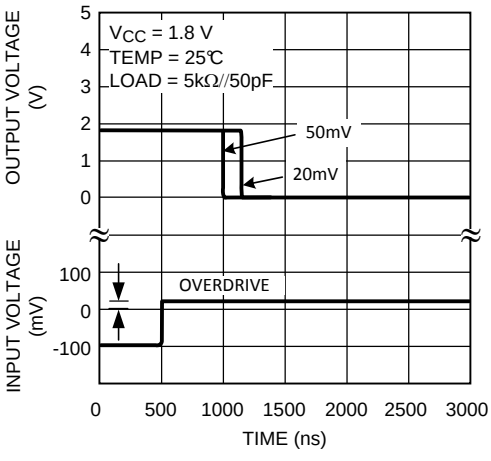


Figure 11. Propagation Delay (t_{PHL})

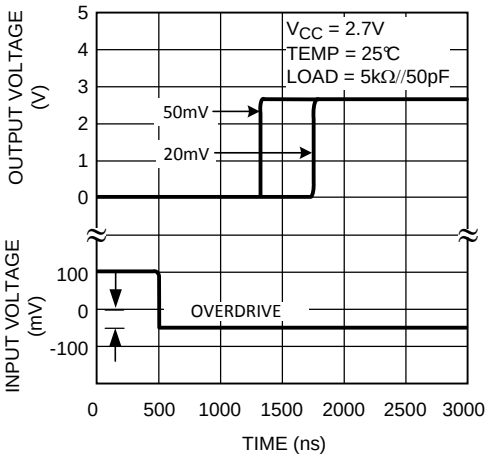


Figure 12. Propagation Delay (t_{PLH})

Typical Characteristics (continued)

T_A = 25°C, Unless otherwise specified.

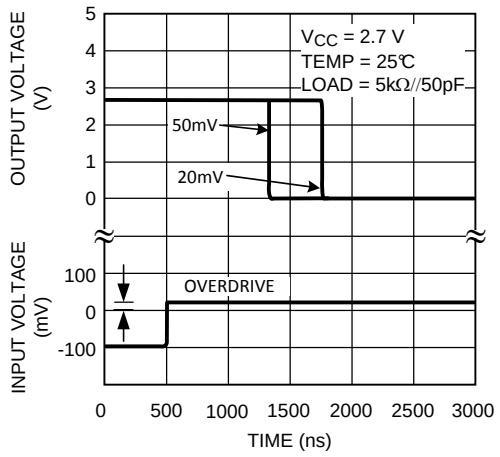


Figure 13. Propagation Delay (t_{PHL})

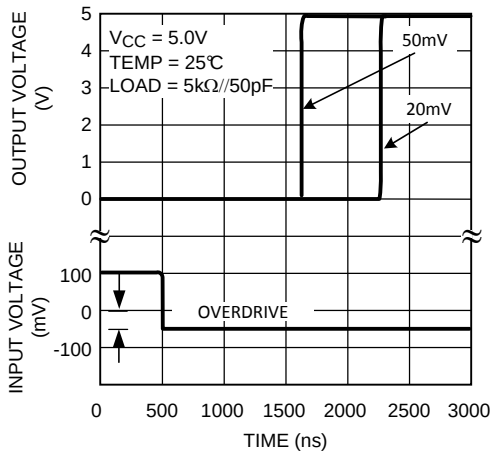


Figure 14. Propagation Delay (t_{PLH})

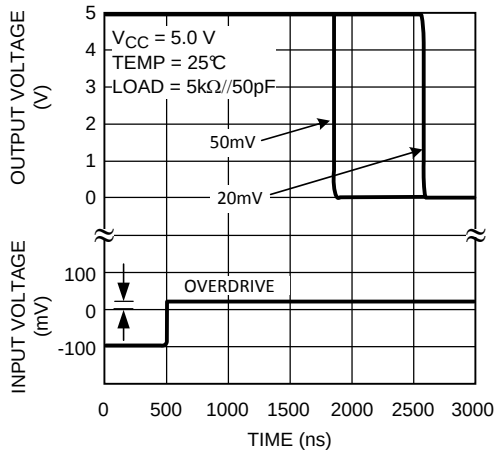


Figure 15. Propagation Delay (t_{PHL})

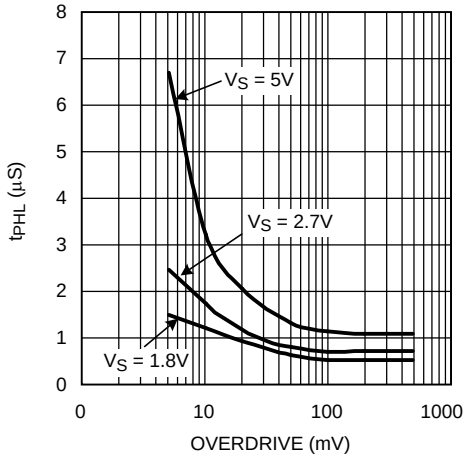


Figure 16. t_{PHL} vs. Overdrive

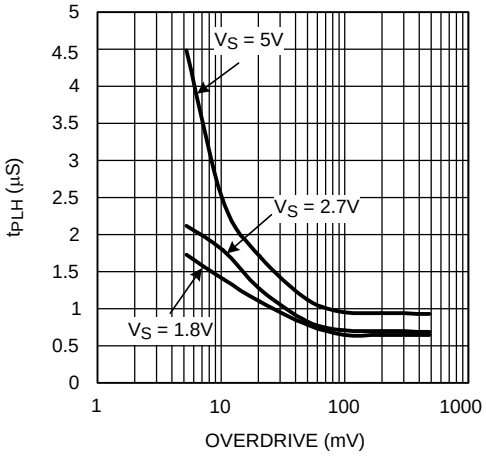


Figure 17. t_{PLH} vs. Overdrive

7 Detailed Description

7.1 Overview

A comparator is often used to convert an analog signal to a digital signal. As shown in Figure 18, the comparator compares an input voltage (V_{IN}) to a reference voltage (V_{REF}). If V_{IN} is less than V_{REF}, the output transistor turns on and pulls the output to V-, and thus the output (V_O) goes low.

However, if V_{IN} is greater than V_{REF}, the output transistor turns off and the voltage (V_O) is pulled high by the external pull-up resistor.

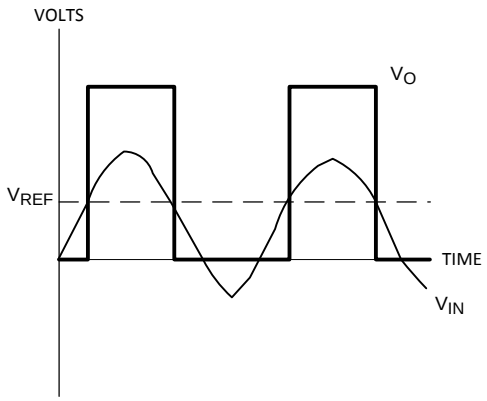
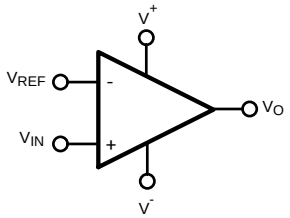


Figure 18. Basic Comparator

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Rail-to-Rail Input Stage

The LMV7275-Q1 has an input common mode voltage range (V_{CM}) of −0.1V below the V^- to 0.1 V above V^+. This is achieved by using paralleled PNP and NPN differential input pairs. When the V_{CM} is near V^+, the NPN pair is on and the PNP pair is off. When the V_{CM} is near V^-, the NPN pair is off and the PNP pair is on. The crossover point between the NPN and PNP input stages is around 950mV from V^+. Because each input stage has its own offset voltage (V_{OS}), the V_{OS} of the comparator becomes a function of the V_{CM}. See curves for V_{OS} vs. V_{CM} in the *Typical Characteristics* section. In application design, it is recommended to keep the V_{CM} away from the crossover point to avoid problems. The wide input voltage range makes LMV7275-Q1 ideal in power supply monitoring circuits, where the comparators are used to sense signals close to ground and power supplies.

Feature Description (continued)

7.3.2 Output Stage

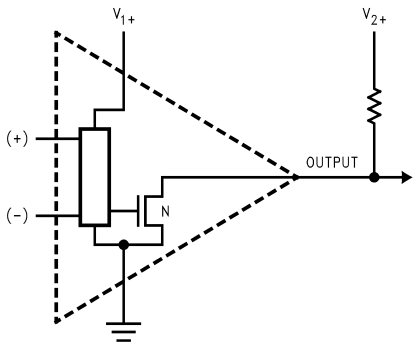


Figure 19. LMV7275-Q1 Open-Drain Output

The LMV7275-Q1 has an open-drain output that requires a pull-up resistor to a positive supply voltage for the output to operate properly. When the internal output transistor is off, the output voltage will be pulled up to the external positive voltage (V_{2+}) by the external pull-up resistor. This allows the output to be OR'ed with other open-drain outputs on the same bus.

The output pull-up resistor may be connected to any voltage level between V- and V+ for level shifting applications.

7.4 Device Functional Modes

7.4.1 Capacitive and Resistive Loads

The propagation delay on the rising edge of the LMV7275-Q1 depends on the load resistance and capacitance values.

7.4.2 Noise

Most comparators have rather low gain. This allows the output to alternate between high and low when the input signal changes slowly. The result is the output may oscillate between high and low when the differential input is near zero and triggers on noise. The high gain of this comparator eliminates this problem. Less than 1 μV of change on the input will drive the output from one rail to the other rail. If the input signal is noisy, the output cannot ignore the noise unless some hysteresis is provided by positive feedback. (See *Hysteresis*.)

7.4.3 Hysteresis

It is a standard procedure to use hysteresis (positive feedback) around a comparator to prevent oscillation due to the comparator triggering its own noise on slowly ramping signals. The following sections will describe various ways to apply hysteresis.

7.4.3.1 Non-inverting Comparator With Hysteresis

Non-inverting comparator with hysteresis requires a two resistor network, and a voltage reference (V_{ref}) at the inverting input. When V_{in} is low, the output is also low. For the output to switch from low to high, V_{in} must rise up to V_{in1} where V_{in1} is calculated by:

$$V_{in1} = \frac{V_{ref}(R_1 + R_2)}{R_2} \quad (1)$$

When V_{in} is high, the output is also high. To make the comparator switch back to its low state, V_{in} must equal V_{ref} before V_A will again equal V_{ref}. V_{in} can be calculated by:

$$V_{in2} = \frac{V_{ref}(R_1 + R_2) - V_{CC}R_1}{R_2} \quad (2)$$

The hysteresis of this circuit is the difference between V_{in1} and V_{in2}.

Device Functional Modes (continued)

$$\Delta V_{in} = V_{CC} R_1 / R_2 \quad (3)$$

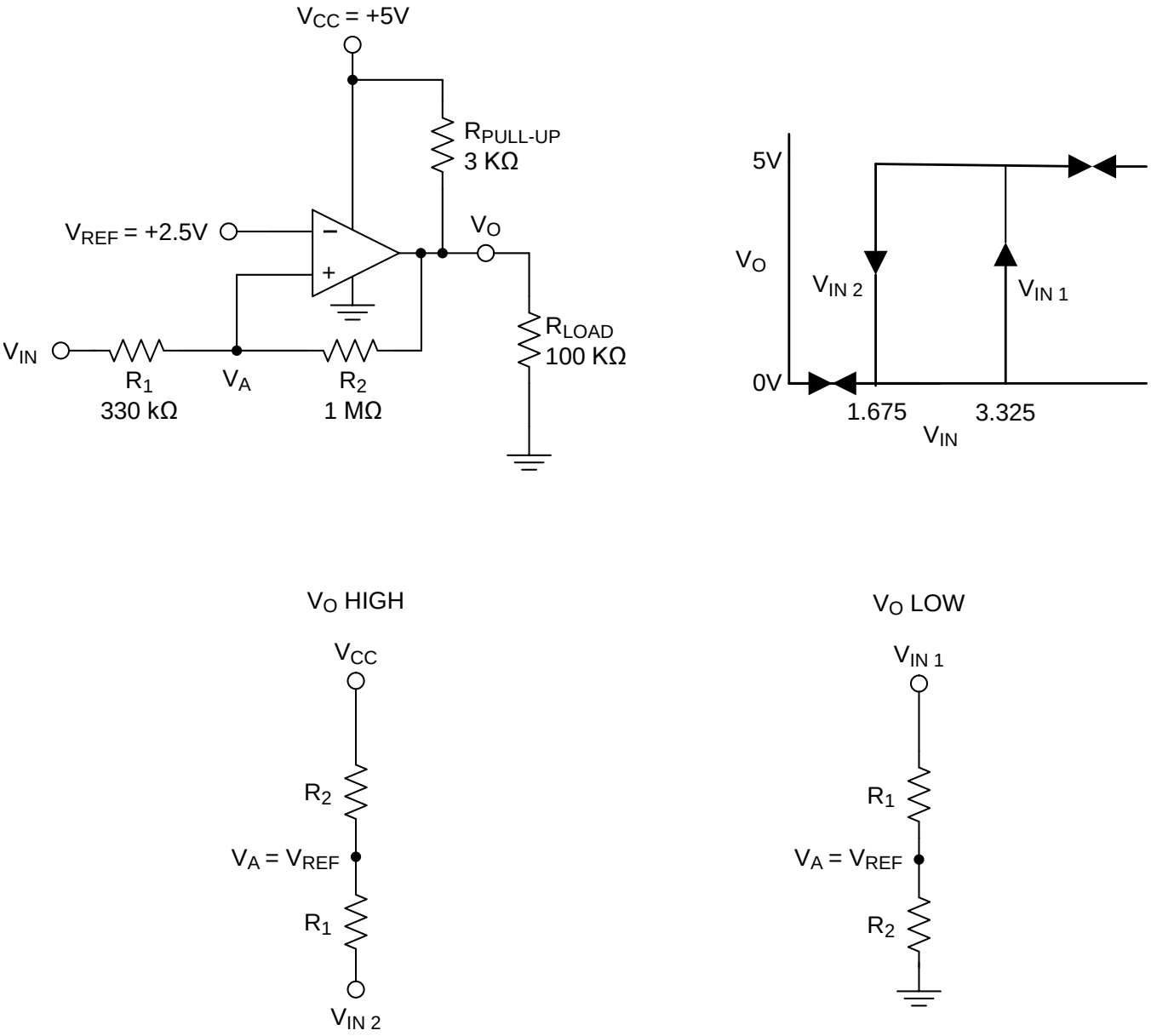


Figure 20. Non-Inverting Comparator With Hysteresis

7.4.3.2 Inverting Comparator With Hysteresis

The inverting comparator with hysteresis requires a three resistor network that are referenced to the supply voltage V_{CC} of the comparator. When V_{in} at the inverting input is less than V_a, the voltage at the non-inverting node of the comparator ($V_{in} < V_a$), the output voltage is high (for simplicity assume V_O switches as high as V_{CC}). The three network resistors can be represented as $R_1//R_3$ in series with R_2. The lower input trip voltage V_{a1} is defined as:

$$V_{a_1} = \frac{V_{CC} \; R_2}{(R_1 \,||\, R_3) + R_2} \quad (4)$$

When V_{in} is greater than V_a ($V_{in} > V_a$), the output voltage is low very close to ground. In this case the three network resistors can be presented as $R_2//R_3$ in series with R_1. The upper trip voltage V_{a2} is defined as:

Device Functional Modes (continued)

$$V_{a2} = \frac{V_{CC}(R_2 // R_3)}{R_1 + (R_2 // R_3)} \quad (5)$$

The total hysteresis provided by the network is defined as:

$$\Delta V_a = V_{a1} - V_{a2} \quad (6)$$

To assure that the comparator will always switch fully to V_{CC} and not be pulled down by the load the resistors values should be chosen as follow:

$$R_{PULL-UP} << R_{LOAD} \quad (7)$$

and $R_1 > R_{PULL-UP}$. (8)

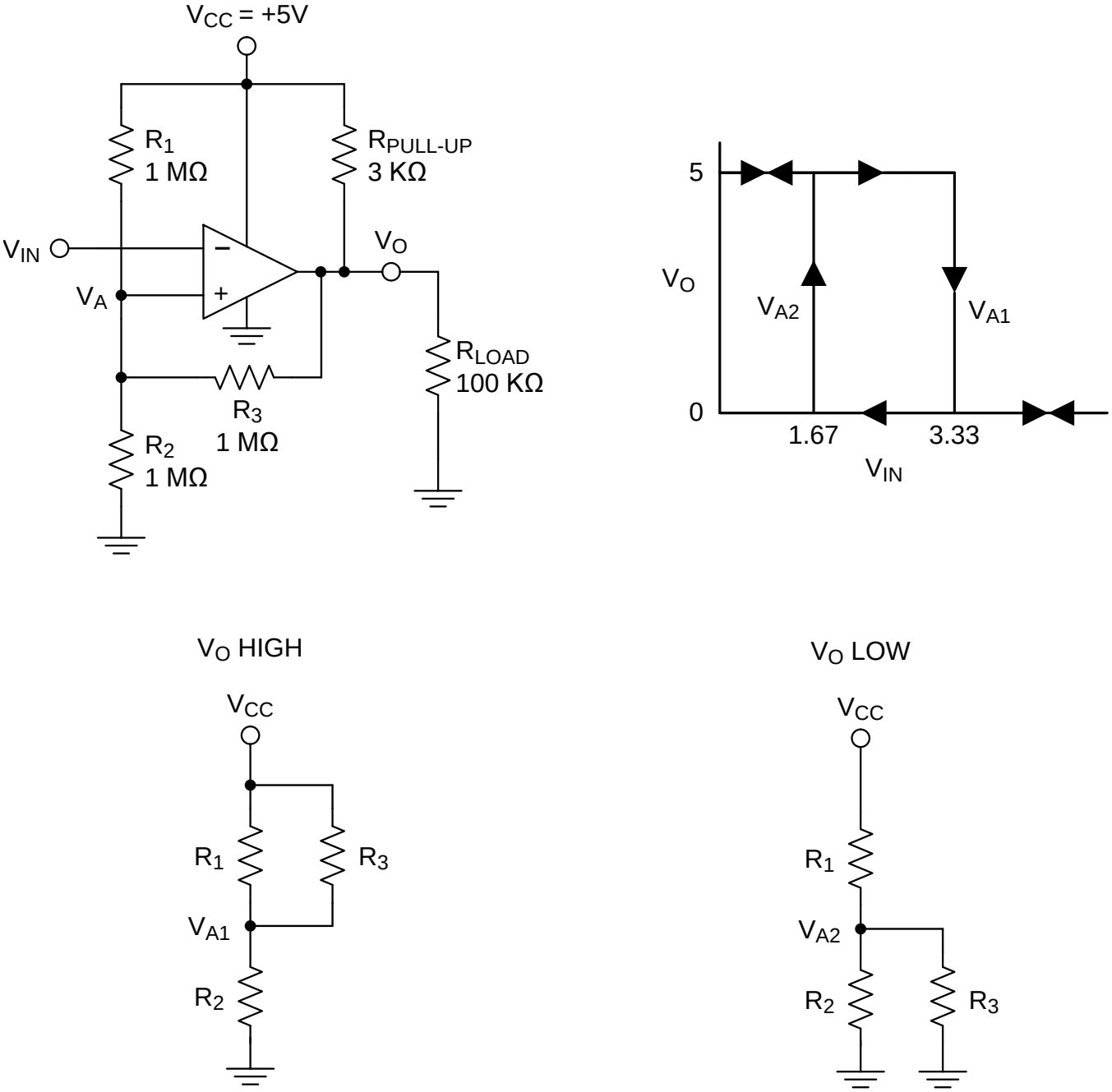


Figure 21. Inverting Comparator With Hysteresis

Device Functional Modes (continued)

7.4.4 Zero Crossing Detector

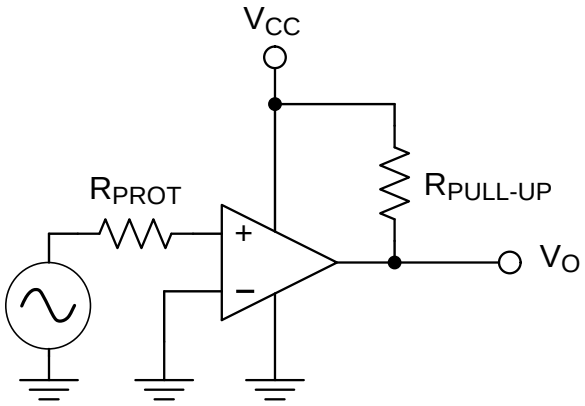


Figure 22. Simple Zero Crossing Detector

In a zero crossing detector circuit, the inverting input is connected to ground and the Non-Inverting input is connected to a 100 mV_{PP} AC signal. As the signal at the Non-Inverting input crosses 0 V, the output of the comparator changes state.

R_{PROT} is an optional input protection resistor to limit the current should the input voltage exceed the supply rails. R_{PROT} should be a minimum of 1 kΩ per volt of expected over-voltage and limit the current to less than ±1mA under worst case fault conditions.

7.4.4.1 Zero Crossing Detector With Hysteresis

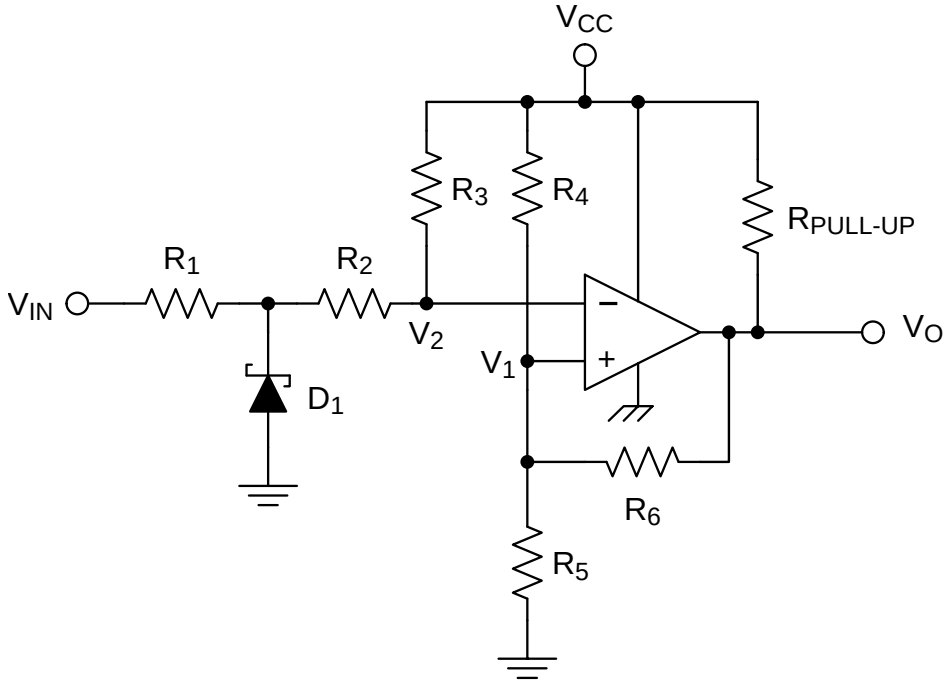


Figure 23. Zero Crossing Detector With Hysteresis

To improve switching times and centering the input threshold to ground a small amount of positive feedback is added to the circuit. Voltage divider R_4 and R_5 establishes a reference voltage, V_1, at the positive input. By making the series resistance, R_1 plus R_2 equal to R_5, the switching condition, $V_1 = V_2$, will be satisfied when $V_{IN} = 0$.

Device Functional Modes (continued)

The positive feedback resistor, R_6, is made very large (with respect to R_5 || R_6 = 2000 R_5). The resultant hysteresis established by this network is very small (ΔV_1 < 10 mV) but it is sufficient to insure rapid output voltage transitions.

Diode D_1 is used to insure that the inverting input terminal of the comparator never goes below approximately −100 mV. As the input terminal goes negative, D_1 will forward bias, clamping the node between R_1 and R_2 to approximately −300 mV. This sets up a voltage divider with R_2 and R_3 preventing V_2 from going below ground. The maximum negative input overdrive is limited by the current handling ability of D_1.

7.4.5 Threshold Detector

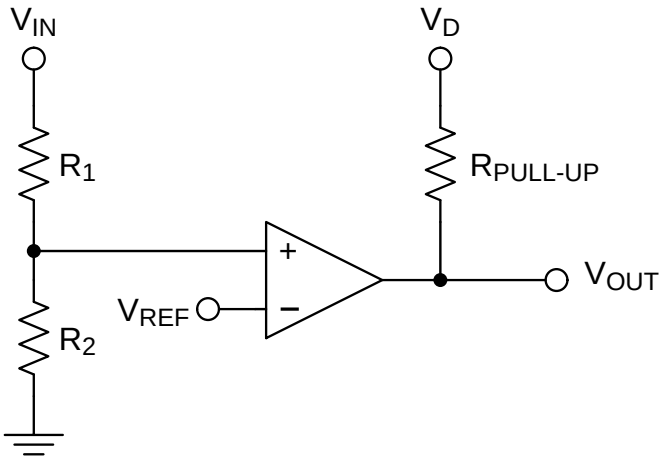


Figure 24. Threshold Detector

Instead of tying the inverting input to 0 V, the inverting input can be tied to a reference voltage. As the input on the Non-Inverting input passes the V_{REF} threshold, the output of the comparator changes state. It is important to use a stable reference voltage to ensure a consistent switching point.

7.4.6 Universal Logic Level Shifter

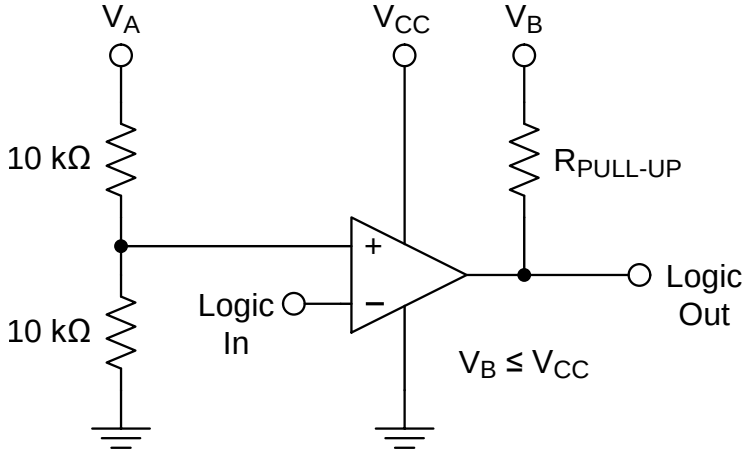


Figure 25. Logic Level Shifter

The output of LMV7275-Q1 is an unconnected drain of an NMOS device, which can be pulled up, through a resistor, to any desired output level below the comparators power supply voltage ($V_B \leq V_{CC}$). Hence, the following simple circuit works as a universal logic level shifter, pulling up the signal to the desired level.

Device Functional Modes (continued)

For example, V_A could be the 5-V analog supply voltage, where V_B could be the 3.3-V supply of the processor. The output will now be compatible with the 3.3-V logic.

7.4.7 OR'ING the Output

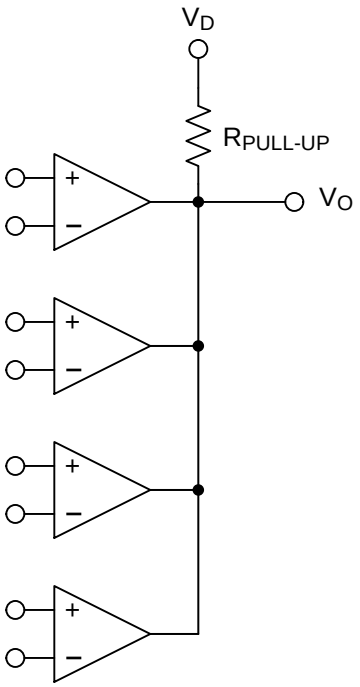


Figure 26. OR'ing the Outputs

Open-drain outputs may be tied together, pulled up to V_D by a common resistor to provide an output OR'ing function. If any of the comparator outputs goes low, the output V_O goes low.

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The LMV7275-Q1 is a single-supply comparator with 880 ns of propagation delay and only 12 µA of supply current.

8.2 Typical Applications

8.2.1 Square Wave Oscillator

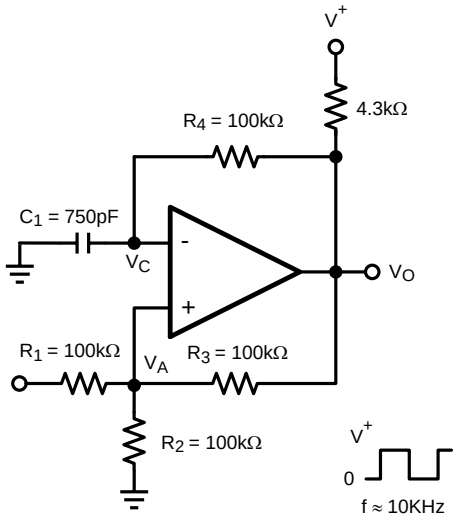


Figure 27. Square Wave Oscillator Application

8.2.1.1 Design Requirements

A typical application for a comparator is as a square wave oscillator. Figure 27 generates a square wave whose period is set by the RC time constant of the capacitor $C_1$and resistor R_4. The maximum frequency is limited by the large signal propagation delay of the comparator, and by the capacitive loading at the output, which limits the output slew rate.

8.2.1.2 Detailed Design Procedure

To analyze the circuit, consider it when the output is high. That implies that the inverted input (V_C) is lower than the Non-Inverting input (V_A).

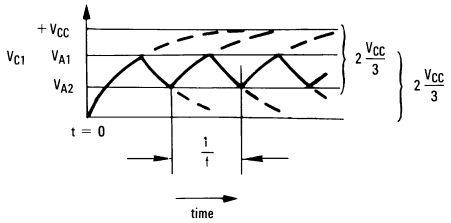


Figure 28. Squarewave Oscillator Timing Thresholds

Typical Applications (continued)

This causes the C_1 to get charged through R_4, and the voltage V_C increases till it is equal to the Non-Inverting input. The value of V_A at this point is

$$V_{A1} = \frac{V_{CC} \cdot R_2}{R_2 + R_1 \| R_3} \tag{9}$$

If $R_1 = R_2 = R_3$, then $V_{A1} = 2V_{CC}/3$

At this point the comparator switches pulling down the output to the negative rail. The value of V_A at this point is

$$V_{A2} = \frac{V_{CC} (R_2 \| R_3)}{R_1 + (R_2 \| R_3)} \tag{10}$$

If $R_1 = R_2 = R_3$, then $V_{A2} = V_{CC}/3$

The capacitor C_1 now discharges through R_4, and the voltage V_C decreases till it is equal to V_{A2}, at which point the comparator switches again, bringing it back to the initial stage. The time period is equal to twice the time it takes to discharge C_1 from $2V_{CC}/3$ to $V_{CC}/3$, which is given by $R_4C_1.\ln 2$. Hence the formula for the frequency is:

$F = 1/(2 \cdot R_4 \cdot C_1 \cdot \ln 2)$

8.2.1.3 Application Curve

Figure 29 shows the simulated results of an oscillator using the following values:

1. $R_1 = R_2 = R_3 = R_4 = 100\ k\Omega$
2. $C_1 = 750$ pF, $C_L = 20$ pF
3. V+ = 5 V, V- = GND
4. C_{STRAY} (not shown) from Va to GND = 10 pF

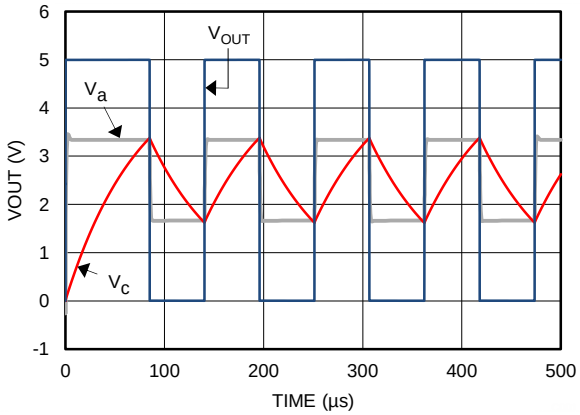


Figure 29. Square Wave Oscillator Output Waveforms

Typical Applications (continued)

8.2.2 Positive Peak Detector

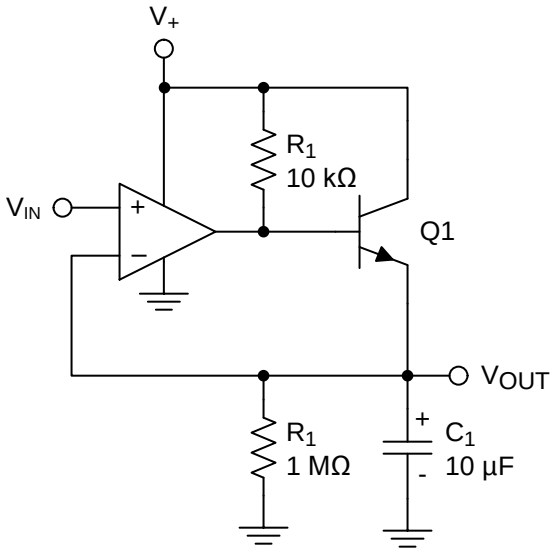


Figure 30. Positive Peak Detector

The positive peak detector is basically the comparator operated as a unity gain follower with a large holding capacitor from the output to ground. A transistor is added to the output to provide a low impedance current source. The upper output swing is limited by the emitter-base forward voltage. This allows capture of the most positive input signal between 0 V and (V+) - 0.7V.

When the output of the comparator goes high, current is passed through the transistor to charge up the capacitor. The only discharge path will be the 1-MΩ resistor shunting C1 and any load that is connected to the output. The decay time can be altered simply by changing the 1-MΩ resistor.

8.2.3 Negative Peak Detector

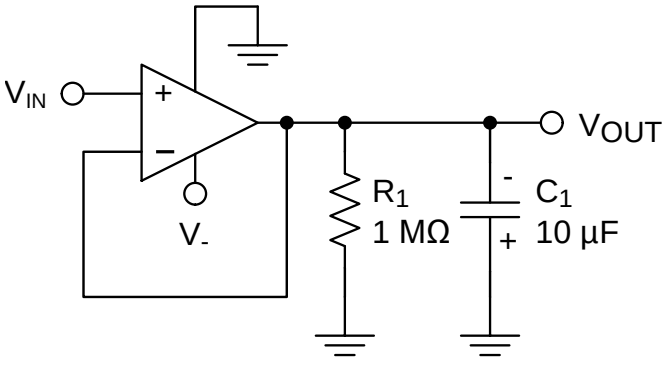


Figure 31. Negative Peak Detector for Negative Supply

The Negative Peak Detector circuit will store the peak negative voltage below ground (0 V to V-). For the negative detector, the output transistor acts as a low-impedance current sink.

When V_{IN} is more negative than V_{OUT}, the output transistor will conduct and pull the output to $-V_{CC}$, charging C1. Charging stops when C_1 reaches the same level as V_{IN}. Because there is no pull-up resistor, the only discharge path will be the 1-MΩ resistor and any load impedance applied. Therefore, the decay time is set by varying the 1-MΩ resistor. Be sure to observe the polarity of C_1!

Typical Applications (continued)

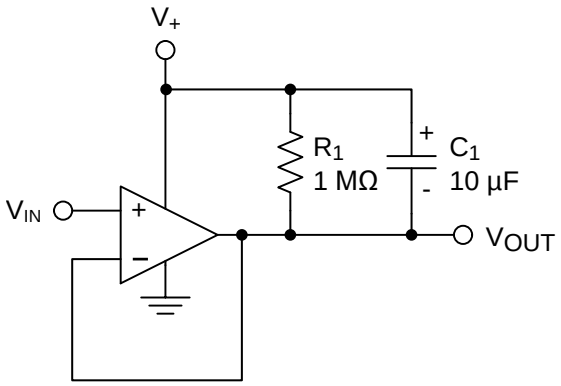


Figure 32. Negative Peak Detector for Positive Supply

An alternate positive supply version is shown in Figure 32 that will capture the lowest applied V_{IN} value between V+ and ground (V+ to 0V).

The output of either version should be buffered by a high-impedance follower stage to prevent loading of the RC circuit.

8.2.4 Window Detector

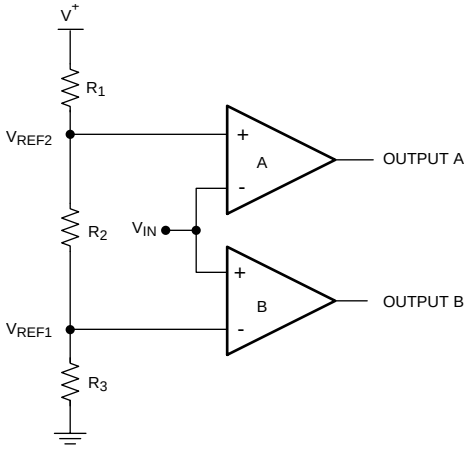


Figure 33. Window Detector

A window detector monitors the input signal to determine if it falls between two voltage levels. Both outputs are true (high) when $V_{REF1} < V_{IN} < V_{REF2}$

Typical Applications (continued)

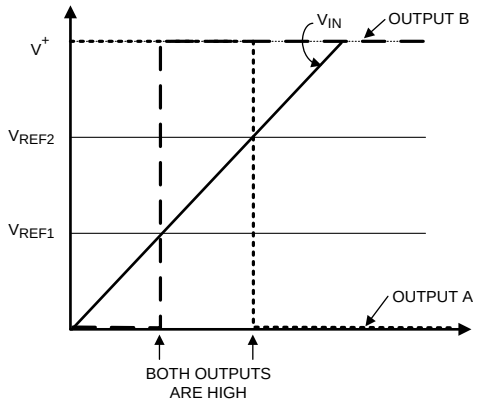


Figure 34. Window Detector Output Signal

The comparator outputs A and B are high only when $V_{REF1} < V_{IN} < V_{REF2}$, or *within the window*, where these are defined as:

$$V_{REF1} = R_3 / (R_1 + R_2 + R_3) \times V+ \quad (11)$$

$$V_{REF2} = (R_2 + R_3) / (R_1 + R_2 + R_3) \times V+ \quad (12)$$

To determine if the input signal falls outside of the two voltage levels, both inputs on each comparators can be reversed to invert the logic.

The outputs should be tied together and use a shared pull-up resistor for a common logic output. If individual limit outputs are needed, then each output will require it's own pull-up resistor.

Other names for window detectors are: threshold detector, level detector, and amplitude trigger or detector.

9 Power Supply Recommendations

To minimize supply noise, power supplies should be decoupled by a 0.01-µF ceramic capacitor in parallel with a 10-µF capacitor.

Due to the nanosecond edges on the output transition, peak supply currents will be drawn during the time the output is transitioning. Peak current depends on the capacitive loading on the output. The output transition can cause transients on poorly bypassed power supplies. These transients can cause a poorly bypassed power supply to *ring* due to trace inductance and low self-resonance frequency of high ESR bypass capacitors.

Treat the LMV7275-Q1 as a high-speed device. Keep the ground paths short and place small (low-ESR ceramic) bypass capacitors directly between the V+ and V– pins.

Output capacitive loading and output toggle rate will cause the average supply current to rise over the quiescent current.

10 Layout

10.1 Layout Guidelines

10.1.1 Circuit Techniques for Avoiding Oscillations in Comparator Applications

Feedback to almost any pin of a comparator can result in oscillation. In addition, when the input signal is a slow voltage ramp or sine wave, the comparator may also burst into oscillation near the crossing point. To avoid oscillation or instability, PCB layout should be engineered thoughtfully. Several precautions are recommended:

1. Power supply bypassing is critical, and will improve stability and response time. Resistance and inductance from power supply wires and board traces increase power supply line impedance. When supply current changes, the power supply line will move due to its impedance. Large enough supply line shift will cause the comparator to malfunction. To avoid problems, a small bypass capacitor, such as 0.1-µF ceramic, should be placed immediately adjacent to the supply pins. An additional 6.8 µF or greater tantalum capacitor should be placed at the point where the power supply for the comparator is introduced onto the board. These capacitors act as an energy reservoir and keep the supply impedance low. In a dual-supply application, a 0.1-µF capacitor is recommended to be placed across V^+ and V^- pins.
2. Keep all leads short to reduce stray capacitance and lead inductance. It will also minimize any unwanted coupling from any high-level signals (such as the output). The comparators can easily oscillate if the output lead is inadvertently allowed to capacitively couple to the inputs through stray capacitance. This shows up only during the output voltage transition intervals as the comparator changes states. Try to avoid a long loop which could act as an inductor (coil).
3. It is a good practice to use an unbroken ground plane on a printed-circuit-board to provide all components with a low inductive ground connection. Make sure ground paths are low-impedance where heavier currents are flowing to avoid ground level shift. Preferably there should be a ground plane under the component.
4. The output trace should be routed away from inputs. The ground plane should extend between the output and inputs to act as a guard. This can be achieved by running a topside ground plane between the output and inputs. A typical PCB layout is shown in Figure 35.
5. When the signal source is applied through a resistive network to one input of the comparator, it is usually advantageous to connect the other input with a resistor with the same value, for both DC and AC consideration. Input traces should be laid out symmetrically if possible.

10.2 Layout Example

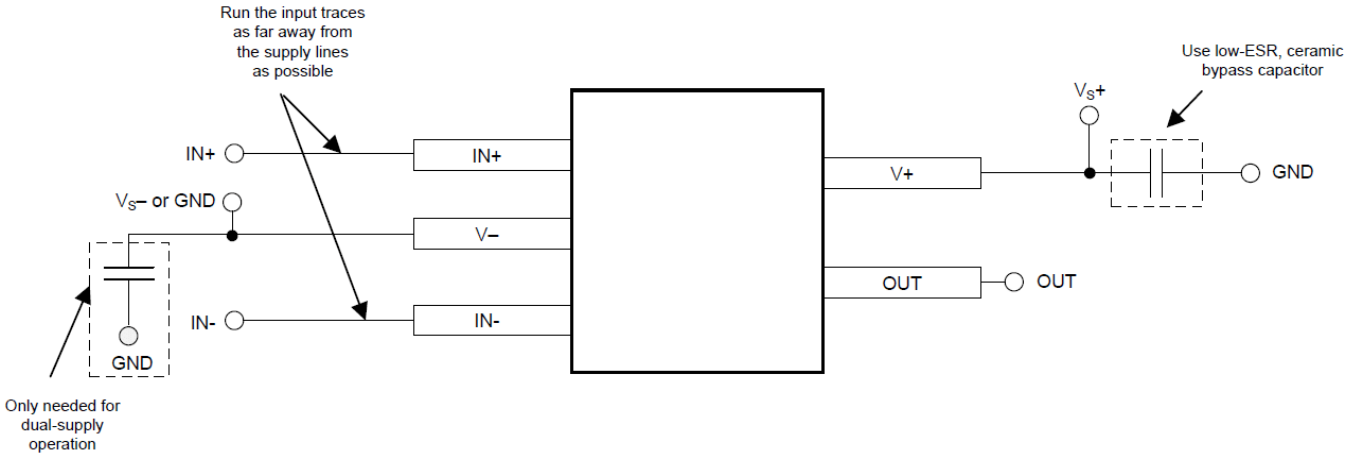


Figure 35. Typical PCB Layout

11 器件和文档支持

11.1 器件支持

11.1.1 开发支持

相关开发支持请参阅以下文档：

- 《LMV7275 PSPICE 模型》，SNOM555
- TINA-TI 基于 SPICE 的模拟仿真程序，http://www.ti.com.cn/tool/cn/tina-ti
- DIP 适配器评估模块，http://www.ti.com.cn/tool/cn/dip-adapter-evm
- TI 通用运行放大器评估模块，http://www.ti.com.cn/tool/cn/opampevm

11.2 文档支持

11.2.1 相关文档

相关文档如下：

- AN-74《四个独立运行的比较器》，SNOA654

11.3 社区资源

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.4 商标

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

11.5 静电放电警告

这些装置包含有限的内置 ESD 保护。 存储或装卸时，应将导线一起截短或将装置放置于导电泡棉中，以防止 MOS 门极遭受静电损伤。

11.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 机械、封装和可订购信息

以下页中包括机械、封装和可订购信息。这些信息是针对指定器件可提供的最新数据。这些数据会在无通知且不对本文档进行修订的情况下发生改变。欲获得该数据表的浏览器版本，请查阅左侧的导航栏。

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LMV7275IDCKRQ1	ACTIVE	SC70	DCK	5	3000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 85	SKA	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

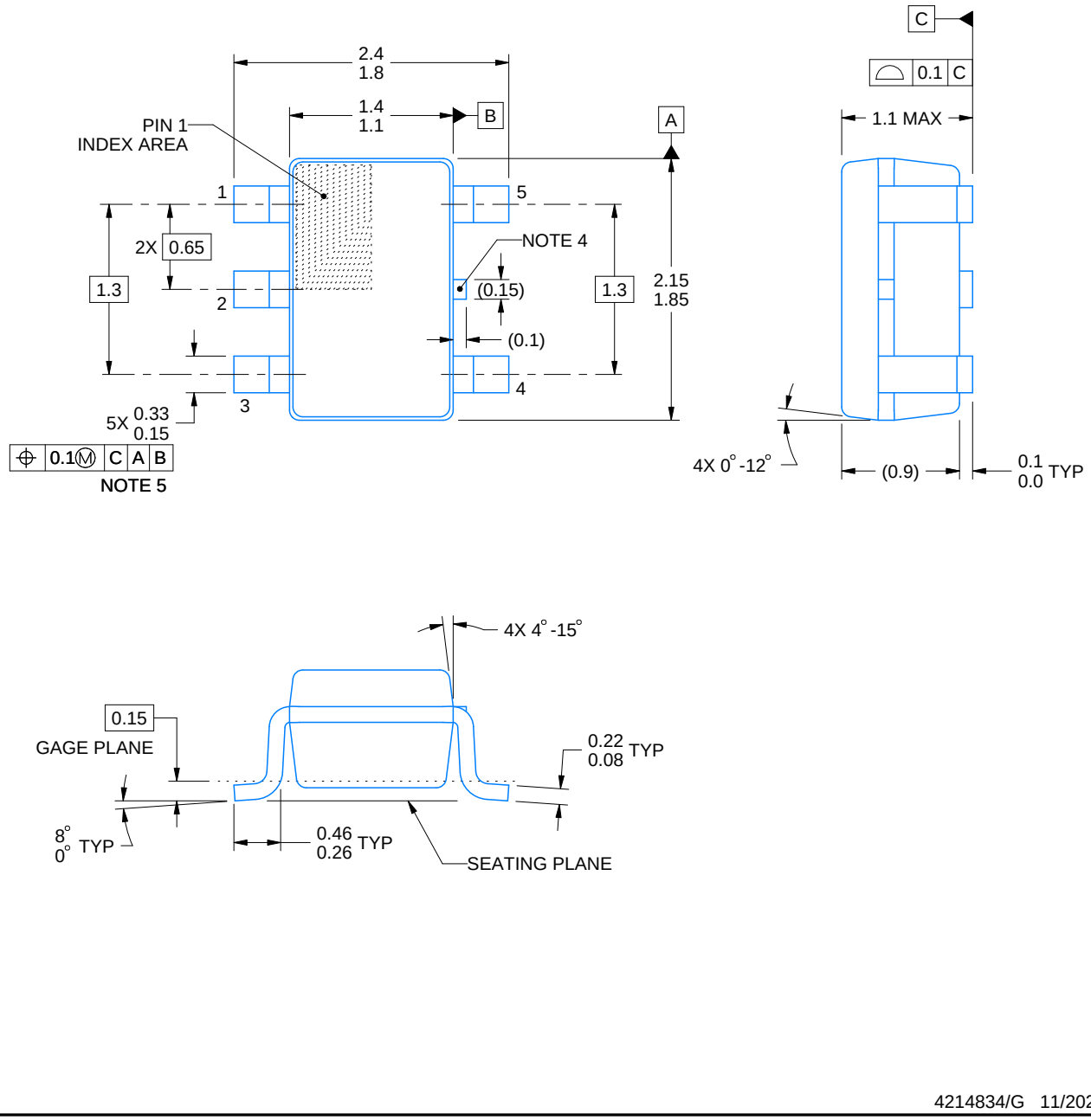
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

PACKAGE OUTLINE

DCK0005A

SOT - 1.1 max height

SMALL OUTLINE TRANSISTOR



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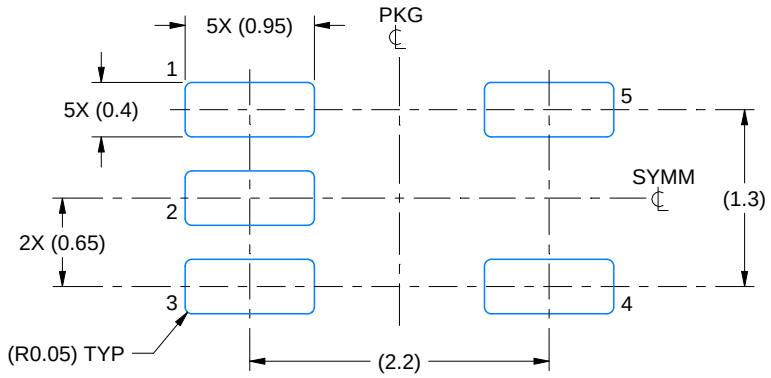
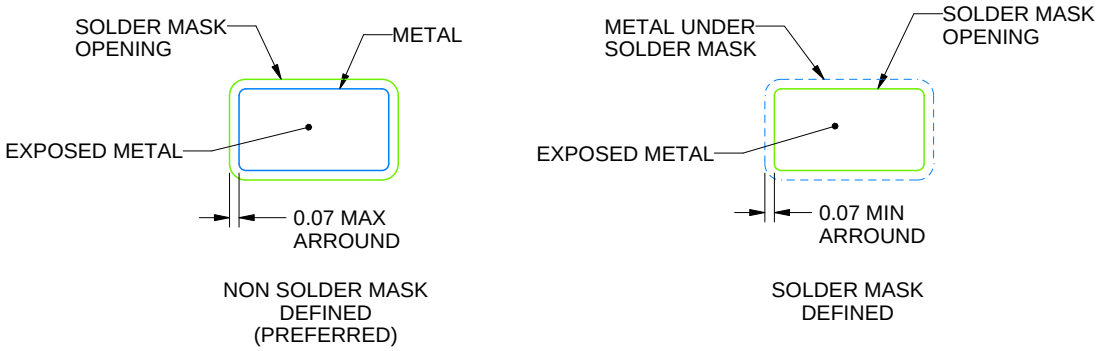
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-203.
4. Support pin may differ or may not be present.
5. Lead width does not comply with JEDEC.
6. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25mm per side



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:18X



SOLDER MASK DETAILS

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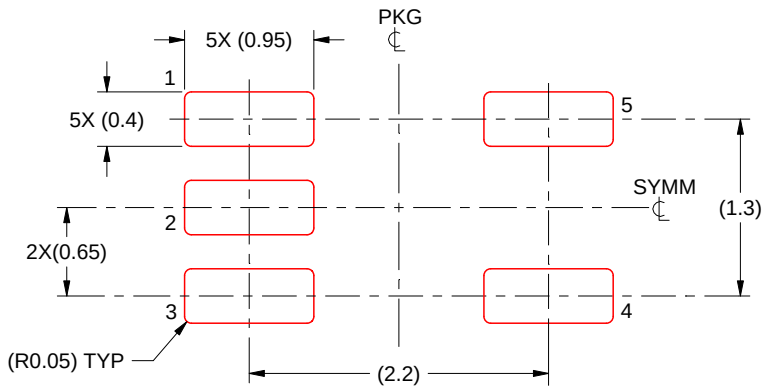
NOTES: (continued)

7. Publication IPC-7351 may have alternate designs.
8. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 THICK STENCIL
SCALE:18X

4214834/G 11/2024

NOTES: (continued)

9. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
10. Board assembly site may have different recommendations for stencil design.

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