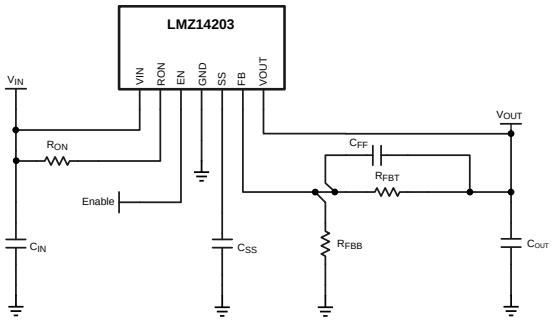
LMZ14203 SIMPLE SWITCHER® 采用引线式 SMT-TO 封装的6V 至 42V 3A 电源模块

1 特性

- 集成屏蔽电感器和简单的 PCB 布局
- 采用外部软启动和精密使能组件实现灵活启动排序
- 针对浪涌电流以及输入 UVLO 和输出短路等故障提供保护
- -40°C 至 125°C 的工作结点温范围
- 用于简单装配和制造的单个外露垫和标准引脚分配
- 针对现场可编程门阵列 (FPGA) 和特定用途集成电路 (ASIC) 供电的快速瞬态响应
- 低输出电压纹波
- 引脚到引脚兼容的系列器件：
  - LMZ1420x（最大 42V 3A、2A、1A）
  - LMZ1200x（最大 20V 3A、2A、1A）
- 针对 WEBENCH®电源设计工具完全启用
- 电气规范
  - 总输出功率最大值达 18W
  - 输出电流高达 3A
  - 输入电压范围：6V 至 42V
  - 输出电压范围：0.8V 至 6V
  - 效率高达 90%
- 性能优势
  - 在较高环境温度下运行不会降低耐热额定值
  - 高效率有效减少了系统产生的热量
  - 经过低辐射发射（电磁干扰 [EMI]）测试，符合 EN55022 B 类标准
  - 通过 10V/m 辐射抗扰性 EMI 测试，符合 EN61000 4-3 标准
- 使用 LMZ14203 并借助 WEBENCH® 电源设计器创建定制设计方案

简化应用电路原理图



2 应用

- 12V 和 24V 输入轨的负载点转换
- 空间受限且热要求高的 应用
- 负输出电压 应用
  （请参阅 AN-2027 SNVA425）

3 说明

LMZ14203 SIMPLE SWITCHER 电源模块是易于使用的降压直流/直流解决方案，可驱动高达 3A 的负载，并具有出色的电源转换效率、线路和负载调节以及输出精度。LMZ14203 采用创新型封装，可提高热性能并允许进行手工和机器焊接。

LMZ14203 支持 6V 至 42V 的输入电压轨范围，可提供低至 0.8V 的高精度可调节输出电压。LMZ14203 仅需三个外部电阻和四个外部电容器即可完善电源解决方案。LMZ14203 是一款稳定可靠的设计，可提供以下保护 功能：热关断、输入 UVLO、输出过压保护、短路保护、输出电流限制并支持启动至预偏置输出。单个电阻最高可将开关频率调节至 1MHz。

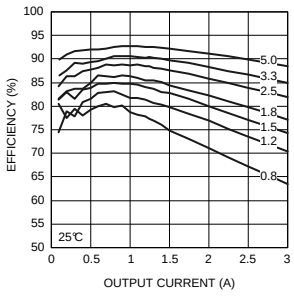
器件信息(1)(2)

器件型号	封装	封装尺寸（标称值）
LMZ14203	TO-PMOD (7)	10.16mm × 9.85mm

(1) 如需了解所有可用封装，请参阅产品说明书末尾的可订购产品附录。

(2) 峰值回流温度等于 245°C。更多详细信息，请参阅 SNAA214。

25°C、输入电压为 12V 时的效率



目录

4 修订历史记录

注：之前版本的页码可能与当前版本有所不同。

Changes from Revision R (October 2015) to Revision S — **Page**

- Changed equation 9 to put a bracket around fsw*delta VIN ... 15
- Changed equation 10 to put a bracket around V_{IN} and R_{ON}^2 ... 16

Changes from Revision Q (August 2015) to Revision R — **Page**

- Added this new bullet to the Power Module SMT Guidelines ... 20

Changes from Revision P (May 2015) to Revision Q — **Page**

- 已更改 文档标题 ... 1

Changes from Revision O (October 2013) to Revision P — **Page**

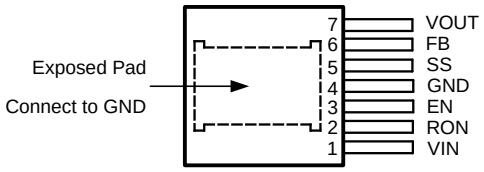
- 已添加 *ESD 额定值*表、*热性能信息*表、*特性 说明* 部分、*器件功能模式*、*应用和实施*部分、*电源相关建议*部分、*布局*部分、*器件和文档支持*部分以及*机械、封装和可订购信息*部分 ... 1
- 删除了易用型引脚封装图 ... 1

Changes from Revision N (March 2013) to Revision O — **Page**

- Changed 12 mils ... 18
- Changed 12 mils ... 20
- Added *Power Module SMT Guidelines* ... 20

5 Pin Configuration and Functions

NDW Package
7-Pin TO-PMOD
Top View



Pin Functions

PIN		TYPE	DESCRIPTION
NAME	NO.		
EN	3	Analog	Enable. Input to the precision enable comparator. Rising threshold is 1.18 V nominal; 90 mV hysteresis nominal. Maximum recommended input level is 6.5 V.
FB	6	Analog	Feedback. Internally connected to the regulation, overvoltage, and short-circuit comparators. The regulation reference point is 0.8 V at this input pin. Connected the feedback resistor divider between the output and ground to set the output voltage.
GND	4	Ground	Ground. Reference point for all stated voltages. Must be externally connected to exposed thermal pad.
RON	2	Analog	ON-time resistor. An external resistor between this pin and the VIN pin sets the ON-time of the application. Typical values range from 25 kΩ to 124 kΩ.
SS	5	Analog	Soft-start. An internal 8-µA current source charges an external capacitor to produce the soft-start function. This node is discharged at 200 µA during disable, overcurrent, thermal shutdown and internal UVLO conditions.
VIN	1	Power	Supply input. Nominal operating range is 6 V to 42 V . A small amount of internal capacitance is contained within the package assembly. Additional external input capacitance is required between this pin and exposed pad.
VOUT	7	Power	Output voltage. Output from the internal inductor. Connect the output capacitor between this pin and exposed pad.
Thermal Pad	—	Ground	Exposed thermal pad. Internally connected to pin 4. Used to dissipate heat from the package during operation. Must be electrically connected to pin 4 external to the package.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)(2)

	MIN	MAX	UNIT
VIN, RON to GND	–0.3	43.5	V
EN, FB, SS to GND	–0.3	7	V
Junction Temperature		150	°C
Peak Reflow Case Temperature (30 sec)		245	°C
Storage Temperature	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) For soldering specifications, refer to the following document: *Absolute Maximum Ratings for Soldering* (SNOA549).

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 (1)	±2000	V

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted) (1)

	MIN	MAX	UNIT
V_{IN}	6	42	V
EN	0	6.5	V
Operation Junction Temperature	−40	125	°C

(1) *Absolute Maximum Ratings* are limits beyond which damage to the device may occur. *Recommended Operating Ratings* are conditions under which operation of the device is intended to be functional. For ensured specifications and test conditions, see the *Electrical Characteristics*.

6.4 Thermal Information

THERMAL METRIC (1)			LMZ14203 NDW (TO-PMOD) 7 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	4-layer JEDEC Printed Circuit Board, No air flow	19.3	°C/W
		2-layer JEDEC Printed Circuit Board, No air flow	21.5	
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	No air flow	1.9	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.5 Electrical Characteristics

T_J = 25°C unless otherwise noted. Minimum and maximum limits are ensured through test, design or statistical correlation. Typical values represent the most likely parametric norm at T_J = 25°C, and are provided for reference purposes only. Unless otherwise stated the following conditions apply: V_{IN} = 24 V, Vout = 3.3 V

PARAMETER		TEST CONDITIONS		MIN (1)	TYP (2)	MAX (1)	UNIT
SYSTEM PARAMETERS							
Enable Control (3)							
V_{EN}	EN threshold trip point	V_{EN} rising	T_J = 25°C		1.18		V
			over the junction temperature (T_J) range of –40°C to +125°C	1.1		1.25	
V_{EN-HYS}	EN threshold hysteresis	V_{EN} falling			90		mV
Soft Start							
I_{SS}	SS source current	V_{SS} = 0V	T_J = 25°C		8		µA
			over the junction temperature (T_J) range of –40°C to +125°C	5		11	
I_{SS-DIS}	SS discharge current				–200		µA
Current Limit							
I_{CL}	Current limit threshold	DC average V_{IN}= 12 V to 24 V	T_J = 25°C		4.2		A
			over the junction temperature (T_J) range of –40°C to +125°C	3.2		5.25	

(1) Minimum and maximum limits are 100% production tested at 25°C. Limits over the operating temperature range are ensured through correlation using Statistical Quality Control (SQC) methods. Limits are used to calculate Average Outgoing Quality Level (AOQL).
(2) Typical numbers are at 25°C and represent the most likely parametric norm.
(3) EN 55022:2006, +A1:2007, FCC Part 15 Subpart B: 2007. See AN-2024 and layout for information on device under test.

Electrical Characteristics (continued)

T_J = 25°C unless otherwise noted. Minimum and maximum limits are ensured through test, design or statistical correlation. Typical values represent the most likely parametric norm at T_J = 25°C, and are provided for reference purposes only. Unless otherwise stated the following conditions apply: V_{IN} = 24 V, Vout = 3.3 V

PARAMETER		TEST CONDITIONS		MIN(1)	TYP(2)	MAX(1)	UNIT
ON/OFF Timer							
t_{ON-MIN}	ON timer minimum pulse width				150		ns
t_{OFF}	OFF timer pulse width				260		ns
Regulation and Overvoltage Comparator							
V_{FB}	In-regulation feedback voltage	V_{SS} > 0.8 V T_J = –40°C to 125°C I_O = 3 A	T_J = 25°C		0.804		V
			over the junction temperature (T_J) range of –40°C to +125°C	0.784		0.825	
		V_{SS} > 0.8 V T_J = 25°C I_O = 10 mA		0.786	0.802	0.818	V
V_{FB-OV}	Feedback overvoltage protection threshold				0.92		V
I_{FB}	Feedback input bias current				5		nA
I_Q	Nonswitching Input Current	V_{FB}= 0.86 V			1		mA
I_{SD}	Shut Down Quiescent Current	V_{EN}= 0 V			25		μA
Thermal Characteristics							
T_{SD}	Thermal Shutdown	Rising			165		°C
$T_{SD-HYST}$	Thermal shutdown hysteresis	Falling			15		°C
PERFORMANCE PARAMETERS							
ΔV_O	Output Voltage Ripple				8		mV_{PP}
$\Delta V_O/\Delta V_{IN}$	Line Regulation	V_{IN} = 12 V to 42 V, I_O= 3 A			0.01%		
$\Delta V_O/I_{OUT}$	Load Regulation	V_{IN} = 24 V			1.5		mV/A
η	Efficiency	V_{IN} = 24 V V_O = 3.3 V I_O = 1 A			92%		
η	Efficiency	V_{IN} = 24 V V_O = 3.3 V I_O = 3 A			85%		

6.6 Typical Characteristics

Unless otherwise specified, the following conditions apply: V_{IN} = 24 V; C_{IN} = 10-µF X7R Ceramic; C_O = 100-µF X7R Ceramic; T_A = 25°C for efficiency curves and waveforms.

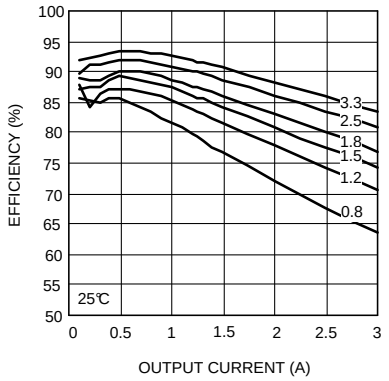


Figure 1. Efficiency 6-V Input at 25°C

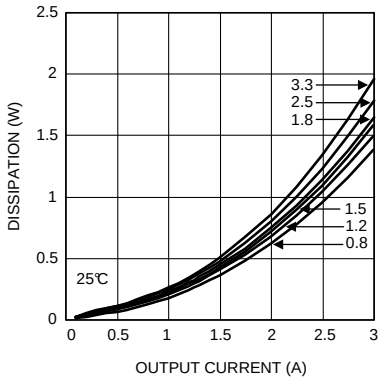


Figure 2. Dissipation 6-V Input at 25°C

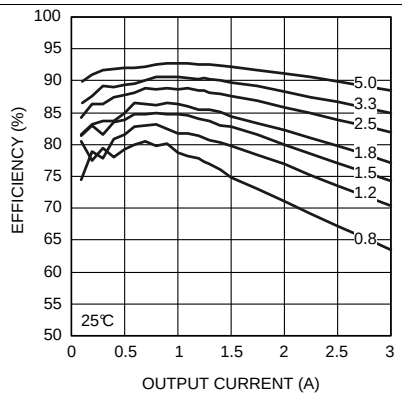


Figure 3. Efficiency 12-V Input at 25°C

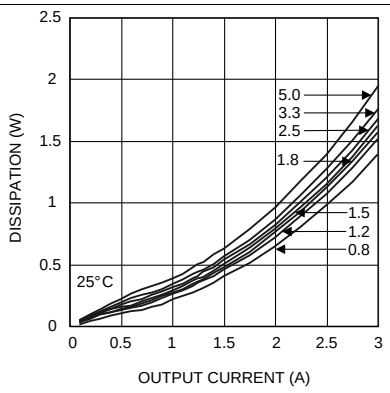


Figure 4. Dissipation 12-V Input at 25°C

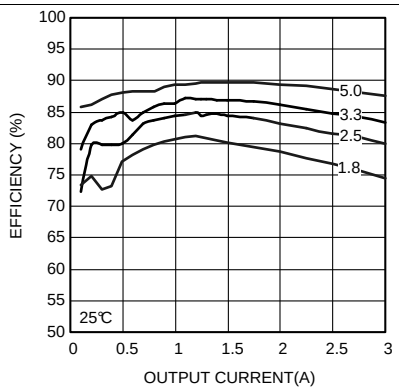


Figure 5. Efficiency 24-V Input at 25°C

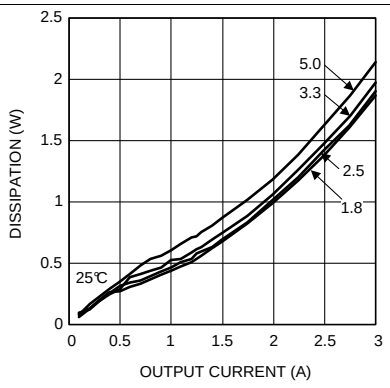


Figure 6. Dissipation 24-V Input at 25°C

Typical Characteristics (continued)

Unless otherwise specified, the following conditions apply: V_{IN} = 24 V; C_{IN} = 10-µF X7R Ceramic; C_O = 100-µF X7R Ceramic; T_A = 25°C for efficiency curves and waveforms.

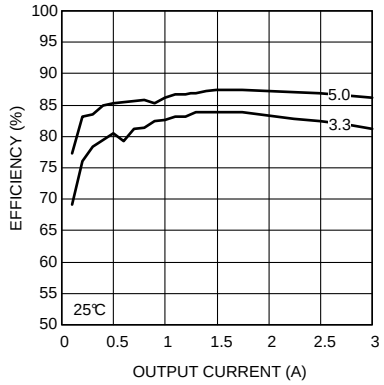


Figure 7. Efficiency 36-V Input at 25°C

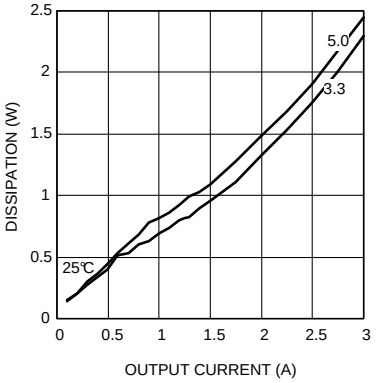


Figure 8. Dissipation 36-V Input at 25°C

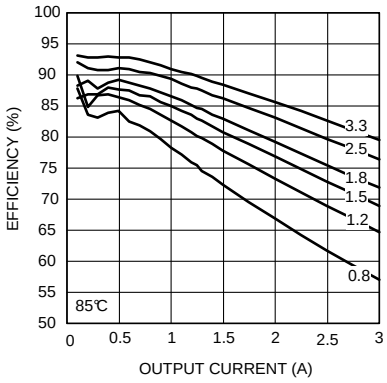


Figure 9. Efficiency 6-V Input at 85°C

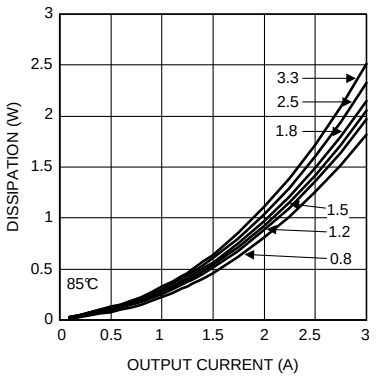


Figure 10. Dissipation 6-V Input at 85°C

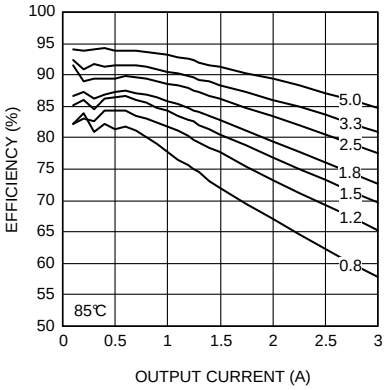


Figure 11. Efficiency 8-V Input at 85°C

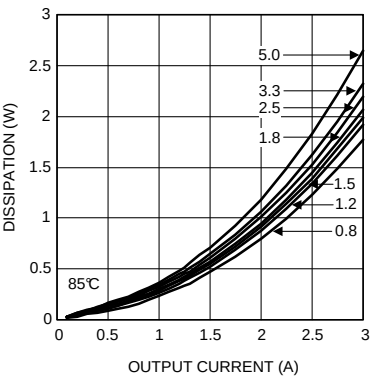


Figure 12. Dissipation 8-V Input at 85°C

Typical Characteristics (continued)

Unless otherwise specified, the following conditions apply: V_{IN} = 24 V; C_{IN} = 10-µF X7R Ceramic; C_O = 100-µF X7R Ceramic; T_A = 25°C for efficiency curves and waveforms.

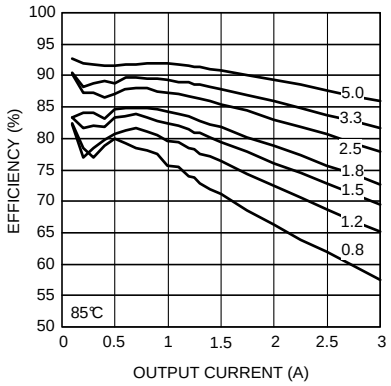


Figure 13. Efficiency 12-V Input at 85°C

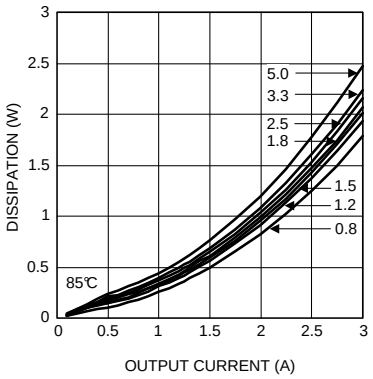


Figure 14. Dissipation 12-V Input at 85°C

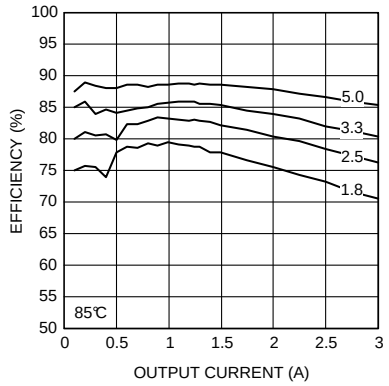


Figure 15. Efficiency 24-V Input at 85°C

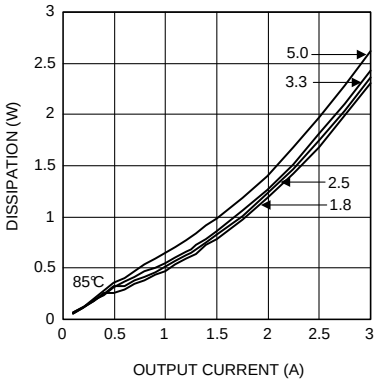


Figure 16. Dissipation 24-V Input at 85°C

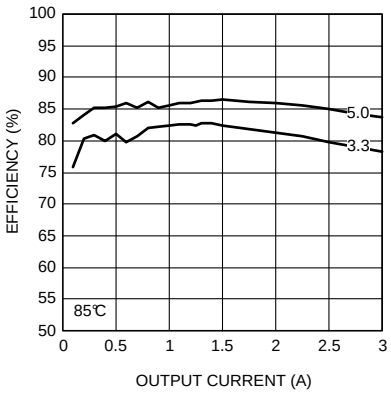


Figure 17. Efficiency 36-V Input at 85°C

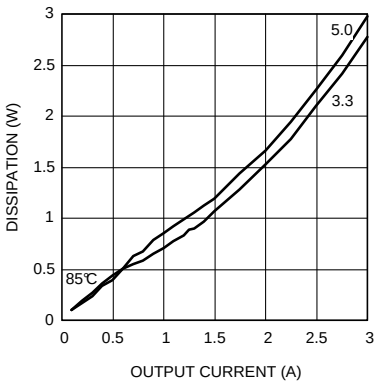


Figure 18. Dissipation 36-V Input at 85°C

Typical Characteristics (continued)

Unless otherwise specified, the following conditions apply: V_{IN} = 24 V; C_{IN} = 10-µF X7R Ceramic; C_O = 100-µF X7R Ceramic; T_A = 25°C for efficiency curves and waveforms.

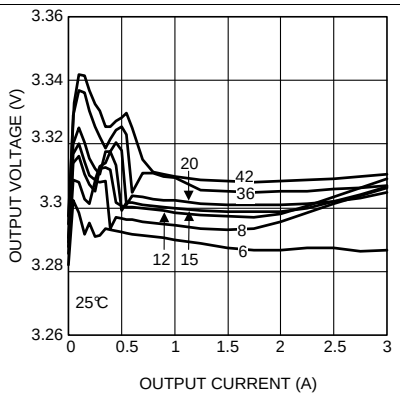


Figure 19. Line and Load Regulation at 25°C

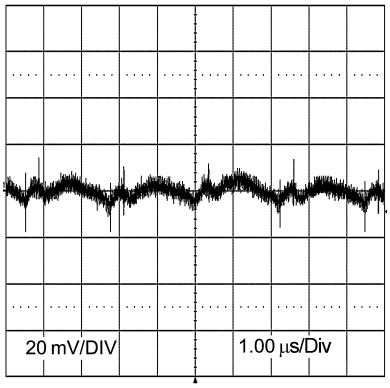


Figure 20. Output Ripple
24 V_{IN} 3.3 V_O 3 A, BW = 200 MHz

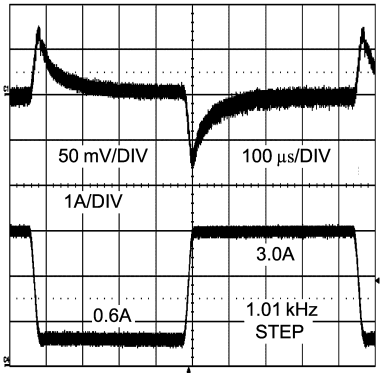


Figure 21. Transient Response
24 V_{IN} 3.3 V_O 0.6-A to 3-A Step

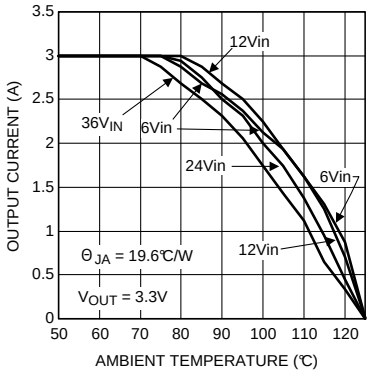


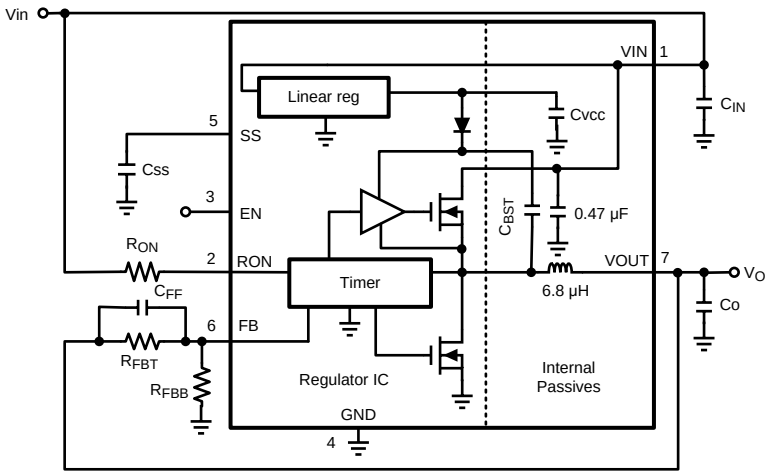
Figure 22. Thermal Derating V_{OUT} = 3.3 V

7 Detailed Description

7.1 Overview

The LMZ14203 power module is an easy-to-use step-down DC-DC solution that can drive up to 3-A load with exceptional power conversion efficiency, line and load regulation, and output accuracy.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 COT Control Circuit Overview

Constant ON-Time control is based on a comparator and an ON-time one shot, with the output voltage feedback compared with an internal 0.8-V reference. If the feedback voltage is below the reference, the main MOSFET is turned on for a fixed ON-time determined by a programming resistor R_{ON}. R_{ON} is connected to V_{IN} such that ON-time is reduced with increasing input supply voltage. Following this ON-time, the main MOSFET remains off for a minimum of 260 ns. If the voltage on the feedback pin falls below the reference level again the ON-time cycle is repeated. Regulation is achieved in this manner.

7.3.2 Output Overvoltage Comparator

The voltage at FB is compared to a 0.92-V internal reference. If FB rises above 0.92 V the ON-time is immediately terminated. This condition is known as overvoltage protection (OVP). It can occur if the input voltage is increased very suddenly or if the output load is decreased very suddenly. Once OVP is activated, the top MOSFET ON-times will be inhibited until the condition clears. Additionally, the synchronous MOSFET will remain on until inductor current falls to zero.

7.3.3 Current Limit

Current limit detection is carried out during the OFF-time by monitoring the current in the synchronous MOSFET. Referring to the Functional Block Diagram, when the top MOSFET is turned off, the inductor current flows through the load, the PGND pin and the internal synchronous MOSFET. If this current exceeds 4.2 A (typical) the current limit comparator disables the start of the next ON-time period. The next switching cycle will occur only if the FB input is less than 0.8 V and the inductor current has decreased below 4.2 A. Inductor current is monitored during the period of time the synchronous MOSFET is conducting. So long as inductor current exceeds 4.2 A, further ON-time intervals for the top MOSFET will not occur. Switching frequency is lower during current limit due to the longer OFF-time.

NOTE

Current limit is dependent on both duty cycle and temperature.

Feature Description (continued)

7.3.4 Thermal Protection

The junction temperature of the LMZ14203 should not be allowed to exceed its maximum ratings. Thermal protection is implemented by an internal Thermal Shutdown circuit which activates at 165 °C (typical) causing the device to enter a low power standby state. In this state the main MOSFET remains off causing V_O to fall, and additionally the CSS capacitor is discharged to ground. Thermal protection helps prevent catastrophic failures for accidental device overheating. When the junction temperature falls back below 145°C (typical hysteresis = 20 °C) the SS pin is released, V_O rises smoothly, and normal operation resumes.

Applications requiring maximum output current especially those at high input voltage may require application derating at elevated temperatures.

7.3.5 Zero Coil Current Detection

The current of the lower (synchronous) MOSFET is monitored by a zero coil current detection circuit which inhibits the synchronous MOSFET when its current reaches zero until the next ON-time. This circuit enables the DCM operating mode, which improves efficiency at light loads.

7.3.6 Prebiased Start-Up

The LMZ14203 will properly start up into a prebiased output. This start-up situation is common in multiple rail logic applications where current paths may exist between different power rails during the start-up sequence. Figure 23 is a scope capture that shows proper behavior during this event.

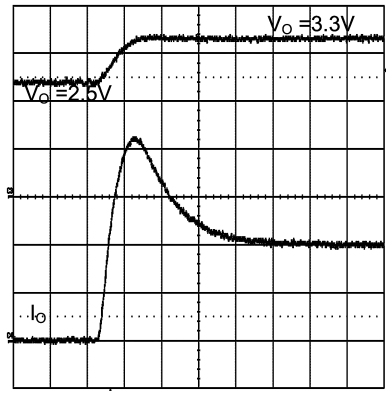


Figure 23. Prebiased Start-Up

7.4 Device Functional Modes

7.4.1 Discontinuous Conduction and Continuous Conduction Modes

At light-load, the regulator operates in discontinuous conduction mode (DCM). With load currents above the critical conduction point, it operates in continuous conduction mode (CCM). When operating in DCM the switching cycle begins at zero amps inductor current; increases up to a peak value, and then recedes back to zero before the end of the OFF-time. During the period of time that inductor current is zero, all load current is supplied by the output capacitor. The next ON-time period starts when the voltage on the FB pin falls below the internal reference. The switching frequency is lower in DCM and varies more with load current as compared to CCM. Conversion efficiency in DCM is maintained because conduction and switching losses are reduced with the smaller load and lower switching frequency.

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The LMZ14203 is a step-down DC-to-DC power module. It is typically used to convert a higher DC voltage to a lower DC voltage with a maximum output current of 3 A. The following design procedure can be used to select components for the LMZ14203. Alternately, the WEBENCH software may be used to generate complete designs.

When generating a design, the WEBENCH software uses iterative design procedure and accesses comprehensive databases of components. For more details, see www.ti.com.

8.2 Typical Application

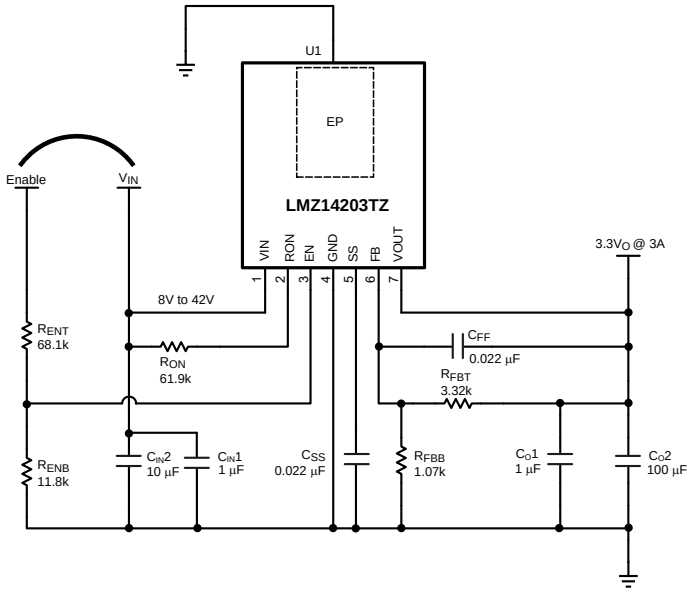


Figure 24. Evaluation Board Schematic Diagram

8.2.1 Design Requirements

For this example the following application parameters exist.

- V_{IN} Range = Up to 42 V
- V_{OUT} = 0.8 V to 5 V
- I_{OUT} = 3 A

Please refer to Table 1 for more information.

Table 1. Component Value Combinations

VOUT (V)	R_{FBT} (kΩ)	R_{FBB} (kΩ)	$R_{DS(on)}$ (kΩ)	VIN (V)	
				MIN	MAX
5	5.62	1.07	100	7.5	42
3.3	3.32		61.9	6	42
2.5	2.26		47.5		30
1.8	1.87	1.5	32.4		25
1.5	1	1.13	28		21
1.2	4.22	8.45	22.6		19
0.8	0	39.2	24.9		18

Table 2. List of Materials

Ref Des	Description	Case Size	Manufacturer	Manufacturer P/N
U1	SIMPLE SWITCHER	PFM-7	Texas Instruments	LMZ14203TZ
C_{IN1}	1 µF, 50 V, X7R	1206	Taiyo Yuden	UMK316B7105KL-T
C_{IN2}	10 µF, 50 V, X7R	1210	Taiyo Yuden	UMK325BJ106MM-T
C_{O1}	1 µF, 50 V, X7R	1206	Taiyo Yuden	UMK316B7105KL-T
C_{O2}	100 µF, 6.3 V, X7R	1210	Taiyo Yuden	JMK325BJ107MM-T
R_{FBT}	3.32 kΩ	0603	Vishay Dale	CRCW06033K32FKEA
R_{FBB}	1.07 kΩ	0603	Vishay Dale	CRCW06031K07FKEA
R_{ON}	61.9 kΩ	0603	Vishay Dale	CRCW060361k9FKEA
R_{ENT}	68.1 kΩ	0603	Vishay Dale	CRCW060368k1FKEA
R_{ENB}	11.8 kΩ	0603	Vishay Dale	CRCW060311k8FKEA
C_{FF}	22 nF, ±10%, X7R, 16 V	0603	TDK	C1608X7R1H223K
C_{SS}	22 nF, ±10%, X7R, 16 V	0603	TDK	C1608X7R1H223K

8.2.2 Detailed Design Procedure

8.2.2.1 Custom Design With WEBENCH® Tools

Click here to create a custom design using the LMZ14203 device with the WEBENCH® Power Designer.

1. Start by entering the input voltage (V_{IN}), output voltage (V_{OUT}), and output current (I_{OUT}) requirements.
2. Optimize the design for key parameters such as efficiency, footprint, and cost using the optimizer dial.
3. Compare the generated design with other possible solutions from Texas Instruments.

The WEBENCH Power Designer provides a customized schematic along with a list of materials with real-time pricing and component availability.

In most cases, these actions are available:

- Run electrical simulations to see important waveforms and circuit performance
- Run thermal simulations to understand board thermal performance
- Export customized schematic and layout into popular CAD formats
- Print PDF reports for the design, and share the design with colleagues

Get more information about WEBENCH tools at www.ti.com/WEBENCH.

8.2.2.2 Design Steps for the LMZ14203 Application

The LMZ14203 is fully supported by WEBENCH and offers the following: Component selection, electrical and thermal simulations as well as the build-it board for a reduction in design time. The following list of steps can be used to manually design the LMZ14203 application.

1. Select minimum operating V_{IN} with enable divider resistors
2. Program V_O with divider resistor selection
3. Program turnon time with soft-start capacitor selection

4. Select C_O
5. Select C_{IN}
6. Set operating frequency with R_{ON}
7. Determine module dissipation
8. Lay out PCB for required thermal performance

8.2.2.2.1 Enable Divider, R_{ENT} and R_{ENB} Selection

The enable input provides a precise 1.18-V band-gap rising threshold to allow direct logic drive or connection to a voltage divider from a higher enable voltage such as V_{IN}. The enable input also incorporates 90 mV (typical) of hysteresis resulting in a falling threshold of 1.09 V. The maximum recommended voltage into the EN pin is 6.5 V. For applications where the midpoint of the enable divider exceeds 6.5 V, a small Zener diode can be added to limit this voltage.

The function of this resistive divider is to allow the designer to choose an input voltage below which the circuit will be disabled. This implements the feature of programmable under voltage lockout. This is often used in battery powered systems to prevent deep discharge of the system battery. It is also useful in system designs for sequencing of output rails or to prevent early turnon of the supply as the main input voltage rail rises at power-up. Applying the enable divider to the main input rail is often done in the case of higher input voltage systems such as 24-V AC/DC systems where a lower boundary of operation should be established. In the case of sequencing supplies, the divider is connected to a rail that becomes active earlier in the power-up cycle than the LMZ14203 output rail. The two resistors should be chosen based on the following ratio:

$$R_{ENT} / R_{ENB} = (V_{IN\ UVLO} / 1.18\ V) - 1 \quad (1)$$

The LMZ14203 demonstration and evaluation boards use 11.8 kΩ for R_{ENB} and 68.1 kΩ for R_{ENT} resulting in a rising UVLO of 8 V. This divider presents 6.25 V to the EN input when the divider input is raised to 42 V.

The EN pin is internally pulled up to VIN and can be left floating for always-on operation.

8.2.2.2.2 Output Voltage Selection

Output voltage is determined by a divider of two resistors connected between V_O and ground. The midpoint of the divider is connected to the FB input. The voltage at FB is compared to a 0.8V internal reference. In normal operation an ON-time cycle is initiated when the voltage on the FB pin falls below 0.8 V. The main MOSFET ON-time cycle causes the output voltage to rise and the voltage at the FB to exceed 0.8 V. As long as the voltage at FB is above 0.8 V, ON-time cycles will not occur.

The regulated output voltage determined by the external divider resistors R_{FBT} and R_{FBB} is:

$$V_O = 0.8\ V \times (1 + R_{FBT} / R_{FBB}) \quad (2)$$

Rearranging terms; the ratio of the feedback resistors for a desired output voltage is:

$$R_{FBT} / R_{FBB} = (V_O / 0.8\ V) - 1 \quad (3)$$

These resistors should be chosen from values in the range of 1 kΩ to 10 kΩ.

For V_O = 0.8 V the FB pin can be connected to the output directly so long as an output preload resistor remains that draws more than 20 uA. Converter operation requires this minimum load to create a small inductor ripple current and maintain proper regulation when no load is present.

A feed-forward capacitor is placed in parallel with R_{FBT} to improve load step transient response. Its value is usually determined experimentally by load stepping between DCM and CCM conduction modes and adjusting for best transient response and minimum output ripple.

A table of values for R_{FBT} , R_{FBB} , C_{FF} and R_{ON} is included in the applications schematic.

8.2.2.2.3 Soft-Start Capacitor Selection

Programmable soft-start permits the regulator to slowly ramp to its steady state operating point after being enabled, thereby reducing current inrush from the input supply and slowing the output voltage rise-time to prevent overshoot.

Upon turnon, after all UVLO conditions have been passed, an internal 8-uA current source begins charging the external soft-start capacitor. The soft-start time duration to reach steady-state operation is given by the formula:

$$t_{SS} = V_{REF} \times C_{SS} / Iss = 0.8\ V \times C_{SS} / 8\ uA \quad (4)$$

This equation can be rearranged as follows:

$$C_{SS} = t_{SS} \times 8\ \mu A / 0.8\ V \quad (5)$$

Use of a 0.022-µF capacitor results in 2.2 ms soft-start duration. This is recommended as a minimum value.

As the soft-start input exceeds 0.8 V the output of the power stage will be in regulation. The soft-start capacitor continues charging until it reaches approximately 3.8 V on the SS pin. Voltage levels between 0.8 V and 3.8 V have no effect on other circuit operation. Note the following conditions will reset the soft-start capacitor by discharging the SS input to ground with an internal 200-µA current sink.

- The enable input being *pulled low*
- Thermal shutdown condition
- Overcurrent fault
- Internal V_{CC} UVLO (Approx 4-V input to V_{IN})

8.2.2.2.4 C_O Selection

None of the required C_O output capacitance is contained within the module. At a minimum, the output capacitor must meet the worst case minimum ripple current rating of 0.5 × $I_{LR\ P-P}$, as calculated in Equation 12 below. Beyond that, additional capacitance will reduce output ripple so long as the ESR is low enough to permit it. A minimum value of 10 µF is generally required. Experimentation will be required if attempting to operate with a minimum value. Ceramic capacitors or other low ESR types are recommended. See AN-2024 SNVA422 for more detail.

The following equation provides a good first pass approximation of C_O for load transient requirements:

$$C_O \geq I_{STEP} \times V_{FB} \times L \times V_{IN} / (4 \times V_O \times (V_{IN} - V_O) \times V_{OUT\text{-}TRAN}) \quad (6)$$

Solving:

$$C_O \geq 3\ A \times 0.8\ V \times 6.8\ \mu H \times 24\ V / (4 \times 3.3\ V \times (24\ V - 3.3\ V) \times 33\ mV) \geq 43\ \mu F \quad (7)$$

The LMZ14203 demonstration and evaluation boards are populated with a 100-uF 6.3-V X5R output capacitor. Locations for extra output capacitors are provided.

8.2.2.2.5 C_{IN} Selection

The LMZ14203 module contains an internal 0.47-µF input ceramic capacitor. Additional input capacitance is required external to the module to handle the input ripple current of the application. This input capacitance should be very close to the module. Input capacitor selection is generally directed to satisfy the input ripple current requirements rather than by capacitance value. Worst-case input ripple current rating is dictated by the equation:

$$I(C_{IN(RMS)}) \cong 1/2 \times I_O \times \sqrt{(D / 1 - D)}$$

where

- $D \cong V_O / V_{IN}$ (8)

(As a point of reference, the worst case ripple current will occur when the module is presented with full load current and when $V_{IN} = 2 \times V_O$).

Recommended minimum input capacitance is 10uF X7R ceramic with a voltage rating at least 25% higher than the maximum applied input voltage for the application. TI also recommends to pay attention to the voltage and temperature deratings of the capacitor selected. Note ripple current rating of ceramic capacitors may be missing from the capacitor data sheet and you may need to contact the capacitor manufacturer for this rating.

If the system design requires a certain minimum value of input ripple voltage ΔV_{IN} be maintained then the following equation may be used.

$$C_{IN} \geq I_O \times D \times (1-D) / (f_{SW\text{-}CCM} \times \Delta V_{IN}) \quad (9)$$

If ΔV_{IN} is 1% of V_{IN} for a 24-V input to 3.3-V output application this equals 240 mV and f_{SW} = 400 kHz.

$C_{IN} \geq 3\ A \times 3.3\ V / 24\ V \times (1 - 3.3\ V / 24\ V) / (400000 \times 0.240\ V)$

$\geq 3.7\ \mu F$

Additional bulk capacitance with higher ESR may be required to damp any resonant effects of the input capacitance and parasitic inductance of the incoming supply lines.

8.2.2.2.6 Discontinuous Conduction and Continuous Conduction Mode Selection

Operating frequency in DCM can be calculated as follows:

$$f_{SW(DCM)} \cong V_O \times (V_{IN}\text{-}1) \times 6.8\ \mu H \times 1.18 \times 10^{20} \times I_O / ((V_{IN} - V_O) \times R_{ON}^2) \quad (10)$$

In CCM, current flows through the inductor through the entire switching cycle and never falls to zero during the OFF-time. The switching frequency remains relatively constant with load current and line voltage variations. The CCM operating frequency can be calculated using Equation 7 above.

Following is a comparison pair of waveforms of the showing both CCM (upper) and DCM operating modes.

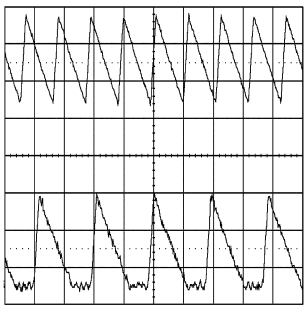


Figure 25. CCM and DCM Operating Modes V_{IN} = 24 V, V_O = 3.3 V, I_O = 3 A/0.4 A 2 µs/div

The approximate formula for determining the DCM/CCM boundary is as follows:

$$I_{DCB} \cong V_O \times (V_{IN} - V_O) / (2 \times 6.8\ \mu H \times f_{SW(CCM)} \times V_{IN}) \quad (11)$$

Following is a typical waveform showing the boundary condition.

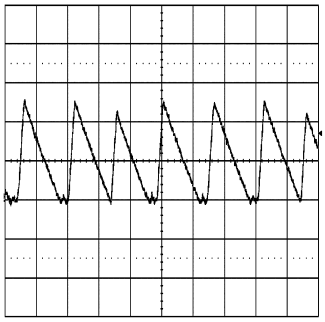


Figure 26. Transition Mode Operation V_{IN} = 24 V, V_O = 3.3 V, I_O = 0.5 A 2 µs/div

The inductor internal to the module is 6.8 µH. This value was chosen as a good balance between low and high input voltage applications. The main parameter affected by the inductor is the amplitude of the inductor ripple current (I_{LR}). I_{LR} can be calculated with:

$$I_{LR\ P\text{-}P} = V_O \times (V_{IN} - V_O) / (6.8\mu H \times f_{SW} \times V_{IN})$$

where

- V_{IN} is the maximum input voltage and f_{SW} is determined from Equation 13. (12)

If the output current I_O is determined by assuming that $I_O = I_L$, the higher and lower peak of I_{LR} can be determined. Be aware that the lower peak of I_{LR} must be positive if CCM operation is required.

8.2.2.2.7 R_{ON} Resistor Selection

Many designs will begin with a desired switching frequency in mind. For that purpose the following equation can be used.

$$f_{SW(CCM)} \cong V_O / (1.3 \times 10^{-10} \times R_{ON}) \quad (13)$$

This can be rearranged as

$$R_{ON} \cong V_O / (1.3 \times 10^{-10} \times f_{SW(CCM)}) \quad (14)$$

The selection of RON and $f_{SW(CCM)}$ must be confined by limitations in the ON-time and OFF-time for the *COT Control Circuit Overview* section.

The ON-time of the LMZ14203 timer is determined by the resistor R_{ON} and the input voltage V_{IN}. It is calculated as follows:

$$t_{ON} = (1.3 \times 10^{-10} \times R_{ON}) / V_{IN} \quad (15)$$

The inverse relationship of t_{ON} and V_{IN} gives a nearly constant switching frequency as V_{IN} is varied. R_{ON} should be selected such that the ON-time at maximum V_{IN} is greater than 150 ns. The ON-timer has a limiter to ensure a minimum of 150 ns for t_{ON}. This limits the maximum operating frequency, which is governed by the following equation:

$$f_{SW(MAX)} = V_O / (V_{IN(MAX)} \times 150 \text{ ns}) \quad (16)$$

This equation can be used to select R_{ON} if a certain operating frequency is desired so long as the minimum ON-time of 150 ns is observed. The limit for R_{ON} can be calculated as follows:

$$R_{ON} \geq V_{IN(MAX)} \times 150 \text{ ns} / (1.3 \times 10^{-10}) \quad (17)$$

If R_{ON} calculated in Equation 14 is less than the minimum value determined in Equation 17 a lower frequency should be selected. Alternatively, $V_{IN(MAX)}$ can also be limited to keep the frequency unchanged.

NOTE

The minimum OFF-time of 260 ns limits the maximum duty ratio. Larger R_{ON} (lower F_{SW}) should be selected in any application requiring large duty ratio.

8.2.3 Application Curves

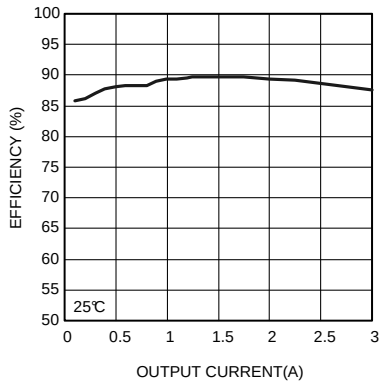


Figure 27. Efficiency V_{IN} = 24 V V_{OUT} = 5.0 V

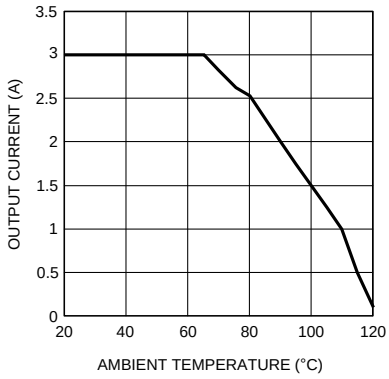


Figure 28. Thermal Derating Curve V_{IN} = 24 V, V_{OUT} = 5.0 V

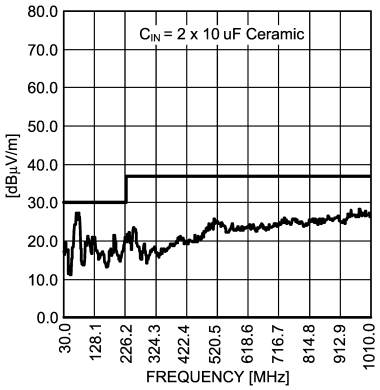


Figure 29. Radiated Emissions (EN 55022 Class B) From Evaluation Board

9 Power Supply Recommendations

The LMZ14203 device is designed to operate from an input voltage supply range between 4.5 V and 42 V. This input supply should be well regulated and able to withstand maximum input current and maintain a stable voltage. The resistance of the input supply rail should be low enough that an input current transient does not cause a high enough drop at the LMZ14203 supply voltage that can cause a false UVLO fault triggering and system reset. If the input supply is located more than a few inches from the LMZ14203, additional bulk capacitance may be required in addition to the ceramic bypass capacitors. The amount of bulk capacitance is not critical, but a 47-μF or 100-μF electrolytic capacitor is a typical choice.

10 Layout

10.1 Layout Guidelines

PCB layout is an important part of DC-DC converter design. Poor board layout can disrupt the performance of a DC-DC converter and surrounding circuitry by contributing to EMI, ground bounce and resistive voltage drop in the traces. These can send erroneous signals to the DC-DC converter resulting in poor regulation or instability. Good layout can be implemented by following a few simple design rules.

1. **Minimize area of switched current loops.**

   From an EMI reduction standpoint, it is imperative to minimize the high di/dt paths during PCB layout. The high current loops that do not overlap have high di/dt content that will cause observable high frequency noise on the output pin if the input capacitor (Cin1) is placed at a distance away from the LMZ14203. Therefore place C_{IN1} as close as possible to the LMZ14203 VIN and GND exposed pad. This will minimize the high di/dt area and reduce radiated EMI. Additionally, grounding for both the input and output capacitor should consist of a localized top side plane that connects to the GND exposed pad (EP).

2. **Have a single point ground.**

   The ground connections for the feedback, soft-start, and enable components should be routed to the GND pin of the device. This prevents any switched or load currents from flowing in the analog ground traces. If not properly handled, poor grounding can result in degraded load regulation or erratic output voltage ripple behavior. Provide the single point ground connection from pin 4 to EP.

3. **Minimize trace length to the FB pin.**

   Both feedback resistors, R_{FBT} and R_{FBB}, and the feed forward capacitor C_{FF}, should be close to the FB pin. Since the FB node is high impedance, maintain the copper area as small as possible. The trace are from R_{FBT}, R_{FBB}, and C_{FF} should be routed away from the body of the LMZ14203 to minimize noise.

4. **Make input and output bus connections as wide as possible.**

   This reduces any voltage drops on the input or output of the converter and maximizes efficiency. To optimize voltage accuracy at the load, ensure that a separate feedback voltage sense trace is made to the load. Doing so will correct for voltage drops and provide optimum output accuracy.

5. **Provide adequate device heat-sinking.**

   Use an array of heat-sinking vias to connect the exposed pad to the ground plane on the bottom PCB layer. If the PCB has a plurality of copper layers, these thermal vias can also be employed to make connection to inner layer heat-spreading ground planes. For best results use a 6 × 6 via array with minimum via diameter of 8 mils thermal vias spaced 59 mils (1.5 mm). Ensure enough copper area is used for heat-sinking to keep the junction temperature below 125°C.

10.2 Layout Example

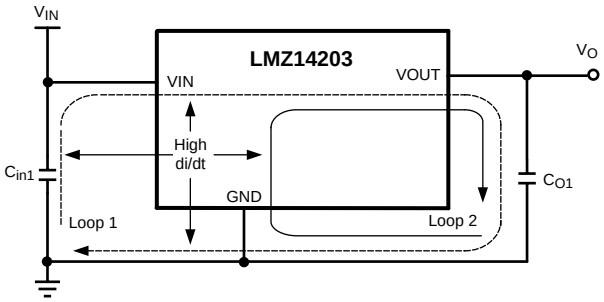


Figure 30. Minimize Area of Current Loops in Buck Module

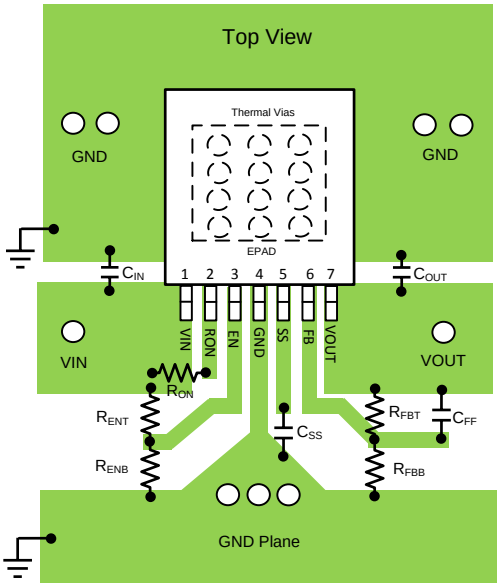


Figure 31. PCB Layout Guide

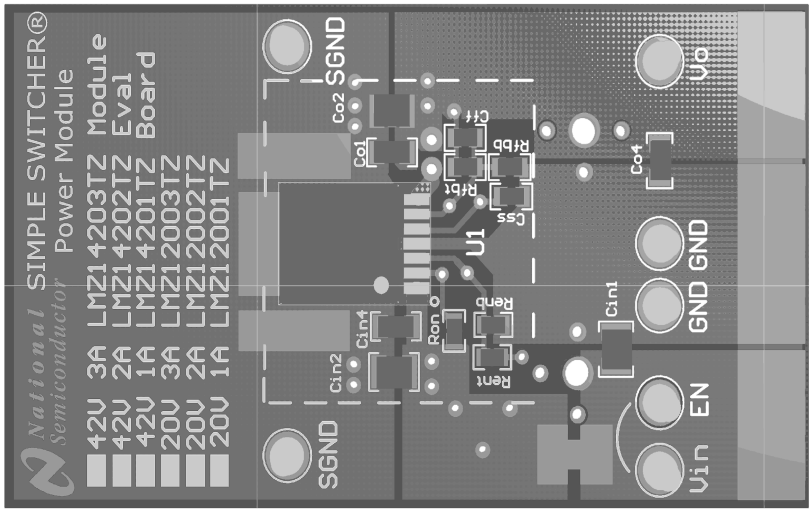


Figure 32. EVM Board Layout - Top View

Layout Example (continued)

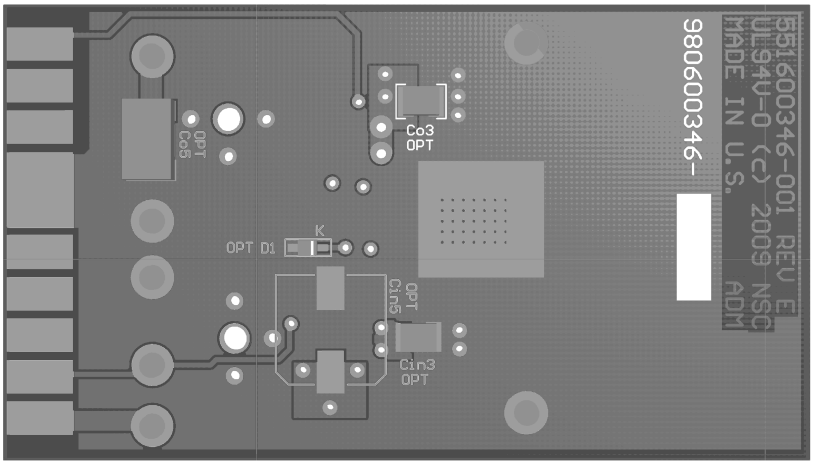


Figure 33. EVM Board Layout - Bottom View

10.3 Power Dissipation and Board Thermal Requirements

For the design case of V_{IN} = 24 V, V_O = 3.3 V, I_O = 3 A, $T_{AMB(MAX)}$ = 85°C , and $T_{JUNCTION}$ = 125°C, the device must see a thermal resistance from case to ambient of:

$$R_{\theta CA} < (T_{J\text{-}MAX} - T_{AMB(MAX)}) / P_{IC\text{-}LOSS} - R_{\theta JC} \quad (18)$$

Given the typical thermal resistance from junction to case to be 1.9°C/W. Use the 85°C power dissipation curves in the *Typical Characteristics* section to estimate the $P_{IC\text{-}LOSS}$ for the application being designed. In this application it is 2.25 W.

$R_{\theta CA} < (125 – 85) / 2.25\ W – 1.9 = 15.8$

To reach $R_{\theta CA}$ = 15.8, the PCB is required to dissipate heat effectively. With no airflow and no external heat, a good estimate of the required board area covered by 1 oz. copper on both the top and bottom metal layers is:

$$\text{Board Area\_cm}^2 > 500°C \times \text{cm}^2/W / R_{\theta CA} \quad (19)$$

As a result, approximately 31.5 square cm of 1 oz copper on top and bottom layers is required for the PCB design. The PCB copper heat sink must be connected to the exposed pad. Approximately thirty six, 8-mil thermal vias spaced 59 mils (1.5 mm) apart must connect the top copper to the bottom copper. For an example of a high thermal performance PCB layout, refer to the Evaluation Board application note AN-2024 SNVA422.

10.4 Power Module SMT Guidelines

The recommendations below are for a standard module surface mount assembly

- Land Pattern – Follow the PCB land pattern with either soldermask defined or non-soldermask defined pads
- Stencil Aperture
  - For the exposed die attach pad (DAP), adjust the stencil for approximately 80% coverage of the PCB land pattern
  - For all other I/O pads use a 1:1 ratio between the aperture and the land pattern recommendation
- Solder Paste – Use a standard SAC Alloy such as SAC 305, type 3 or higher
- Stencil Thickness – 0.125 mm to 0.15 mm
- Reflow - Refer to solder paste supplier recommendation and optimized per board size and density
- Refer to AN SNAA214 for Reflow information.
- Maximum number of reflows allowed is one

Power Module SMT Guidelines (continued)

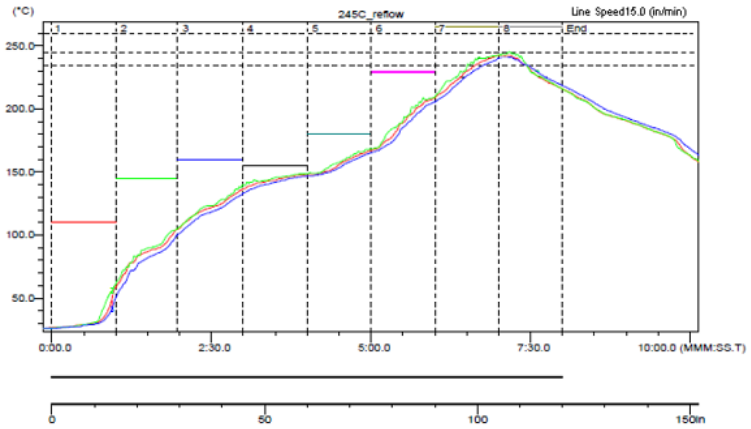


Figure 34. Sample Reflow Profile

Table 3. Sample Reflow Profile Table

Probe	Max Temp (°C)	Reached Max Temp	Time Above 235°C	Reached 235°C	Time Above 245°C	Reached 245°C	Time Above 260°C	Reached 260°C
#1	242.5	6.58	0.49	6.39	0.00	–	0.00	–
#2	242.5	7.10	0.55	6.31	0.00	7.10	0.00	–
#3	241.0	7.09	0.42	6.44	0.00	–	0.00	–

11 器件和文档支持

11.1 使用 WEBENCH® 工具创建定制设计

请单击此处，使用 LMZ14203 器件并借助 WEBENCH® 电源设计器创建定制设计方案。

1. 在开始阶段键入输出电压 (V_{IN})、输出电压 (V_{OUT}) 和输出电流 (I_{OUT}) 要求。
2. 使用优化器拨盘优化关键设计参数，如效率、封装和成本。
3. 将生成的设计与德州仪器 (TI) 的其他解决方案进行比较。

WEBENCH Power Designer 提供一份定制原理图以及罗列实时价格和组件可用性的物料清单。

在多数情况下，可执行以下操作：

- 运行电气仿真，观察重要波形以及电路性能
- 运行热性能仿真，了解电路板热性能
- 将定制原理图和布局方案导出至常用 CAD 格式
- 打印设计方案的 PDF 报告并与同事共享

有关 WEBENCH 工具的详细信息，请访问 www.ti.com/WEBENCH。

11.2 器件支持

11.2.1 开发支持

WEBENCH 软件采用一种迭代设计过程并可访问综合元件数据库。欲了解更多信息，请访问 www.ti.com/webench。

11.2.2 Third-Party Products Disclaimer

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11.3 文档支持

11.3.1 相关文档

本节包含了以下附加支持文档。

- *《LMZ1 和 LMZ2 电源模块设计摘要》*，SNAA214
- *《LMZ14203 SIMPLE SWITCHER 电源模块的反向应用》*，SNVA425
- *《评估板应用手册 AN-2024》*，SNVA422
- *《焊接的绝对最大额定值》*，SNOA549

11.4 接收文档更新通知

要接收文档更新通知，请导航至德州仪器 TI.com.cn 上的器件产品文件夹。请单击右上角的*通知我* 进行注册，即可收到任意产品信息更改每周摘要。有关更改的详细信息，请查看任意已修订文档中包含的修订历史记录。

11.5 社区资源

下列链接提供到 TI 社区资源的连接。链接的内容由各个分销商“按照原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的 《使用条款》。

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设计支持 ***TI 参考设计支持*** **可帮助您快速查找有帮助的 E2E 论坛、设计支持工具以及技术支持的联系信息。**

11.6 商标

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11.6 商标 (接下页)

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11.7 静电放电警告

这些装置包含有限的内置 ESD 保护。 存储或装卸时，应将导线一起截短或将装置放置于导电泡棉中，以防止 MOS 门极遭受静电损伤。

11.8 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 机械、封装和可订购信息

以下页面包括机械、封装和可订购信息。这些信息是指定器件的最新可用数据。这些数据发生变化时，我们可能不会另行通知或修订此文档。如欲获取此产品说明书的浏览器版本，请参阅左侧的导航栏。

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LMZ14203TZ-ADJ/NOPB	ACTIVE	TO-PMOD	NDW	7	250	RoHS & Green	SN	Level-3-245C-168 HR	-40 to 125	LMZ14203 TZ-ADJ	Samples
LMZ14203TZE-ADJ/NOPB	ACTIVE	TO-PMOD	NDW	7	45	RoHS & Green	SN	Level-3-245C-168 HR	-40 to 125	LMZ14203 TZ-ADJ	Samples
LMZ14203TZX-ADJ/NOPB	ACTIVE	TO-PMOD	NDW	7	500	RoHS & Green	SN	Level-3-245C-168 HR	-40 to 125	LMZ14203 TZ-ADJ	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

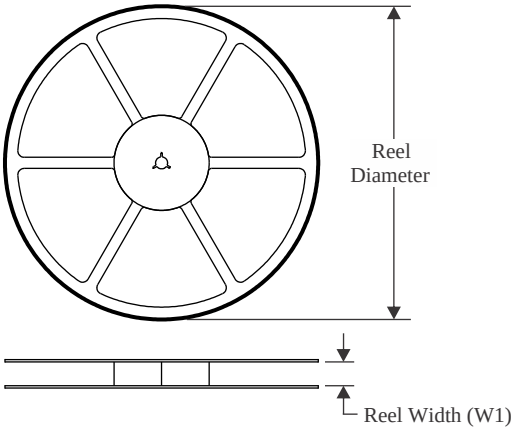
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

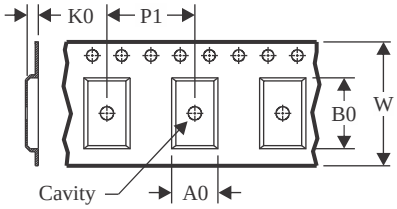
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

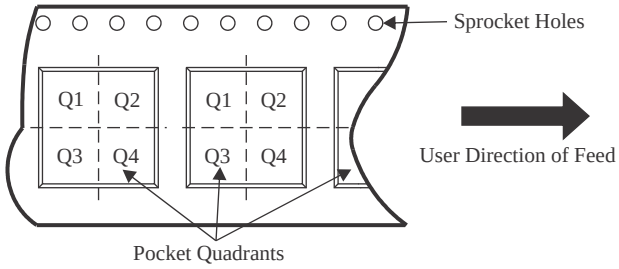


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

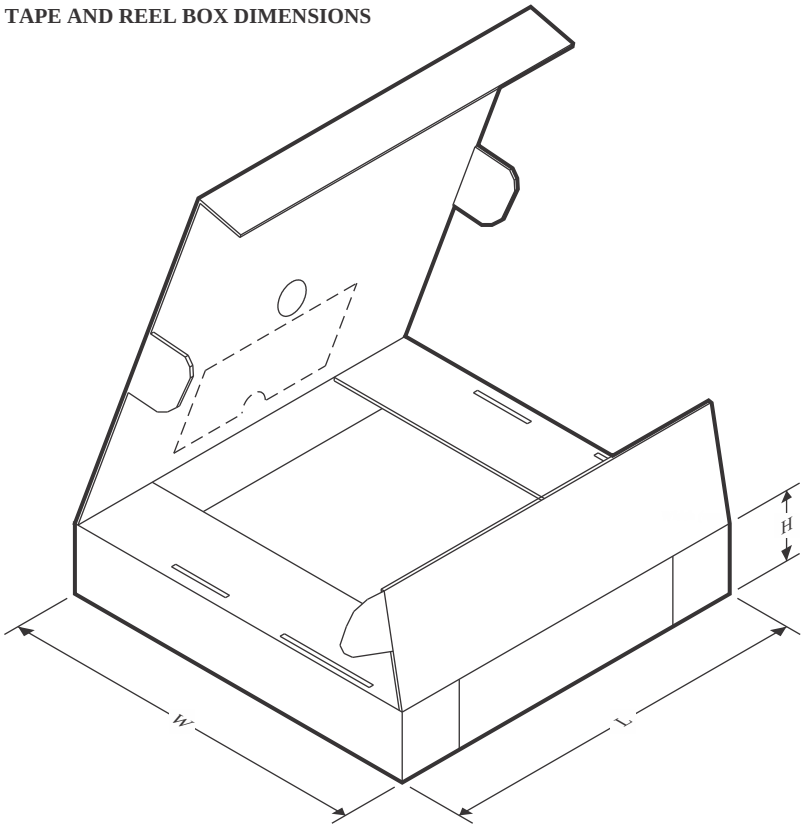
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LMZ14203TZ-ADJ/NOPB	TO-PMOD	NDW	7	250	330.0	24.4	10.6	14.22	5.0	16.0	24.0	Q2
LMZ14203TZX-ADJ/NOPB	TO-PMOD	NDW	7	500	330.0	24.4	10.6	14.22	5.0	16.0	24.0	Q2

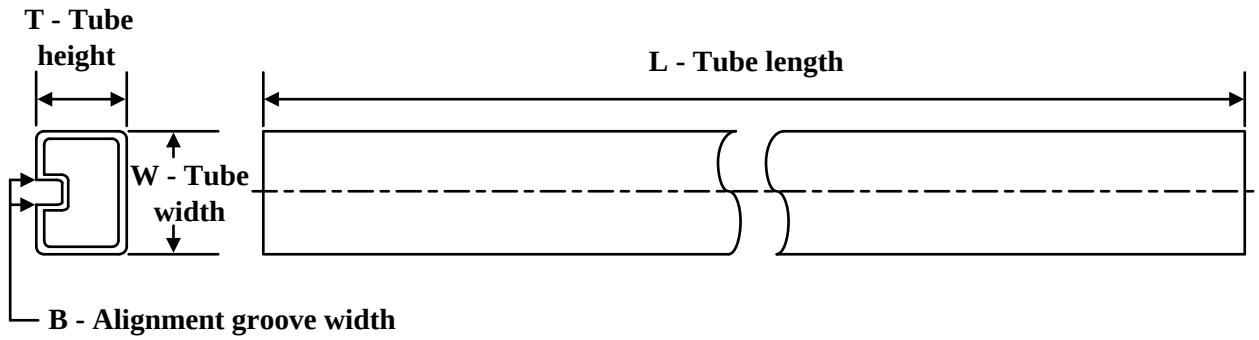
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LMZ14203TZ-ADJ/NOPB	TO-PMOD	NDW	7	250	356.0	356.0	45.0
LMZ14203TZX-ADJ/NOPB	TO-PMOD	NDW	7	500	356.0	356.0	45.0

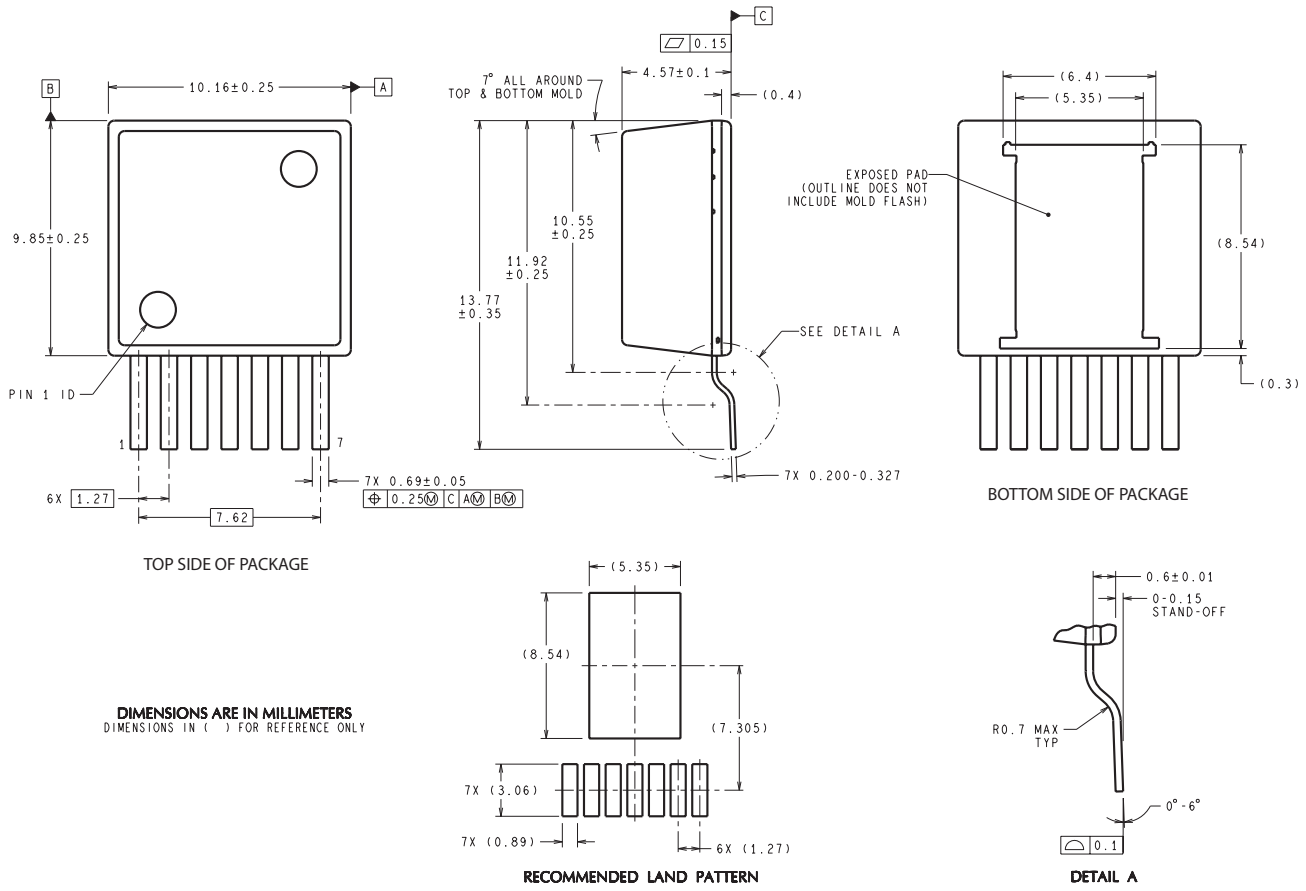
TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
LMZ14203TZE-ADJ/NOPB	NDW	TO-PMOD	7	45	502	17	6700	8.4

NDW0007A



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