LV2862 60V、600mA、高效、宽输入电压范围降压转换器

1 特性

- 输入范围为 4V 至 60V，可承受 65V 瞬态
- 770kHz（X 版本）或 2.1MHz（Y 版本）开关频率
- 凭借 Eco-mode，可以在轻负载下实现超高的效率
- 低压降运行
- 高达 600mA 的输出电流
- 高电压精密使能输入
- 过流保护
- 过热保护
- 内部补偿
- 内部软启动
- 小型总体解决方案尺寸（SOT-6L 封装）

2 应用

- 电网基础设施
- 电器
- 电机驱动器
- 通用宽输入电压电源

3 说明

LV2862 是一款 PWM 直流/直流降压稳压器。该器件具有 4V 至 60V 的宽输入范围，适用于从非稳压源进行电源调节的各种工业和汽车应用。1μA 的超低关断电流可进一步延长电池使用寿命。工作频率固定在 770kHz（X 版本）和 2.1MHz（Y 版本）上，可在保证低输出纹波电压的同时，支持使用小型外部元件。软启动和补偿电路在内部实现，从而最大限度地减少了器件所用的外部元件。

LV2862 针对高达 600mA 的负载电流进行了优化。该器件具有 0.765V 的标称反馈电压。

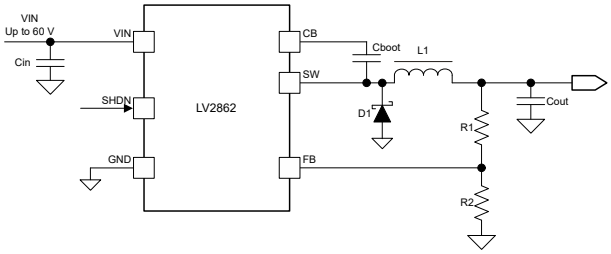
该器件内置多种保护特性，例如逐脉冲电流限制、热感应和应对功耗过大的热关断。LV2862 采用扁平 SOT-6L 封装。

封装信息

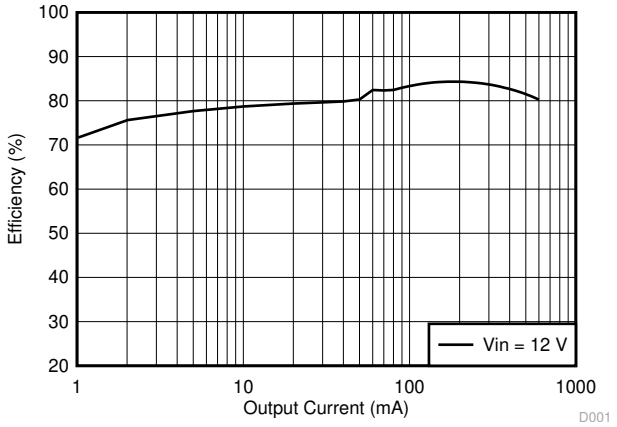
器件型号	封装(1)	封装尺寸(2)
LV2862	DDC（SOT，6）	2.90 mm × 2.8 mm

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。

(2) 封装尺寸（长 x 宽）为标称值，并包括引脚（如适用）。



简化原理图



效率与输出电流间的关系
(f_{sw} = 0.7MHz, V_{OUT} = 3.3V)

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4 Revision History

注：以前版本的页码可能与当前版本的页码不同

Changes from Revision A (June 2020) to Revision B (June 2023)	Page
• 更新了整个文档中的表格、图和交叉参考的编号格式	1
• 更新了*封装信息* 表格式	1
• Moved storage temperature row from the *Handling Ratings* table to the *Absolute Maximum Ratings* table	4
• Updated the *Handling Ratings* table to *ESD Ratings* table	4
• Corrected part number typo in the *Power Supply Recommendations* section	15

Changes from Revision * (December 2014) to Revision A (June 2020)	Page
• 首次公开发布	1

5 Pin Configuration and Functions

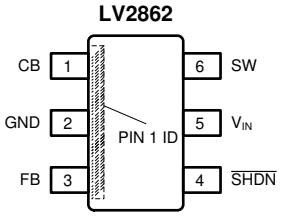


图 5-1. SOT (DDC) 6 Pins Top View

表 5-1. Pin Functions

PIN		DESCRIPTION
NAME	NO.	
CB	1	Switch FET gate bias voltage. Connect C_{boot} cap between CB and SW.
GND	2	Ground connection
FB	3	Set feedback voltage divider ratio with $V_{OUT} = V_{FB}$ (1 + (R1 / R2))
$\overline{SHDN}$	4	Enable and disable input (high voltage tolerant). Internal pullup current source. Pull below 1.25 V to disable. Float to enable. Establish the input undervoltage lockout with a two-resistor divider.
V_{IN}	5	Power input voltage pin. Input for internal supply and drain node input for internal high-side MOSFET.
SW	6	Switch node. Connect to inductor, diode, and C_{boot} cap.

6 Specifications

6.1 Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted) (1)

		MIN	MAX	UNIT
Input voltages	V_{IN} to GND	–0.3	65	V
	$\overline{SHDN}$ to GND	–0.3	65	
	FB to GND	–0.3	7	
	CB to SW	–0.3	7	
Output voltages	SW to GND	–1	65	
	SW to GND less than 30-ns transients	–2	65	
T_J operating junction temperature		–40	150	°C
T_{stg} storage temperature range		–55	165	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

			MIN	MAX	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)		2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2)		500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
Buck Regulator	VIN	4	60	V
	CB	4	66	
	CB to SW	–0.3	6	
	SW	–1	60	
	FB	0	5	
Control	$\overline{SHDN}$	0	60	V
Temperature	Operating junction temperature, T_J	–40	125	°C

6.4 Thermal Information

THERMAL METRIC(1)		LV2862 TSOT 6 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	102	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	36.9	
$R_{\theta JB}$	Junction-to-board characterization parameter	28.4	

(1) All numbers apply for packages soldered directly onto a 3" x 3" PC board with 2 oz. copper on 4 layers in still air in accordance to JEDEC standards. Thermal resistance varies greatly with layout, copper thickness, number of layers in PCB, power distribution,

number of thermal vias, board size, ambient temperature, and air flow. For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

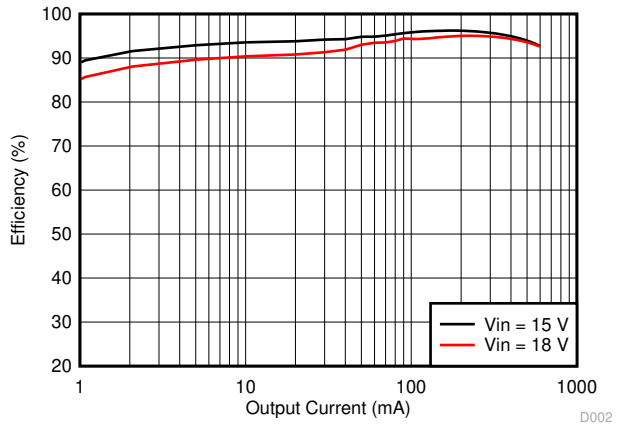
6.5 Electrical Characteristics

V_{IN} = 12 V, $\overline{SHDN}$ = V_{IN}. T_J = 25°C unless otherwise noted.

PARAMETER	CONDITION	MIN	TYP	MAX	UNIT
VIN (Input Power Supply)					
Operating input voltage		4		60	V
Shutdown supply current	EN = 0 V		1	3	µA
Undervoltage lockout thresholds	Rising			4	V
	Falling	3			V
I_Q	Eco-mode, no load, V_{IN} = 12 V, not switching		28		µA
$\overline{SHDN}$ and UVLO					
Rising $\overline{SHDN}$ Threshold Voltage		1.05	1.25	1.38	V
$\overline{SHDN}$ PIN current	$\overline{SHDN}$ = 2.3 V		– 4.2		µA
	$\overline{SHDN}$ = 0.9 V		– 1		µA
Hysteresis current			-3		µA
HIGH-SIDE MOSFET					
On-resistance	V_{IN} = 12 V, CB to SW = 5.8 V		900		mΩ
t_{ON-min}	f_{SW} = 2.1 MHz		80		ns
D_{MAX} : Maximum duty cycle			96%		
V_{FB} : Feedback voltage		0.74	0.765	0.79	V
CURRENT LIMIT					
Peak Current limit threshold			1200		mA
f_{SW} Switching frequency	LV2862X	560	770	980	kHz
	LV2862Y	1785	2100	2415	
THERMAL PERFORMANCE					
$T_{SHUTDOWN}$ Thermal shutdown trip point			170		ºC
T_{hys}	Hysteresis		10		ºC

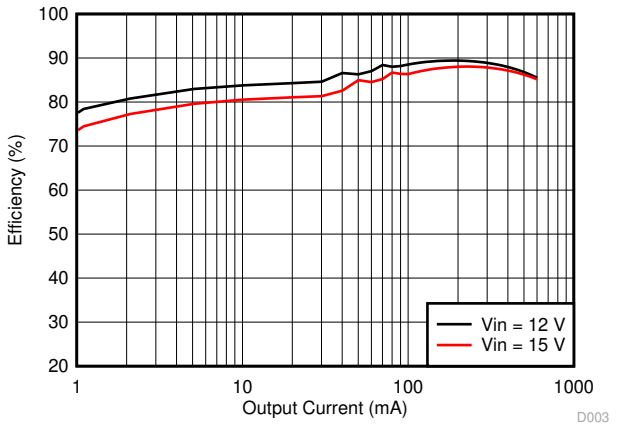
6.6 Typical Characteristics

Unless otherwise specified the following conditions apply: V_{IN} = 12 V, SHDN = V_{IN}, T_A = 25°C



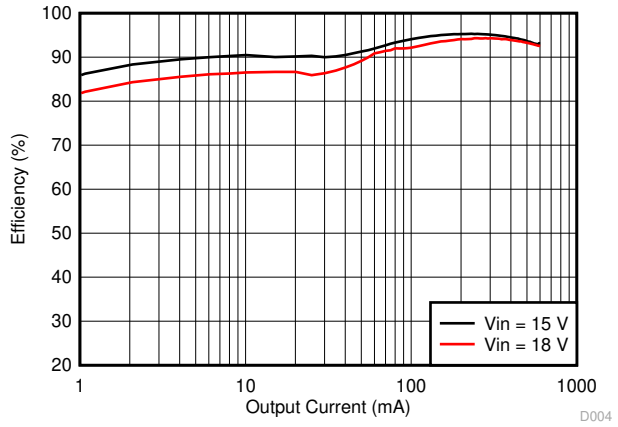
V_{OUT} = 12 V　　f_{SW} = 770 kHz
L1 = 22 µH　　C_{OUT} = 10 µF

图 6-1. Efficiency versus Load Current



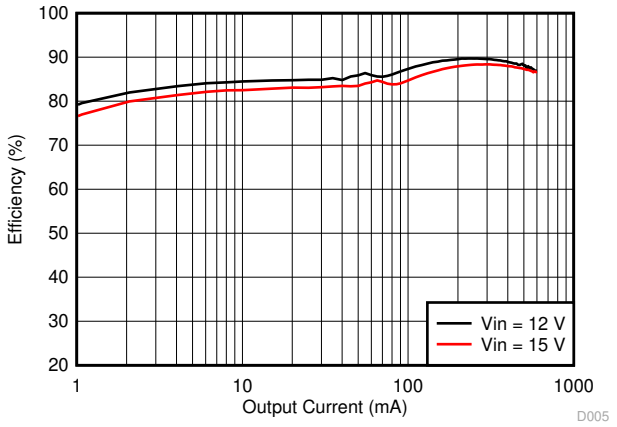
V_{OUT} = 5 V　　f_{SW} = 770 kHz
L1 = 22 µH　　C_{OUT} = 10 µF

图 6-2. Efficiency versus Load Current



V_{OUT} = 12 V　　f_{SW} = 2.1 MHz
L1 = 10 µH　　C_{OUT} = 10 µF

图 6-3. Efficiency versus Load Current



V_{OUT} = 5 V　　f_{SW} = 2.1 MHz
L1 = 10 µH　　C_{OUT} = 10 µF

图 6-4. Efficiency versus Load Current

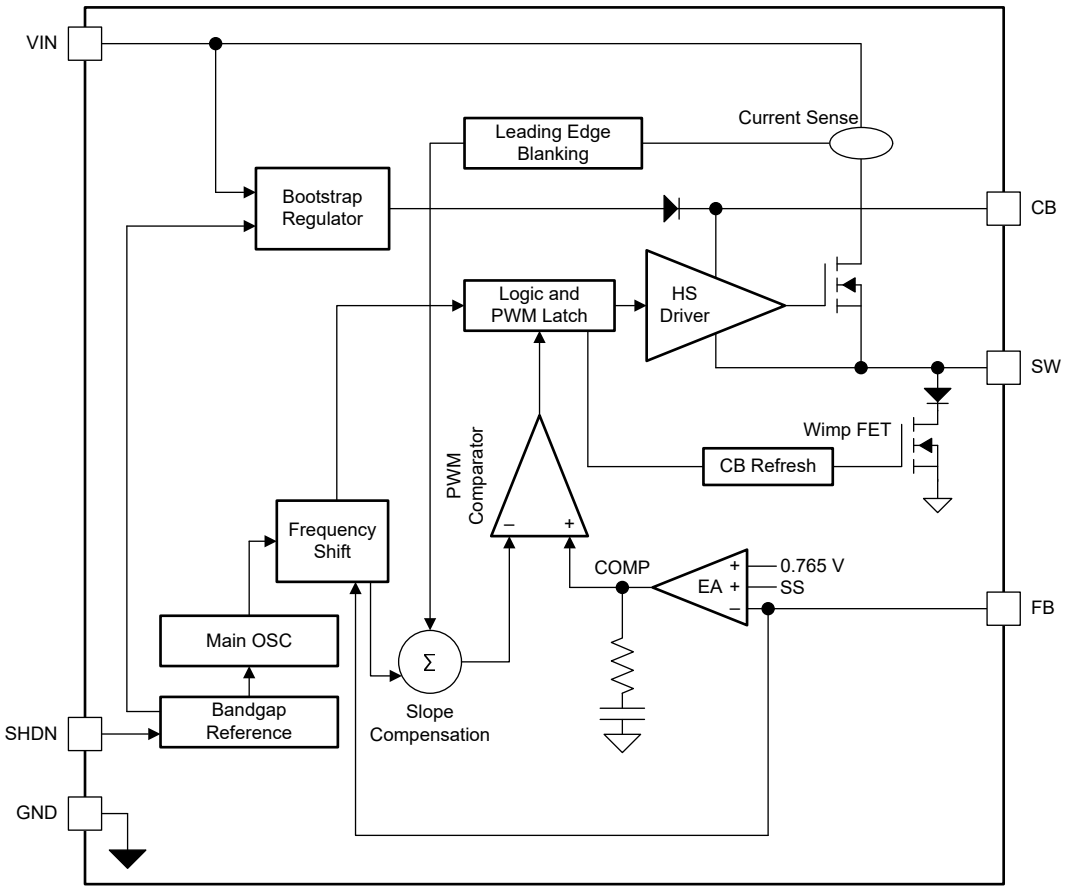
7 Detailed Description

7.1 Overview

The LV2862 device is a 60-V, 600-mA, step-down (buck) regulator. The buck regulator has a very low quiescent current during light load to prolong the battery life.

The LV2862 improves performance during line and load transients by implementing a constant frequency, current mode control which reduces output capacitance and simplifies frequency compensation design. The LV2862 reduces the external component count by integrating the boot recharge diode. The bias voltage for the integrated high-side MOSFET is supplied by a capacitor on the CB to SW pin. The boot capacitor voltage is monitored by a UVLO circuit and turns the high-side MOSFET off when the boot voltage falls below a preset threshold. The LV2862 can operate at high duty cycles because of the boot UVLO and refresh the wimp FET. The output voltage can be stepped down to as low as the 0.8 V. Internal soft start is featured to minimize inrush currents.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Continuous Conduction Mode

The LV2862 steps the input voltage down to a lower output voltage. In continuous conduction mode (when the inductor current never reaches zero at CCM), the buck regulator operates in two cycles. The power switch is connected between V_{IN} and SW. In the first cycle of operation, the transistor is closed and the diode is reverse biased. Energy is collected in the inductor and the load current is supplied by Cout and the rising current through the inductor. During the second cycle, the transistor is open and the diode is forward biased due to the fact that the inductor current cannot instantaneously change direction. The energy stored in the inductor is transferred to the load and output capacitor. The ratio of these two cycles determines the output voltage. The output voltage is

defined approximately as: D = V_{OUT} / V_{IN} and D' = (1 - D) where D is the duty cycle of the switch. D and D' are required for design calculations.

7.3.2 Fixed Frequency PWM Control

The LV2862 has two fixed frequency options and implements peak current mode control. The output voltage is compared through external resistors on the FB pin to an internal voltage reference by an error amplifier that drives the internal COMP node. An internal oscillator initiates the turnon of the high-side power switch. The error amplifier output is compared to the high-side power switch current. When the power switch current reaches the level set by the internal COMP voltage, the power switch is turned off. The internal COMP node voltage increases and decreases as the output current increases and decreases. The device implements a current limit by clamping the COMP node voltage to a maximum level.

7.3.3 Eco-mode

The LV2862 operates in Eco-mode at light load currents to improve efficiency by reducing switching and gate drive losses. For Eco-mode operation, the LV2862 senses peak current, not average or load current, so the load current where the device enters Eco-mode is dependent on V_{IN}, V_{OUT}, and the output inductor value. When the load current is low and the output voltage is within regulation, the device enters ECO mode (see 图 8-10) and draws only 28-µA input quiescent current.

7.3.4 Bootstrap Voltage (CB)

The LV2862 has an integrated boot regulator, and requires a small ceramic capacitor between the CB and SW pins to provide the gate drive voltage for the high-side MOSFET. The CB capacitor is refreshed when the high-side MOSFET is off and the low-side diode conducts.

To improve dropout, the LV2862 is designed to operate at 96% duty cycle as long as the CB to SW pin voltage is greater than 3 V. When the voltage from CB to SW drops below 3 V, the high-side MOSFET is turned off using an UVLO circuit which allows the low-side diode to conduct and refresh the charge on the CB capacitor. Because the supply current sourced from the CB capacitor is low, the high-side MOSFET can remain on for more switching cycles than is required to refresh the capacitor, thus the effective duty cycle of the switching regulator is high.

Attention must be taken in maximum duty cycle applications with light load. To ensure SW can be pulled to ground to refresh the CB capacitor, an internal circuit charges the CB capacitor when the load is light or the device is working in dropout condition.

7.3.5 Enable ($\overline{\text{SHDN}}$) and VIN Undervoltage Lockout (UVLO)

The LV2862 $\overline{\text{SHDN}}$ pin is a high-voltage tolerant input with an internal pullup circuit. The device can be enabled even if the $\overline{\text{SHDN}}$ pin is floating. The regulator can also be turned on using 1.25 V or higher logic signals. It can be used if the use of a higher voltage is desired due to system or other constraints. A 100-kΩ or larger resistor is recommended between the applied voltage and the $\overline{\text{SHDN}}$ pin to protect the device. When $\overline{\text{SHDN}}$ is pulled down to 0 V, the chip is turned off and enters the lowest shutdown current mode. In shutdown mode, the supply current is decreased to approximately 1 µA. If the shutdown function is not to be used, the $\overline{\text{SHDN}}$ pin can be tied to V_{IN} through a 100-kΩ resistor. The maximum voltage to the $\overline{\text{SHDN}}$ pin must not exceed 60 V. The LV2862 has an internal UVLO circuit to shut down the output if the input voltage falls below an internally fixed UVLO threshold level. This ensures that the regulator is not latched into an unknown state during low input voltage conditions. The regulator powers up when the input voltage exceeds the voltage level. If there is a requirement for a higher UVLO voltage, the $\overline{\text{SHDN}}$ pin can be used to adjust the input voltage UVLO by using external resistors.

7.3.6 Setting the Output Voltage

The output voltage is set using the feedback pin and a resistor divider connected to the output as shown on the front page schematic. The feedback pin voltage is 0.765 V, so the ratio of the feedback resistors sets the output voltage according to 方程式 1:

$$V_{OUT} = 0.765\ V\ (1 + (R1 / R2)) \quad (1)$$

Typically, R2 is given as 1 kΩ – 100 kΩ for a starting value. To solve for R1 given R2 and V_{OUT}, use R1 = R2 ((V_{OUT} / 0.765 V) – 1).

7.3.7 Current Limit

The LV2862 implements current mode control which uses the internal COMP voltage to turn off the high-side MOSFET on a cycle-by-cycle basis. Each cycle, the switch current and internal COMP voltage are compared. When the peak switch current intersects the COMP voltage, the high-side switch is turned off. During overcurrent conditions that pull the output voltage low, the error amplifier responds by driving the COMP node high, increasing the switch current. The error amplifier output is clamped internally, which functions as a switch current limit.

7.3.8 Thermal Shutdown

The device implements an internal thermal shutdown to protect itself if the junction temperature exceeds 170°C (typ). The thermal shutdown forces the device to stop switching when the junction temperature exceeds the thermal trip threshold. After the junction temperature decreases below 160°C (typ), the device reinitiates the power-up sequence.

7.4 Device Functional Modes

This device does not have any device functional modes.

8 Application and Implementation

备注

以下应用部分中的信息不属于 TI 器件规格的范围，TI 不担保其准确性和完整性。TI 的客 户应负责确定器件是否适用于其应用。客户应验证并测试其设计，以确保系统功能。

8.1 Application Information

The LV2862 is a PWM DC/DC buck (step-down) regulator. With a wide input range from 4 V to 60 V, it is suitable for a wide range of applications from, industrial to automotive, for power conditioning from unregulated source. Soft start and compensation circuits are implemented internally, which allow the device to be used with minimized external components.

8.2 Typical Application

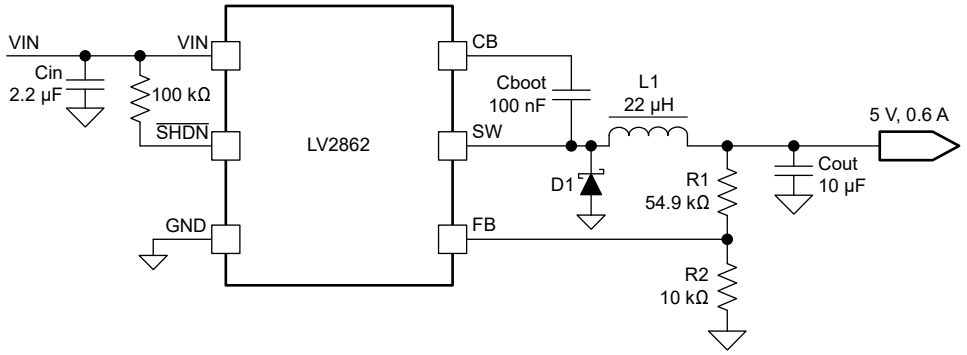


图 8-1. Application Circuit, 5-V Output

8.2.1 Design Requirements

8.2.1.1 Design Guide – Step By Step Design Procedure

表 8-1 details the design of a high frequency switching regulator using ceramic output capacitors. A few parameters must be known to start the design process. These parameters are typically determined at the system level:

表 8-1. Design Parameters

Input Voltage, V_{IN}		9 V to 16 V, Typical 12 V
Output Voltage, V_{OUT}		5.0 V ± 3%
Maximum Output Current Example I_{O_max}		0.6 A
Minimum Output Current Example I_{O_min}		0.03 A
Transient Response 0.03 A to 0.6 A		5%
Output Voltage Ripple		1%
Switching Frequency f_{SW}		770 kHz
Target during Load Transient	Overvoltage Peak Value	106% of Output Voltage
	Undervoltage Value	91% of Output Voltage

8.2.2 Detailed Design Procedure

8.2.2.1 Selecting the Switching Frequency

The first step is to decide on a switching frequency for the regulator. Typically, choose the highest switching frequency possible because this switching frequency produces the smallest solution size. The high switching frequency allows for lower valued inductors and smaller output capacitors compared to a power supply that

switches at a lower frequency. The switching frequency that can be selected is limited by the minimum on-time of the internal power switch, the input voltage and the output voltage, and the frequency shift limitation. For this example, the output voltage is 5 V, the maximum input voltage is 16 V, and a switching frequency of 770 kHz is used.

8.2.2.2 Output Inductor Selection

The most critical parameters for the inductor are the inductance, peak current, and the DC resistance. The inductance is related to the peak-to-peak inductor ripple current, the input, and the output voltages. Because the ripple current increases with the input voltage, the maximum input voltage is always used to determine the inductance. To calculate the minimum value of the output inductor, use 方程式 1. A reasonable value for the ripple current is 40% (K_{IND}) of the DC output current. For this design example, the minimum inductor value is calculated to be 20.4 µH, and a nearest standard value was chosen: 22 µH. For the output filter inductor, it is important that the RMS current and saturation current ratings not be exceeded. The RMS and peak inductor current can be found in 方程式 3 and 方程式 4. The inductor ripple current is 0.22 A, and the RMS current is 0.6 A. As the equation set demonstrates, lower ripple currents reduce the output voltage ripple of the regulator but require a larger value of inductance. A good starting point for most applications is 22 µH with a 1.6-A current rating. Using a rating near 1.6 A enables the LV2862 to current limit without saturating the inductor. This is preferable to the LV2862 going into thermal shutdown mode and the possibility of damaging the inductor if the output is shorted to ground or other long-term overload.

$$L_{o\,\min} = \frac{V_{in\,\max} - V_{out}}{I_o \times K_{IND}} \times \frac{V_{out}}{V_{in\,\max} \times f_{sw}} \tag{2}$$

$$I_{ripple} = \frac{V_{out} \times (V_{in\,\max} - V_{out})}{V_{in\,\max} \times L_o \times f_{sw}} \tag{3}$$

$$I_{L\text{-}RMS} = \sqrt{I_o^{\,2} + \frac{1}{12} I_{ripple}^{\,2}} \tag{4}$$

$$I_{L-peak} = I_o + \frac{I_{ripple}}{2} \tag{5}$$

8.2.2.3 Output Capacitor Selection

The selection of C_{OUT} is mainly driven by three primary considerations. The output capacitor determines the modulator pole, the output voltage ripple, and how the regulator responds to a large change in load current. The output capacitance needs to be selected based on the most stringent of these three criteria.

The first criterion is the desired response to a large change in the load current. The regulator usually needs two or more clock cycles for the control loop to see the change in load current and output voltage and adjust the duty cycle to react to the change. The output capacitance must be large enough to supply the difference in current for two clock cycles while only allowing a tolerable amount of droop in the output voltage. 方程式 5 shows the minimum output capacitance necessary to accomplish this. The transient load response is specified as a 3% change in V_{OUT} for a load step from 0.03 A to 0.6 A (full load), ΔI_{OUT} = 0.6 - 0.03 = 0.57 A and ΔV_{OUT} = 0.03 × 5 = 0.15 V. Using these numbers gives a minimum capacitance of 10.8 µF. For ceramic capacitors, the ESR is usually small enough to ignore in this calculation. Aluminum electrolytic and tantalum capacitors have higher ESR that must be taken into account.

The stored energy in the inductor produces an output voltage overshoot when the load current rapidly decreases. The output capacitor must also be sized to absorb energy stored in the inductor when transitioning from a high load current to a lower load current. 方程式 6 is used to calculate the minimum capacitance to keep the output voltage overshoot to a desired value. Where L is the value of the inductor, I_{OH}, is the output current under heavy load, I_{OL} is the output under light load, V_f is the final peak output voltage, and V_i is the initial capacitor voltage. For this example, the worst case load step is from 0.6 A to 0.03 A. The output voltage increases during this load transition and the stated maximum in our specification is 3% of the output voltage.

This makes $V_{o\_overshoot}$ = 1.03 × 5 = 5.15 V. V_i is the initial capacitor voltage which is the nominal output voltage of 5 V. Using these numbers in 方程式 6 yields a minimum capacitance of 5.2 µF.

方程式 7 calculates the minimum output capacitance needed to meet the output voltage ripple specification where f_{SW} is the switching frequency, V_{o_ripple} is the maximum allowable output voltage ripple, and I_{L_ripple} is the inductor ripple current. 方程式 7 yields 0.26 µF. 方程式 8 calculates the maximum ESR an output capacitor can have to meet the output voltage ripple specification. indicates the ESR must be less than 680 mΩ.

Additional capacitance de-ratings for aging, temperature, and dc bias must be factored in which increases this minimum value. For this example, 10-µF ceramic capacitors are used. Capacitors in the range of 10 µF – 100 µF are a good starting point with an ESR of 0.7 Ω or less.

$$C_{out} > \frac{2 \times \Delta I_{out}}{fsw \times \Delta V_{out}} \tag{6}$$

$$C_{out} > L_o \times \frac{(Ioh^2 - Iol^2)}{(Vf^2 - Vi^2)} \tag{7}$$

$$C_{out} > \frac{1}{8 \times fsw} \times \frac{1}{\frac{V_{o\_ripple}}{I_{L\_ripple}}} \tag{8}$$

$$R_{ESR} < \frac{V_{o\_ripple}}{I_{L\_ripple}} \tag{9}$$

8.2.2.4 Schottky Diode Selection

The breakdown voltage rating of the diode is preferred to be 25% higher than the maximum input voltage. In the target application, the current rating for the diode must be equal to the maximum output current for best reliability in most applications. In cases where the input voltage is not much greater than the output voltage, the average diode current is lower. In this case, it is possible to use a diode with a lower average current rating, approximately (1 - D) × I_{OUT}. However, the peak current rating must be higher than the maximum load current. A 0.5-A to 1-A rated diode is a good starting point.

8.2.2.5 Input Capacitor Selection

A low ESR ceramic capacitor is needed between the VIN pin and ground pin. This capacitor prevents large voltage transients from appearing at the input. Use a 2.2 µF – 10 µF value with X5R or X7R dielectric. Depending on construction, the value of a ceramic capacitor can decrease up to 50% of its nominal value when rated voltage is applied. Consult with the capacitor manufacturer's data sheet for information on capacitor derating over voltage and temperature. The capacitor must also have a ripple current rating greater than the maximum input current ripple of the LV2862. The input ripple current can be calculated using 方程式 10 and 方程式 11.

For this example design, one 4.7-µF, 50-V capacitor is selected. The input capacitance value determines the input ripple voltage of the regulator. The input voltage ripple can be calculated using 方程式 10. Using the design example values, I_{outmax} = 0.6 A, C_{in} = 2.2 µF, and f_{sw} = 770 kHz yields an input voltage ripple of 97 mV and an RMS input ripple current of 0.3 A.

$$I_{cirms} = I_{out} \times \sqrt{\frac{V_{out}}{V_{in\,\min}} \times \frac{(V_{in\,\min} - V_{out})}{V_{in\,\min}}} \tag{10}$$

$$\Delta V_{in} = \frac{I_{out\,\max} \times 0.25}{C_{in} \times fsw} \tag{11}$$

8.2.2.5.1 Bootstrap Capacitor Selection

A 0.1-μF ceramic capacitor or larger is recommended for the bootstrap capacitor (C_{BOOT}). For applications where the input voltage is close to output voltage, a larger capacitor is recommended, generally 0.1 μF to 1 μF to ensure plenty of gate drive for the internal switches and a consistently low R_{DSON}. A ceramic capacitor with an X7R or X5R grade dielectric with a voltage rating of 10 V or higher is recommended because of the stable characteristics over temperature and voltage.

表 8-2. Output Voltage Inductor and Capacitor Combinations

P/N	V_{OUT} (V)	R1 (kΩ)	R2 (kΩ)	L (μH)	C_{OUT} (μF)
LV2862X	5	54.9 (1%)	10 (1%)	22	10
LV2862X	5.7	64.9 (1%)	10 (1%)	22	10
LV2862X	12	147 (1%)	10 (1%)	22	10

8.2.2.5.1.1 Typical Application Circuits

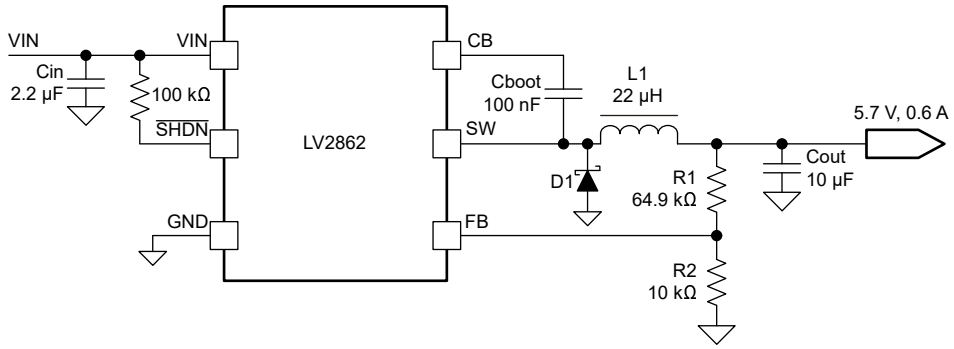


图 8-2. Application Circuit, 5.7-V Output

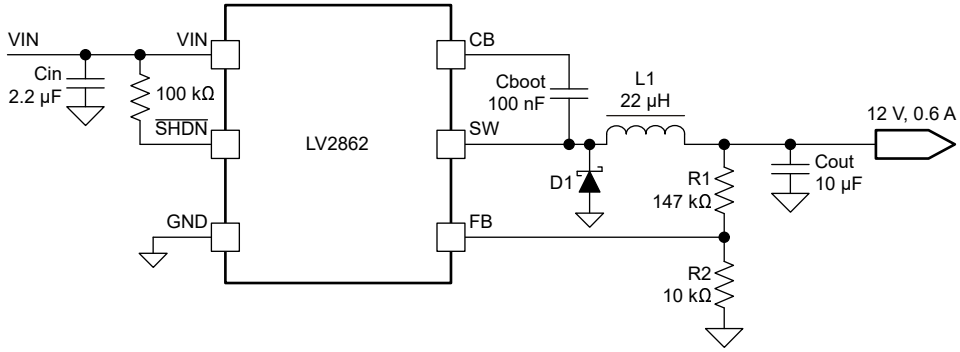
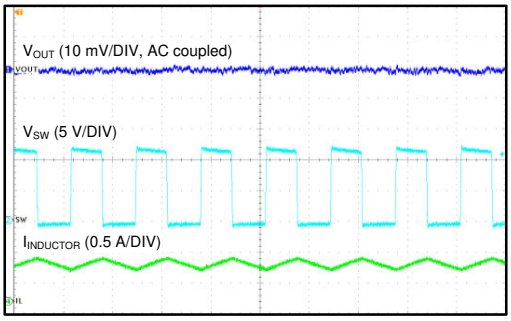


图 8-3. Application Circuit, 12-V Output

表 8-2 lists the recommended typical output voltage inductor/capacitor combinations for optimized total solution size.

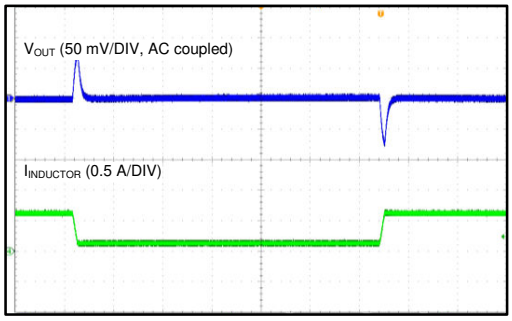
8.2.3 Application Curves

Unless otherwise specified the following conditions apply: V_{IN} = 12 V, f_{SW} = 770 kHz, L = 22 µH, C_{OUT} = 10 µF, T_A = 25°C



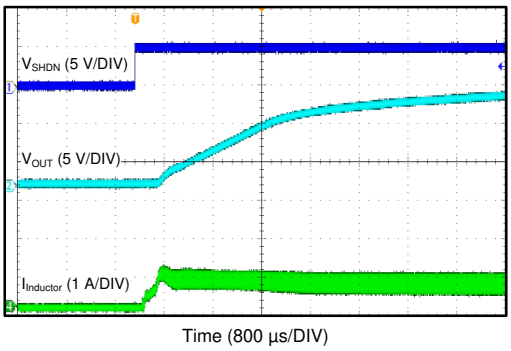
V_{OUT} = 5 V I_{OUT} = 600 mA

图 8-4. Switching Node and Output Voltage Waveform



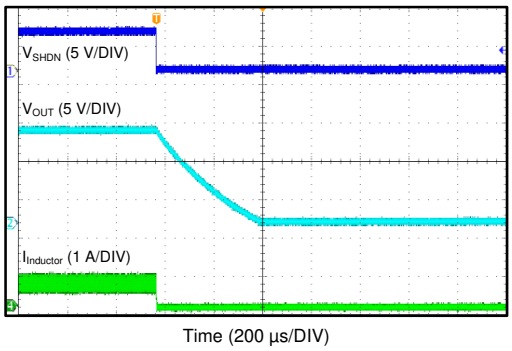
V_{OUT} = 5 V

图 8-5. Load Transient Between 0.1 A and 0.6 A



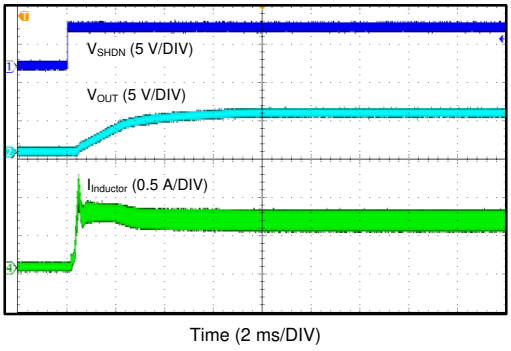
V_{IN} = 15 V V_{OUT} = 12 V / 600 mA

图 8-6. Start-up Waveform



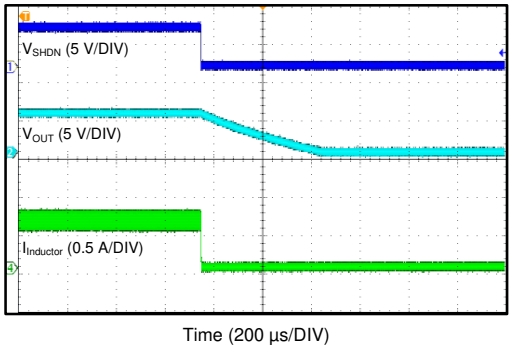
V_{IN} = 15 V V_{OUT} = 12 V / 600 mA

图 8-7. Shutdown Waveform



V_{IN} = 12 V V_{OUT} = 5 V / 600 mA

图 8-8. Start-up Waveform



V_{IN} = 12 V V_{OUT} = 5 V / 600 mA

图 8-9. Shutdown Waveform

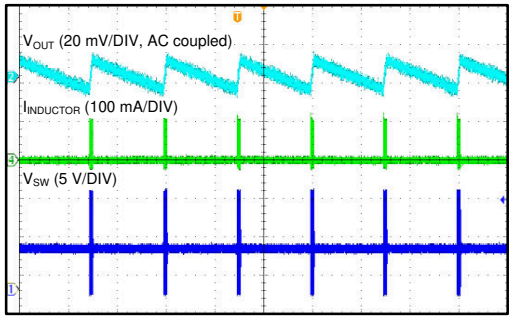


图 8-10. Eco-mode Operation

8.3 Power Supply Recommendations

The LV2862 is designed to operate from an input voltage supply range between 4 V and 60 V. This input supply must be able to withstand the maximum input current and maintain a voltage above 4 V. The resistance of the input supply rail must be low enough that an input current transient does not cause a high enough drop at the LV2862 supply voltage that can cause a false UVLO fault triggering and system reset. If the input supply is located more than a few inches from the LV2862, additional bulk capacitance can be required in addition to the ceramic input capacitors.

8.4 Layout

8.4.1 Layout Guidelines

Layout is a critical portion of good power supply design. The following guidelines helps users design a PCB with the best power conversion performance, thermal performance, and minimized generation of unwanted EMI.

1. The feedback network, resistors R1 and R2, must be kept close to the FB pin and away from the inductor to minimize coupling noise into the feedback pin.
2. The input capacitor C_{IN} must be placed close to the V_{IN} pin. This reduces copper trace inductance which affects input voltage ripple of the IC.
3. The inductor L1 must be placed close to the SW pin to reduce magnetic and electrostatic noise.
4. The output capacitor C_{OUT} must be placed close to the junction of L1 and the diode D1. The L1, D1, and C_{OUT} trace must be as short as possible to reduce conducted and radiated noise.
5. The ground connection for the diode, C_{IN} and C_{OUT} must be tied to the system ground plane in only one spot (preferably at the C_{OUT} ground point) to minimize conducted noise in the system ground plane.
6. For more detail on switching power supply layout considerations, see Application Note AN-1149, *Layout Guidelines for Switching Power Supplies*.

8.4.2 Layout Example

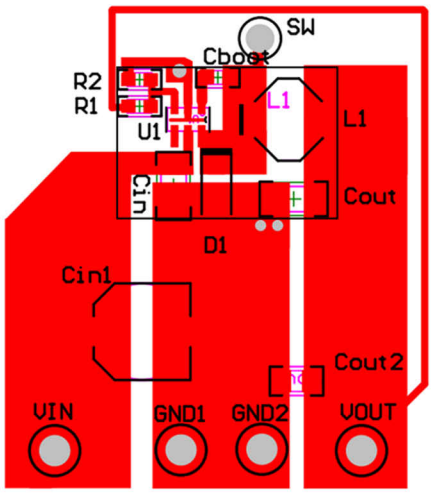


图 8-11. Layout Example

9 Device and Documentation Support

9.1 Documentation Support

9.1.1 Related Documentation

Texas Instruments, *Layout Guidelines for Switching Power Supplies* application report

9.2 接收文档更新通知

要接收文档更新通知，请导航至 ti.com 上的器件产品文件夹。点击 *订阅更新* 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

9.3 支持资源

TI E2E™ 支持论坛是工程师的重要参考资料，可直接从专家获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题可获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的《使用条款》。

9.4 Trademarks

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ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

9.6 术语表

TI 术语表	本术语表列出并解释了术语、首字母缩略词和定义。

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
LV2862XLVDDCR	Active	Production	SOT-23-THIN (DDC) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	C02X
LV2862XLVDDCR.A	Active	Production	SOT-23-THIN (DDC) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	C02X
LV2862XLVDDCT	Active	Production	SOT-23-THIN (DDC) | 6	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	C02X
LV2862XLVDDCT.A	Active	Production	SOT-23-THIN (DDC) | 6	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	C02X
LV2862YDDCR	Active	Production	SOT-23-THIN (DDC) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	C02Y
LV2862YDDCR.A	Active	Production	SOT-23-THIN (DDC) | 6	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	C02Y
LV2862YDDCT	Active	Production	SOT-23-THIN (DDC) | 6	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	C02Y
LV2862YDDCT.A	Active	Production	SOT-23-THIN (DDC) | 6	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	C02Y

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

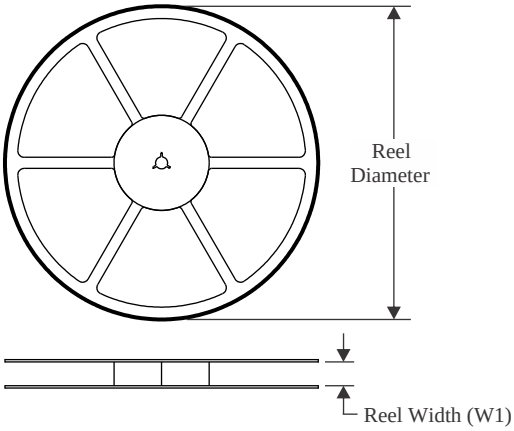
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

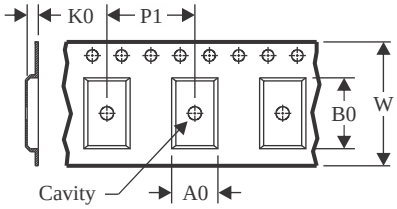
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

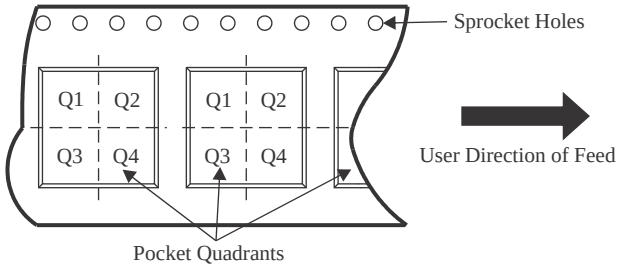


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

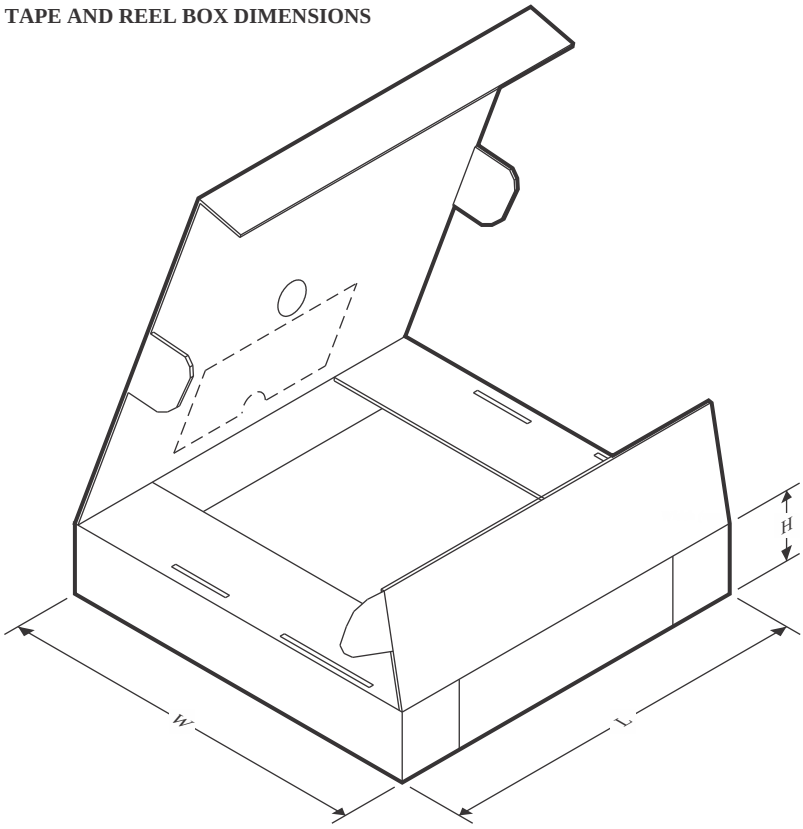
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LV2862XLVDDCR	SOT-23-THIN	DDC	6	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LV2862XLVDDCT	SOT-23-THIN	DDC	6	250	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LV2862YDDCR	SOT-23-THIN	DDC	6	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LV2862YDDCT	SOT-23-THIN	DDC	6	250	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

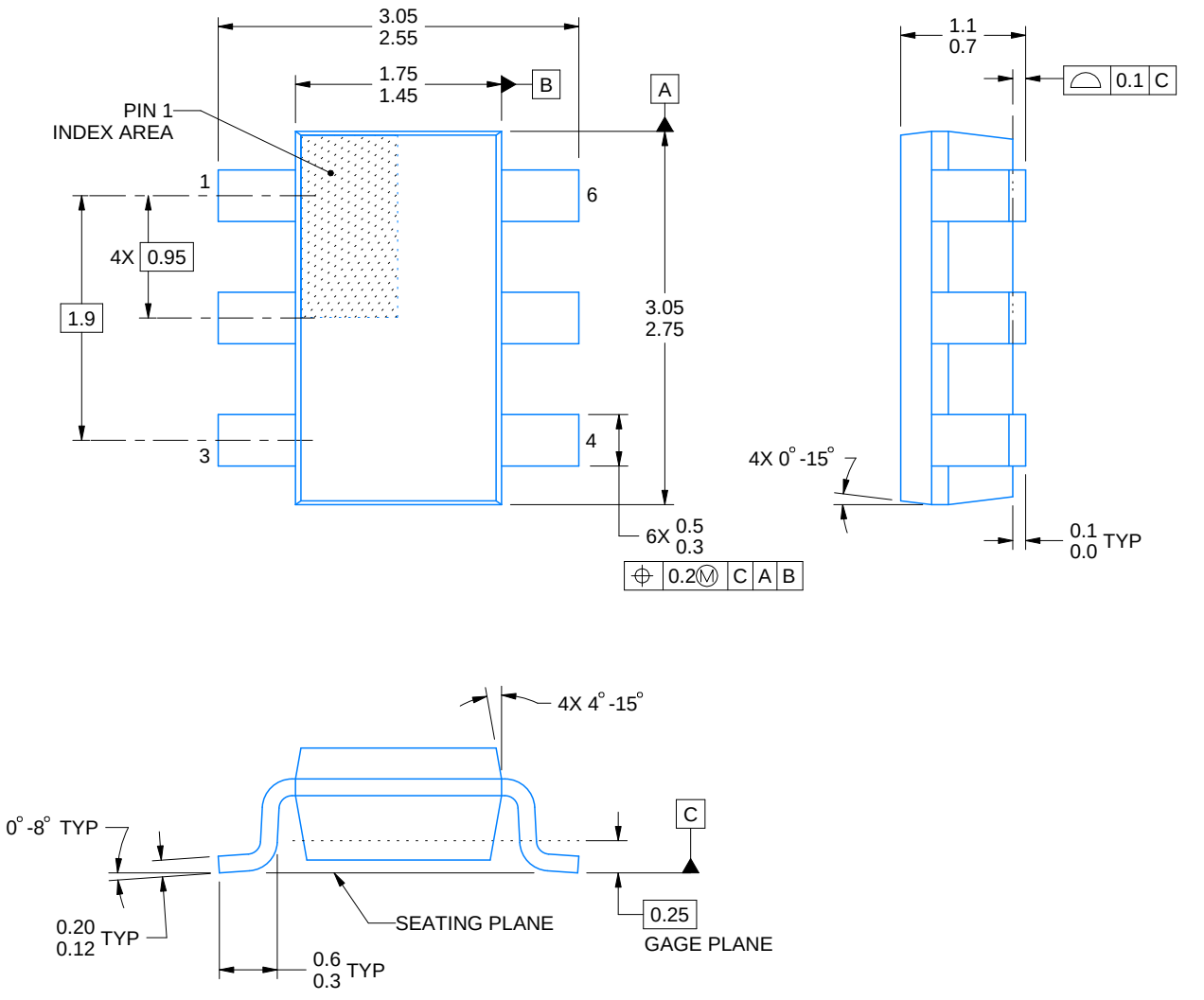
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LV2862XLVDDCR	SOT-23-THIN	DDC	6	3000	208.0	191.0	35.0
LV2862XLVDDCT	SOT-23-THIN	DDC	6	250	208.0	191.0	35.0
LV2862YDDCR	SOT-23-THIN	DDC	6	3000	208.0	191.0	35.0
LV2862YDDCT	SOT-23-THIN	DDC	6	250	208.0	191.0	35.0

PACKAGE OUTLINE

DDC0006A

SOT-23 - 1.1 max height

SMALL OUTLINE TRANSISTOR



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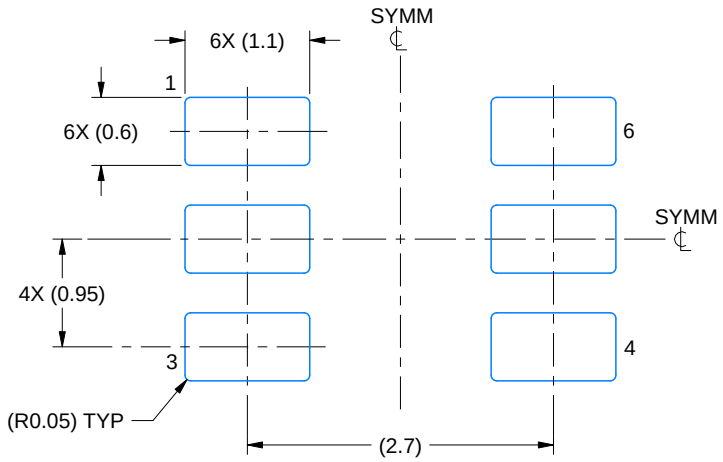
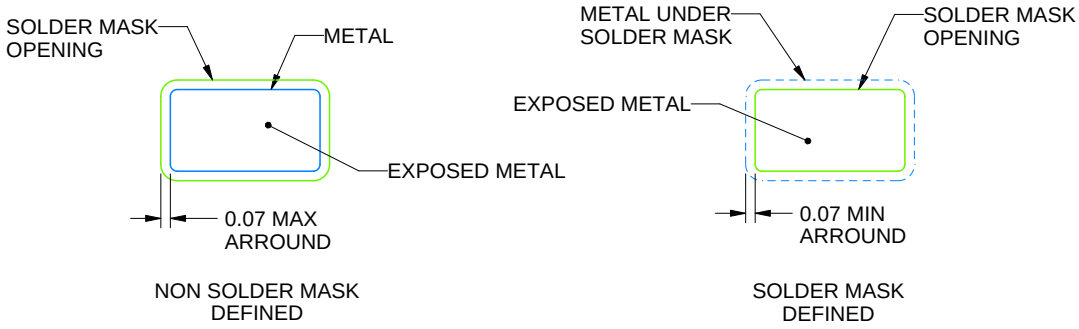
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC MO-193.



LAND PATTERN EXAMPLE
EXPLOSED METAL SHOWN
SCALE:15X



SOLDERMASK DETAILS

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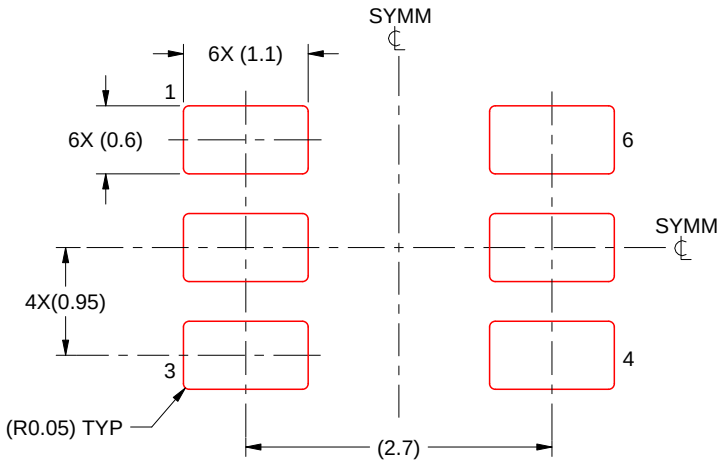
NOTES: (continued)

4. Publication IPC-7351 may have alternate designs.
5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 THICK STENCIL
SCALE:15X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
7. Board assembly site may have different recommendations for stencil design.

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最后更新日期：2025 年 10 月