SoundPLUS™ 高性能、双极输入音频运算放大器

查询样品: OPA1602, OPA1604

特性

- 出色的音质
- 超低噪声：**1 kHz** 时为 **2.5nV/√Hz**
- 超低失真：**1 kHz** 时为 **0.00003%**
- 高压摆率：**20V/μs**
- 高带宽：**35MHz (G = +1)**
- 高开环增益：**120dB**
- 单位增益稳定
- 低静态电流：
  每通道 **2.6mA**
- 轨至轨输出
- 宽泛电源电压：**±2.25V** 至 **±18V**
- 双通道及四通道产品已供货

应用范围

- 专业音频设备
- 广播演播室设备
- 模拟与数字混频器
- 高端 **A/V** 接收器
- 高端 蓝光™ 播放器

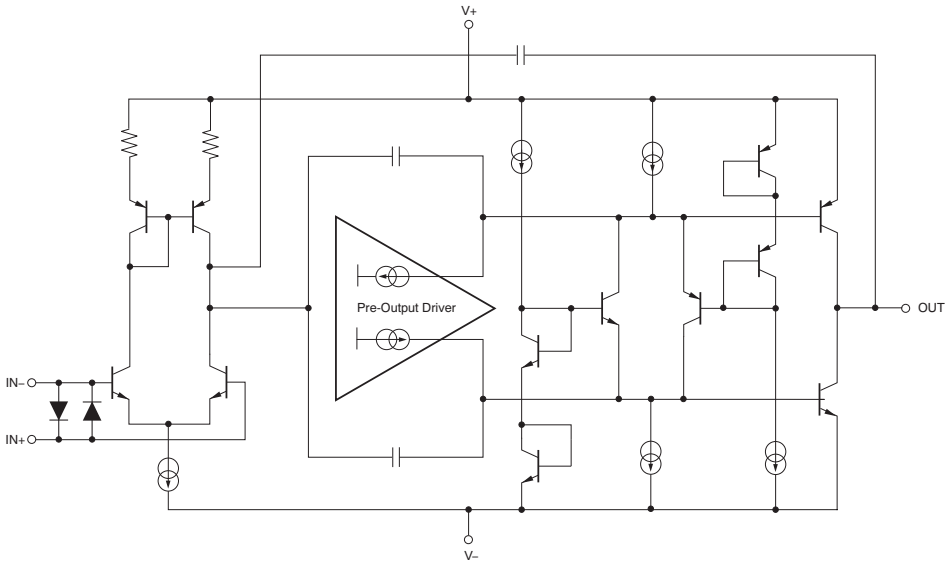
说明

OPA1602 与 OPA1604 双极输入运算放大器能够以超低失真（1kHz 时为 0.00003%）实现 2.5nV/√Hz 的极低噪声密度。 OPA1602 与 OPA1604 系列运算放大器可在 2 kΩ 负载下支持 600 mV 以内的轨至轨输出摆幅，其可提高预留空间，将动态范围最大化。 此外，这些器件还具有 ±30mA 的高输出驱动能力。

上述器件支持 ±2.25 V 至 ±18 V 的极宽泛工作电源，每通道电源电流仅为 2.6 mA。 OPA1602 与 OPA1604 不但单位增益稳定，而且可在各种负载条件下提供优异的动态特性。

它们还采用完全独立的电路系统，可最小化串扰，即便在过驱动或过载时也不受通道间互动的干扰。

OPA1602 与 OPA1604 额定温度范围为 –40°C 至 +85°C。



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ABSOLUTE MAXIMUM RATINGS(1)

Over operating free-air temperature range (unless otherwise noted).

		VALUE	UNIT
Supply Voltage	V_S = (V+) – (V–)	40	V
Input Voltage		(V–) – 0.5 to (V+) + 0.5	V
Input Current (All pins except power-supply pins)		±10	mA
Output Short-Circuit(2)		Continuous	
Operating Temperature		–55 to +125	°C
Storage Temperature		–65 to +150	°C
Junction Temperature		200	°C
ESD Ratings	Human Body Model (HBM)	4	kV
	Charged Device Model (CDM)	1	kV
	Machine Model (MM)	200	V

(1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not supported.
(2) Short-circuit to V_S/2 (ground in symmetrical dual supply setups), one amplifier per package.

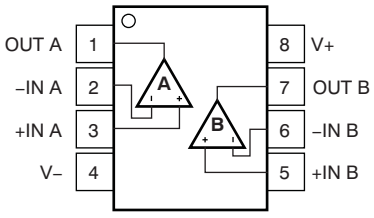
PACKAGE INFORMATION(1)

PRODUCT	PACKAGE-LEAD	PACKAGE DESIGNATOR	PACKAGE MARKING
OPA1602	SO-8	D	O1602A
	MSOP-8	DGK	OCKQ
OPA1604	SO-14	D	O1604A
	TSSOP-14	PW	O1604A

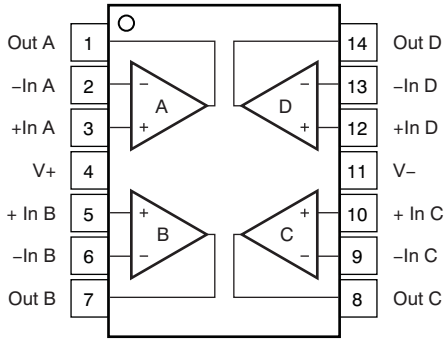
(1) For the most current package and ordering information see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.

PIN CONFIGURATIONS

OPA1602
SO-8, MSOP-8
(TOP VIEW)



OPA1604
SO-14, TSSOP-14
(TOP VIEW)



ELECTRICAL CHARACTERISTICS: V_S = ±2.25V to ±18V

At T_A = +25°C and R_L = 2kΩ, unless otherwise noted. V_{CM} = V_{OUT} = midsupply, unless otherwise noted.

PARAMETER		CONDITIONS	OPA1602, OPA1604 MIN	TYP	MAX	UNIT
AUDIO PERFORMANCE						
Total Harmonic Distortion + Noise	THD+N	G = +1, f = 1kHz, V_O = 3V_{RMS}		0.00003		%
				–130		dB
Intermodulation Distortion	IMD	G = +1, V_O = 3V_{RMS}				
		SMPTE/DIN Two-Tone, 4:1 (60Hz and 7kHz)		0.00003		%
				–130		dB
		DIM 30 (3kHz square wave and 15kHz sine wave)		0.00003		%
				–130		dB
		CCIF Twin-Tone (19kHz and 20kHz)		0.00003		%
				–130		dB
FREQUENCY RESPONSE						
Gain-Bandwidth Product	GBW	G = +1		35		MHz
Slew Rate	SR	G = –1		20		V/µs
Full Power Bandwidth[1]		V_O = 1V_P		3		MHz
Overload Recovery Time		G = –10		1		µs
NOISE						
Input Voltage Noise		f = 20Hz to 20kHz		2.5		μV_{PP}
Input Voltage Noise Density	e_n	f = 100Hz		2.5		nV/√Hz
		f = 1kHz		2.5		nV/√Hz
Input Current Noise Density	I_n	f = 100Hz		2.2		pA/√Hz
		f = 1kHz		1.8		pA/√Hz
OFFSET VOLTAGE						
Input Offset Voltage	V_{OS}	V_S = ±15V		±0.1	±1	mV
vs Power Supply	PSRR	V_S = ±2.25V to ±18V		0.5	2	µV/V
Channel Separation (Dual and Quad)		f = 1kHz		-130		dB
INPUT BIAS CURRENT						
Input Bias Current	I_B	V_{CM} = 0V		±20	±200	nA
Input Offset Current	I_{OS}	V_{CM} = 0V		±20	±200	nA
INPUT VOLTAGE RANGE						
Common-Mode Voltage Range	V_{CM}		(V–) + 2		(V+) – 2	V
Common-Mode Rejection Ratio	CMRR	(V–) + 2V ≤ V_{CM} ≤ (V+) – 2V, V_S ≥ ±5V	114	120		dB
		(V–) + 2V ≤ V_{CM} ≤ (V+) – 2V, V_S < ±5V	100	110		dB
INPUT IMPEDANCE						
Differential				20k || 2		Ω || pF
Common-Mode				10^9 || 2.5		Ω || pF
OPEN-LOOP GAIN						
Open-Loop Voltage Gain	A_{OL}	(V–) + 0.6V ≤ V_O ≤ (V+) – 0.6V, R_L = 2kΩ, V_S ≥ ±5V	114	120		dB
		(V–) + 0.6V ≤ V_O ≤ (V+) – 0.6V, R_L = 2kΩ, V_S < ±5V	106	114		dB
OUTPUT						
Voltage Output	V_{OUT}	R_L = 2kΩ, A_{OL} ≥ 114dB, V_S ≥ ±5V	(V–) + 0.6		(V+) – 0.6	V
		R_L = 2kΩ, A_{OL} ≥ 106dB, V_S < ±5V	(V–) + 0.6		(V+) – 0.6	V
Output Current	I_{OUT}	See Typical Characteristics				mA
Open-Loop Output Impedance	Z_O	f = 1MHz		25		Ω
Short-Circuit Current[2]	I_{SC}			+70/–60		mA
Capacitive Load Drive	C_{LOAD}	See Typical Characteristics				pF

(1) Full-power bandwidth = SR/(2π × V_P), where SR = slew rate.
(2) One channel at a time.

ELECTRICAL CHARACTERISTICS: V_S = ±2.25V to ±18V (continued)

At T_A = +25°C and R_L = 2kΩ, unless otherwise noted. V_{CM} = V_{OUT} = midsupply, unless otherwise noted.

PARAMETER		CONDITIONS	OPA1602, OPA1604			UNIT
			MIN	TYP	MAX	
POWER SUPPLY						
Specified Voltage	V_S		±2.25		±18	V
Quiescent Current(3) Dual, per channel	I_Q	I_{OUT} = 0A		2.6	3.2	mA
Quad, per channel	I_Q	I_{OUT} = 0A		2.8	3.4	mA
TEMPERATURE RANGE						
Specified Range			–40		+85	°C
Operating Range			–55		+125	°C

(3) I_Q value is based on flash test.

THERMAL INFORMATION: OPA1602

THERMAL METRIC(1)		OPA1602 D 8 PINS	OPA1602 DGK 8 PINS	UNITS
θ_{JA}	Junction-to-ambient thermal resistance	105.4	154.7	°C/W
θ_{JCtop}	Junction-to-case (top) thermal resistance	58.6	49.7	
θ_{JB}	Junction-to-board thermal resistance	64.2	107.9	
ψ_{JT}	Junction-to-top characterization parameter	14.1	2.5	
ψ_{JB}	Junction-to-board characterization parameter	66.5	106.7	
θ_{JCbot}	Junction-to-case (bottom) thermal resistance	N/A	N/A	

(1) 有关传统和新的热度量的更多信息，请参阅 *IC* 封装热度量 应用报告 SPRA953。

THERMAL INFORMATION: OPA1604

THERMAL METRIC(1)		OPA1604 D 14 PINS	OPA1604 PW 14 PINS	UNITS
θ_{JA}	Junction-to-ambient thermal resistance	92.8	122.5	°C/W
θ_{JCtop}	Junction-to-case (top) thermal resistance	44.4	36.5	
θ_{JB}	Junction-to-board thermal resistance	39.6	53.9	
ψ_{JT}	Junction-to-top characterization parameter	10.4	2.5	
ψ_{JB}	Junction-to-board characterization parameter	39.3	53.2	
θ_{JCbot}	Junction-to-case (bottom) thermal resistance	N/A	N/A	

(1) 有关传统和新的热度量的更多信息，请参阅 *IC* 封装热度量 应用报告 SPRA953。

TYPICAL CHARACTERISTICS

At T_A = +25°C, V_S = ±15V, and R_L = 2kΩ, unless otherwise noted.

INPUT VOLTAGE NOISE DENSITY AND INPUT CURRENT NOISE DENSITY vs FREQUENCY

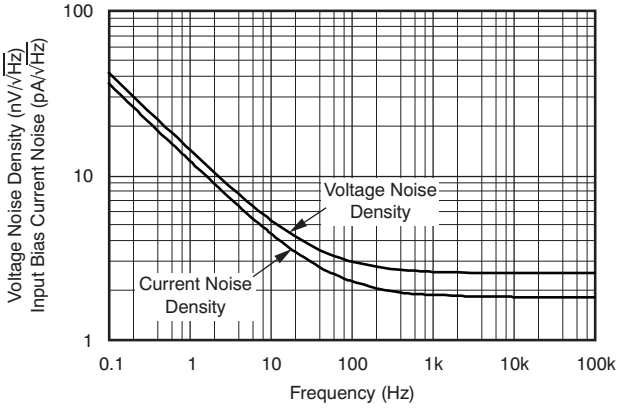


Figure 1.

0.1Hz TO 10Hz NOISE

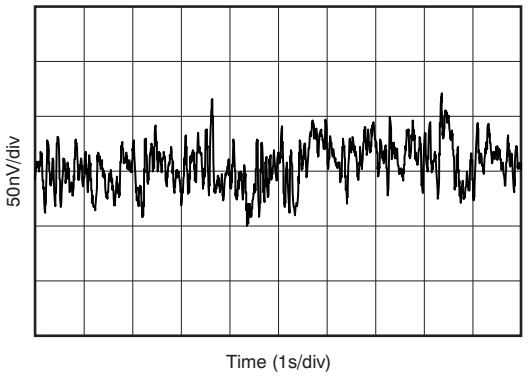


Figure 2.

VOLTAGE NOISE vs SOURCE RESISTANCE

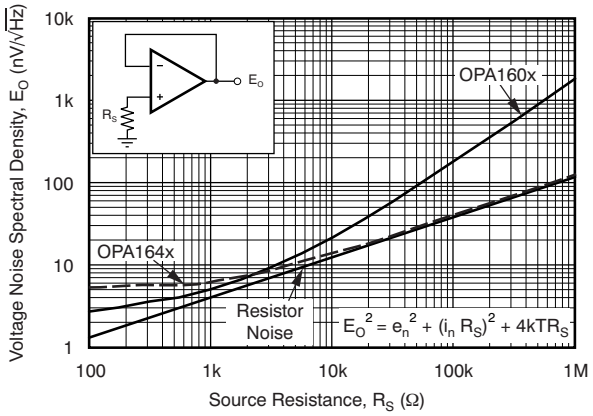


Figure 3.

MAXIMUM OUTPUT VOLTAGE vs FREQUENCY

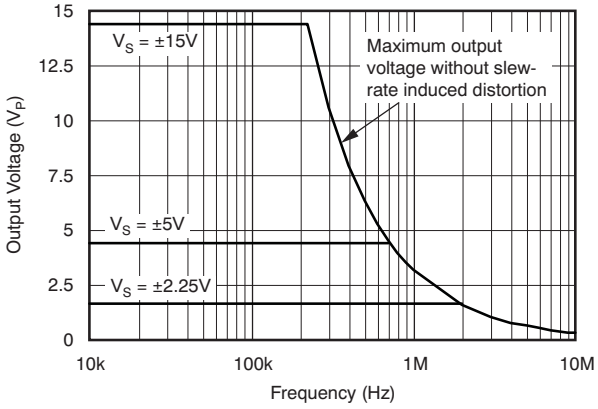


Figure 4.

GAIN AND PHASE vs FREQUENCY

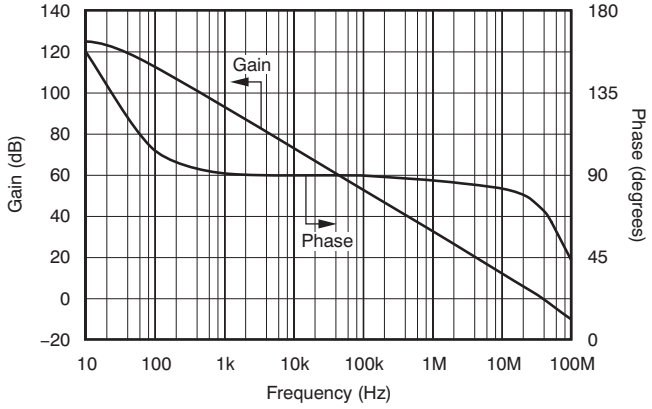


Figure 5.

CLOSED-LOOP GAIN vs FREQUENCY

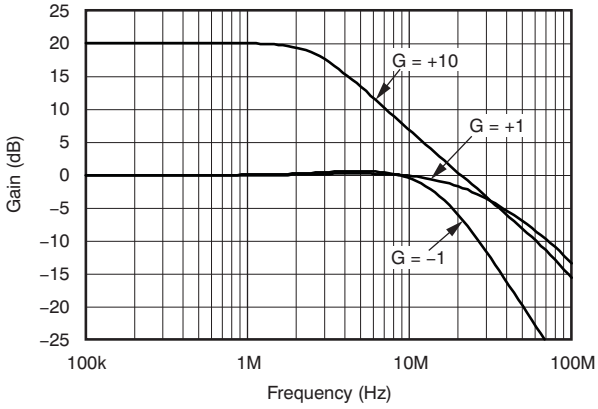


Figure 6.

TYPICAL CHARACTERISTICS (continued)

At T_A = +25°C, V_S = ±15V, and R_L = 2kΩ, unless otherwise noted.

THD+N RATIO vs FREQUENCY

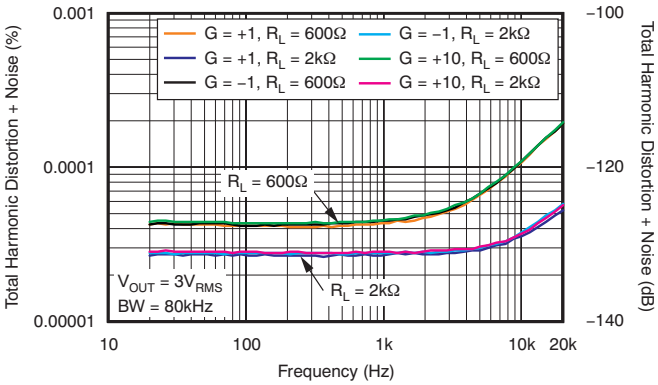


Figure 7.

THD+N RATIO vs FREQUENCY

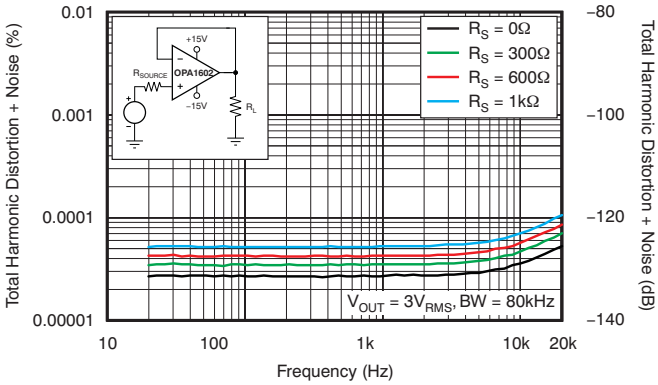


Figure 8.

THD+N RATIO vs FREQUENCY

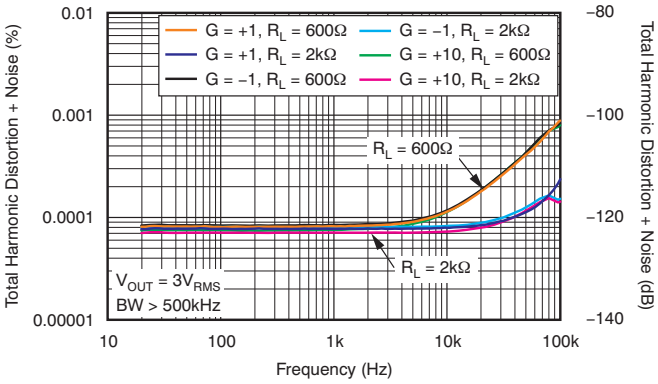


Figure 9.

THD+N RATIO vs FREQUENCY

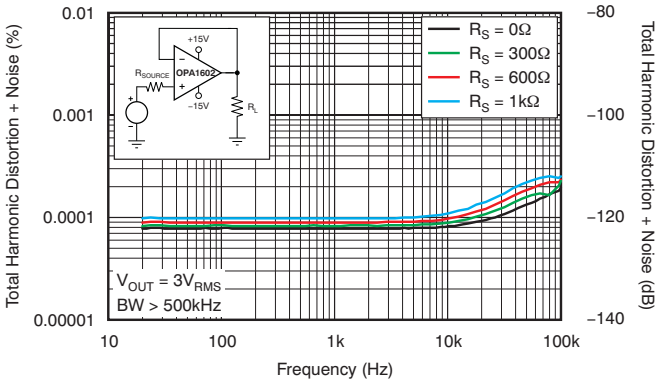


Figure 10.

THD+N RATIO vs OUTPUT AMPLITUDE

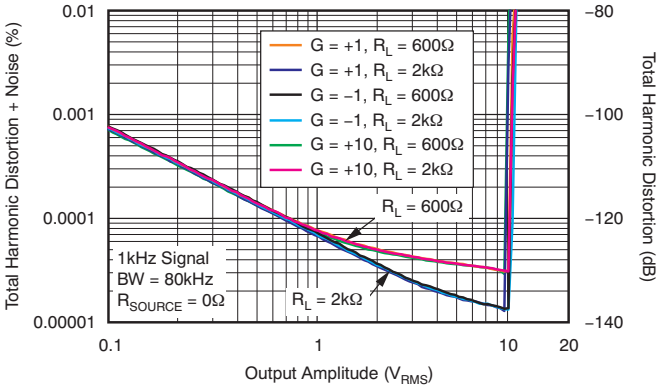


Figure 11.

INTERMODULATION DISTORTION vs OUTPUT AMPLITUDE

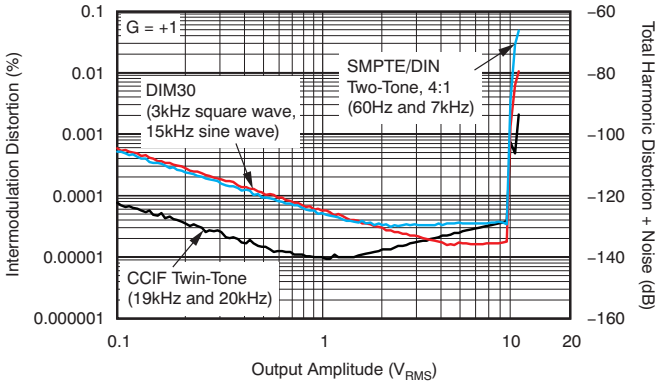


Figure 12.

TYPICAL CHARACTERISTICS (continued)

At T_A = +25°C, V_S = ±15V, and R_L = 2kΩ, unless otherwise noted.

CHANNEL SEPARATION vs FREQUENCY

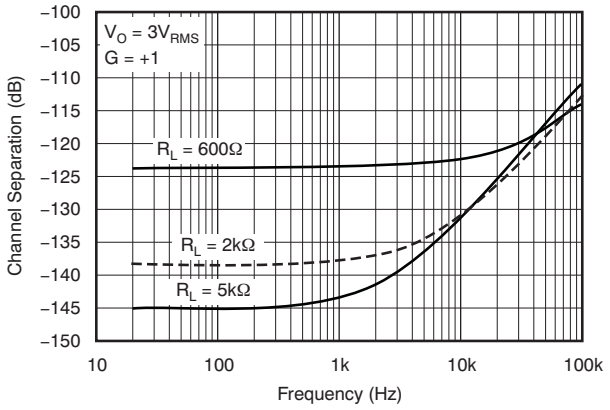


Figure 13.

CMRR AND PSRR vs FREQUENCY (Referred to Input)

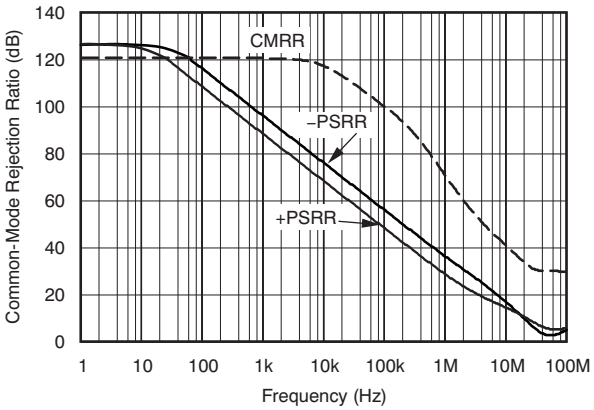


Figure 14.

SMALL-SIGNAL STEP RESPONSE (100mV)

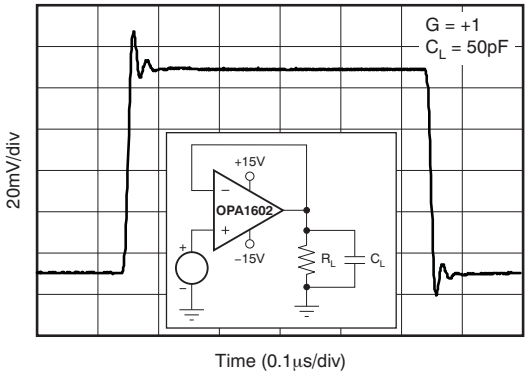


Figure 15.

SMALL-SIGNAL STEP RESPONSE (100mV)

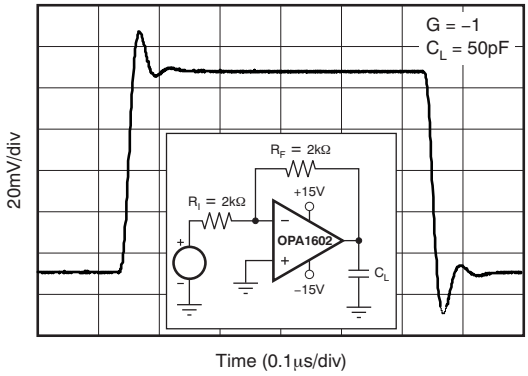


Figure 16.

LARGE-SIGNAL STEP RESPONSE

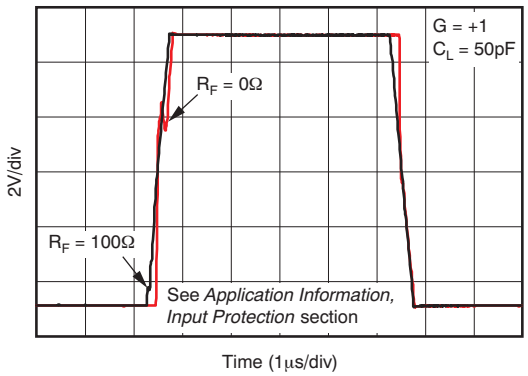


Figure 17.

LARGE-SIGNAL STEP RESPONSE

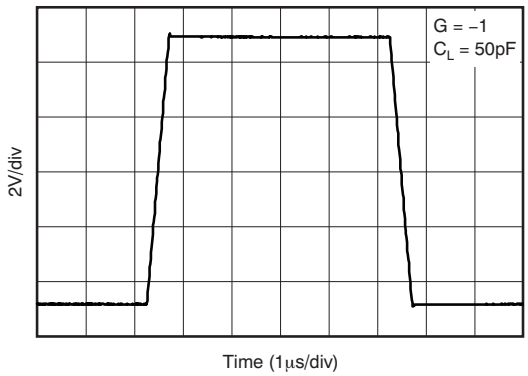


Figure 18.

TYPICAL CHARACTERISTICS (continued)

At T_A = +25°C, V_S = ±15V, and R_L = 2kΩ, unless otherwise noted.

SMALL-SIGNAL OVERSHOOT vs CAPACITIVE LOAD (100mV Output Step)

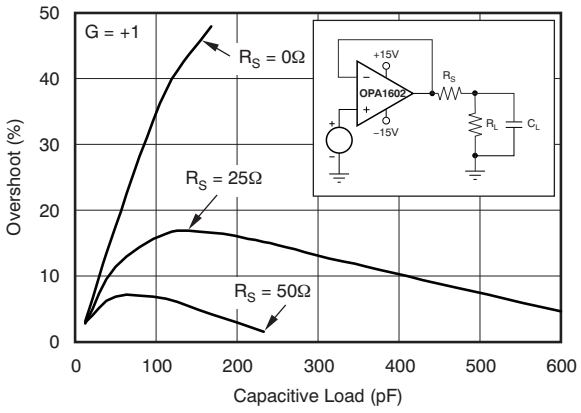


Figure 19.

SMALL-SIGNAL OVERSHOOT vs CAPACITIVE LOAD (100mV Output Step)

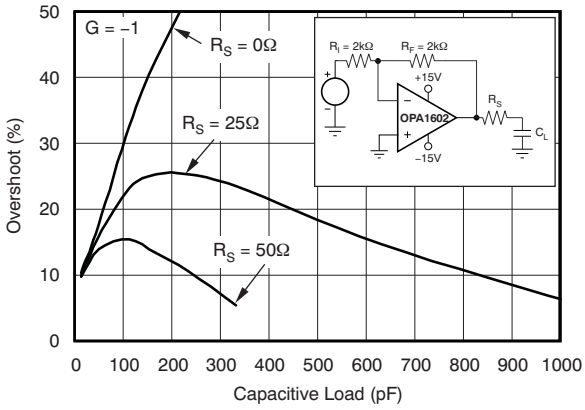


Figure 20.

SMALL-SIGNAL OVERSHOOT vs FEEDBACK CAPACITOR (100mV Output Step)

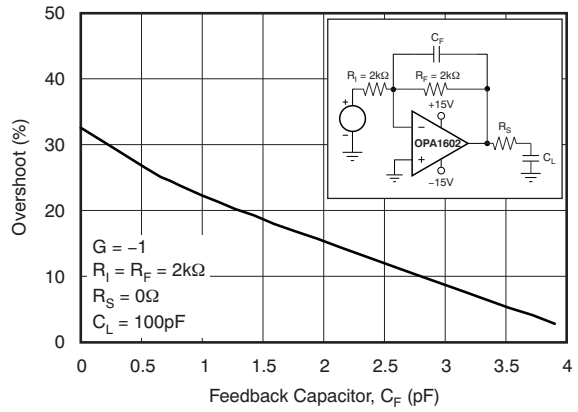


Figure 21.

OPEN-LOOP GAIN vs TEMPERATURE

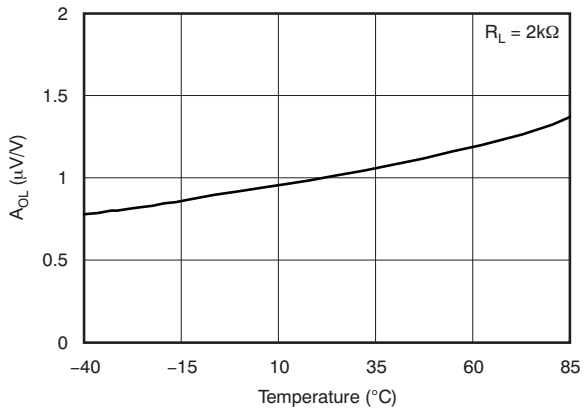


Figure 22.

I_B AND I_{OS} vs TEMPERATURE

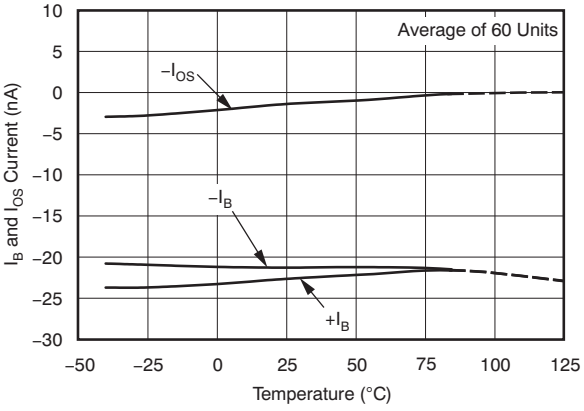


Figure 23.

I_B AND I_{OS} vs COMMON-MODE VOLTAGE

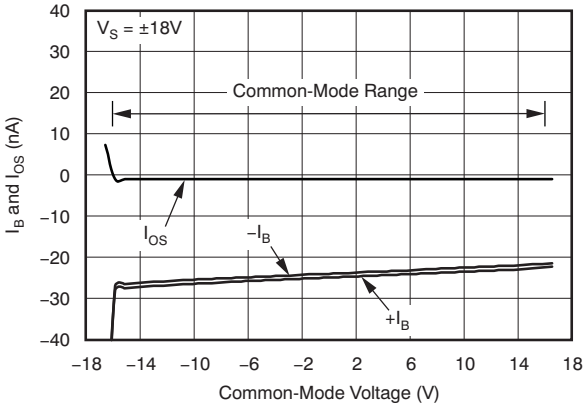


Figure 24.

TYPICAL CHARACTERISTICS (continued)

At T_A = +25°C, V_S = ±15V, and R_L = 2kΩ, unless otherwise noted.

QUIESCENT CURRENT vs TEMPERATURE

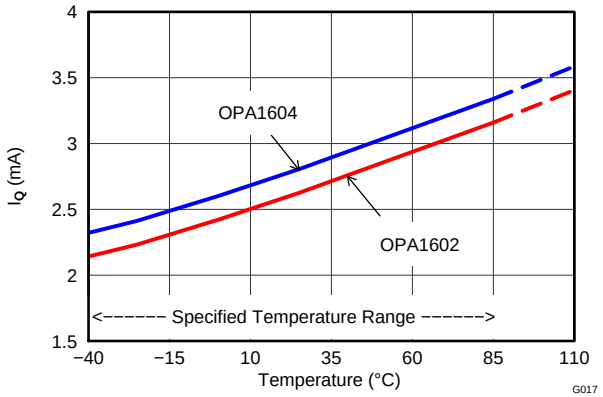


Figure 25.

QUIESCENT CURRENT vs SUPPLY VOLTAGE

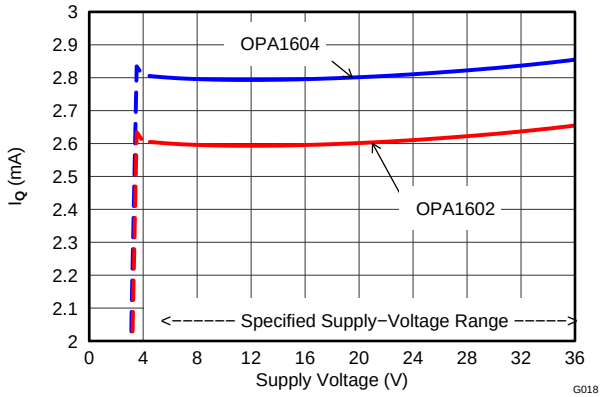


Figure 26.

I_Q WARMUP
(Difference from I_Q at Startup, Per Channel)

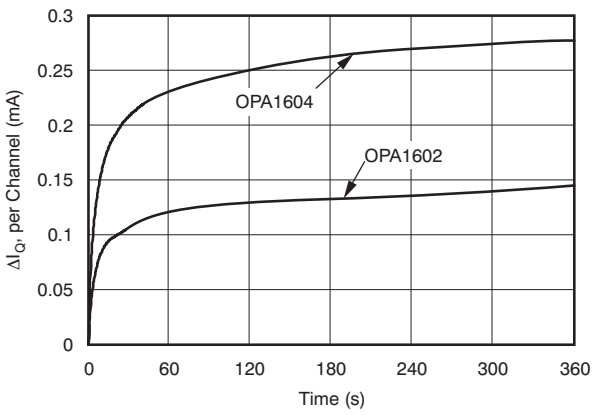


Figure 27.

SHORT-CIRCUIT CURRENT vs TEMPERATURE

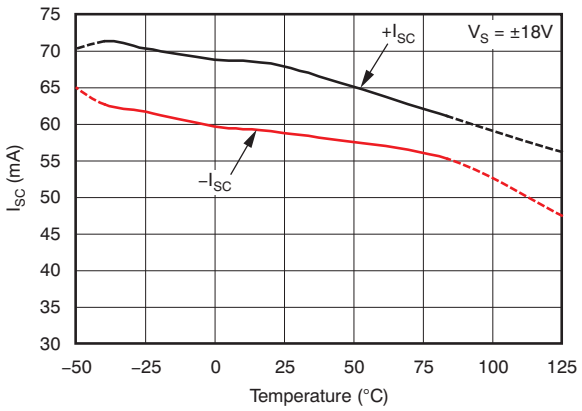


Figure 28.

OUTPUT VOLTAGE vs OUTPUT CURRENT

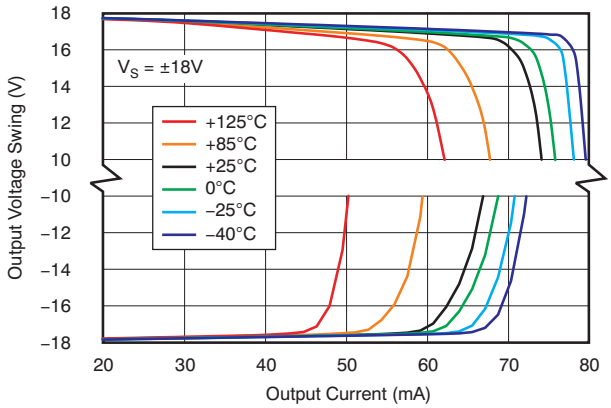


Figure 29.

OPEN-LOOP OUTPUT IMPEDANCE vs FREQUENCY

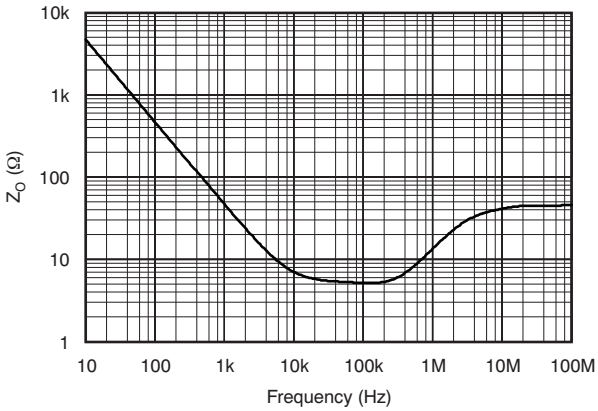


Figure 30.

APPLICATION INFORMATION

The OPA1602 and OPA1604 are unity-gain stable, precision dual and quad op amps with very low noise. Applications with noisy or high-impedance power supplies require decoupling capacitors close to the device pins. In most cases, 0.1µF capacitors are adequate. Figure 31 shows a simplified schematic of the OPA160x (one channel shown).

OPERATING VOLTAGE

The OPA160x series op amps operate from ±2.25V to ±18V supplies while maintaining excellent performance. The OPA160x series can operate with as little as +4.5V between the supplies and with up to +36V between the supplies. However, some applications do not require equal positive and negative output voltage swing. With the OPA160x series, power-supply voltages do not need to be equal. For example, the positive supply could be set to +25V with the negative supply at –5V.

In all cases, the common-mode voltage must be maintained within the specified range. In addition, key parameters are assured over the specified temperature range of T_A = –40°C to +85°C. Parameters that vary significantly with operating voltage or temperature are shown in the Typical Characteristics.

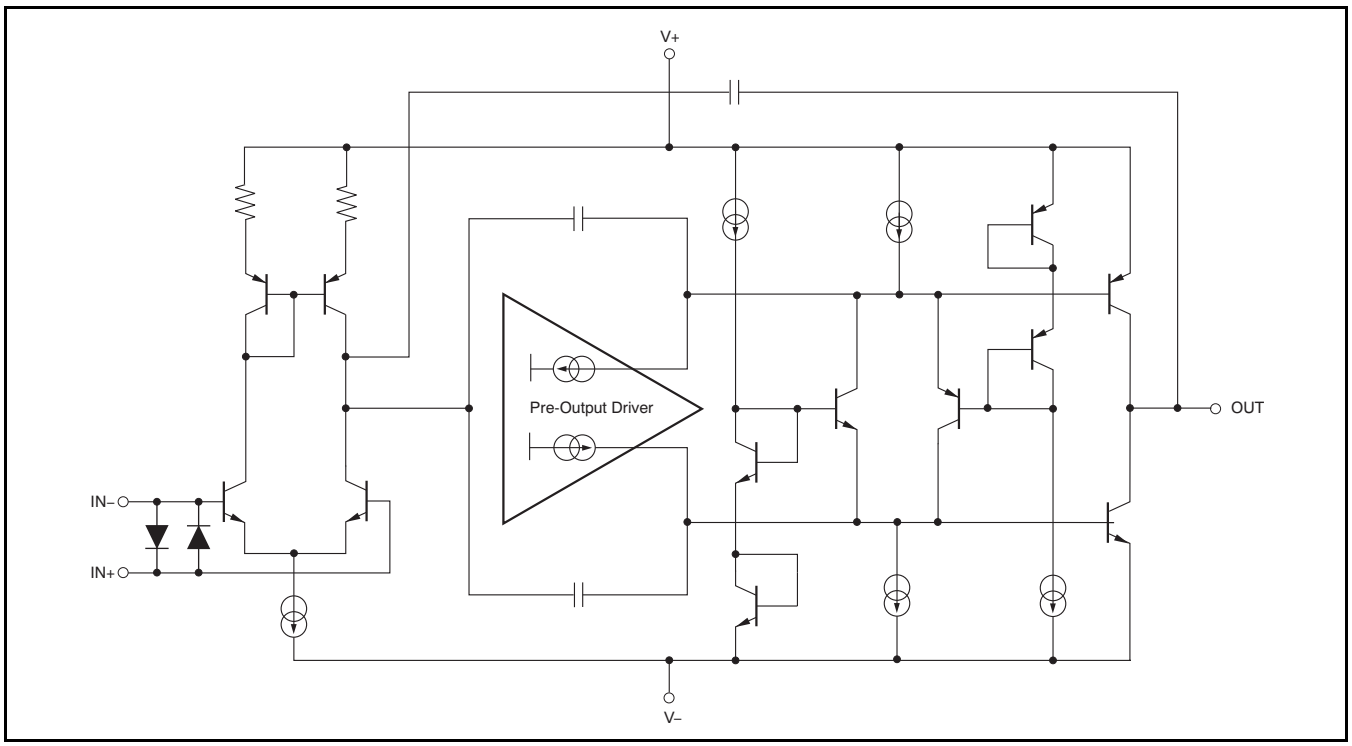


Figure 31. OPA160x Simplified Schematic

INPUT PROTECTION

The input terminals of the OPA1602 and OPA1604 are protected from excessive differential voltage with back-to-back diodes, as Figure 32 illustrates. In most circuit applications, the input protection circuitry has no consequence. However, in low-gain or G = +1 circuits, fast ramping input signals can forward bias these diodes because the output of the amplifier cannot respond rapidly enough to the input ramp. This effect is illustrated in Figure 17 of the Typical Characteristics. If the input signal is fast enough to create this forward bias condition, the input signal current must be limited to 10mA or less. If the input signal current is not inherently limited, an input series resistor (R_I) and/or a feedback resistor (R_F) can be used to limit the signal input current. This resistor degrades the low-noise performance of the OPA160x and is examined in the following *Noise Performance* section. Figure 32 shows an example configuration when both current-limiting input and feeback resistors are used.

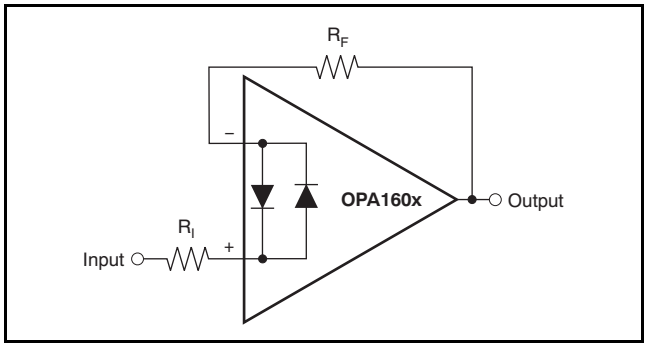


Figure 32. Pulsed Operation

NOISE PERFORMANCE

Figure 33 shows the total circuit noise for varying source impedances with the op amp in a unity-gain configuration (no feedback resistor network, and therefore no additional noise contributions).

The OPA160x (GBW = 35MHz, G = +1) is shown with total circuit noise calculated. The op amp itself contributes both a voltage noise component and a current noise component. The voltage noise is commonly modeled as a time-varying component of the offset voltage. The current noise is modeled as the time-varying component of the input bias current and reacts with the source resistance to create a voltage component of noise. Therefore, the lowest noise op amp for a given application depends on the source impedance. For low source impedance, current noise is negligible, and voltage noise generally dominates. The low voltage noise of the OPA160x series op amps makes them a better choice for low source impedances of less than 1kΩ.

The equation in Figure 33 shows the calculation of the total circuit noise, with these parameters:

- e_n = Voltage noise
- i_n = Current noise
- R_S = Source impedance
- k = Boltzmann's constant = 1.38×10^{-23} J/K
- T = Temperature in degrees Kelvin (K)

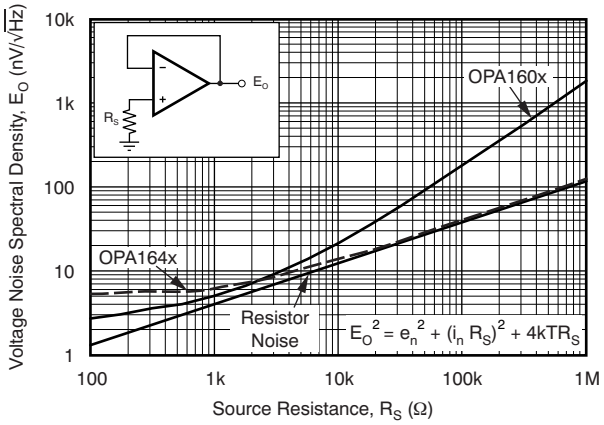


Figure 33. Noise Performance of the OPA160x in Unity-Gain Buffer Configuration

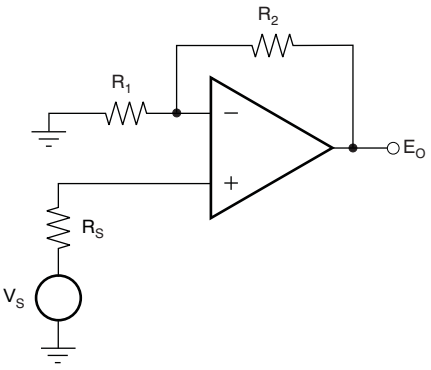
BASIC NOISE CALCULATIONS

Design of low-noise op amp circuits requires careful consideration of a variety of possible noise contributors: noise from the signal source, noise generated in the op amp, and noise from the feedback network resistors. The total noise of the circuit is the root-sum-square combination of all noise components.

The resistive portion of the source impedance produces thermal noise proportional to the square root of the resistance. Figure 33 plots this equation. The source impedance is usually fixed; consequently, select the op amp and the feedback resistors to minimize the respective contributions to the total noise.

Figure 34 illustrates both inverting and noninverting op amp circuit configurations with gain. In circuit configurations with gain, the feedback network resistors also contribute noise. The current noise of the op amp reacts with the feedback resistors to create additional noise components. The feedback resistor values can generally be chosen to make these noise sources negligible. The equations for total noise are shown for both configurations.

A) Noise in Noninverting Gain Configuration



Noise at the output:

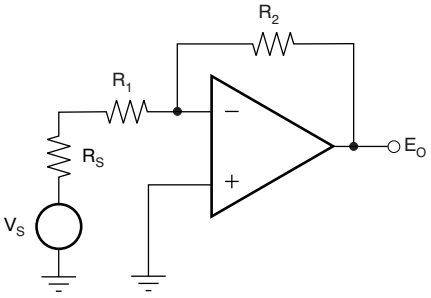
$$E_O^2 = \left(1 + \frac{R_2}{R_1}\right)^2 e_n^2 + \left(\frac{R_2}{R_1}\right)^2 e_1^2 + e_2^2 + \left(1 + \frac{R_2}{R_1}\right)^2 e_s^2$$

Where $e_S = \sqrt{4kTR_S}$ = thermal noise of R_S

$e_1 = \sqrt{4kTR_1}$ = thermal noise of R_1

$e_2 = \sqrt{4kTR_2}$ = thermal noise of R_2

B) Noise in Inverting Gain Configuration



Noise at the output:

$$E_O^2 = \left(1 + \frac{R_2}{R_1 + R_S}\right)^2 e_n^2 + \left(\frac{R_2}{R_1 + R_S}\right)^2 e_1^2 + e_2^2 + \left(\frac{R_2}{R_1 + R_S}\right)^2 e_s^2$$

Where $e_S = \sqrt{4kTR_S}$ = thermal noise of R_S

$e_1 = \sqrt{4kTR_1}$ = thermal noise of R_1

$e_2 = \sqrt{4kTR_2}$ = thermal noise of R_2

Note: For the OPA160x series of op amps at 1kHz, $e_n = 2.5nV/\sqrt{Hz}$ and $i_n = 1.8pA\sqrt{Hz}$.

Figure 34. Noise Calculation in Gain Configurations

TOTAL HARMONIC DISTORTION MEASUREMENTS

The OPA160x series op amps have excellent distortion characteristics. THD + noise is below 0.00008% (G = +1, V_O = 3V_{RMS}, BW = 80kHz) throughout the audio frequency range, 20Hz to 20kHz, with a 2kΩ load (see Figure 7 for characteristic performance).

The distortion produced by the OPA160x series op amps is below the measurement limit of many commercially available distortion analyzers. However, a special test circuit (such as Figure 35 shows) can be used to extend the measurement capabilities.

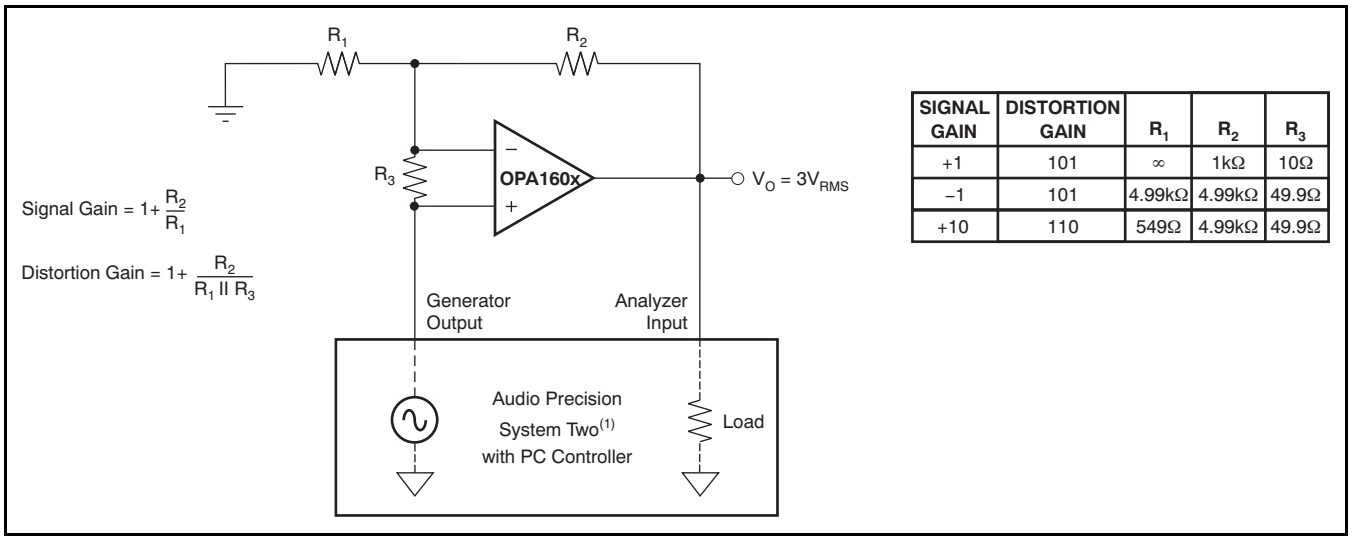
Op amp distortion can be considered an internal error source that can be referred to the input. Figure 35 shows a circuit that causes the op amp distortion to be gained up (refer to the table in Figure 35 for the distortion gain factor for various signal gains). The addition of R_3 to the otherwise standard noninverting amplifier configuration alters the feedback factor or noise gain of the circuit. The closed-loop gain is unchanged, but the feedback available for error correction is reduced by the distortion gain factor, thus extending the resolution by the same amount. Note that the input signal and load applied to the op amp are the same as with conventional feedback without R_3. The value of R_3 should be kept small to minimize its effect on the distortion measurements.

The validity of this technique can be verified by duplicating measurements at high gain and/or high frequency where the distortion is within the measurement capability of the test equipment. Measurements for this data sheet were made with an Audio Precision System Two distortion/noise analyzer, which greatly simplifies such repetitive measurements. The measurement technique can, however, be performed with manual distortion measurement instruments.

CAPACITIVE LOADS

The dynamic characteristics of the OPA1602 and OPA1604 have been optimized for commonly encountered gains, loads, and operating conditions. The combination of low closed-loop gain and high capacitive loads decreases the phase margin of the amplifier and can lead to gain peaking or oscillations. As a result, heavier capacitive loads must be isolated from the output. The simplest way to achieve this isolation is to add a small resistor (R_S equal to 50Ω, for example) in series with the output.

This small series resistor also prevents excess power dissipation if the output of the device becomes shorted. Figure 19 illustrates a graph of *Small-Signal Overshoot vs Capacitive Load* for several values of R_S. Also, refer to Applications Bulletin AB-028 (literature number SBOA015, available for download from the TI web site) for details of analysis techniques and application circuits.



SIGNAL GAIN	DISTORTION GAIN	R_1	R_2	R_3
+1	101	∞	1kΩ	10Ω
–1	101	4.99kΩ	4.99kΩ	49.9Ω
+10	110	549Ω	4.99kΩ	49.9Ω

(1) For measurement bandwidth, see Figure 7 through Figure 12.

Figure 35. Distortion Test Circuit

POWER DISSIPATION

The OPA1602 and OPA1604 series op amps are capable of driving 2kΩ loads with a power-supply voltage up to ±18V and full operating temperature range. Internal power dissipation increases when operating at high supply voltages. Copper leadframe construction used in the OPA160x series op amps improves heat dissipation compared to conventional materials. Circuit board layout can also help minimize junction temperature rise. Wide copper traces help dissipate the heat by acting as an additional heat sink. Temperature rise can be further minimized by soldering the devices to the circuit board rather than using a socket.

ELECTRICAL OVERSTRESS

Designers often ask questions about the capability of an operational amplifier to withstand electrical overstress. These questions tend to focus on the device inputs, but may involve the supply voltage pins or even the output pin. Each of these different pin functions have electrical stress limits determined by the voltage breakdown characteristics of the particular semiconductor fabrication process and specific circuits connected to the pin. Additionally, internal electrostatic discharge (ESD) protection is built into these circuits to protect them from accidental ESD events both before and during product assembly.

It is helpful to have a good understanding of this basic ESD circuitry and its relevance to an electrical overstress event. Figure 36 illustrates the ESD circuits contained in the OPA160x (indicated by the dashed line area). The ESD protection circuitry involves several current-steering diodes connected from the input and output pins and routed back to the internal power-supply lines, where they meet at an absorption device internal to the operational amplifier. This protection circuitry is intended to remain inactive during normal circuit operation.

An ESD event produces a short duration, high-voltage pulse that is transformed into a short duration, high-current pulse as it discharges through a semiconductor device. The ESD protection circuits are designed to provide a current path around the operational amplifier core to prevent it from being damaged. The energy absorbed by the protection circuitry is then dissipated as heat.

When an ESD voltage develops across two or more of the amplifier device pins, current flows through one or more of the steering diodes. Depending on the path that the current takes, the absorption device may activate. The absorption device internal to the OPA160x triggers when a fast ESD voltage pulse is impressed across the supply pins. Once triggered, it quickly activates, clamping the ESD pulse to a safe voltage level.

When the operational amplifier connects into a circuit such as that illustrated in Figure 36, the ESD protection components are intended to remain inactive and not become involved in the application circuit operation. However, circumstances may arise where an applied voltage exceeds the operating voltage range of a given pin. Should this condition occur, there is a risk that some of the internal ESD protection circuits may be biased on, and conduct current. Any such current flow occurs through steering diode paths and rarely involves the absorption device.

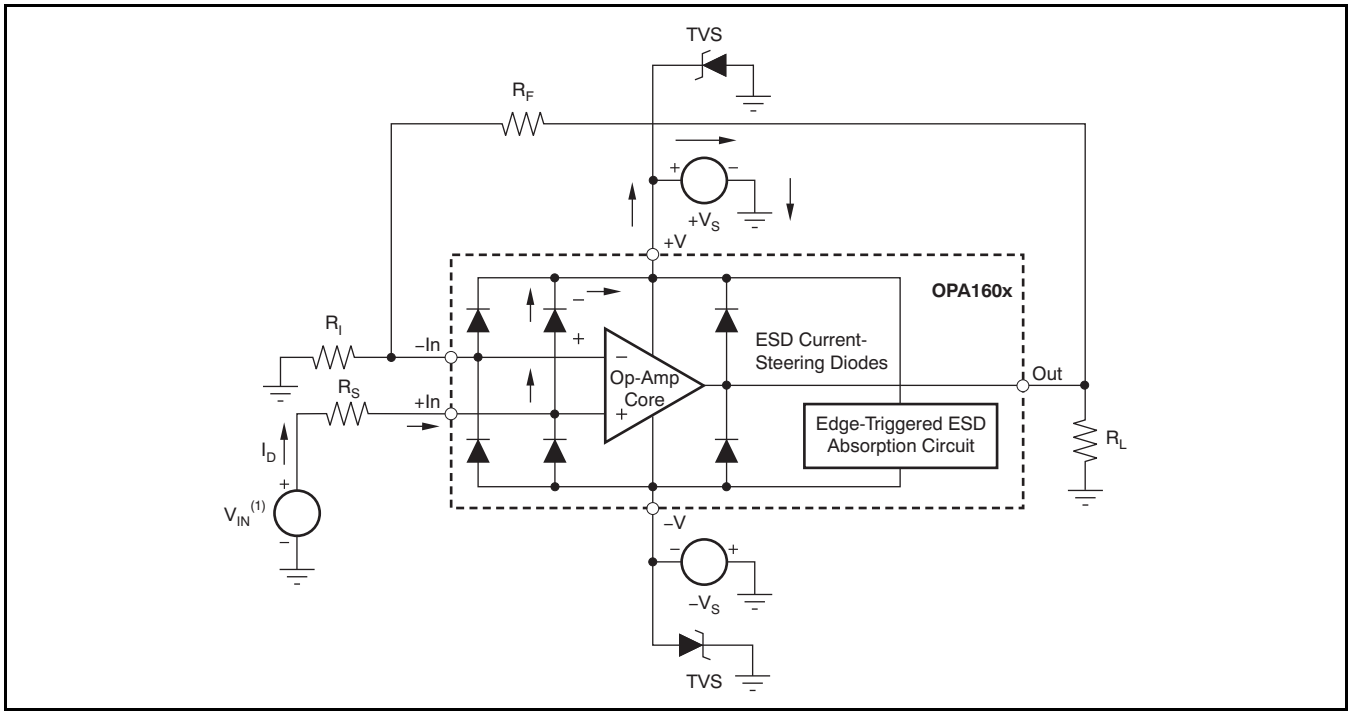
Figure 36 depicts a specific example where the input voltage, V_{IN}, exceeds the positive supply voltage ($+V_S$) by 500mV or more. Much of what happens in the circuit depends on the supply characteristics. If $+V_S$ can sink the current, one of the upper input steering diodes conducts and directs current to $+V_S$. Excessively high current levels can flow with increasingly higher V_{IN}. As a result, the datasheet specifications recommend that applications limit the input current to 10mA.

If the supply is not capable of sinking the current, V_{IN} may begin sourcing current to the operational amplifier, and then take over as the source of positive supply voltage. The danger in this case is that the voltage can rise to levels that exceed the operational amplifier absolute maximum ratings. In extreme but rare cases, the absorption device triggers on while $+V_S$ and $–V_S$ are applied. If this event happens, a direct current path is established between the $+V_S$ and $–V_S$ supplies. The power dissipation of the absorption device is quickly exceeded, and the extreme internal heating destroys the operational amplifier.

Another common question involves what happens to the amplifier if an input signal is applied to the input while the power supplies $+V_S$ and/or $–V_S$ are at 0V. Again, it depends on the supply characteristic while at 0V, or at a level below the input signal amplitude. If the supplies appear as high impedance, then the operational amplifier supply current may be supplied by the input source via the current steering diodes. This state is not a normal bias condition; the amplifier most likely will not operate normally. If the supplies are low impedance, then the current through the steering diodes can become quite high. The current level depends on the ability of the input source to deliver current, and any resistance in the input path.

If there is an uncertainty about the ability of the supply to absorb this current, external zener diodes may be added to the supply pins as shown in Figure 36.

The zener voltage must be selected such that the diode does not turn on during normal operation. However, its zener voltage should be low enough so that the zener diode conducts if the supply pin begins to rise above the safe operating supply voltage level.



(1) $V_{IN} = +V_S + 500mV$.

Figure 36. Equivalent Internal ESD Circuitry and Its Relation to a Typical Circuit Application (Single Channel Shown)

APPLICATION CIRCUIT

An additional application idea is shown in Figure 37.

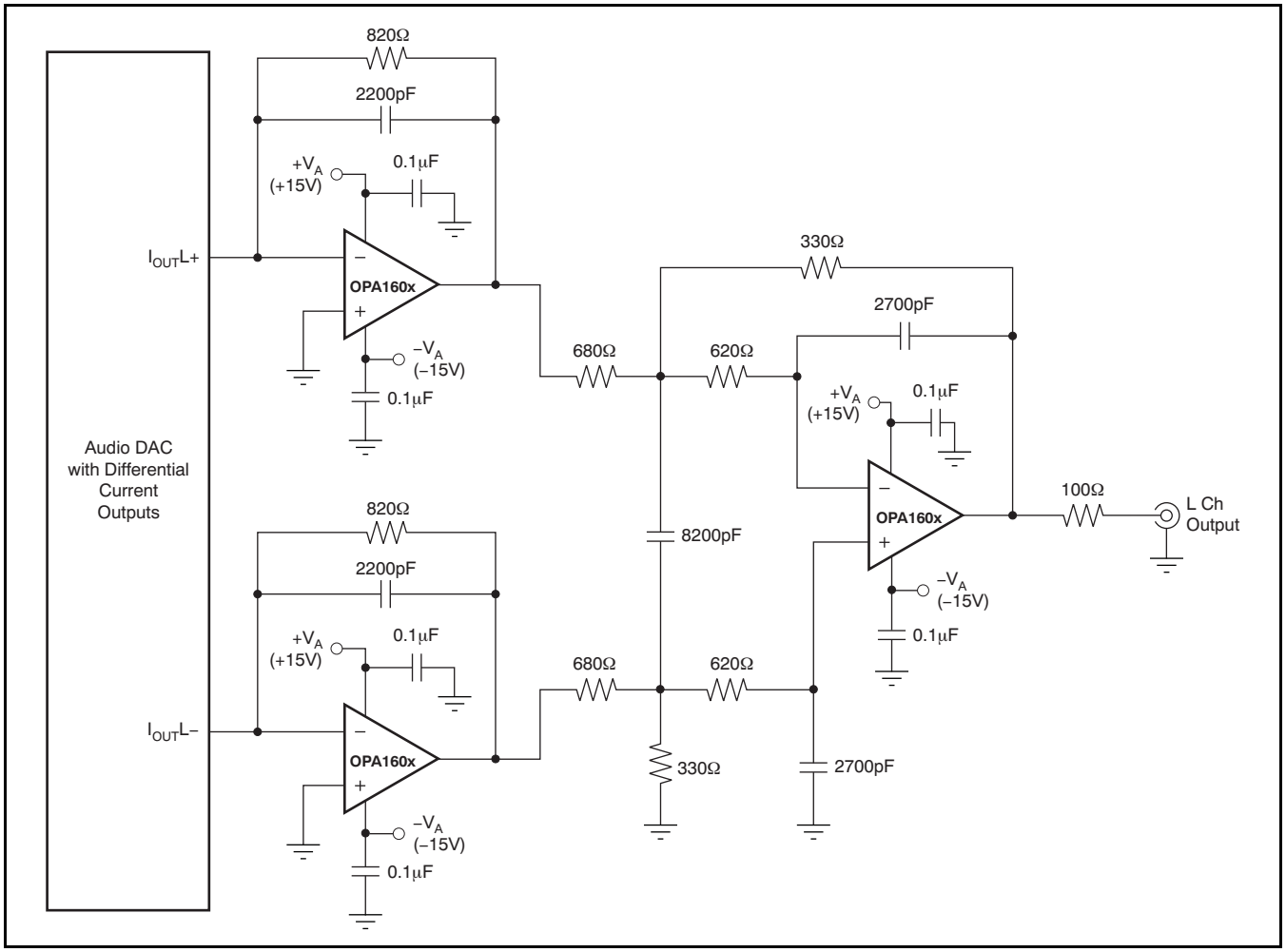


Figure 37. Audio DAC I/V Converter and Output Filter

REVISION HISTORY

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (April, 2011) to Revision B **Page**

- Revised minimum and typical *Common-mode rejection ratio* specifications 3
- Added footnote (2) to *Electrical Characteristics* table 3
- Added separate quiescent current specifications for dual and quad versions 4
- Added footnote (3) to *Electrical Characteristics* table 4
- Corrected product identification and values in OPA1602 *Thermal Information* table 4
- Added values to OPA1604 *Thermal Information* table. 4
- Updated device name in Figure 3 5
- Updated Figure 25 to show both devices 9
- Updated Figure 26 to show both devices 9
- Updated device name in Figure 33 11
- Changed *Power Dissipation* section 14

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
OPA1602AID	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	01602A	Samples
OPA1602AIDGK	ACTIVE	VSSOP	DGK	8	80	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	OCKQ	Samples
OPA1602AIDGKR	ACTIVE	VSSOP	DGK	8	2500	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	OCKQ	Samples
OPA1602AIDR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	01602A	Samples
OPA1604AID	ACTIVE	SOIC	D	14	50	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	01604A	Samples
OPA1604AIDR	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	01604A	Samples
OPA1604AIPW	ACTIVE	TSSOP	PW	14	90	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	OPA1604	Samples
OPA1604AIPWR	ACTIVE	TSSOP	PW	14	2000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	OPA1604	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

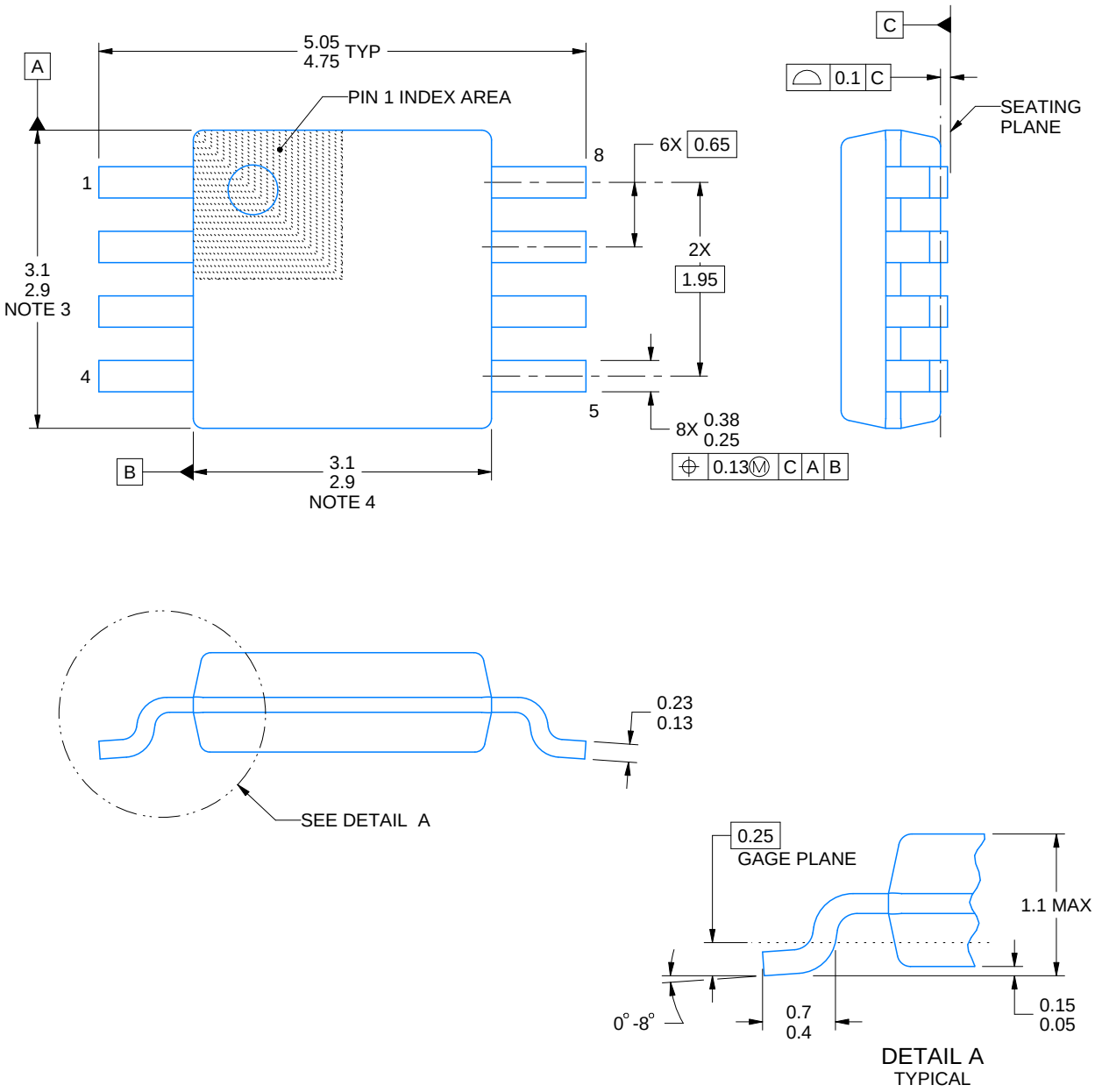
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

PACKAGE OUTLINE

DGK0008A

VSSOP - 1.1 mm max height

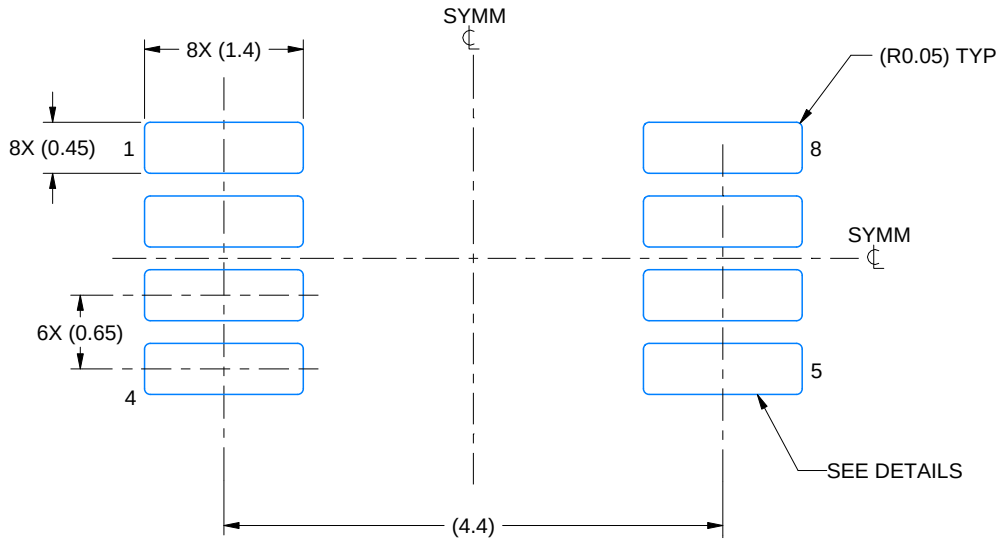
SMALL OUTLINE PACKAGE



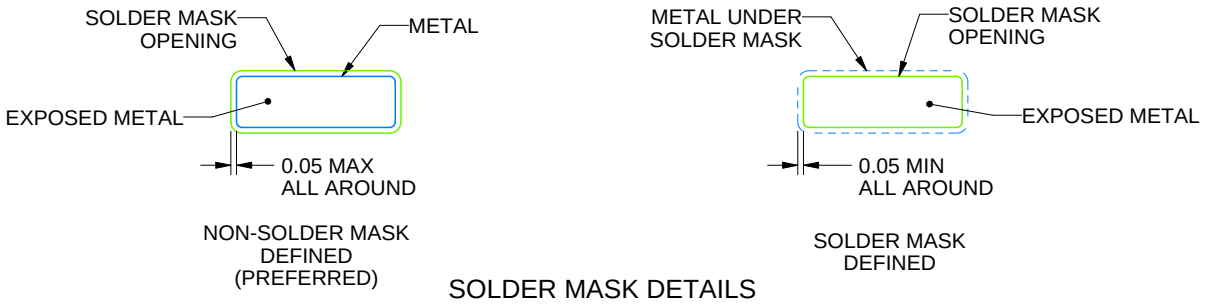
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X

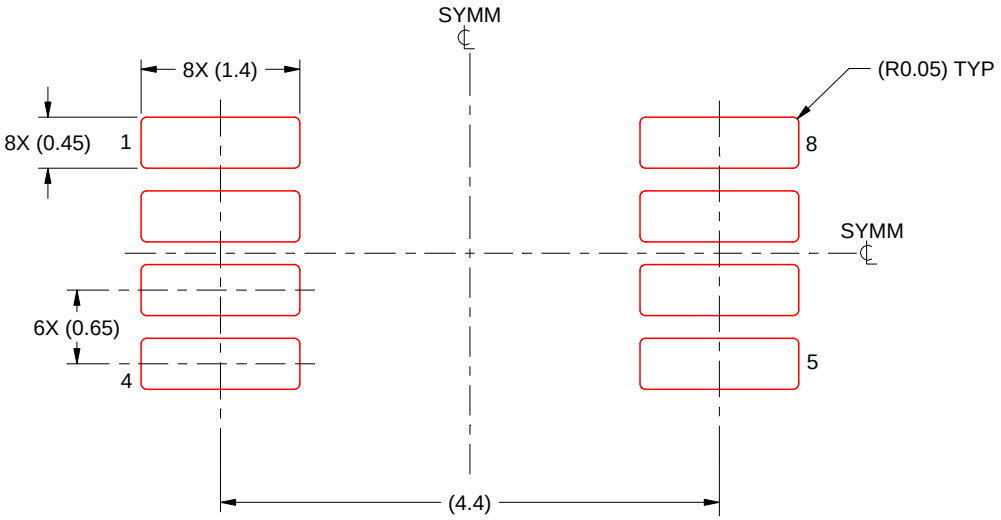


SOLDER MASK DETAILS

4214862/A 04/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.

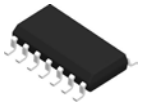


SOLDER PASTE EXAMPLE
SCALE: 15X

4214862/A 04/2023

NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

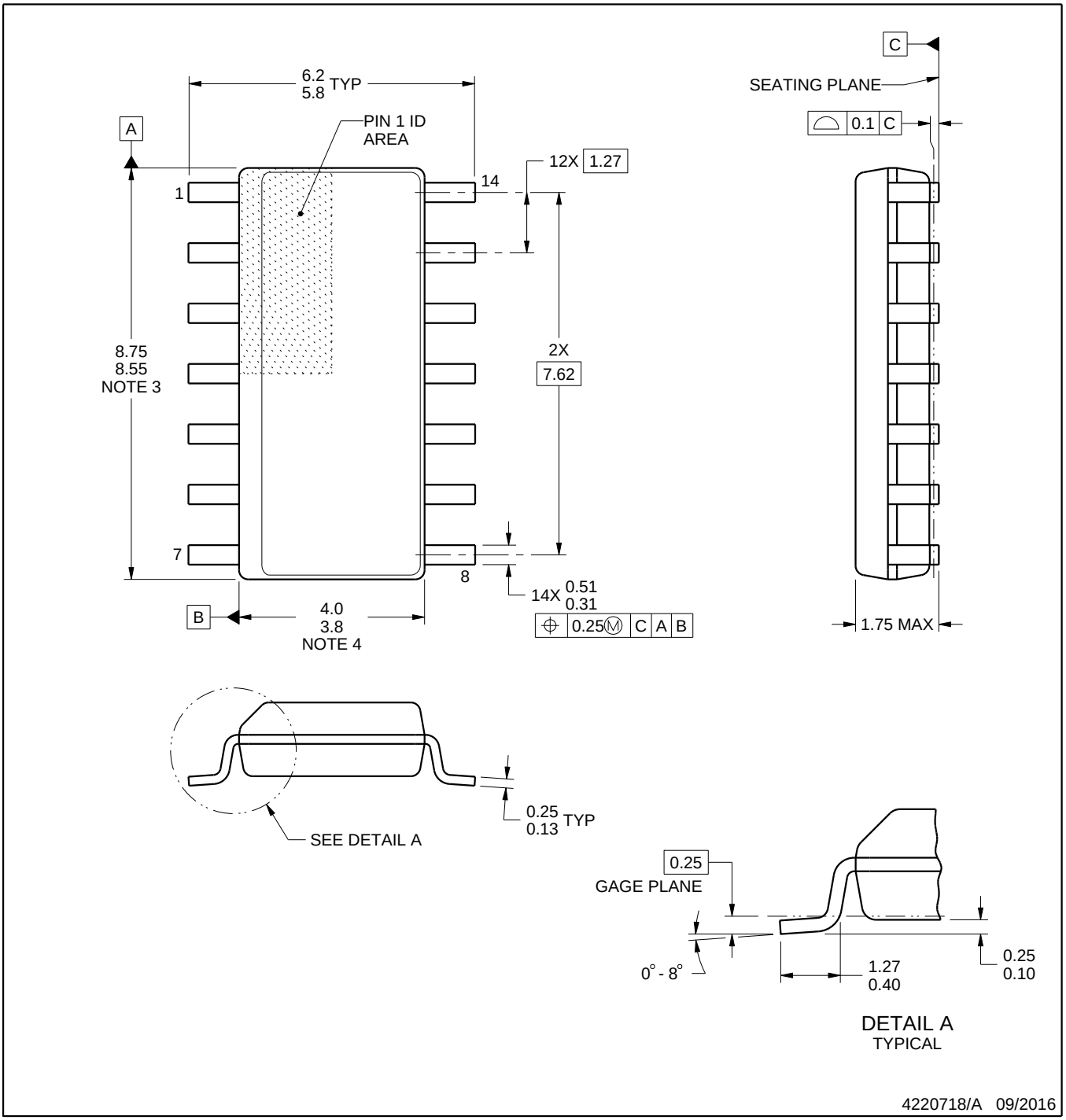


PACKAGE OUTLINE

D0014A

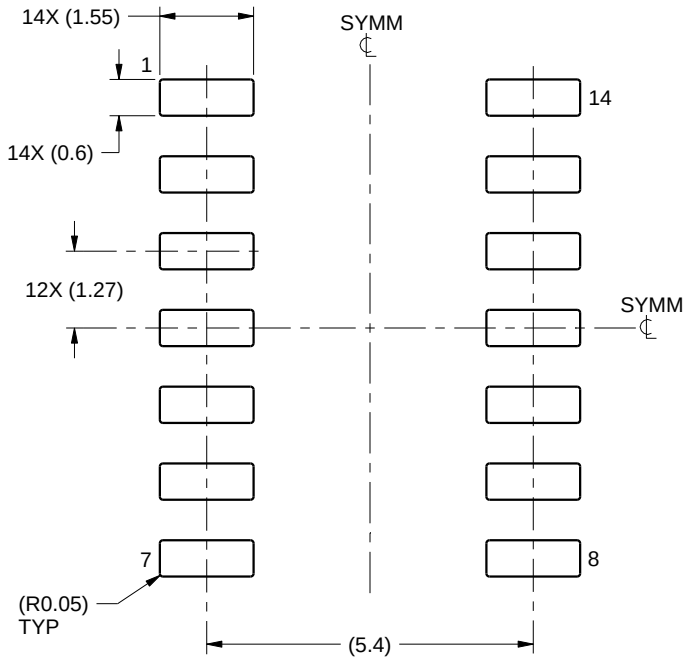
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

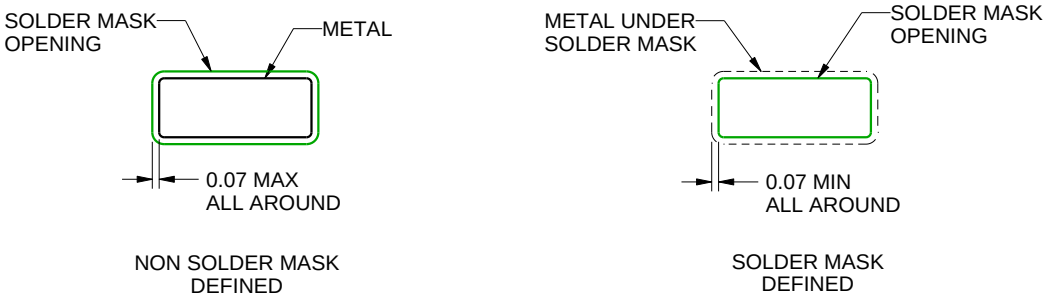


NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm, per side.
5. Reference JEDEC registration MS-012, variation AB.



LAND PATTERN EXAMPLE
SCALE:8X



SOLDER MASK DETAILS

4220718/A 09/2016

NOTES: (continued)

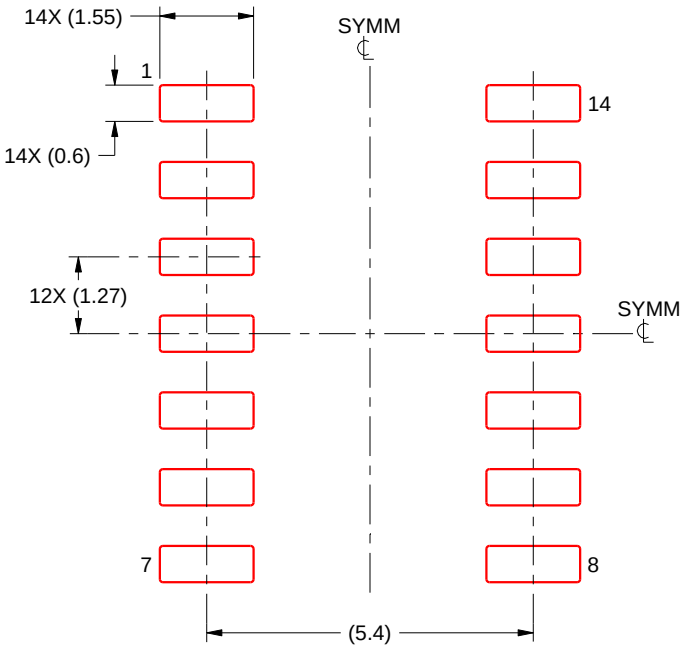
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

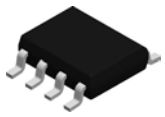


SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:8X

4220718/A 09/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

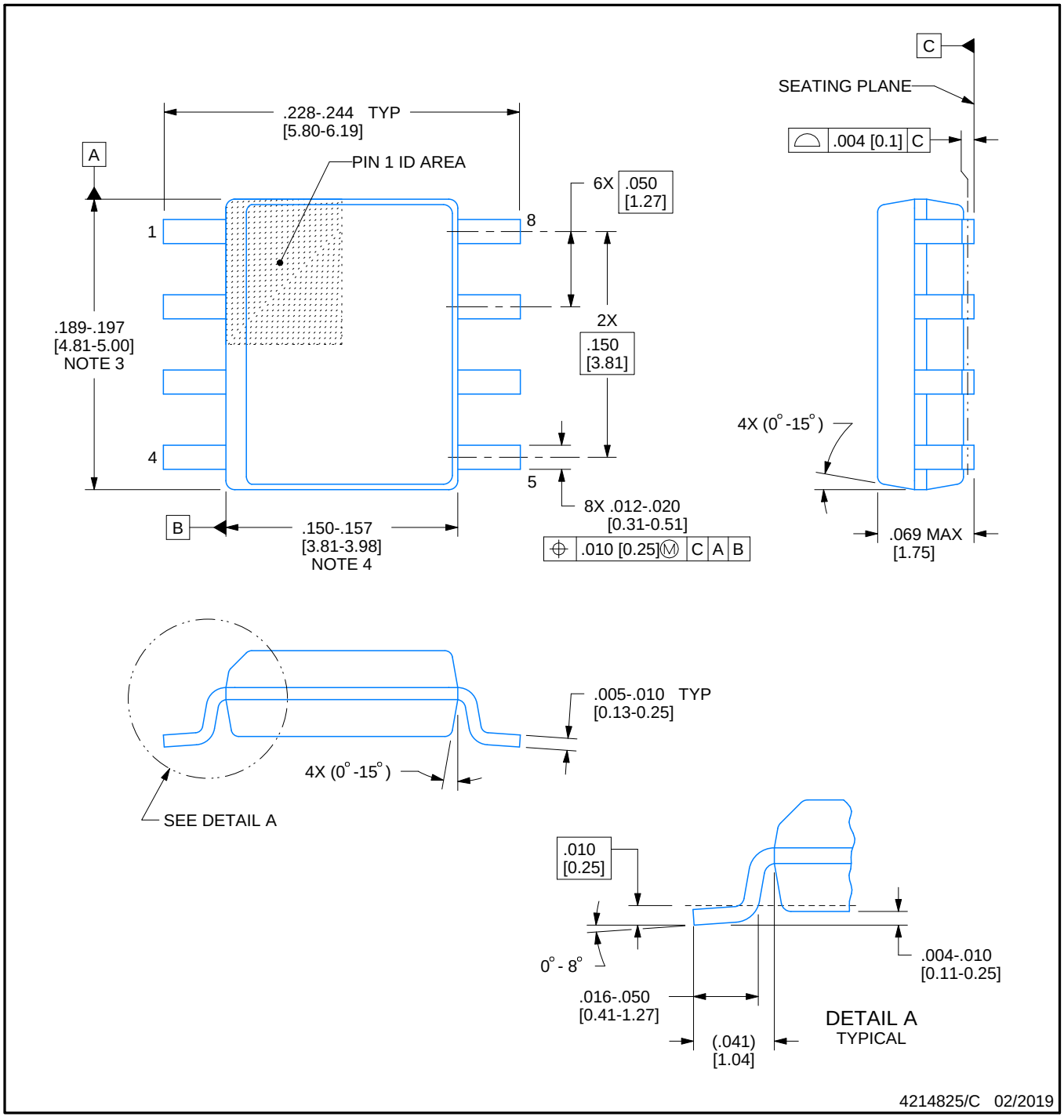


PACKAGE OUTLINE

D0008A

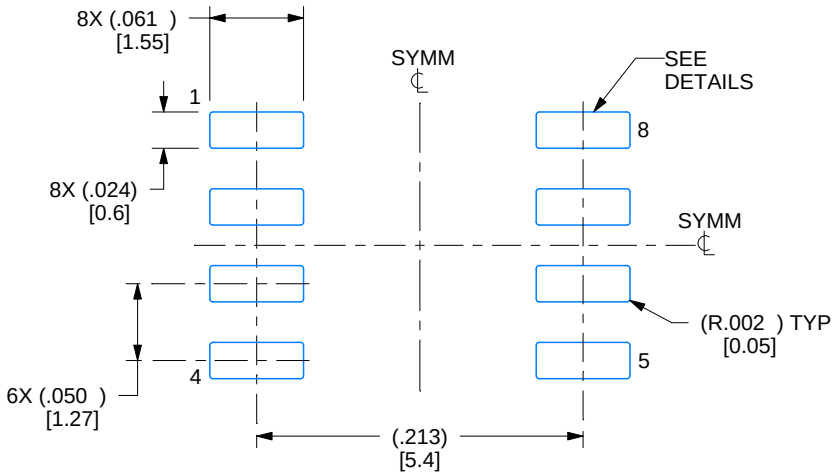
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

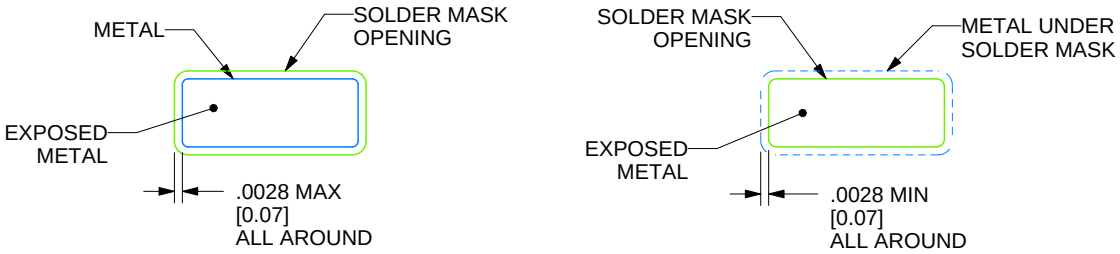


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

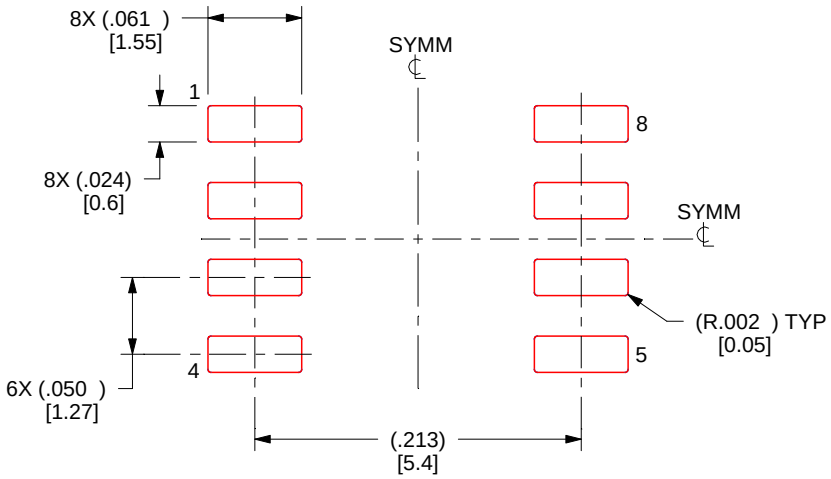
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

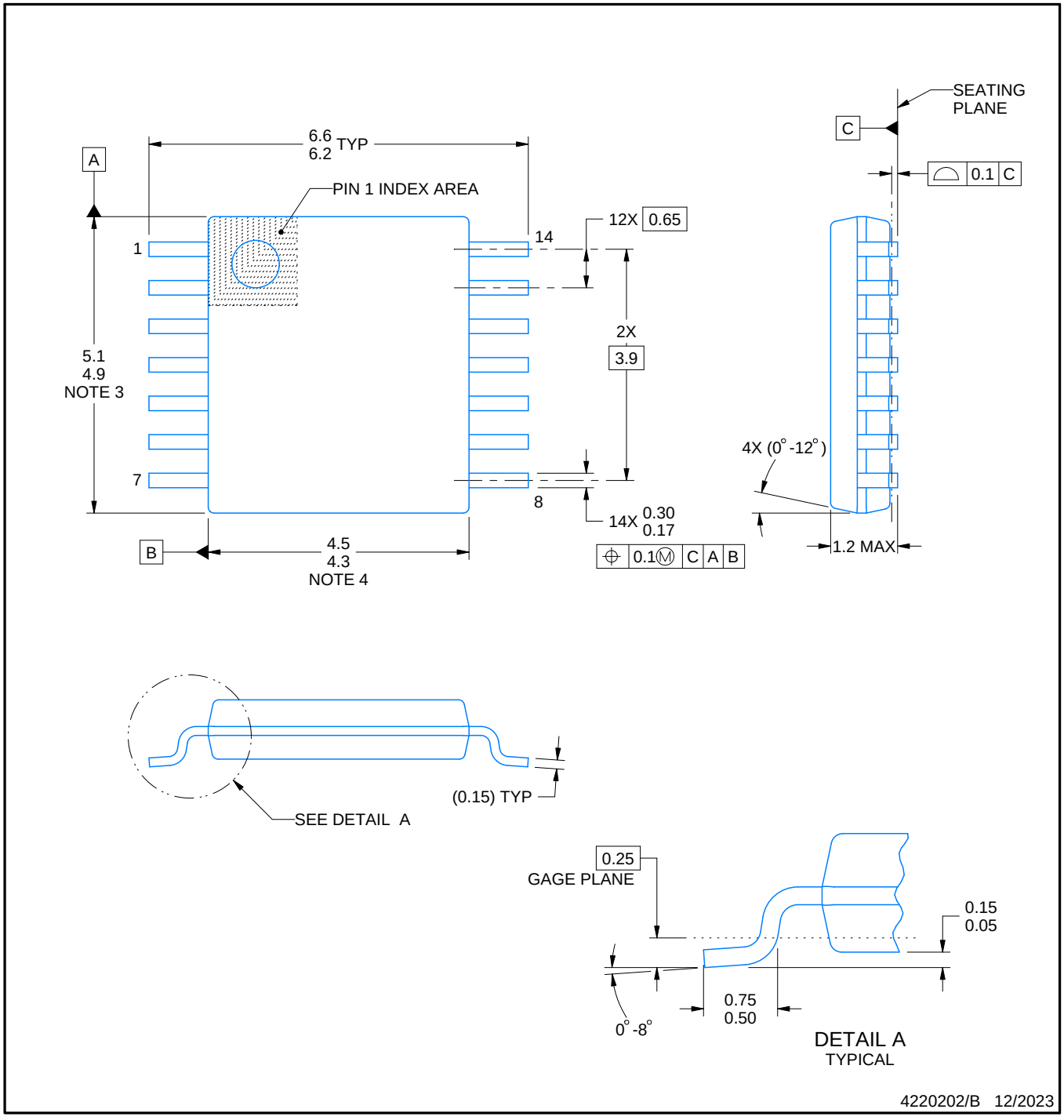
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

PW0014A

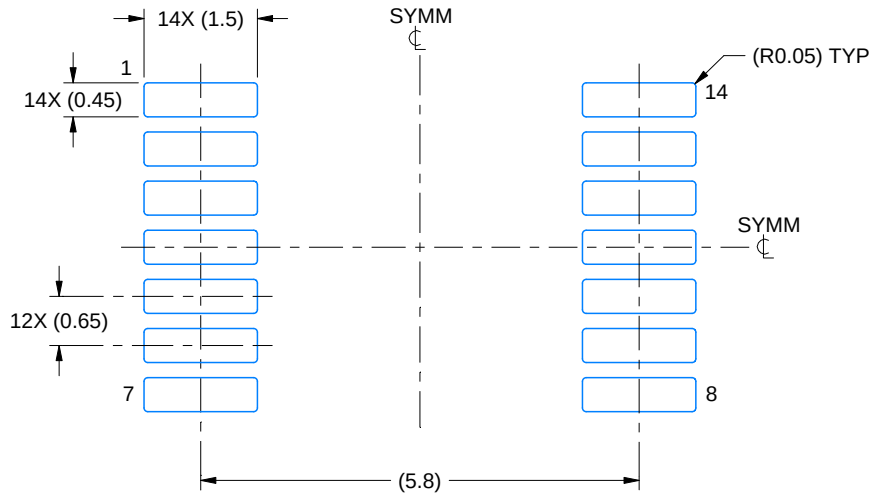
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

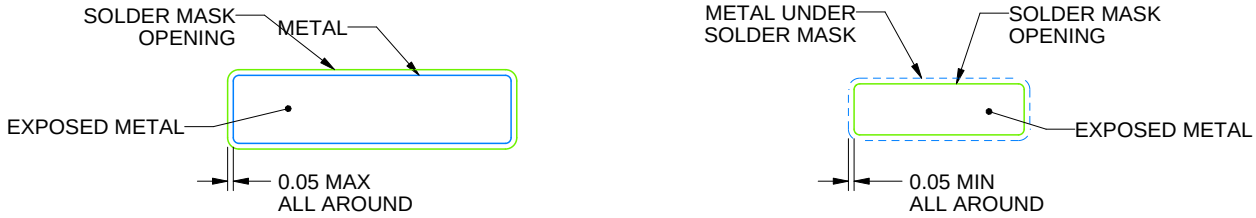


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

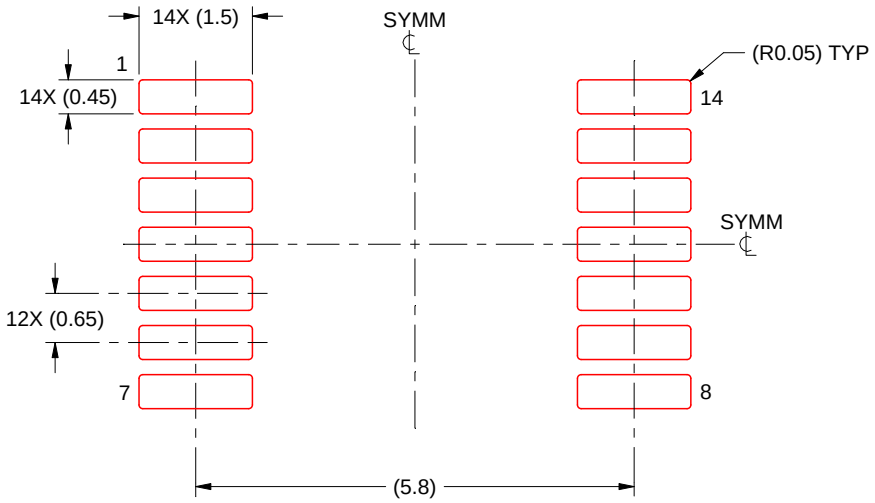


SOLDER MASK DETAILS

4220202/B 12/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220202/B 12/2023

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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