OPA2156 36V 超低噪声、高带宽、CMOS、精密轨至轨运算放大器

1 特性

- 超低噪声：10kHz 时为 3nV/√Hz
- 低失调电压：±25µV
- 低失调电压温漂：±0.5µV/°C
- 低偏置电流：±5pA
- 共模抑制：120dB
- 低噪声：10kHz 时为 3nV/√Hz
- 高带宽：25MHz GBW
- 开环电压增益：154dB
- 高输出电流：100mA
- 轨至轨输入和输出
- 高压摆率：40V/µs
- 较短的建立时间：600ns（10V 阶跃，0.01%）
- 宽电源电压范围：±2.25V 至 ±18V，4.5V 至 36V
- 行业标准封装：
  - SOIC-8 和 VSSOP-8 双列封装

2 应用

- 数据采集 (DAQ)
- 光电二极管跨阻放大器
- 振动监控器模块
- 模拟输入模块
- 高分辨率 ADC 驱动器放大器
- 医疗设备

3 说明

OPA2156 是计划推出的新一代 36V 轨至轨运算放大器中的第一款。

这款器件具有非常低的失调电压 (±25µV)、漂移 (±0.5µV/°C) 和低偏置电流 (±5pA)，同时还具有非常低的宽带电压噪声 (3nV/√Hz)。

OPA2156 拥有 独特特性，例如轨至轨输入和输出电压范围、宽带宽 (25MHz)、高输出电流 (100mA) 和高压摆率 (40V/µs)，是一款功能强大、性能出色的运算放大器，适用于高压精密工业 应用中节省电路板空间。

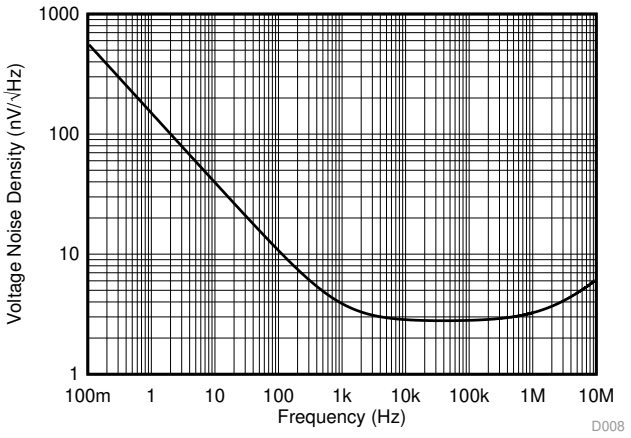
OPA2156 运算放大器可提供 8 引脚 SOIC 和 VSSOP 封装，可在 –40°C 至 +125°C 的工业温度范围内正常工作。

器件信息(1)

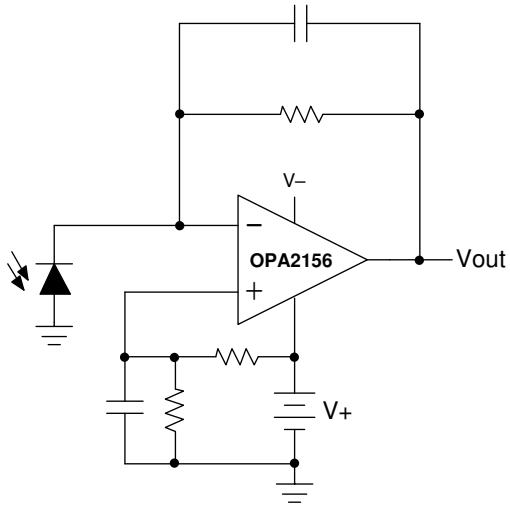
器件型号	封装	封装尺寸（标称值）
OPA2156	SOIC (8)	4.90mm × 3.90mm
	VSSOP (8)	3.00mm × 3.00mm

(1) 如需了解所有可用封装，请参阅数据表末尾的封装选项附录。

低输入电压噪声频谱密度



OPA2156 跨阻配置



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4 修订历史记录

注：之前版本的页码可能与当前版本有所不同。

Changes from Revision A (December 2018) to Revision B **Page**

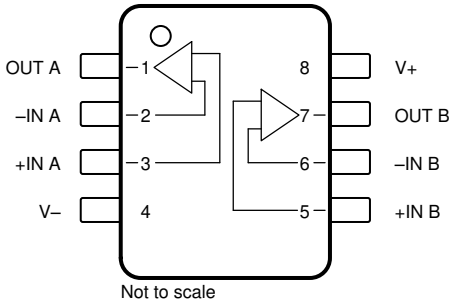
- 已添加 向数据表中添加了新的 DGK (VSSOP) 封装和相关内容 ... 1
- 已更改 Figure 8, *Input Voltage Noise Spectral Density*, to include frequencies up to 10 MHz ... 8
- 已更改 title of input bias and offset current curves (Figures 12 to 14) to specify SOIC package performance ... 9

Changes from Original (September 2018) to Revision A **Page**

- 首次发布生产数据数据表 ... 1

5 Pin Configuration and Functions

D and DGK Packages
8-Pin SOIC and 8-Pin VSSOP
Top View



Not to scale

Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
+IN A	3	I	Noninverting input, channel A
+IN B	5	I	Noninverting input, channel B
–IN A	2	I	Inverting input, channel A
–IN B	6	I	Inverting input, channel B
OUT A	1	O	Output, channel A
OUT B	7	O	Output, channel B
V+	8	—	Positive (highest) power supply
V–	4	—	Negative (lowest) power supply

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
Supply voltage, V_S = (V+) – (V–)				±20 (+40, single supply)	V
Signal input pins	Voltage	Common-mode	(V–) – 0.5	(V+) + 0.5	V
		Differential		0.5	
	Current			±10	mA
Output short circuit(2)			Continuous		
Temperature	Operating junction		–40	150	°C
	Storage, T_{stg}		–65	150	

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. Theseare stress ratings only, which do not imply functional operation of the device at these or anyother conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extendedperiods may affect device reliability.
(2) Short-circuit to ground, one amplifier per package.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±3000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±1000	V

(1) JEDEC document JEP155 states that 500-V HBM allows safemanufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safemanufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

	MIN	NOM	MAX	UNIT
Supply voltage, V_S = (V+) – (V–)	4.5 (±2.25)		36 (±18)	V
Specified temperature (SOIC)(1)	–40		125	°C

(1) Please see Thermal Considerations section for information on ambient vs device junction temperature

6.4 Thermal Information: OPA2156

THERMAL METRIC(1)		OPA2156		UNIT
		8 PINS		
		D (SOIC)	DGK (VSSOP)	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	119.2	163.8	°C/W
$R_{\theta JC(top)}$	Junction-to-case(top) thermal resistance	51.1	52.5	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	64.7	86.5	°C/W
ψ_{JT}	Junction-to-top characterization parameter	9.7	5.1	°C/W
ψ_{JB}	Junction-to-board characterization parameter	63.5	84.7	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

6.5 Electrical Characteristics

at T_A = 25°C, V_S = ±2.25V to ±18V, V_{CM} = V_{OUT} = V_S / 2, and R_L = 2 kΩ connected to V_S / 2 (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
OFFSET VOLTAGE							
V_{OS}	Input offset voltage, PMOS				±25	±200	µV
		T_A = –40°C to +85°C				±300	µV
		T_A = –40°C to +125°C			See Typical Characteristics		
V_{OS}	Input offset voltage, NMOS	V_{CM} = (V+) – 1.25 V			±0.25	±3	mV
		V_{CM} = (V+) – 1.25 V, T_A = –40°C to +125°C (SOIC)				±5	mV
		V_{CM} = (V+) – 1.25 V, T_A = –40°C to +105°C (MSOP)					
dV_{OS}/dT	Input offset voltage drift	PMOS, SOIC	T_A = –40°C to +125°C		±0.5	±3	µV/°C
		PMOS, MSOP	T_A = –40°C to +105°C				
		NMOS, V_{CM} = (V+) – 1.25 V	T_A = –40°C to +125°C		±1		
PSRR	Power-supply rejection ratio				±0.3	±4.5	µV/V
		T_A = –40°C to +125°C (SOIC)				±5	
		T_A = –40°C to +105°C (MSOP)					
INPUT BIAS CURRENT							
I_B	Input bias current	SOIC			±5	±40	pA
		MSOP			±5	±80	pA
		T_A = –40°C to +85°C (SOIC)				±1.5	nA
		T_A = –40°C to +85°C (MSOP)				±15	nA
		T_A = –40°C to +125°C			See Typical Characteristics		nA
I_{OS}	Input offset current				±2	±40	pA
		T_A = –40°C to +85°C (SOIC)				±1.5	nA
		T_A = –40°C to +85°C (MSOP)				±2.5	nA
		T_A = –40°C to +125°C			See Typical Characteristics		nA
NOISE							
E_n	Input voltage noise	(V–) < V_{CM} < (V+) – 2.25 V	f = 0.1 Hz to 10 Hz		1.9		μV_{PP}
		(V+) – 1.25 V < V_{CM} < (V+)	f = 0.1 Hz to 10 Hz		3.4		
e_n	Input voltage noise density	(V–) < V_{CM} < (V+) – 2.25 V	f = 100 Hz		12.0		$nV/\sqrt{Hz}$
			f = 1 kHz		4		
			f = 10 kHz		3.0		
e_n	Input voltage noise density	(V+) – 1.25 V < V_{CM} < (V+)	f = 100 Hz		13.0		
			f = 1 kHz		9.7		
			f = 10 kHz		4.0		
i_n	Input current noise density	f = 1 kHz			19		$fA/\sqrt{Hz}$
INPUT VOLTAGE							
V_{CM}	Common-mode voltage range			(V–) – 0.1		(V+) + 0.1	V
CMRR	Common-mode rejection ratio, PMOS	(V–) < V_{CM} < (V+) – 2.25 V, V_S = ±18 V		106	120		dB
CMRR	Common-mode rejection ratio, PMOS	T_A = –40°C to +125°C (SOIC)		100			
CMRR	Common-mode rejection ratio, PMOS	T_A = –40°C to +105°C (MSOP)					
CMRR	Common-mode rejection ratio, NMOS	(V+) – 1.25 V < V_{CM} < (V+), V_S = ±18 V		82	120		
CMRR	Common-mode rejection ratio, NMOS	T_A = –40°C to +125°C (SOIC)		74			
CMRR	Common-mode rejection ratio, NMOS	T_A = –40°C to +105°C (MSOP)					

Electrical Characteristics (continued)

at T_A = 25°C, V_S = ±2.25V to ±18V, V_{CM} = V_{OUT} = V_S / 2, and R_L = 2 kΩ connected to V_S / 2 (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
INPUT IMPEDANCE							
Z_{ID}	Differential				100 || 9.1		MΩ || pF
Z_{IC}	Common-mode				6 || 1.9		10^{12}Ω || pF
OPEN-LOOP GAIN							
A_{OL}	Open-loop voltage gain	(V–) + 0.6 V < V_O < (V+) – 0.6 V, V_S = ±18 V (SOIC)		130	154		dB
		(V–) + 0.6 V < V_O < (V+) – 0.6 V, V_S = ±18 V (MSOP)		128	154		
		T_A = –40°C to +85°C		126			
FREQUENCY RESPONSE							
GBW	Unity gain bandwidth				20		MHz
	Gain bandwidth product	G = 100			25		MHz
SR	Slew rate	V_S = ±18 V, G = –1, 10-V step			40		V/µs
t_s	Settling time	To 0.01%, C_L = 20 pF	V_S = ±18 V, G = –1, 10-V step		600		ns
t_{OR}	Overload recovery time	G = –10			100		ns
THD+N	Total harmonic distortion + noise	G = 1, f = 1 kHz, V_O = 3.5 V_{RMS}			–132		dB
					0.000025 %		
		G = 1, f = 20 kHz, V_O = 3.5 V_{RMS}			–126		dB
					0.00005%		
	Crosstalk	dc			150		dB
		f = 100 kHz			120		dB
OUTPUT							
V_O	Voltage output swing from power supply				200	250	mV
I_{SC}	Short-circuit current	V_S = ±18 V			100		mA
C_L	Capacitive load drive				See Typical Characteristics		pF
Z_O	Open-loop output impedance	f = 1 MHz, I_O = 0 A			25		Ω
POWER SUPPLY							
I_Q	Quiescent current per amplifier	I_O = 0 A			4.4	5.2	mA
			T_A = –40°C to +125°C (SOIC)			5.2	mA
			T_A = –40°C to +105°C (MSOP)				mA
TEMPERATURE							
	Thermal protection				170		°C
	Thermal hysteresis				15		°C

6.6 Typical Characteristics

表 1. Table of Graphs

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at T_A = 25°C, V_S = ±18 V, V_{CM} = V_S / 2, R_L = 10 kΩ connected to V_S / 2, and C_L = 30 pF (unless otherwise noted)

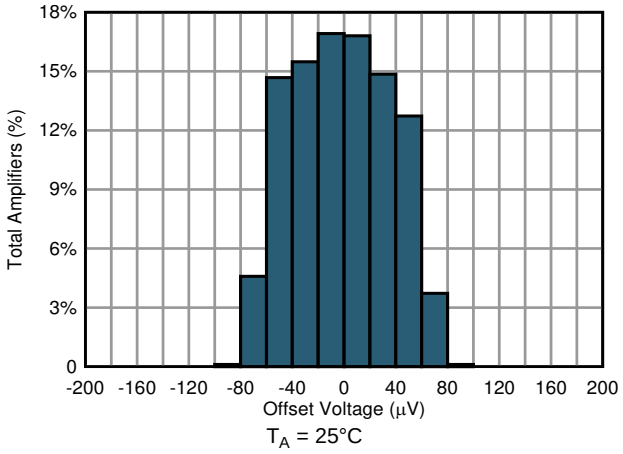


图 1. Offset Voltage Production Distribution

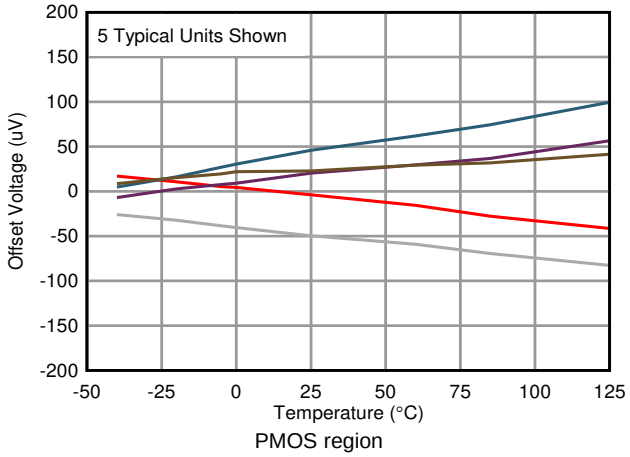


图 2. Offset Voltage vs Temperature (PMOS)

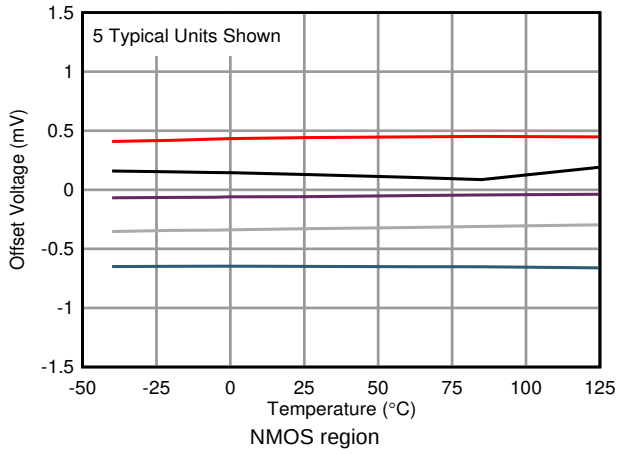


图 3. Offset Voltage vs Temperature (NMOS)

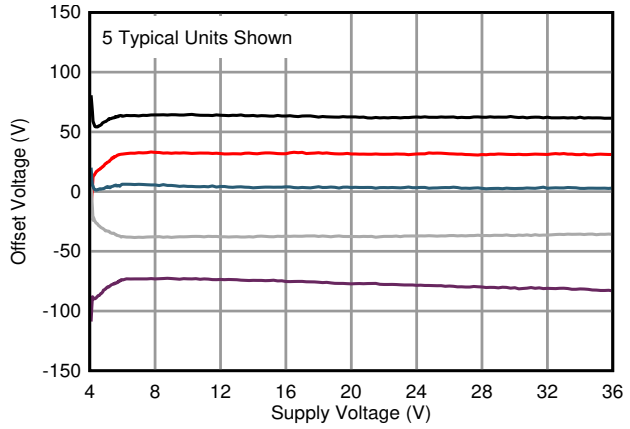


图 4. Offset Voltage vs Power Supply

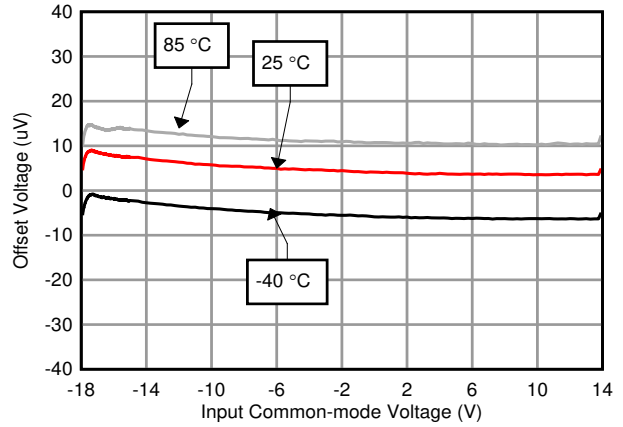


图 5. Offset Voltage vs Common-Mode Voltage

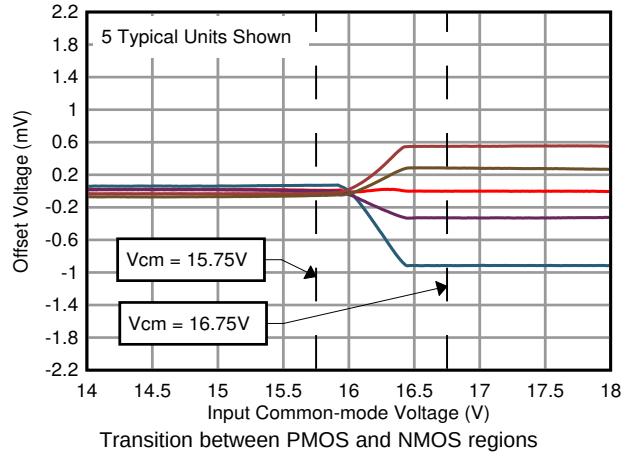


图 6. Offset Voltage vs Common-Mode Voltage in Transition Region

at T_A = 25°C, V_S = ±18 V, V_{CM} = V_S / 2, R_L = 10 kΩ connected to V_S / 2, and C_L = 30 pF (unless otherwise noted)

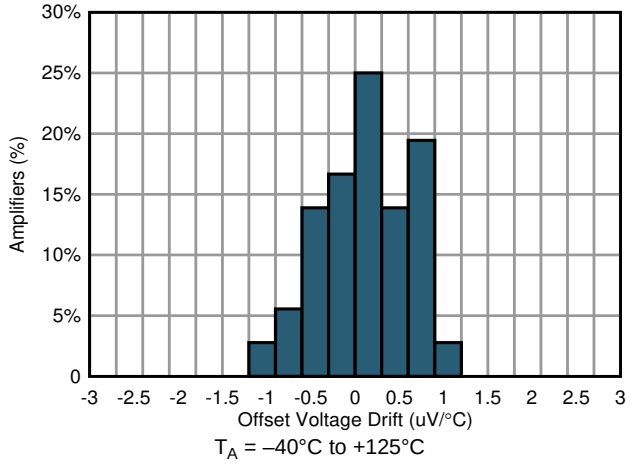


图 7. Offset Voltage Drift

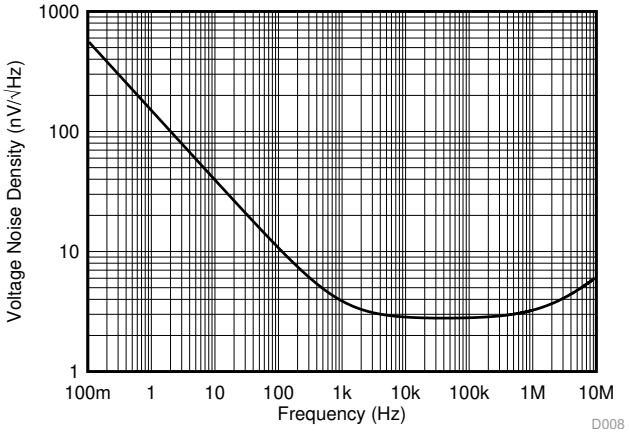


图 8. Input Voltage Noise Spectral Density

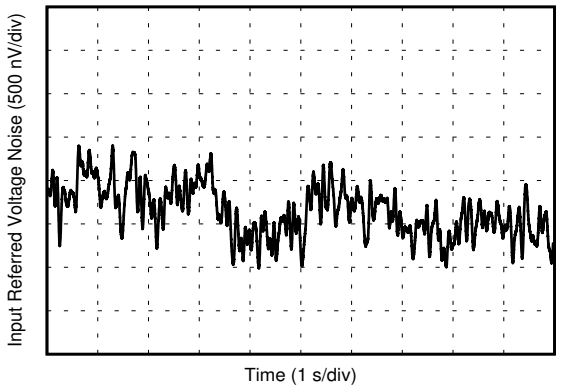


图 9. 0.1-Hz to 10-Hz Noise

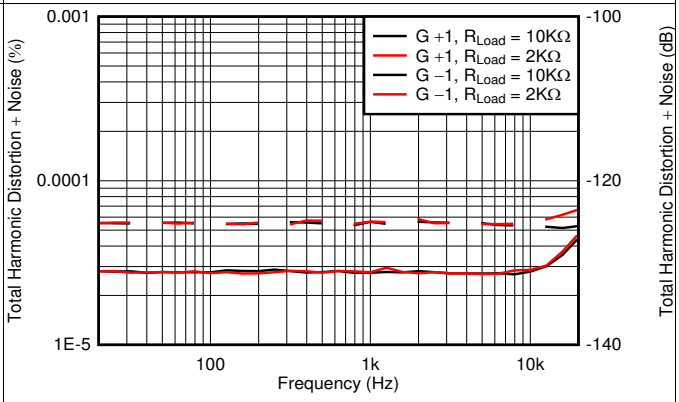


图 10. THD+N vs Frequency

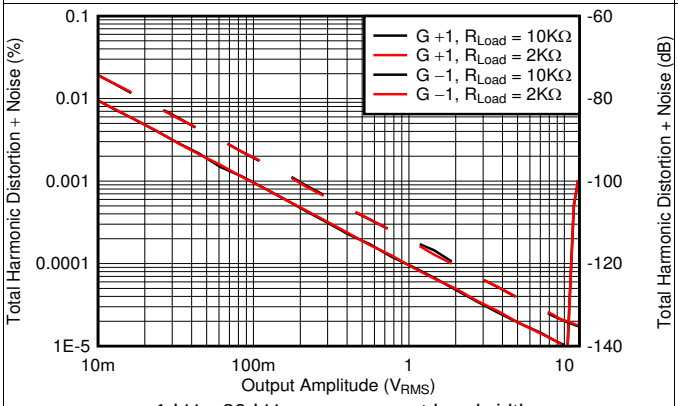


图 11. THD+N vs Output Amplitude

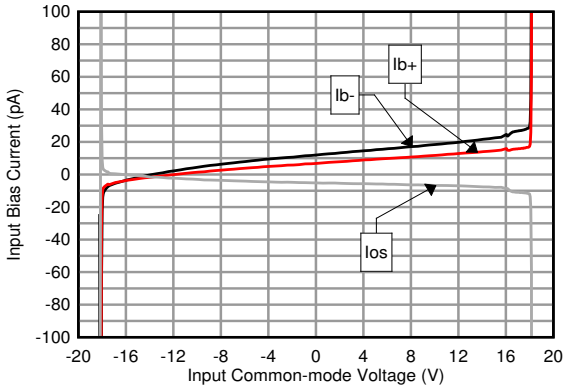


图 12. Input Bias and Offset Current vs Common-Mode Voltage (SOIC)

at T_A = 25°C, V_S = ±18 V, V_{CM} = V_S / 2, R_L = 10 kΩ connected to V_S / 2, and C_L = 30 pF (unless otherwise noted)

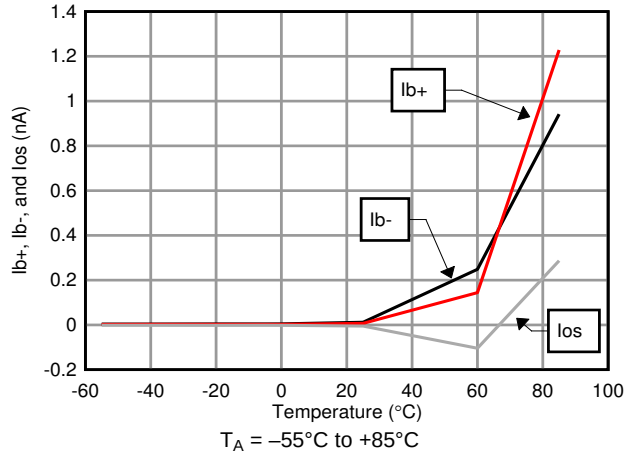


图 13. Input Bias and Offset Current vs Temperature (SOIC)

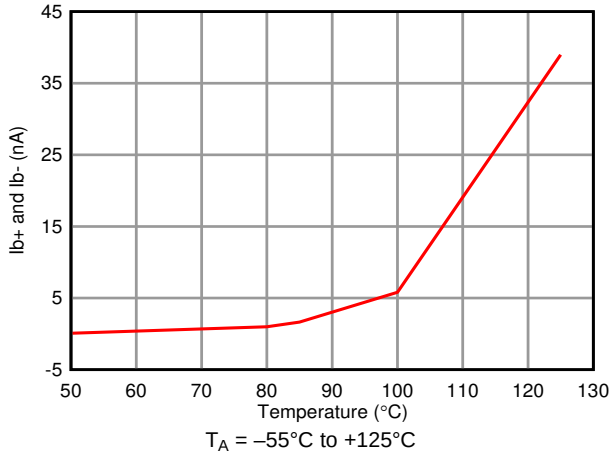


图 14. Input Bias and Offset Current vs Temperature (SOIC)

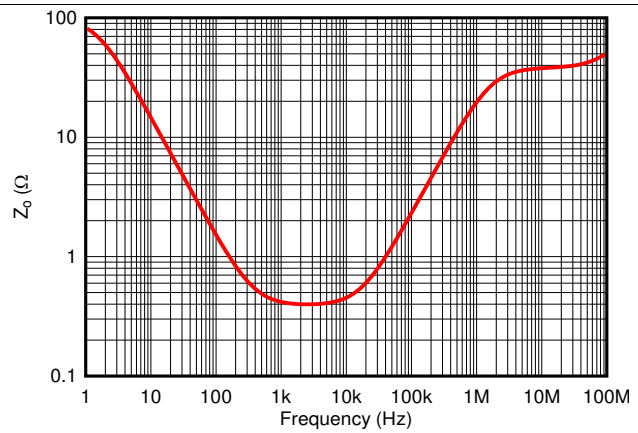


图 15. Open-Loop Output Impedance vs Frequency

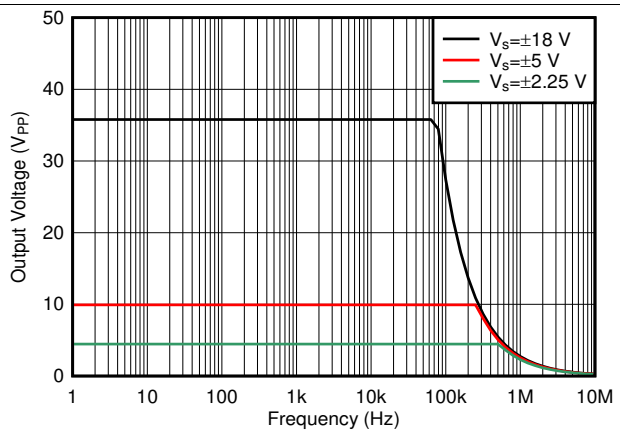


图 16. Maximum Output Voltage vs Frequency

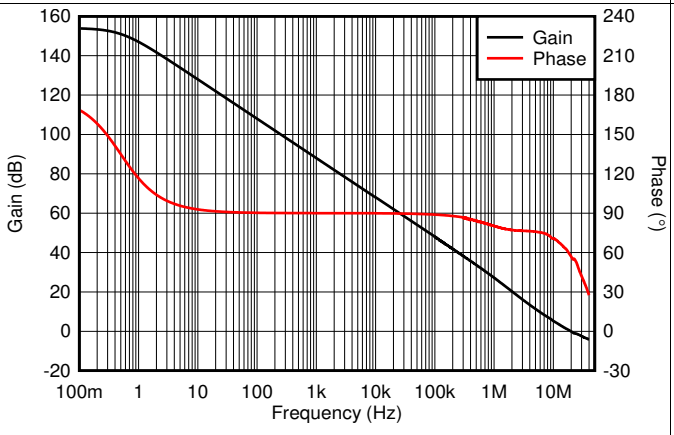


图 17. Open-Loop Gain and Phase vs Frequency

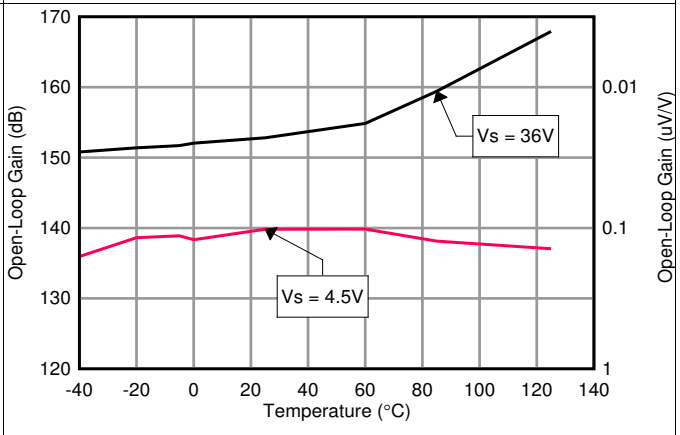


图 18. Open-Loop Gain vs Temperature

at T_A = 25°C, V_S = ±18 V, V_{CM} = V_S / 2, R_L = 10 kΩ connected to V_S / 2, and C_L = 30 pF (unless otherwise noted)

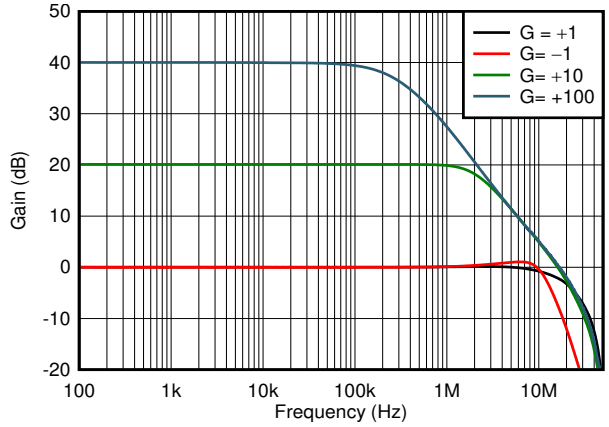


图 19. Closed-Loop Gain vs Frequency

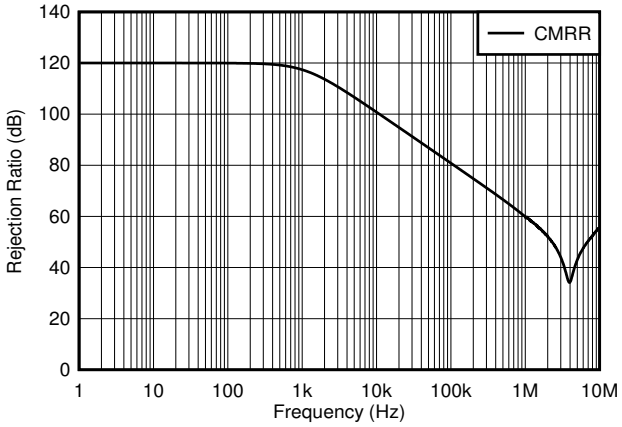


图 20. CMRR vs Frequency

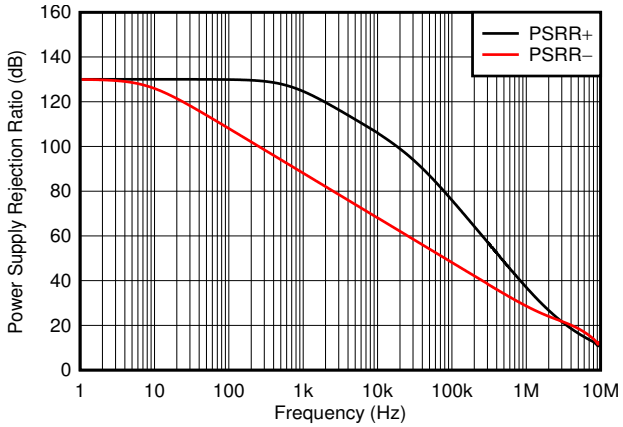


图 21. PSRR vs Frequency

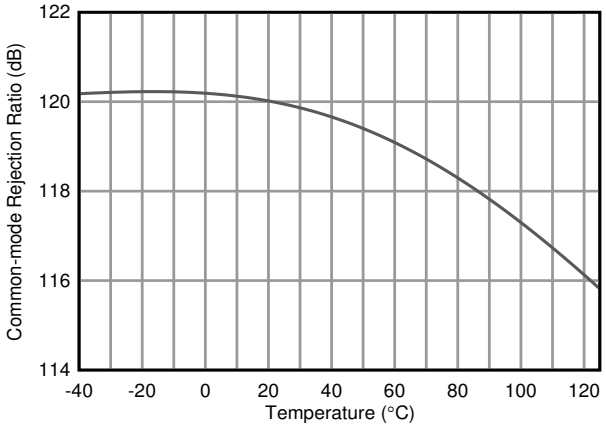


图 22. CMRR vs Temperature

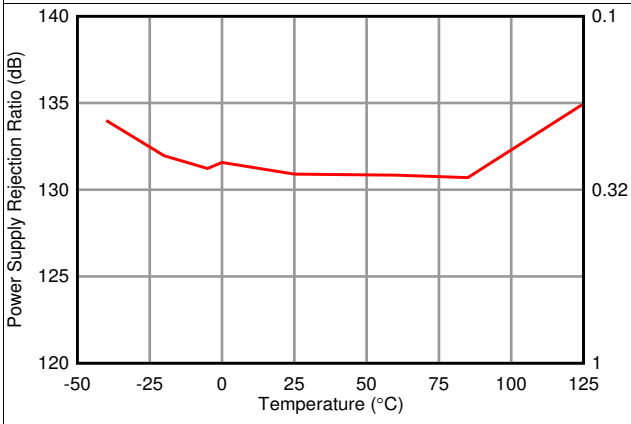


图 23. PSRR vs Temperature

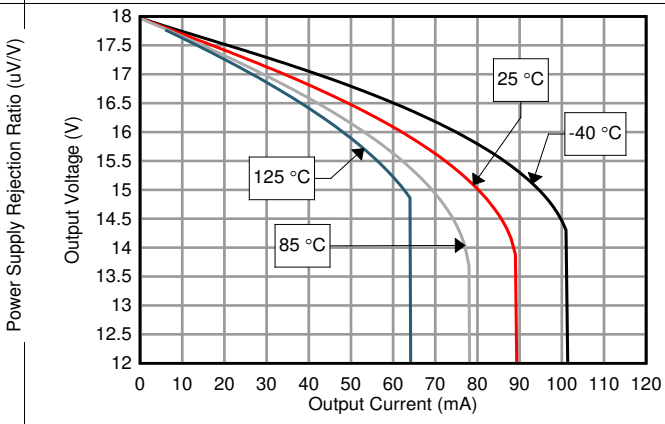


图 24. Positive Output Voltage vs Output Current

at T_A = 25°C, V_S = ±18 V, V_{CM} = V_S / 2, R_L = 10 kΩ connected to V_S / 2, and C_L = 30 pF (unless otherwise noted)

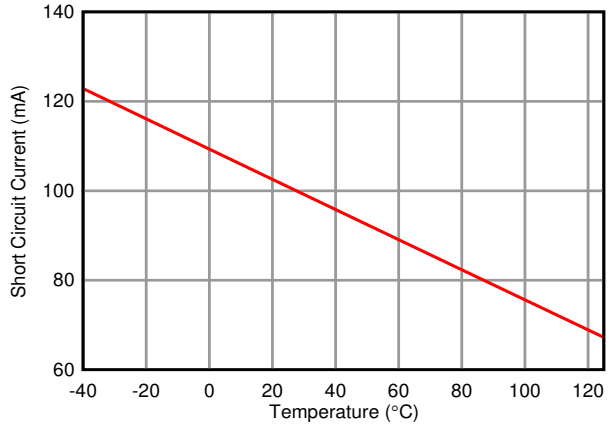


图 25. Short-Circuit Current vs Temperature

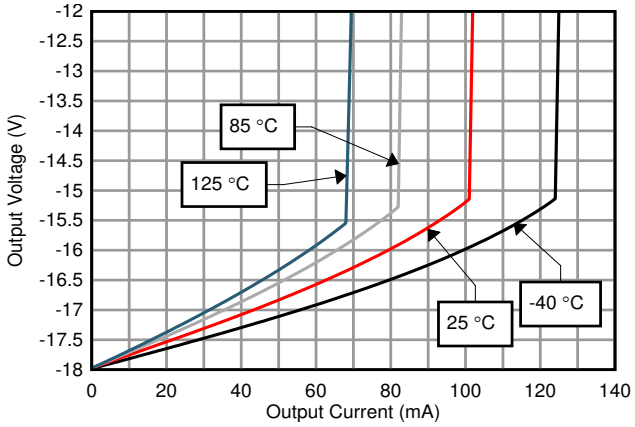


图 26. Negative Output Voltage vs Output Current

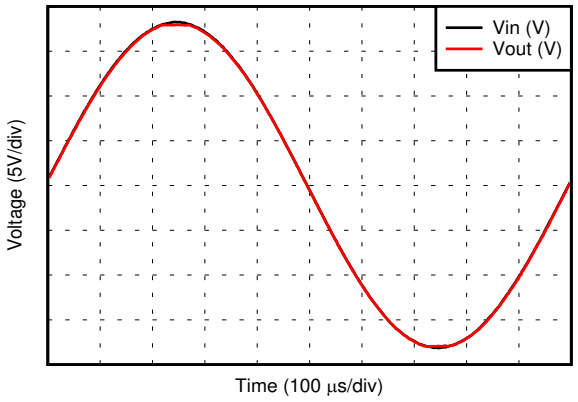


图 27. No Phase Reversal

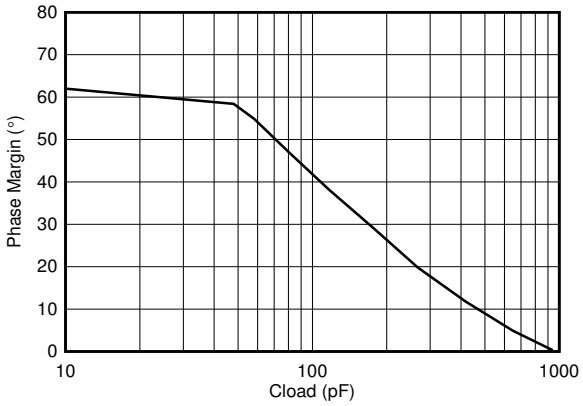


图 28. Phase Margin vs Capacitive Load

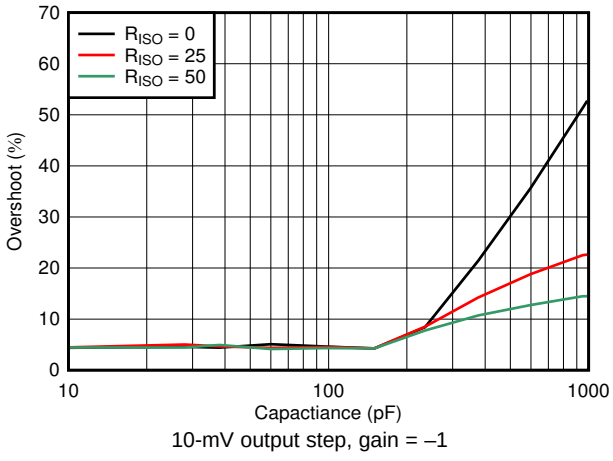


图 29. Small Signal Overshoot vs Capacitive Load

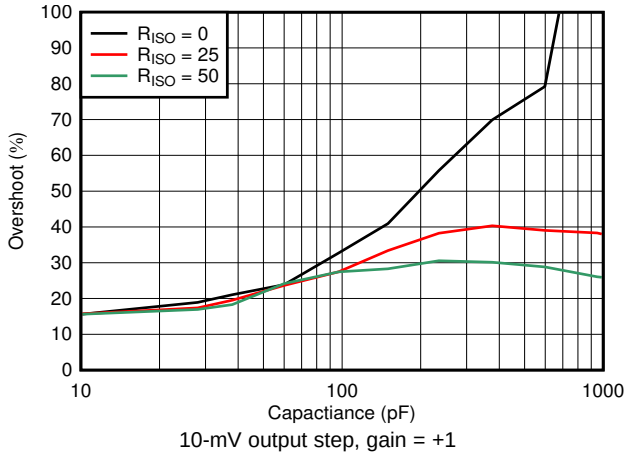
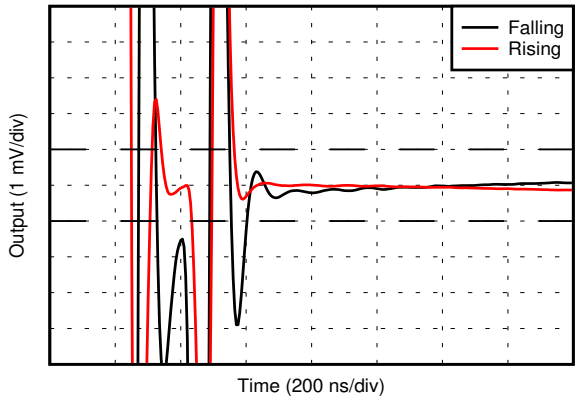


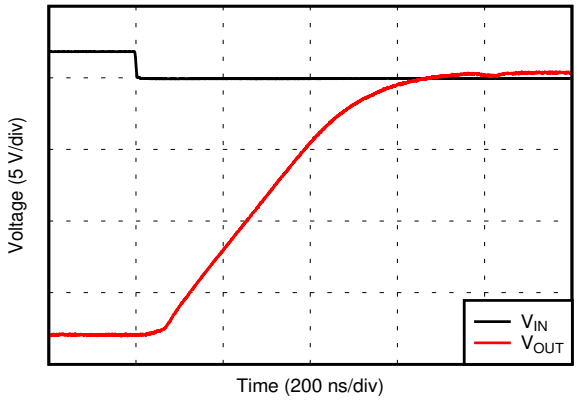
图 30. Small Signal Overshoot vs Capacitive Load

at T_A = 25°C, V_S = ±18 V, V_{CM} = V_S / 2, R_L = 10 kΩ connected to V_S / 2, and C_L = 30 pF (unless otherwise noted)



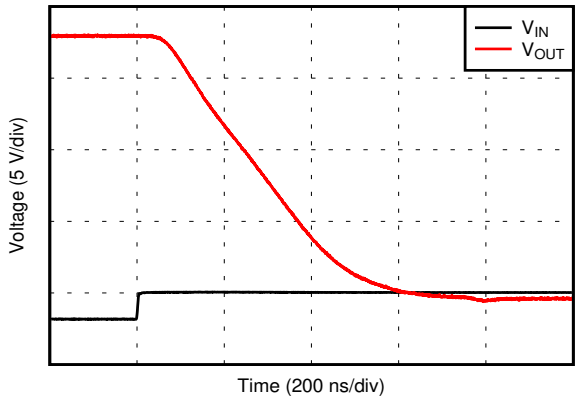
Vin = 5-Vpp

图 31. Normalized Settling Time



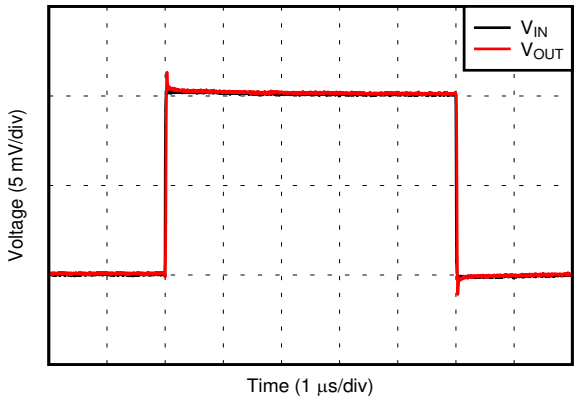
Gain = –10

图 32. Negative Overload Recovery



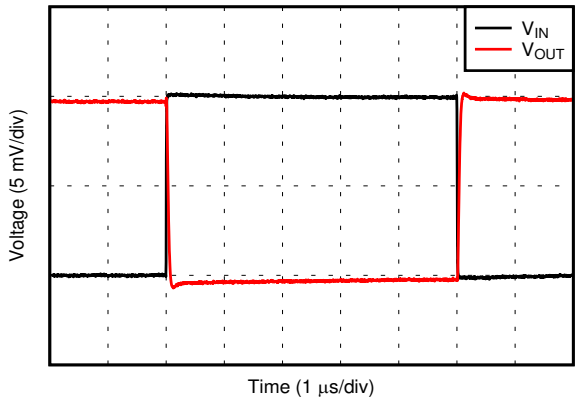
Gain = –10

图 33. Positive Overload Recovery



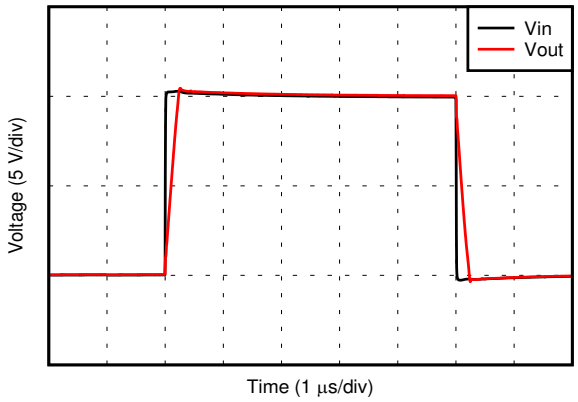
Vin = 10 mVpp, gain = 1

图 34. Small-Signal Step Response (Noninverting)



Vin = 10 mVpp, gain = –1

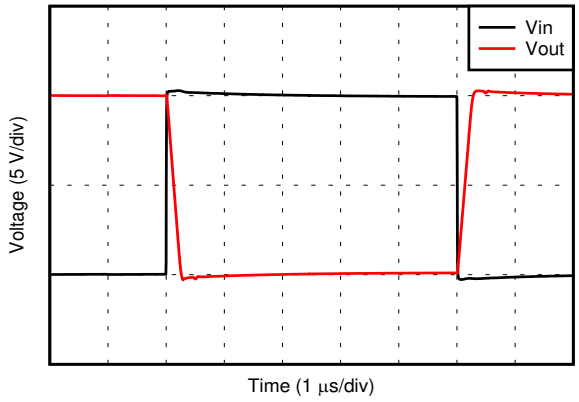
图 35. Small-Signal Step Response (Inverting)



Vin = 5 Vpp, gain = 1

图 36. Large-Signal Step Response (Noninverting)

at T_A = 25°C, V_S = ±18 V, V_{CM} = V_S / 2, R_L = 10 kΩ connected to V_S / 2, and C_L = 30 pF (unless otherwise noted)



Vin = 5 Vpp, gain = –1

图 37. Large Signal Step Response (Inverting)

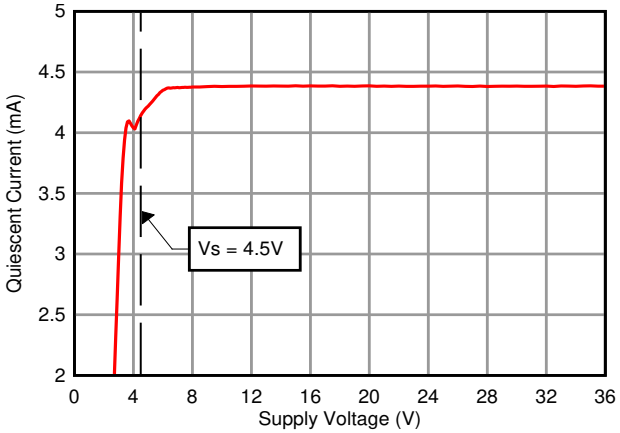


图 38. Quiescent Current vs Supply Voltage

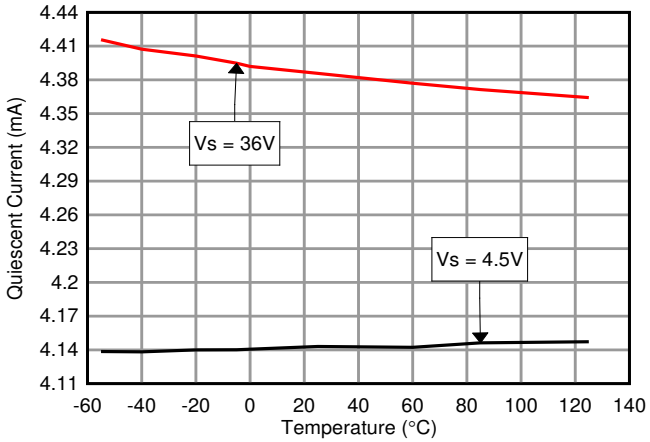


图 39. Quiescent Current vs Temperature

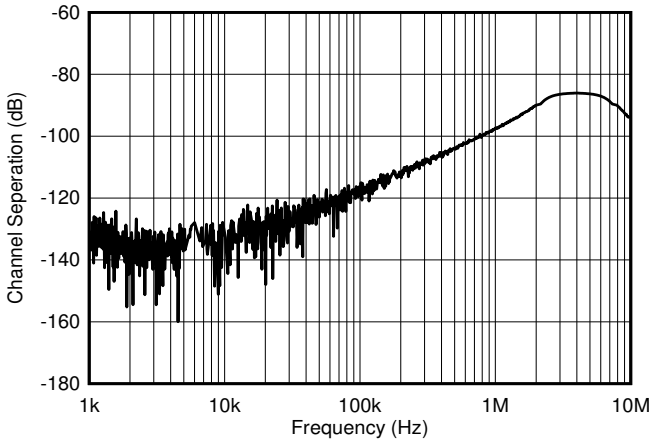
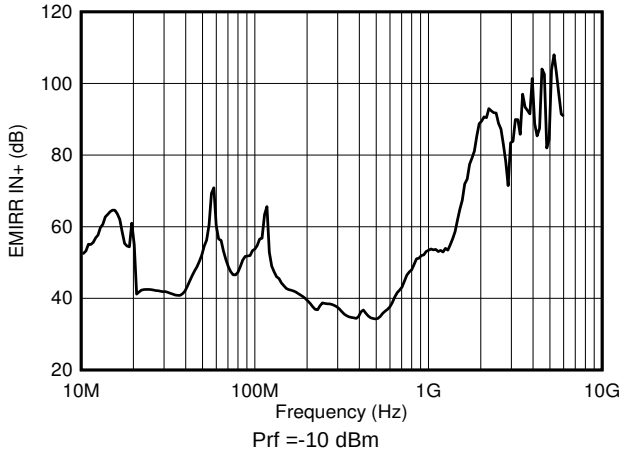


图 40. Channel Separation vs Frequency



Prf =-10 dBm

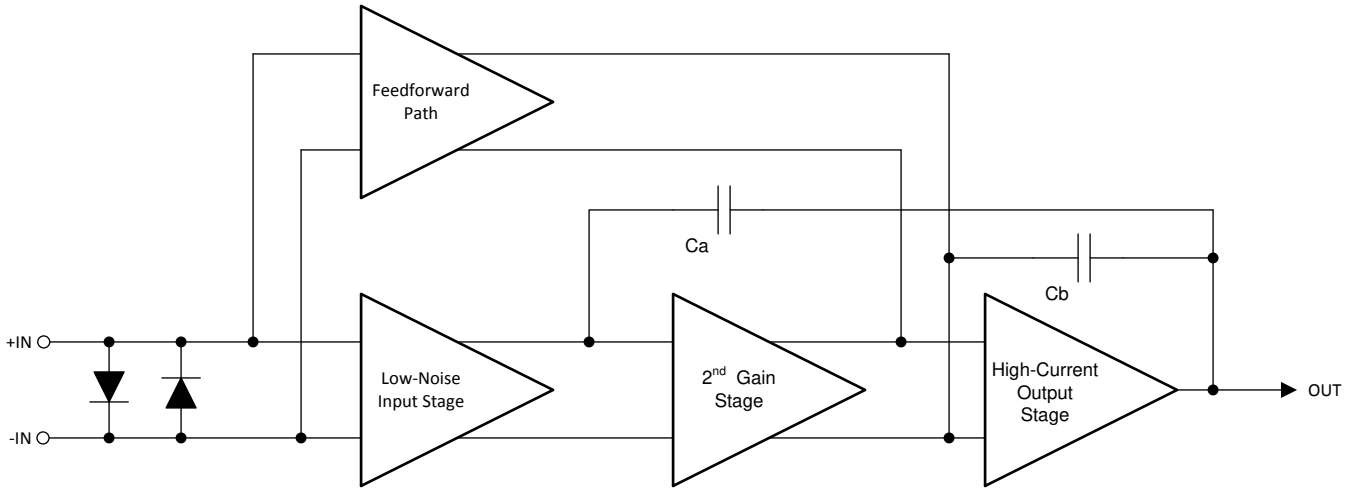
图 41. EMIRR vs Frequency

7 Detailed Description

7.1 Overview

The OPA2156 is laser trimmed to improve offset and uses a three-gain-stage architecture to achieve very low noise and distortion. The *Functional Block Diagram* shows a simplified schematic of the OPA2156 (one channel shown). The device consists of a low noise input stage and feed-forward pathway coupled to a high-current output stage. This topology exhibits superior distortion performance under a wide range of loading conditions compared to other operational amplifiers.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Phase Reversal Protection

The OPA2156 has internal phase-reversal protection. Many op amps exhibit phase reversal when the input is driven beyond the linear common-mode range. This condition is most often encountered in noninverting circuits when the input is driven beyond the specified common-mode voltage range, causing the output to reverse into the opposite rail. The input of the OPA2156 prevents phase reversal with excessive common-mode voltage. Instead, the appropriate rail limits the output voltage. This performance is shown in 图 42.

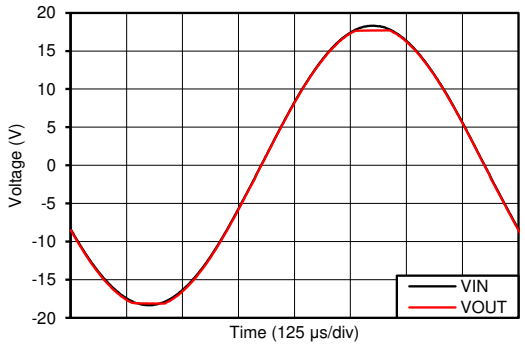


图 42. Output Waveform Devoid of Phase Reversal During an Input Overdrive Condition

Feature Description (接下页)

7.3.2 Electrical Overstress

Designers often ask questions about the capability of an operational amplifier to withstand electrical overstress. These questions tend to focus on the device inputs, but can involve the supply voltage pins or even the output pin. Each of these different pin functions have electrical stress limits determined by the voltage breakdown characteristics of the particular semiconductor fabrication process and specific circuits connected to the pin. Additionally, internal electrostatic discharge (ESD) protection is built into these circuits to protect them from accidental ESD events both before and during product assembly.

A good understanding of this basic ESD circuitry and the relevance to an electrical overstress event is helpful. 图 43 illustrates the ESD circuits contained in the OPA2156 (indicated by the dashed line area). The ESD protection circuitry involves several current-steering diodes connected from the input and output pins and routed back to the internal power-supply lines, where the diodes meet at an absorption device internal to the operational amplifier. This protection circuitry is intended to remain inactive during normal circuit operation.

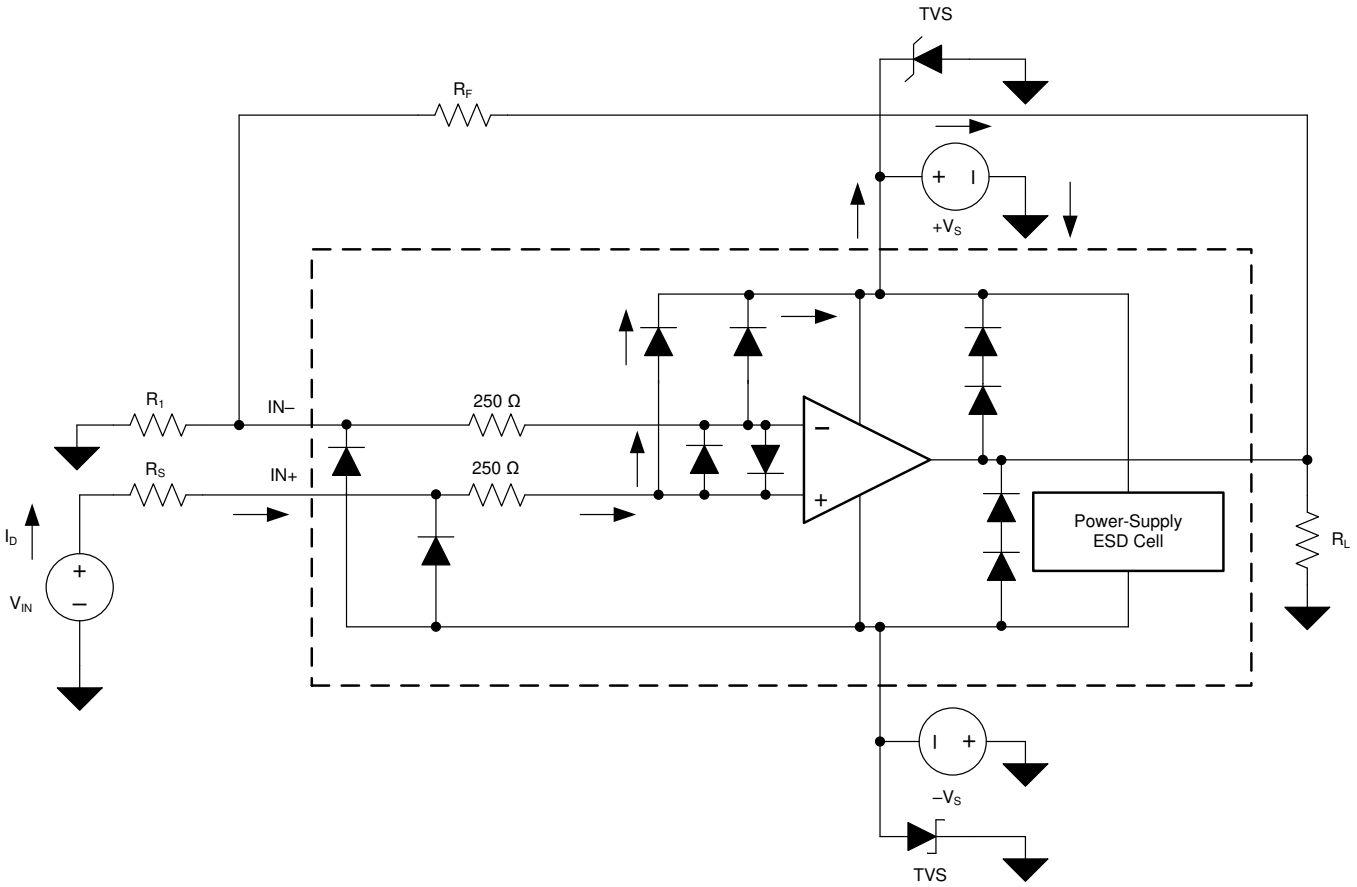


图 43. Equivalent Internal ESD Circuitry Relative to a Typical Circuit Application

An ESD event produces a short-duration, high-voltage pulse that is transformed into a short-duration, high-current pulse when discharging through a semiconductor device. The ESD protection circuits are designed to provide a current path around the operational amplifier core to prevent damage. The energy absorbed by the protection circuitry is then dissipated as heat.

When an ESD voltage develops across two or more amplifier device pins, current flows through one or more steering diodes. Depending on the path that the current takes, the absorption device can activate. The absorption device has a trigger, or threshold voltage, that is above the normal operating voltage of the OPA2156 but below the device breakdown voltage level. When this threshold is exceeded, the absorption device quickly activates and clamps the voltage across the supply rails to a safe level.

Feature Description (接下页)

When the operational amplifier connects into a circuit (see 图 43), the ESD protection components are intended to remain inactive and do not become involved in the application circuit operation. However, circumstances may arise where an applied voltage exceeds the operating voltage range of a given pin. If this condition occurs, there is a risk that some internal ESD protection circuits can turn on and conduct current. Any such current flow occurs through steering-diode paths and rarely involves the absorption device.

图 43 shows a specific example where the input voltage (V_{IN}) exceeds the positive supply voltage (V+) by 500 mV or more. Much of what happens in the circuit depends on the supply characteristics. If V+ can sink the current, one of the upper input steering diodes conducts and directs current to V+. Excessively high current levels can flow with increasingly higher V_{IN}. As a result, the data sheet specifications recommend that applications limit the input current to 10 mA.

If the supply is not capable of sinking the current, V_{IN} can begin sourcing current to the operational amplifier and then take over as the source of positive supply voltage. The danger in this case is that the voltage can rise to levels that exceed the operational amplifier absolute maximum ratings.

Another common question involves what happens to the amplifier if an input signal is applied to the input when the power supplies (V+ or V–) are at 0 V. Again, this question depends on the supply characteristic when at 0 V, or at a level below the input signal amplitude. If the supplies appear as high impedance, then the input source supplies the operational amplifier current through the current-steering diodes. This state is not a normal bias condition; most likely, the amplifier does not operate normally. If the supplies are low impedance, then the current through the steering diodes can become quite high. The current level depends on the ability of the input source to deliver current, and any resistance in the input path.

If there is any uncertainty about the ability of the supply to absorb this current, add external Zener diodes to the supply pins; see 图 43. Select the Zener voltage so that the diode does not turn on during normal operation. However, the Zener voltage must be low enough so that the Zener diode conducts if the supply pin begins to rise above the safe-operating, supply-voltage level.

Feature Description (接下页)

7.3.3 Thermal Considerations

Through normal operation the OPA2156 will experience self-heating, a natural increase in the die junction temperature which occurs in every amplifier. This is a result of several factors including the quiescent power consumption, the package's thermal dissipation, PCB layout and the device operating conditions.

To fully ensure the amplifier will operate without entering thermal shutdown it is important to calculate the approximate junction (die) temperature which can be done using 公式 1.

$$T_J = P_D * \Theta J_A + T_A \tag{1}$$

公式 2 shows the approximate junction temperature for the OPA2156 while unloaded with an ambient temperature of 25°C.

$$T_J = (36V * 4.4mA) * 120°C / W + 25°C$$
$$T_J = 44°C \tag{2}$$

For high voltage, high precision amplifiers such as the OPA2156 the junction temperature can easily be 10s of degrees higher than the ambient temperature in a quiescent (unloaded) condition. If the device then begins to drive a heavy load the junction temperature may rise and trip the thermal shutdown circuit. The 图 44 shows the maximum output voltage of the OPA2156 without entering thermal shutdown vs ambient temperature in both a loaded and unloaded condition.

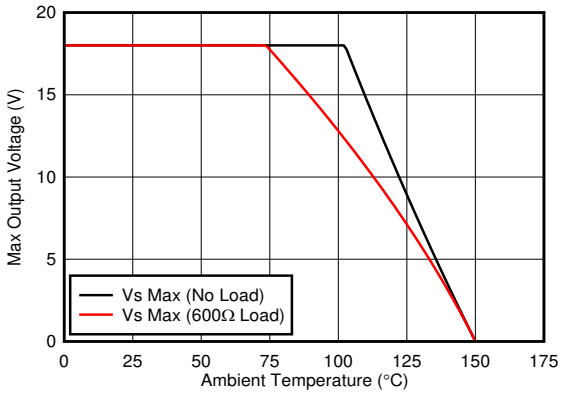


图 44. OPA2156 Thermal Safe Operating Area

Feature Description (接下页)

7.3.4 Thermal Shutdown

The internal power dissipation of any amplifier causes the internal (junction) temperature to rise. This phenomenon is called *self heating*. The OPA2156 has a thermal protection feature that prevents damage from self heating.

This thermal protection works by monitoring the temperature of the output stage and turning off the op amp output drive for temperatures above approximately 170°C. Thermal protection forces the output to a high-impedance state. The OPA2156 is also designed with approximately 15°C of thermal hysteresis. Thermal hysteresis prevents the output stage from cycling in and out of the high-impedance state. The OPA2156 returns to normal operation when the output stage temperature falls below approximately 155°C.

The absolute maximum junction temperature of the OPA2156 is 150°C. Exceeding the limits shown in the *Absolute Maximum Ratings* table may cause damage to the device. Thermal protection triggers at 170°C because of unit-to-unit variance, but does not interfere with device operation up to the absolute maximum ratings. This thermal protection is not designed to prevent this device from exceeding absolute maximum ratings, but rather from excessive thermal overload.

7.3.5 Common-Mode Voltage Range

The OPA2156 is a 36-V, true rail-to-rail input operational amplifier with an input common-mode range that extends 100 mV beyond either supply rail. This wide range is achieved with paralleled complementary N-channel and P-channel differential input pairs. The N-channel pair is active for input voltages close to the positive rail, typically (V+) – 2.25 V to 100 mV above the positive supply. The P-channel pair is active for inputs from 100 mV below the negative supply to approximately (V+) – 1.25 V. There is a small transition region, typically (V+) – 2.25V to (V+) – 1.25 V in which both input pairs are active. This transition region varies modestly with process variation. Within this region PSRR, CMRR, offset voltage, offset drift, noise, and THD performance are degraded compared to operation outside this region.

To achieve the best performance for two-stage rail-to-rail input amplifiers, avoid the transition region when possible. The OPA2156 uses a precision trim for both the N-channel and P-channel regions. This technique enables significantly lower levels of offset than previous-generation devices, causing variance in the transition region of the input stages to appear exaggerated relative to offset over the full common-mode range.

7.3.6 Overload Recovery

Overload recovery is defined as the time required for the op amp output to recover from a saturated state to a linear state. The output devices of the op amp enter a saturation region when the output voltage exceeds the rated operating voltage, either due to the high input voltage or the high gain. After the device enters the saturation region, the charge carriers in the output devices require time to return back to the linear state. After the charge carriers return back to the linear state, the device begins to slew at the specified slew rate. Thus, the propagation delay in case of an overload condition is the sum of the overload recovery time and the slew time.

7.4 Device Functional Modes

The OPA2156 has a single functional mode and is operational when the power-supply voltage is greater than 4.5 V (±2.25 V). The maximum power supply voltage for the OPA2156 is 36 V (±18 V).

8 Application and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The OPA2156 offers excellent dc precision and ac performance. The device operates with up to 36-V supply rails offering true rail-to-rail input/output, low offset voltage and offset voltage drift, as well as 25-MHz bandwidth and low input bias. These features make the OPA2156 a robust, high-performance operational amplifier for high-voltage industrial applications.

8.1.1 Slew Rate Limit for Input Protection

In control systems for valves or motors, abrupt changes in voltages or currents can cause mechanical damages. By controlling the slew rate of the command voltages into the drive circuits, the load voltages ramps up and down at a safe rate. For symmetrical slew-rate applications (positive slew rate equals negative slew rate), one additional op amp provides slew-rate control for a given analog gain stage. The unique input protection and high output current and slew rate of the OPA2156 make the device an optimal amplifier to achieve slew rate control for both dual- and single-supply systems.图 45 shows the OPA2156 in a slew-rate limit design.

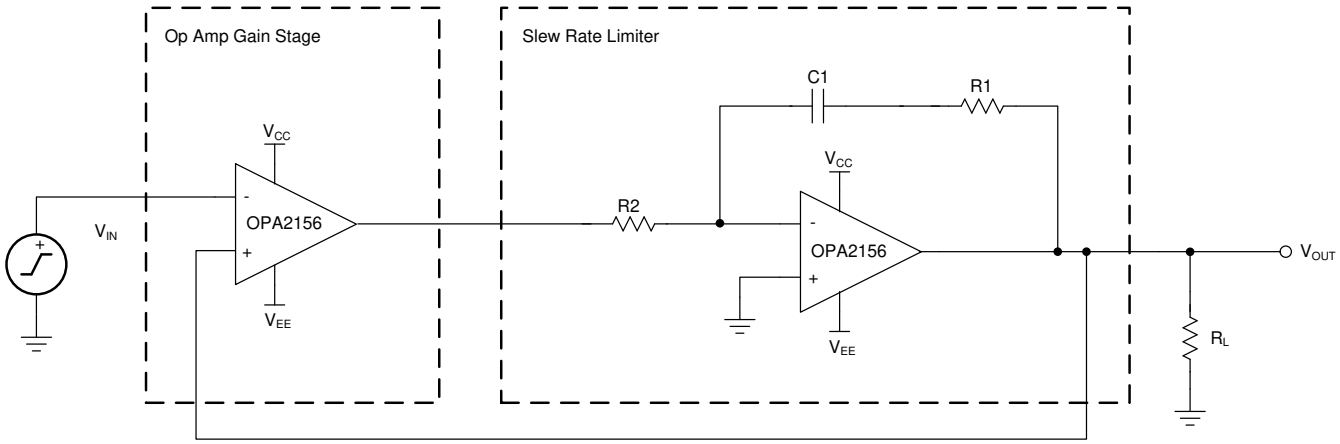


图 45. Slew Rate Limiter Uses One Op Amp

For step-by-step design procedure, circuit schematics, bill of materials, PCB files, simulation results, and test results, refer to TI Precision Design TIDU026, *Slew Rate Limiter Uses One Op Amp*.

8.2 Typical Application

The combination of low input bias, high slew rate and a rail-to-rail input and output enable the OPA2156 to serve as an accurate differential photodiode transimpedance amplifier. This application example shows the design of such a system.

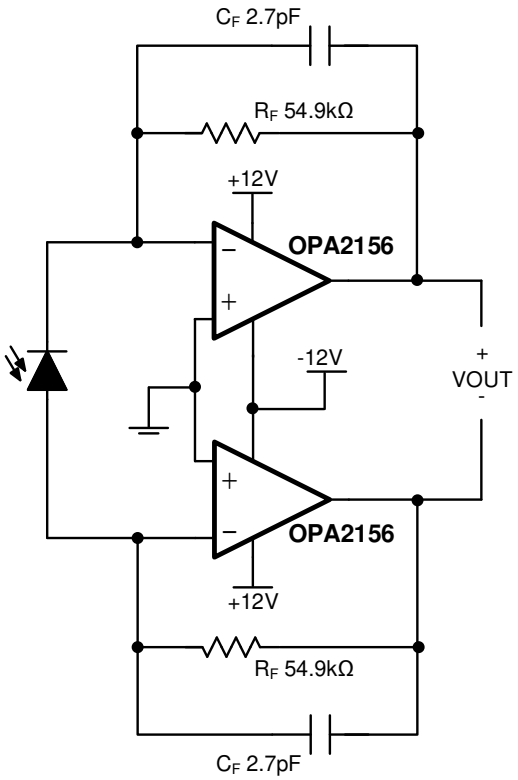


图 46. OPA2156 Configured as a Differential Photodiode Transimpedance Amplifier

8.2.1 Design Requirements

The design requirements for this design are:

- Photodiode current: 0 µA to 90 µA
- Output voltage: –5 V to 5 V
- Supply voltage: ±12 V
- Filter cutoff frequency: 1 MHz

8.2.2 Detailed Design Procedure

In this example the OPA2156 serves as a transimpedance amplifier for a differential photodiode. The differential configuration allows for a wider output range (0 to 10-V differential) compared to a single-ended configuration (0 V to 5 V). This output can be connected to a differential successive approximation register (SAR) analog-to-digital converter (ADC). The basic equation for a differential transimpedance amplifier output voltage is shown in 公式 3.

$$V_{OUT} = I_{PD} \times 2 \times R_F \quad (3)$$

公式 3 can be rearranged to calculate the value of the feedback resistors as shown in 公式 4.

Typical Application (接下页)

$$\frac{V_{OUT(MAX)} - V_{OUT(MIN)}}{2 \times I_{IN(MAX)}} \le R_F$$
$$\frac{5V - (-5V)}{2 \times 90\mu A} \le 55.6k\Omega \quad (4)$$

Adding a capacitor to the feedback loop creates a filter which will remove undesired noise beyond its cutoff frequency. For this application a 1-MHz cutoff frequency was selected. The equation for an RC filter is provided in 公式 5.

$$f_C = \frac{1}{2 \times \pi \times R_F \times C_F} \quad (5)$$

Rearranging this equation to solve for the capacitor value is show in 公式 6.

$$C_F \le \frac{1}{2 \times \pi \times 54k\Omega \times 1MHz} \le 2.7\,pF \quad (6)$$

For more information on photodiode transimpedance amplifier system design and for a single-ended example, see *TIDU535: 1 MHz, Single-Supply, Photodiode Amplifier Reference Design*.

8.2.3 Application Curves

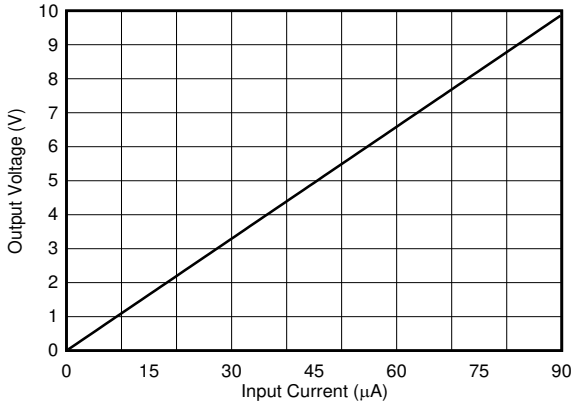


图 47. Differential Photodiode DC Transfer

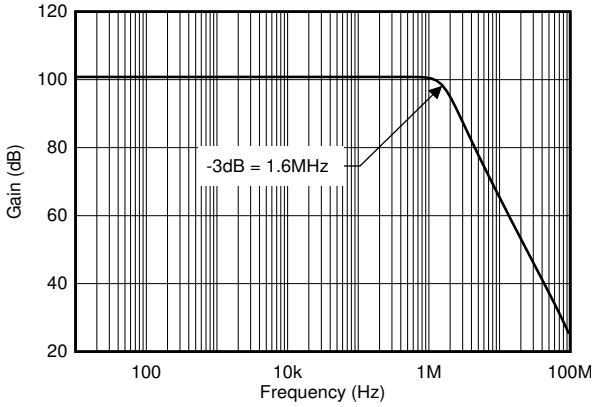


图 48. Differential Photodiode AC Transfer

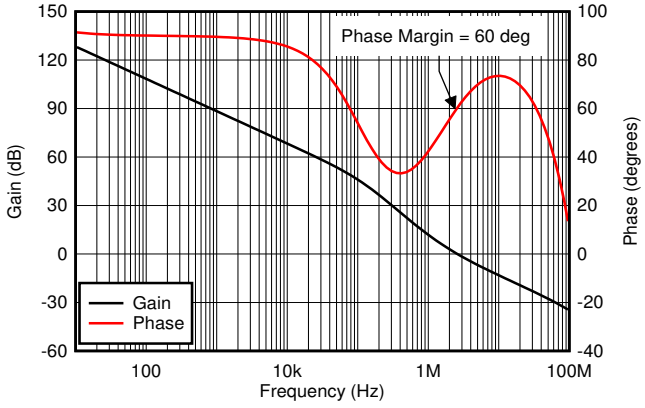


图 49. Differential Photodiode Stability

9 Power Supply Recommendations

The OPA2156 is specified for operation from 4.5 V to 36 V (±2.25 V to ±18 V); many specifications apply from –40°C to 125°C. Parameters that can exhibit significant variance with regard to operating voltage or temperature are presented in the *Typical Characteristics*.

CAUTION

Supply voltages larger than 40 V can permanently damage the device; see the *Absolute Maximum Ratings*.

10 Layout

10.1 Layout Guidelines

For best operational performance of the device, use good PCB layout practices, including:

- Connect low-ESR, 0.1-µF ceramic bypass capacitors between each supply pin and ground, placed as close as possible to the device. A single bypass capacitor from V+ to ground is applicable for single-supply applications.
  - Noise can propagate into analog circuitry through the power pins of the circuit as a whole and op amp itself. Bypass capacitors are used to reduce the coupled noise by providing low-impedance power sources local to the analog circuitry.
- Make sure to physically separate digital and analog grounds paying attention to the flow of the ground current. Separate grounding for analog and digital portions of circuitry is one of the simplest and most-effective methods of noise suppression. One or more layers on multilayer PCBs are usually devoted to ground planes. A ground plane helps distribute heat and reduces EMI noise pickup.
- In order to reduce parasitic coupling, run the input traces as far away as possible from the supply or output traces. If these traces cannot be kept separate, crossing the sensitive trace perpendicular is much better as opposed to in parallel with the noisy trace.
- Place the external components as close to the device as possible. As shown in 图 50, keeping RF and RG close to the inverting input minimizes parasitic capacitance.
- Keep the length of input traces as short as possible. Always remember that the input traces are the most sensitive part of the circuit.
- Consider a driven, low-impedance guard ring around the critical traces. A guard ring can significantly reduce leakage currents from nearby traces that are at different potentials.
- Clean the PCB following board assembly for best performance.
- Any precision integrated circuit may experience performance shifts due to moisture ingress into the plastic package. After any aqueous PCB cleaning process, bake the PCB assembly to remove moisture introduced into the device packaging during the cleaning process. A low-temperature, post-cleaning bake at 85°C for 30 minutes is sufficient for most circumstances.

10.1.1 Power Dissipation

The OPA2156 op amp is capable of driving a variety of loads with a power-supply voltage up to ±18 V and full operating temperature range. Internal power dissipation increases when operating at high supply voltages and/or high output currents. Copper leadframe construction used in the OPA2156 improves heat dissipation compared to conventional materials. Circuit board layout can also help minimize junction temperature rise. Wide copper traces help dissipate the heat by acting as an additional heat sink. Temperature rise can be further minimized by soldering the devices to the circuit board rather than using a socket.

Layout Guidelines (接下页)

The OPA2156 has an internal thermal protection feature which prevents it from being damaged due to self heating, or the internal heating generated during normal operation. The protection circuitry works by monitoring the temperature of the output stage and turns of the output drive if the junction temperature of the device rises to approximately 170°C. The device has a thermal hysteresis of approximately 15°C, which allows the device to safely cool down before returning to normal operation at approximately 155°C. TI recommends that the system design takes into account the thermal dissipation of the OPA2156 to ensure that the recommended operating junction temperature of 125°C is not exceeded to avoid decreasing the lifespan of the device or permanently damaging the amplifier.

10.2 Layout Example

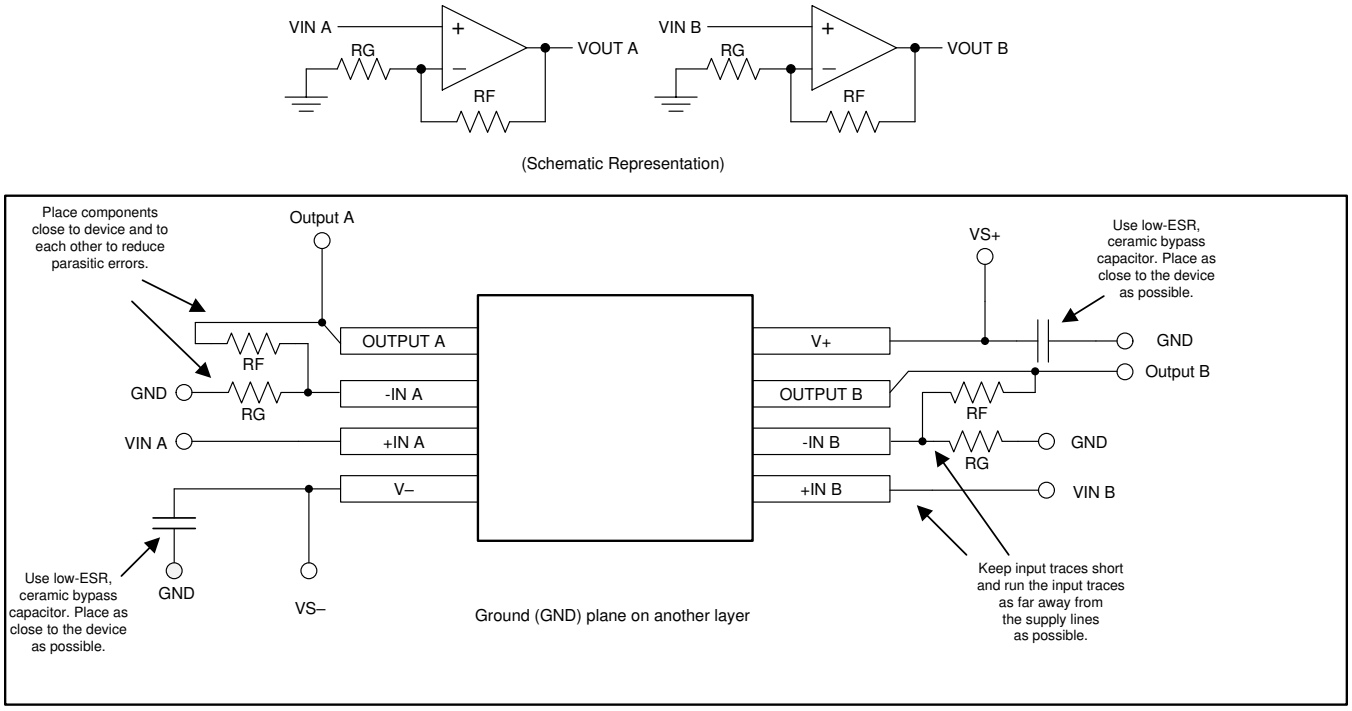


图 50. Operational Amplifier Board Layout for Noninverting Configuration

11 器件和文档支持

11.1 器件支持

11.1.1 开发支持

11.1.1.1 TINA-TI™（免费软件下载）

TINA™是一款简单、功能强大且易于使用的电路仿真程序，此程序基于 SPICE 引擎。TINA-TI 是 TINA 软件的一款免费全功能版本，除了一系列无源和有源模型外，此版本软件还预先载入了一个宏模型库。TINA-TI 提供所有传统的 SPICE 直流、瞬态和频域分析，以及其他设计功能。

TINA-TI 可通过模拟电子实验室设计中心免费下载，该软件提供了丰富的后处理能力，允许用户以各种方式设置结果的格式。虚拟仪器提供选择输入波形和探测电路节点、电压以及波形的功能，从而构建一个动态的快速入门工具。

注

这些文件需要安装 TINA 软件（由 DesignSoft™提供）或者 TINA-TI 软件。请从 TINA-TI 文件夹中下载免费的 TINA-TI 软件（网址为 http://www.ti.com.cn/tool/cn/tina-ti）。

11.1.1.2 TI 高精度设计

TI 高精度设计（请访问 http://www.ti.com.cn/ww/analog/precision-designs/ 获取）是由 TI 公司高精度模拟 应用 专家创建的模拟解决方案，提供了许多实用电路的工作原理、组件选择、仿真、完整印刷电路板 (PCB) 电路原理图和布局布线、物料清单以及性能测量结果。

11.2 文档支持

11.2.1 相关文档

- 德州仪器 (TI)，*《运算放大器的 EMI 抑制比》* 应用报告
- 德州仪器 (TI)，*《0-1A 单电源低侧电流检测解决方案》* 参考设计
- 德州仪器 (TI)，*《适合所有人的运算放大器》* 设计参考

11.3 接收文档更新通知

要接收文档更新通知，请导航至 TI.com.cn 上的器件产品文件夹。单击右上角的*通知我* 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

11.4 社区资源

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.5 商标

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11.6 静电放电警告

ESD 可能会损坏该集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理措施和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。 精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

11.7 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 机械、封装和可订购信息

以下页面包含机械、封装和可订购信息。这些信息是指定器件的最新可用数据。数据如有变更，恕不另行通知，且不会对此文档进行修订。如需获取此数据表的浏览器版本，请查阅左侧的导航栏。

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
OPA2156ID	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OP2156
OPA2156ID.A	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OP2156
OPA2156IDG4	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OP2156
OPA2156IDG4.A	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OP2156
OPA2156IDGKR	Active	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	Yes	NIPDAUAG | SN	Level-2-260C-1 YEAR	-40 to 125	1THV
OPA2156IDGKR.A	Active	Production	VSSOP (DGK) | 8	2500 | LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 125	1THV
OPA2156IDGKT	Active	Production	VSSOP (DGK) | 8	250 | SMALL T&R	Yes	NIPDAUAG | SN	Level-2-260C-1 YEAR	-40 to 125	1THV
OPA2156IDGKT.A	Active	Production	VSSOP (DGK) | 8	250 | SMALL T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 125	1THV
OPA2156IDR	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OP2156
OPA2156IDR.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OP2156

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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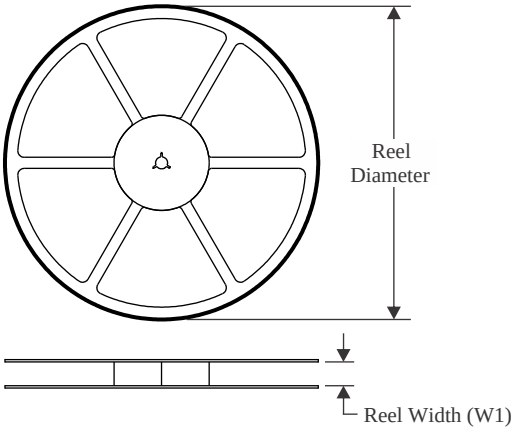
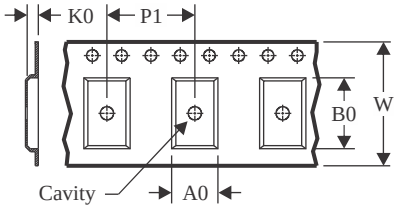
TAPE AND REEL INFORMATION

REEL DIMENSIONS

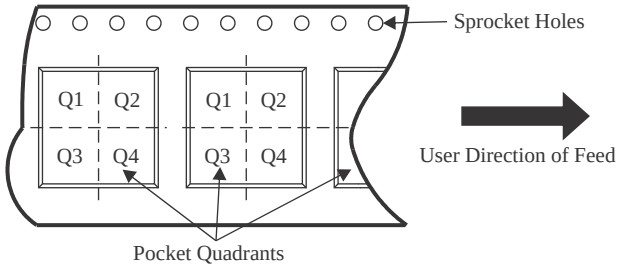


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

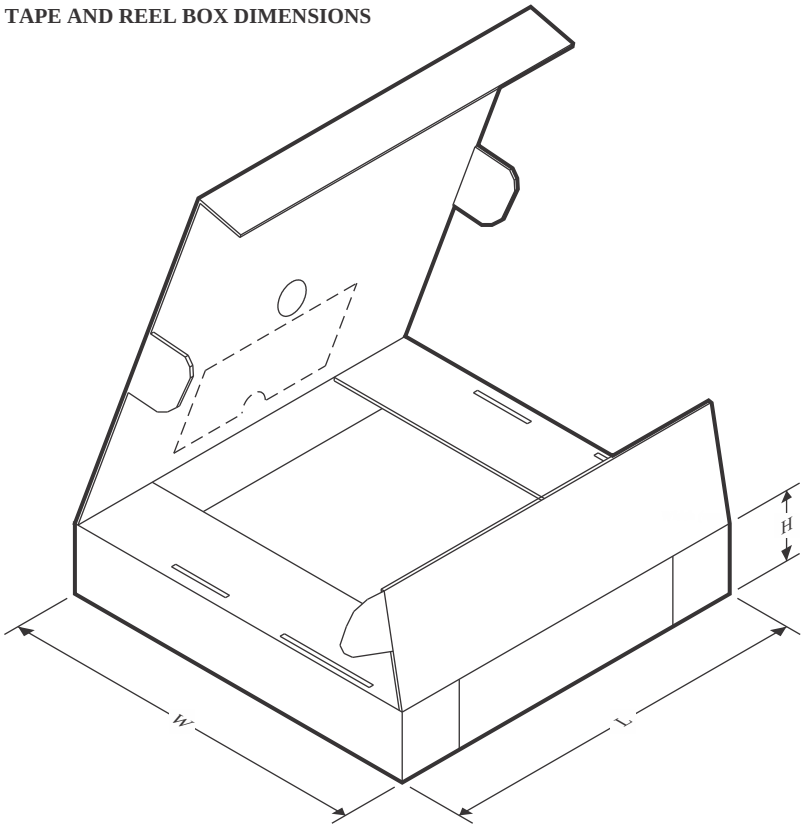
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
OPA2156IDGKR	VSSOP	DGK	8	2500	330.0	12.4	5.25	3.35	1.25	8.0	12.0	Q1
OPA2156IDGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
OPA2156IDGKT	VSSOP	DGK	8	250	330.0	12.4	5.25	3.35	1.25	8.0	12.0	Q1
OPA2156IDGKT	VSSOP	DGK	8	250	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
OPA2156IDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

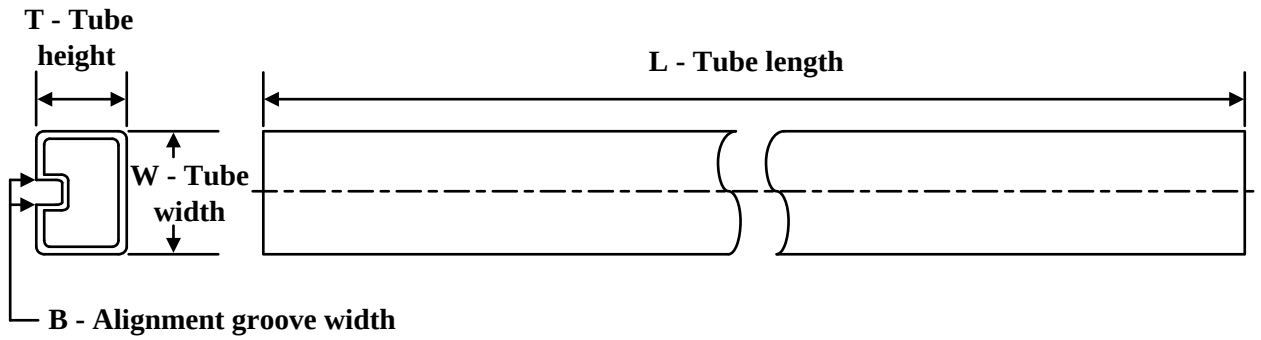
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
OPA2156IDGKR	VSSOP	DGK	8	2500	366.0	364.0	50.0
OPA2156IDGKR	VSSOP	DGK	8	2500	366.0	364.0	50.0
OPA2156IDGKT	VSSOP	DGK	8	250	366.0	364.0	50.0
OPA2156IDGKT	VSSOP	DGK	8	250	366.0	364.0	50.0
OPA2156IDR	SOIC	D	8	2500	353.0	353.0	32.0

TUBE



*All dimensions are nominal

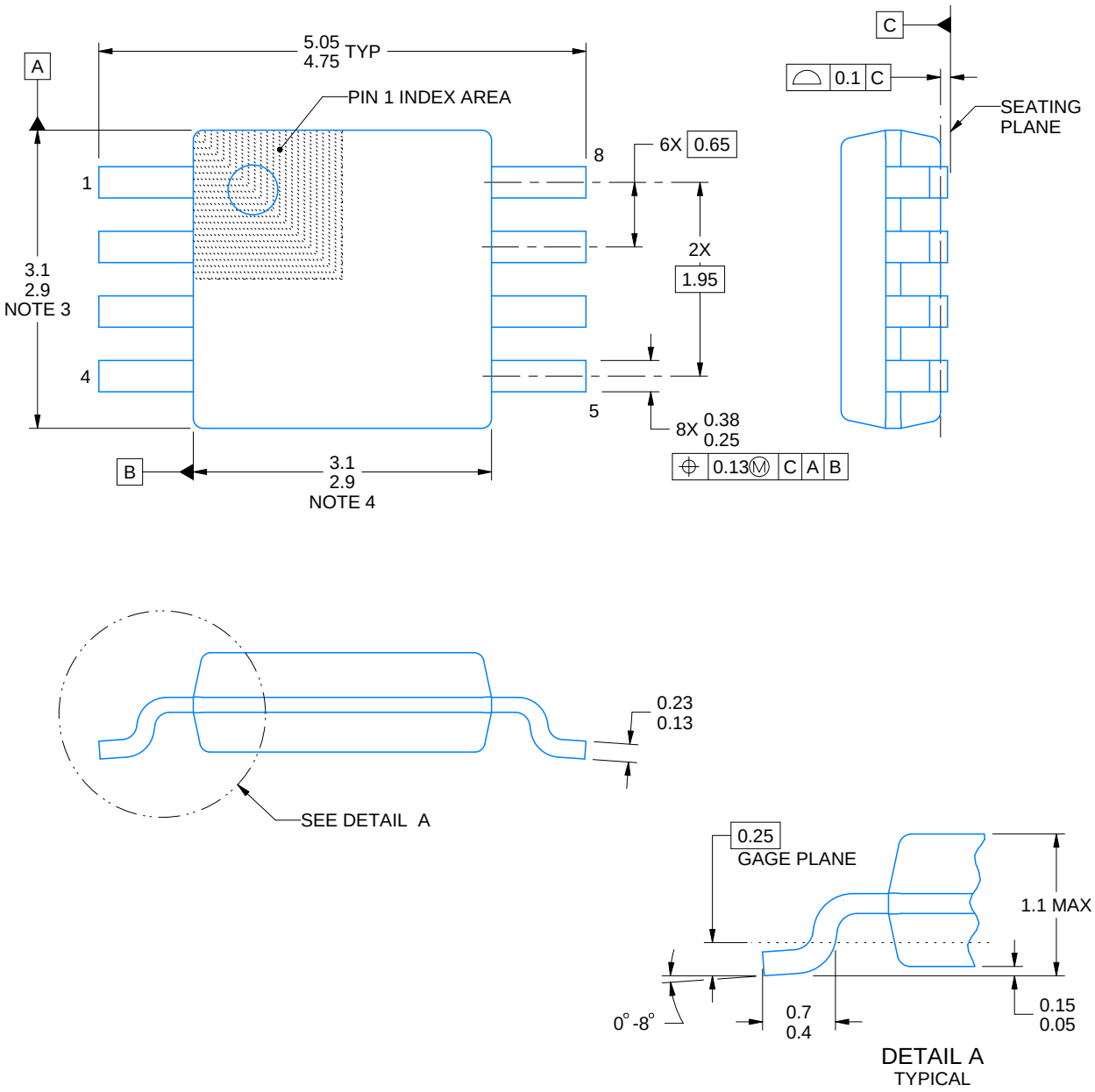
Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
OPA2156ID	D	SOIC	8	75	506.6	8	3940	4.32
OPA2156ID.A	D	SOIC	8	75	506.6	8	3940	4.32
OPA2156IDG4	D	SOIC	8	75	506.6	8	3940	4.32
OPA2156IDG4.A	D	SOIC	8	75	506.6	8	3940	4.32

PACKAGE OUTLINE

DGK0008A

VSSOP - 1.1 mm max height

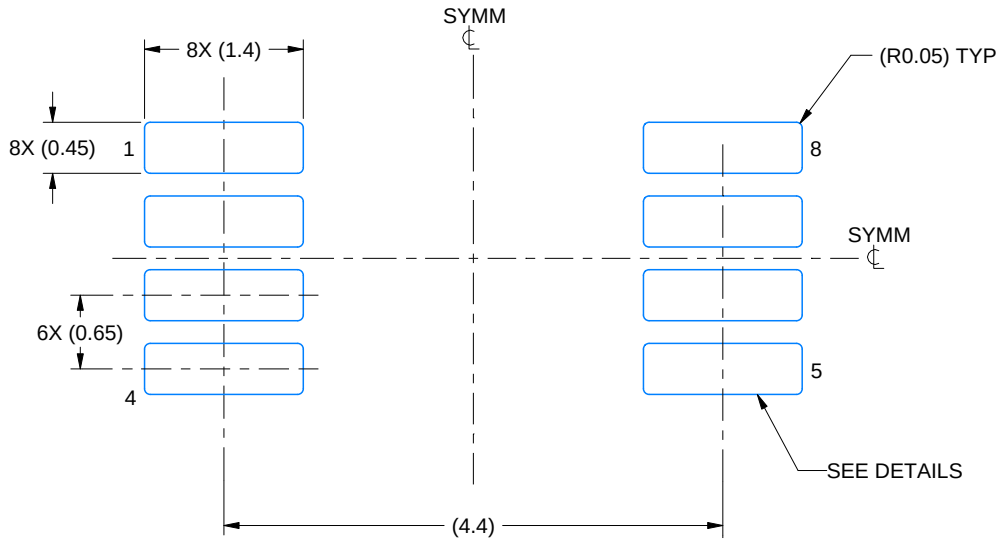
SMALL OUTLINE PACKAGE



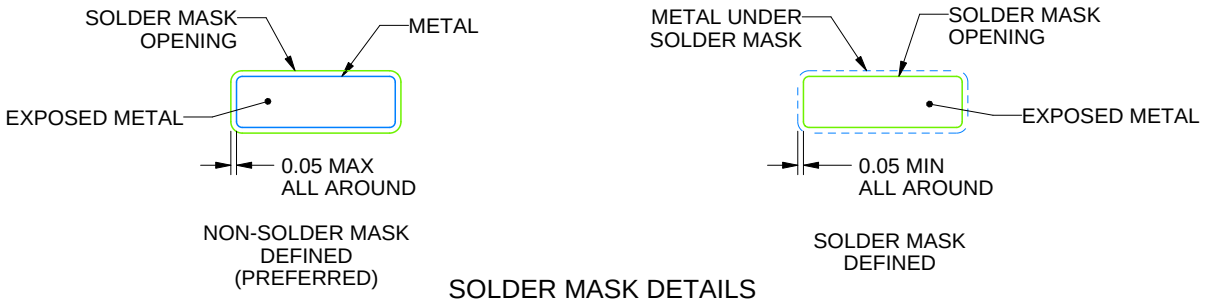
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X

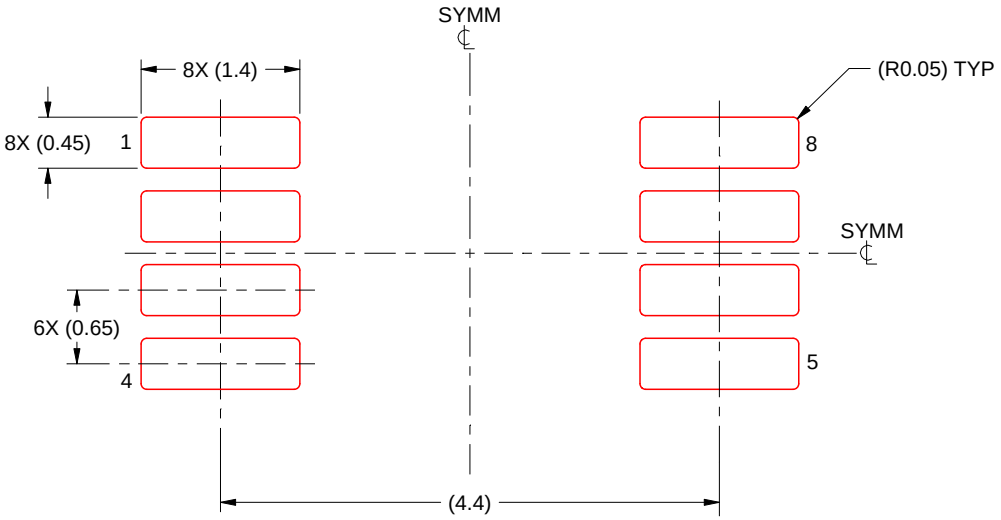


SOLDER MASK DETAILS

4214862/A 04/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.

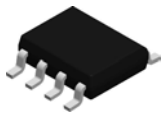


SOLDER PASTE EXAMPLE
SCALE: 15X

4214862/A 04/2023

NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

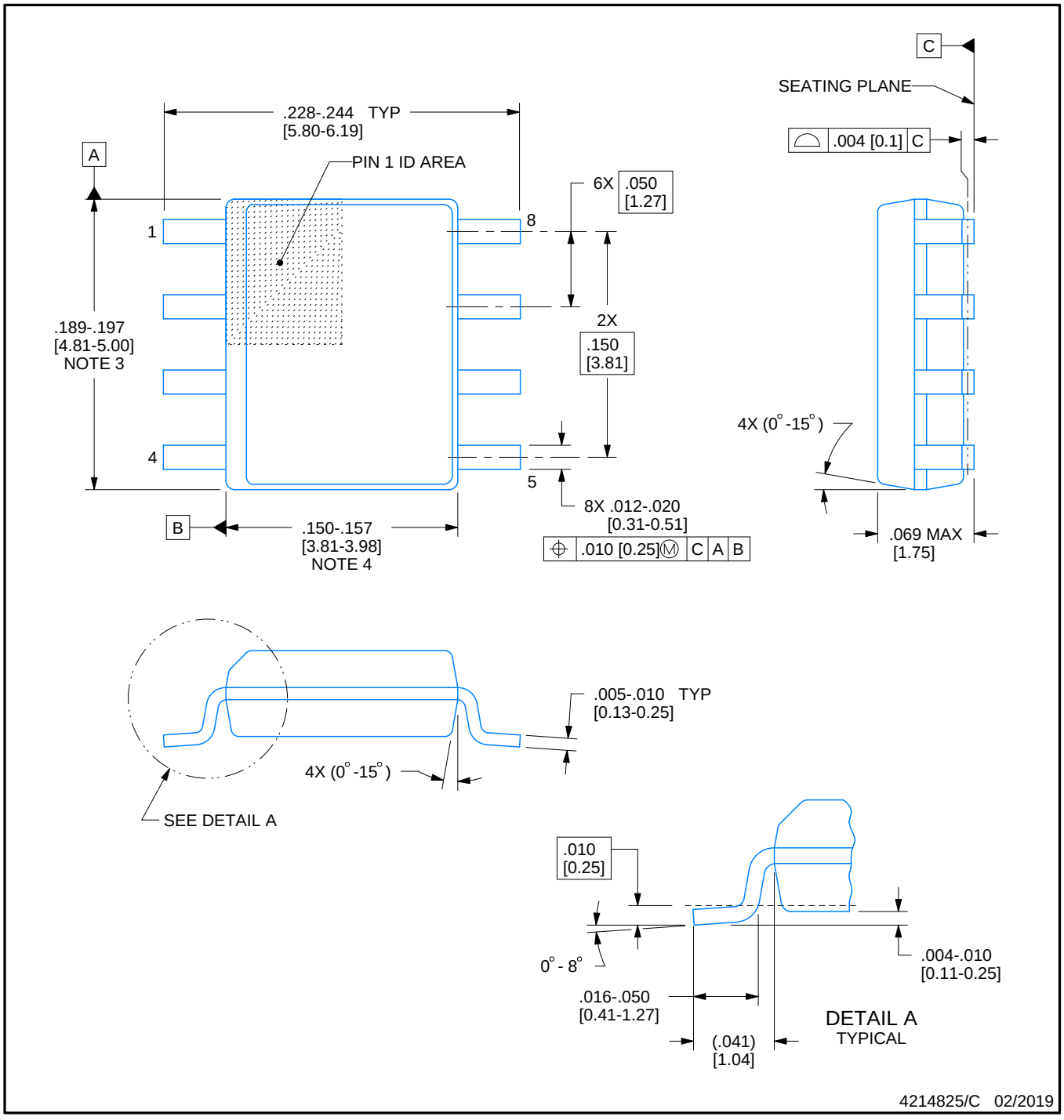


PACKAGE OUTLINE

D0008A

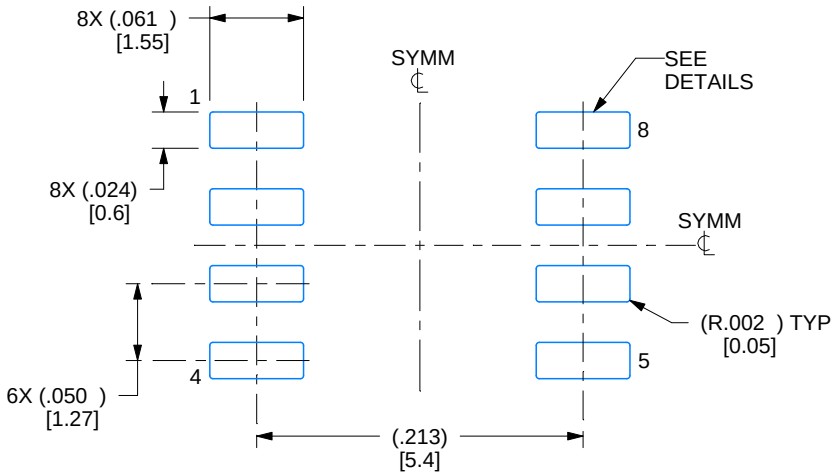
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

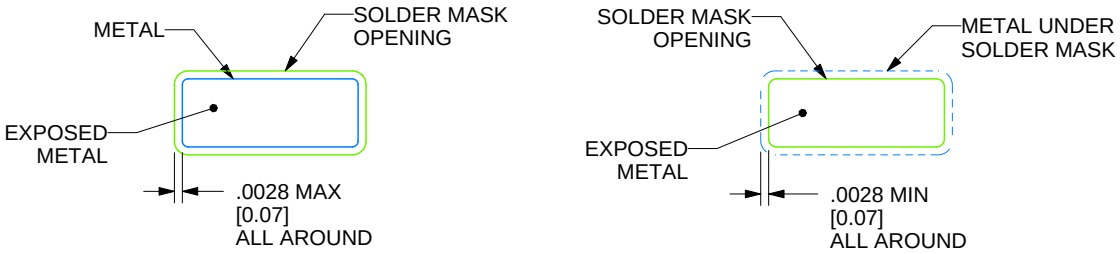


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

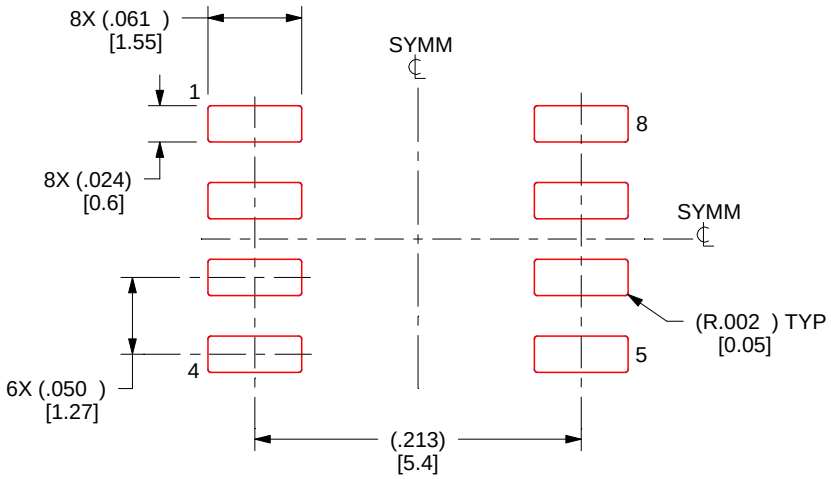
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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最后更新日期：2025 年 10 月