1.1nV/√Hz噪声、低功耗、精密运算放大器

查询样品: **OPA2211-HT**

特性

- 低电压噪声：**1kHz** 时为 **1.1nV/√Hz**
- 输入电压噪声：
  $80nV_{PP}$（**0.1Hz** 至 **10Hz**）
- 总谐波失真 **(THD)+N**：**-136dB (G=1**，**f=1kHz)**
- 偏移电压：**350μV**（最大值）
- 偏移电压漂移：**0.35μV/°C**（典型值）
- 低电源电流：每通道 **6mA**（最大值）
- 单位增益稳定
- 增益带宽产品：
  80MHz (G= 100)
  45MHz (G= 1)
- 转换速率：**27V/μs**
- **16** 位稳定时间：**700ns**
- 宽电源范围：
  ±2.25V 至 **±18V**，或者 **4.5V** 至 **36V**
- 轨至轨输出
- 输出电流：**30 mA**

应用范围

- 潜孔打钻
- 高温环境

支持极端温度环境下的应用

- 受控基线
- 一个组装**/**测试场所
- 一个制造场所
- 可在极端温度范围内 **(-55°C/150°C)** 工作 [(1)]
- 延长的产品生命周期
- 延长的产品变更通知
- 产品可追溯性
- 德州仪器 （**TI**） 高温产品利用高度优化的硅（芯片）解决方案，此解决方案对设计和制造工艺进行了提升以在拓展的温度范围内大大地提高性能。

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(1) 可定制工作温度范围

说明

OPA2211 精密运算放大器用一个电流只有 3.6mA 的电源电流实现极低 1.1nV/√Hz噪声密度。 这个器件还提供轨到轨输出摆幅，这大大增加了动态范围。

OPA2211 的极低电压和低电流噪声、高速度、和宽输出摆幅使得这些器件成为锁相环 (PLL) 应用中环路滤波放大器的理想选择。

在精准数据采集应用中，OPA2211 在整个 10V 输出摆幅内实现 16 位精度所需的稳定时间为 700ns。 这个交流性能，与温度范围内只有 240μV 的偏移和
0.35μV/°C 的漂移组合在一起，使得 OPA2211 成为驱动高精度 16 位模数转换器 (ADC) 或者缓冲高分辨率数模转换器 (DAC) 输出的理想选择。

OPA2211 可在 ±2.25V 至 ±18V 的宽双电源范围，或者 4.5V 至 36V 的单电源范围内运行。

这个运算放大器的额定温度范围 T_A= -55°C 至 150°C。

English Data Sheet: SBOS684

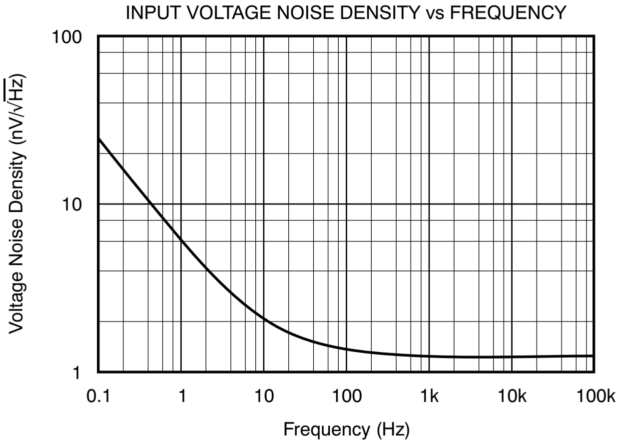


Table 1. ORDERING INFORMATION(1)

T_J	PACKAGE	ORDERABLE PART NUMBER	TOP-SIDE MARKING
–55°C to 150°C	PWP	OPA2211SPWP	OP2211S

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI Web site at www.ti.com.

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ABSOLUTE MAXIMUM RATINGS(1)

Over operating free-air temperature range (unless otherwise noted).

		VALUE	UNIT
Supply Voltage	V_S = (V+) – (V–)	40	V
Input Voltage		(V–) – 0.5 to (V+) + 0.5	V
Input Current (Any pin except power-supply pins)		±10	mA
Output Short-Circuit(2)		Continuous	
Storage Temperature, (T_S)		–65 to +165	°C
Junction Temperature, (T_J)		–55 to +165	°C
ESD Ratings	Human Body Model (HBM)	3000	V
	Charged Device Model (CDM)	1000	V

(1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not supported.

(2) Short-circuit to V_S/2 (ground in symmetrical dual supply setups), one amplifier per package.

THERMAL INFORMATION

THERMAL METRIC(1)		OPA2211-HT PWP 20 PINS	UNITS
θ_{JA}	Junction-to-ambient thermal resistance(2)	41.2	°C/W
θ_{JCtop}	Junction-to-case (top) thermal resistance(3)	21.4	
θ_{JB}	Junction-to-board thermal resistance(4)	23.9	
ψ_{JT}	Junction-to-top characterization parameter(5)	1.1	
ψ_{JB}	Junction-to-board characterization parameter(6)	23.7	
θ_{JCbot}	Junction-to-case (bottom) thermal resistance(7)	1.1	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

(2) The junction-to-ambient thermal resistance under natural convection is obtained in a simulation on a JEDEC-standard, high-K board, as specified in JESD51-7, in an environment described in JESD51-2a.

(3) The junction-to-case (top) thermal resistance is obtained by simulating a cold plate test on the package top. No specific JEDEC-standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.

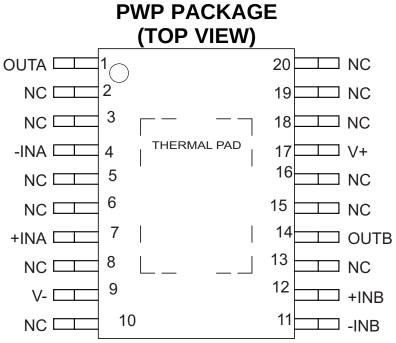
(4) The junction-to-board thermal resistance is obtained by simulating in an environment with a ring cold plate fixture to control the PCB temperature, as described in JESD51-8.

(5) The junction-to-top characterization parameter, ψ_{JT}, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining θ_{JA}, using a procedure described in JESD51-2a (sections 6 and 7).

(6) The junction-to-board characterization parameter, ψ_{JB}, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining θ_{JA} , using a procedure described in JESD51-2a (sections 6 and 7).

(7) The junction-to-case (bottom) thermal resistance is obtained by simulating a cold plate test on the exposed (power) pad. No specific JEDEC standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.

PIN CONFIGURATION



ELECTRICAL CHARACTERISTICS: V_S = ±2.25V to ±18V

BOLDFACE limits apply over the specified temperature range, T_J = –55°C to +150°C.
At T_J = +25°C, R_L = 10kΩ connected to midsupply, V_{CM} = V_{OUT} = midsupply, unless otherwise noted.

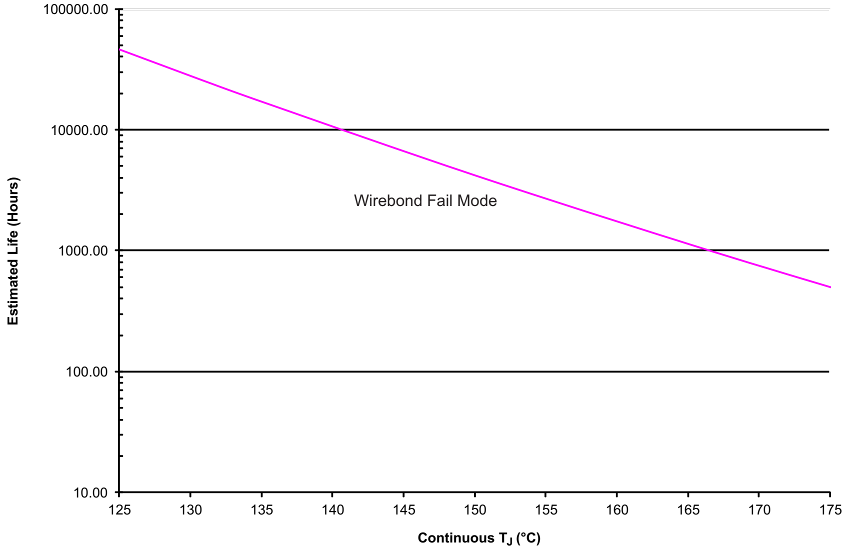
PARAMETER		CONDITIONS	Standard Grade OPA2211			UNIT
			MIN	TYP	MAX	
OFFSET VOLTAGE						
Input Offset Voltage	V_{OS}	V_S = ±15V		±50	±175	μV
Over Temperature					±350	μV
Drift	**dV_{OS}/dT**			**0.35**		**μV/°C**
vs Power Supply	PSRR	V_S = ±2.25V to ±18V		0.1	1	μV/V
Over Temperature					**3**	**μV/V**
INPUT BIAS CURRENT						
Input Bias Current	I_B	V_{CM} = 0V		±60	±215	nA
Over Temperature					**±350**	**nA**
Offset Current	I_{OS}	V_{CM} = 0V		±25	±120	nA
Over Temperature					**±200**	**nA**
NOISE						
Input Voltage Noise	e_n	f = 0.1Hz to 10Hz		80		nV_{PP}
Input Voltage Noise Density		f = 10Hz		2		nV/√Hz
		f = 100Hz		1.4		nV/√Hz
		f = 1kHz		1.1		nV/√Hz
Input Current Noise Density	I_n	f = 10Hz		3.2		pA/√Hz
		f = 1kHz		1.7		pA/√Hz
INPUT VOLTAGE RANGE						
Common-Mode Voltage Range[1]	V_{CM}	V_S ≥ ±5V	(V–) + 1.8		(V+) – 1.4	V
		V_S < ±5V	(V–) + 2		(V+) – 1.4	V
Common-Mode Rejection Ratio	**CMRR**	**V_S ≥ ±5V, (V–) + 2V ≤ V_{CM} ≤ (V+) – 2V**	**114**	**120**		**dB**
		V_S < ±5V, (V–) + 2V ≤ V_{CM} ≤ (V+) – 2V	**106**	**120**		**dB**
INPUT IMPEDANCE						
Differential				20k || 8		Ω || pF
Common-Mode				10^9 || 2		Ω || pF
OPEN-LOOP GAIN						
Open-Loop Voltage Gain	**A_{OL}**	**(V–) + 0.2V ≤ V_O ≤ (V+) – 0.2V, R_L = 10kΩ**	**114**	**130**		**dB**
	A_{OL}	(V–) + 0.6V ≤ V_O ≤ (V+) – 0.6V, R_L = 600Ω	110	114		dB
Over Temperature	**A_{OL}**	**(V–) + 0.6V ≤ V_O ≤ (V+) – 0.6V, I_O ≤ 15mA**	**100**			**dB**
FREQUENCY RESPONSE						
Gain-Bandwidth Product	GBW	G = 100		80		MHz
		G = 1		45		MHz
Slew Rate	SR			27		V/μs
Settling Time, 0.01%	t_S	V_S = ±15V, G = –1, 10V Step, C_L = 100pF		400		ns
0.0015% (16-bit)		V_S = ±15V, G = –1, 10V Step, C_L = 100pF		700		ns
Overload Recovery Time		G = –10		500		ns
Total Harmonic Distortion + Noise	THD+N	G = +1, f = 1kHz, V_O = $3V_{RMS}$, R_L = 600Ω		0.000015		%
				–136		dB

(1) The OPA2211-HT is not intended to be used as a comparator due to its limited differential input range capability. Refer to the INPUT PROTECTION section of this data sheet.

ELECTRICAL CHARACTERISTICS: V_S = ±2.25V to ±18V (continued)

BOLDFACE limits apply over the specified temperature range, T_J = –55°C to +150°C.
At T_J = +25°C, R_L = 10kΩ connected to midsupply, V_{CM} = V_{OUT} = midsupply, unless otherwise noted.

PARAMETER		CONDITIONS	Standard Grade OPA2211 MIN	TYP	MAX	UNIT
OUTPUT						
Voltage Output	V_{OUT}	**R_L = 10kΩ, A_{OL} ≥ 114dB**	**(V–) + 0.2**		**(V+) – 0.2**	**V**
		R_L = 600Ω, A_{OL} ≥ 110dB	(V–) + 0.6		(V+) – 0.6	V
		I_O < 15mA, A_{OL} ≥ 100dB	**(V–) + 0.6**		**(V+) – 0.6**	**V**
Short-Circuit Current	I_{SC}			+30/–45		mA
Capacitive Load Drive	C_{LOAD}		See Typical Characteristics			pF
Open-Loop Output Impedance	Z_O	f = 1MHz		5		Ω
POWER SUPPLY						
Specified Voltage	V_S		±2.25		±18	V
Quiescent Current (per channel)	I_Q	I_{OUT} = 0A		3.6	4.5	mA
Over Temperature					**6**	**mA**
TEMPERATURE RANGE						
Specified Range		T_A	–55		+150	°C
Operating Range		T_A	–55		+150	°C



(1) See Datasheet for Absolute Maximum and Minimum Recommended Operating Conditions.

(2) Silicon operating life design goal is 10 years at 105°C junction temperature (does not include package interconnect life).

(3) The predicted operating lifetime vs. junction temperature is based on reliability modeling and available qualification data.

(4) Device is qualified for 1000 hour operation at 150°C. Device is functional at 175°C, but at reduced operating life.

Figure 1. OPA2211-HT Wirebond Life Derating Chart

TYPICAL CHARACTERISTICS

At T_A = +25°C, V_S = ±18V, and R_L = 10kΩ, unless otherwise noted.

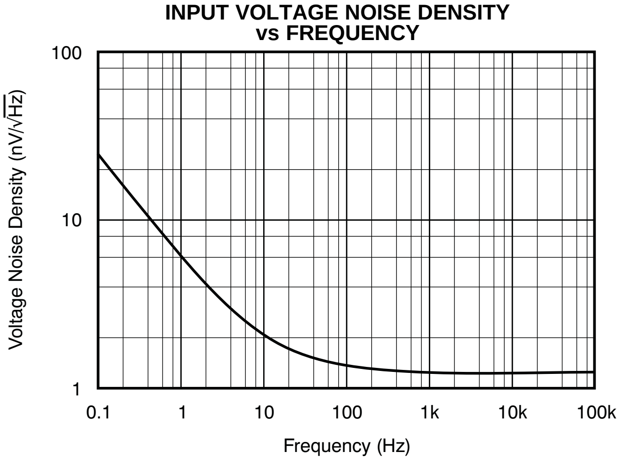


Figure 2.

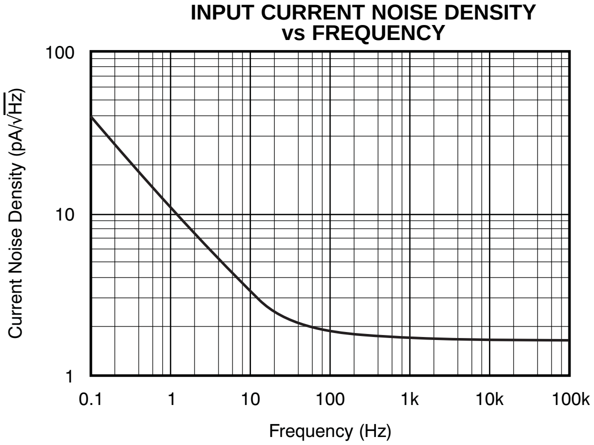


Figure 3.

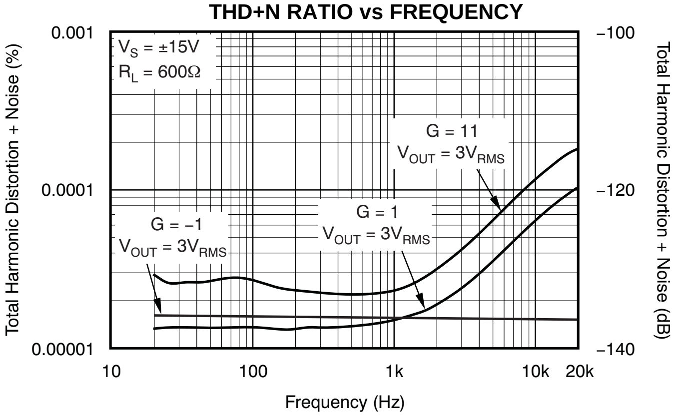


Figure 4.

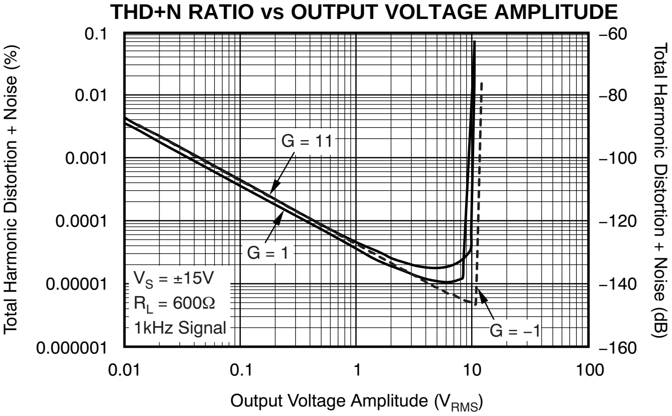


Figure 5.

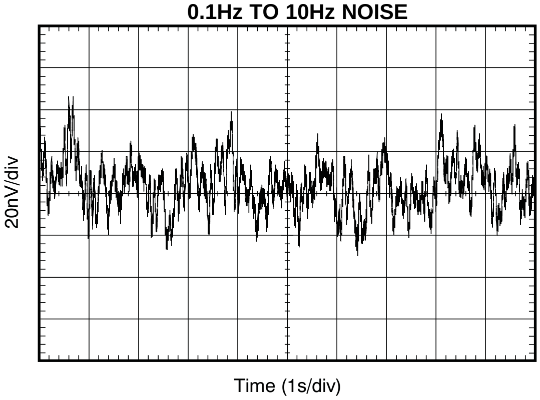


Figure 6.

TYPICAL CHARACTERISTICS (continued)

At T_A = +25°C, V_S = ±18V, and R_L = 10kΩ, unless otherwise noted.

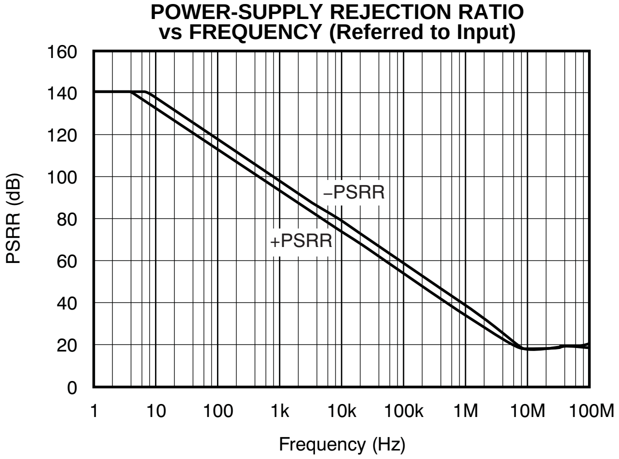


Figure 7.

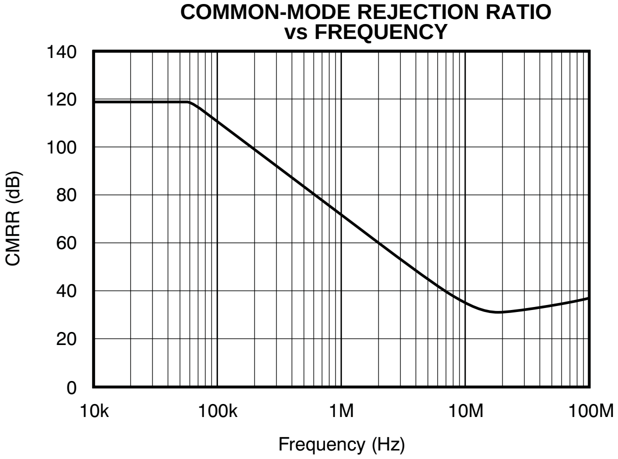


Figure 8.

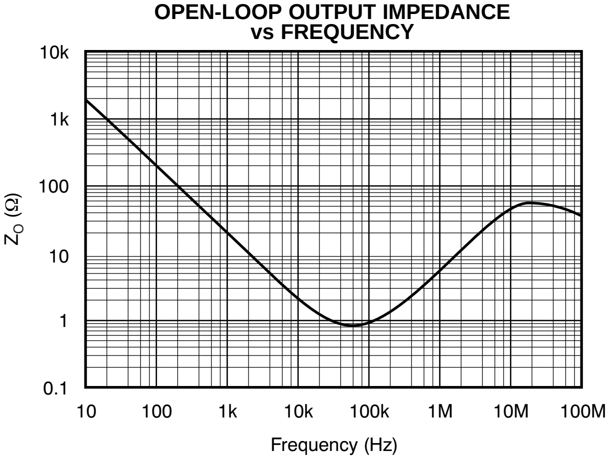


Figure 9.

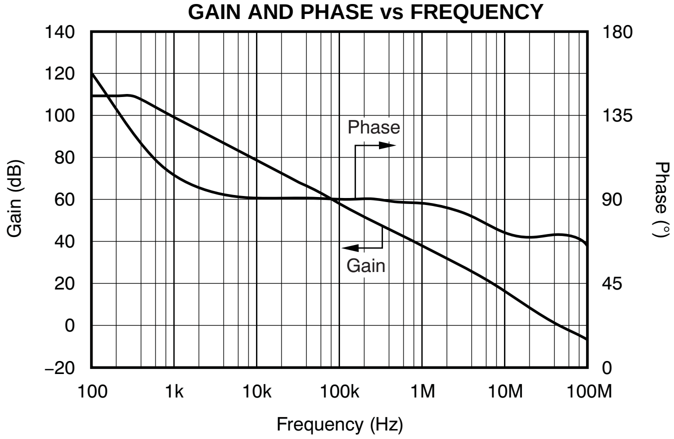


Figure 10.

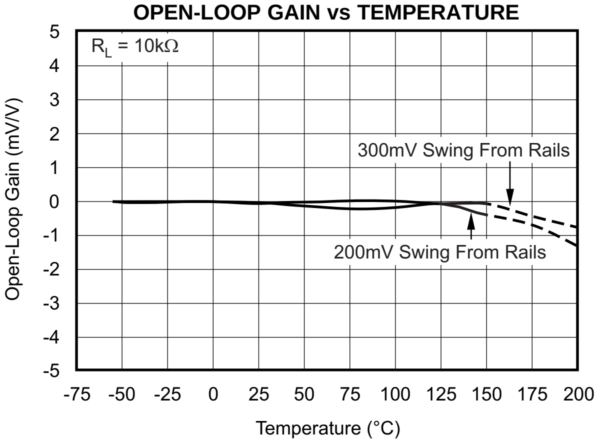


Figure 11.

TYPICAL CHARACTERISTICS (continued)

At T_A = +25°C, V_S = ±18V, and R_L = 10kΩ, unless otherwise noted.

OFFSET VOLTAGE PRODUCTION DISTRIBUTION

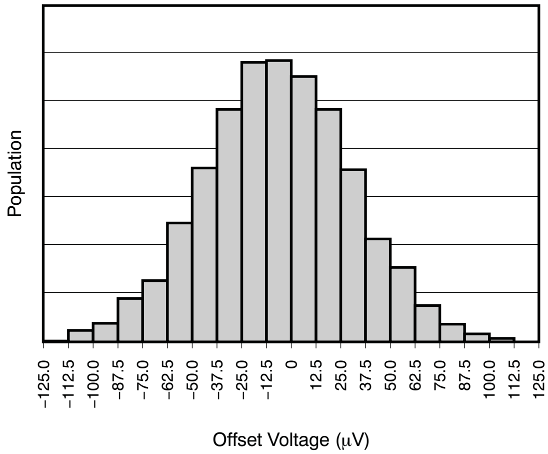


Figure 12.

OFFSET VOLTAGE DRIFT PRODUCTION DISTRIBUTION

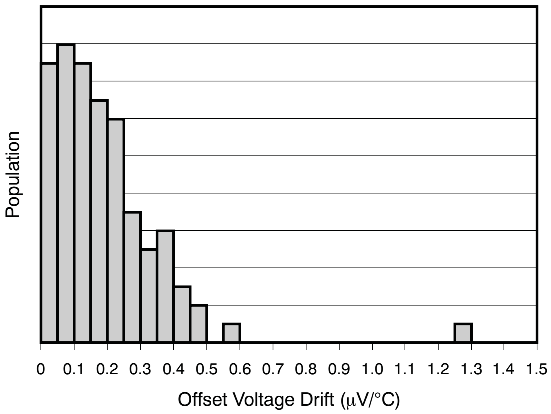


Figure 13.

I_B AND I_{OS} CURRENT vs TEMPERATURE

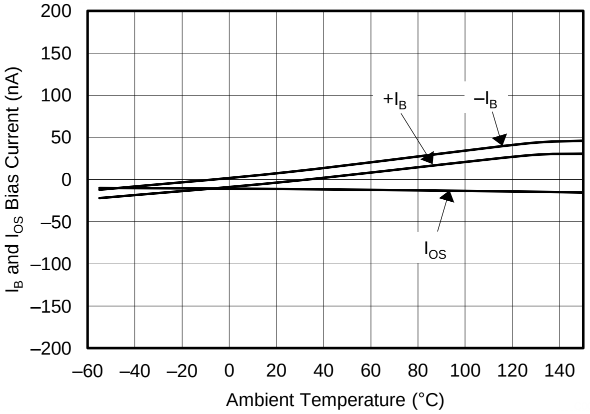


Figure 14.

OFFSET VOLTAGE vs COMMON-MODE VOLTAGE

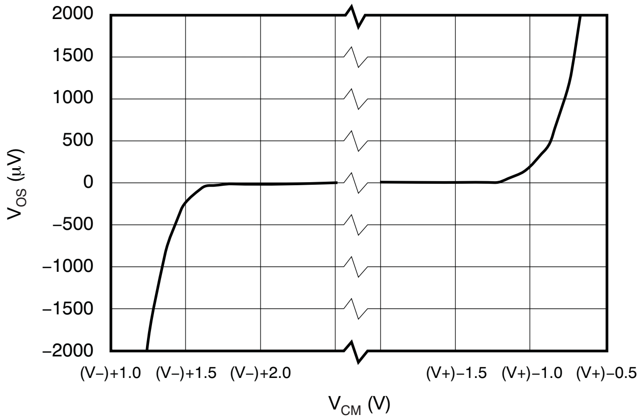


Figure 15.

V_{OS} WARMUP

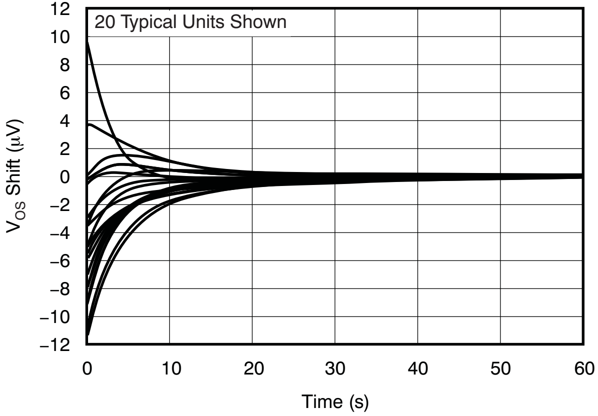


Figure 16.

INPUT OFFSET CURRENT vs SUPPLY VOLTAGE

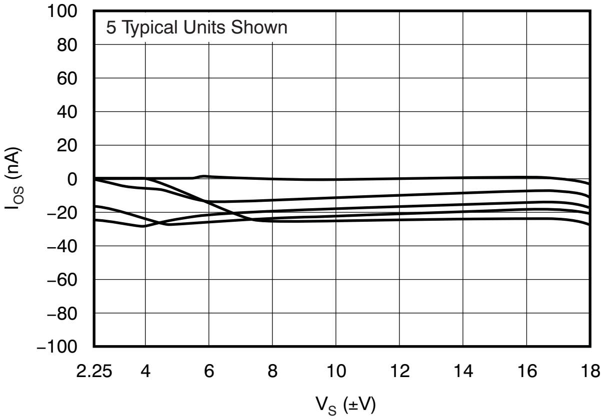


Figure 17.

TYPICAL CHARACTERISTICS (continued)

At T_A = +25°C, V_S = ±18V, and R_L = 10kΩ, unless otherwise noted.

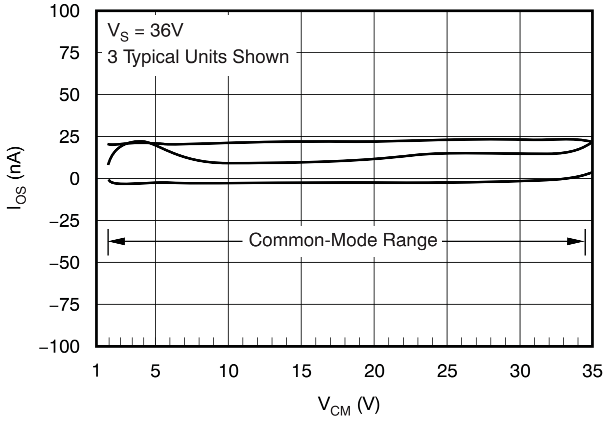

INPUT OFFSET CURRENT vs COMMON-MODE VOLTAGE

Figure 18.

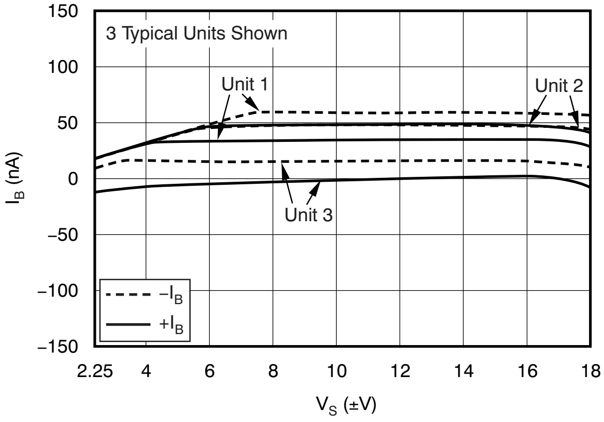

INPUT BIAS CURRENT vs SUPPLY VOLTAGE

Figure 19.

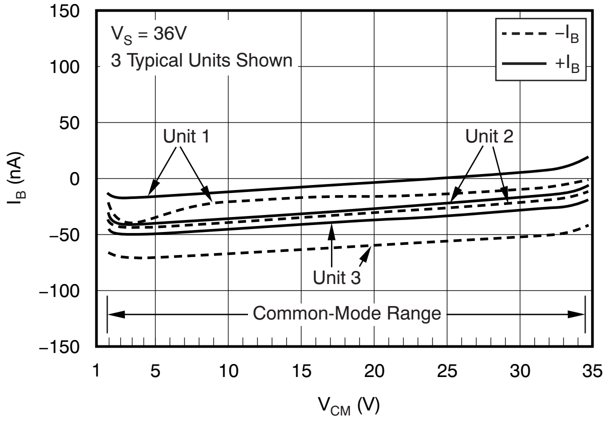

INPUT BIAS CURRENT vs COMMON-MODE VOLTAGE

Figure 20.

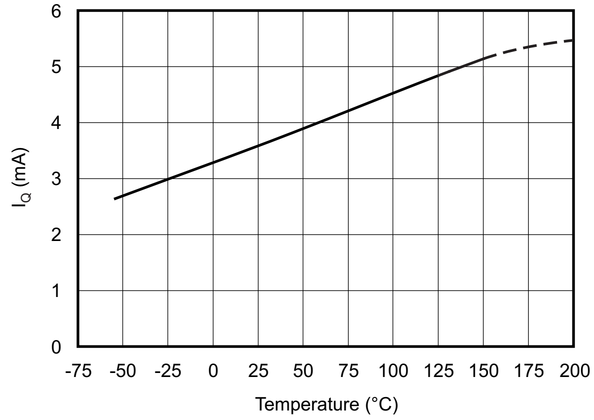

QUIESCENT CURRENT vs TEMPERATURE

Figure 21.

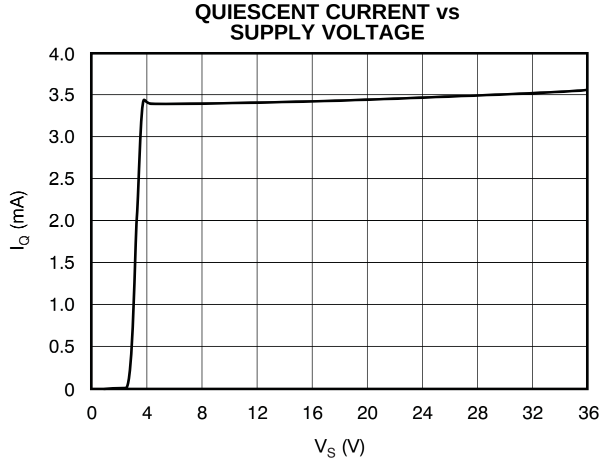

QUIESCENT CURRENT vs SUPPLY VOLTAGE

Figure 22.

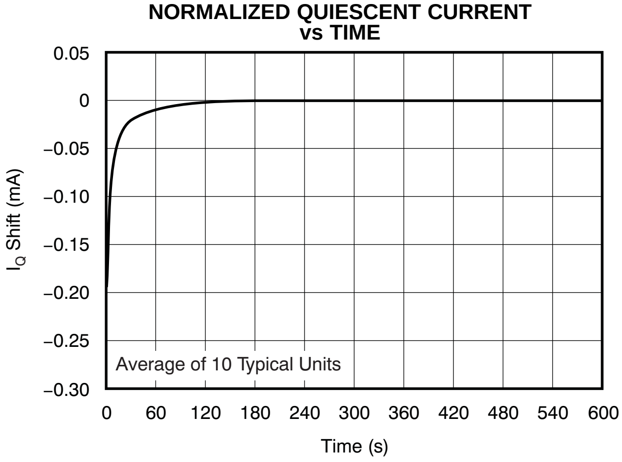

NORMALIZED QUIESCENT CURRENT vs TIME

Figure 23.

TYPICAL CHARACTERISTICS (continued)

At T_A = +25°C, V_S = ±18V, and R_L = 10kΩ, unless otherwise noted.

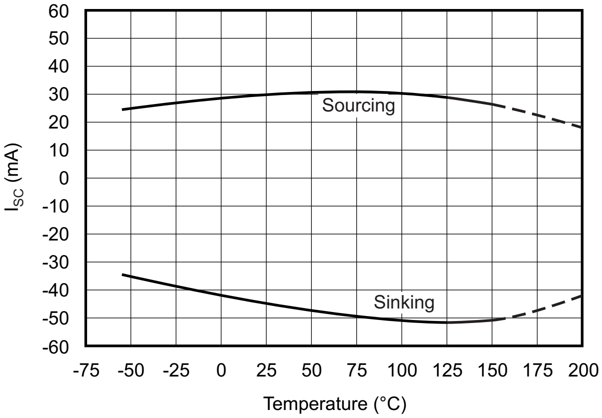

SHORT-CIRCUIT CURRENT vs TEMPERATURE

Figure 24.

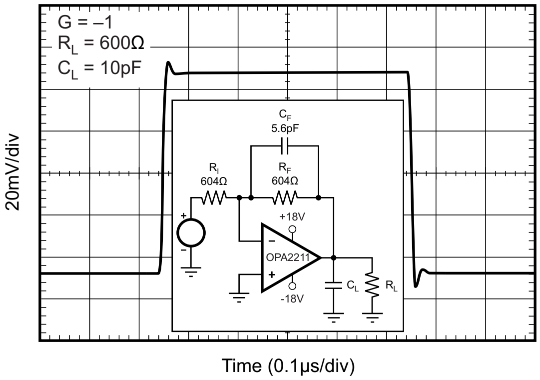

SMALL-SIGNAL STEP RESPONSE (100mV)

Figure 25.

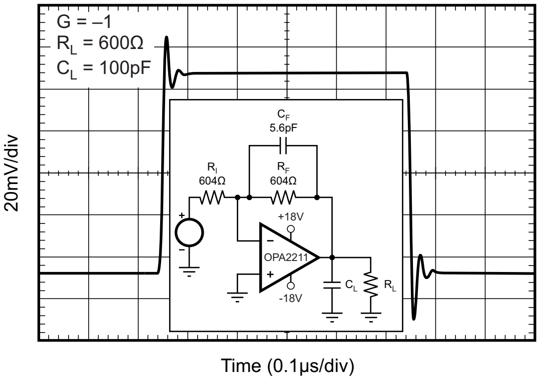

SMALL-SIGNAL STEP RESPONSE (100mV)

Figure 26.

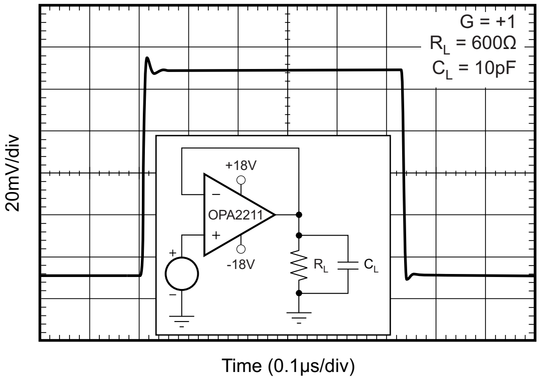

SMALL-SIGNAL STEP RESPONSE (100mV)

Figure 27.

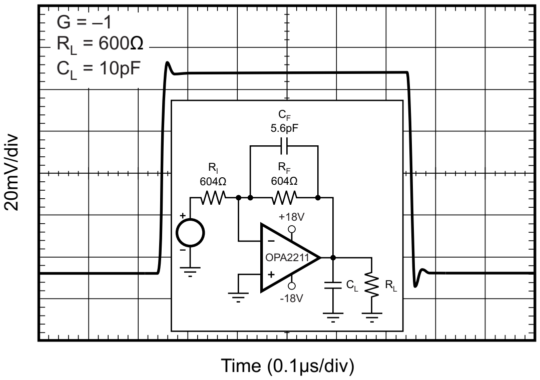

SMALL-SIGNAL STEP RESPONSE (100mV)

Figure 28.

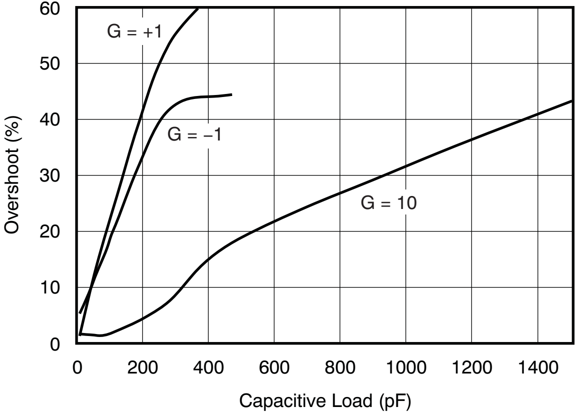

SMALL-SIGNAL OVERSHOOT vs CAPACITIVE LOAD (100mV Output Step)

Figure 29.

TYPICAL CHARACTERISTICS (continued)

At T_A = +25°C, V_S = ±18V, and R_L = 10kΩ, unless otherwise noted.

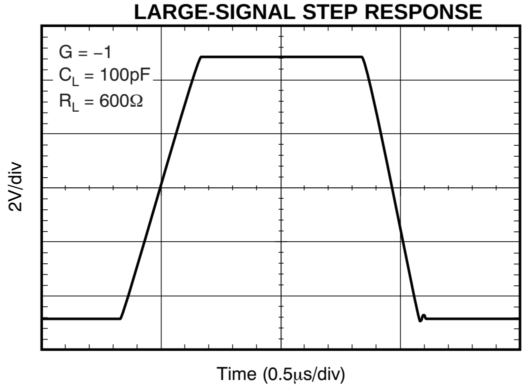
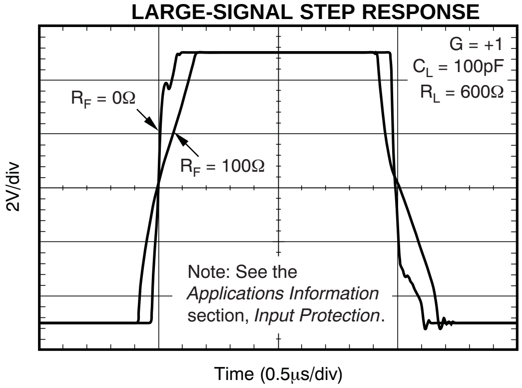


Figure 30.



Note: See the *Applications Information* section, *Input Protection*.

Figure 31.

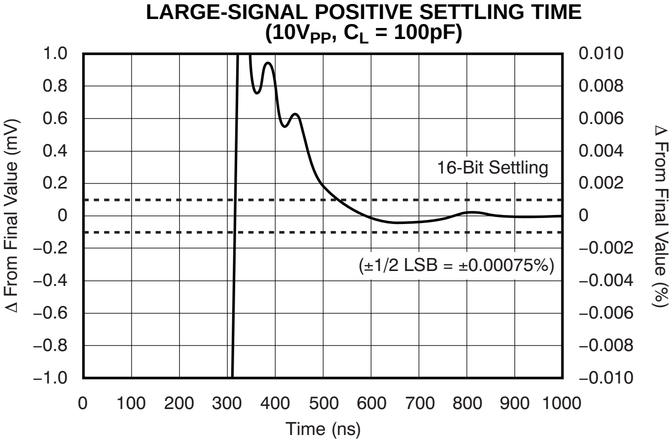


Figure 32.

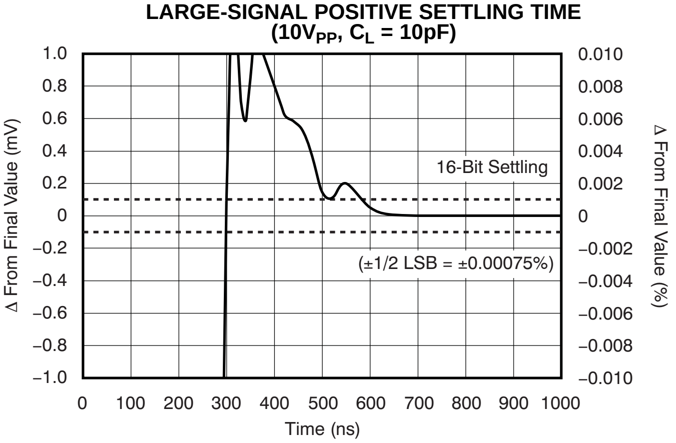


Figure 33.

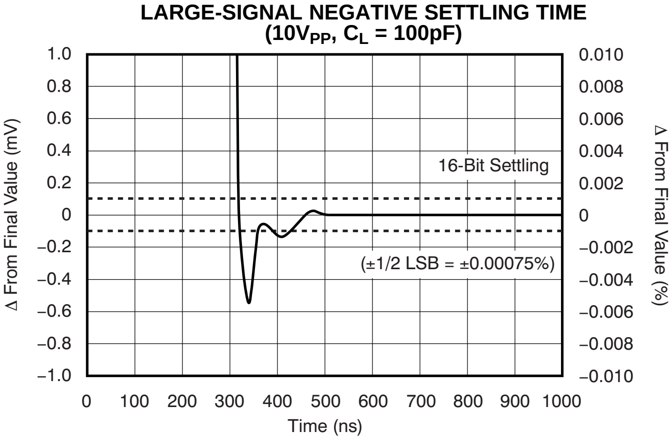


Figure 34.

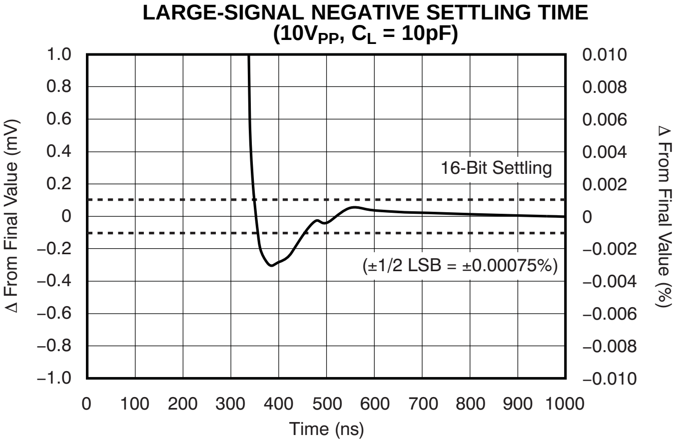


Figure 35.

TYPICAL CHARACTERISTICS (continued)

At T_A = +25°C, V_S = ±18V, and R_L = 10kΩ, unless otherwise noted.

NEGATIVE OVERLOAD RECOVERY

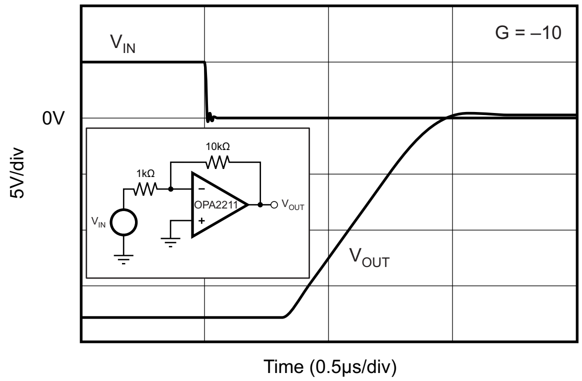


Figure 36.

POSITIVE OVERLOAD RECOVERY

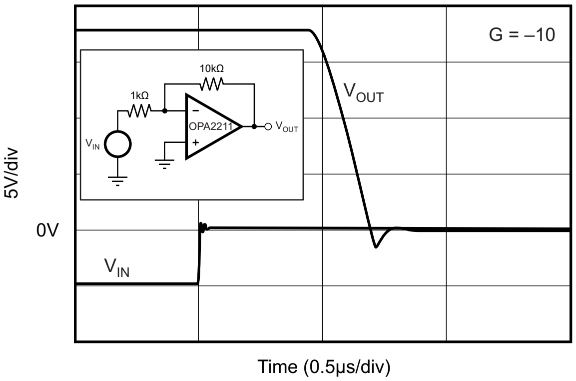


Figure 37.

OUTPUT VOLTAGE vs OUTPUT CURRENT

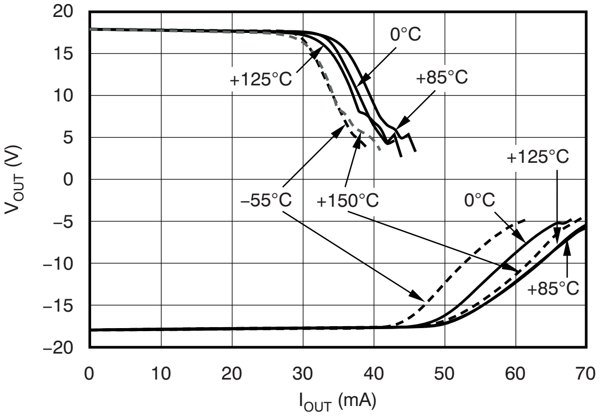


Figure 38.

NO PHASE REVERSAL

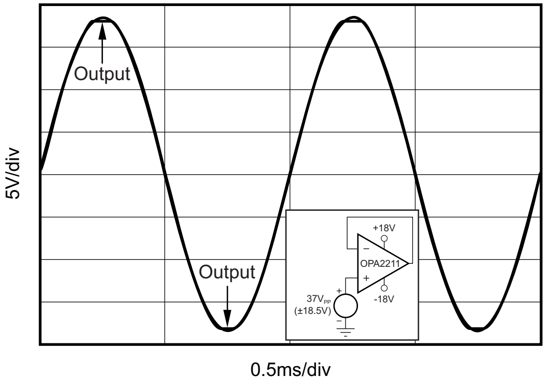


Figure 39.

APPLICATION INFORMATION

The OPA2211 is a unity-gain stable, precision op amp with very low noise. Applications with noisy or high-impedance power supplies require decoupling capacitors close to the device pins. In most cases, 0.1μF capacitors are adequate. Figure 40 shows a simplified schematic of the OPA2211. This die uses a SiGe bipolar process and contains 180 transistors.

OPERATING VOLTAGE

OPA2211 series op amps operate from ±2.25V to ±18V supplies while maintaining excellent performance. The OPA2211 series can operate with as little as +4.5V between the supplies and with up to +36V between the supplies. However, some applications do not require equal positive and negative output voltage swing. With the OPA2211 series, power-supply voltages do not need to be equal. For example, the positive supply could be set to +25V with the negative supply at –5V or vice-versa.

The common-mode voltage must be maintained within the specified range. In addition, key parameters are assured over the specified temperature range, T_J = –55°C to +150°C. Parameters that vary significantly with operating voltage or temperature are shown in the Typical Characteristics.

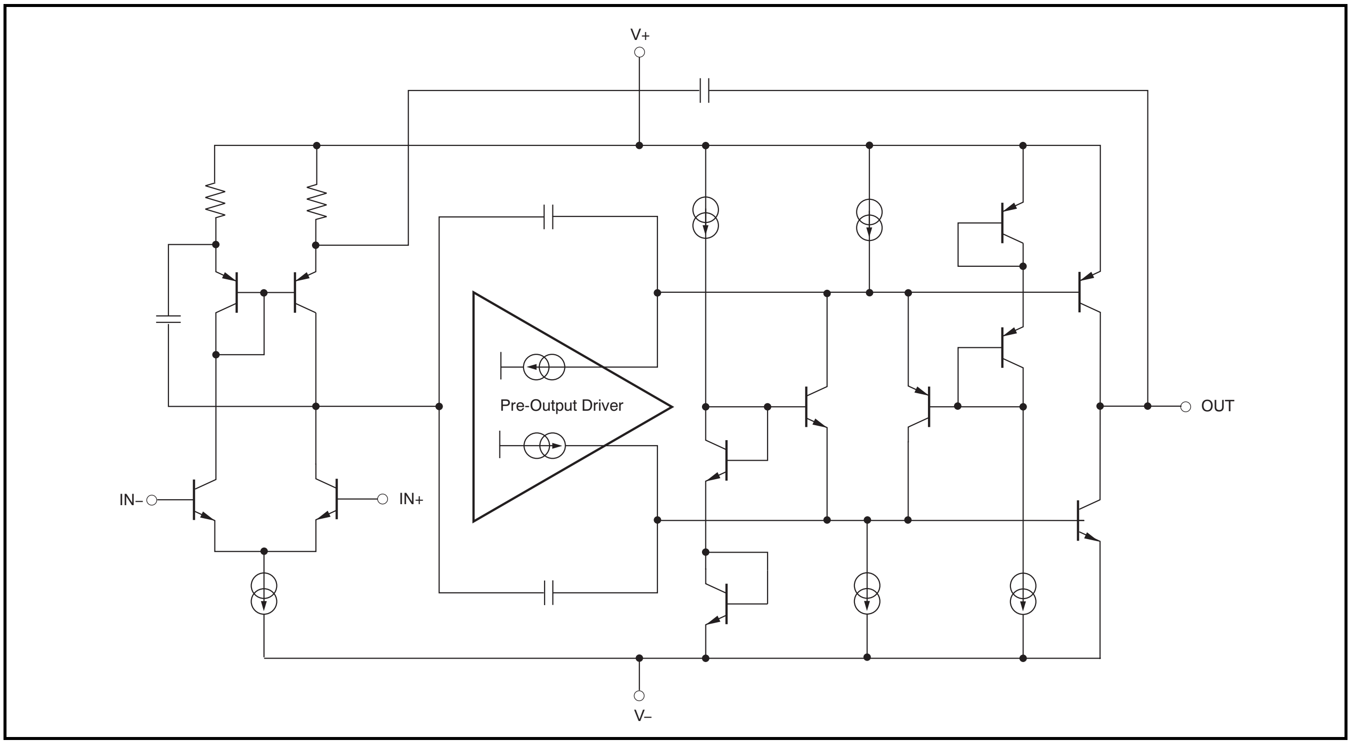


Figure 40. OPA2211 Simplified Schematic

INPUT PROTECTION

The input terminals of the OPA2211 are protected from excessive differential voltage with back-to-back diodes, as shown in Figure 41. In most circuit applications, the input protection circuitry has no consequence. However, in low-gain or G = 1 circuits, fast ramping input signals can forward bias these diodes because the output of the amplifier cannot respond rapidly enough to the input ramp. This effect is illustrated in Figure 31 of the Typical Characteristics. If the input signal is fast enough to create this forward bias condition, the input signal current must be limited to 10mA or less. If the input signal current is not inherently limited, an input series resistor can be used to limit the signal input current. This input series resistor degrades the low-noise performance of the OPA2211, and is discussed in the *Noise Performance* section of this data sheet. Figure 41 shows an example implementing a current-limiting feedback resistor.

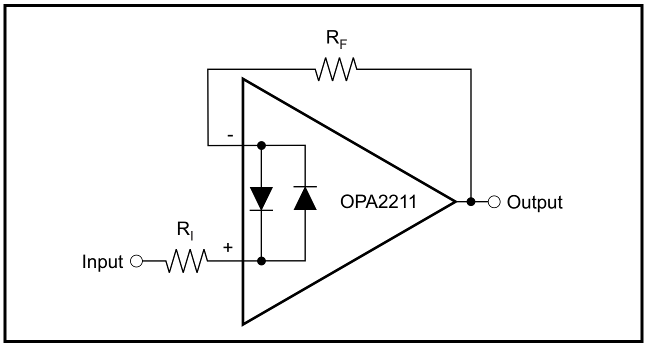


Figure 41. Pulsed Operation

NOISE PERFORMANCE

Figure 42 shows total circuit noise for varying source impedances with the op amp in a unity-gain configuration (no feedback resistor network, and therefore no additional noise contributions). Two different op amps are shown with total circuit noise calculated. The OPA2211 has very low voltage noise, making it ideal for low source impedances (less than 2kΩ). A similar precision op amp, the OPA227, has somewhat higher voltage noise but lower current noise. It provides excellent noise performance at moderate source impedance (10kΩ to 100kΩ). Above 100kΩ, a FET-input op amp such as the OPA132 (very low current noise) may provide improved performance. The equation in Figure 42 is shown for the calculation of the total circuit noise. Note that e_n = voltage noise, I_n = current noise, R_S = source impedance, k = Boltzmann's constant = 1.38 × 10^{-23} J/K, and T is temperature in K.

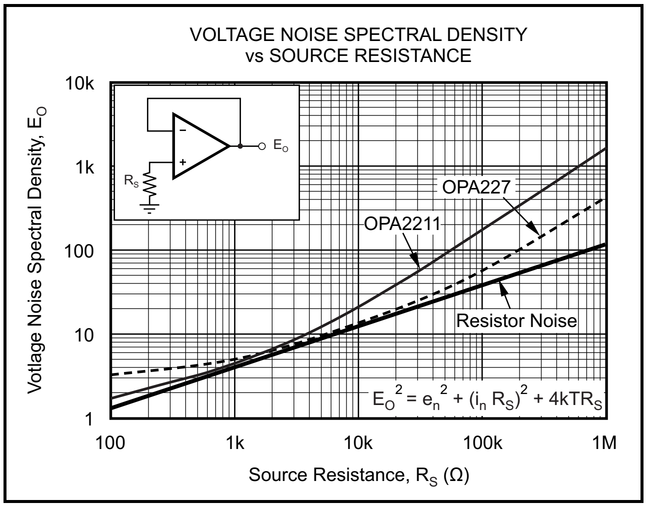


Figure 42. Noise Performance of the OPA2211 and OPA227 in Unity-Gain Buffer Configuration

BASIC NOISE CALCULATIONS

Design of low-noise op amp circuits requires careful consideration of a variety of possible noise contributors: noise from the signal source, noise generated in the op amp, and noise from the feedback network resistors. The total noise of the circuit is the root-sum-square combination of all noise components.

The resistive portion of the source impedance produces thermal noise proportional to the square root of the resistance. This function is plotted in Figure 42. The source impedance is usually fixed; consequently, select the op amp and the feedback resistors to minimize the respective contributions to the total noise.

Figure 42 depicts total noise for varying source impedances with the op amp in a unity-gain configuration (no feedback resistor network, and therefore no additional noise contributions). The operational amplifier itself contributes both a voltage noise component and a current noise component. The voltage noise is commonly modeled as a time-varying component of the offset voltage. The current noise is modeled as the time-varying component of the input bias current and reacts with the source resistance to create a voltage component of noise. Therefore, the lowest noise op amp for a given application depends on the source impedance. For low source impedance, current noise is negligible and voltage noise generally dominates. For high source impedance, current noise may dominate.

illustrates both inverting and noninverting op amp circuit configurations with gain. In circuit configurations with gain, the feedback network resistors also contribute noise. The current noise of the op amp reacts with the feedback resistors to create additional noise components. The feedback resistor values can generally be chosen to make these noise sources negligible. The equations for total noise are shown for both configurations.

TOTAL HARMONIC DISTORTION MEASUREMENTS

OPA2211 series op amps have excellent distortion characteristics. THD + Noise is below 0.0001% (G = +1, V_O = $3V_{RMS}$) throughout the audio frequency range, 20Hz to 20kHz, with a 600Ω load.

The distortion produced by OPA2211 series op amps is below the measurement limit of many commercially available distortion analyzers. However, a special test circuit illustrated in can be used to extend the measurement capabilities.

Op amp distortion can be considered an internal error source that can be referred to the input. shows a circuit that causes the op amp distortion to be 101 times greater than that normally produced by the op amp. The addition of R_3 to the otherwise standard noninverting amplifier configuration alters the feedback factor or noise gain of the circuit. The closed-loop gain is unchanged, but the feedback available for error correction is reduced by a factor of 101, thus extending the resolution by 101. Note that the input signal and load applied to the op amp are the same as with conventional feedback without R_3. The value of R_3 should be kept small to minimize its effect on the distortion measurements.

Validity of this technique can be verified by duplicating measurements at high gain and/or high frequency where the distortion is within the measurement capability of the test equipment. Measurements for this data sheet were made with an Audio Precision System Two distortion/noise analyzer, which greatly simplifies such repetitive measurements. The measurement technique can, however, be performed with manual distortion measurement instruments.

ELECTRICAL OVERSTRESS

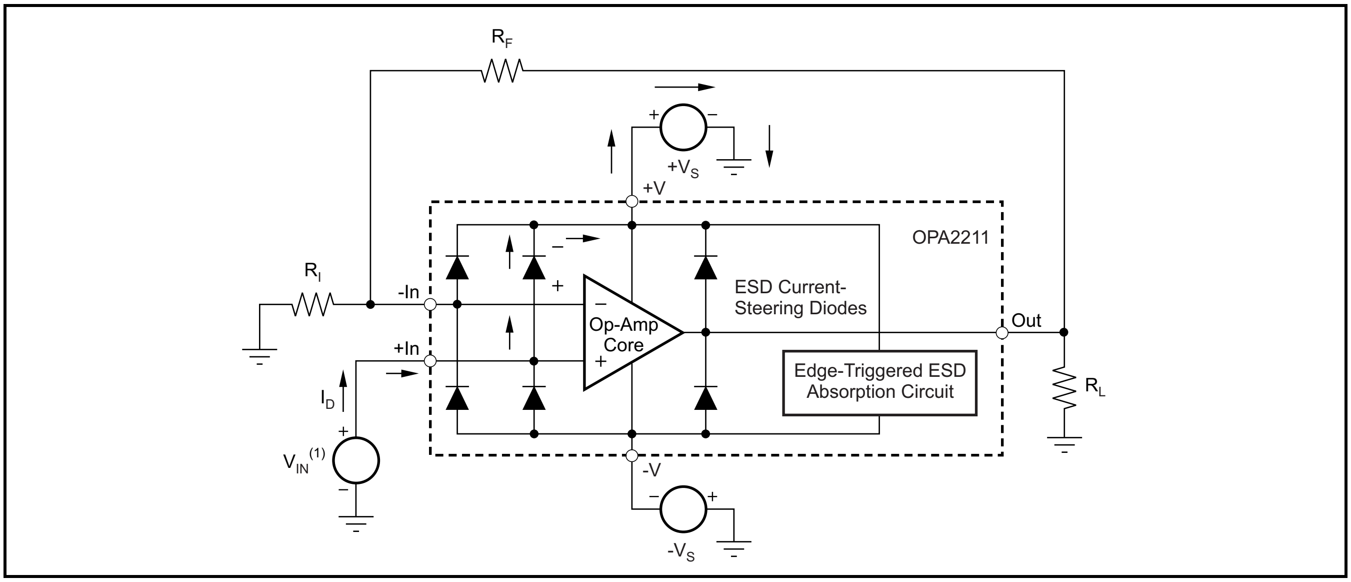
Designers often ask questions about the capability of an operational amplifier to withstand electrical overstress. These questions tend to focus on the device inputs, but may involve the supply voltage pins or even the output pin. Each of these different pin functions have electrical stress limits determined by the voltage breakdown characteristics of the particular semiconductor fabrication process and specific circuits connected to the pin. Additionally, internal electrostatic discharge (ESD) protection is built into these circuits to protect them from accidental ESD events both before and during product assembly.

It is helpful to have a good understanding of this basic ESD circuitry and its relevance to an electrical overstress event. Figure 43 illustrates the ESD circuits contained in the OPA2211 (indicated by the dashed line area). The ESD protection circuitry involves several current-steering diodes connected from the input and output pins and routed back to the internal power-supply lines, where they meet at an absorption device internal to the operational amplifier. This protection circuitry is intended to remain inactive during normal circuit operation.

An ESD event produces a short duration, high-voltage pulse that is transformed into a short duration, high-current pulse as it discharges through a semiconductor device. The ESD protection circuits are designed to provide a current path around the operational amplifier core to prevent it from being damaged. The energy absorbed by the protection circuitry is then dissipated as heat.

When an ESD voltage develops across two or more of the amplifier device pins, current flows through one or more of the steering diodes. Depending on the path that the current takes, the absorption device may activate. The absorption device has a trigger, or threshold voltage, that is above the normal operating voltage of the OPA2211 but below the device breakdown voltage level. Once this threshold is exceeded, the absorption device quickly activates and clamps the voltage across the supply rails to a safe level.

When the operational amplifier connects into a circuit such as that illustrated in Figure 43, the ESD protection components are intended to remain inactive and not become involved in the application circuit operation. However, circumstances may arise where an applied voltage exceeds the operating voltage range of a given pin. Should this condition occur, there is a risk that some of the internal ESD protection circuits may be biased on, and conduct current. Any such current flow occurs through steering diode paths and rarely involves the absorption device.



(1) $V_{IN} = +V_S + 500mV$.

Figure 43. Equivalent Internal ESD Circuitry and Its Relation to a Typical Circuit Application

Figure 43 depicts a specific example where the input voltage, V_{IN}, exceeds the positive supply voltage ($+V_S$) by 500mV or more. Much of what happens in the circuit depends on the supply characteristics. If $+V_S$ can sink the current, one of the upper input steering diodes conducts and directs current to $+V_S$. Excessively high current levels can flow with increasingly higher V_{IN}. As a result, the datasheet specifications recommend that applications limit the input current to 10mA.

If the supply is not capable of sinking the current, V_{IN} may begin sourcing current to the operational amplifier, and then take over as the source of positive supply voltage. The danger in this case is that the voltage can rise to levels that exceed the operational amplifier absolute maximum ratings. In extreme but rare cases, the absorption device triggers on while $+V_S$ and $–V_S$ are applied. If this event happens, a direct current path is established between the $+V_S$ and $–V_S$ supplies. The power dissipation of the absorption device is quickly exceeded, and the extreme internal heating destroys the operational amplifier.

Another common question involves what happens to the amplifier if an input signal is applied to the input while the power supplies $+V_S$ and/or $–V_S$ are at 0V. Again, it depends on the supply characteristic while at 0V, or at a level below the input signal amplitude. If the supplies appear as high impedance, then the operational amplifier supply current may be supplied by the input source via the current steering diodes. This state is not a normal bias condition; the amplifier most likely will not operate normally. If the supplies are low impedance, then the current through the steering diodes can become quite high. The current level depends on the ability of the input source to deliver current, and any resistance in the input path.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
OPA2211SPWP	ACTIVE	HTSSOP	PWP	20	70	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-55 to 150	OP2211S	Samples

[1] The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

[2] **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

[3] MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

[4] There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

[5] Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

[6] Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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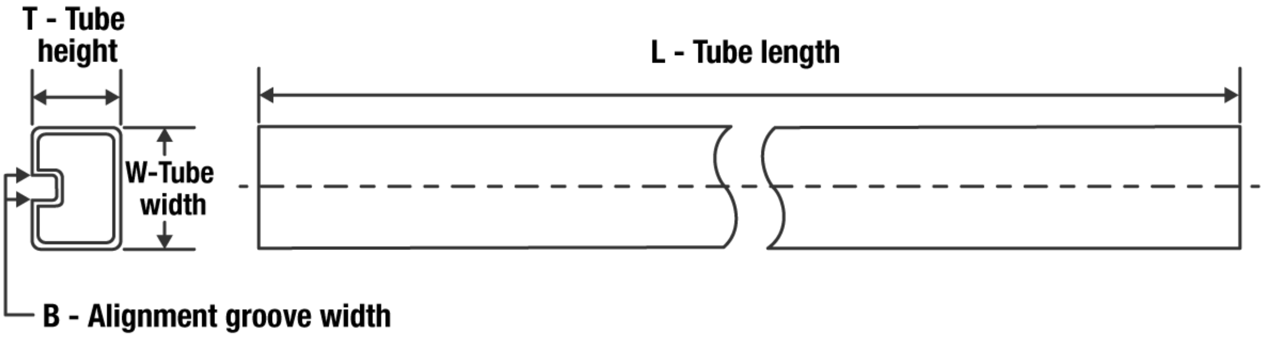
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
OPA2211SPWP	PWP	HTSSOP	20	70	530	10.2	3600	3.5

GENERIC PACKAGE VIEW

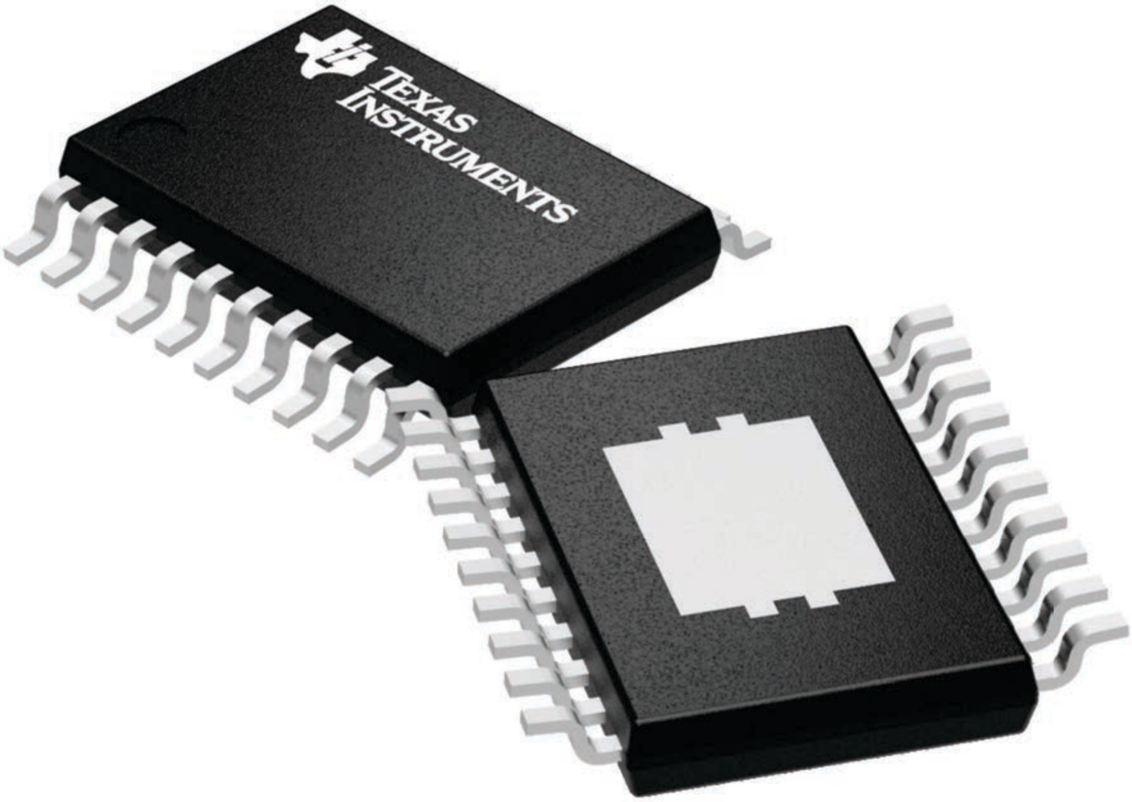
PWP 20

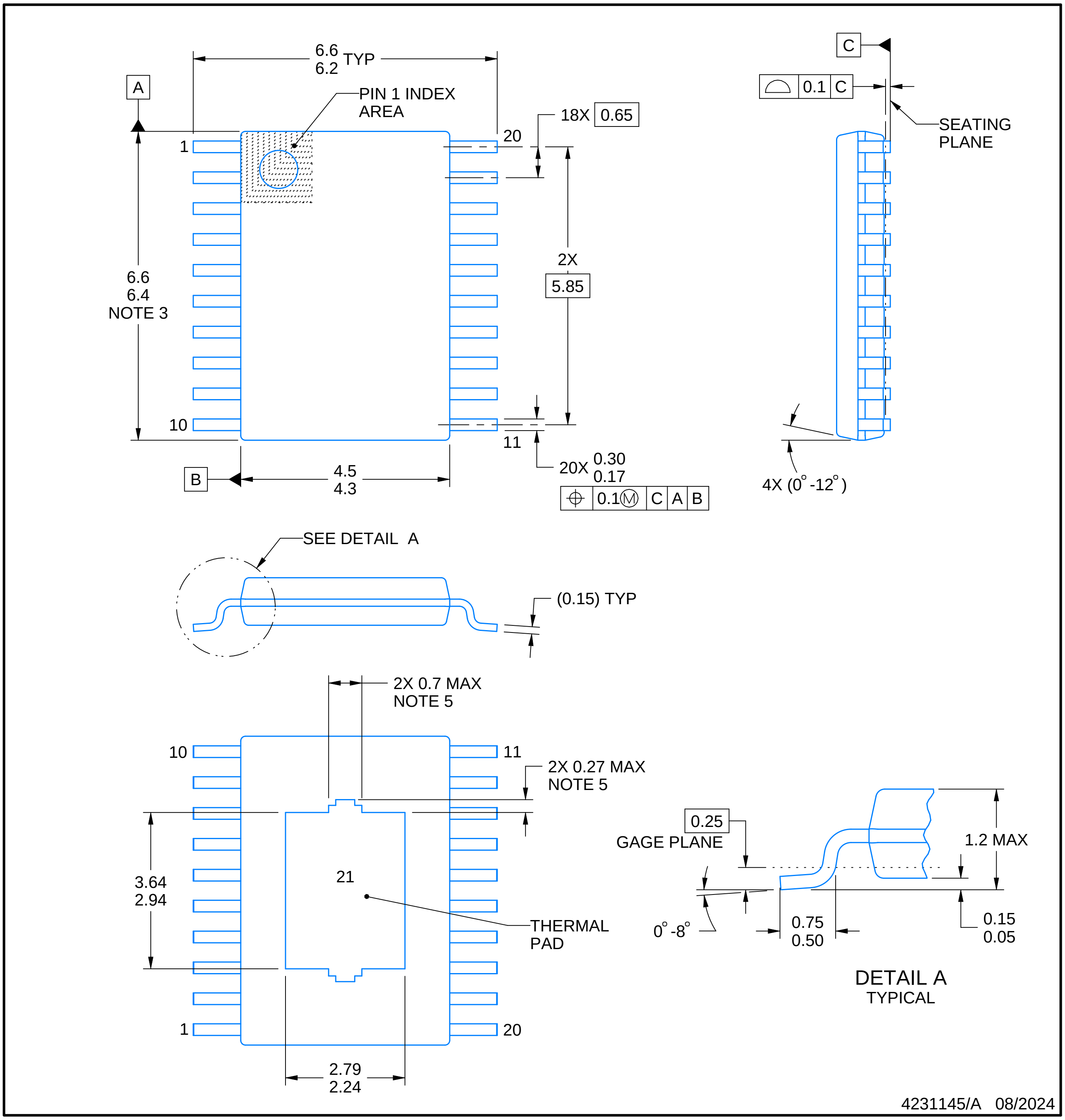
HTSSOP - 1.2 mm max height

6.5 x 4.4, 0.65 mm pitch

SMALL OUTLINE PACKAGE

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

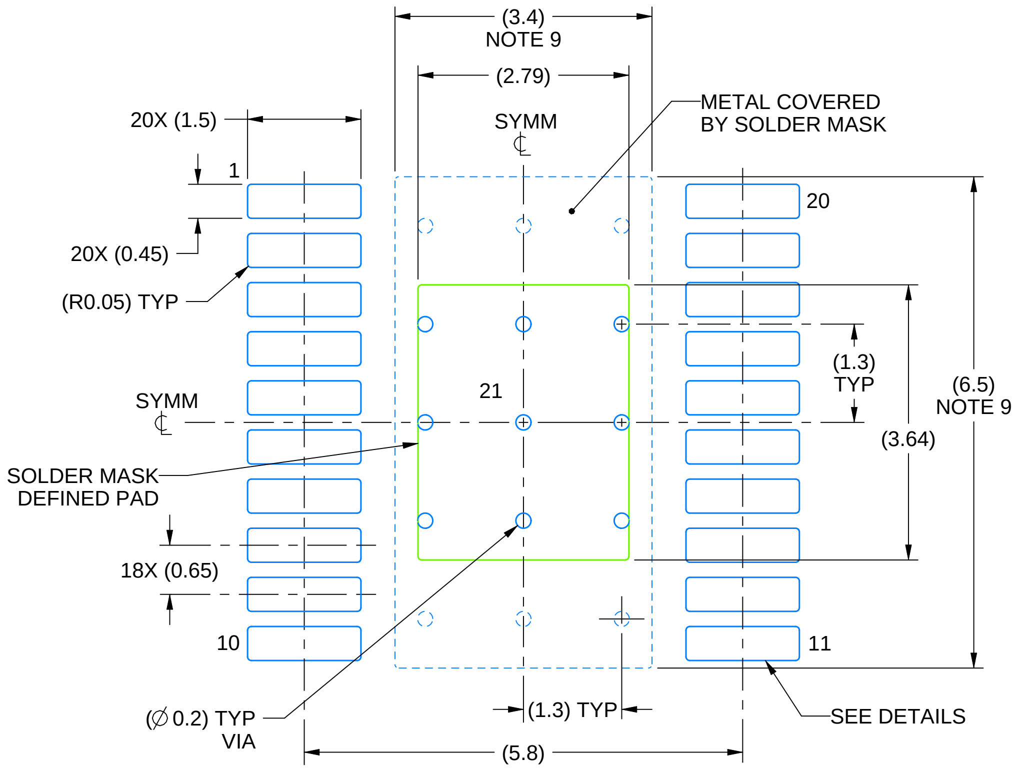




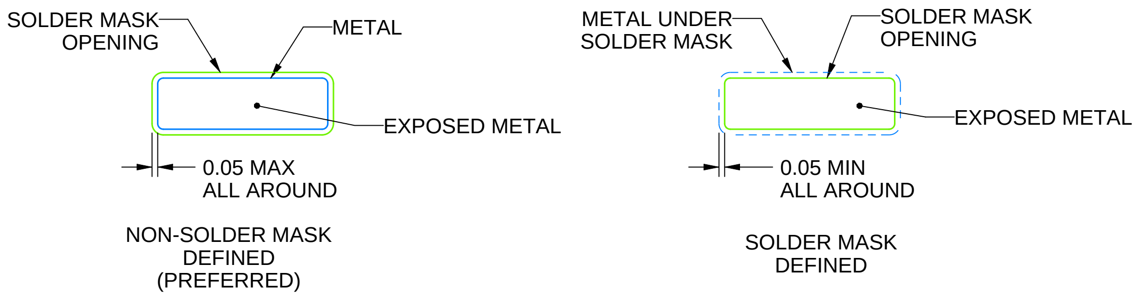
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-153.
5. Features may differ or may not be present.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

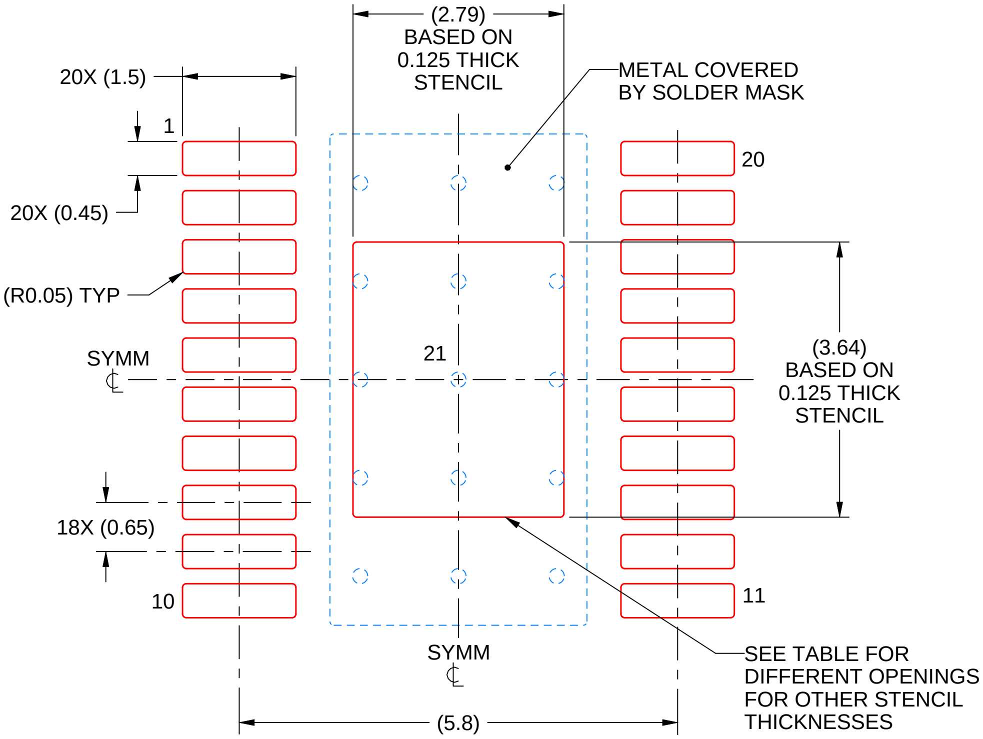


SOLDER MASK DETAILS

4231145/A 08/2024

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
9. Size of metal pad may vary due to creepage requirement.
10. Vias are optional depending on application, refer to device data sheet. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	3.12 X 4.07
0.125	2.79 X 3.64 (SHOWN)
0.15	2.55 X 3.32
0.175	2.36 X 3.08

NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

重要通知和免责声明

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