适用于成本敏感型系统的 **OPA2313-Q1** 低功耗、轨至轨输入/输出、**500μV** 典型失调电压、**1MHz** 运算放大器

1 特性

- 符合面向汽车应用的 AEC-Q100 标准
  - 器件温度等级 1：
    –40°C 至 +125°C T_A
- 面向成本敏感型系统的精密放大器
- 低 I_Q：50μA/ch
- 宽电源电压：1.8V 至 5.5V
- 低噪声：1kHz 下为 25nV/√Hz
- 增益带宽：1MHz
- 轨到轨输入/输出
- 低输入偏置电流：0.2pA
- 低失调电压：0.5mV
- 单位增益稳定
- 内部射频干扰 (RFI)/电磁干扰 (EMI) 滤波器

2 应用

- 信息娱乐
- 引擎控制单元
- 汽车照明
- 低侧检测
- 电池管理系统
- 无源安全性
- 电容式检测
- 燃油泵

3 说明

OPA2313-Q1 双通道运算放大器兼具低功耗和高性能优势。因此，可将其用于广泛的 应用，例如信息娱乐系统、发动机控制单元、汽车照明等。OPA2313-Q1 具有 轨至轨输入和输出 (RRIO) 摆幅、低静态电流（典型值：50μA）、高带宽 (1MHz) 以及超低噪声（1kHz 时为 25nV/√Hz）等特性，因此特别适合需要在成本和性能之间取得良好平衡的各种 应用 。此外，由于具有低输入偏置电流，该器件非常适合用于 源阻抗高达兆欧级 的应用。

OPA2313-Q1 采用稳健耐用的设计，方便电路设计人员使用。该器件在容性负载高达 150pF 的条件下具有单位增益稳定性，集成了 RFI/EMI 抑制滤波器，在过驱条件下无相位反转，并具有高静电放电 (ESD) 保护 (4kV HBM)。

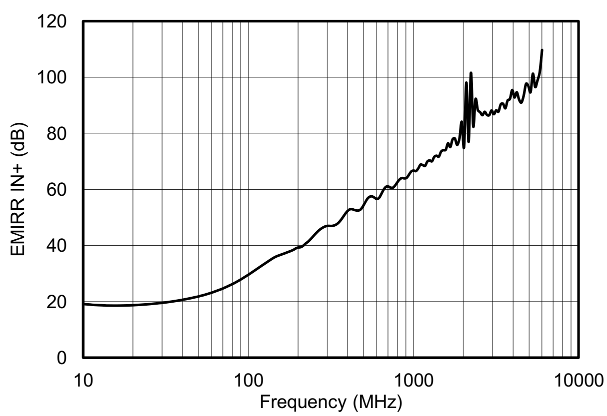
此器件经过优化，适合在低至 1.8V (±0.9V) 和高达 5.5V (±2.75V) 的电压下工作，且额定的扩展工作温度范围为 –40°C 至 +125°C。

器件信息(1)

器件型号	封装	封装尺寸（标称值）
OPA2313-Q1	SOIC (8)	4.90mm × 3.91mm
	VSSOP (8)	3.00mm × 3.00mm

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。

EMIRR IN+ 与频率间的关系



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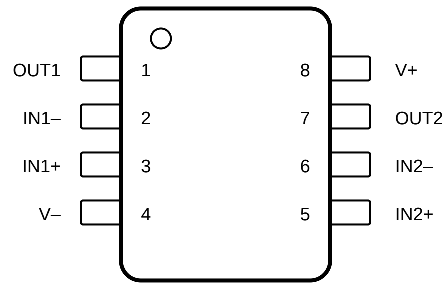
4 修订历史记录

日期	修订版本	说明
2018 年 12 月	*	最初发布版本。

5 Pin Configuration and Functions

OPA2313-Q1 D, DGK Packages
8-Pin SOIC, VSSOP
Top View



Not to scale

Pin Functions: OPA2313-Q1

PIN		I/O	DESCRIPTION
NAME	NO.		
IN1–	2	I	Inverting input, channel 1
IN1+	3	I	Noninverting input, channel 1
IN2–	6	I	Inverting input, channel 2
IN2+	5	I	Noninverting input, channel 2
OUT1	1	O	Output, channel 1
OUT2	7	O	Output, channel 2
V–	4	—	Negative (lowest) supply or ground (for single-supply operation)
V+	8	—	Positive (highest) supply

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)[1]

		MIN	MAX	UNIT
Voltage	Supply voltage (V+) – (V–)	0	7	V
	Signal input terminals[2]	(V–) – (0.5)	(V+) + 0.5	
Current	Signal input terminals[2]	–10	10	mA
	Output short circuit[3]	Continuous		
Temperature	Operating, T_A	–40	150	°C
	Junction, T_J		150	
	Storage, T_{stg}	–65	150	

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Input pins are diode-clamped to the power-supply rails. Input signals that may swing more than 0.5 V beyond the supply rails must be current limited to 10 mA or less.
(3) Short-circuit to ground, one amplifier per package.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001[1] HBM ESD Classification Level 3A	±4000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101[2] CDM ESD Classification Level C6	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V_S	Supply voltage (V+) – (V–)	1.8	5.5	V
T_A	Specified temperature	–40	125	°C

6.4 Thermal Information

THERMAL METRIC[1]		OPA2313-Q1		UNIT
		D (SOIC)	DGK (VSSOP)	
		8 Pins	8 Pins	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	138.4	191.2	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	89.5	61.9	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	78.6	111.9	°C/W
ψ_{JT}	Junction-to-top characterization parameter	29.9	5.1	°C/W
ψ_{JB}	Junction-to-board characterization parameter	78.1	110.2	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.5 Electrical Characteristics: 5.5 V(1)

For V_S= (V+) – (V–) = 5.5 V at T_A = 25°C, R_L = 10 kΩ connected to V_S / 2, and V_{CM} = V_{OUT} = V_S / 2, (unless otherwise noted)(1)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
OFFSET VOLTAGE							
V_{OS}	Input offset voltage				0.5	2.5	mV
dV_{OS}/dT	Input offset voltage vs temperature		T_A = –40°C to 125°C		2		µV/°C
PSRR	Power-supply rejection ratio		T_A = –40°C to 125°C	74	90		dB
	Channel separation, dc	At dc			10		µV/V
INPUT VOLTAGE RANGE							
V_{CM}	Common-mode voltage range	No phase reversal, rail-to-rail input		(V–) – 0.2		(V+) + 0.2	V
CMRR	Common-mode rejection ratio	(V–) – 0.2 V < V_{CM} < (V+) – 1.3 V	T_A = –40°C to 125°C	70	85		dB
		V_{CM} = –0.2 V to 5.7 V	T_A = –40°C to 125°C	64	80		
INPUT BIAS CURRENT							
I_B	Input bias current				±0.2	±10	pA
			T_A = –40°C to 85°C(2)			±50	
			T_A = –40°C to 125°C(2)			±600	
I_{OS}	Input offset current				±0.2	±10	pA
			T_A = –40°C to 85°C(2)			±50	
			T_A = –40°C to 125°C(2)			±600	
NOISE							
	Input voltage noise (peak-to-peak)	f = 0.1 Hz to 10 Hz			6		$µV_{PP}$
e_n	Input voltage noise density	f = 10 kHz			22		nV/√Hz
		f = 1 kHz			25		
i_n	Input current noise density	f = 1 kHz			5		fA/√Hz
INPUT CAPACITANCE							
C_{IN}	Differential				1		pF
	Common-mode				5		
OPEN-LOOP GAIN							
A_{OL}	Open-loop voltage gain	0.05 V < V_O < (V+) – 0.05 V, R_L = 100 kΩ		90	104		dB
		0.3 V < V_O < (V+) – 0.3 V, R_L = 2 kΩ		100	110		
		0.1 V < V_O < (V+) – 0.1 V	T_A = –40°C to 125°C	104	116		
	Phase margin	V_S = 5 V, G = +1			65		°
FREQUENCY RESPONSE							
GBW	Gain-bandwidth product	V_S = 5 V, C_L = 10 pF			1		MHz
SR	Slew rate	V_S = 5 V, G = +1			0.5		V/µs
t_S	Settling time	To 0.1%, V_S = 5 V, 2-V step, G = +1			5		µs
		To 0.01%, V_S = 5 V, 2-V step, G = +1			6		
	Overload recovery time	V_S = 5 V, V_{IN} × Gain > V_S			3		
THD+N	Total harmonic distortion + noise(3)	V_S = 5 V, V_O = 1 V_{RMS}, G = +1, f = 1 kHz			0.0045%		
OUTPUT							
V_O	Voltage output swing from supply rails	R_L = 100 kΩ(2)			5	20	mV
		R_L = 100 kΩ(2)	T_A = –40°C to 125°C			30	
		R_L = 2 kΩ(2)			75	100	
		R_L = 2 kΩ(2)	T_A = –40°C to 125°C			125	
I_{SC}	Short-circuit current				±15		mA
			T_A = –40°C to 125°C		±12		
R_O	Open-loop output impedance				2300		Ω

(1) Parameters with minimum or maximum specification limits are 100% production tested at 25°C, unless otherwise noted. Over-temperature limits are based on characterization and statistical analysis.
(2) Specified by design and characterization; not production tested.
(3) Third-order filter; bandwidth = 80 kHz at –3 dB.

Electrical Characteristics: 5.5 V(1) (continued)

For V_S= (V+) – (V–) = 5.5 V at T_A = 25°C, R_L = 10 kΩ connected to V_S / 2, and V_{CM} = V_{OUT} = V_S / 2, (unless otherwise noted)(1)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
POWER SUPPLY							
V_S	Specified voltage range			1.8 (±0.9)		5.5 (±2.75)	V
I_Q	Quiescent current per amplifier	V_S = 5 V, I_O = 0 mA			50	60	µA
		V_S = 5 V, I_O = 0 mA	T_A = –40°C to 125°C			85	
	Power-on time	V_S = 0 V to 5 V, to 90% I_Q level			10		µs

6.6 Electrical Characteristics: 1.8 V[1]

For V_S= (V+) – (V–) = 1.8 V at T_A = 25°C, R_L = 10 kΩ connected to V_S / 2, V_{CM} = V_{S+} – 1.3 V, and V_{OUT} = V_S / 2, (unless otherwise noted)[1]

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
OFFSET VOLTAGE							
V_{OS}	Input offset voltage				0.5	2.5	mV
dV_{OS}/dT	Input offset voltage vs temperature		T_A = –40°C to 125°C		2		µV/°C
PSRR	Power-supply rejection ratio		T_A = –40°C to 125°C	74	90		dB
	Channel separation, dc	At dc			10		µV/V
INPUT VOLTAGE RANGE							
V_{CM}	Common-mode voltage range	No phase reversal, rail-to-rail input		(V–) – 0.2		(V+) + 0.2	V
CMRR	Common-mode rejection ratio	(V–) – 0.2 V < V_{CM} < (V+) – 1.3 V	T_A = –40°C to 125°C	70	85		dB
		V_S= 1.8 V, V_{CM} = –0.2 V to 1.8 V		58	73		
		V_{CM} = –0.2 V to 1.6 V	T_A = –40°C to 125°C	58	70		
INPUT BIAS CURRENT							
I_B	Input bias current				±0.2	±10	pA
			T_A = –40°C to 85°C[2]			±50	
			T_A = –40°C to 125°C[2]			±600	
I_{OS}	Input offset current				±0.2	±10	pA
			T_A = –40°C to 85°C[2]			±50	
			T_A = –40°C to 125°C[2]			±600	
NOISE							
	Input voltage noise (peak-to-peak)	f = 0.1 Hz to 10 Hz			6		μV_{PP}
e_n	Input voltage noise density	f = 10 kHz			22		nV/√Hz
		f = 1 kHz			25		
i_n	Input current noise density	f = 1 kHz			5		fA/√Hz
INPUT CAPACITANCE							
C_{IN}	Differential				1		pF
	Common-mode				5		
OPEN-LOOP GAIN							
A_{OL}	Open-loop voltage gain	0.05 V < V_O < (V+) – 0.05 V, R_L = 100 kΩ		100	110		dB
		0.1 V < V_O < (V+) – 0.1 V	T_A = –40°C to 125°C	90	110		
FREQUENCY RESPONSE							
GBW	Gain-bandwidth product	C_L = 10 pF			0.9		MHz
SR	Slew rate	G = +1			0.45		V/µs
t_S	Settling time	To 0.1%, V_S = 5 V, 2-V step, G = +1			5		µs
		To 0.01%, V_S = 5 V, 2-V step, G = +1			6		
	Overload recovery time	V_S = 5 V, V_{IN} × Gain > V_S			3		
THD+N	Total harmonic distortion + noise[3]	V_S = 5 V, V_O = 1 V_{RMS}, G = +1, f = 1kHz			0.0045%		
OUTPUT							
V_O	Voltage output swing from supply rails	R_L = 100 kΩ[2]			5	15	mV
		R_L = 100 kΩ[2]	T_A = –40°C to 125°C			30	
		R_L = 2 kΩ[2]			25	50	
		R_L = 2 kΩ[2]	T_A = –40°C to 125°C			125	
I_{SC}	Short-circuit current				±6		mA
R_O	Open-loop output impedance				2300		Ω

(1) Parameters with minimum or maximum specification limits are 100% production tested at 25°C, unless otherwise noted. Over-temperature limits are based on characterization and statistical analysis.
(2) Specified by design and characterization; not production tested.
(3) Third-order filter; bandwidth = 80 kHz at –3 dB.

Electrical Characteristics: 1.8 V(1) (continued)

For V_S= (V+) – (V–) = 1.8 V at T_A = 25°C, R_L = 10 kΩ connected to V_S / 2, V_{CM} = V_{S+} – 1.3 V, and V_{OUT} = V_S / 2, (unless otherwise noted)(1)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER SUPPLY						
V_S	Specified voltage range		1.8 (±0.9)		5.5 (±2.75)	V
I_Q	Quiescent current per amplifier	V_S = 5 V, I_O = 0 mA		50	60	µA
	Power-on time	V_S = 0 V to 5 V, to 90% I_Q level		10		µs

6.7 Typical Characteristics: Tables of Graphs

表 1. Characteristic Performance Measurements

TITLE	FIGURE
Open-Loop Gain and Phase vs Frequency	图 1
Open-Loop Gain vs Temperature	图 2
Quiescent Current vs Supply Voltage	图 3
Quiescent Current vs Temperature	图 4
Offset Voltage Production Distribution	图 5
Offset Voltage Drift Distribution	图 6
Offset Voltage vs Common-Mode Voltage (Maximum Supply)	图 7
Offset Voltage vs Temperature	图 8
CMRR and PSRR vs Frequency (RTI)	图 9
CMRR and PSRR vs Temperature	图 10
0.1-Hz to 10-Hz Input Voltage Noise (5.5 V)	图 11
Input Voltage Noise Spectral Density vs Frequency (1.8 V, 5.5 V)	图 12
Input Voltage Noise vs Common-Mode Voltage (5.5 V)	图 13
Input Bias and Offset Current vs Temperature	图 14
Open-Loop Output Impedance vs Frequency	图 15
Maximum Output Voltage vs Frequency and Supply Voltage	图 16
Output Voltage Swing vs Output Current (over Temperature)	图 17
Closed-Loop Gain vs Frequency, G = 1, –1, 10 (1.8 V)	图 18
Closed-Loop Gain vs Frequency, G = 1, –1, 10 (5.5 V)	图 19
Small-Signal Overshoot vs Load Capacitance	图 20
Phase Margin vs Capacitive Load	图 21
Small-Signal Step Response, Noninverting (1.8 V)	图 22
Small-Signal Step Response, Noninverting (5.5 V)	图 23
Large-Signal Step Response, Noninverting (1.8 V)	图 24
Large-Signal Step Response, Noninverting (5.5 V)	图 25
Positive Overload Recovery	图 26
Negative Overload Recovery	图 27
No Phase Reversal	图 28
Channel Separation vs Frequency (Dual)	图 29
THD+N vs Amplitude (G = +1, 2 kΩ, 10 kΩ)	图 30
THD+N vs Amplitude (G = –1, 2 kΩ, 10 kΩ)	图 31
THD+N vs Frequency (0.5 V_{RMS}, G = +1, 2 kΩ, 10 kΩ)	图 32
EMIRR IN+ vs Frequency	图 33

6.8 Typical Characteristics

At T_A = 25°C, V_S = 5 V, R_L = 10 kΩ connected to V_S / 2, and V_{CM} = V_{OUT} = V_S / 2, unless otherwise noted.

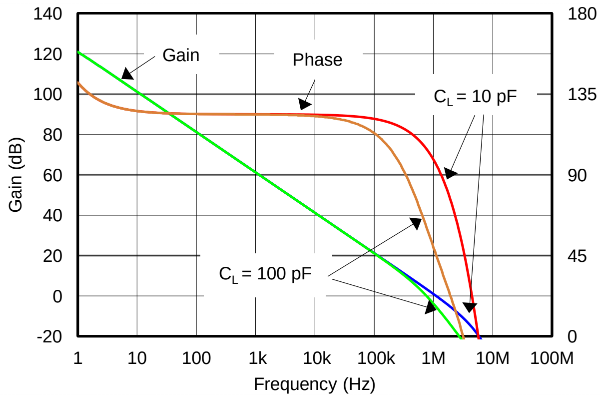


图 1. Open-Loop Gain and Phase vs Frequency

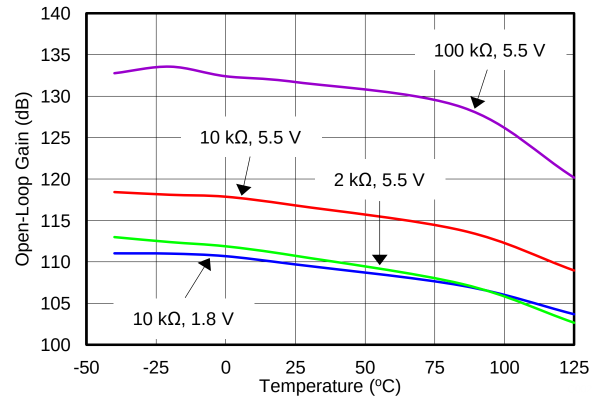


图 2. Open-Loop Gain vs Temperature

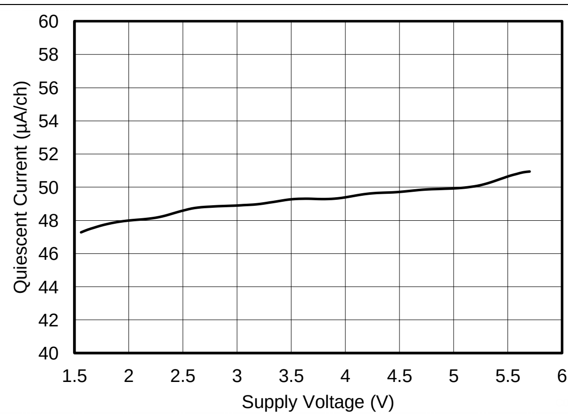


图 3. Quiescent Current vs Supply

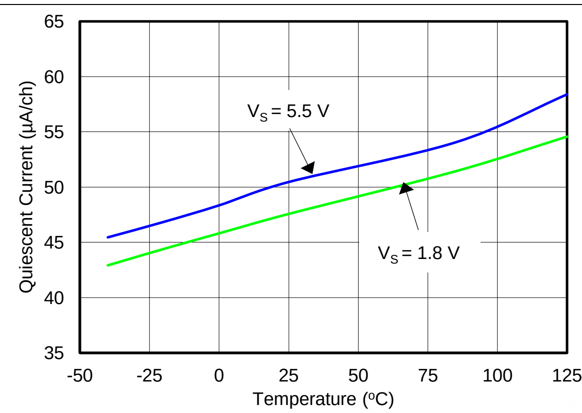


图 4. Quiescent Current vs Temperature

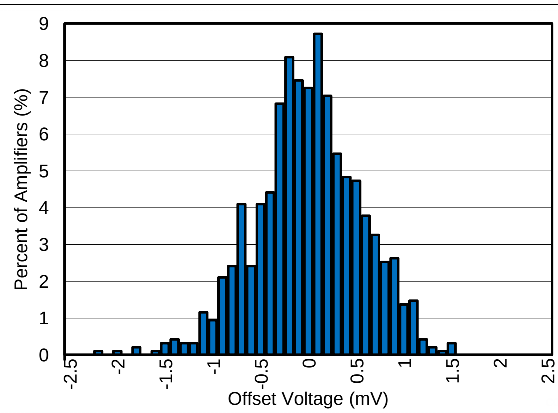


图 5. Offset Voltage Production Distribution

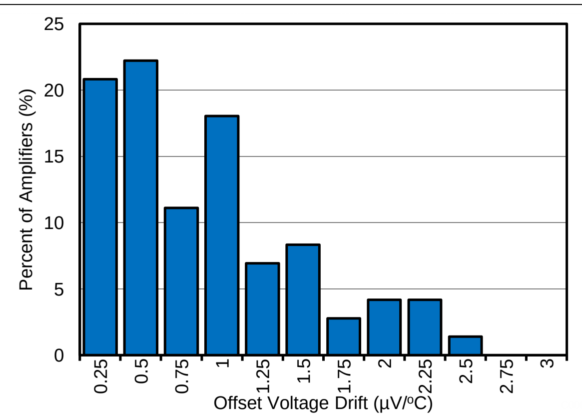


图 6. Offset Voltage Drift Distribution

Typical Characteristics (接下页)

At T_A = 25°C, V_S = 5 V, R_L = 10 kΩ connected to V_S / 2, and V_{CM} = V_{OUT} = V_S / 2, unless otherwise noted.

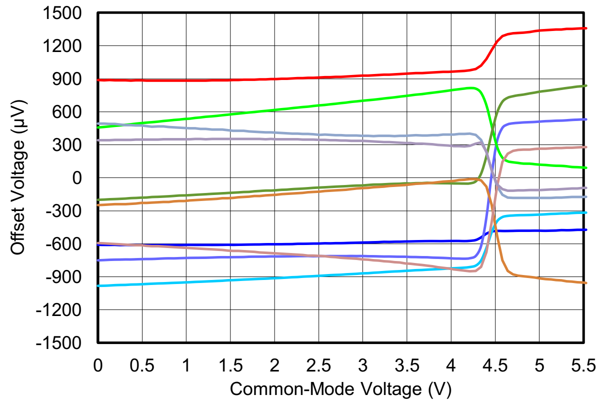


图 7. Offset Voltage vs Common-Mode Voltage

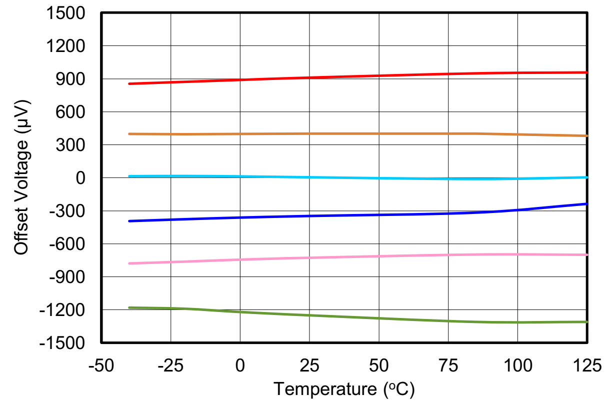


图 8. Offset Voltage vs Temperature

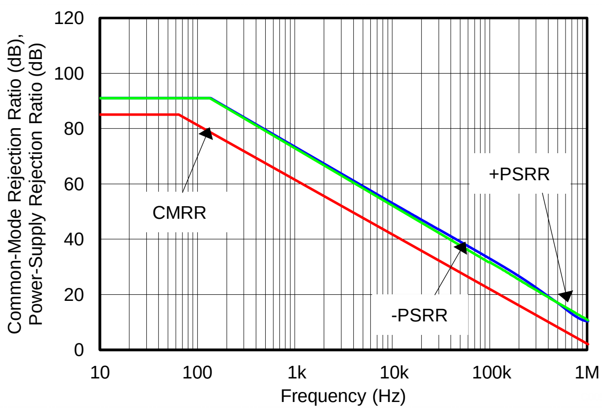


图 9. CMRR and PSRR vs Frequency (Referred-to-Input)

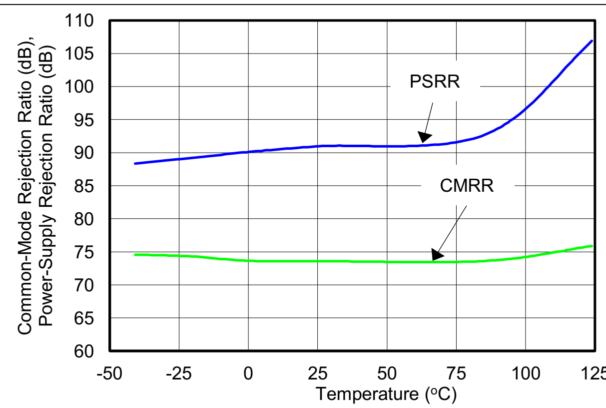


图 10. CMRR and PSRR vs Temperature

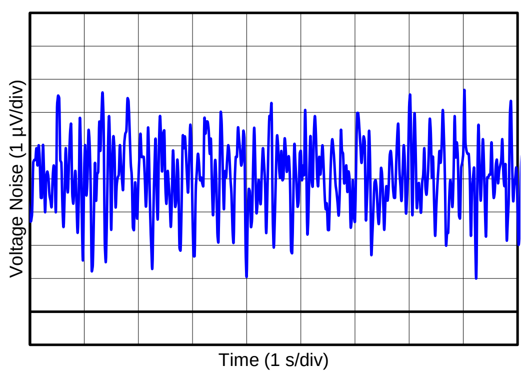


图 11. 0.1-Hz to 10-Hz Input Voltage Noise

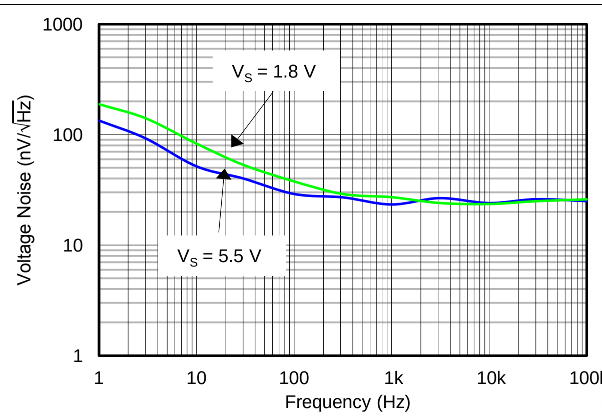


图 12. Input Voltage Noise Spectral Density vs Frequency

Typical Characteristics (接下页)

At T_A = 25°C, V_S = 5 V, R_L = 10 kΩ connected to V_S / 2, and V_{CM} = V_{OUT} = V_S / 2, unless otherwise noted.

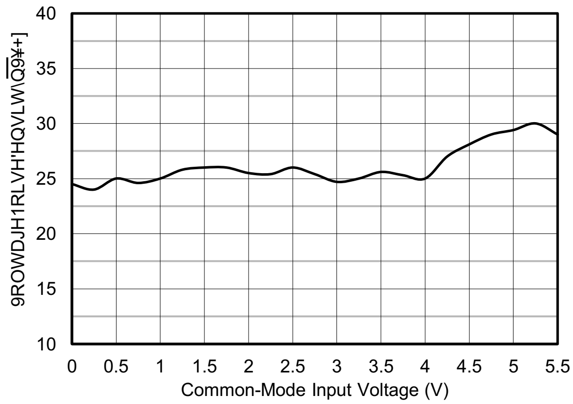


图 13. Voltage Noise vs Common-Mode Voltage

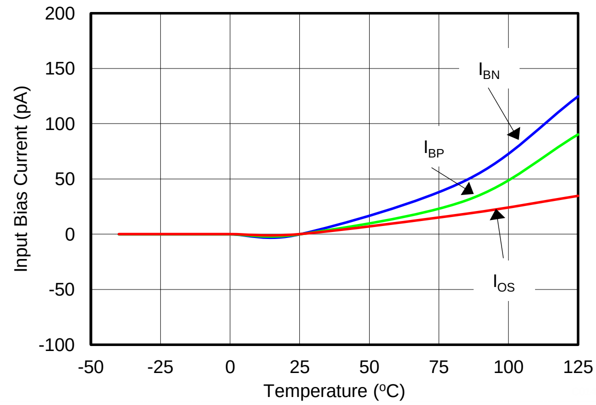


图 14. Input Bias and Offset Current vs Temperature

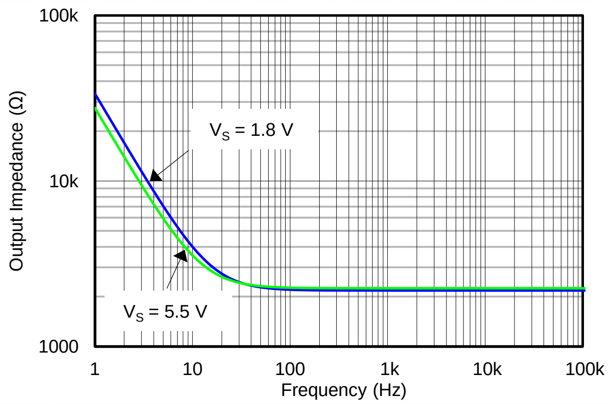


图 15. Open-Loop Output Impedance vs Frequency

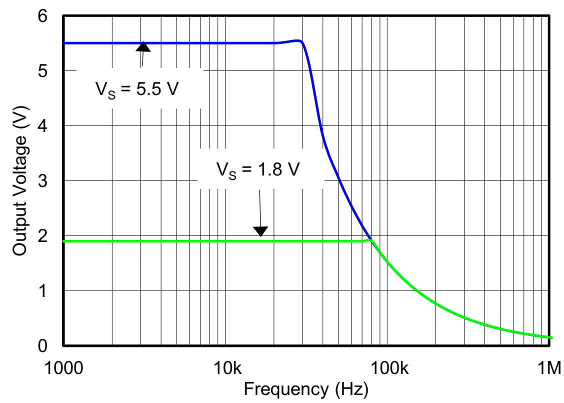


图 16. Maximum Output Voltage vs Frequency and Supply Voltage

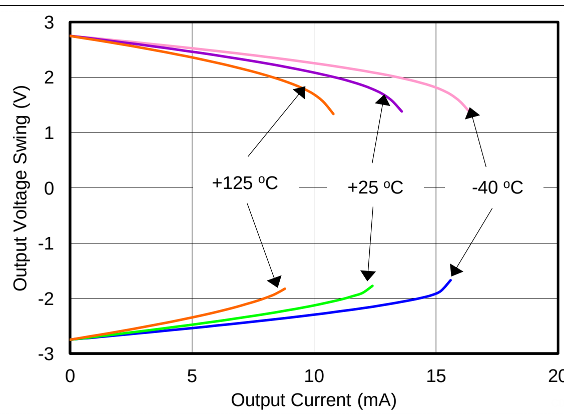


图 17. Output Voltage Swing vs Output Current (Over Temperature)

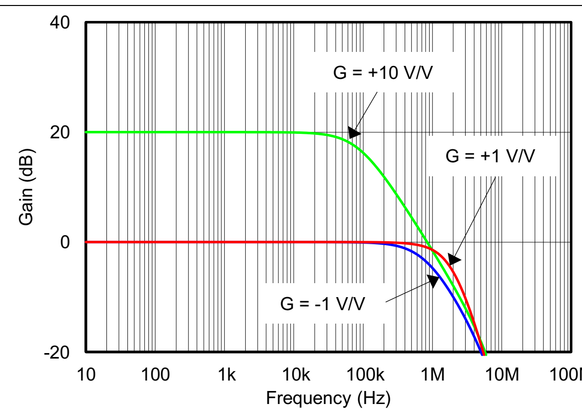


图 18. Closed-Loop Gain vs Frequency (Minimum Supply)

Typical Characteristics (接下页)

At T_A = 25°C, V_S = 5 V, R_L = 10 kΩ connected to V_S / 2, and V_{CM} = V_{OUT} = V_S / 2, unless otherwise noted.

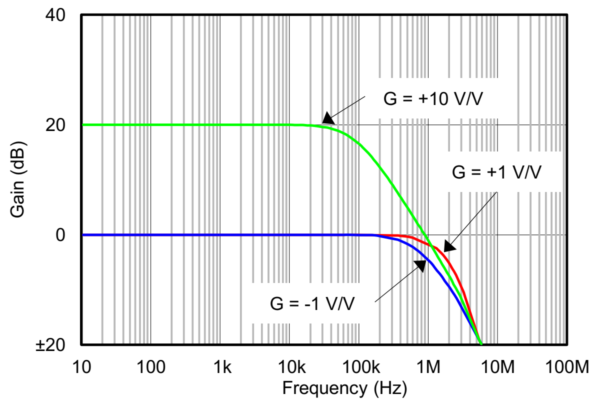


图 19. Closed-Loop Gain vs Frequency (Maximum Supply)

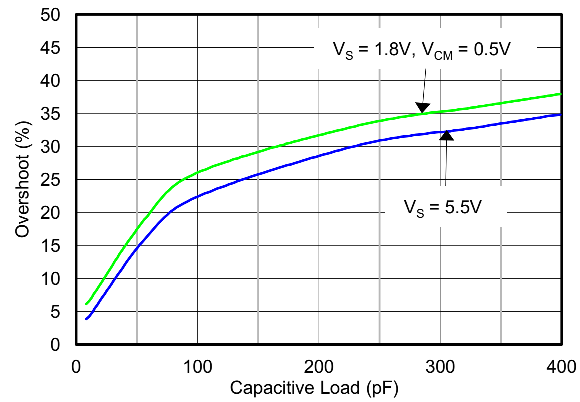


图 20. Small-Signal Overshoot vs Load Capacitance

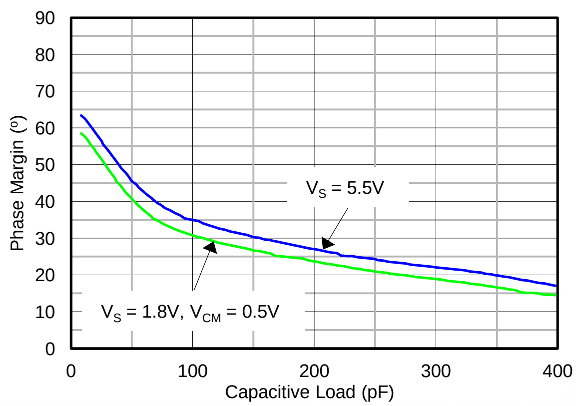


图 21. Phase Margin vs Capacitive Load

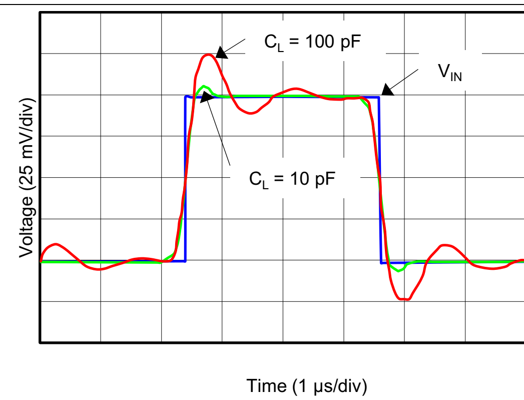


图 22. Small-Signal Pulse Response (Minimum Supply)

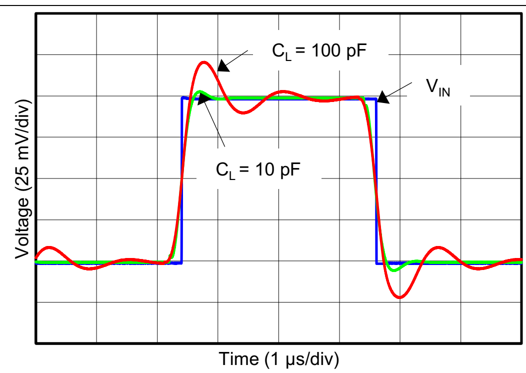


图 23. Small-Signal Pulse Response (Maximum Supply)

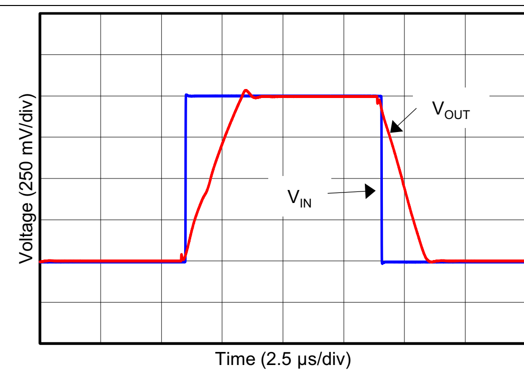


图 24. Large-Signal Pulse Response (Minimum Supply)

Typical Characteristics (接下页)

At T_A = 25°C, V_S = 5 V, R_L = 10 kΩ connected to V_S / 2, and V_{CM} = V_{OUT} = V_S / 2, unless otherwise noted.

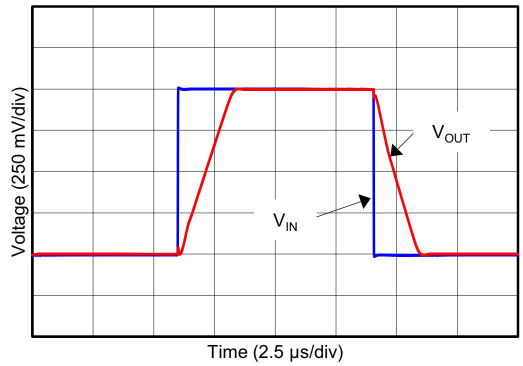


图 25. Large-Signal Pulse Response (Maximum Supply)

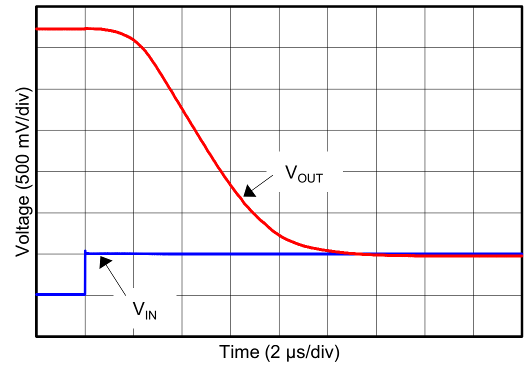


图 26. Positive Overload Recovery

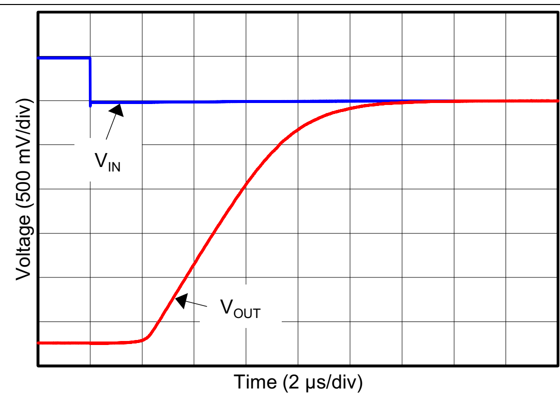


图 27. Negative Overload Recovery

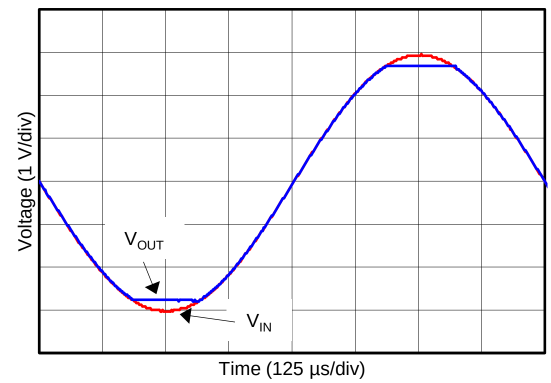


图 28. No Phase Reversal

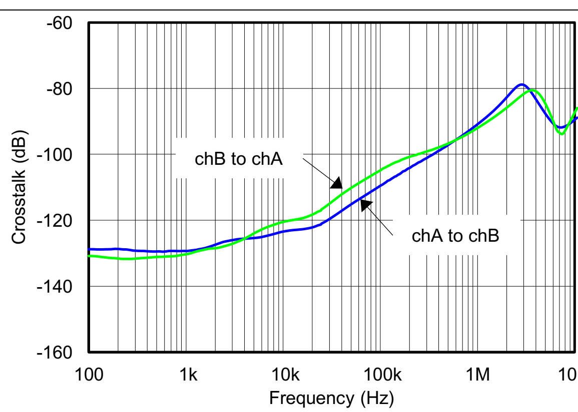


图 29. Channel Separation vs Frequency

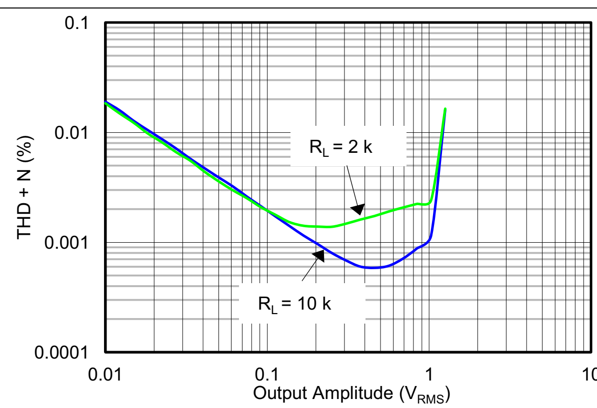


图 30. THD+N vs Output Amplitude (Minimum Supply)

Typical Characteristics (接下页)

At T_A = 25°C, V_S = 5 V, R_L = 10 kΩ connected to V_S / 2, and V_{CM} = V_{OUT} = V_S / 2, unless otherwise noted.

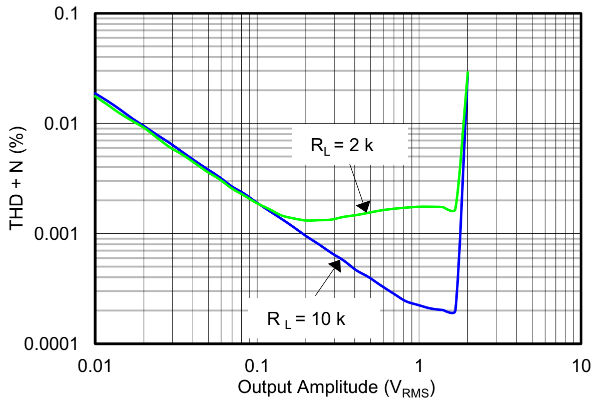


图 31. THD+N vs Output Amplitude (Maximum Supply)

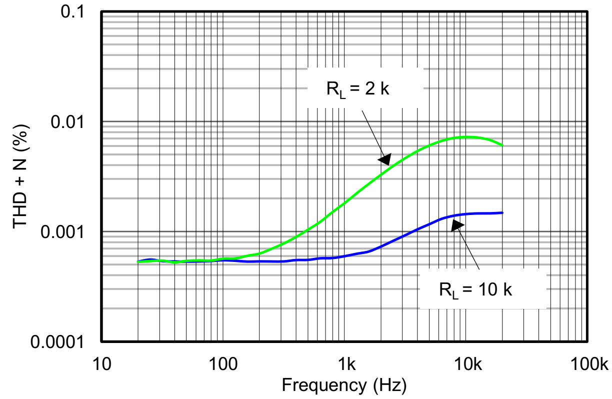


图 32. THD+N vs Frequency

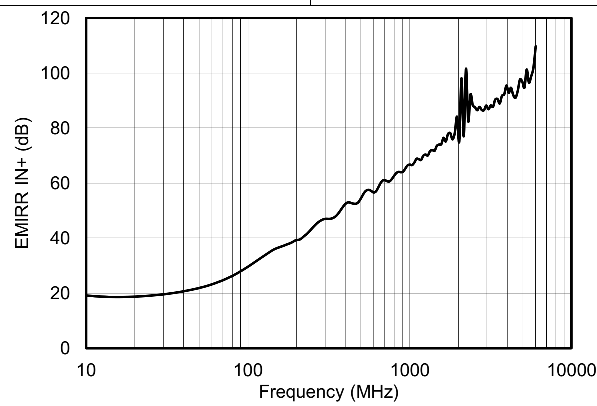


图 33. EMIRR IN+ vs Frequency

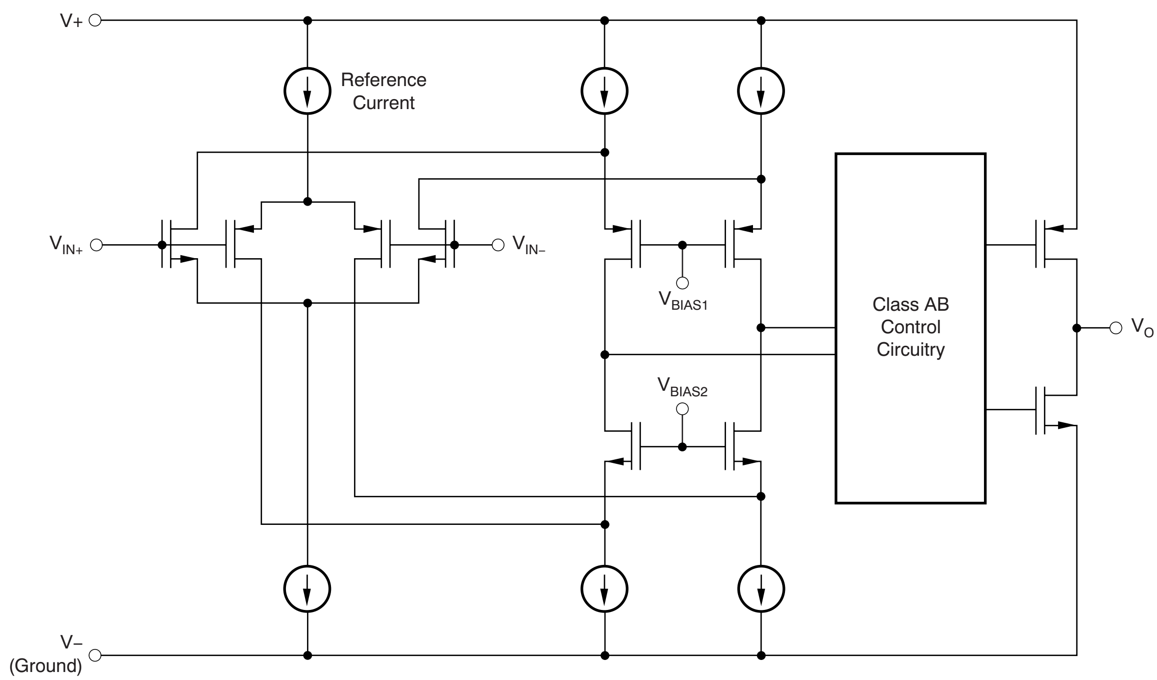
7 Detailed Description

7.1 Overview

The OPA2313-Q1 is a low-power, rail-to-rail input and output operational amplifier designed for cost-constrained applications. This device operates from 1.8 V to 5.5 V, is unity-gain stable, and suitable for a wide range of general-purpose applications. The class AB output stage is capable of driving loads greater than 10-kΩ connected to any point between V+ and ground. The input common-mode voltage range includes both rails, and allows the OPA2313-Q1 to be used in virtually any single-supply application. Rail-to-rail input and output swing significantly increases dynamic range, especially in low-supply applications, and makes this device ideal for driving sampling analog-to-digital converters (ADCs).

The OPA2313-Q1 features 1-MHz bandwidth and 0.5-V/µs slew rate with only 50-µA supply current per channel, providing good ac performance at very low power consumption. Low frequency (dc) applications are also well served with a low input noise voltage of 25 nV/$\sqrt{Hz}$ at 1 kHz, low input bias current (0.2 pA), and an input offset voltage of 0.5 mV (typical). The typical offset voltage drift is 2 µV/°C; over the full temperature range the input offset voltage changes only 200 µV (0.5 mV to 0.7 mV).

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Operating Voltage

The OPA2313-Q1 device is fully specified and tested from 1.8 V to 5.5 V (±0.9 V to ±2.75 V). Parameters that vary with supply voltage are illustrated in the *Typical Characteristics* section.

7.3.2 Rail-to-Rail Input

The input common-mode voltage range of the OPA2313-Q1 device extends 200 mV beyond the supply rails. This performance is achieved with a complementary input stage: an N-channel input differential pair in parallel with a P-channel differential pair, as shown in the *Functional Block Diagram* section. The N-channel pair is active for input voltages close to the positive rail, typically (V+) – 1.3 V to 200 mV above the positive supply, while the P-channel pair is on for inputs from 200 mV below the negative supply to approximately (V+) – 1.3 V. There is a small transition region, typically (V+) – 1.4 V to (V+) – 1.2 V, in which both pairs are on. This 200-mV transition region may vary up to 300 mV with process variation. Thus, the transition region (both stages on) may range from (V+) – 1.7 V to (V+) – 1.5 V on the low end, up to (V+) – 1.1 V to (V+) – 0.9 V on the high end. Within this transition region, PSRR, CMRR, offset voltage, offset drift, and THD may be degraded compared to device operation outside this region.

7.3.3 Rail-to-Rail Output

Designed as a micro-power, low-noise operational amplifier, the OPA2313-Q1 delivers a robust output drive capability. A class AB output stage with common-source transistors is used to achieve full rail-to-rail output swing capability. For resistive loads up to 10 kΩ, the output swings typically to within 5 mV of either supply rail regardless of the power-supply voltage applied. Different load conditions change the ability of the amplifier to swing close to the rails, as shown in 图 17.

7.3.4 Common-Mode Rejection Ratio (CMRR)

CMRR for the OPA2313-Q1 device is specified in several ways so the best match for a given application may be used; see the *Electrical Characteristics*. First, the CMRR of the device in the common-mode range below the transition region (V_{CM} < (V+) – 1.3 V) is given. This specification is the best indicator of the capability of the device when the application requires use of one of the differential input pairs. Second, the CMRR over the entire common-mode range is specified at (V_{CM} = –0.2 V to 5.7 V). This last value includes the variations seen through the transition region, as shown in 图 7.

7.3.5 Capacitive Load and Stability

The OPA2313-Q1 device is designed to be used in applications where driving a capacitive load is required. As with all op amps, there may be specific instances where the OPA2313-Q1 device may become unstable. The particular op amp circuit configuration, layout, gain, and output loading are some of the factors to consider when establishing whether or not an amplifier is stable in operation. An op amp in the unity-gain (+1-V/V) buffer configuration that drives a capacitive load exhibits a greater tendency to be unstable than an amplifier operated at a higher noise gain. The capacitive load, in conjunction with the op amp output resistance, creates a pole within the feedback loop that degrades the phase margin. The degradation of the phase margin increases as the capacitive loading increases. When operating in the unity-gain configuration, the OPA2313-Q1 device remains stable with a pure capacitive load up to approximately 1 nF. The equivalent series resistance (ESR) of some capacitors (C_L greater than 1 µF) is sufficient to alter the phase characteristics in the feedback loop such that the amplifier remains stable. Increasing the amplifier closed-loop gain allows the amplifier to drive increasingly larger capacitance. This increased capability is evident when observing the overshoot response of the amplifier at higher voltage gains. See the typical characteristic graph, 图 20.

Feature Description (接下页)

One technique for increasing the capacitive load drive capability of the amplifier when it operates in a unity-gain configuration is to insert a small resistor, typically 10 Ω to 20 Ω, in series with the output, as shown in 图 34. This resistor significantly reduces the overshoot and ringing associated with large capacitive loads. One possible problem with this technique is that a voltage divider is created with the added series resistor and any resistor connected in parallel with the capacitive load. The voltage divider introduces a gain error at the output that reduces the output swing.

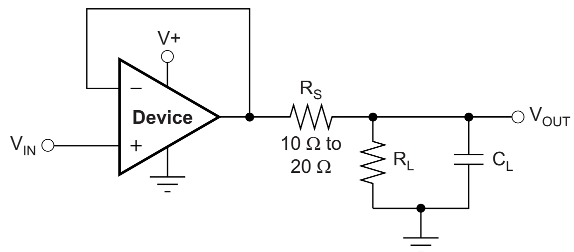


图 34. Improving Capacitive Load Drive

7.3.6 EMI Susceptibility and Input Filtering

Operational amplifiers vary with regard to the susceptibility of the device to electromagnetic interference (EMI). If conducted EMI enters the op amp, the DC offset observed at the amplifier output may shift from the nominal value while EMI is present. This shift is a result of signal rectification associated with the internal semiconductor junctions. While all op amp pin functions may be affected by EMI, the signal input pins are likely to be the most susceptible. The OPA2313-Q1 device incorporates an internal input low-pass filter that reduces the amplifiers response to EMI. Both common-mode and differential mode filtering are provided by this filter. The filter is designed for a common-mode cutoff frequency of approximately 35 MHz (–3 dB), with a rolloff of 20 dB per decade.

Texas Instruments has developed the ability to accurately measure and quantify the immunity of an operational amplifier over a broad frequency spectrum extending from 10 MHz to 6 GHz. The EMI rejection ratio (EMIRR) metric allows op amps to be directly compared by the EMI immunity. 图 33 illustrates the results of this testing on the OPA2313-Q1 device. Detailed information may be found in *EMI Rejection Ratio of Operational Amplifiers*, available for download from www.ti.com.

7.3.7 Input and ESD Protection

The OPA2313-Q1 device incorporates internal electrostatic discharge (ESD) protection circuits on all pins. In the case of input and output pins, this protection primarily consists of current-steering diodes connected between the input and power-supply pins. The ESD protection diodes also provide in-circuit, input overdrive protection, as long as the current is limited to 10 mA as stated in the *Absolute Maximum Ratings*. 图 35 shows how a series input resistor may be added to the driven input to limit the input current. The added resistor contributes thermal noise at the amplifier input and the value must be kept to a minimum in noise-sensitive applications.

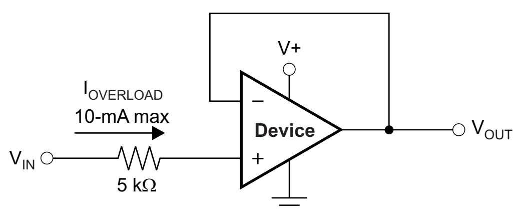


图 35. Input Current Protection

7.4 Device Functional Modes

The OPA2313-Q1 device has a single functional mode. The device is powered on as long as the power-supply voltage is between 1.8 V (±0.9 V) and 5.5 V (±2.75 V).

8 Application and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The OPA2313-Q1 device is a low-power, rail-to-rail input and output operational amplifier. The device operates from 1.8 V to 5.5 V, is unity-gain stable, and is designed for a wide range of general-purpose applications. The class AB output stage is capable of driving loads greater than 10 kΩ connected to any point between V+ and ground. The input common-mode voltage range includes both rails, and allows the OPA2313-Q1 to be used in virtually any single-supply application.

8.2 Typical Application

A typical application for an operational amplifier is an inverting amplifier, as shown in 图 36. An inverting amplifier takes a positive voltage on the input and outputs a signal inverted to the input, making a negative voltage of the same magnitude. In the same manner, the amplifier also makes negative input voltages positive on the output. In addition, amplification may be added by selecting the input resistor (R_I) and the feedback resistor (R_F.)

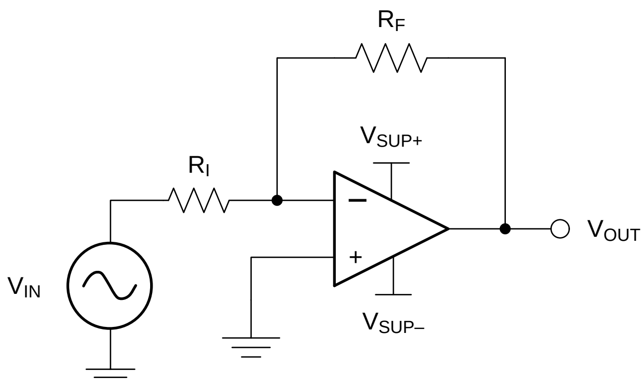


图 36. Inverting Amplifier Application

8.2.1 Design Requirements

The supply voltage must be chosen to be larger than the input voltage range and the desired output range. The limits of the input common-mode range (V_{CM}) and the output voltage swing to the rails (V_O) must also be considered. For instance, this application scales a signal of ±0.5 V (1 V) to ±1.8 V (3.6 V). Setting the supply at ±2.5 V is sufficient to accommodate this application.

8.2.2 Detailed Design Procedure

Determine the gain required by the inverting amplifier using 公式 1 and 公式 2:

$$A_V = \frac{V_{OUT}}{V_{IN}} \quad (1)$$

$$A_V = \frac{1.8}{-0.5} = -3.6 \quad (2)$$

Typical Application (接下页)

When the desired gain is determined, choose a value for R_I or R_F. Choosing a value in the kilohm range is desirable for general-purpose applications because the amplifier circuit uses currents in the milliamp range. This milliamp current range ensures the device does not draw too much current. The trade-off is that very large resistors (100s of kilohms) draw the smallest current but generate the highest noise. Small resistors (100s of ohms) generate low noise but draw high current. This example uses 10 kΩ for R_I, resulting in a 36-kΩ resistor being used for R_F. The values are determined by 公式 3:

$$A_V = -\frac{R_F}{R_I} \quad (3)$$

8.2.3 Application Curve

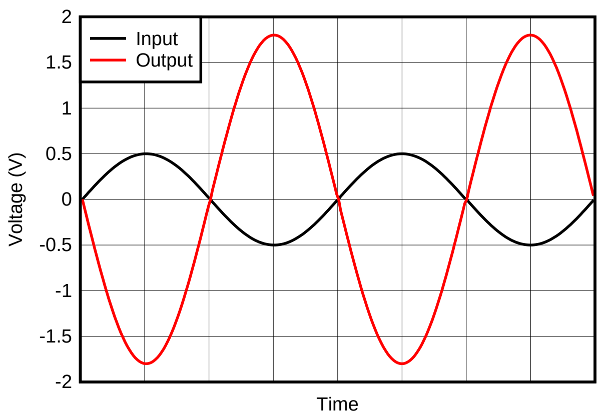
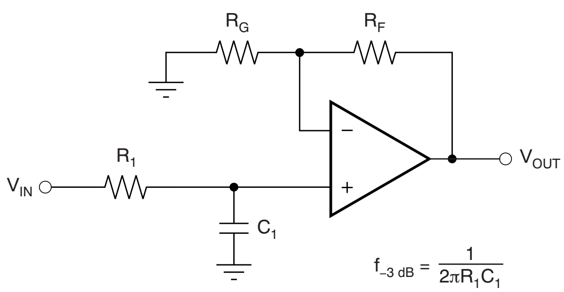


图 37. Inverting Amplifier Input and Output

8.3 System Examples

When receiving low-level signals, limiting the bandwidth of the incoming signals into the system is often required. The simplest way to establish this limited bandwidth is to place an RC filter at the noninverting terminal of the amplifier, as shown in 图 38.



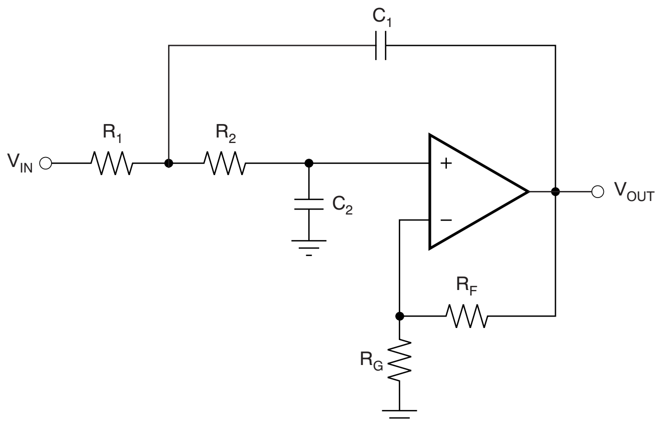
$$f_{-3\,dB} = \frac{1}{2\pi R_1 C_1}$$

$$\frac{V_{OUT}}{V_{IN}} = \left(1 + \frac{R_F}{R_G}\right)\left(\frac{1}{1 + sR_1C_1}\right)$$

图 38. Single-Pole Low-Pass Filter

System Examples (接下页)

If even more attenuation is needed, a multiple pole filter is required. The Sallen-Key filter may be used for this task, as shown in 图 39. For best results, the amplifier must have a bandwidth that is 8 to 10 times the filter frequency bandwidth. Failure to follow this guideline may result in phase shift of the amplifier.



$$f_{-3\,dB} = \frac{1}{2\pi RC}$$

$$R_G = \frac{R_F}{\left(2 - \frac{1}{Q}\right)}$$

图 39. Two-Pole, Low-Pass, Sallen-Key Filter

9 Power Supply Recommendations

The OPA2313-Q1 device is specified for operation from 1.8 V to 5.5 V (±0.9 V to ±2.75 V); many specifications apply from –40°C to +125°C. The *Typical Characteristics* section presents parameters that may exhibit significant variance with regard to operating voltage or temperature.

> **CAUTION**
>
> Supply voltages larger than 7 V can permanently damage the device (see the *Absolute Maximum Ratings* table).

Place 0.1-µF bypass capacitors close to the power-supply pins to reduce errors coupling in from noisy or high-impedance power supplies. For more detailed information on bypass capacitor placement, refer to the *Layout Guidelines* section.

10 Layout

10.1 Layout Guidelines

For best operational performance of the device, use good printed circuit board (PCB) layout practices, including:

- Noise may propagate into analog circuitry through the power pins of the circuit and the operational amplifier. Use bypass capacitors to reduce the coupled noise by providing low-impedance power sources local to the analog circuitry.
  - Connect low-ESR, 0.1-µF ceramic bypass capacitors between each supply pin and ground, placed as close to the device as possible. A single bypass capacitor from V+ to ground is applicable for single-supply applications.
- Separate grounding for analog and digital portions of the circuitry is one of the simplest and most effective methods of noise suppression. One or more layers on multilayer PCBs are usually devoted to ground planes. A ground plane helps distribute heat and reduces EMI noise pickup. Take care to physically separate digital and analog grounds, paying attention to the flow of the ground current. For more detailed information, see *Circuit Board Layout Techniques*.
- To reduce parasitic coupling, run the input traces as far away from the supply or output traces as possible. If the traces cannot be kept separate, crossing the sensitive trace perpendicularly is much better than crossing in parallel with the noisy trace.
- Place the external components as close to the device as possible. Keep R_F and R_G close to the inverting input to minimize parasitic capacitance, as shown in 图 40.
- Keep the length of input traces as short as possible. Remember that the input traces are the most sensitive part of the circuit.
- Consider a driven, low-impedance guard ring around the critical traces. A guard ring may significantly reduce leakage currents from nearby traces that are at different potentials.

10.2 Layout Example

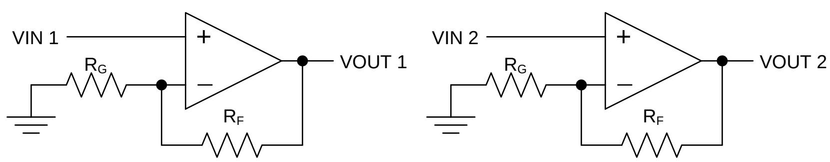


图 40. Schematic Representation for 图 41

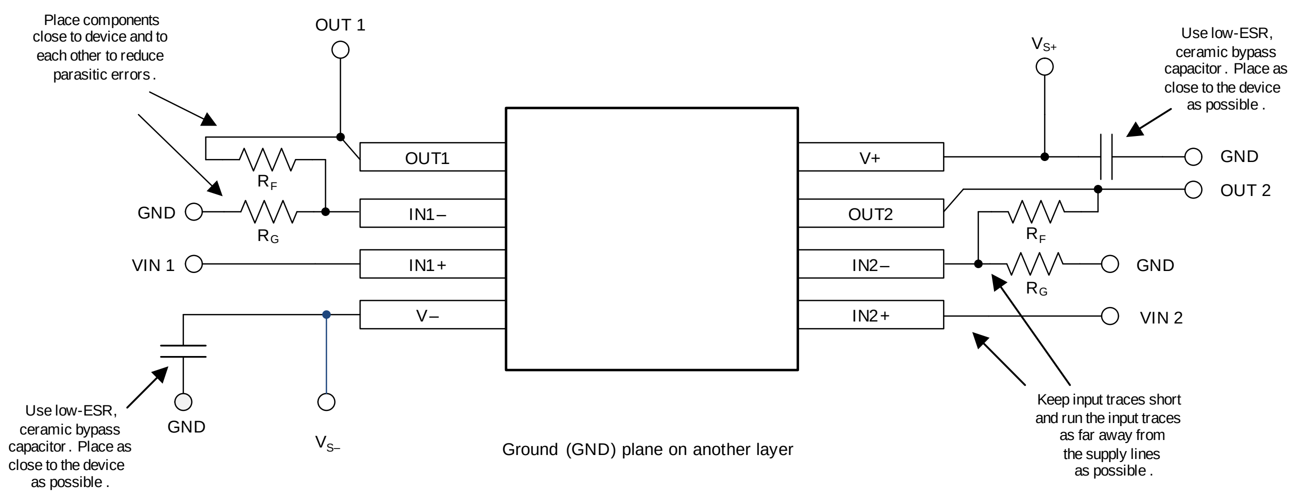


图 41. Layout Example

11 器件和文档支持

11.1 文档支持

11.1.1 相关文档

请参阅如下相关文档：

- *《运算放大器的电磁干扰 (EMI) 抑制比》*
- *《电路板布局布线技巧》*

11.2 接收文档更新通知

要接收文档更新通知，请导航至 TI.com.cn 上的器件产品文件夹。单击右上角的*通知我*进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

11.3 社区资源

下列链接提供到 TI 社区资源的连接。链接的内容由各个分销商"按照原样"提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的 《使用条款》。

TI E2E™ 在线社区 ***TI 的工程师对工程师 (E2E) 社区。*** 此社区的创建目的在于促进工程师之间的协作。在 e2e.ti.com 中，您可以咨询问题、分享知识、拓展思路并与同行工程师一道帮助解决问题。

设计支持 ***TI 参考设计支持*** 可帮助您快速查找有帮助的 E2E 论坛、设计支持工具以及技术支持的联系信息。

11.4 商标

E2E is a trademark of Texas Instruments.

11.5 静电放电警告

ESD 可能会损坏该集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理措施和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。 精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

11.6 术语表

SLYZ022 — *TI 术语表*。

这份术语表列出并解释术语、缩写和定义。

12 机械、封装和可订购信息

以下页面包含机械、封装和可订购信息。这些信息是指定器件的最新可用数据。数据如有变更，恕不另行通知，且不会对此文档进行修订。如需获取此数据表的浏览器版本，请查阅左侧的导航栏。

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
OPA2313QDGKRQ1	ACTIVE	VSSOP	DGK	8	2500	RoHS & Green	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	23131	Samples
OPA2313QDRQ1	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	O2313Q	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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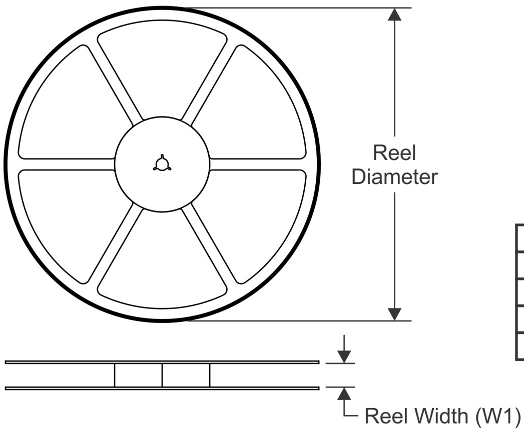
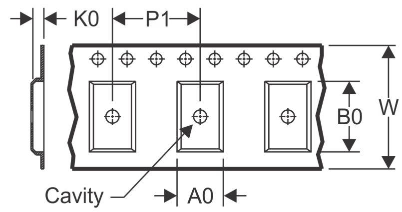
TAPE AND REEL INFORMATION

REEL DIMENSIONS

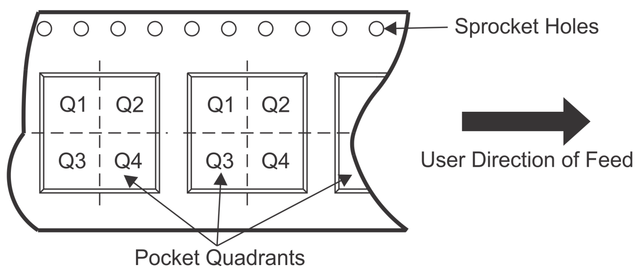


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

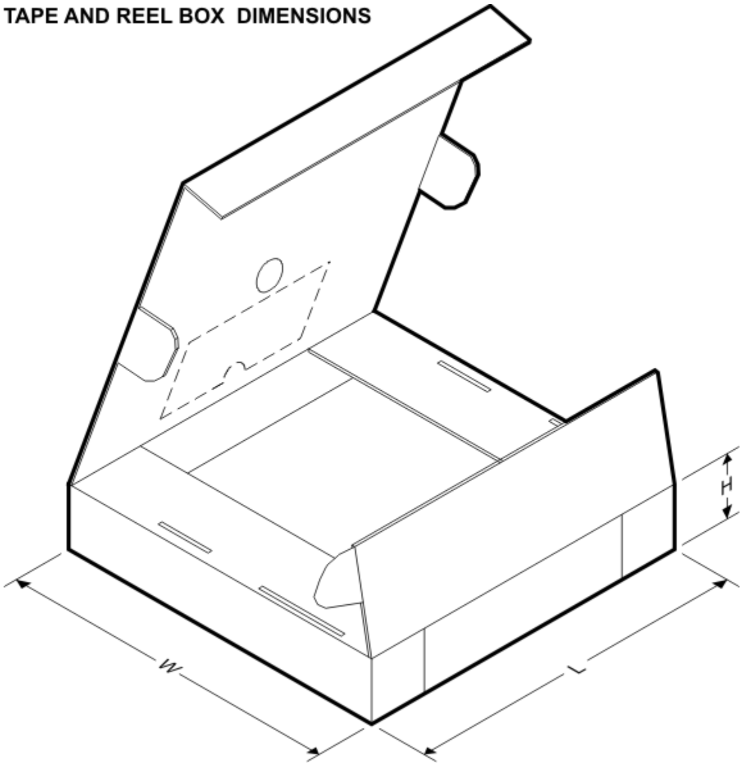
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

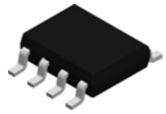
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
OPA2313QDGKRQ1	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
OPA2313QDRQ1	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
OPA2313QDGKRQ1	VSSOP	DGK	8	2500	366.0	364.0	50.0
OPA2313QDRQ1	SOIC	D	8	2500	340.5	336.1	25.0

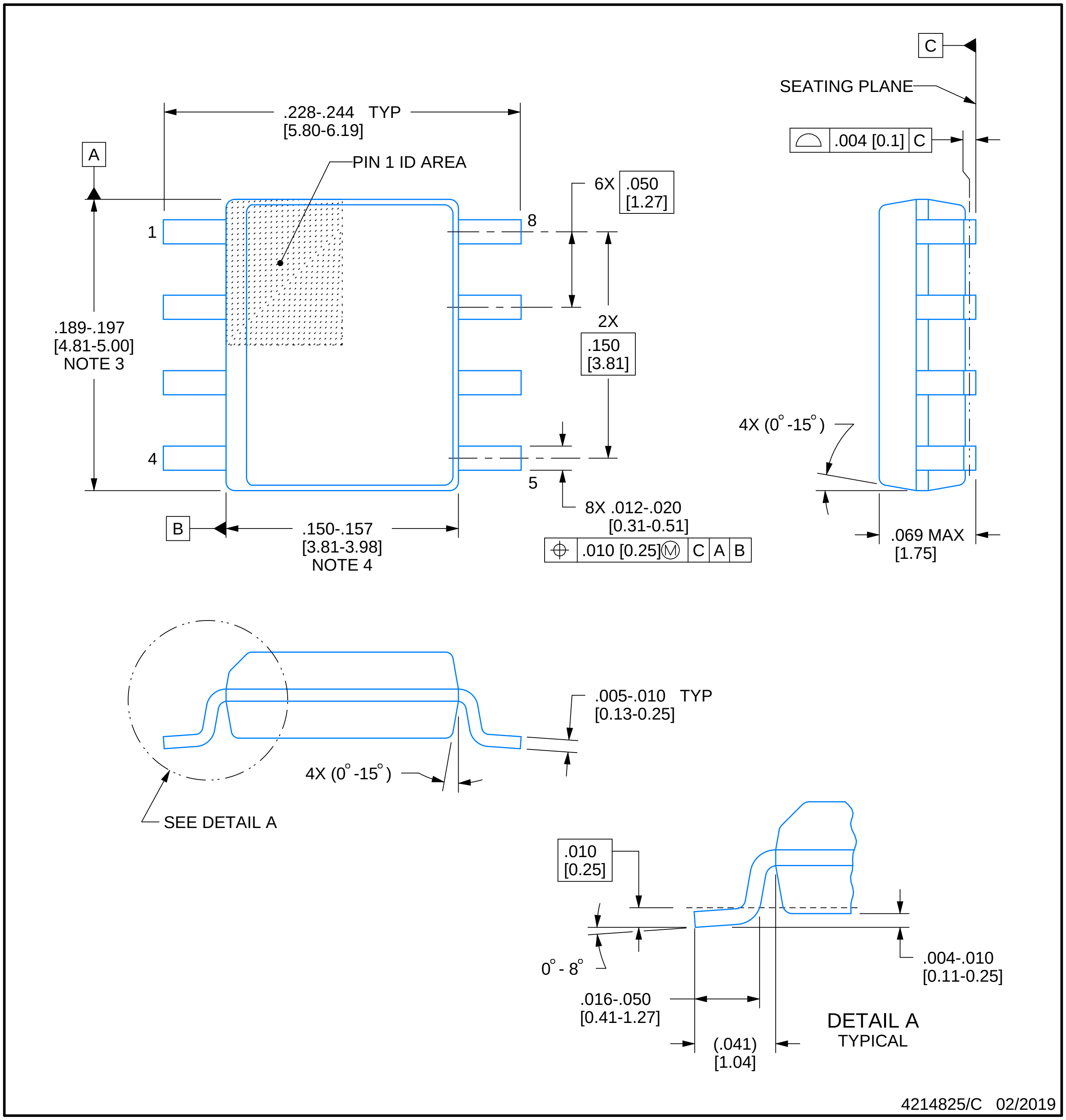


PACKAGE OUTLINE

D0008A

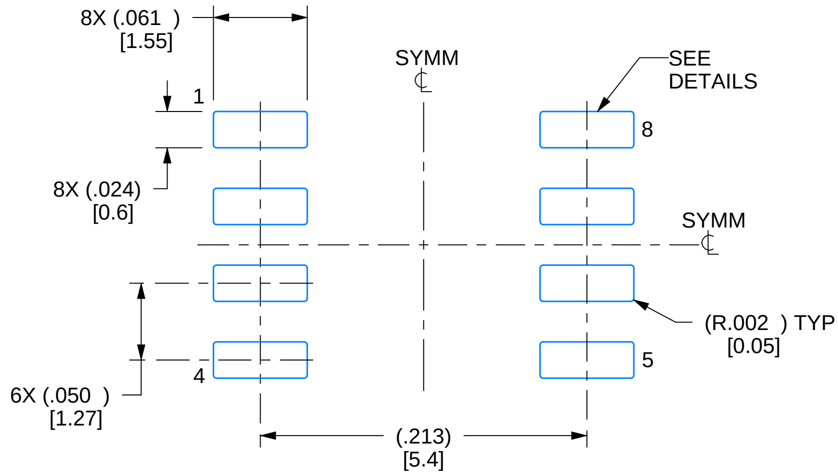
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

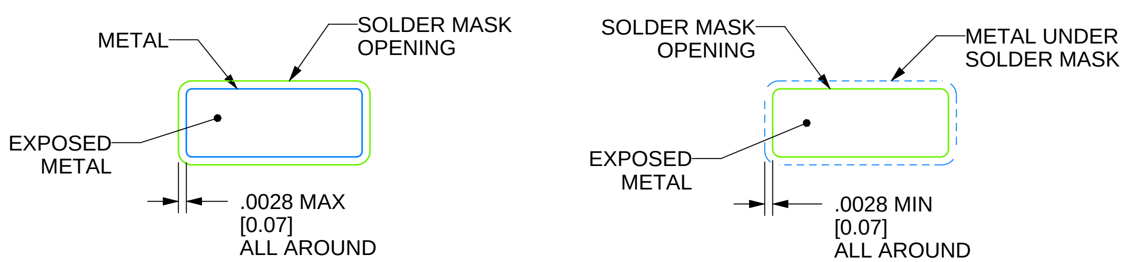


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



NON SOLDER MASK
DEFINED

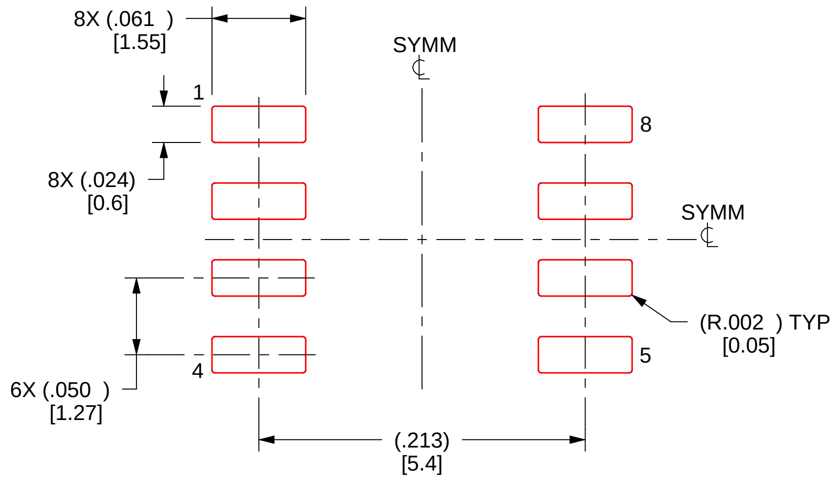
SOLDER MASK
DEFINED

SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

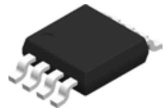


SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

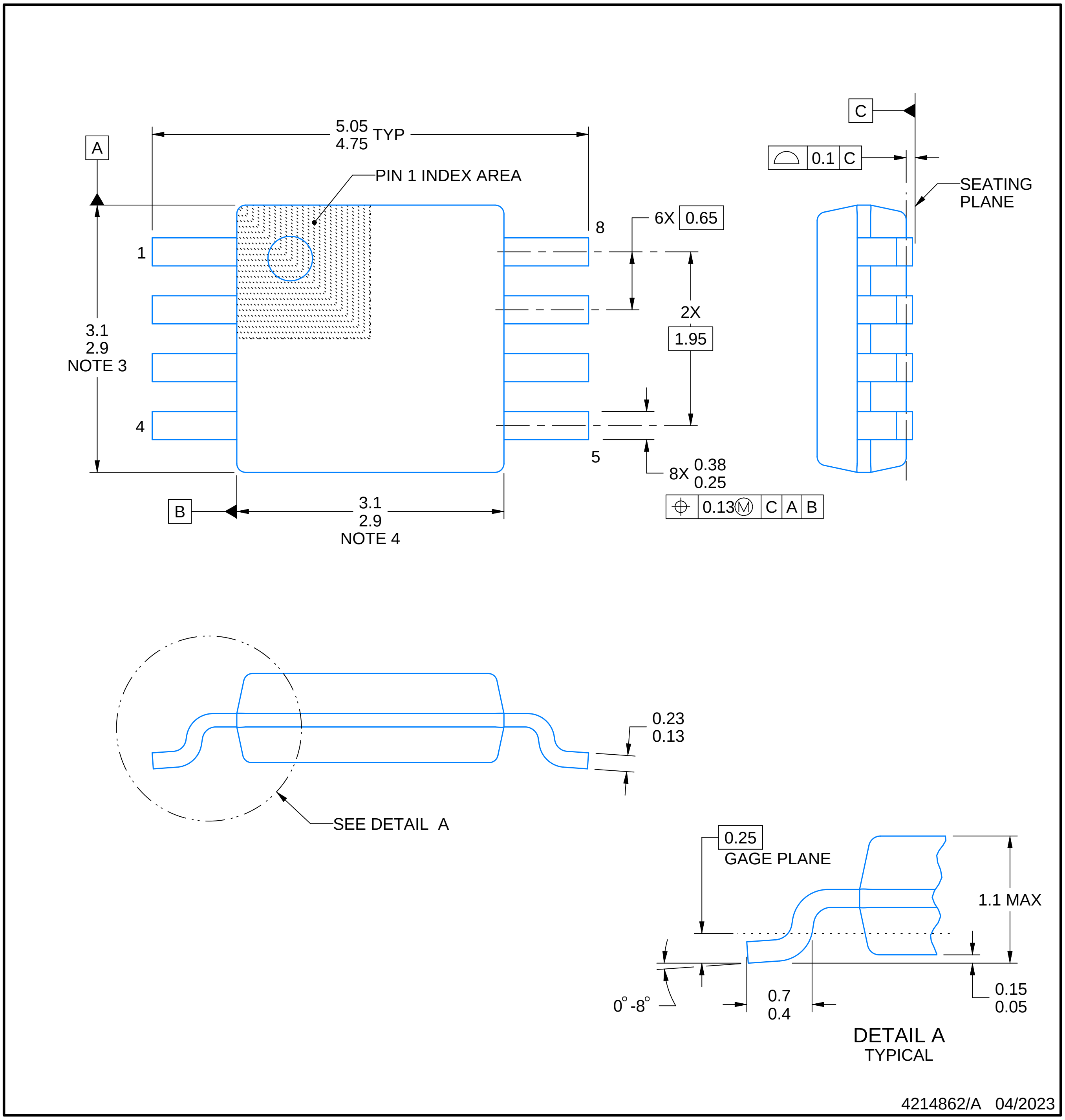
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.



DGK0008A

VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE

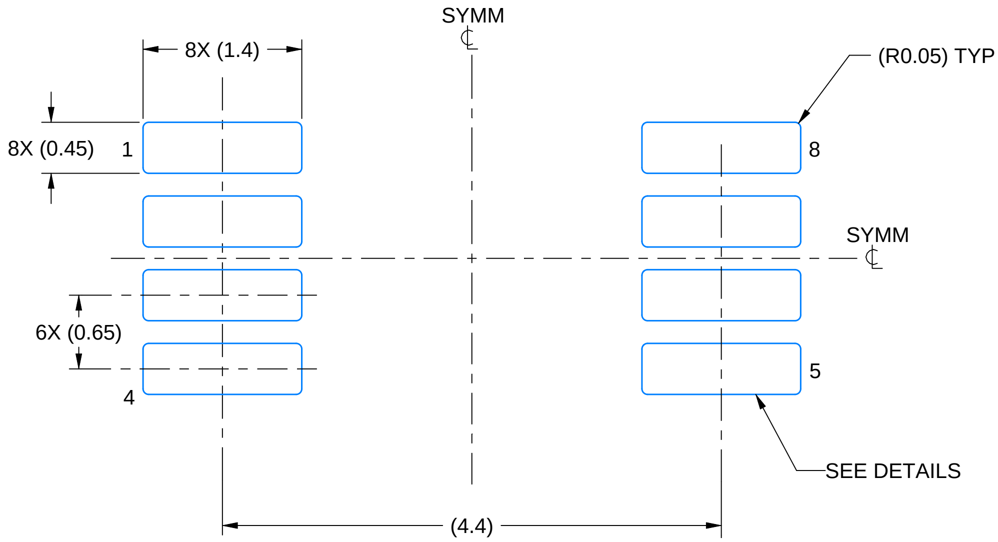


4214862/A 04/2023

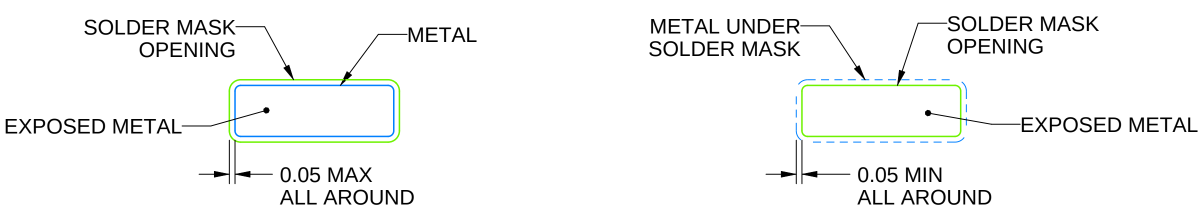
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X



NON-SOLDER MASK
DEFINED
(PREFERRED)

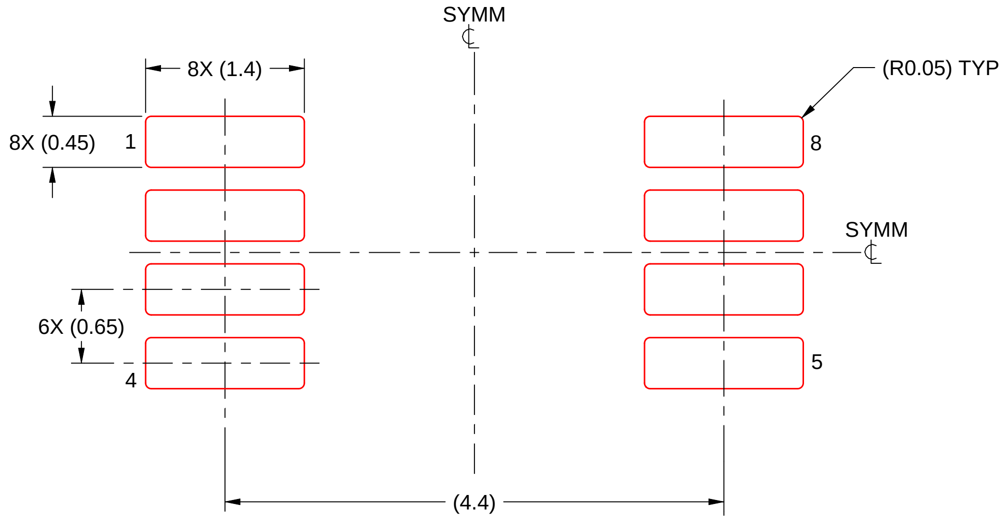
SOLDER MASK
DEFINED

SOLDER MASK DETAILS

4214862/A 04/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.



SOLDER PASTE EXAMPLE
SCALE: 15X

4214862/A 04/2023

NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

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