Single Port, High Output Current VDSL2 Line Driver with Power Control

Check for Samples: OPA2670

FEATURES

- **WIDEBAND +12V OPERATION: 420MHz (G = +5V/V)**
- **HIGH OUTPUT CURRENT: 700mA**
- **OUTPUT VOLTAGE SWING: 9.4V_{PP} into 10Ω Single-Ended Load**
- **HIGH DIFFERENTIAL SLEW RATE: 5000V/μs**
- **LOW SUPPLY CURRENT: 30.5mA**
- **FLEXIBLE POWER CONTROL**

APPLICATIONS

- **POWER LINE MODEM**
- **xDSL LINE DRIVERS**
- **CABLE MODEM DRIVERS**
- **BROADBAND VIDEO LINE DRIVERS**
- **ARB LINE DRIVERS**

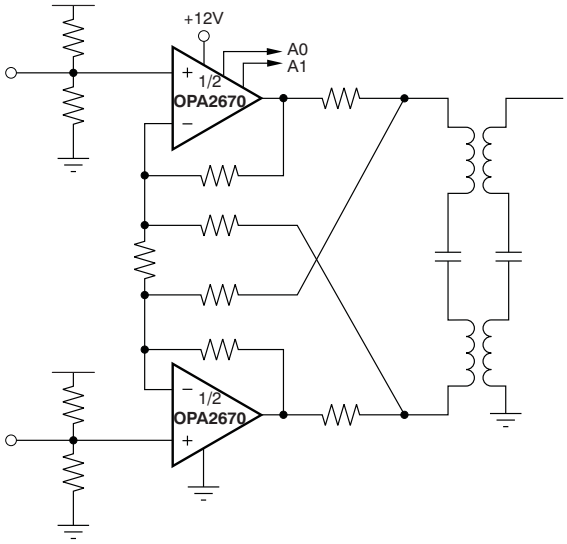
DESCRIPTION

The OPA2670 provides the high output current and low distortion required in emerging xDSL and Power Line Modem driver applications. Operating on a single +12V supply, the OPA2670 consumes a low 30.5mA quiescent current to deliver a very high 700mA output current. This output current supports even the most demanding xDSL requirements with greater than 450mA minimum output current (+25°C minimum value) with low harmonic distortion. Differential driver applications deliver less than –71dBc distortion at the peak upstream power levels of full-rate ADSL. The high 420MHz bandwidth also supports the most demanding VDSL2 line driver requirements.

Power control features are included to allow system power to be minimized. Two logic control lines allow four quiescent power settings, including full power, 66% power, 33% power, and shutdown.

RELATED PRODUCTS

DUALS	NOTES
OPA2673	Single +12V capable, active off-line control
OPA2674	Dual wideband, high output current, operational amplifier with current limit
THS6214	Dual port VDSL2 line driver amplifier



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

PACKAGE/ORDERING INFORMATION(1)

PRODUCT	PACKAGE-LEAD	PACKAGE DESIGNATOR	SPECIFIED TEMPERATURE RANGE	PACKAGE MARKING	ORDERING NUMBER	TRANSPORT MEDIA, QUANTITY
OPA2670	QFN-16	RGV	–40°C to +85°C	OPA2670 IRGV	OPA2670IRGVT	Tape and Reel, 250
					OPA2670IRGVR	Tape and Reel, 2500

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or visit the device product folder at www.ti.com.

ABSOLUTE MAXIMUM RATINGS(1)

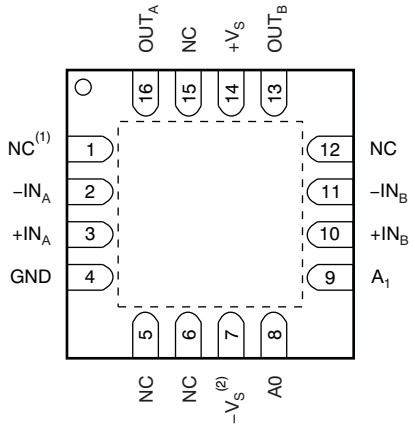
Over operating free-air temperature range, unless otherwise noted.

		OPA2670	UNIT
Supply voltage (–40°C to +85°C)		±6.5	V_{DC}
Supply voltage (0°C to +70°C)		±6.65	V_{DC}
Internal power dissipation		See Thermal Characteristics	
Differential input voltage		±4	V
Input common-mode voltage range		$\pm V_S$	V
Storage temperature range: RGV		–65 to +125	°C
Junction temperature (T_J)		+150	°C
Continuous operating junction temperature		+130	°C
ESD rating	Human body model (HBM)	2000	V
	Charged device model (CDM)	1000	V
	Machine model (MM)	200	V

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

PIN CONFIGURATION

RGV PACKAGE
4×4 QFN-16
(TOP VIEW)



(1) NC = Not connected.

(2) $-V_S$ connected through PowerPAD™.

ELECTRICAL CHARACTERISTICS: V_S = +12V

Boldface limits are tested at +25°C. At T_A = +25°C, A_0 = A_1 = 0 (full power), G = +5V/V, R_F = 432Ω, and R_L = 100Ω, and fully differential specifications, unless otherwise noted. See Figure 38 for ac performance only.

PARAMETER	CONDITIONS	OPA2670IRGV			UNITS	TEST LEVEL (1)
		MIN	TYP	MAX		
AC PERFORMANCE						
Small-signal bandwidth	G = +5V/V, R_F = 750Ω, V_O = 2V_{PP}		420		MHz	C
	G=+10V/V, R_F = 750Ω, V_O = 500mV_{PP}		140		MHz	C
Bandwidth for 0.1dB flatness	G = +5V/V, V_O = 2V_{PP}		80		MHz	C
Large-signal bandwidth	G = +5V/V, V_O = 10V_{PP}		300		MHz	C
Slew rate (differential)	G = +5V/V, 16V step		5000		V/µs	C
Rise-and-fall time (differential)	G = +5V/V, 2V step		1.3		ns	C
Harmonic distortion	G = +5V/V, V_O = 2V_{PP}, 10MHz					
2nd harmonic	R_L = 100Ω, Diff		–71		dBc	C
3rd harmonic	R_L = 100Ω, Diff		–80		dBc	C
Input voltage noise	f > 1MHz, single-ended model		3.6		nV/√Hz	C
Noninverting input current noise	f > 1MHz, single-ended model		6		pA/√Hz	C
Inverting input current noise	f > 1MHz, single-ended model		38		pA/√Hz	C
DC PERFORMANCE (2)						
Open-loop transimpedance gain (Z_{OL})	V_O = 0V, R_L = 100Ω, single-ended amplifier	90	150		kΩ	A
Input offset voltage	V_{CM} = 0V, single-ended amplifier		±2	**±6**	mV	A
	–40°C to +85°C			±7.2	mV	B
Input offset voltage drift	V_{CM} = 0V, single-ended amplifier		±8	±20	µV/°C	B
Input offset voltage matching	V_{CM} = 0V, single-ended amplifier		±0.5	**±4**	mV	A
Noninverting input bias current	V_{CM} = 0V, single-ended amplifier		±6	**±24**	µA	A
	–40°C to +85°C			±26	µA	B
Noninverting input bias current drift	V_{CM} = 0V, single-ended amplifier		±9	±40	nA/°C	B
Noninverting Input bias current matching	V_{CM} = 0V, single-ended amplifier		±0.5	**±5**	µA	A
Inverting input bias current	V_{CM} = 0V, single-ended amplifier		±5	**±34**	µA	A
	–40°C to +85°C			±38	µA	B
Inverting input bias current drift	V_{CM} = 0V, single-ended amplifier		±8	±62	µA/°C	B
INPUT (2)						
Common-mode input range	Each amplifier	**±3.5**	±3.8		V	A
Common-mode rejection ratio	V_{CM} = 0V, input-referred, single-ended amplifier	**50**	56		dB	A
	–40°C to +85°C	48			dB	B
Noninverting input impedance	Each amplifier		1.5 || 1		MΩ || pF	C
Inverting input resistance	Open-loop, each amplifier	16	45	60	Ω	B
Maximum logic 0	A_1, A_0			**0.8**	V	A
Minimum logic 1	A_1, A_0	**2**			V	A
Logic input current	A_1 = 0V, A_0 = 0V, each line		+5	**+10**	µA	A
Shutdown isolation	G = +4V/V, f = 1MHz, A_1 = A_0 = 1		85		dB	C

(1) Test levels: **(A)** 100% tested at +25°C. Over temperature limits set by characterization and simulation. **(B)** Limits set by characterization and simulation. **(C)** Typical value only for information.
(2) Current is considered positive-out-of node. V_{CM} is the input common-mode voltage.

ELECTRICAL CHARACTERISTICS: V_S = +12V (continued)

Boldface limits are tested at +25°C. At T_A = +25°C, A_0 = A_1 = 0 (full power), G = +5V/V, R_F = 432Ω, and R_L = 100Ω, and fully differential specifications, unless otherwise noted. See Figure 38 for ac performance only.

PARAMETER	CONDITIONS	OPA2670IRGV MIN	OPA2670IRGV TYP	OPA2670IRGV MAX	UNITS	TEST LEVEL (1)
OUTPUT						
Voltage output swing	No load, each amplifier		±5		V	C
	50Ω differential load, each amplifier	±4.7	±4.8		V	B
	20Ω differential load, each amplifier	**±4.55**	±4.7		V	A
Output current at full bias (peak)	V_O = 0V, A_1 = 0, A_0 = 0, each amplifier	**±500**	±700		mA	A
Output current at mid bias (peak)	V_O = 0V, A_1 = 0, A_0 = 1, each amplifier	**±500**	±600		mA	A
Output current at low bias (peak)	V_O = 0V, A_1 = 1, A_0 = 0, each amplifier	**±450**	±500		mA	A
Short-circuit current	V_O = 0V, each amplifier		1.2		A	C
Closed-loop output impedance at full bias	G = +4V/V, f ≤ 100kHz, A_1 = 0, A_0 = 0, each amplifier		0.01		Ω	C
Closed-loop output impedance at mid bias	G = +4V/V, f ≤ 1MHz, A_1 = 0, A_0 = 1, each amplifier		0.01		Ω	C
Closed-loop output impedance at low bias	G = +4V/V, f ≤ 1MHz, A_1 = 1, A_0 = 0, each amplifier		0.02		Ω	C
Output impedance at shutdown	each amplifier		25 || 4		kΩ || pF	C
Output switching glitch	Inputs at GND, each amplifier		±20		mV	C
POWER SUPPLY						
Specified operating voltage		+5.5	+12	**+12.6**	V	A
	–40°C to +85°C			+12.6	V	B
Quiescent current at full bias	V_S = +12V, A_1 = 0, A_0 = 0	**29.5**	30.5	**31.5**	mA	A
	–40°C to +85°C	28.5		32.5	mA	B
Supply current at mid bias	V_S = +12V, A_1 = 0, A_0 = 1	**20**	22	**24**	mA	A
	–40°C to +85°C	19		25	mA	B
Supply current at low bias	V_S = +12V, A_1 = 1, A_0 = 0	**13**	14	**16**	mA	A
	–40°C to +85°C	12		17	mA	B
Supply current (disabled)	V_S = +12V, A_1 = 1, A_0 = 1		0.9	**1**	mA	A
	–40°C to +85°C			1.2	mA	B
Supply current step time	Time to reach 90% final value		250		ns	C
Power-supply rejection ratio (+PSRR)	Input-referred	**48**	54		dB	A
THERMAL CHARACTERISTICS						
Specified operating temperature range	R_GV package		–40 to +85		°C	C
Thermal resistance, θ_{JA}	Junction-to-ambient					
RGV QFN-16	PowerPAD soldered to PCB		51.2		°C/W	C
	PowerPAD floating (3)		75		°C/W	C

(3) PowerPAD is physically connected to the negative supply (–V_S) for dual-supply configuration or the ground (GND) for single-supply configuration.

THERMAL INFORMATION

THERMAL METRIC (1)		OPA2670 RGV 16 PINS	UNITS
θ_{JA}	Junction-to-ambient thermal resistance	51.2	°C/W
θ_{JCtop}	Junction-to-case (top) thermal resistance	56.7	
θ_{JB}	Junction-to-board thermal resistance	54.3	
ψ_{JT}	Junction-to-top characterization parameter	3.5	
ψ_{JB}	Junction-to-board characterization parameter	35.6	
θ_{JCbot}	Junction-to-case (bottom) thermal resistance	2.5	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

TYPICAL CHARACTERISTICS: Full Bias

At T_A = +25°C, I_Q = 30.5mA, Full Bias, and $R_{L\_Differential}$ = 100Ω, unless otherwise noted.

SMALL-SIGNAL FREQUENCY RESPONSE

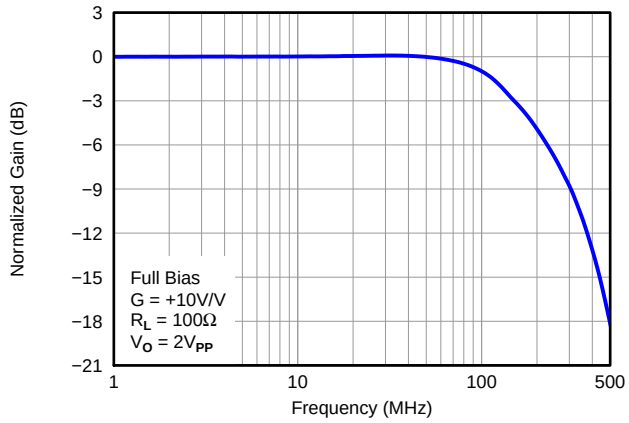


Figure 1.

SMALL-SIGNAL FREQUENCY RESPONSE

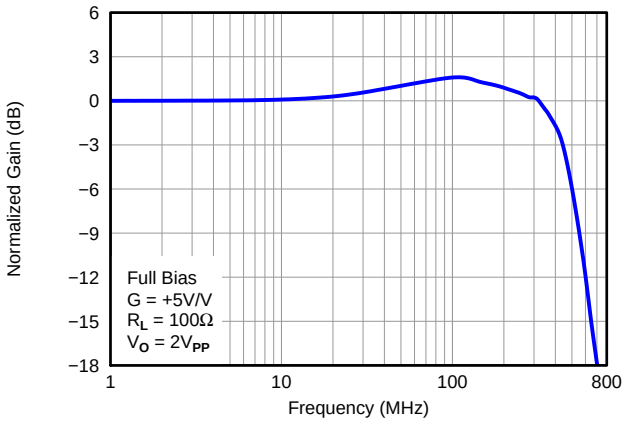


Figure 2.

LARGE-SIGNAL FREQUENCY RESPONSE

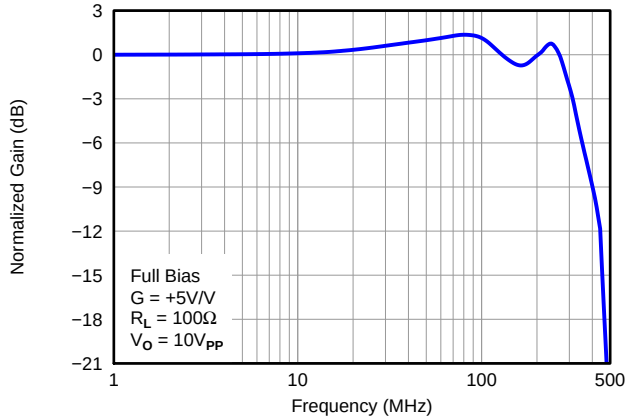


Figure 3.

OUTPUT VOLTAGE AND OUTPUT CURRENT LIMITATIONS

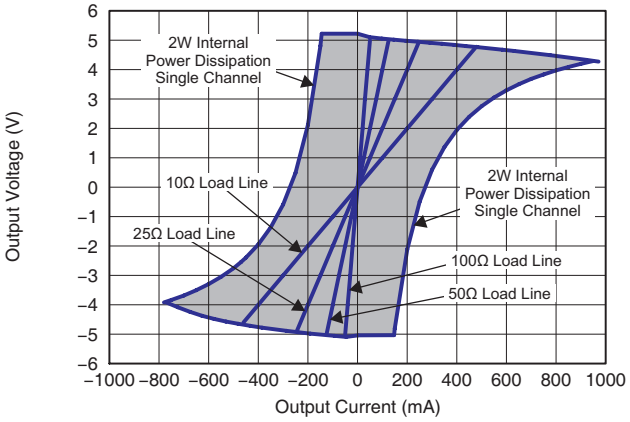


Figure 4.

OVERDRIVE RECOVERY

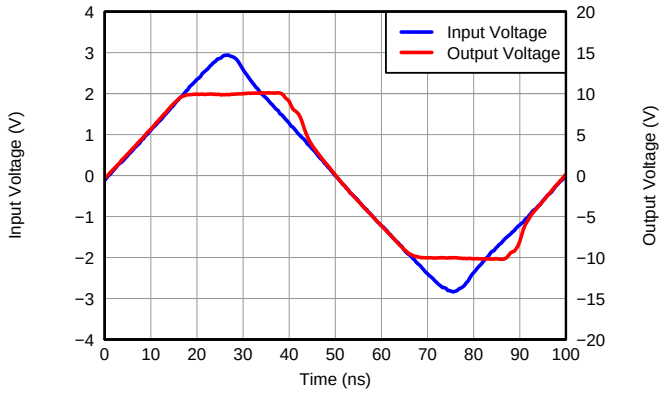


Figure 5.

INPUT OFFSET VOLTAGE

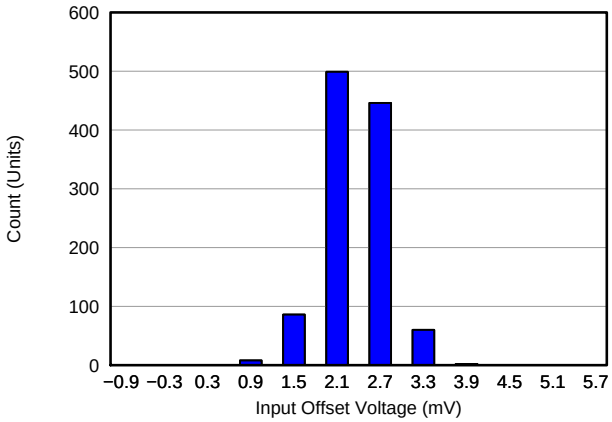


Figure 6.

TYPICAL CHARACTERISTICS: Full Bias (continued)

At T_A = +25°C, I_Q = 30.5mA, Full Bias, and $R_{L\_Differential}$ = 100Ω, unless otherwise noted.

HARMONIC DISTORTION vs FREQUENCY

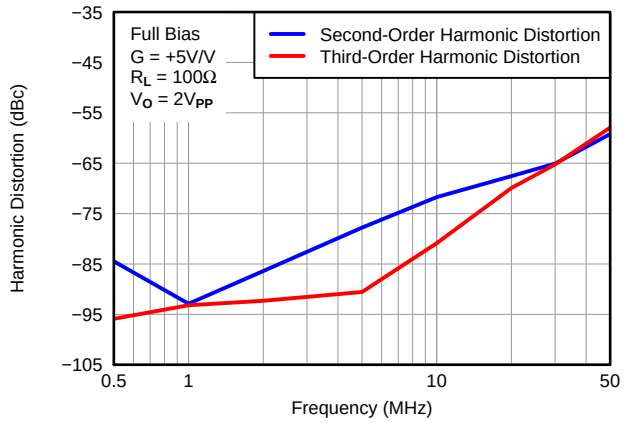


Figure 7.

HARMONIC DISTORTION vs LOAD

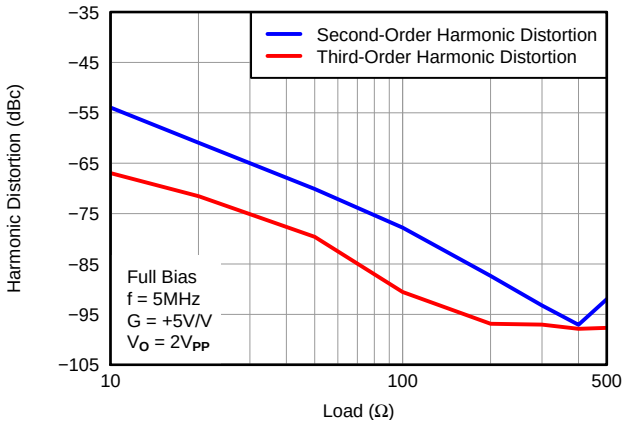


Figure 8.

HARMONIC DISTORTION vs OUTPUT VOLTAGE

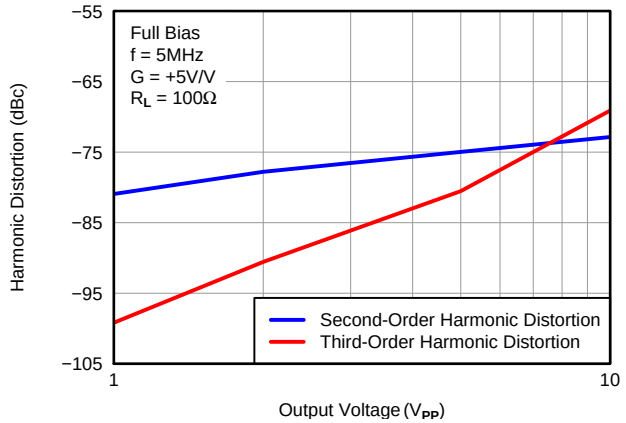


Figure 9.

HARMONIC DISTORTION vs SUPPLY VOLTAGE

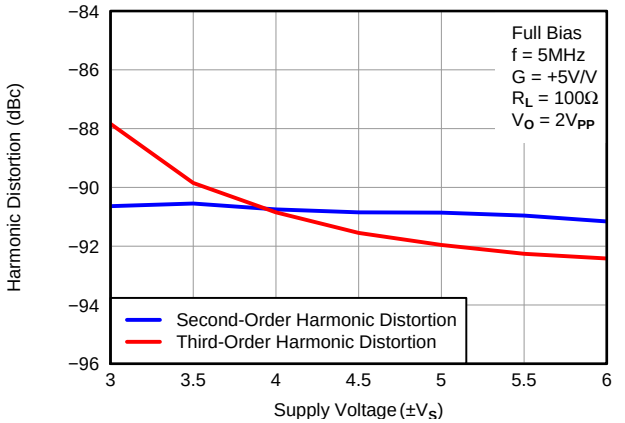


Figure 10.

HARMONIC DISTORTION vs BIAS CURRENT

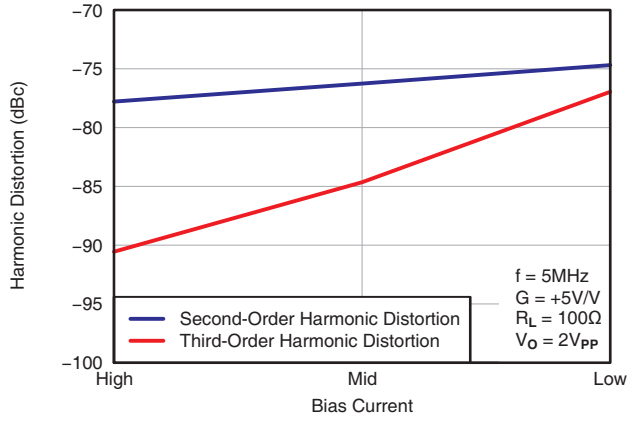


Figure 11.

TWO-TONE, THIRD-ORDER INTERMODULATION INTERCEPT

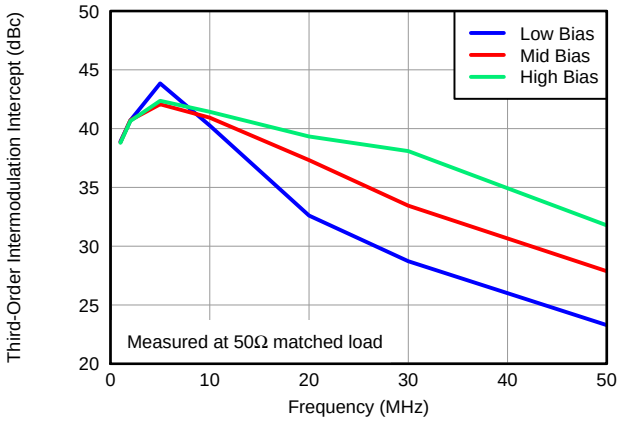


Figure 12.

TYPICAL CHARACTERISTICS: Full Bias (continued)

At T_A = +25°C, I_Q = 30.5mA, Full Bias, and $R_{L\_Differential}$ = 100Ω, unless otherwise noted.

LARGE-SIGNAL ENABLE/DISABLE RESPONSE

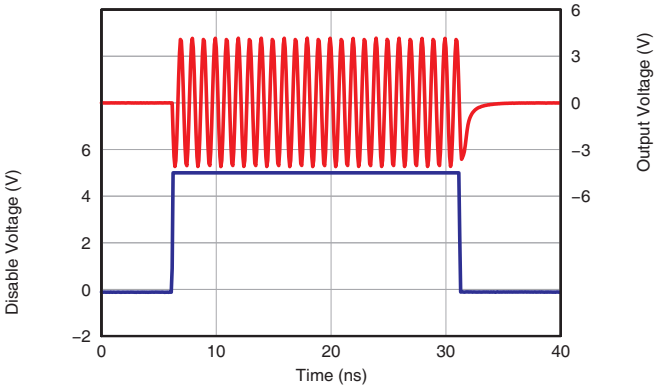


Figure 13.

DISABLE FEEDTHROUGH vs FREQUENCY

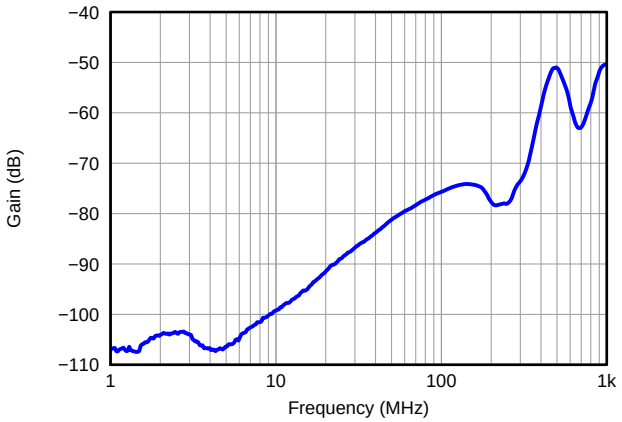


Figure 14.

OPEN-LOOP TRANSIMPEDANCE GAIN AND PHASE

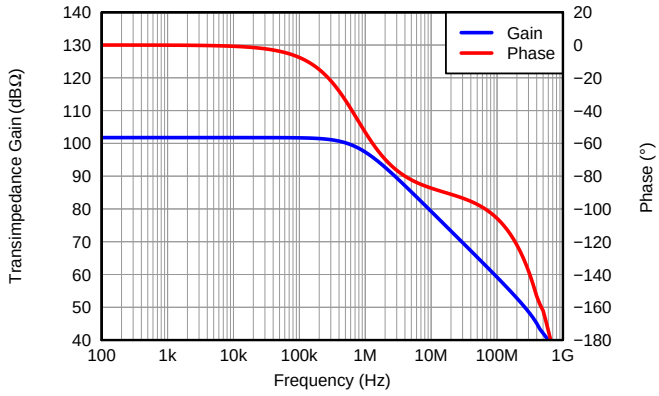


Figure 15.

INPUT NOISE DENSITY

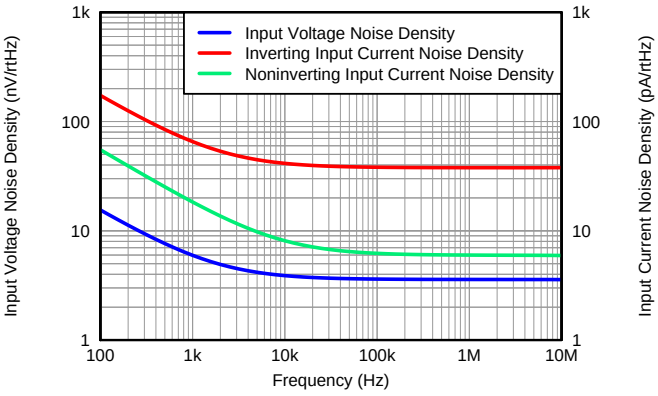


Figure 16.

COMMON-MODE REJECTION RATIO AND POWER-SUPPLY REJECTION RATIO

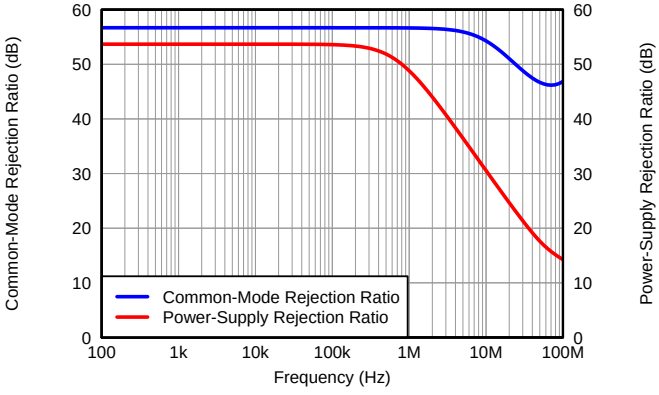


Figure 17.

OUTPUT IMPEDANCE

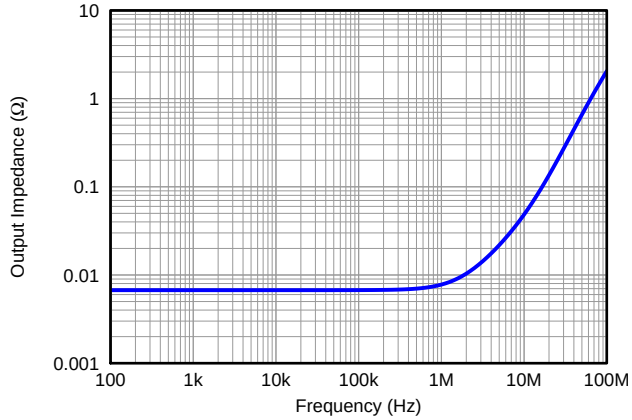


Figure 18.

TYPICAL CHARACTERISTICS: Full Bias (continued)

At T_A = +25°C, I_Q = 30.5mA, Full Bias, and $R_{L\_Differential}$ = 100Ω, unless otherwise noted.

QUIESCENT CURRENT AND OUTPUT CURRENT vs TEMPERATURE

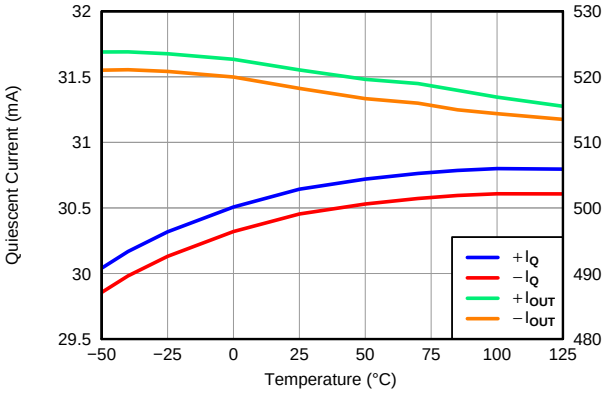


Figure 19.

TYPICAL DC DRIFT vs TEMPERATURE

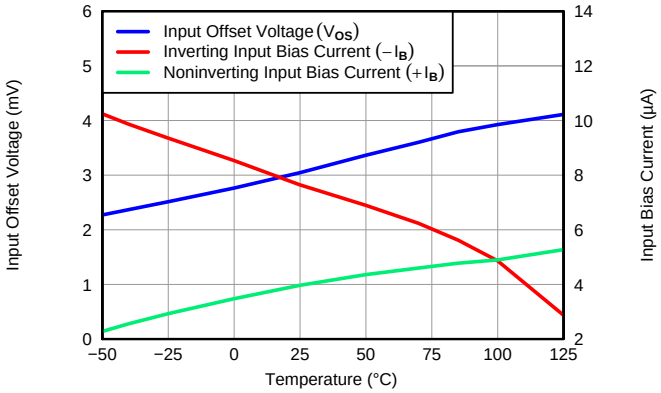


Figure 20.

TYPICAL DC DRIFT MATCHING vs TEMPERATURE

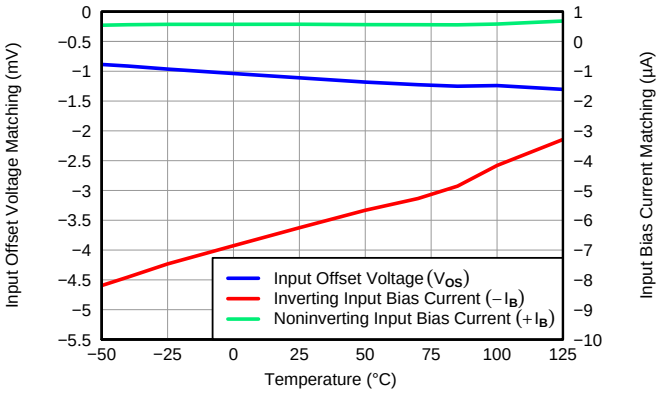


Figure 21.

QUIESCENT CURRENT vs SUPPLY VOLTAGE

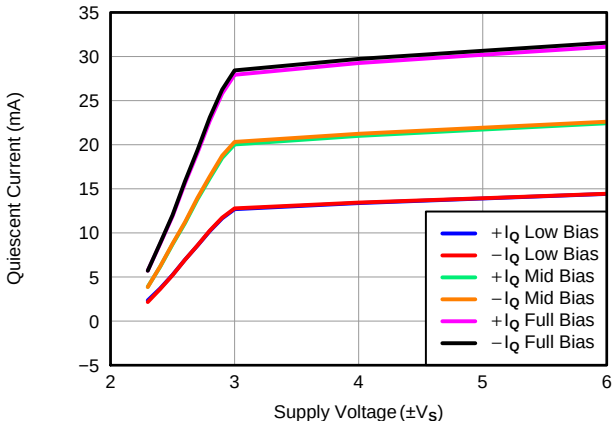


Figure 22.

SERIES RESISTANCE vs CAPACITIVE LOAD

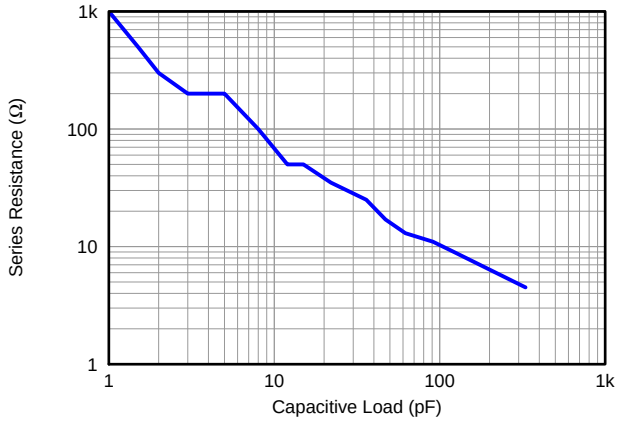


Figure 23.

SMALL-SIGNAL FREQUENCY RESPONSE vs FREQUENCY

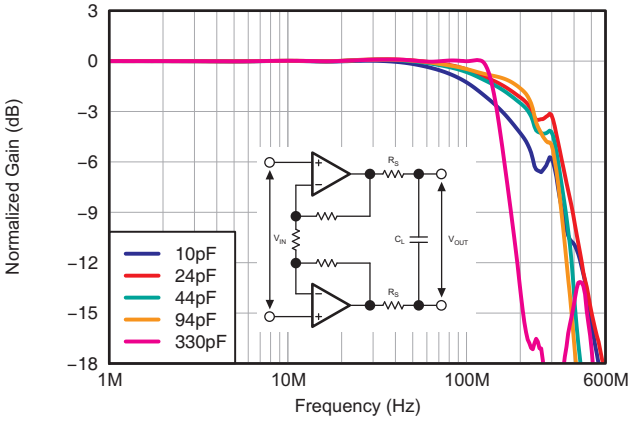


Figure 24.

TYPICAL CHARACTERISTICS: Full Bias (continued)

At T_A = +25°C, I_Q = 30.5mA, Full Bias, and $R_{L\_Differential}$ = 100Ω, unless otherwise noted.

PULSE RESPONSE

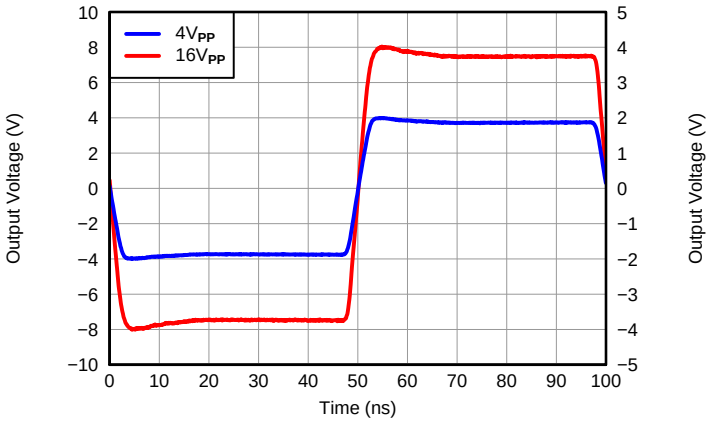


Figure 25.

TYPICAL CHARACTERISTICS: Mid Bias

At T_A = +25°C, I_Q = 22mA, Mid Bias, and $R_{L\_Differential}$ = 100Ω, unless otherwise noted.

SMALL-SIGNAL FREQUENCY RESPONSE

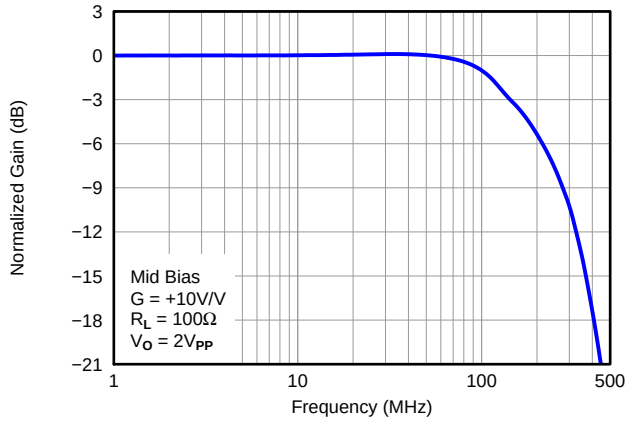


Figure 26.

SMALL-SIGNAL FREQUENCY RESPONSE

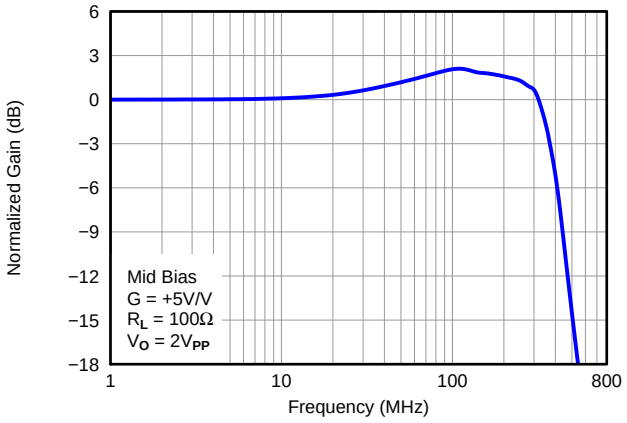


Figure 27.

LARGE-SIGNAL FREQUENCY RESPONSE

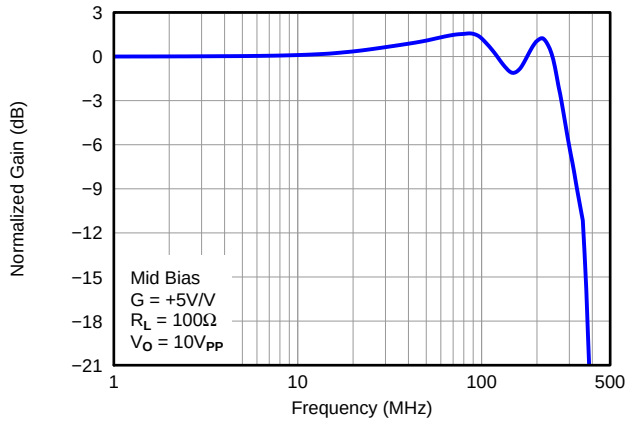


Figure 28.

HARMONIC DISTORTION vs FREQUENCY

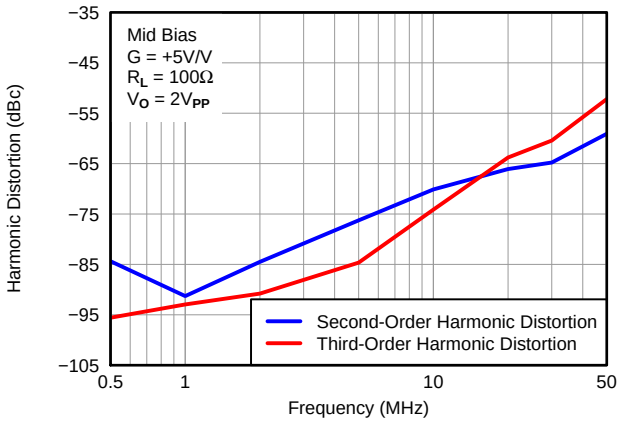


Figure 29.

HARMONIC DISTORTION vs LOAD

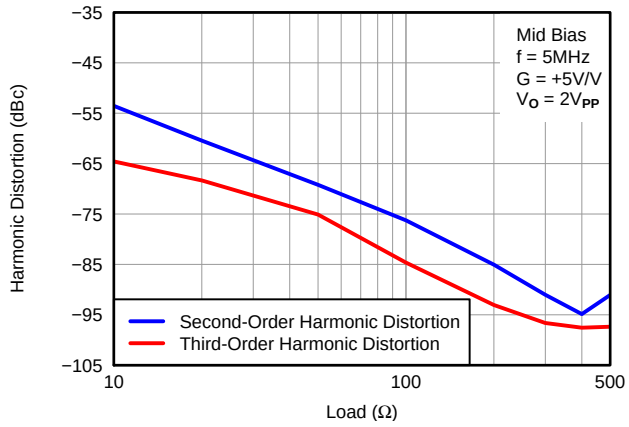


Figure 30.

HARMONIC DISTORTION vs OUTPUT VOLTAGE

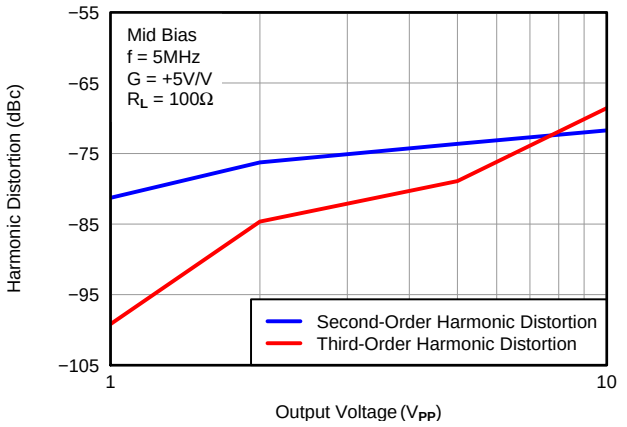


Figure 31.

TYPICAL CHARACTERISTICS: Low Bias

At T_A = +25°C, I_Q = 14mA, Low Bias, and $R_{L\_Differential}$ = 100Ω, unless otherwise noted.

SMALL-SIGNAL FREQUENCY RESPONSE

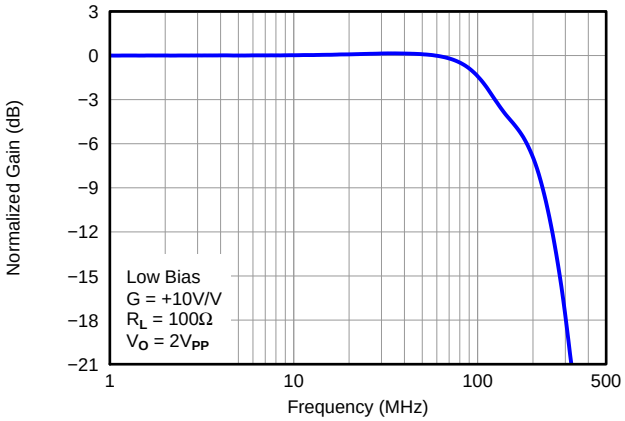


Figure 32.

SMALL-SIGNAL FREQUENCY RESPONSE

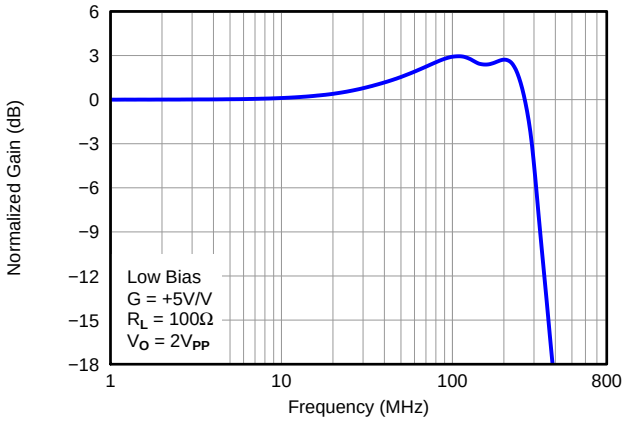


Figure 33.

LARGE-SIGNAL FREQUENCY RESPONSE

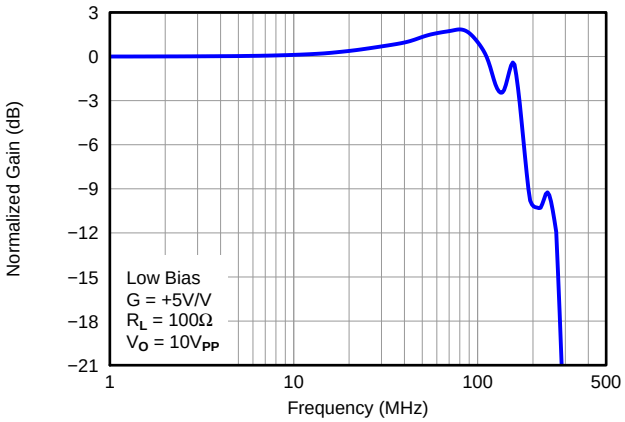


Figure 34.

HARMONIC DISTORTION vs FREQUENCY

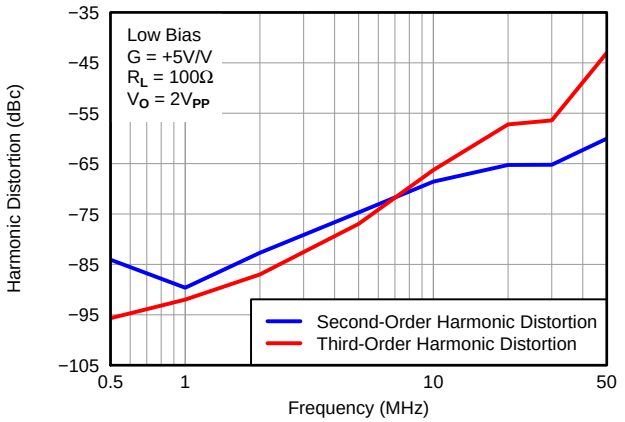


Figure 35.

HARMONIC DISTORTION vs LOAD

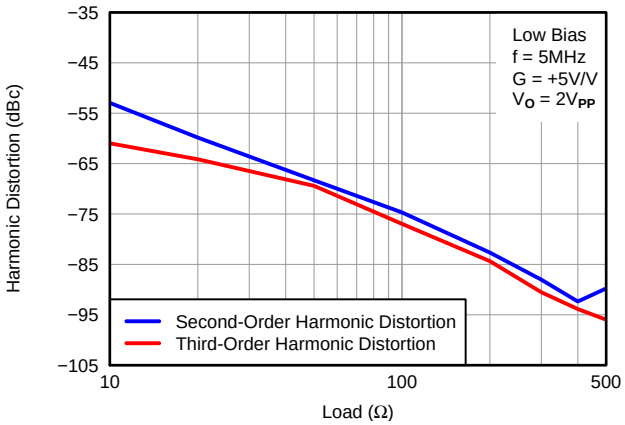


Figure 36.

HARMONIC DISTORTION vs OUTPUT VOLTAGE

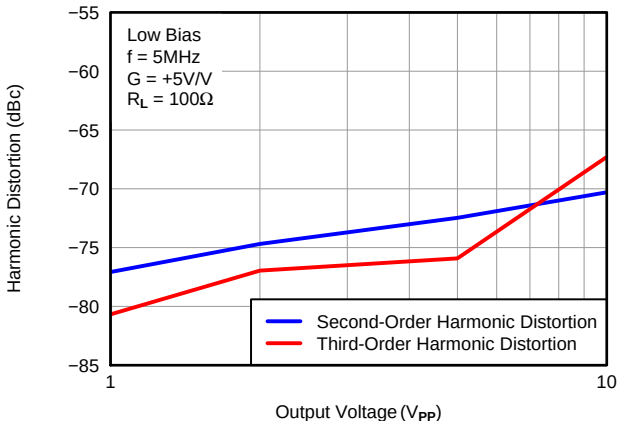


Figure 37.

APPLICATION INFORMATION

WIDEBAND CURRENT-FEEDBACK OPERATION

The OPA2670 provides the exceptional ac performance of a wideband current-feedback op amp with a highly linear, high-power output stage. Requiring only 21mA/port quiescent current, the OPA2670 swings to within 1V of either supply rail on a 100Ω load and delivers in excess of 700mA at room temperature. This low-output headroom requirement, along with supply voltage independent biasing, provides remarkable +12V supply operation. The OPA2670 delivers greater than 420MHz bandwidth driving a $2V_{PP}$ output into 100Ω on a +12V supply. Previous boosted output stage amplifiers typically suffer from very poor crossover distortion as the output current goes through zero. The OPA2670 achieves a comparable power gain with much better linearity. The primary advantage of a current-feedback op amp over a voltage-feedback op amp is that ac performance (bandwidth and distortion) is relatively independent of signal gain. Figure 38 shows the dc-coupled, gain of +10V/V, dual power-supply circuit configuration used as the basis of the +12V Electrical and Typical Characteristics. For test purposes, the input impedance is set to 50Ω with a resistor to ground and the output impedance is set to 50Ω with a series output resistor. Voltage swings reported in the Electrical Characteristics are taken directly at the input and output pins, whereas load powers (dBm) are defined at a matched 50Ω load. For the circuit of Figure 38, the total effective load is 100Ω || 750Ω || 750Ω = 78.9Ω.

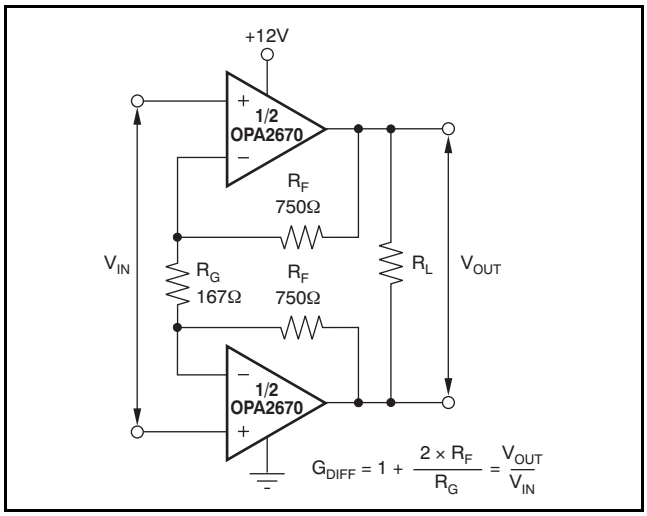


Figure 38. Noninverting Differential I/O Amplifier

This approach allows the user to set a source termination impedance at the input that is independent of the signal gain. For instance, simple differential filters may be included in the signal path right up to the noninverting inputs with no interaction with the gain setting. The differential signal gain for the circuit of Figure 38 is:

$$A_D = 1 + 2 \times \frac{R_F}{R_G} \quad (1)$$

Where A_D = differential gain.

Figure 38 shows a value of 167Ω for the A_D = +10V/V design. Because the OPA2670 is a current feedback (CFB) amplifier, its bandwidth is primarily controlled with the feedback resistor value; the differential gain, however, may be adjusted with considerable freedom using just the R_G resistor. In fact, R_G may be reduced by a reactive network that provides a very isolated shaping to the differential frequency response.

Various combinations of single-supply or ac-coupled gain can also be delivered using the basic circuit of Figure 38. Common-mode bias voltages on the two noninverting inputs pass on to the output with a gain of +1V/V because an equal dc voltage at each inverting node creates no current through R_G. This circuit does show a common-mode gain of +1V/V from input to output. The source connection should either remove this common-mode signal if undesired (using an input transformer can provide this function), or the common-mode voltage at the inputs can be used to set the output common-mode bias. If the low common-mode rejection of this circuit is a problem, the output interface can also be used to reject that common-mode. For instance, most modern differential input analog-to-digital converters (ADCs) reject common-mode signals very well, while a line driver application through a transformer also attenuates the common-mode signal through to the line.

DUAL-SUPPLY VDSL DOWNSTREAM

Figure 39 shows an example of a dual-supply VDSL downstream driver. Both channels of the OPA2670 are configured as a differential gain stage to provide signal drive to the primary winding of the transformer (in Figure 39, a step-up transformer with a turns ratio of 1:n). The main advantage of this configuration is the cancellation of all even harmonic-distortion products. Another important advantage for VDSL is that each amplifier must only swing half of the total output required driving the load.

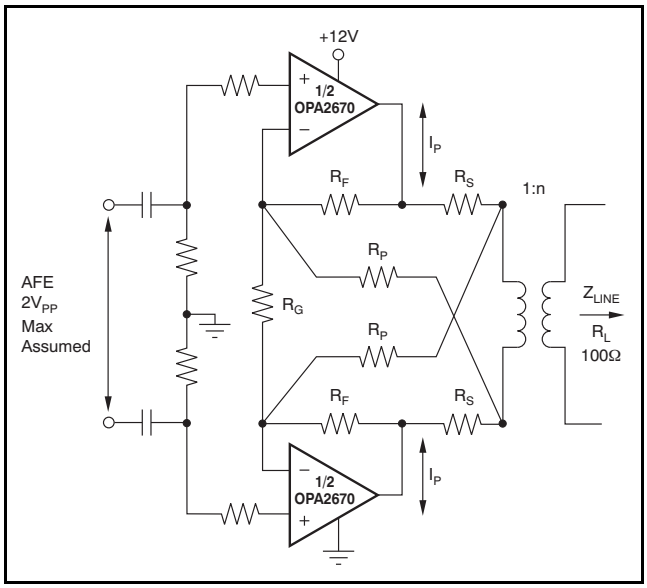


Figure 39. Dual-Supply VDSL Downstream Driver

The analog front-end (AFE) signal is ac-coupled to the driver, and the noninverting input of each amplifier is biased to the mid-supply voltage (ground in this case). In addition to providing the proper biasing to the amplifier, this approach also provides a high-pass filtering with a corner frequency. Because the signal bandwidth starts at 26kHz, this high-pass filter does not generate any problem and has the advantage of filtering out unwanted lower frequencies.

The input signal is amplified with a gain set by the following equation:

$$G_D = 1 + \frac{2 \times R_F}{R_G} \quad (2)$$

The two back-termination resistors (R_S) added at each terminal of the transformer make the impedance of the modem match the impedance of the phone line, and also provide a means of detecting the received signal for the receiver. The value of these resistors (R_S) is a function of the line impedance and the transformer turns ratio (n), given by the following equation:

$$R_S = \frac{Z_{LINE}}{2n^2} \quad (3)$$

LINE DRIVER HEADROOM MODEL

The first step in a transformer-coupled, twisted-pair driver design is to compute the peak-to-peak output voltage from the target specifications. This calculation is done using the following equations:

$$P_L = 10 \times \log \frac{V_{RMS}^2}{(1mW) \times R_L} \quad (4)$$

with:

- P_L = power at the load
- V_{RMS} = voltage at the load
- R_L = load impedance

These values produce the following:

$$V_{RMS} = \sqrt{(1mW) \times R_L \times 10^{\frac{P_L}{10}}} \quad (5)$$

$$V_P = \text{CrestFactor} \times V_{RMS} = CF \times V_{RMS} \quad (6)$$

with:

- V_P = peak voltage at the load
- C_F = Crest Factor

$$V_{LPP} = 2 \times CF \times V_{RMS} \quad (7)$$

with V_{LPP} = peak-to-peak voltage at the load.

Consolidating Equation 4 through Equation 7 allows us to express the required peak-to-peak voltage at the load as a function of the crest factor, the load impedance, and the power at the load. Thus:

$$V_{LPP} = 2 \times CF \times \sqrt{(1mW) \times R_L \times 10^{\frac{P_L}{10}}} \quad (8)$$

V_{LPP} is usually computed for a nominal line impedance and may be taken as a fixed design target.

The next step in the design is to compute the individual amplifier output voltage and currents as a function of peak-to-peak voltage on the line and transformer turns ratio.

As this turns ratio changes, the minimum allowed supply voltage changes along with it. The peak current in the amplifier output is given by:

$$\pm I_P = \frac{1}{2} \times \frac{2 \times V_{LPP}}{n} \times \frac{1}{4R_S} \quad (9)$$

with V_{PP} as defined in Equation 8, and R_M as defined in Equation 3 and shown in Figure 40.

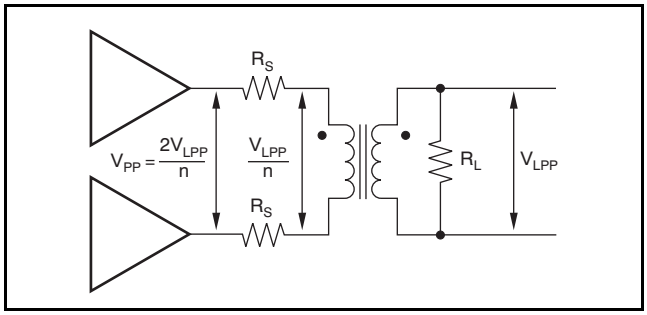


Figure 40. Driver Peak Output Voltage

With the previous information available, it is now possible to select a supply voltage and the turns ratio desired for the transformer, as well as calculate the headroom for the OPA2670.

The model, shown in Figure 41, can be described with the following set of equations:

1. As the available output swing:

$$V_{PP} = V_{CC} - (V_1 + V_2) - I_P \times (R_1 + R_2) \quad (10)$$

2. Or as the required supply voltage:

$$V_{CC} = V_{PP} + (V_1 + V_2) + I_P \times (R_1 + R_2) \quad (11)$$

The minimum supply voltage for power and load requirements is given by Equation 11.

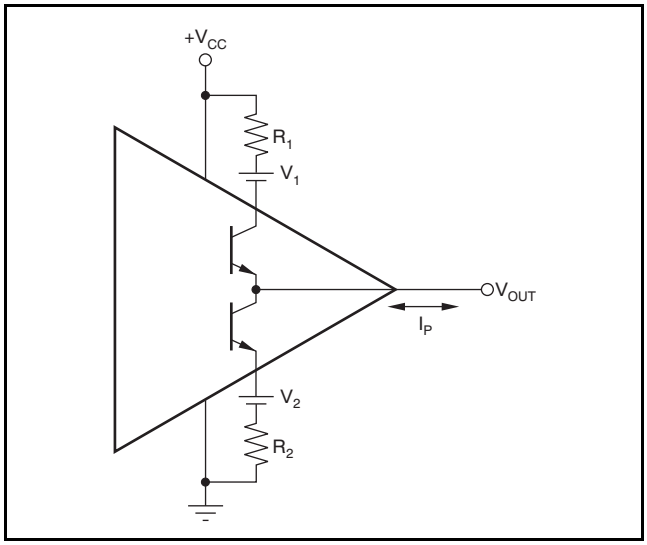


Figure 41. Line Driver Headroom Model

V_1,V_2, R_1, and R_2 are given in Table 1 for +12V operation.

Table 1. Line Driver Headroom Model Values

	V_1	R_1	V_2	R_2
+12V	0.8V	0.3Ω	0.8V	0.6Ω

When using a synthetic output impedance circuit (see Figure 39), a significant drop is noticed in bandwidth from the specification that appears in the Electrical Characteristics table. This apparent drop in bandwidth for the differential signal is a result of the apparent increase in the feedback transimpedance as seen for each amplifier. This feedback transimpedance equation is given below.

$$Z_{FB} = R_F \times \frac{1 + 2 \times \frac{R_S}{R_L} + \frac{R_S}{R_P}}{1 + 2 \times \frac{R_S}{R_L} + \frac{R_S}{R_P} - \frac{R_F}{R_P}} \quad (12)$$

To increase 0.1dB flatness to the frequency of interest, adding a serial RC in parallel with the gain resistor may be needed, as shown in Figure 42.

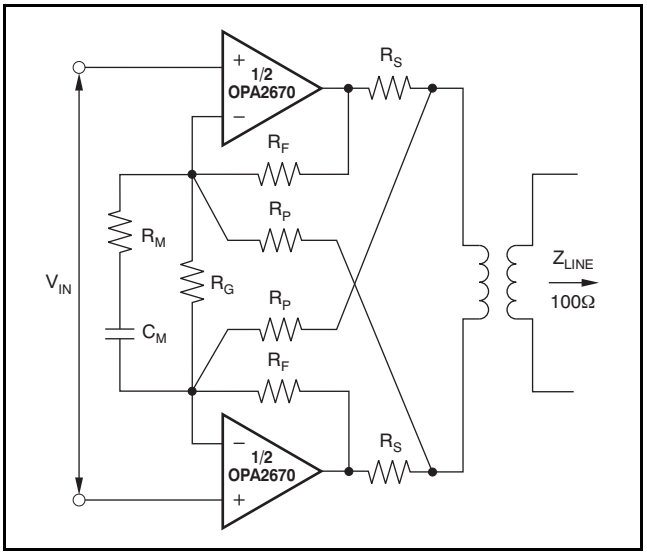


Figure 42. +0.1dB Flatness Compensation Circuit

TOTAL DRIVER POWER FOR xDSL APPLICATIONS

The total internal power dissipation for the OPA2670 in an xDSL line driver application is the sum of the quiescent power and the output stage power. The OPA2670 holds a relatively constant quiescent current versus supply voltage—giving a power contribution that is simply the quiescent current times the supply voltage used. The total output stage power can be computed with reference to Figure 43.

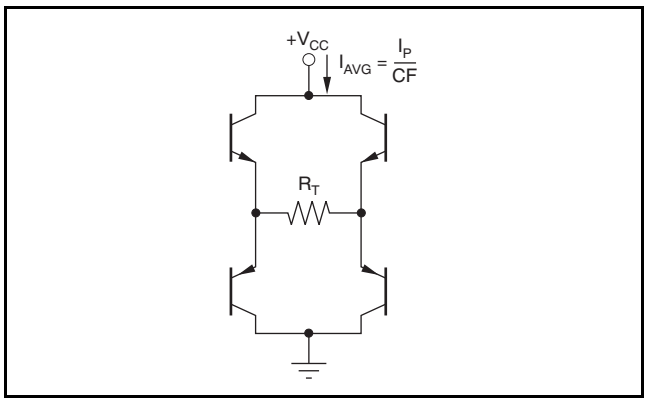


Figure 43. Output Stage Power Model

The two output stages used to drive the load of Figure 40 can be seen as an H-Bridge in Figure 43. The average current drawn from the supply into this H-Bridge and load is the peak current in the load divided by the crest factor (CF) for the xDSL modulation. This total power from the supply is then reduced by the power in R_T, leaving the power dissipated internal to the drivers in the four output stage transistors. That power is simply the target line power used in Equation 4 plus the power lost in the matching elements (R_S). In the following examples, a perfect match is targeted giving the same power in the matching elements as in the load.

For a target line power of 100mW into 100Ω, the voltage at the load is $3.16V_{RMS}$ and the current is $31.6mA_{RMS}$. Bringing this load current to the amplifier side and using a 1:2 turns ratio to be $63.2mA_{RMS}$, the average current is then:

$$I_{AVG} = 63.2mA_{RMS} \times \sqrt{2} \times \frac{2}{\pi} = 56.89mA \text{ (average)} \quad (13)$$

With a +12V power supply, the average driving power is 683mW.

If the total quiescent current is used to drive the load, the total average power consumption for Low Bias mode is then (per port):

$$12V \times 14mA \times \frac{2}{5} + 683mW = 750mW \quad (14)$$

OUTPUT CURRENT AND VOLTAGE

The OPA2670 provides output voltage and current capabilities that are unsurpassed in a low-cost, dual monolithic op amp. The output voltage for a 50Ω differential load tested at +25°C typically swings closer than 1.3V to either supply rail. Into a 20Ω load (the minimum tested load), the amplifier delivers more than ±450mA continuous and greater than ±1A peak output current.

The specifications described above, though familiar in the industry, consider voltage and current limits separately. In many applications, it is the voltage times current (or V-I product) that is more relevant to circuit operation. Refer to the *Output Voltage and Current Limitations* plot (Figure 4) in the Typical Characteristics. The X- and Y-axes of this graph show the zero-voltage output current limit and the zero-current output voltage limit, respectively. The four quadrants give a more detailed view of the OPA2670 output drive capabilities, noting that the graph is bounded by a safe operating area of 2W maximum internal power dissipation (in this case, for one channel only). Superimposing resistor load lines onto the plot shows that the OPA2670 can drive ±5.1V into 100Ω or ±5V into 50Ω without exceeding the output capabilities or the 1W dissipation limit. A 100Ω load line (the standard test circuit load) shows the full +12V output swing capability, as shown in the Electrical Characteristics table. The minimum specified output voltage and current over temperature are set by worst-case simulations at the cold temperature extreme. Only at cold startup do the output current and voltage decrease to the numbers shown in the Electrical Characteristics table. As the output transistors deliver power, the junction temperature increases, decreasing the V_{BE}s (increasing the available output voltage swing), and increasing the current gains (increasing the available output current). In steady-state operation, the available output voltage and current are always greater than that shown in the over-temperature specifications, because the output stage junction temperatures are higher than the minimum specified operating ambient temperature. To maintain maximum output stage linearity, no output short-circuit protection is provided. This absence of short-circuit protection is normally not a problem because most applications include a series-matching resistor at the output that limits the internal power dissipation if the output side of this resistor is shorted to ground. However, shorting the output pin directly to the adjacent positive power-supply pin, in most cases, destroys the amplifier. If additional short-circuit protection is required, a small series resistor may be included in the supply lines. Under heavy output loads, this additional resistor reduces the available output voltage swing. A 5Ω series resistor in each power-supply lead limits the internal power dissipation to less than 2W for an output short-circuit,

while decreasing the available output voltage swing only 0.5V for up to 100mA desired load currents. Always place the 0.1μF power-supply decoupling capacitors after these supply current limiting resistors, directly on the supply pins.

DRIVING CAPACITIVE LOADS

One of the most demanding and yet very common load conditions for an op amp is capacitive loading. Often, the capacitive load is the input of an ADC—including additional external capacitance that may be recommended to improve the ADC linearity. A high-speed, high open-loop gain amplifier such as the OPA2670 can be very susceptible to decreased stability and closed-loop response peaking when a capacitive load is placed directly on the output pin. When the amplifier open-loop output resistance is considered, this capacitive load introduces an additional pole in the signal path that can decrease the phase margin. Several external solutions to this problem have been suggested.

When the primary considerations are frequency response flatness, pulse response fidelity, and/or distortion, the simplest and most effective solution is to isolate the capacitive load from the feedback loop by inserting a series isolation resistor between the amplifier output and the capacitive load. This series resistor does not eliminate the pole from the loop response, but shifts it and adds a zero at a higher frequency. The additional zero acts to cancel the phase lag from the capacitive load pole, thus increasing the phase margin and improving stability. The Typical Characteristics show the recommended *R_S vs Capacitive Load* (see Figure 23 and Figure 24) and the resulting frequency response at the load. Parasitic capacitive loads greater than 2pF can begin to degrade device performance. Long printed circuit board (PCB) traces, unmatched cables, and connections to multiple devices can easily cause this value to be exceeded. Always consider this effect carefully, and add the recommended series resistor as close as possible to the OPA2670 output pin (see the Board Layout Guidelines section).

DISTORTION PERFORMANCE

The OPA2670 provides good distortion performance into a 100Ω load on +12V supplies. Relative to alternative solutions, the amplifier provides exceptional performance into lighter loads. Generally, until the fundamental signal reaches very high frequency or power levels, the second harmonic dominates the distortion with a negligible third-harmonic component. Focusing then on the second harmonic, increasing the load impedance improves distortion directly. Remember that the total load includes the feedback network—in the noninverting, fully-differential configuration (see Figure 38), this value is the sum of $2R_F + R_G$.

In most op amps, increasing the output voltage swing directly increases harmonic distortion. The Typical Characteristics show the second harmonic increasing at a little less than the expected 2x rate, whereas the third harmonic increases at a little less than the expected 3x rate. Where the test power doubles, the difference between it and the second harmonic decreases less than the expected 6dB, whereas the difference between it and the third harmonic decreases by less than the expected 12dB. This difference also shows up in the two-tone, third-order intermodulation spurious (IM3) response curves. The third-order spurious levels are extremely low at low-output power levels. The output stage continues to hold them low even as the fundamental power reaches very high levels.

DIFFERENTIAL NOISE PERFORMANCE

The OPA2670 is designed to be used as a differential driver in xDSL applications. Therefore, it is important to analyze the noise in such a configuration. Figure 44 shows the op amp noise model for the differential configuration.

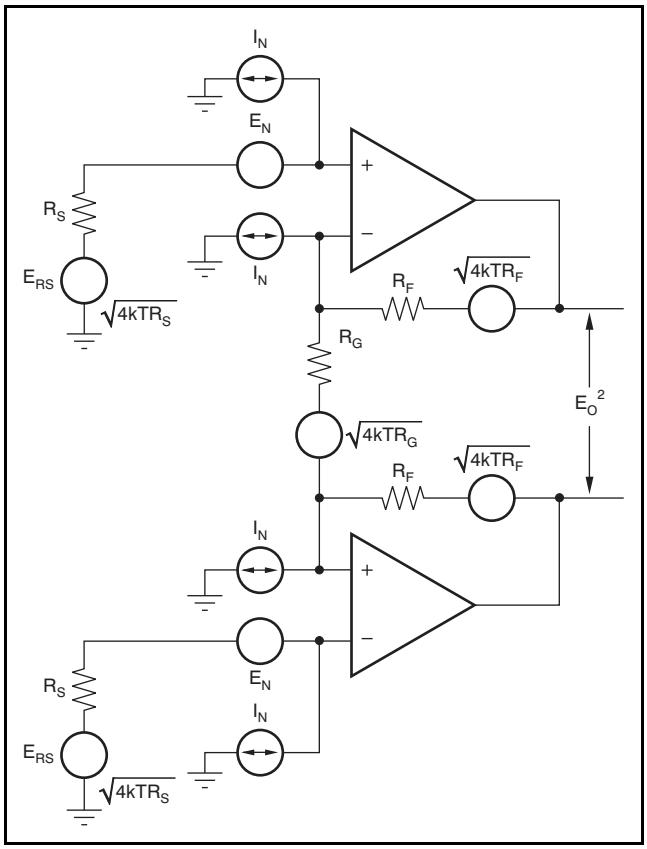


Figure 44. Differential Op Amp Noise Analysis Model

As a reminder, the differential gain is expressed as:

$$G_D = 1 + \frac{2 \times R_F}{R_G} \quad (15)$$

The output noise can be expressed as shown below:

$$E_O = \sqrt{2 \times G_D^2 \times \left[e_N^2 + (i_N \times R_S)^2 + 4kTR_S \right] + 2(i_I R_F)^2 + 2(4kTR_F G_D)} \quad (16)$$

Dividing this expression by the differential noise gain [$G_D = (1 + 2R_F/R_G)$] gives the equivalent input-referred spot noise voltage at the noninverting input, as shown in Equation 17.

$$E_O = \sqrt{2 \times \left[e_N^2 + (i_N \times R_S)^2 + 4kTR_S \right] + 2\left(\frac{i_I R_F}{G_D} \right)^2 + 2\left(\frac{4kTR_F}{G_D} \right)} \quad (17)$$

Evaluating these equations for the OPA2670 ADSL circuit and component values of Figure 39 gives a total output spot noise voltage of 66.7nV/$\sqrt{Hz}$ and a total equivalent input spot noise voltage of 6.67nV/$\sqrt{Hz}$

In order to minimize the output noise as a result of the noninverting input bias current noise, it is recommended to keep the noninverting source impedance as low as possible.

DC ACCURACY AND OFFSET CONTROL

A current-feedback op amp such as the OPA2670 provides exceptional bandwidth in high gains, giving fast pulse settling but only moderate dc accuracy. The Electrical Characteristics show an input offset voltage comparable to high-speed, voltage-feedback amplifiers; however, the two input bias currents are somewhat higher and are unmatched. While bias current cancellation techniques are very effective with most voltage-feedback op amps, they do not generally reduce the output dc offset for wideband current-feedback op amps. Because the two input bias currents are unrelated in both magnitude and polarity, matching the input source impedance to reduce error contribution to the output is ineffective. Evaluating the configuration of Figure 38, using a worst-case condition at +25°C input offset voltage and the two input bias currents, gives a worst-case output offset range equal to:

$V_{OFF} = \pm(NG \times V_{OS(MAX)}) + (I_{BN} \times R_S/2 \times NG) \pm(I_{BI} \times R_F)$

where NG = noninverting signal gain

$= \pm(10 \times 6mV) + (24\mu A \times 25\Omega \times 10) \pm(750\Omega \times 34\mu A)$

$= \pm 60mV \pm 6mV \pm 25.5mV$

$V_{OFF} = \pm 121.8mV$

BOARD LAYOUT GUIDELINES

Achieving optimum performance with a high-frequency amplifier such as the OPA2670 requires careful attention to board layout parasitic and external component types. Recommendations that optimize performance include:

a) Minimize parasitic capacitance to any ac ground for all of the signal I/O pins. Parasitic capacitance on the output and inverting input pins can cause instability; on the noninverting input, it can react with the source impedance to cause unintentional band limiting. To reduce unwanted capacitance, a window around the signal I/O pins should be opened in all of the ground and power planes around those pins. Otherwise, ground and power planes should be unbroken elsewhere on the board. .

b) Minimize the distance (less than 0.25in, or 6,35mm) from the power-supply pins to high-frequency 0.1μF decoupling capacitors. At the device pins, the ground and power plane layout should not be in close proximity to the signal I/O pins. Avoid narrow power and ground traces to minimize inductance between the pins and the decoupling capacitors. The power-supply connections should always be decoupled with these capacitors. An optional supply decoupling capacitor across the two power supplies (for bipolar operation) improves second-harmonic distortion performance. Larger (2.2μF to 6.8μF) decoupling capacitors, effective at lower frequencies, should also be used on the main supply pins. These capacitors can be placed somewhat farther from the device and may be shared among several devices in the same area of the PCB.

c) Careful selection and placement of external components preserve the high-frequency performance of the OPA2670. Resistors should be a very low reactance type. Surface-mount resistors work best and allow a tighter overall layout. Metal film and carbon composition, axially-leaded resistors can also provide good high-frequency performance.

Again, keep leads and PCB trace length as short as possible. Never use wire-wound type resistors in a high-frequency application. Although the output pin and inverting input pin are the most sensitive to parasitic capacitance, always position the feedback and series output resistor, if any, as close as possible to the output pin. Other network components, such as noninverting input termination resistors, should also be placed close to the package. Where double-side component mounting is allowed, place the feedback resistor directly under the package on the other side of the board between the output and inverting input pins. The frequency response is primarily determined by the feedback resistor value as described previously. Increasing the value reduces the bandwidth, whereas decreasing it leads to a more peaked frequency response. The 750Ω feedback resistor used in the Typical Characteristics at a gain of +10V/V on +12V supplies is a good starting point for design.

d) Connections to other wideband devices on the board may be made with short direct traces or through onboard transmission lines. For short connections, consider the trace and the input to the next device as a lumped capacitive load. Relatively wide traces (50mils to 100mils [.050in to .100in, or 1,27mm to 2,54mm]) should be used, preferably with ground and power planes opened up around them. Estimate the total capacitive load and set R_S from the plot of *R_S vs Capacitive Load* (see Figure 23 and Figure 24). Low parasitic capacitive loads (less than 5pF) may not need an isolation resistor because the OPA2670 is nominally compensated to operate with a 2pF parasitic load. If a long trace is required, and the 6dB signal loss intrinsic to a doubly-terminated transmission line is acceptable, implement a matched-impedance transmission line using microstrip or stripline techniques (consult an ECL design handbook for microstrip and stripline layout techniques). A 50Ω environment is not necessary on board; in fact, a higher impedance environment improves distortion (see the distortion versus load plots). With a characteristic board trace impedance defined based on board material and trace dimensions, a matching series resistor into the trace from the output of the OPA2670 is used, as well as a terminating shunt resistor at the input of the destination device. Remember also that the terminating impedance is the parallel combination of the shunt resistor and the input impedance of the destination device.

This total effective impedance should be set to match the trace impedance. The high output voltage and current capability of the OPA2670 allows multiple destination devices to be handled as separate transmission lines, each with their own series and shunt terminations. If the 6dB attenuation of a doubly-terminated transmission line is unacceptable, a long trace can be series-terminated at the source end only.

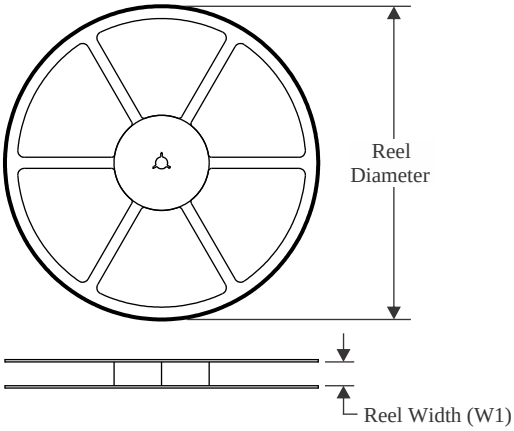
Treat the trace as a capacitive load in this case and set the series resistor value as shown in the plot of *R_S vs Capacitive Load*. However, this configuration does not preserve signal integrity as well as a doubly-terminated line. If the input impedance of the destination device is low, there is some signal attenuation as a result of the voltage divider formed by the series output into the terminating impedance.

e) Socketing a high-speed part such as the OPA2670 is not recommended. The additional lead length and pin-to-pin capacitance introduced by the socket can create an extremely troublesome parasitic network, which can make it almost impossible to achieve a smooth, stable frequency response. Best results are obtained by soldering the OPA2670 directly onto the board.

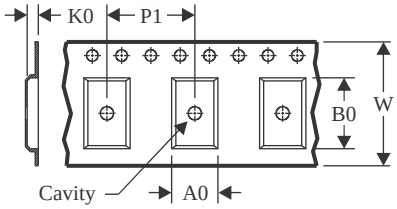
f) Use the $-V_S$ plane to conduct heat out of the QFN-16 PowerPAD package. This package attaches the die directly to an exposed thermal pad on the bottom, which should be soldered to the board. This pad must be connected electrically to the same voltage plane as the most negative supply applied to the OPA2670 (in Figure 39, this supply is GND).

TAPE AND REEL INFORMATION

REEL DIMENSIONS

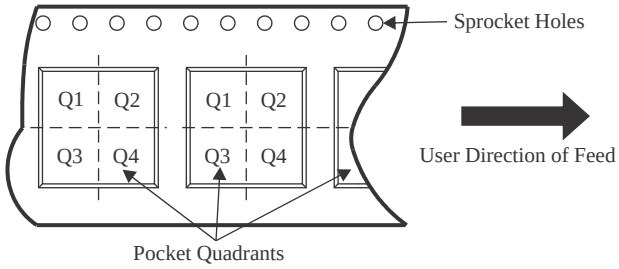


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

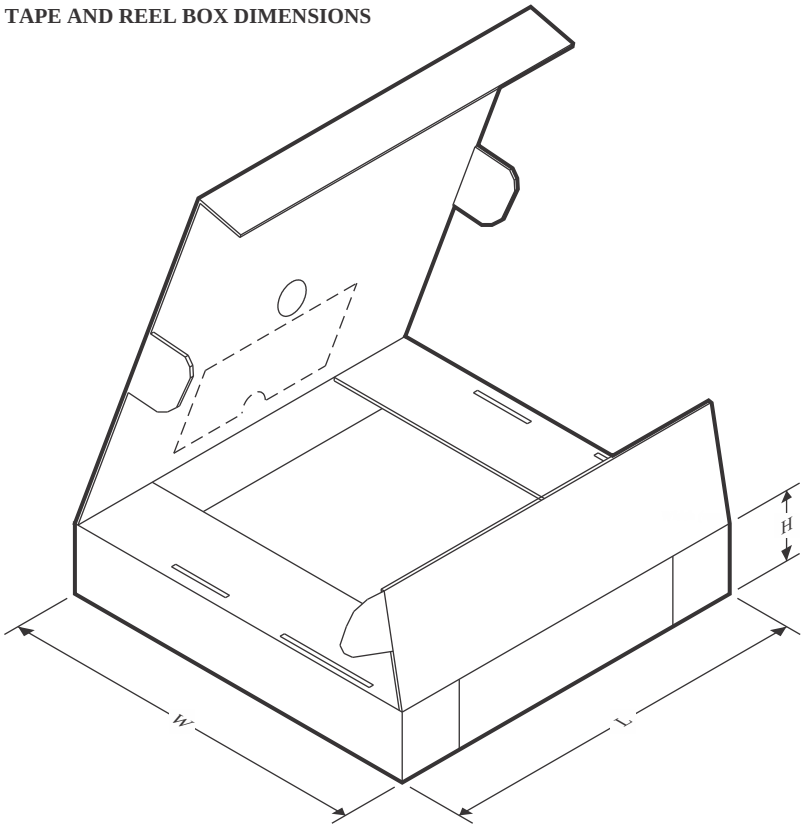
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
OPA2670IRGVR	VQFN	RGV	16	2500	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
OPA2670IRGVT	VQFN	RGV	16	250	180.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
OPA2670IRGVR	VQFN	RGV	16	2500	356.0	356.0	35.0
OPA2670IRGVT	VQFN	RGV	16	250	210.0	185.0	35.0

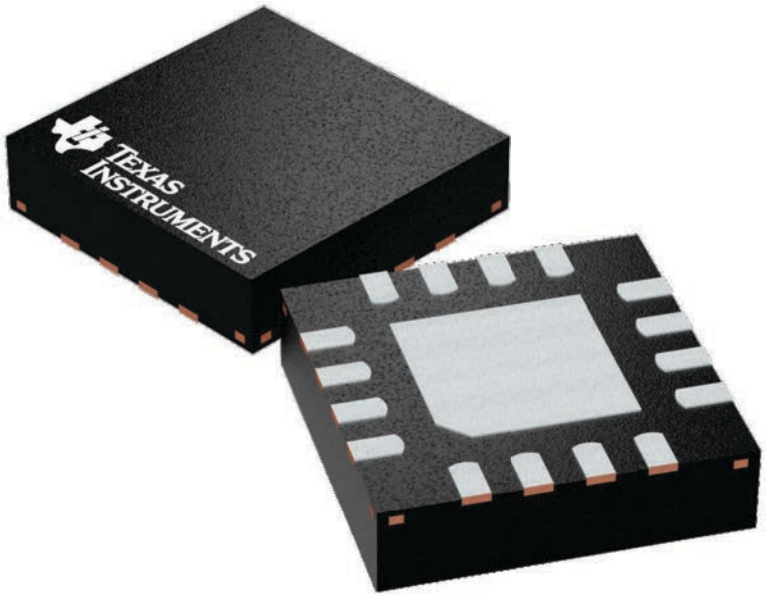
GENERIC PACKAGE VIEW

RGV 16

VQFN - 1 mm max height

4 x 4, 0.65 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

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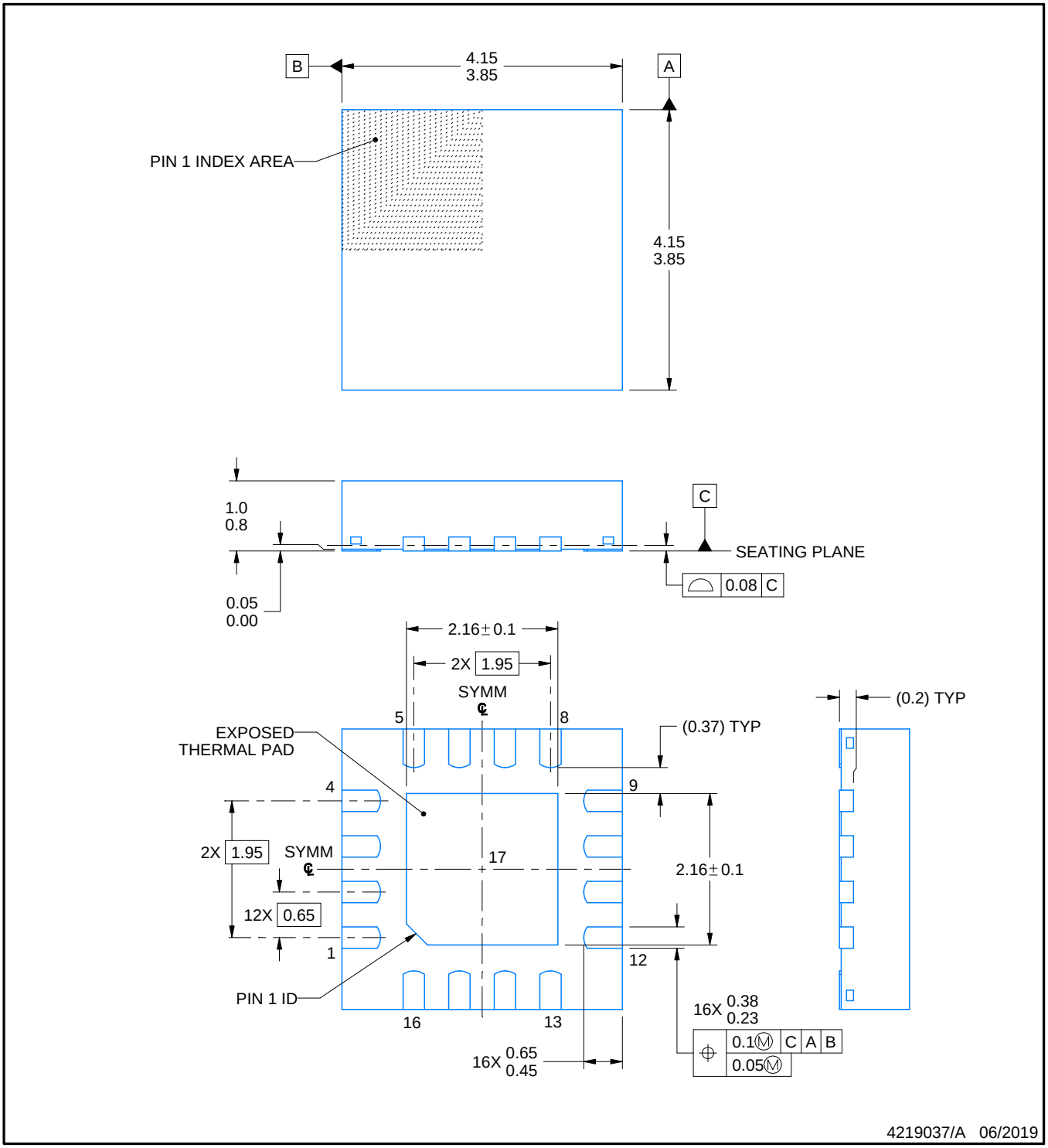
RGV0016A

PACKAGE OUTLINE

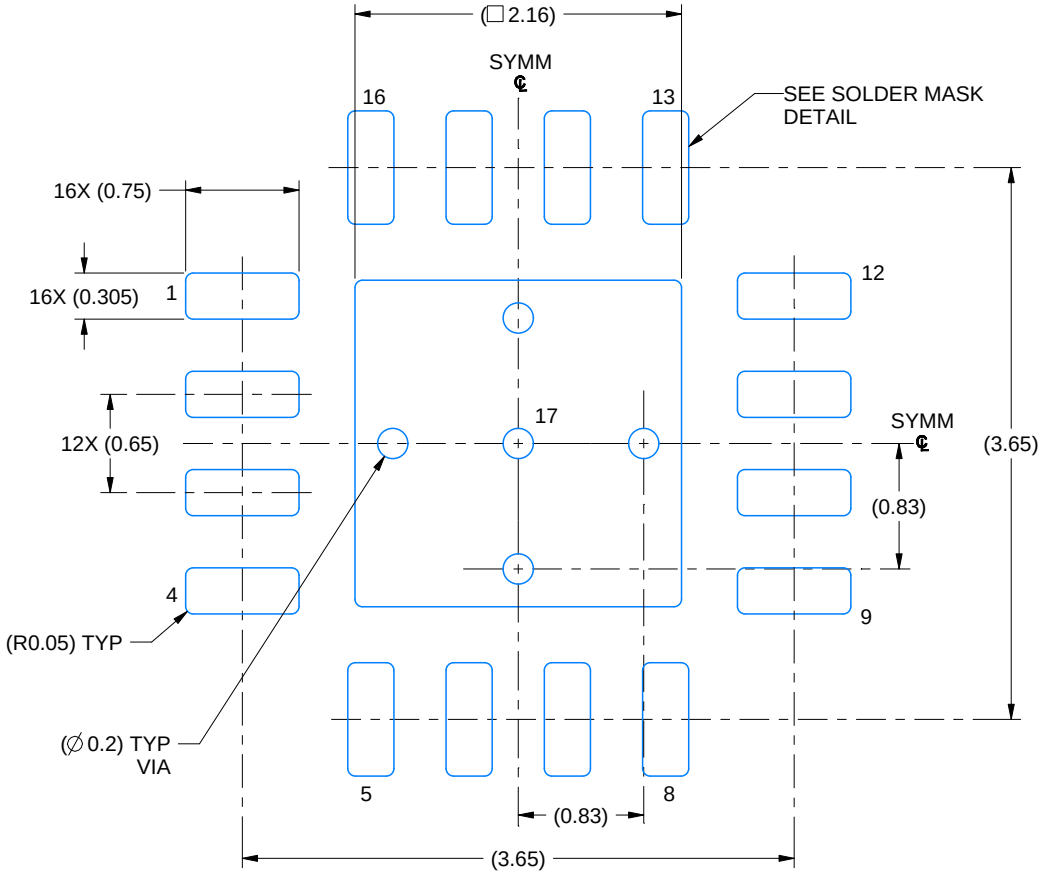
VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

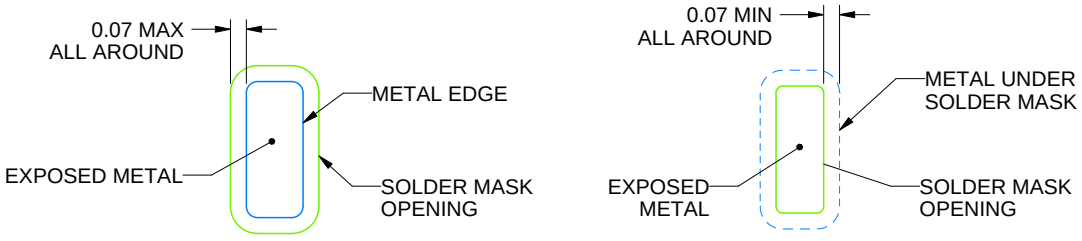


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 20X



NON SOLDER MASK DEFINED (PREFERRED)

SOLDER MASK DEFINED

SOLDER MASK DETAILS

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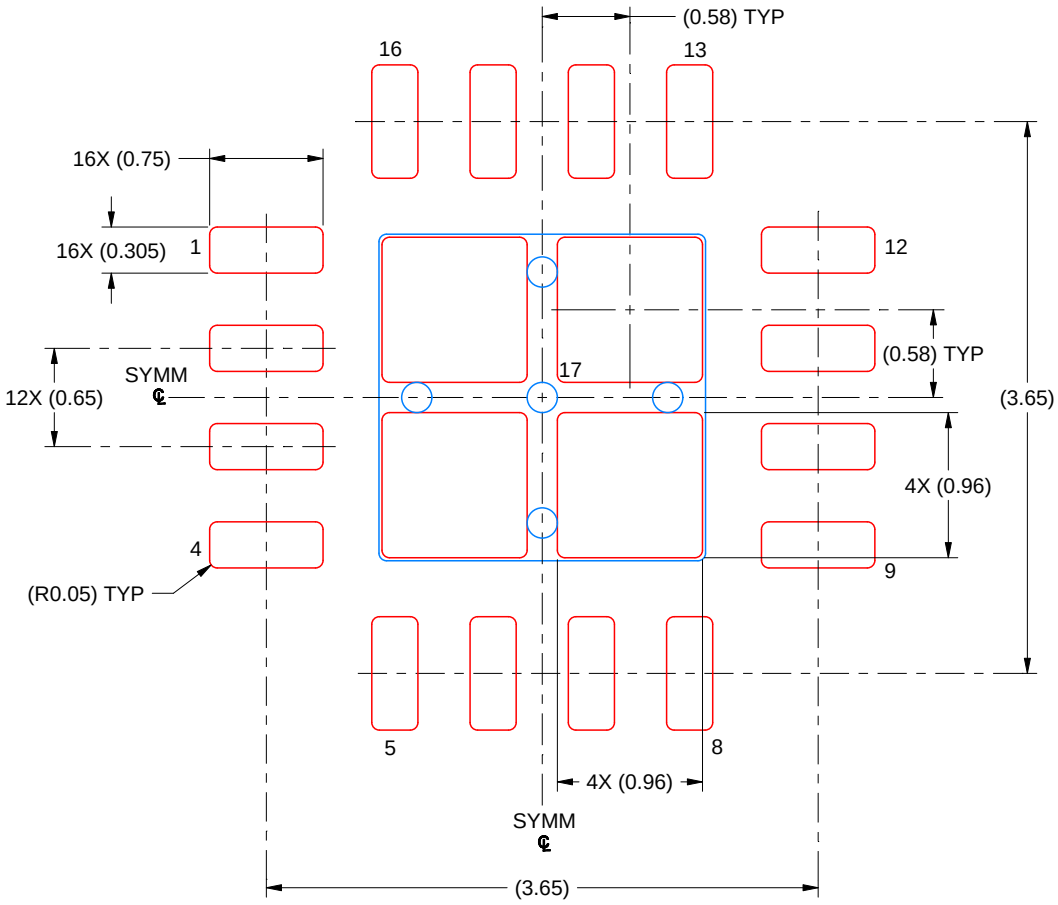
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 MM THICK STENCIL
SCALE: 20X

EXPOSED PAD 17
79% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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