

单电源、10MHz、轨至轨输出、 低噪声、JFET 放大器

 查询样品: [OPA141](#), [OPA2141](#), [OPA4141](#)

特性

- 低电源电流: **2.3mA** (最大值)
- 低失调漂移: **10 μ V/°C** (最大值)
- 低输入偏置电流: **20pA** (最大值)
- 超低1/f噪声: **250nV_{pp}**
- 低噪声: **6.5nV/ $\sqrt{\text{Hz}}$**
- 宽带宽: **10MHz**
- 转换速率: **20 V/ μ s**
- 输入电压范围包括V_—
- 轨至轨输出
- 单电源操作: **4.5V至36V**
- 双电源操作: **$\pm 2.25\text{V}$ 至 $\pm 18\text{V}$**
- 无相位反转
- **MSOP-8、TSSOP** 封装

应用

- 电池供电型仪器
- 工业控制
- 医疗仪表
- 光电二极管放大器
- 有源滤波器
- 数据采集系统
- 便携式音频
- 自动测试系统

说明

OPA141、OPA2141 和 OPA4141放大器系列为低功耗 JFET输入放大器, 具有优良的漂移特性和低输入偏置电流。轨至轨输出摆幅与包括了V_—的输入范围使得设计人员不仅能够充分利用 JFET 放大器的低噪声特性, 同时还能实现与新式的单电源、高精度模数转换器 (ADC) 和数模转换器 (DAC) 的连接。

OPA141 实现了10MHz 的单位增益带宽和 20 V/ μ s 的转换速率, 而仅消耗 1.8mA (典型值) 的静态电流。该器件采用 4.5V 至 36V 的单工作电源或 $\pm 2.25\text{V}$ 至 $\pm 18\text{V}$ 的双工作电源。

所有版本的技术规格均针对 -40°C 至 $+125^{\circ}\text{C}$ 的温度范围而拟订, 以便在最严苛的环境中使用。

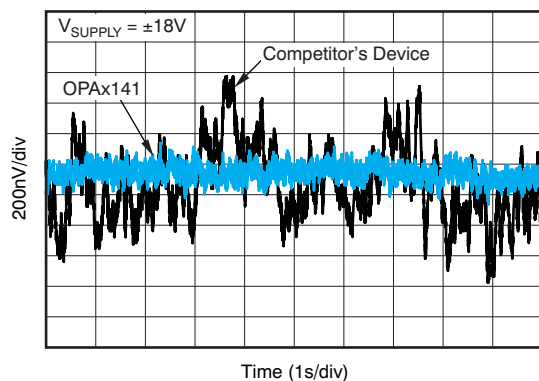
OPA141 (单通道器件) 和 OPA2141 (双通道器件) 版本采用MSOP-8 和 SO-8 封装; OPA4141 (四通道器件) 则采用 SO-14 和 TSSOP-14 封装。

相关产品

特性	产品
高精度、低功耗、10MHz FET输入工业运算放大器	OPA140⁽¹⁾
采用SOT-23封装的2.2nV/ $\sqrt{\text{Hz}}$ 、低功耗、36V运算放大器	OPA209⁽¹⁾
低噪声、高精度、JFET 输入运算放大器	OPA827
低噪声、低I _Q 、高精度运算放大器	OPA376
高速、FET 输入运算放大器	OPA132

1. 前瞻性产品, 预计于2010年第三季度供货。

图 1. 0.1Hz至10Hz噪声



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

All trademarks are the property of their respective owners.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of the Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

Over operating free-air temperature range (unless otherwise noted).

		VALUE	UNIT
Supply Voltage		±20	V
Signal Input Terminals	Voltage ⁽²⁾	(V–) –0.5 to (V+) +0.5	V
	Current ⁽²⁾	±10	mA
Output Short-Circuit ⁽³⁾		Continuous	
Operating Temperature, T _A		–55 to +150	°C
Storage Temperature, T _A		–65 to +150	°C
Junction Temperature, T _J		+150	°C
ESD Ratings	Human Body Model (HBM)	2000	V
	Charged Device Model (CDM)	500	V

- (1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not supported.
- (2) Input terminals are diode-clamped to the power-supply rails. Input signals that can swing more than 0.5V beyond the supply rails should be current limited to 10 mA or less.
- (3) Short-circuit to V_S/2 (ground in symmetrical dual-supply setups), one amplifier per package.

PACKAGE INFORMATION⁽¹⁾

PRODUCT	PACKAGE-LEAD	PACKAGE DESIGNATOR	PACKAGE MARKING
OPA141	SO-8	D	O141A
	MSOP-8	DGK	141
OPA2141	SO-8	D	O2141A
	MSOP-8	DGK	2141
OPA4141	TSSOP-14	PW	O4141A
	SO-14	D	O4141AG4

- (1) For the most current package and ordering information see the Package Option Addendum at the end of this document, or visit the device product folder at www.ti.com.

THERMAL INFORMATION

THERMAL METRIC		OPA141, OPA2141	OPA141, OPA2141	UNITS
		D (SO)	DGK (MSOP) ⁽¹⁾	
		8	8	
θ_{JA}	Junction-to-ambient thermal resistance ⁽²⁾	160	180	°C/W
$\theta_{JC(top)}$	Junction-to-case(top) thermal resistance ⁽³⁾	75	55	
θ_{JB}	Junction-to-board thermal resistance ⁽⁴⁾	60	130	
ψ_{JT}	Junction-to-top characterization parameter ⁽⁵⁾	9	n/a	
ψ_{JB}	Junction-to-board characterization parameter ⁽⁶⁾	50	120	
$\theta_{JC(bottom)}$	Junction-to-case(bottom) thermal resistance ⁽⁷⁾	n/a	n/a	

- (1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, [SPRA953](#).
- (2) The junction-to-ambient thermal resistance under natural convection is obtained in a simulation on a JEDEC-standard, high-K board, as specified in JESD51-7, in an environment described in JESD51-2a.
- (3) The junction-to-case (top) thermal resistance is obtained by simulating a cold plate test on the package top. No specific JEDEC-standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.
- (4) The junction-to-board thermal resistance is obtained by simulating in an environment with a ring cold plate fixture to control the PCB temperature, as described in JESD51-8.
- (5) The junction-to-top characterization parameter, ψ_{JT} , estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining θ_{JA} , using a procedure described in JESD51-2a (sections 6 and 7).
- (6) The junction-to-board characterization parameter, ψ_{JB} , estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining θ_{JA} , using a procedure described in JESD51-2a (sections 6 and 7).
- (7) The junction-to-case (bottom) thermal resistance is obtained by simulating a cold plate test on the exposed (power) pad. No specific JEDEC standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.

THERMAL INFORMATION

THERMAL METRIC		OPA4141	OPA4141	UNITS
		D (SO)	PW (TSSOP) ⁽¹⁾	
		14	14	
θ_{JA}	Junction-to-ambient thermal resistance ⁽²⁾	97	135	°C/W
$\theta_{JC(top)}$	Junction-to-case(top) thermal resistance ⁽³⁾	56	45	
θ_{JB}	Junction-to-board thermal resistance ⁽⁴⁾	53	66	
ψ_{JT}	Junction-to-top characterization parameter ⁽⁵⁾	19	n/a	
ψ_{JB}	Junction-to-board characterization parameter ⁽⁶⁾	46	60	
$\theta_{JC(bottom)}$	Junction-to-case(bottom) thermal resistance ⁽⁷⁾	n/a	n/a	

- (1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, [SPRA953](#).
- (2) The junction-to-ambient thermal resistance under natural convection is obtained in a simulation on a JEDEC-standard, high-K board, as specified in JESD51-7, in an environment described in JESD51-2a.
- (3) The junction-to-case (top) thermal resistance is obtained by simulating a cold plate test on the package top. No specific JEDEC-standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.
- (4) The junction-to-board thermal resistance is obtained by simulating in an environment with a ring cold plate fixture to control the PCB temperature, as described in JESD51-8.
- (5) The junction-to-top characterization parameter, ψ_{JT} , estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining θ_{JA} , using a procedure described in JESD51-2a (sections 6 and 7).
- (6) The junction-to-board characterization parameter, ψ_{JB} , estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining θ_{JA} , using a procedure described in JESD51-2a (sections 6 and 7).
- (7) The junction-to-case (bottom) thermal resistance is obtained by simulating a cold plate test on the exposed (power) pad. No specific JEDEC standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.

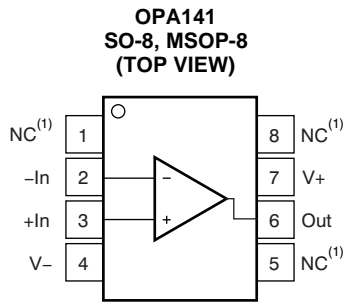
ELECTRICAL CHARACTERISTICS: $V_S = +4.5V$ to $+36V$; $\pm 2.25V$ to $\pm 18V$ (continued)

Boldface limits apply over the specified temperature range, $T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$.

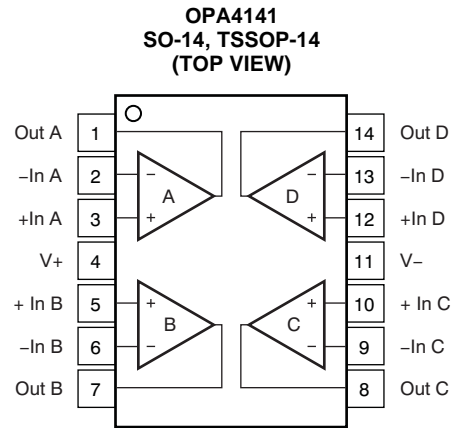
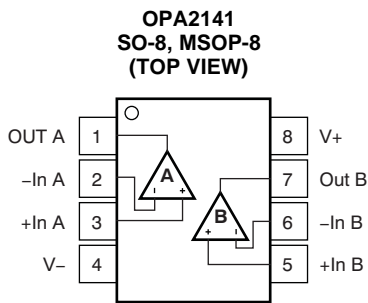
At $T_A = +25^\circ\text{C}$, $R_L = 2k\Omega$ connected to midsupply, $V_{CM} = V_{OUT} = \text{midsupply}$, unless otherwise noted.

PARAMETER	CONDITIONS	OPA141, OPA2141, OPA4141			UNIT
		MIN	TYP	MAX	
OUTPUT					
Voltage Output V_O	$R_L = 10k\Omega$	$(V^-)+0.2$		$(V^+)-0.2$	V
	$R_L = 2k\Omega$	$(V^-)+0.35$		$(V^+)-0.35$	V
Short-Circuit Current I_{SC}	Source		+36		mA
	Sink		-30		mA
Capacitive Load Drive C_{LOAD}		See Figure 20 and Figure 21			
Open-Loop Output Impedance R_O	$f = 1\text{MHz}$, $I_O = 0$ (See Figure 19)		10		Ω
POWER SUPPLY					
Specified Voltage Range V_S		± 2.25		± 18	V
Quiescent Current (per amplifier) I_Q	$I_O = 0\text{mA}$		1.8	2.3	mA
		Over Temperature		3.1	mA
CHANNEL SEPARATION					
Channel Separation	At dc		0.02		$\mu\text{V/V}$
	At 100kHz		10		$\mu\text{V/V}$
TEMPERATURE RANGE					
Specified Range		-40		+125	$^\circ\text{C}$
Operating Range		-55		+150	$^\circ\text{C}$

PIN ASSIGNMENTS



(1) NC denotes no internal connection.



SIMPLIFIED BLOCK DIAGRAM

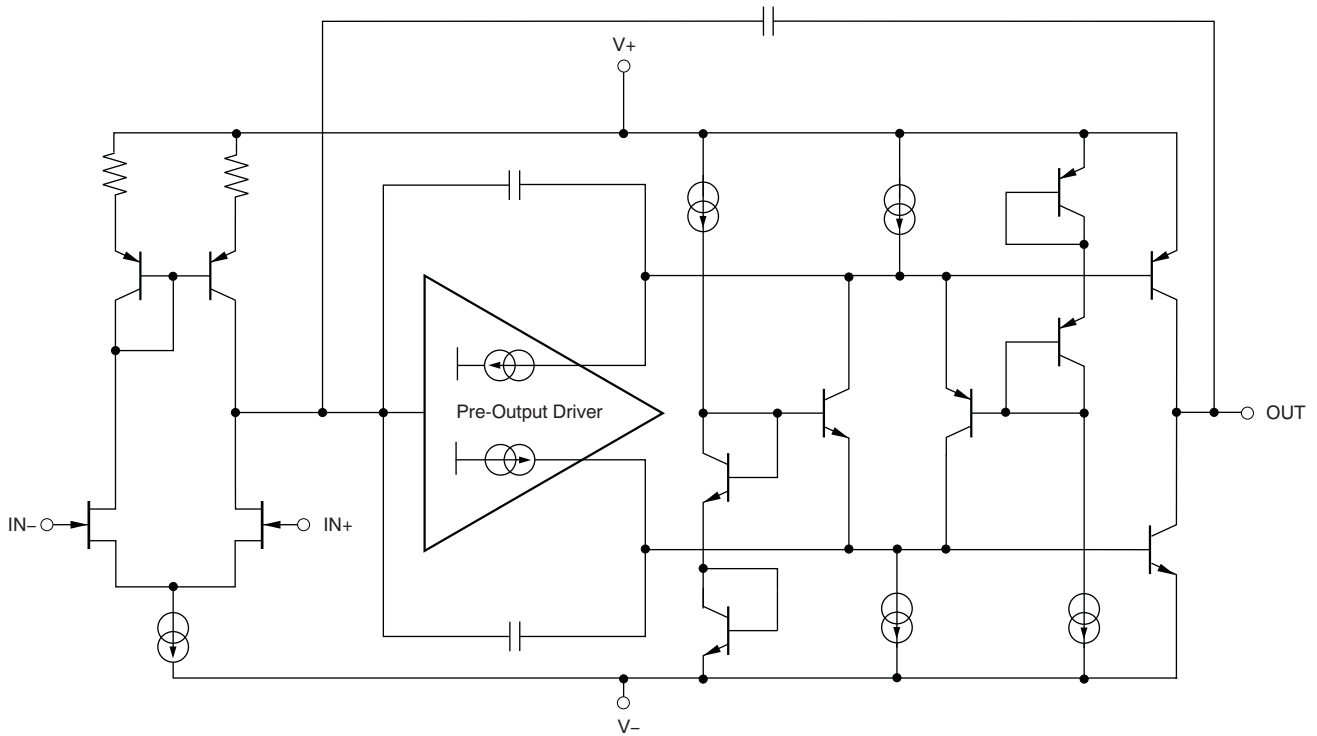


Figure 2.

TYPICAL CHARACTERISTICS SUMMARY

TABLE OF GRAPHS

Table 1. Characteristic Performance Measurements

DESCRIPTION	FIGURE
Offset Voltage Production Distribution	Figure 3
Offset Voltage Drift Distribution	Figure 4
Offset Voltage vs Common-Mode Voltage (Max Supply)	Figure 5
I_B and I_{OS} vs Common-Mode Voltage	Figure 6
Output Voltage Swing vs Output Current	Figure 7
CMRR and PSRR vs Frequency (RTI)	Figure 8
Common-Mode Rejection Ratio vs Temperature	Figure 9
0.1Hz to 10Hz Noise	Figure 10
Input Voltage Noise Density vs Frequency	Figure 11
THD+N Ratio vs Frequency (80kHz AP Bandwidth)	Figure 12
THD+N Ratio vs Output Amplitude	Figure 13
Quiescent Current vs Temperature	Figure 14
Quiescent Current vs Supply Voltage	Figure 15
Gain and Phase vs Frequency	Figure 16
Closed-Loop Gain vs Frequency	Figure 17
Open-Loop Gain vs Temperature	Figure 18
Open-Loop Output Impedance vs Frequency	Figure 19
Small-Signal Overshoot vs Capacitive Load ($G = +1$)	Figure 20
Small-Signal Overshoot vs Capacitive Load ($G = -1$)	Figure 21
No Phase Reversal	Figure 22
Positive Overload Recovery	Figure 23
Negative Overload Recovery	Figure 24
Small-Signal Step Response ($G = +1$)	Figure 25
Small-Signal Step Response ($G = -1$)	Figure 26
Large-Signal Step Response ($G = +1$)	Figure 27
Large-Signal Step Response ($G = -1$)	Figure 28
Short-Circuit Current vs Temperature	Figure 29
Maximum Output Voltage vs Frequency	Figure 30
Channel Separation vs Frequency	Figure 31

TYPICAL CHARACTERISTICS

At $T_A = +25^\circ\text{C}$, $V_S = \pm 18\text{V}$, $R_L = 2\text{k}\Omega$ connected to midsupply, $V_{CM} = V_{OUT} = \text{midsupply}$, unless otherwise noted.

OFFSET VOLTAGE PRODUCTION DISTRIBUTION

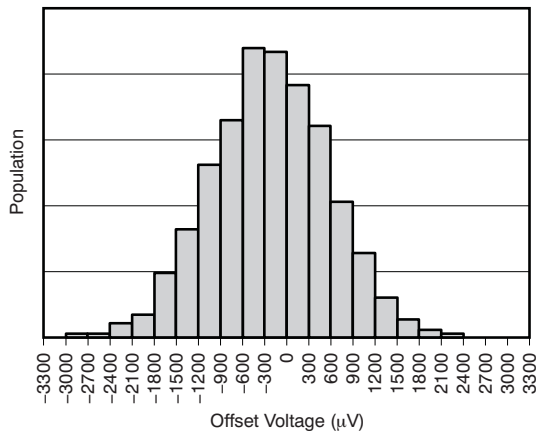


Figure 3.

OFFSET VOLTAGE DRIFT DISTRIBUTION

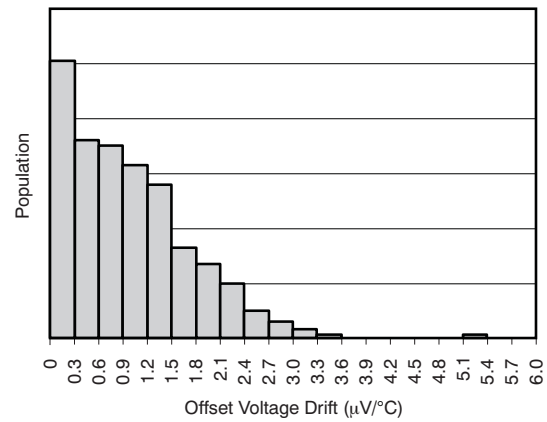


Figure 4.

OFFSET VOLTAGE vs COMMON-MODE VOLTAGE

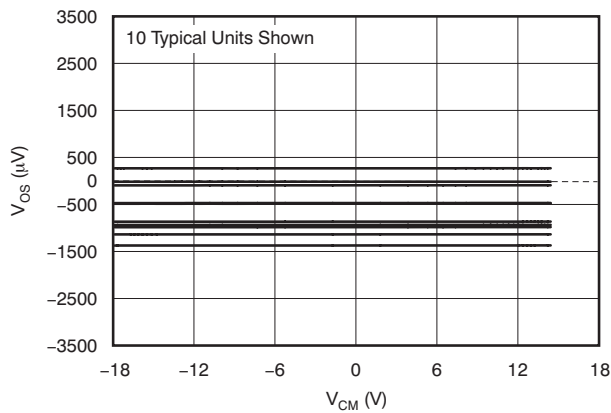


Figure 5.

I_B AND I_{OS} vs COMMON-MODE VOLTAGE

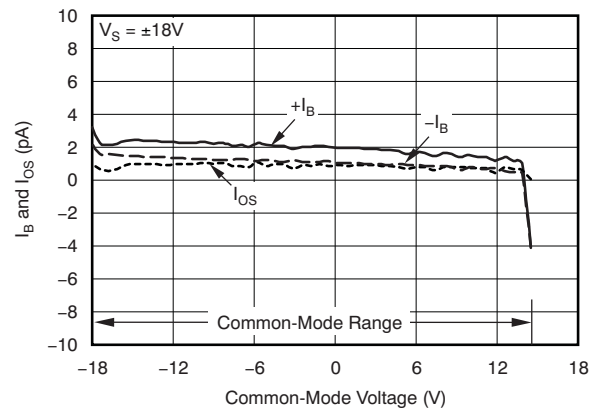


Figure 6.

OUTPUT VOLTAGE SWING vs OUTPUT CURRENT (MAX SUPPLY)

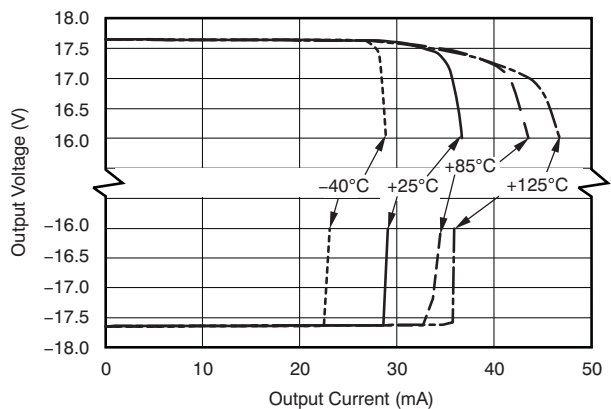


Figure 7.

CMRR AND PSRR vs FREQUENCY (Referred to Input)

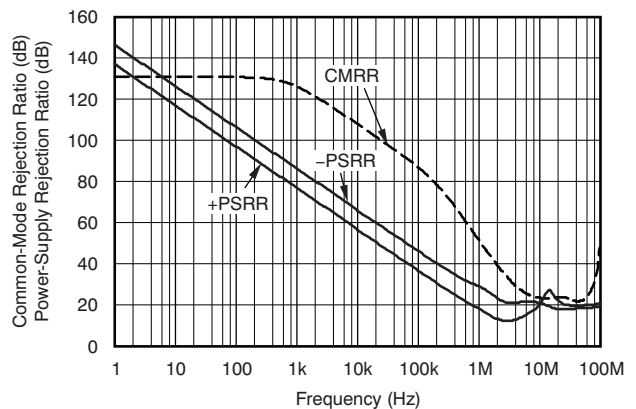


Figure 8.

TYPICAL CHARACTERISTICS (continued)

At $T_A = +25^\circ\text{C}$, $V_S = \pm 18\text{V}$, $R_L = 2\text{k}\Omega$ connected to midsupply, $V_{CM} = V_{OUT} = \text{midsupply}$, unless otherwise noted.

COMMON-MODE REJECTION RATIO vs TEMPERATURE

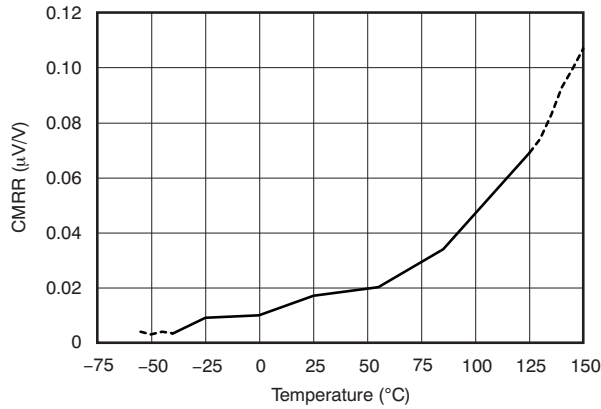


Figure 9.

0.1Hz to 10Hz NOISE

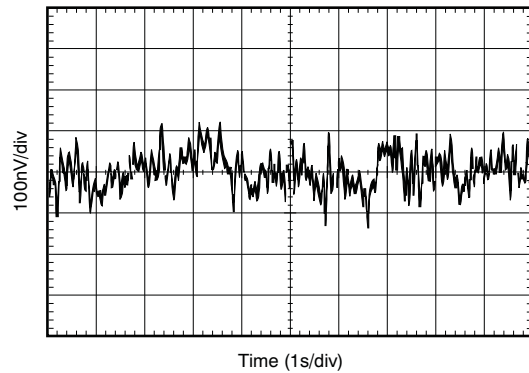


Figure 10.

INPUT VOLTAGE NOISE DENSITY vs FREQUENCY

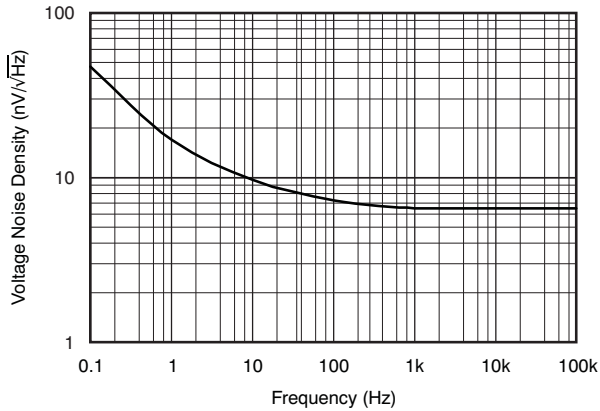


Figure 11.

THD+N RATIO vs FREQUENCY

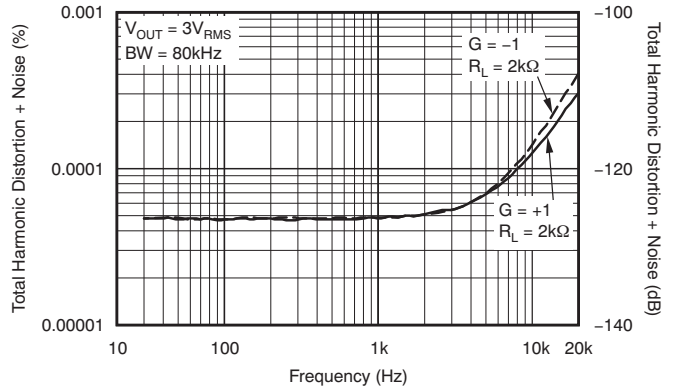


Figure 12.

THD+N RATIO vs OUTPUT AMPLITUDE

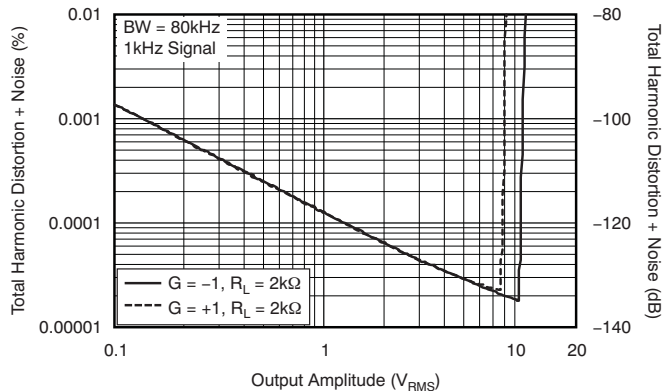


Figure 13.

QUIESCENT CURRENT vs TEMPERATURE

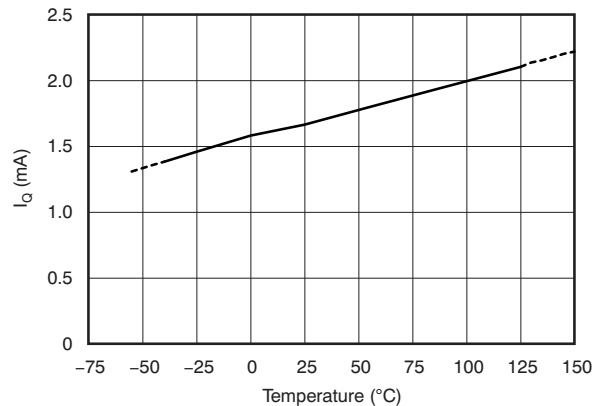


Figure 14.

TYPICAL CHARACTERISTICS (continued)

At $T_A = +25^\circ\text{C}$, $V_S = \pm 18\text{V}$, $R_L = 2\text{k}\Omega$ connected to midsupply, $V_{CM} = V_{OUT} = \text{midsupply}$, unless otherwise noted.

QUIESCENT CURRENT vs SUPPLY VOLTAGE

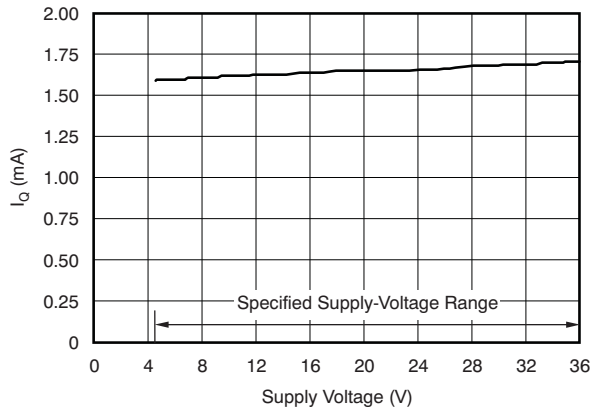


Figure 15.

GAIN AND PHASE vs FREQUENCY

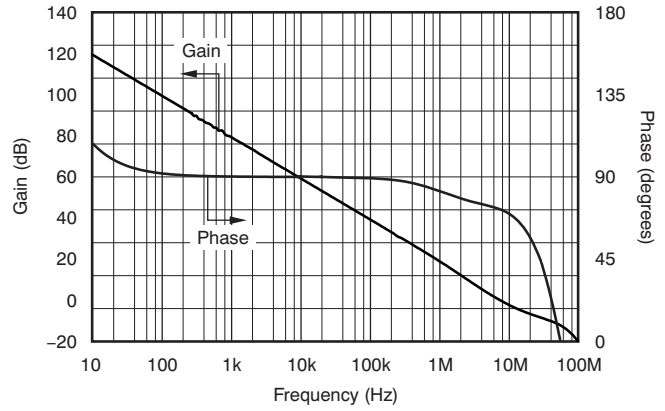


Figure 16.

CLOSED-LOOP GAIN vs FREQUENCY

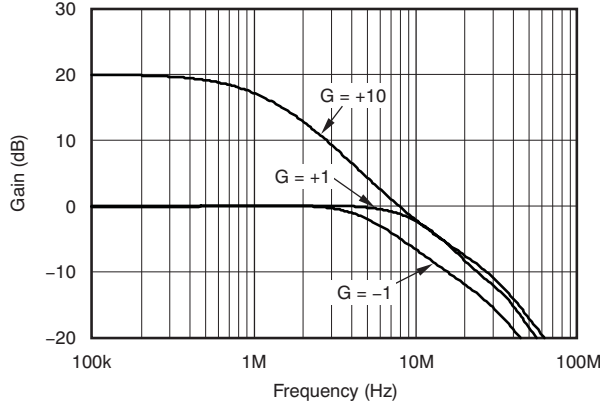


Figure 17.

OPEN-LOOP GAIN vs TEMPERATURE

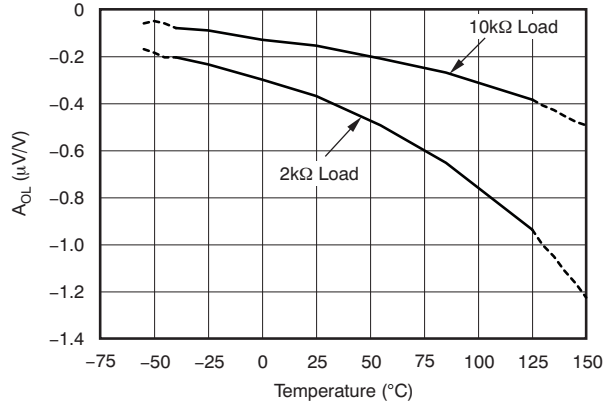


Figure 18.

OPEN-LOOP OUTPUT IMPEDANCE vs FREQUENCY

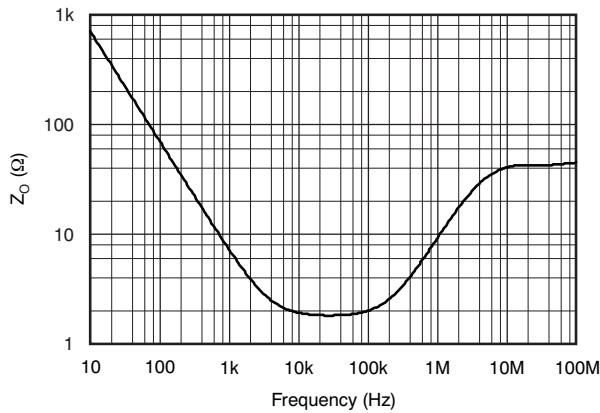


Figure 19.

SMALL-SIGNAL OVERSHOOT vs CAPACITIVE LOAD (100mV Output Step)

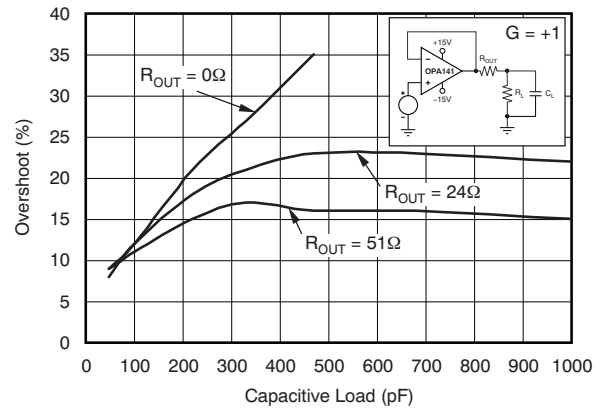


Figure 20.

TYPICAL CHARACTERISTICS (continued)

At $T_A = +25^\circ\text{C}$, $V_S = \pm 18\text{V}$, $R_L = 2\text{k}\Omega$ connected to midsupply, $V_{CM} = V_{OUT} = \text{midsupply}$, unless otherwise noted.

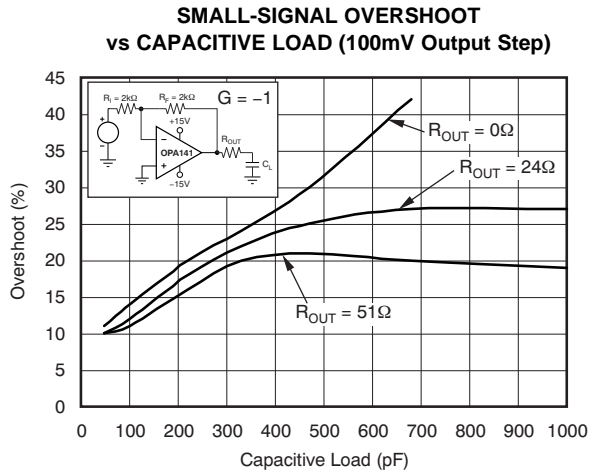


Figure 21.

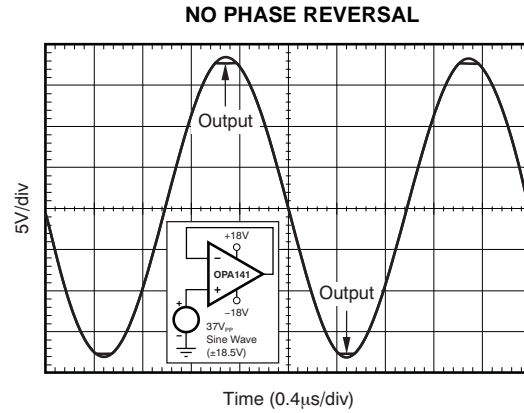


Figure 22.

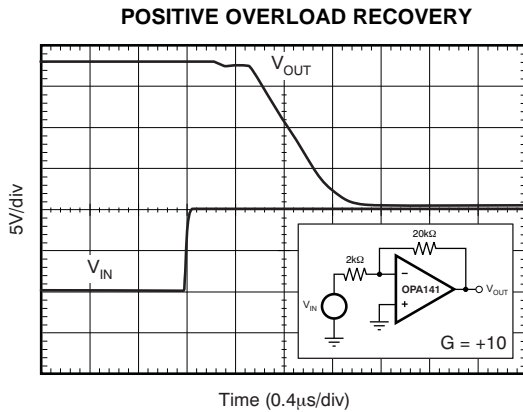


Figure 23.

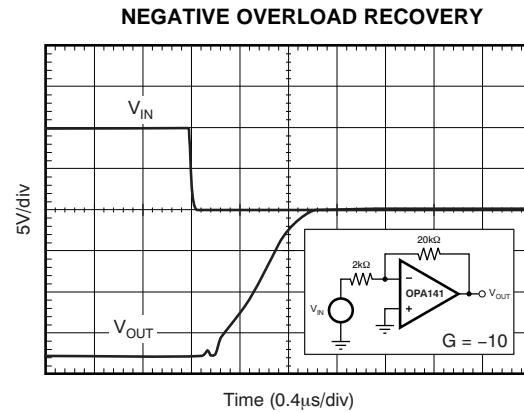


Figure 24.

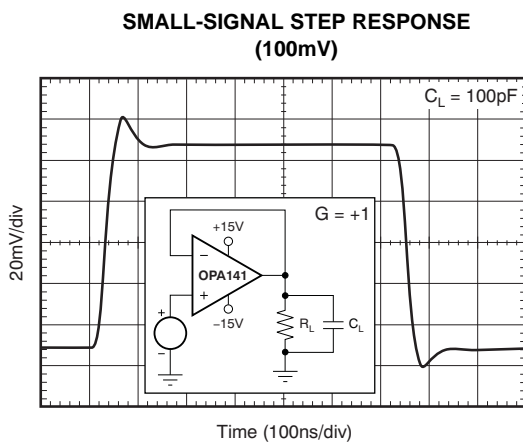


Figure 25.

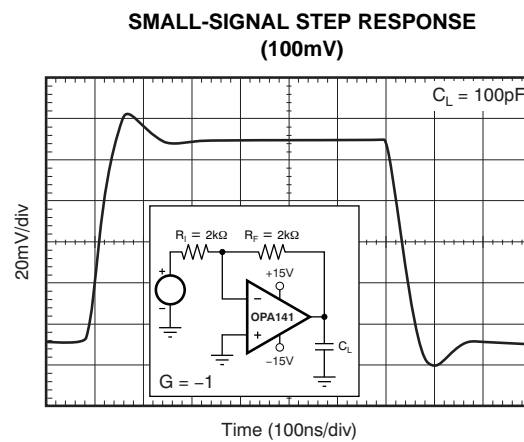


Figure 26.

TYPICAL CHARACTERISTICS (continued)

At $T_A = +25^\circ\text{C}$, $V_S = \pm 18\text{V}$, $R_L = 2\text{k}\Omega$ connected to midsupply, $V_{CM} = V_{OUT} = \text{midsupply}$, unless otherwise noted.

LARGE-SIGNAL STEP RESPONSE

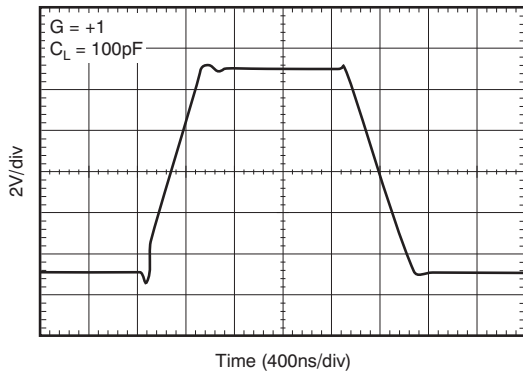


Figure 27.

LARGE-SIGNAL STEP RESPONSE

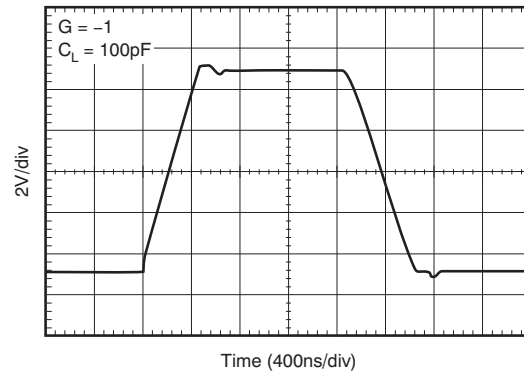


Figure 28.

SHORT-CIRCUIT CURRENT vs TEMPERATURE

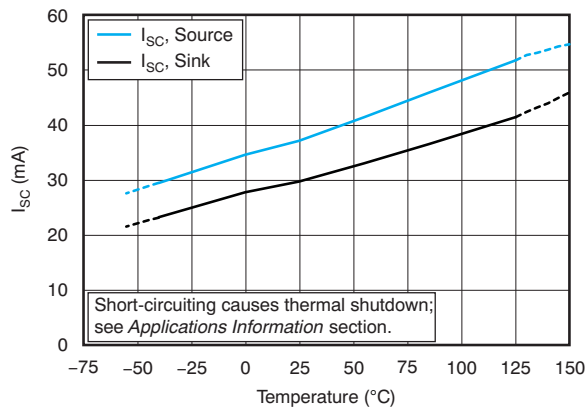


Figure 29.

MAXIMUM OUTPUT VOLTAGE vs FREQUENCY

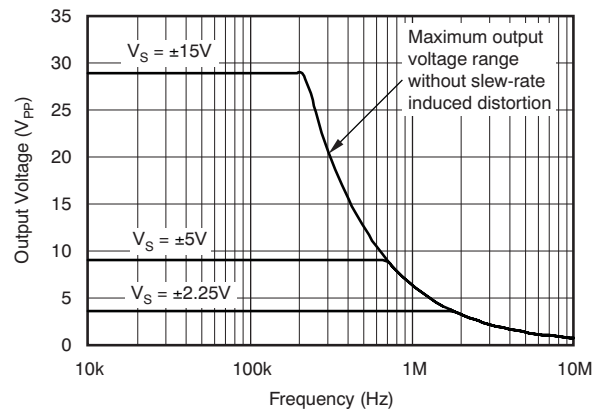


Figure 30.

CHANNEL SEPARATION vs FREQUENCY

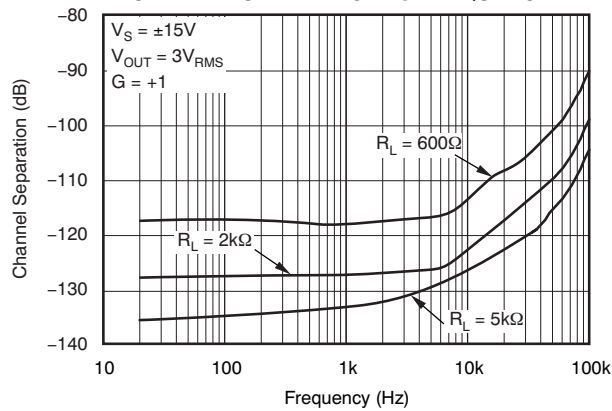


Figure 31.

APPLICATION INFORMATION

The OPA141, OPA2141, and OPA4141 are unity-gain stable, operational amplifiers with very low noise, input bias current, and input offset voltage. Applications with noisy or high-impedance power supplies require decoupling capacitors placed close to the device pins. In most cases, 0.1µF capacitors are adequate. Figure 2 shows a simplified schematic of the OPA141.

OPERATING VOLTAGE

The OPA141, OPA2141, and OPA4141 series of op amps can be used with single or dual supplies from an operating range of $V_S = +4.5V (\pm 2.25V)$ and up to $V_S = +36V (\pm 18V)$. These devices do not require symmetrical supplies; they only require a minimum supply voltage of +4.5V ($\pm 2.25V$). For V_S less than $\pm 3.5V$, the common-mode input range does not include midsupply. Supply voltages higher than +40V can permanently damage the device; see the [Absolute Maximum Ratings](#) table. Key parameters are specified over the operating temperature range, $T_A = -40^\circ C$ to $+125^\circ C$. Key parameters that vary over the supply voltage or temperature range are shown in the [Typical Characteristics](#) section of this data sheet.

CAPACITIVE LOAD AND STABILITY

The dynamic characteristics of the OPAx141 have been optimized for commonly encountered gains, loads, and operating conditions. The combination of low closed-loop gain and high capacitive loads decreases the phase margin of the amplifier and can lead to gain peaking or oscillations. As a result, heavier capacitive loads must be isolated from the output. The simplest way to achieve this isolation is to add a small resistor (R_{OUT} equal to 50Ω, for example) in series with the output.

Figure 20 and Figure 21 illustrate graphs of *Small-Signal Overshoot vs Capacitive Load* for several values of R_{OUT} . Also, refer to [Applications Bulletin AB-028](#) (literature number [SBOA015](#), available for download from the [TI web site](#)) for details of analysis techniques and application circuits.

NOISE PERFORMANCE

Figure 32 shows the total circuit noise for varying source impedances with the operational amplifier in a unity-gain configuration (with no feedback resistor network and therefore no additional noise contributions). The OPA141 and OPA211 are shown with total circuit noise calculated. The op amp itself

contributes both a voltage noise component and a current noise component. The voltage noise is commonly modeled as a time-varying component of the offset voltage. The current noise is modeled as the time-varying component of the input bias current and reacts with the source resistance to create a voltage component of noise. Therefore, the lowest noise op amp for a given application depends on the source impedance. For low source impedance, current noise is negligible, and voltage noise generally dominates. The OPA141, OPA2141, and OPA4141 family has both low voltage noise and extremely low current noise because of the FET input of the op amp. As a result, the current noise contribution of the OPAx141 series is negligible for any practical source impedance, which makes it the better choice for applications with high source impedance.

The equation in Figure 32 shows the calculation of the total circuit noise, with these parameters:

- e_n = voltage noise
- I_n = current noise
- R_S = source impedance
- k = Boltzmann's constant = 1.38×10^{-23} J/K
- T = temperature in degrees Kelvin (K)

For more details on calculating noise, see the section on [Basic Noise Calculations](#).

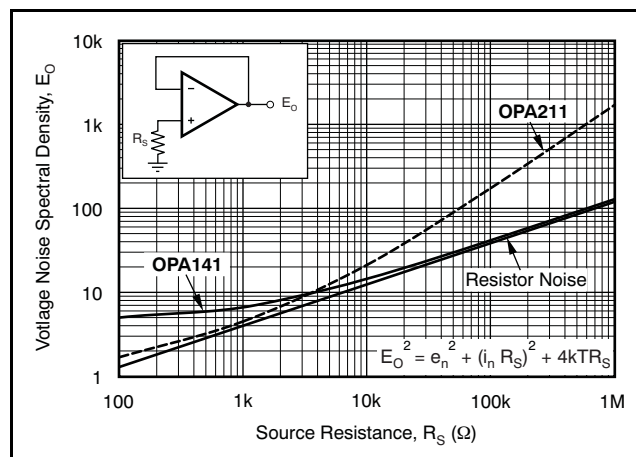


Figure 32. Noise Performance of the OPA141 and OPA211 in Unity-Gain Buffer Configuration

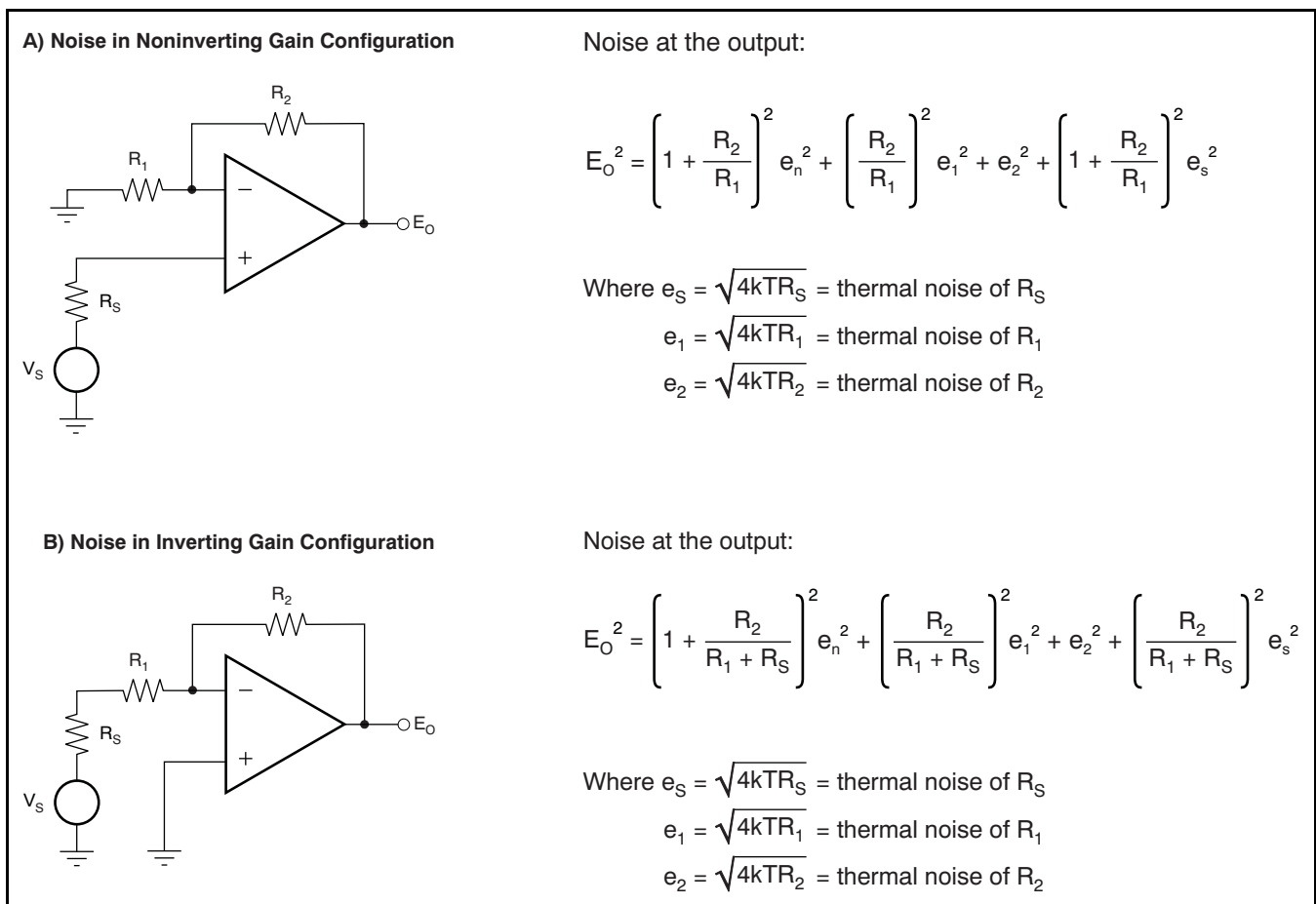
BASIC NOISE CALCULATIONS

Low-noise circuit design requires careful analysis of all noise sources. External noise sources can dominate in many cases; consider the effect of source resistance on overall op amp noise performance. Total noise of the circuit is the root-sum-square combination of all noise components.

The resistive portion of the source impedance produces thermal noise proportional to the square root of the resistance. This function is plotted in [Figure 32](#). The source impedance is usually fixed; consequently, select the op amp and the feedback resistors to minimize the respective contributions to the total noise.

[Figure 33](#) illustrates both noninverting (A) and inverting (B) op amp circuit configurations with gain. In circuit configurations with gain, the feedback network resistors also contribute noise. In general, the current noise of the op amp reacts with the feedback resistors to create additional noise components. However, the extremely low current noise of the OPAX141 means that its current noise contribution can be neglected.

The feedback resistor values can generally be chosen to make these noise sources negligible. Note that low impedance feedback resistors load the output of the amplifier. The equations for total noise are shown for both configurations.



For the OPAX141 series of operational amplifiers at 1kHz, $e_n = 6.5\text{nV}/\sqrt{\text{Hz}}$.

Figure 33. Noise Calculation in Gain Configurations

PHASE-REVERSAL PROTECTION

The OPA141, OPA2141, and OPA4141 family has internal phase-reversal protection. Many FET- and bipolar-input op amps exhibit a phase reversal when the input is driven beyond its linear common-mode range. This condition is most often encountered in noninverting circuits when the input is driven beyond the specified common-mode voltage range, causing the output to reverse into the opposite rail. The input circuitry of the OPA141, OPA2141, and OPA4141 prevents phase reversal with excessive common-mode voltage; instead, the output limits into the appropriate rail (see [Figure 22](#)).

OUTPUT CURRENT LIMIT

The output current of the OPAx141 series is limited by internal circuitry to +36mA/–30mA (sourcing/sinking), to protect the device if the output is accidentally shorted. This short-circuit current depends on temperature, as shown in [Figure 29](#).

POWER DISSIPATION AND THERMAL PROTECTION

The OPAx141 series of op amps are capable of driving 2k Ω loads with power-supply voltages of up to ± 18 V over the specified temperature range. In a single-supply configuration, where the load is connected to the negative supply voltage, the minimum load resistance is 2.8k Ω at a supply voltage of +36V. For lower supply voltages (either single-supply or symmetrical supplies), a lower load resistance may be used, as long as the output current does not exceed 13mA; otherwise, the device short-circuit current protection circuit may activate.

Internal power dissipation increases when operating at high supply voltages. Copper leadframe construction used in the OPA141, OPA2141, and OPA4141 series devices improves heat dissipation compared to conventional materials. Printed circuit board (PCB) layout can also help reduce a possible increase in junction temperature. Wide copper traces help dissipate the heat by acting as an additional heatsink. Temperature rise can be further minimized by soldering the devices directly to the PCB rather than using a socket.

Although the output current is limited by internal protection circuitry, accidental shorting of one or more output channels of a device can result in excessive heating. For instance, when an output is shorted to mid-supply, the typical short-circuit current of 36mA leads to an internal power dissipation of over 600mW at a supply of ± 18 V.

In the case of a dual OPA2141 in an MSOP-8 package (thermal resistance $\theta_{JA} = 180^{\circ}\text{C/W}$), such power dissipation would lead the die temperature to be 220 $^{\circ}\text{C}$ above ambient temperature, when both channels are shorted. This temperature increase significantly decreases the operating life of the device.

In order to prevent excessive heating, the OPAx141 series has an internal thermal shutdown circuit, which shuts down the device if the die temperature exceeds approximately +180 $^{\circ}\text{C}$. Once this thermal shutdown circuit activates, a built-in hysteresis of 15 $^{\circ}\text{C}$ ensures that the die temperature must drop to approximately +165 $^{\circ}\text{C}$ before the device switches on again.

Additional consideration should be given to the combination of maximum operating voltage, maximum operating temperature, load, and package type. [Figure 34](#) and [Figure 35](#) show several practical considerations when evaluating the OPA2141 (dual version) and the OPA4141 (quad version).

As an example, the OPA4141 has a maximum total quiescent current of 12.4mA (3.1mA/channel) over temperature. The TSSOP-14 package has a typical thermal resistance of 135 $^{\circ}\text{C/W}$. This parameter means that because the junction temperature should not exceed 150 $^{\circ}\text{C}$ in order to ensure reliable operation, either the supply voltage must be reduced, or the ambient temperature should remain low enough so that the junction temperature does not exceed 150 $^{\circ}\text{C}$. This condition is illustrated in [Figure 34](#) for various package types. Moreover, resistive loading of the output causes additional power dissipation and thus self-heating, which also must be considered when establishing the maximum supply voltage or operating temperature. To this end, [Figure 35](#) shows the maximum supply voltage versus temperature for a worst-case dc load resistance of 2k Ω .

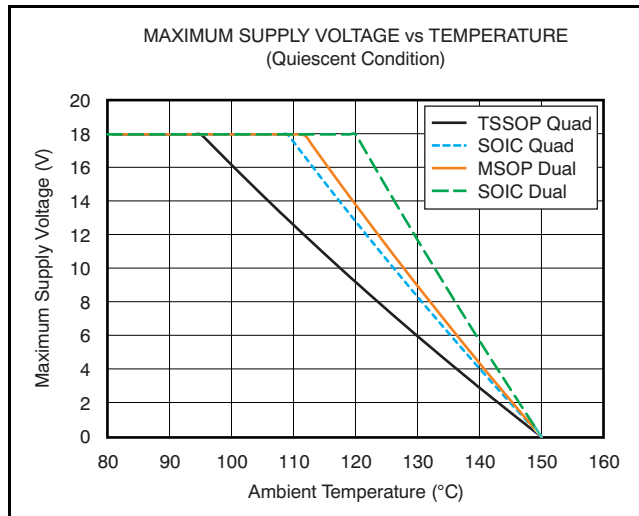


Figure 34. Maximum Supply Voltage vs Temperature (OPA2141 and OPA4141), Quiescent Condition

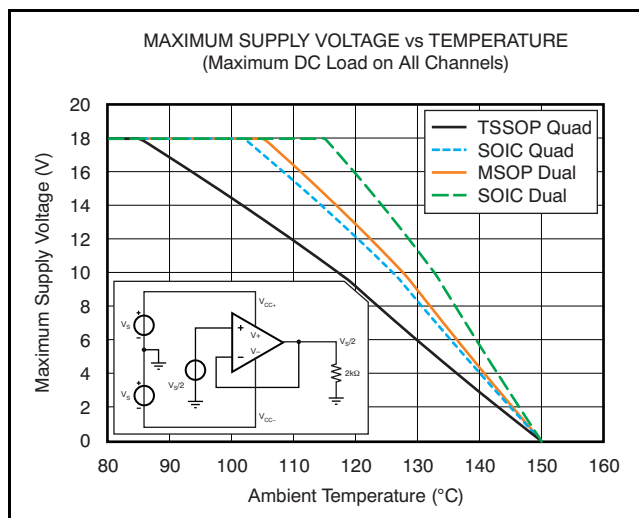


Figure 35. Maximum Supply Voltage vs Temperature (OPA2141 and OPA4141), Maximum DC Load

ELECTRICAL OVERSTRESS

Designers often ask questions about the capability of an operational amplifier to withstand electrical overstress. These questions tend to focus on the device inputs, but may involve the supply voltage pins or even the output pin. Each of these different pin

functions have electrical stress limits determined by the voltage breakdown characteristics of the particular semiconductor fabrication process and specific circuits connected to the pin. Additionally, internal electrostatic discharge (ESD) protection is built into these circuits to protect them from accidental ESD events both before and during product assembly.

It is helpful to have a good understanding of this basic ESD circuitry and its relevance to an electrical overstress event. See [Figure 36](#) for an illustration of the ESD circuits contained in the OPAx141 series (indicated by the dashed line area). The ESD protection circuitry involves several current-steering diodes connected from the input and output pins and routed back to the internal power-supply lines, where they meet at an absorption device internal to the operational amplifier. This protection circuitry is intended to remain inactive during normal circuit operation.

An ESD event produces a short duration, high-voltage pulse that is transformed into a short duration, high-current pulse as it discharges through a semiconductor device. The ESD protection circuits are designed to provide a current path around the operational amplifier core to prevent it from being damaged. The energy absorbed by the protection circuitry is then dissipated as heat.

When an ESD voltage develops across two or more of the amplifier device pins, current flows through one or more of the steering diodes. Depending on the path that the current takes, the absorption device may activate. The absorption device has a trigger, or threshold voltage, that is above the normal operating voltage of the OPAx141 but below the device breakdown voltage level. Once this threshold is exceeded, the absorption device quickly activates and clamps the voltage across the supply rails to a safe level.

When the operational amplifier connects into a circuit such as the one [Figure 36](#) shows, the ESD protection components are intended to remain inactive and not become involved in the application circuit operation. However, circumstances may arise where an applied voltage exceeds the operating voltage range of a given pin. Should this condition occur, there is a risk that some of the internal ESD protection circuits may be biased on, and conduct current. Any such current flow occurs through steering diode paths and rarely involves the absorption device.

Figure 36 depicts a specific example where the input voltage, V_{IN} , exceeds the positive supply voltage ($+V_S$) by 500mV or more. Much of what happens in the circuit depends on the supply characteristics. If $+V_S$ can sink the current, one of the upper input steering diodes conducts and directs current to $+V_S$. Excessively high current levels can flow with increasingly higher V_{IN} . As a result, the datasheet specifications recommend that applications limit the input current to 10mA.

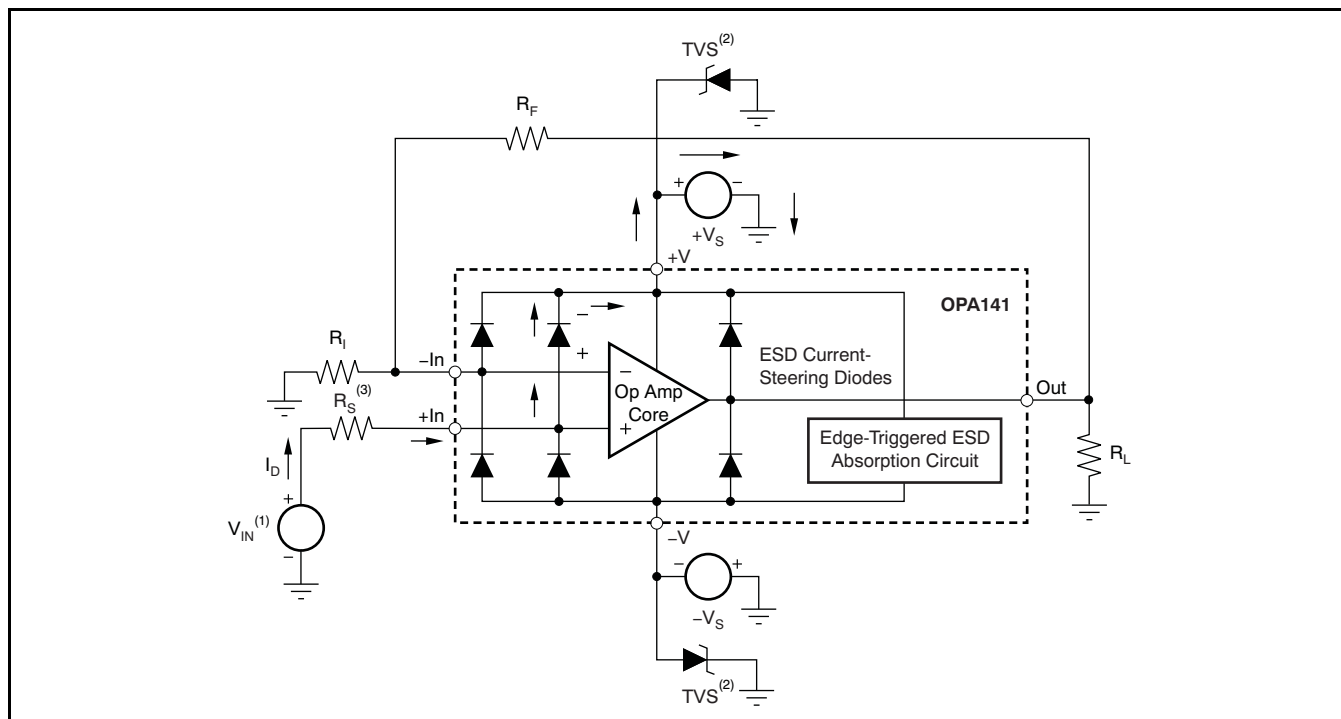
If the supply is not capable of sinking the current, V_{IN} may begin sourcing current to the operational amplifier, and then take over as the source of positive supply voltage. The danger in this case is that the voltage can rise to levels that exceed the operational amplifier absolute maximum ratings.

Another common question involves what happens to the amplifier if an input signal is applied to the input while the power supplies $+V_S$ and/or $-V_S$ are at 0V.

Again, it depends on the supply characteristic while at 0V, or at a level below the input signal amplitude. If the supplies appear as high impedance, then the operational amplifier supply current may be supplied by the input source via the current steering diodes. This state is not a normal bias condition; the amplifier most likely will not operate normally. If the supplies are low impedance, then the current through the steering diodes can become quite high. The current level depends on the ability of the input source to deliver current, and any resistance in the input path.

If there is an uncertainty about the ability of the supply to absorb this current, external zener diodes may be added to the supply pins as shown in Figure 36. The zener voltage must be selected such that the diode does not turn on during normal operation.

However, its zener voltage should be low enough so that the zener diode conducts if the supply pin begins to rise above the safe operating supply voltage level.



- (1) $V_{IN} = +V_S + 500\text{mV}$.
- (2) TVS: $+V_{S(\text{max})} > V_{\text{TVSBR}(\text{Min})} > +V_S$
- (3) Suggested value approximately 1k Ω .

Figure 36. Equivalent Internal ESD Circuitry and Its Relation to a Typical Circuit Application

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
OPA141AID	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	O141A	Samples
OPA141AIDGKR	ACTIVE	VSSOP	DGK	8	2500	RoHS & Green	Call TI NIPDAUAG NIPDAU	Level-2-260C-1 YEAR	-40 to 125	141	Samples
OPA141AIDGKT	ACTIVE	VSSOP	DGK	8	250	RoHS & Green	Call TI NIPDAUAG NIPDAU	Level-2-260C-1 YEAR	-40 to 125	141	Samples
OPA141AIDR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	O141A	Samples
OPA2141AID	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	O2141A	Samples
OPA2141AIDGKR	ACTIVE	VSSOP	DGK	8	2500	RoHS & Green	Call TI NIPDAUAG NIPDAU	Level-2-260C-1 YEAR	-40 to 125	2141	Samples
OPA2141AIDGKT	ACTIVE	VSSOP	DGK	8	250	RoHS & Green	Call TI NIPDAUAG NIPDAU	Level-2-260C-1 YEAR	-40 to 125	2141	Samples
OPA2141AIDR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	O2141A	Samples
OPA4141AID	ACTIVE	SOIC	D	14	50	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	O4141A	Samples
OPA4141AIDR	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	O4141A	Samples
OPA4141AIPW	ACTIVE	TSSOP	PW	14	90	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	O4141A	Samples
OPA4141AIPWR	ACTIVE	TSSOP	PW	14	2000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	O4141A	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSELETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

- (3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.
- (4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.
- (5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.
- (6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer:The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
OPA141AIDGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
OPA141AIDGKT	VSSOP	DGK	8	250	180.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
OPA141AIDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
OPA2141AIDGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
OPA2141AIDGKT	VSSOP	DGK	8	250	180.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
OPA2141AIDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
OPA4141AIDR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
OPA4141AIPWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
OPA141AIDGKR	VSSOP	DGK	8	2500	356.0	356.0	35.0
OPA141AIDGKT	VSSOP	DGK	8	250	210.0	185.0	35.0
OPA141AIDR	SOIC	D	8	2500	356.0	356.0	35.0
OPA2141AIDGKR	VSSOP	DGK	8	2500	353.0	353.0	32.0
OPA2141AIDGKT	VSSOP	DGK	8	250	210.0	185.0	35.0
OPA2141AIDR	SOIC	D	8	2500	356.0	356.0	35.0
OPA4141AIDR	SOIC	D	14	2500	356.0	356.0	35.0
OPA4141AIPWR	TSSOP	PW	14	2000	356.0	356.0	35.0

TUBE


*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
OPA141AID	D	SOIC	8	75	506.6	8	3940	4.32
OPA2141AID	D	SOIC	8	75	506.6	8	3940	4.32
OPA4141AID	D	SOIC	14	50	506.6	8	3940	4.32
OPA4141AIPW	PW	TSSOP	14	90	508	8.5	3250	2.8

DGK0008A



PACKAGE OUTLINE

VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



4214862/A 04/2023

NOTES:

PowerPAD is a trademark of Texas Instruments.

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.

EXAMPLE BOARD LAYOUT

DGK0008A

TM VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X



SOLDER MASK DETAILS

4214862/A 04/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.

EXAMPLE STENCIL DESIGN

DGK0008A

TM VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
SCALE: 15X

4214862/A 04/2023

NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.



D0014A

PACKAGE OUTLINE

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



4220718/A 09/2016

NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm, per side.
5. Reference JEDEC registration MS-012, variation AB.

EXAMPLE BOARD LAYOUT

D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE
SCALE:8X



SOLDER MASK DETAILS

4220718/A 09/2016

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:8X

4220718/A 09/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PW0014A



PACKAGE OUTLINE
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



4220202/B 12/2023

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

EXAMPLE BOARD LAYOUT

PW0014A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



4220202/B 12/2023

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

PW0014A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220202/B 12/2023

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.



D0008A

PACKAGE OUTLINE

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



4214825/C 02/2019

NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed $.006$ [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.

EXAMPLE BOARD LAYOUT

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

重要声明和免责声明

TI“按原样”提供技术和可靠性数据（包括数据表）、设计资源（包括参考设计）、应用或其他设计建议、网络工具、安全信息和其他资源，不保证没有瑕疵且不做任何明示或暗示的担保，包括但不限于对适销性、某特定用途方面的适用性或不侵犯任何第三方知识产权的暗示担保。

这些资源可供使用 TI 产品进行设计的熟练开发人员使用。您将自行承担以下全部责任：(1) 针对您的应用选择合适的 TI 产品，(2) 设计、验证并测试您的应用，(3) 确保您的应用满足相应标准以及任何其他功能安全、信息安全、监管或其他要求。

这些资源如有变更，恕不另行通知。TI 授权您仅可将这些资源用于研发本资源所述的 TI 产品的应用。严禁对这些资源进行其他复制或展示。您无权使用任何其他 TI 知识产权或任何第三方知识产权。您应全额赔偿因在这些资源的使用中对 TI 及其代表造成的任何索赔、损害、成本、损失和债务，TI 对此概不负责。

TI 提供的产品受 [TI 的销售条款](#) 或 [ti.com](#) 上其他适用条款/TI 产品随附的其他适用条款的约束。TI 提供这些资源并不会扩展或以其他方式更改 TI 针对 TI 产品发布的适用的担保或担保免责声明。

TI 反对并拒绝您可能提出的任何其他或不同的条款。

邮寄地址：Texas Instruments, Post Office Box 655303, Dallas, Texas 75265

Copyright © 2024，德州仪器 (TI) 公司