OPAx172 36V 单电源 10MHz 轨到轨输出运算放大器

1 特性

- 宽电源范围：
  +4.5V 至 +36V，±2.25V 至 ±18V
- 低偏移电压：±0.2mV
- 低偏移漂移：±0.3μV/°C
- 增益带宽：10MHz
- 低输入偏置电流 ：±8pA
- 低静态电流：每放大器 1.6mA
- 低噪声：7nV/√Hz
- 已过滤电磁干扰 (EMI) 和射频干扰 (RFI) 的输入
- 输入范围包括负电源
- 输入范围运行至正电源
- 轨到轨输出
- 高共模抑制：120dB
- 行业标准封装：
  - SOIC-8、VSSOP-8、SOIC-14、TSSOP-14
- *微型*封装：单电源版本采用 SC70 和 SOT-23 封装；
  双电源版本采用 WSON-8 封装

2 应用

- 电源模块内的跟踪放大器
- 商用电源
- 传感器放大器
- 桥式放大器
- 温度测量
- 应力计放大器
- 精密积分器
- 测试设备

3 说明

OPA172、OPA2172 和 OPA4172 (OPAx172) 属于 36V、单电源、低噪声运算放大器系列，该系列放大器能够在 +4.5V (±2.25V) 至 +36V (±18V) 的电源范围内运行。这款最新补充的高压 CMOS 运算放大器与 OPAx171 和 OPAx170 搭配，为用户提供了广泛的带宽、噪声和功率选择，可以满足各种应用的 需要。OPAx172 采用微型封装并且提供低偏移、漂移和静态电流。这些器件还提供宽带宽、快速转换率和高输出电流驱动能力。单通道、双通道和四通道版本均具有相同的技术规格，可最大程度地提高设计灵活性。

与大多数只在一个电源电压下额定运行的运算放大器不同，OPAx172 系列可在 +4.5 至 +36V 的电压范围内额定运行。超过电源轨的输入信号不会导致相位反向。输入可在负电源轨以下 100mV 以及正电源轨 2V 之内正常运行。请注意这些器件可在正电源轨之上 100mV 的满轨到轨输入上运行，但是在正电源轨 2V 之内运行时性能会受到影响。

OPAx172 系列运算放大器额定运行温度范围为 -40°C 至 +125°C。

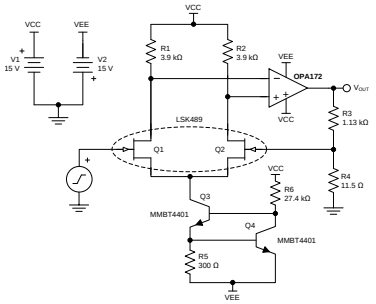
器件信息(1)

器件型号	封装	封装尺寸（标称值）
OPA172	SC70 (5)	2.00mm × 1.25mm
	SOT-23 (5)	2.90mm × 1.60mm
	SOIC (8)	4.90mm × 3.91mm
OPA2172	SOIC (8)	4.90mm × 3.91mm
	VSSOP (8)(2)	3.00mm × 3.00mm
	WSON (8)	3.00mm × 3.00mm
OPA4172	SOIC (14)	8.65mm × 3.91mm
	TSSOP (14)	4.40mm × 5.00mm

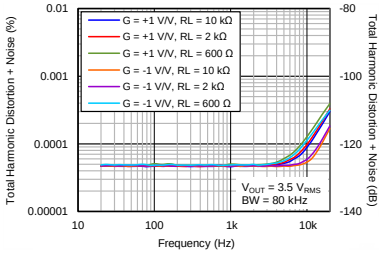
(1) 如需了解所有可用封装，请参见产品说明书末尾的封装选项附录。

(2) VSSOP 封装与 MSOP 封装相同。

JFET 输入低噪声放大器



出色的总谐波失真 (THD) 性能



目录

4 修订历史记录

Changes from Revision H (September 2015) to Revision I — **Page**

- Changed supply voltage values within *Absolute Maximum Ratings* table ... 7

Changes from Revision G (June 2015) to Revision H — **Page**

- 已添加 DRG 封装至 OPA2172 器件 ... 1
- 已添加 WSON 至最后一个特性要点 ... 1
- 已添加 OPA2172 WSON 行至*器件信息*表 ... 1
- Added WSON-8 to OPA2172 row of *Device Comparison* table ... 4
- Added DRG pinout drawing ... 6
- Added DRG column to OPA2172 and OPA4172 *Pin Functions* table ... 6
- Added DRG column to OPA2172 *Thermal Information* table ... 8

Changes from Revision F (June 2015) to Revision G — **Page**

- Added input bias current (I_B) values for DGK and PW packages. ... 9

Changes from Revision E (December 2014) to Revision F — **Page**

- 已将器件状态从混合状态改为量产数据 ... 1
- 已将 OPA2172 DGK 和 OPA4172 PW 封装改为量产数据 ... 1
- 已添加 OPA2172 VSSOP 和 OPA4172 TSSOP 行至*器件信息*表 ... 1
- Deleted footnote from *Device Comparison* table ... 4
- Deleted footnote from OPA2172 DGK and OPA4172 PW pin out drawings ... 6
- Added OPA2172 DGK thermal information ... 8

Changes from Revision D (September 2014) to Revision E **Page**

- 已将 OPA2172 D 封装从产品预览改为量产数据 1
- 已更改*器件信息表* 1
- Changed *Device Comparison* table note (1) to show preview packages 4
- Changed *Handling Ratings* table to *ESD Ratings* table 7

Changes from Revision C (July 2014) to Revision D **Page**

- 已更改低噪声 特性 要点值，从 6nV/√Hz 改为 7 1
- 已将 特性 要点中的 MSOP 改为 VSSOP 1
- 已添加封装和新的注释 2 至*器件信息表* 1
- Changed OPAx172 voltage noise density from 6 nV/√Hz to 7 in *Device Family Comparison* table 4
- Changed OPA4172 package from DGK to PW in *Pin Functions* table 6
- Added OPA2172 *Thermal Information* table 8
- Changed input voltage noise value in *Electrical Characteristics* from 1.2 μV_{PP} to 2.5 μV_{PP} 9
- Changed input voltage noise density value at 100 Hz in *Electrical Characteristics* from 8.6 nV/√Hz to 12 9
- Changed input voltage noise density value at 1 kHz in *Electrical Characteristics* from 6 nV/√Hz to 7 9
- Changed voltage output swing values in the *Electrical Characteristics* 10
- Changed 图 13 13
- Changed 图 14 13
- Added new note to *Applications and Implementation* section 25

Changes from Revision B (May 2014) to Revision C **Page**

- 已将 OPA4172 D 封装 (SOIC-14) 从产品预览改为量产数据 1
- Added OPA4172-D Thermal information 8
- Added Channel separation parameter to the *Electrical Characteristics* 9
- Added Channel Separation vs Frequency plot 17

Changes from Revision A (April 2014) to Revision B **Page**

- 已将 DCK (SC70) 封装从产品预览改为量产数据 1

Changes from Original (December 2013) to Revision A **Page**

- 已更改文档格式以符合最新产品说明书标准；已添加*处理额定值*、*建议运行条件*以及*器件和文档支持*部分，并已移动现有部分 1
- Changed DCK package pin names from IN+ and IN– to +IN and –IN, respectively 5
- Changed DBV package from product preview to production data 5
- Changed 图 9 12
- Added *Functional Block Diagram* section 19
- Added *Capacitive Load Drive Solution Using an Isolation Resistor* section 25
- Added *Power-Supply Recommendations* section 28
- Changed *Layout Guidelines* section 29

5 Device Comparison

5.1 Device Comparison

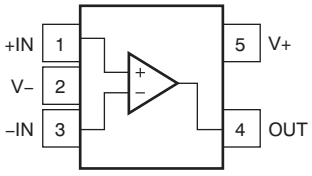
DEVICE	PACKAGE
OPA172 (single)	SC70-5, SOT-23-5, SOIC-8
OPA2172 (dual)	SOIC-8, VSSOP-8, WSON-8
OPA4172 (quad)	SOIC-14, TSSOP-14

5.2 Device Family Comparison

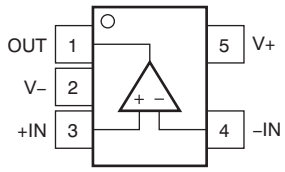
DEVICE	QUIESCENT CURRENT (I_Q)	GAIN BANDWIDTH PRODUCT (GBP)	VOLTAGE NOISE DENSITY (e_n)
OPAx172	1600 µA	10 MHz	7 nV/$\sqrt{Hz}$
OPAx171	475 µA	3.0 MHz	14 nV/$\sqrt{Hz}$
OPAx170	110 µA	1.2 MHz	19 nV/$\sqrt{Hz}$

6 Pin Configuration and Functions

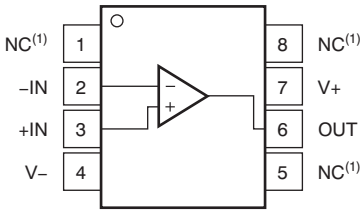
DCK Package: OPA172
SC70-5
Top View



DBV Package: OPA172
SOT-23-5
Top View



D Package: OPA172
SOIC-8
Top View

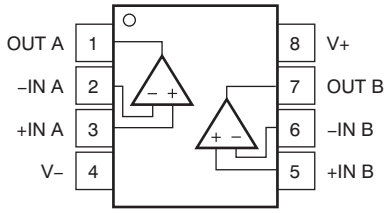


(1) No internal connection.

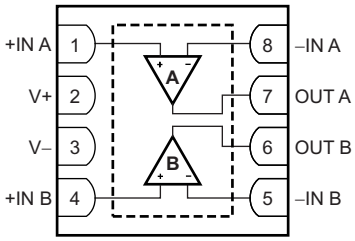
Pin Functions: OPA172

PIN				I/O	DESCRIPTION
	OPA172				
NAME	D (SOIC)	DBV (SOT)	DCK (SC70)		
+IN	3	3	1	I	Noninverting input
–IN	2	4	3	I	Inverting input
NC	1, 5, 8	—	—	—	No internal connection
OUT	6	1	4	O	Output
V+	7	5	5	—	Positive (highest) power supply
V–	4	2	2	—	Negative (lowest) power supply

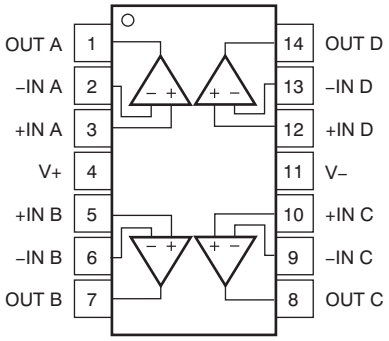
D and DGK Packages: OPA2172
SOIC-8 and VSSOP-8
Top View



DRG Package: OPA2172
WSON-8
Top View



D and PW Packages: OPA4172
SO-14 and TSSOP-14
Top View



Pin Functions: OPA2172 and OPA4172

PIN				I/O	DESCRIPTION
	OPA2172		OPA4172		
NAME	D (SOIC), DGK (VSSOP)	DRG (WSON)	D (SOIC), PW (TSSOP)		
+IN A	3	1	3	I	Noninverting input, channel A
+IN B	5	4	5	I	Noninverting input, channel B
+IN C	—	—	10	I	Noninverting input, channel C
+IN D	—	—	12	I	Noninverting input, channel D
–IN A	2	8	2	I	Inverting input, channel A
–IN B	6	5	6	I	Inverting input, channel B
–IN C	—	—	9	I	Inverting input,,channel C
–IN D	—	—	13	I	Inverting input, channel D
OUT A	1	7	1	O	Output, channel A
OUT B	7	6	7	O	Output, channel B
OUT C	—	—	8	O	Output, channel C
OUT D	—	—	14	O	Output, channel D
V+	8	2	4	—	Positive (highest) power supply
V–	4	3	11	—	Negative (lowest) power supply

7 Specifications

7.1 Absolute Maximum Ratings(1)

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
Supply voltage, [(V+) – (V-)]				40	V
Signal input pins	Voltage(2)	Common-mode	(V–) – 0.5	(V+) + 0.5	V
		Differential(3)		±0.5	
Signal input pins	Current			±10	mA
Output short circuit(4)			Continuous		
Operating temperature			–55	+150	°C
Junction temperature, T_J				+150	°C
Storage temperature, T_{stg}			–65	+150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Transient conditions that exceed these voltage ratings must be current limited to 10 mA or less.
(3) Refer to the *Electrical Overstress* section for more information.
(4) Short-circuit to ground, one amplifier per package.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±4000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

	MIN	MAX	UNIT
Supply voltage (V+ – V–)	4.5 (±2.25)	36 (±18)	V
Specified temperature	–40	125	°C

7.4 Thermal Information: OPA172

THERMAL METRIC(1)		OPA172			UNIT
		D (SOIC)	DBV (SOT-23)	DCK (SC70)	
		8 PINS	5 PINS	5 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	126.5	227.9	285.2	°C/W
$R_{\theta JC(top)}$	Junction-to-case(top) thermal resistance	80.6	115.7	60.5	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	67.1	65.9	78.9	°C/W
ψ_{JT}	Junction-to-top characterization parameter	31.0	10.7	0.8	°C/W
ψ_{JB}	Junction-to-board characterization parameter	66.6	65.3	77.9	°C/W
$R_{\theta JC(bot)}$	Junction-to-case(bottom) thermal resistance	N/A	N/A	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC package Thermal Metrics* application report.

7.5 Thermal Information: OPA2172

THERMAL METRIC(1)		OPA2172			UNIT
		D (SOIC)	DGK (VSSOP)	DRG (WSON)	
		8 PINS	8 PINS	8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	116.1	158	63.2	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	69.8	48.6	63.5	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	56.6	78.7	36.5	°C/W
ψ_{JT}	Junction-to-top characterization parameter	22.5	3.9	1.4	°C/W
ψ_{JB}	Junction-to-board characterization parameter	56.1	77.3	36.6	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	6.3	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC package Thermal Metrics* application report.

7.6 Thermal Information: OPA4172

THERMAL METRIC(1)		OPA4172		UNIT
		D (SOIC)	PW (TSSOP)	
		14 PINS	14 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	82.7	111.1	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	42.3	40.8	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	37.3	54.1	°C/W
ψ_{JT}	Junction-to-top characterization parameter	8.9	3.8	°C/W
ψ_{JB}	Junction-to-board characterization parameter	37	53.3	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC package Thermal Metrics* application report.

7.7 Electrical Characteristics

At T_A = +25°C, V_S = ±2.25 V to ±18 V, V_{CM} = V_{OUT} = V_S / 2, and R_L = 10 kΩ connected to V_S / 2 (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
OFFSET VOLTAGE							
V_{OS}	Input offset voltage				±0.2	±1	mV
		T_A = –40°C to +125°C				±1.15	
dV_{OS}/dT	Drift	T_A = –40°C to +125°C	OPA172, OPA4172		±0.3	±1.5	µV/°C
			OPA2172			±1.8	
PSRR	vs power supply	T_A = –40°C to +125°C			±1	±3	µV/V
	Channel separation, dc	At dc			5		µV/V
INPUT BIAS CURRENT							
I_B	Input bias current				±8	±15	pA
		T_A = –40°C to +125°C				±14	nA
		T_A = –40°C to +125°C	OPA2172IDGK			±18	
			OPA41721PW				
I_{OS}	Input offset current				±2	±15	pA
		T_A = –40°C to +125°C	OPA172, OPA4172			±1	nA
			OPA2172			±3	
NOISE							
E_n	Input voltage noise	f = 0.1 Hz to 10 Hz			2.5		μV_{PP}
e_n	Input voltage noise density	f = 100 Hz			12		$nV/\sqrt{Hz}$
		f = 1 kHz			7		
i_n	Input current noise density	f = 1 kHz			1.6		$fA/\sqrt{Hz}$

Electrical Characteristics (continued)

At T_A = +25°C, V_S = ±2.25 V to ±18 V, V_{CM} = V_{OUT} = V_S / 2, and R_L = 10 kΩ connected to V_S / 2 (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
INPUT VOLTAGE							
V_{CM}	Common-mode voltage range(1)			(V–) – 0.1 V		(V+) – 2 V	V
CMRR	Common-mode rejection ratio	V_S = ±2.25 V, (V–) – 0.1 V < V_{CM} < (V+) – 2 V, T_A = –40°C to +125°C		90	104		dB
		V_S = ±18 V, (V–) – 0.1 V < V_{CM} < (V+) – 2 V, T_A = –40°C to +125°C		110	120		
INPUT IMPEDANCE							
	Differential				100 || 4		MΩ || pF
	Common-mode				6 || 4		10^{13}Ω || pF
OPEN-LOOP GAIN							
A_{OL}	Open-loop voltage gain	(V–) + 0.35 V < V_O < (V+) – 0.35 V, R_L = 10 kΩ, T_A = –40°C to +125°C	OPA172, OPA4172	110	130		dB
			OPA2172	107	115		
		(V–) + 0.5 V < V_O < (V+) – 0.5 V, R_L = 2 kΩ, T_A = –40°C to +125°C	OPA172, OPA4172		116		
			OPA2172		107		
FREQUENCY RESPONSE							
GBP	Gain bandwidth product				10		MHz
SR	Slew rate	G = +1			10		V/µs
t_S	Settling time	To 0.1%, V_S = ±18 V, G = +1, 10-V step			2		µs
		To 0.01% (12 bit), V_S = ±18 V, G = +1, 10-V step			3.2		
	Overload recovery time	V_{IN} × Gain > V_S			200		ns
THD+N	Total harmonic distortion + noise	V_S = +36 V, G = +1, f = 1 kHz, V_O = 3.5 V_{RMS}			0.00005%		
OUTPUT							
V_O	Voltage output swing from rail	V_S = +36 V	R_L = 10 kΩ		70	90	mV
			R_L = 2 kΩ		330	400	
		V_S = +36 V, T_A = –40°C to +125°C	R_L = 10 kΩ		95	120	
			R_L = 2 kΩ		470	530	
		V_S = +4.5V	R_L = 10 kΩ		10	20	
			R_L = 2 kΩ		40	50	
		V_S = +4.5 V, T_A = –40°C to +125°C	R_L = 10 kΩ		10	25	
			R_L = 2 kΩ		55	70	
I_{SC}	Short-circuit current				±75		mA
C_{LOAD}	Capacitive load drive				See *Typical Characteristics*		pF
Z_O	Open-loop output impedance	f = 1 MHz, I_O = 0 A			60		Ω
POWER SUPPLY							
V_S	Specified voltage range			+4.5		+36	V
I_Q	Quiescent current per amplifier	I_O = 0 A			1.6	1.8	mA
		I_O = 0 A, T_A = –40°C to +125°C				2	
TEMPERATURE							
	Specified range			–40		+125	°C

(1) The input range can be extended beyond (V+) – 2 V up to (V+) + 0.1 V. For additional information, see the *Typical Characteristics* and *Application Information* sections.

7.8 Typical Characteristics: Table of Graphs

表 1. List of Typical Characteristics

DESCRIPTION	FIGURE
Offset Voltage Production Distribution	图 1
Offset Voltage Drift Distribution	图 2
Offset Voltage vs Temperature (V_S = ±18 V)	图 3
Offset Voltage vs Common-Mode Voltage (V_S = ±18 V)	图 4
Offset Voltage vs Common-Mode Voltage (Upper Stage)	图 5
Offset Voltage vs Power Supply	图 6
I_B vs Common-Mode Voltage	图 7
Input Bias Current vs Temperature	图 8
Output Voltage Swing vs Output Current (Maximum Supply)	图 9
CMRR and PSRR vs Frequency (Referred-to Input)	图 10
CMRR vs Temperature	图 11
PSRR vs Temperature	图 12
0.1-Hz to 10-Hz Noise	图 13
Input Voltage Noise Spectral Density vs Frequency	图 14
THD+N Ratio vs Frequency	图 15
THD+N vs Output Amplitude	图 16
Quiescent Current vs Temperature	图 17
Quiescent Current vs Supply Voltage	图 18
Open-Loop Gain and Phase vs Frequency	图 19
Closed-Loop Gain vs Frequency	图 20
Open-Loop Gain vs Temperature	图 21
Open-Loop Output Impedance vs Frequency	图 22
Small-Signal Overshoot vs Capacitive Load (100-mV Output Step)	图 23, 图 24
Positive Overload Recovery	图 25, 图 26
Negative Overload Recovery	图 27, 图 28
Small-Signal Step Response (10 mV)	图 29, 图 30
Small-Signal Step Response (100 mV)	图 31, 图 32
Large-Signal Step Response (1 V)	图 33, 图 34
Large-Signal Settling Time (10-V Positive Step)	图 35
Large-Signal Settling Time (10-V Negative Step)	图 36
No Phase Reversal	图 37
Short-Circuit Current vs Temperature	图 38
Maximum Output Voltage vs Frequency	图 39
EMIRR vs Frequency	图 40
Channel Separation vs Frequency	图 41

7.9 Typical Characteristics

At V_S = ±18 V, V_{CM} = V_S / 2, R_{LOAD} = 10 kΩ connected to V_S / 2, and C_L = 100 pF, unless otherwise noted.

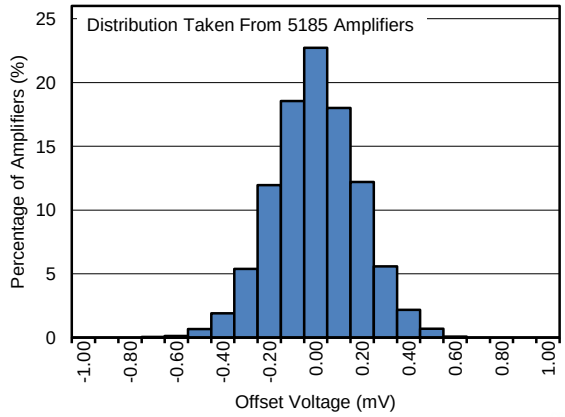


图 1. Offset Voltage Production Distribution

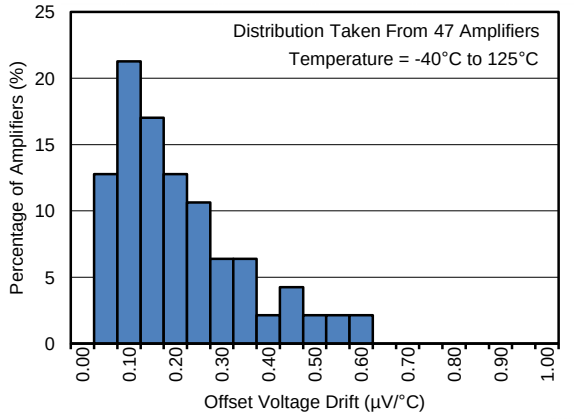


图 2. Offset Voltage Drift Production Distribution

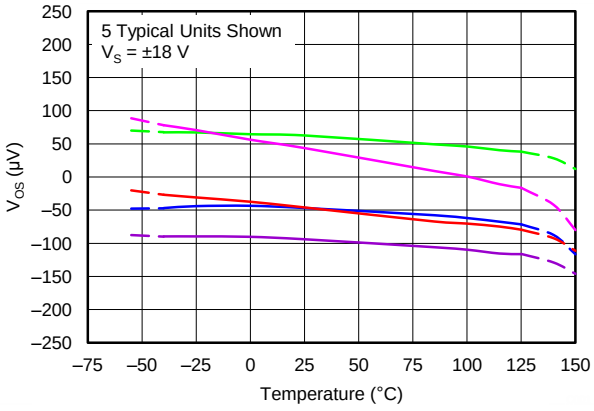


图 3. Offset Voltage vs Temperature (V_S = ±18 V)

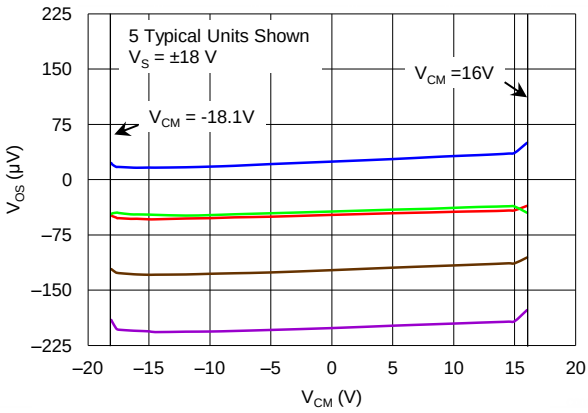


图 4. Offset Voltage vs Common-Mode Voltage (V_S = ±18 V)

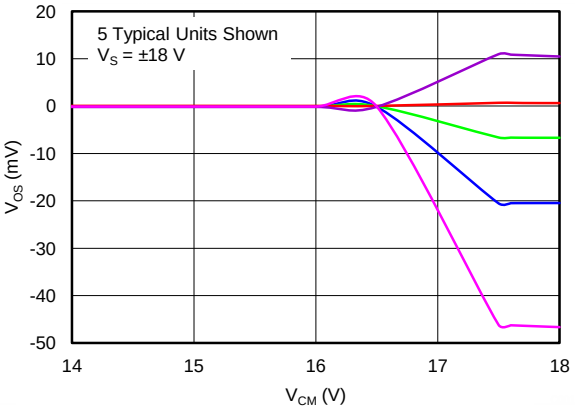


图 5. Offset Voltage vs Common-Mode Voltage (Upper Stage)

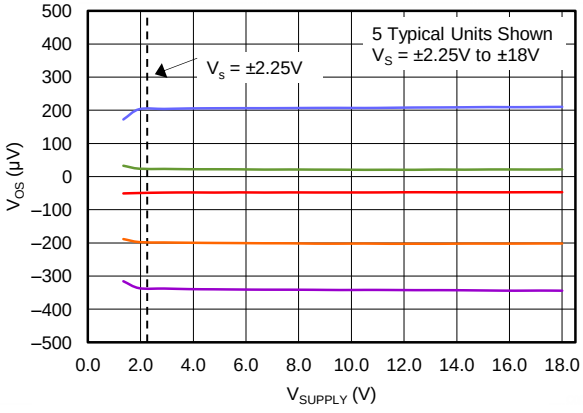


图 6. Offset Voltage vs Power Supply

Typical Characteristics (接下页)

At V_S = ±18 V, V_{CM} = V_S / 2, R_{LOAD} = 10 kΩ connected to V_S / 2, and C_L = 100 pF, unless otherwise noted.

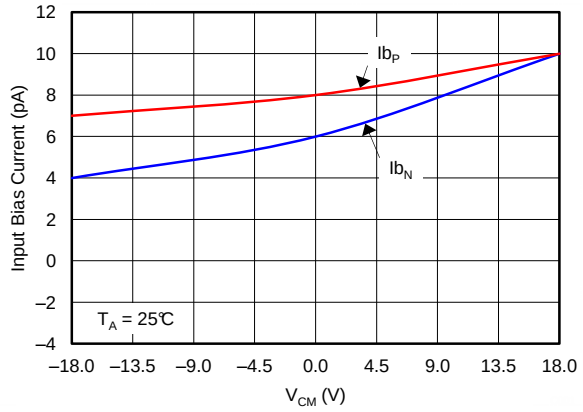


图 7. Input Bias Current vs Common-Mode Voltage

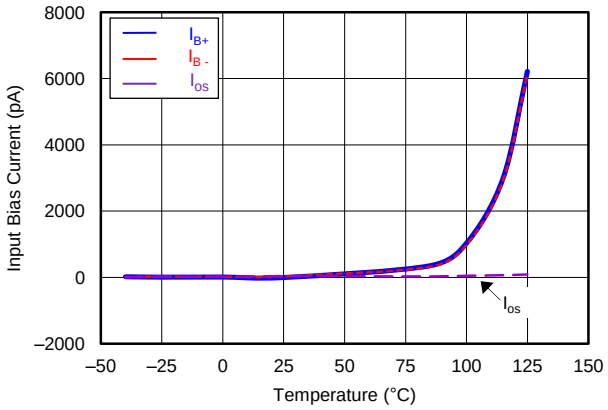


图 8. Input Bias Current vs Temperature

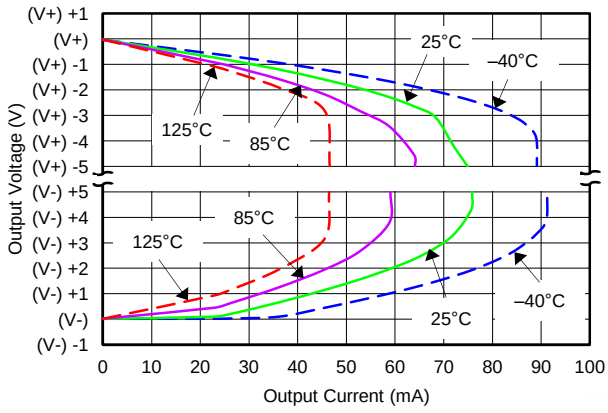


图 9. Output Voltage Swing vs Output Current (Maximum Supply)

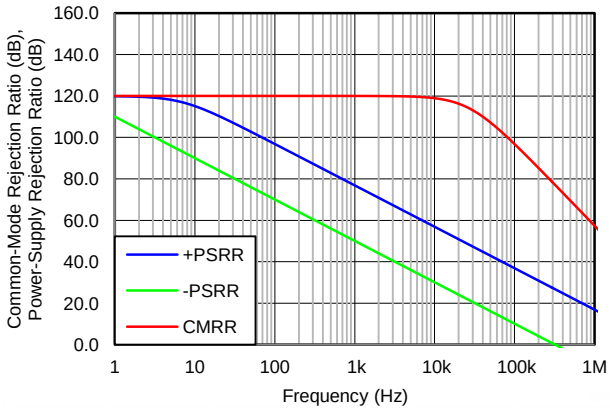


图 10. CMRR and PSRR vs Frequency (Referred-To-Input)

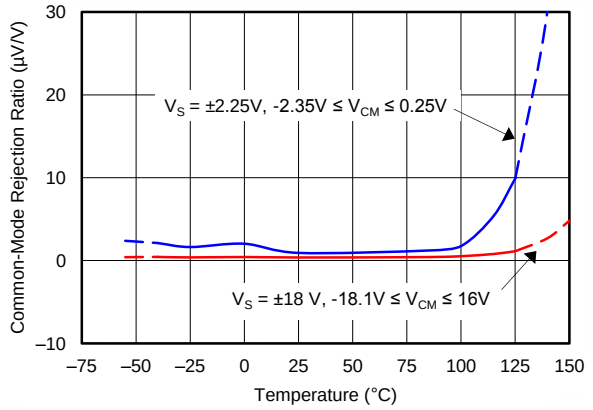


图 11. CMRR vs Temperature

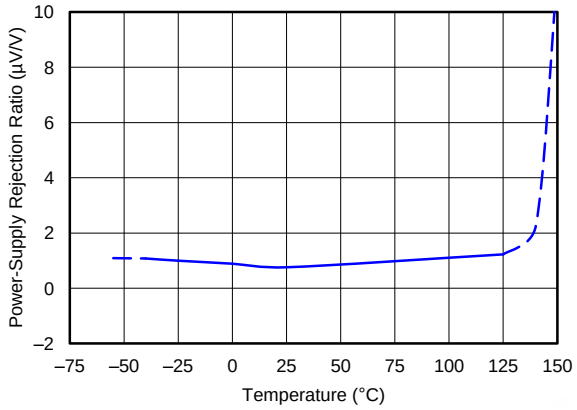


图 12. PSRR vs Temperature

Typical Characteristics (接下页)

At V_S = ±18 V, V_{CM} = V_S / 2, R_{LOAD} = 10 kΩ connected to V_S / 2, and C_L = 100 pF, unless otherwise noted.

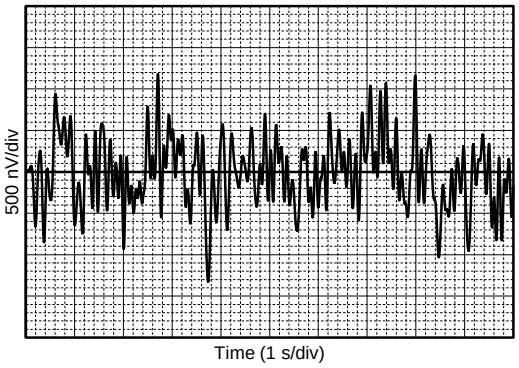


图 13. 0.1-Hz to 10-Hz Noise

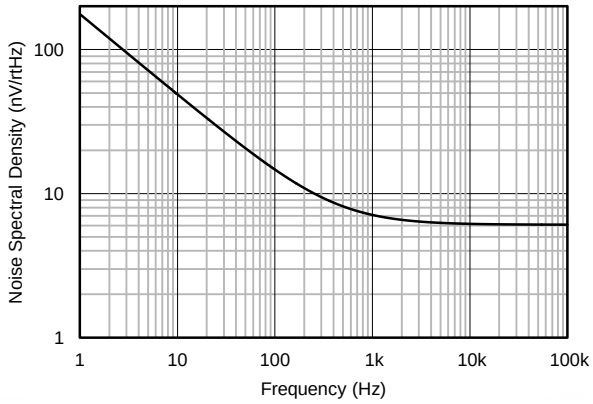


图 14. Input Voltage Noise Spectral Density vs Frequency

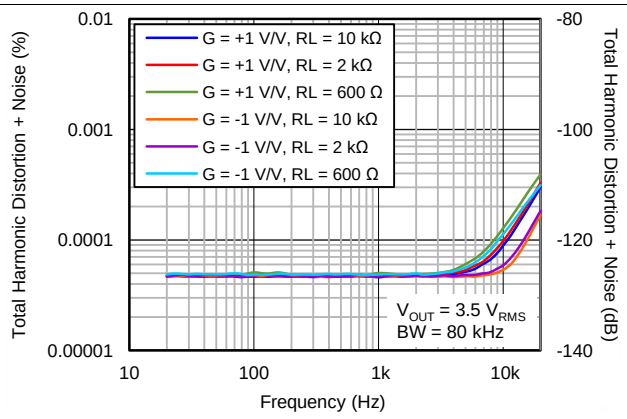


图 15. THD+N Ratio vs Frequency

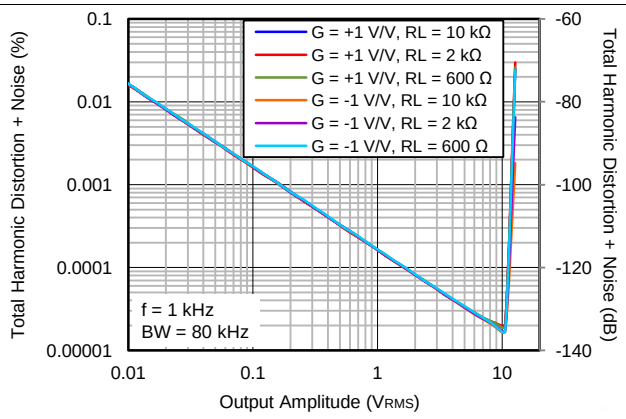


图 16. THD+N vs Output Amplitude

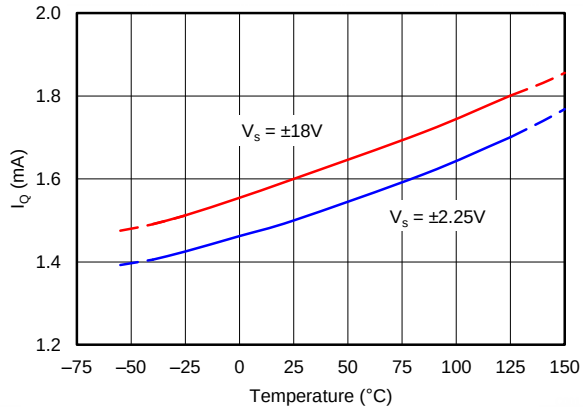


图 17. Quiescent Current vs Temperature

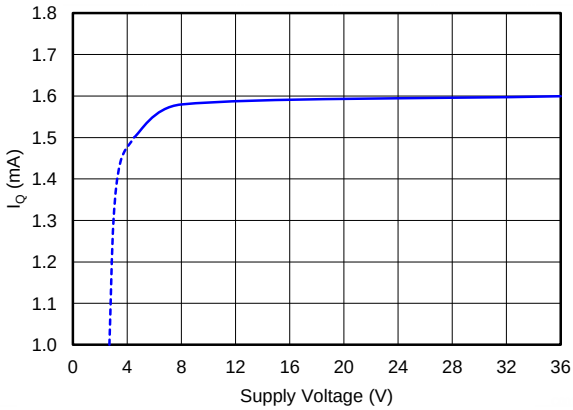


图 18. Quiescent Current vs Supply Voltage

Typical Characteristics (接下页)

At V_S = ±18 V, V_{CM} = V_S / 2, R_{LOAD} = 10 kΩ connected to V_S / 2, and C_L = 100 pF, unless otherwise noted.

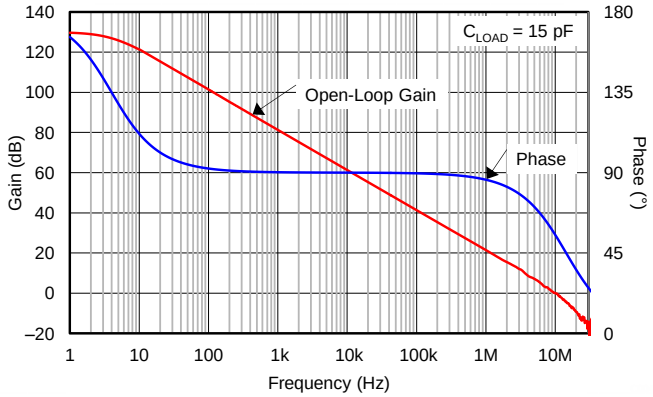


图 19. Open-Loop Gain and Phase vs Frequency

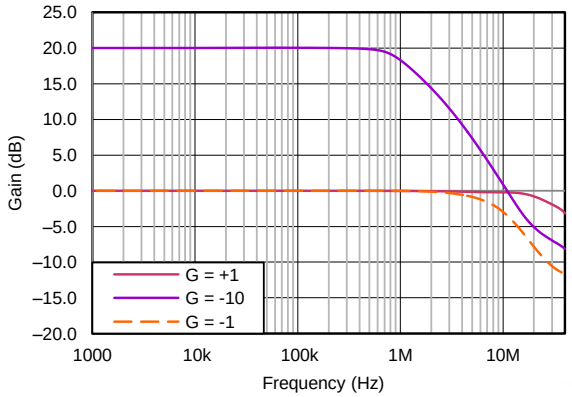


图 20. Closed-Loop Gain vs Frequency

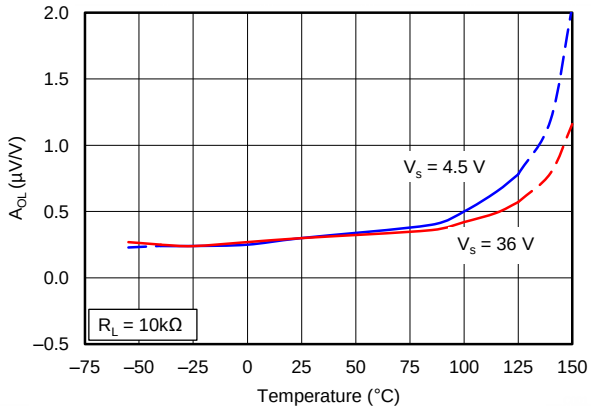


图 21. Open-Loop Gain vs Temperature

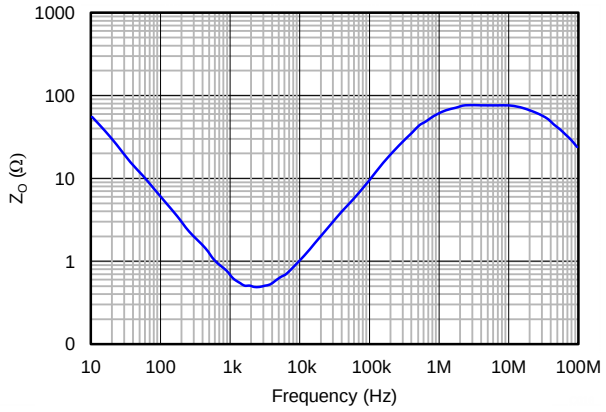


图 22. Open-Loop Output Impedance vs Frequency

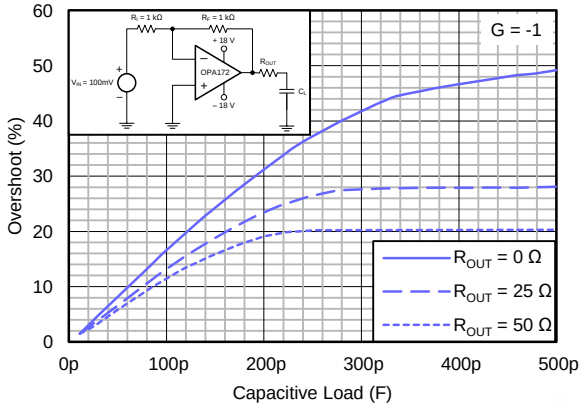


图 23. Small-Signal Overshoot vs Capacitive Load (100-mV Output Step)

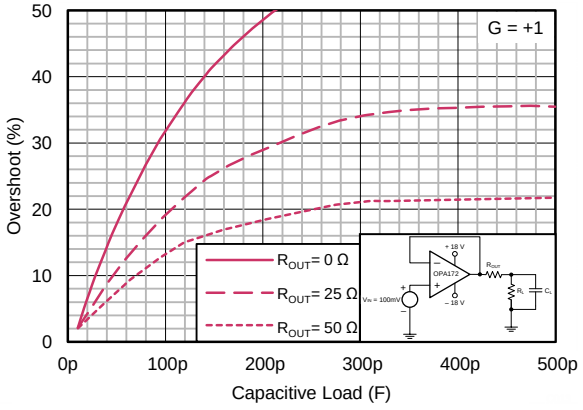


图 24. Small-Signal Overshoot vs Capacitive Load (100-mV Output Step)

Typical Characteristics (接下页)

At V_S = ±18 V, V_{CM} = V_S / 2, R_{LOAD} = 10 kΩ connected to V_S / 2, and C_L = 100 pF, unless otherwise noted.

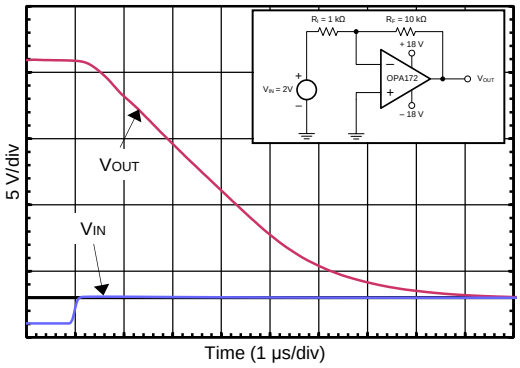


图 25. Positive Overload Recovery

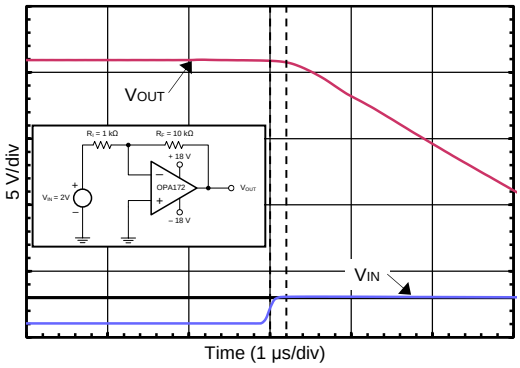


图 26. Positive Overload Recovery (Zoomed In)

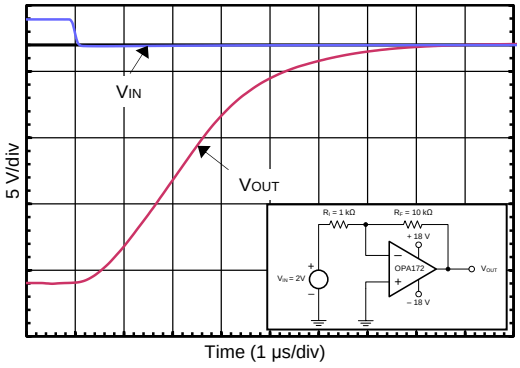


图 27. Negative Overload Recovery

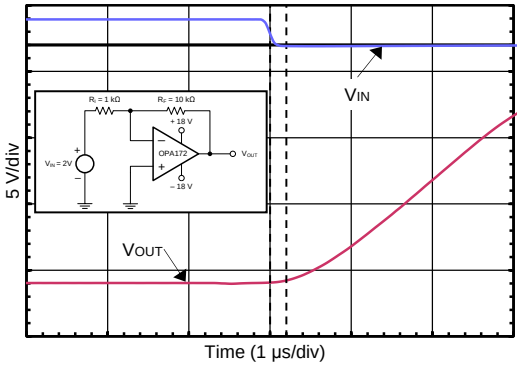


图 28. Negative Overload Recovery (Zoomed In)

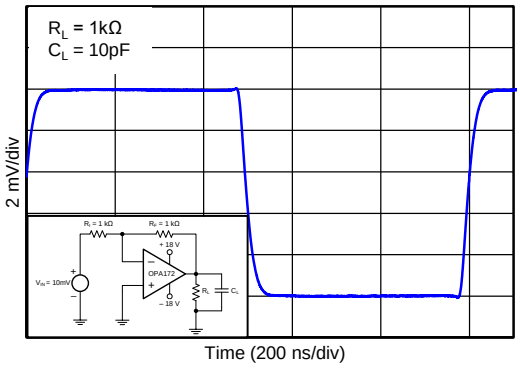


图 29. Small-Signal Step Response (10 mV, G = –1)

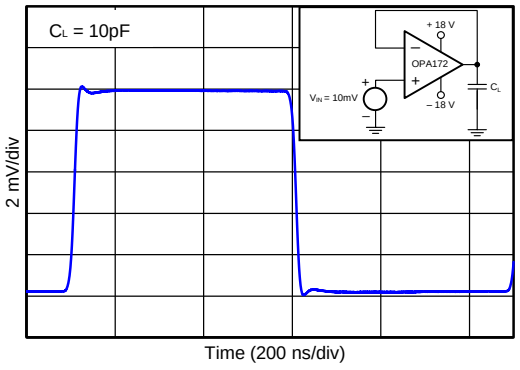


图 30. Small-Signal Step Response (10 mV, G = +1)

Typical Characteristics (接下页)

At V_S = ±18 V, V_{CM} = V_S / 2, R_{LOAD} = 10 kΩ connected to V_S / 2, and C_L = 100 pF, unless otherwise noted.

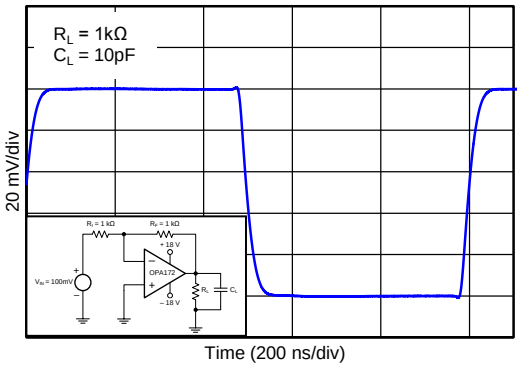


图 31. Small-Signal Step Response (100 mV, G = –1)

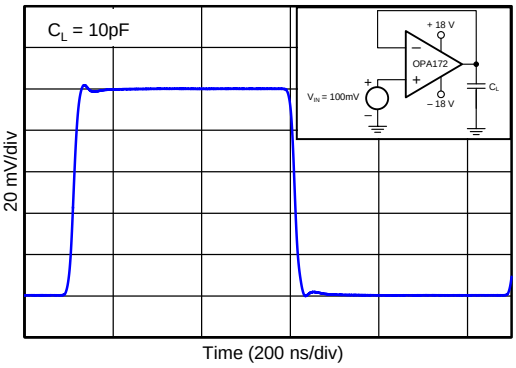


图 32. Small-Signal Step Response (100 mV, G = +1)

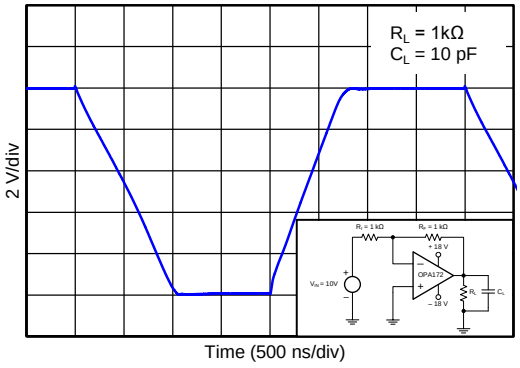


图 33. Large-Signal Step Response (10 V, G = –1)

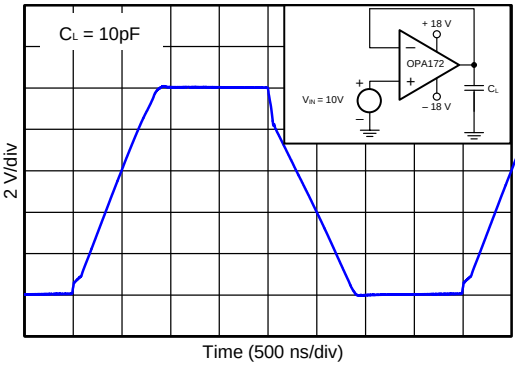


图 34. Large-Signal Step Response (10 V, G = +1)

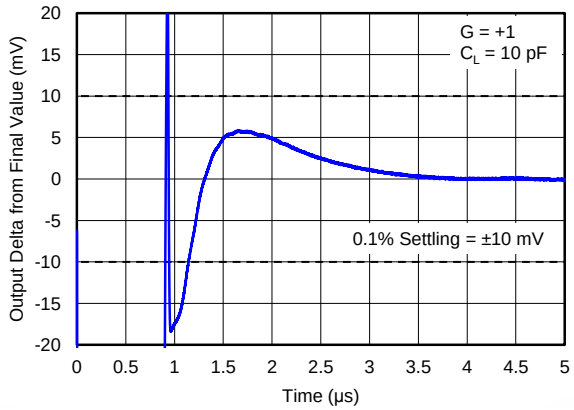


图 35. Large-Signal Settling Time (10-V Positive Step)

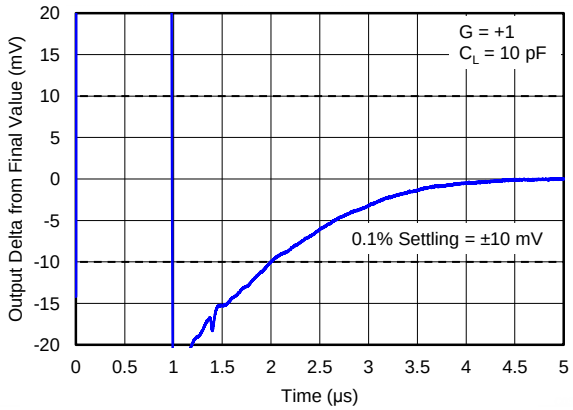


图 36. Large-Signal Settling Time (10-V Negative Step)

Typical Characteristics (接下页)

At V_S = ±18 V, V_{CM} = V_S / 2, R_{LOAD} = 10 kΩ connected to V_S / 2, and C_L = 100 pF, unless otherwise noted.

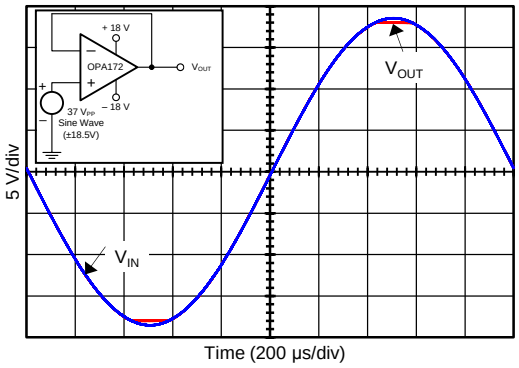


图 37. No Phase Reversal

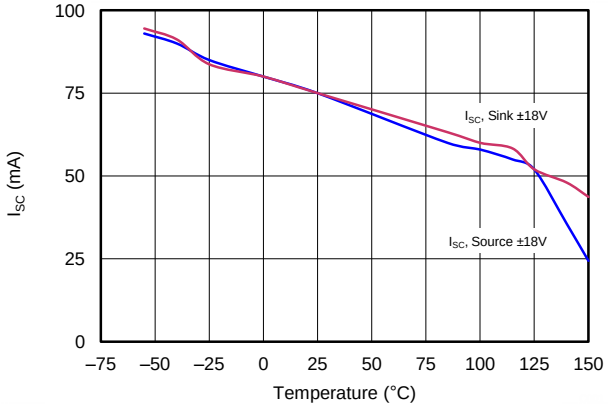


图 38. Short-Circuit Current vs Temperature

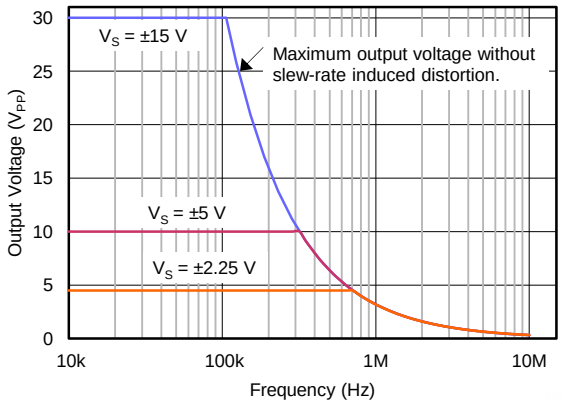


图 39. Maximum Output Voltage vs Frequency

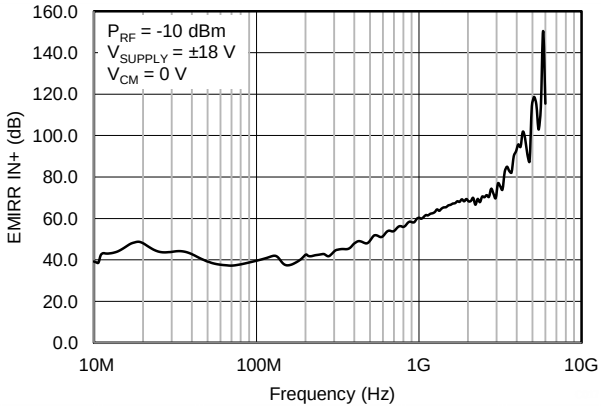


图 40. EMIRR vs Frequency

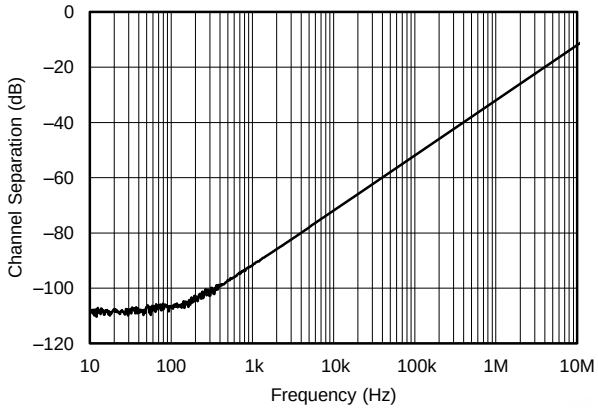


图 41. Channel Separation vs Frequency

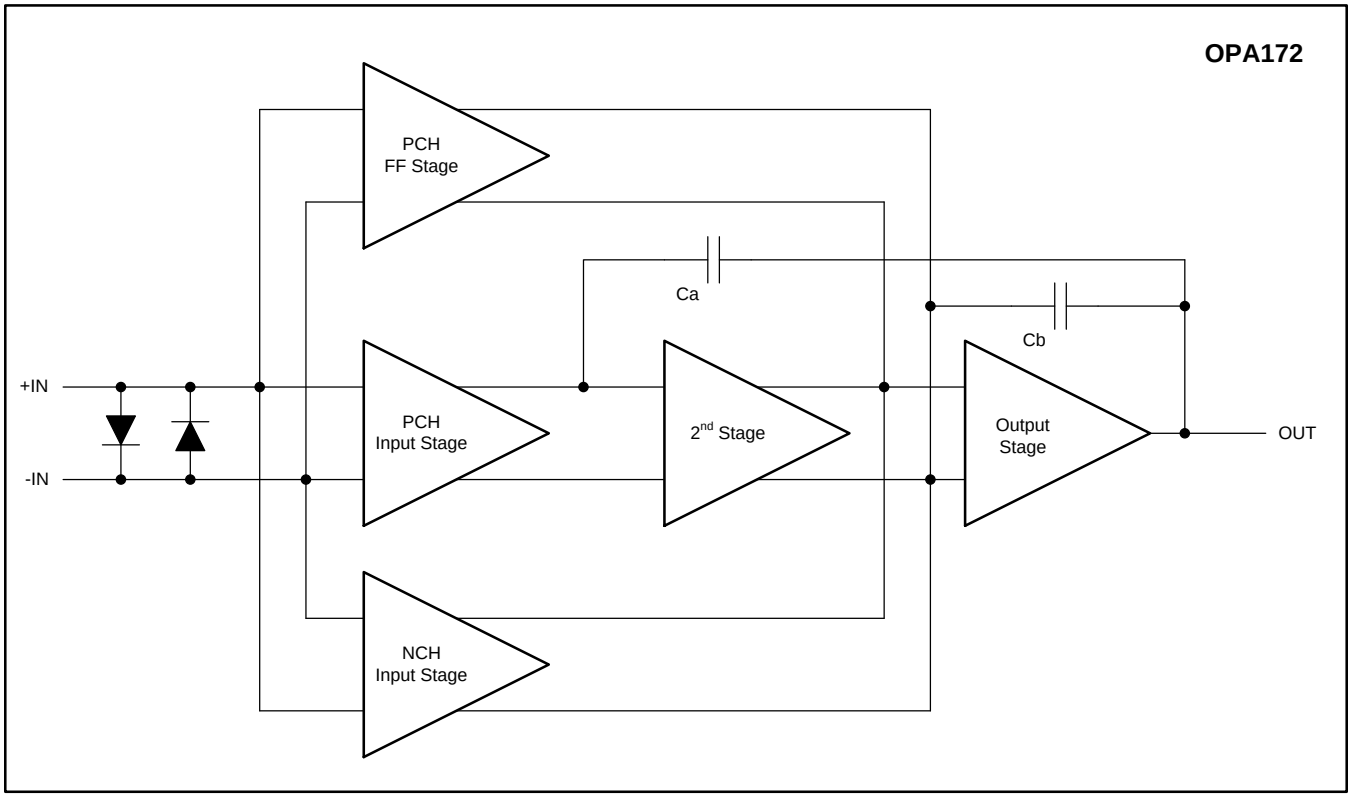
8 Detailed Description

8.1 Overview

The OPAx172 family of operational amplifiers provide high overall performance, making them ideal for many general-purpose applications. The excellent offset drift of only 1.5 µV/°C (max) provides excellent stability over the entire temperature range. In addition, the device offers very good overall performance with high CMRR, PSRR, A_{OL}, and superior THD.

The *Functional Block Diagram* section shows the simplified diagram of the OPA172 design. The design topology is a highly-optimized, three-stage amplifier with an active-feedforward gain stage.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 EMI Rejection

The OPAx172 uses integrated electromagnetic interference (EMI) filtering to reduce the effects of EMI from sources such as wireless communications and densely-populated boards with a mix of analog signal chain and digital components. EMI immunity can be improved with circuit design techniques; the OPAx172 benefits from these design improvements. Texas Instruments has developed the ability to accurately measure and quantify the immunity of an operational amplifier over a broad frequency spectrum extending from 10 MHz to 6 GHz. 图 42 shows the results of this testing on the OPAx172. 表 2 shows the EMIRR IN+ values for the OPAx172 at particular frequencies commonly encountered in real-world applications. Applications listed in 表 2 can be centered on or operated near the particular frequency shown. Detailed information can also be found in Application Report SBOA128, *EMI Rejection Ratio of Operational Amplifiers*, available for download from www.ti.com.

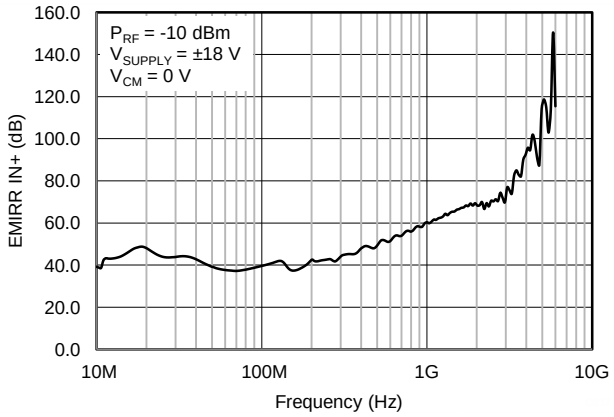


图 42. EMIRR Testing

表 2. OPAx172 EMIRR IN+ for Frequencies of Interest

FREQUENCY	APPLICATION OR ALLOCATION	EMIRR IN+
400 MHz	Mobile radio, mobile satellite, space operation, weather, radar, ultrahigh frequency (UHF) applications	47.6 dB
900 MHz	Global system for mobile communications (GSM) applications, radio communication, navigation, GPS (to 1.6 GHz), GSM, aeronautical mobile, UHF applications	58.5 dB
1.8 GHz	GSM applications, mobile personal communications, broadband, satellite, L-band (1 GHz to 2 GHz)	68 dB
2.4 GHz	802.11b, 802.11g, 802.11n, Bluetooth®, mobile personal communications, industrial, scientific and medical (ISM) radio band, amateur radio and satellite, S-band (2 GHz to 4 GHz)	69.2 dB
3.6 GHz	Radiolocation, aero communication and navigation, satellite, mobile, S-band	82.9 dB
5.0 GHz	802.11a, 802.11n, aero communication and navigation, mobile communication, space and satellite operation, C-band (4 GHz to 8 GHz)	114 dB

8.3.2 Phase-Reversal Protection

The OPAx172 family has internal phase-reversal protection. Many op amps exhibit a phase reversal when the input is driven beyond the linear common-mode range. This condition is most often encountered in noninverting circuits when the input is driven beyond the specified common-mode voltage range, causing the output to reverse into the opposite rail. The input of the OPAx172 prevents phase reversal with excessive common-mode voltage. Instead, the appropriate rail limits the output voltage. This performance is shown in 图 43.

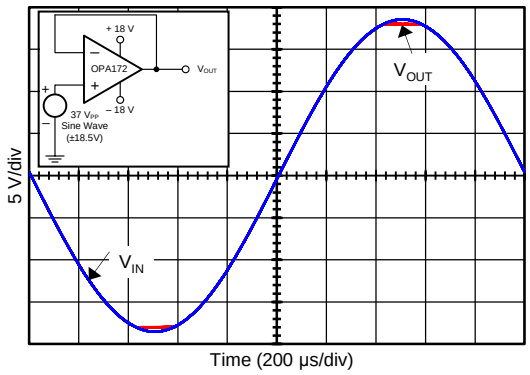


图 43. No Phase Reversal

8.3.3 Capacitive Load and Stability

The dynamic characteristics of the OPAx172 are optimized for commonly-used operating conditions. The combination of low closed-loop gain and high capacitive loads decreases the phase margin of the amplifier and may lead to gain peaking or oscillations. As a result, heavier capacitive loads must be isolated from the output. The simplest way to achieve this isolation is to add a small resistor (for example, R_{OUT} = 50 Ω) in series with the output. 图 44 and 图 45 show graphs of small-signal overshoot versus capacitive load for several values of R_{OUT}. Refer to Application Bulletin SBOA015 (AB-028), *Feedback Plots Define Op Amp AC Performance*, available for download from www.ti.com, for details of analysis techniques and application circuits.

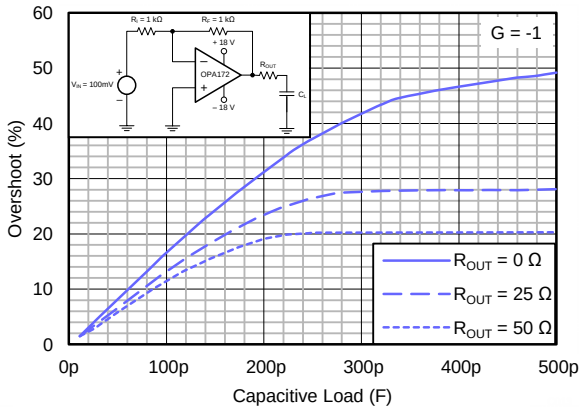


图 44. Small-Signal Overshoot vs Capacitive Load (100-mV Output Step)

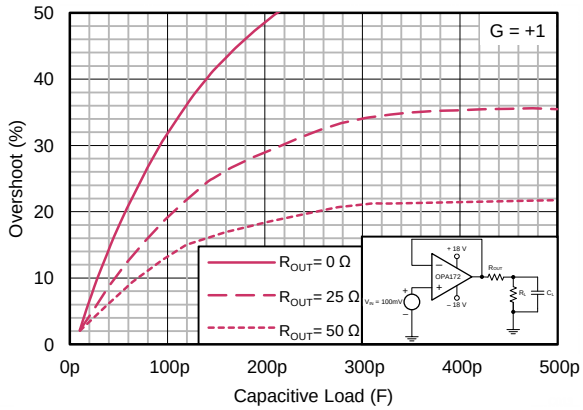


图 45. Small-Signal Overshoot vs Capacitive Load (100-mV Output Step)

8.4 Device Functional Modes

8.4.1 Common-Mode Voltage Range

The input common-mode voltage range of the OPAx172 series extends 100 mV below the negative rail and within 2 V of the top rail for normal operation.

This device can operate with full rail-to-rail input 100 mV beyond the top rail, but with reduced performance within 2 V of the top rail. The typical performance in this range is summarized in 表 3.

表 3. Typical Performance Range (V_S = ±18 V)

PARAMETER	MIN	TYP	MAX	UNIT
Input Common-Mode Voltage	(V+) – 2		(V+) + 0.1	V
Offset voltage		5		mV
Offset voltage vs temperature (T_A = –40°C to +125°C)		10		µV/°C
Common-mode rejection		70		dB
Open-loop gain		60		dB
Gain bandwidth product (GBP)		4		MHz
Slew rate		4		V/µs
Noise at f = 1 kHz		22		nV/√Hz

8.4.2 Electrical Overstress

Designers often ask questions about the capability of an operational amplifier to withstand electrical overstress. These questions tend to focus on the device inputs, but may involve the supply voltage terminals or even the output terminal. Each of these different terminal functions have electrical stress limits determined by the voltage breakdown characteristics of the particular semiconductor fabrication process and specific circuits connected to the terminal. Additionally, internal electrostatic discharge (ESD) protection is built into these circuits to protect them from accidental ESD events both before and during product assembly.

A good understanding of this basic ESD circuitry and its relevance to an electrical overstress event is helpful. 图 46 illustrates the ESD circuits contained in the OPAx172 (indicated by the dashed line area). The ESD protection circuitry involves several current-steering diodes connected from the input and output terminals and routed back to the internal power-supply lines, where the diodes meet at an absorption device internal to the operational amplifier. This protection circuitry is intended to remain inactive during normal circuit operation.

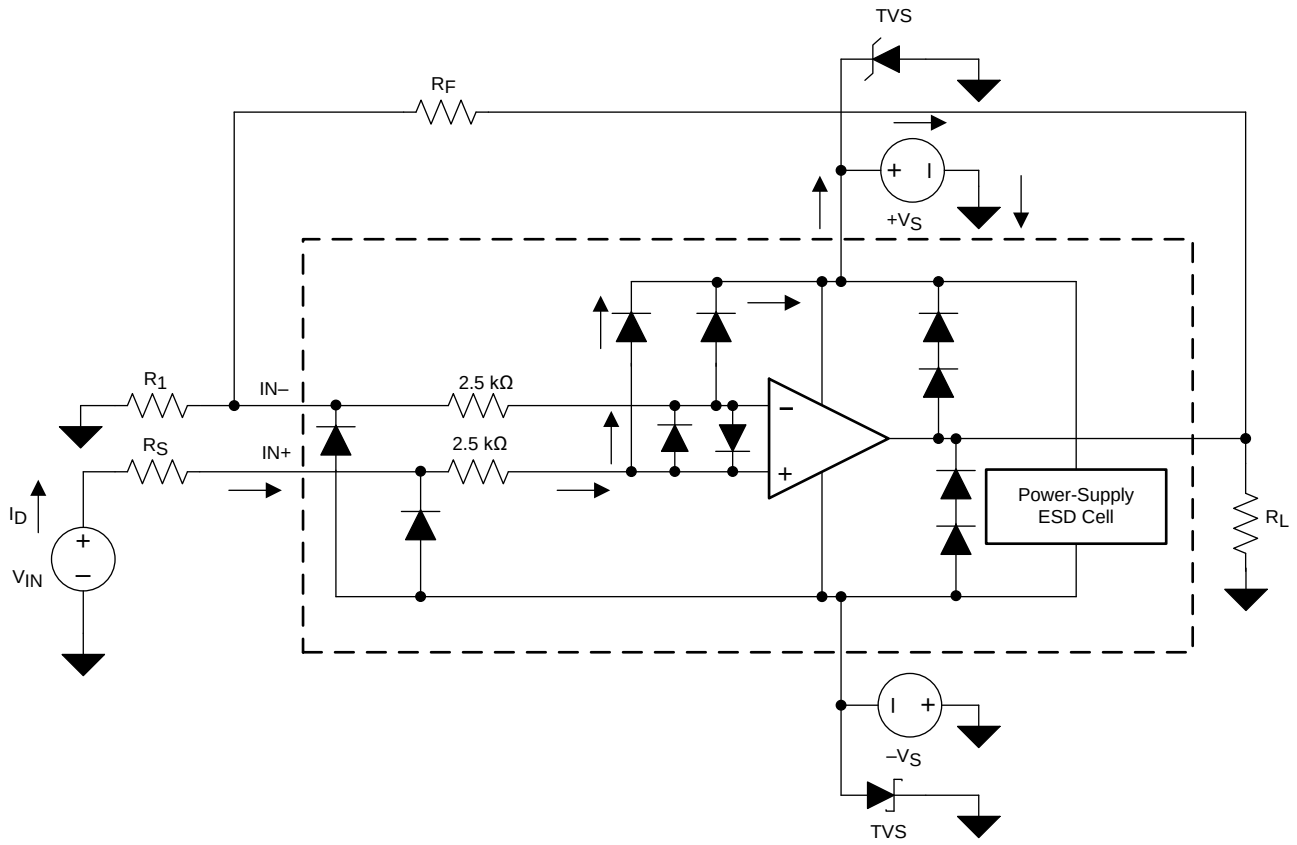


图 46. Equivalent Internal ESD Circuitry Relative to a Typical Circuit Application

An ESD event produces a short-duration, high-voltage pulse that is transformed into a short-duration, high-current pulse while discharging through a semiconductor device. The ESD protection circuits are designed to provide a current path around the operational amplifier core to prevent damage. The energy absorbed by the protection circuitry is then dissipated as heat.

When an ESD voltage develops across two or more amplifier device terminals, current flows through one or more steering diodes. Depending on the path that the current takes, the absorption device may activate. The absorption device has a trigger, or threshold voltage, that is above the normal operating voltage of the OPAx172 but below the device breakdown voltage level. When this threshold is exceeded, the absorption device quickly activates and clamps the voltage across the supply rails to a safe level.

When the operational amplifier connects into a circuit (as shown in 图 46), the ESD protection components are intended to remain inactive and do not become involved in the application circuit operation. However, circumstances may arise where an applied voltage exceeds the operating voltage range of a given terminal. If this condition occurs, there is a risk that some internal ESD protection circuits can turn on and conduct current. Any such current flow occurs through steering-diode paths and rarely involves the absorption device.

图 46 shows a specific example where the input voltage (V_{IN}) exceeds the positive supply voltage ($+V_S$) by 500 mV or more. Much of what happens in the circuit depends on the supply characteristics. If $+V_S$ can sink the current, one of the upper input steering diodes conducts and directs current to $+V_S$. Excessively high current levels can flow with increasingly higher V_{IN}. As a result, the data sheet specifications recommend that applications limit the input current to 10 mA.

If the supply is not capable of sinking the current, V_{IN} can begin sourcing current to the operational amplifier, and then take over as the source of positive supply voltage. The danger in this case is that the voltage can rise to levels that exceed the operational amplifier absolute maximum ratings.

Another common question involves what happens to the amplifier if an input signal is applied to the input while the power supplies $+V_S$ or $–V_S$ are at 0 V. Again, this question depends on the supply characteristic while at 0 V, or at a level below the input-signal amplitude. If the supplies appear as high impedance, then the input source supplies the operational amplifier current through the current-steering diodes. This state is not a normal bias condition; most likely, the amplifier will not operate normally. If the supplies are low impedance, then the current through the steering diodes can become quite high. The current level depends on the ability of the input source to deliver current, and any resistance in the input path.

If there is any uncertainty about the ability of the supply to absorb this current, add external zener diodes to the supply terminals; see 图 46. Select the zener voltage so that the diode does not turn on during normal operation. However, the zener voltage must be low enough so that the zener diode conducts if the supply terminal begins to rise above the safe-operating, supply-voltage level.

The OPAx172 input terminals are protected from excessive differential voltage with back-to-back diodes; see 图 46. In most circuit applications, the input protection circuitry has no effect. However, in low-gain or G = 1 circuits, fast-ramping input signals can forward-bias these diodes because the output of the amplifier cannot respond rapidly enough to the input ramp. If the input signal is fast enough to create this forward-bias condition, limit the input signal current to 10 mA or less. If the input signal current is not inherently limited, an input series resistor can be used to limit the input signal current. This input series resistor degrades the low-noise performance of the OPAx172. 图 46 illustrates an example configuration that implements a current-limiting feedback resistor.

8.4.3 Overload Recovery

Overload recovery is defined as the time it takes for the op amp output to recover from the saturated state to the linear state. The output devices of the op amp enter the saturation region when the output voltage exceeds the rated operating voltage, either due to the high input voltage or the high gain. After the device enters the saturation region, the charge carriers in the output devices need time to return back to the normal state. After the charge carriers return back to the equilibrium state, the device begins to slew at the normal slew rate. Thus, the propagation delay in case of an overload condition is the sum of the overload recovery time and the slew time. The overload recovery time for the OPAx172 is approximately 200 ns.

9 Applications and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The OPAx172 family of amplifiers is specified for operation from 4.5 V to 36 V (±2.25 V to ±18 V). Many of the specifications apply from –40°C to +125°C. Parameters that can exhibit significant variance with regard to operating voltage or temperature are presented in the *Typical Characteristics*.

9.2 Typical Applications

The following application examples highlight only a few of the circuits where the OPAx172 can be used.

9.2.1 Capacitive Load Drive Solution Using an Isolation Resistor

The OPA172 can be used capacitive loads such as cable shields, reference buffers, MOSFET gates, and diodes. The circuit uses an isolation resistor (R_{ISO}) to stabilize the output of an op amp. R_{ISO} modifies the open-loop gain of the system to ensure the circuit has sufficient phase margin.

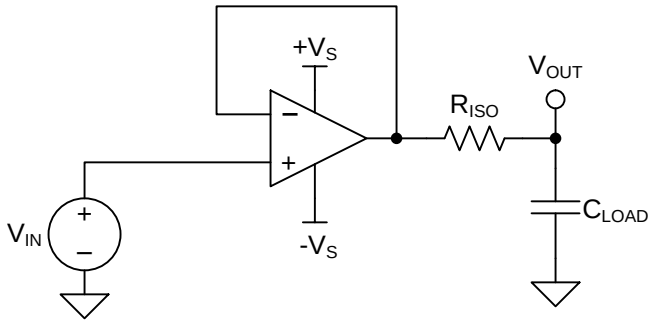


图 47. Unity-Gain Buffer with R_{ISO} Stability Compensation

9.2.1.1 Design Requirements

The design requirements are:

- Supply voltage: 30 V (±15 V)
- Capacitive loads: 100 pF, 1000 pF, 0.01 μF, 0.1 μF, and 1 μF
- Phase margin: 45° and 60°

Typical Applications (接下页)

9.2.1.2 Detailed Design Procedure

图 47 depicts a unity-gain buffer driving a capacitive load. 公式 1 shows the transfer function for the circuit in 图 47. Not depicted in 图 47 is the open-loop output resistance of the op amp, R_o.

$$T(s) = \frac{1 + C_{LOAD} \times R_{ISO} \times s}{1 + (R_o + R_{ISO}) \times C_{LOAD} \times s} \quad (1)$$

The transfer function in 公式 1 has a pole and a zero. The frequency of the pole (f_p) is determined by (R_o + R_{ISO}) and C_{LOAD}. Components R_{ISO} and C_{LOAD} determine the frequency of the zero (f_z). A stable system is obtained by selecting R_{ISO} such that the rate of closure (ROC) between the open-loop gain (A_{OL}) and 1 / β is 20 dB per decade. 图 48 shows the concept. Note that the 1 / β curve for a unity-gain buffer is 0 dB.

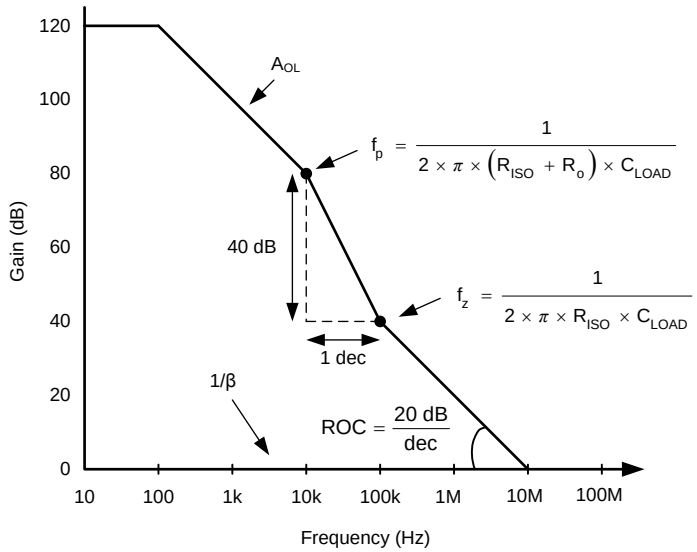


图 48. Unity-Gain Amplifier with R_{ISO} Compensation

ROC stability analysis is typically simulated. The validity of the analysis depends on multiple factors, especially the accurate modeling of R_o. In addition to simulating the ROC, a robust stability analysis includes a measurement of overshoot percentage and ac gain peaking of the circuit using a function generator, oscilloscope, and gain and phase analyzer. Phase margin is then calculated from these measurements. 表 4 shows the overshoot percentage and ac gain peaking that correspond to phase margins of 45° and 60°. For more details on this design and other alternative devices that can be used in place of the OPA172, refer to the precision design, *Capacitive Load Drive Solution using an Isolation Resistor* (TIPD128).

表 4. Phase Margin versus Overshoot and AC Gain Peaking

PHASE MARGIN	OVERSHOOT	AC GAIN PEAKING
45°	23.3%	2.35 dB
60°	8.8%	0.28 dB

9.2.1.3 Application Curve

The OPA172 meets the supply voltage requirements of 30 V. The OPA172 is tested for various capacitive loads and R_{ISO} is adjusted to get an overshoot corresponding to 表 4. The results of the these tests are summarized in 图 49.

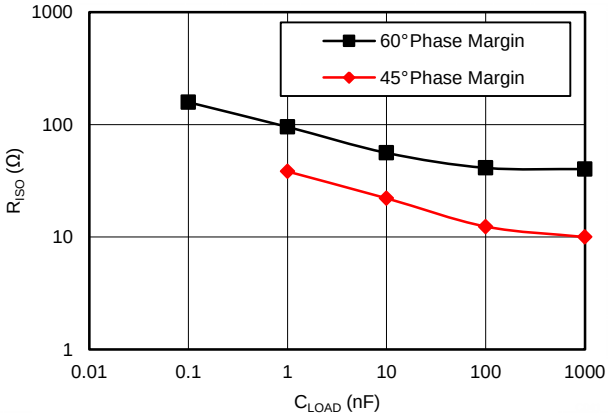


图 49. R_{ISO} vs C_{LOAD}

9.2.2 Bidirectional Current Source

The improved Howland current-pump topology shown in 图 50 provides excellent performance because of the extremely tight tolerances of the on-chip resistors of the INA132. By buffering the output using an OPA172, the output current the circuit is able to deliver is greatly extended.

The circuit dc transfer function is shown in 公式 2:

$$I_{OUT} = V_{IN} / R1 \quad (2)$$

The OPA172 can also be used as the feedback amplifier because the low bias current minimizes error voltages produced across R1. However, for improved performance, select a FET-input device with extremely low offset, such as the OPA192, OPA140, or OPA188 as the feedback amplifier.

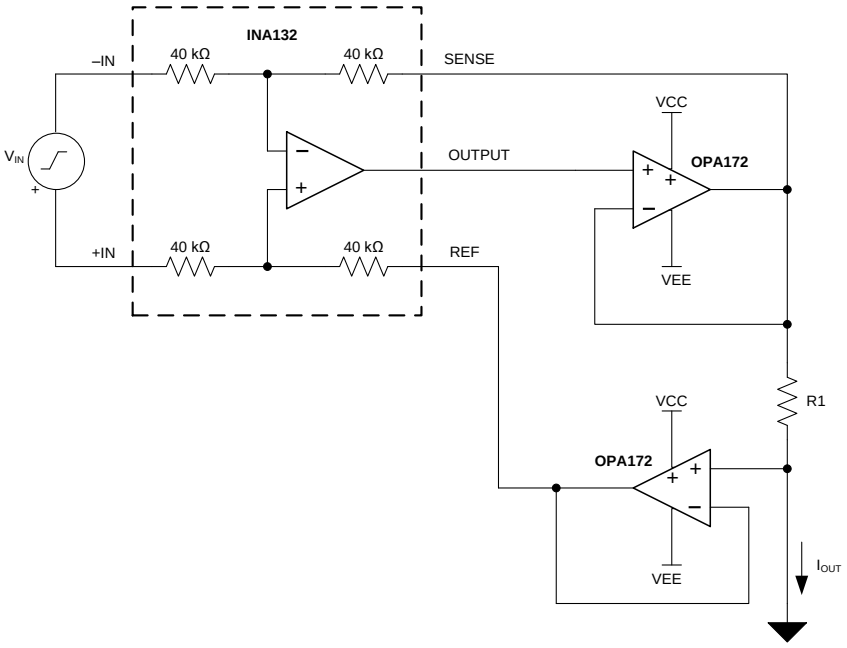


图 50. Bidirectional Current Source

9.2.3 JFET-Input Low-Noise Amplifier

图 51 shows a low-noise composite amplifier built by adding a low noise JFET pair (Q1 and Q2) as an input preamplifier for the OPA172. Transistors Q3 and Q4 form a 2-mA current sink that biases each JFET with 1 mA of drain current. Using 3.9-kΩ drain resistors produces a gain of approximately 10 in the input amplifier, making the extremely-low, broadband-noise spectral density of the JFET pair, Q1 and Q2, the dominant noise source of the amplifier. The output impedance of the input differential amplifier is large enough that a FET-input amplifier such as the OPA172 provides superior noise performance over bipolar-input amplifiers.

The gain of the composite amplifier is given by 公式 3:

$$A_V = (1 + R3 / R4) \quad (3)$$

The resistances shown are standard 1% resistor values that produce a gain of approximately 100 (99.26) with 68° of phase margin. Gains less than 10 may require additional compensation methods to provide stability. Select low resistor values to minimize the resistor thermal noise contribution to the total output noise.

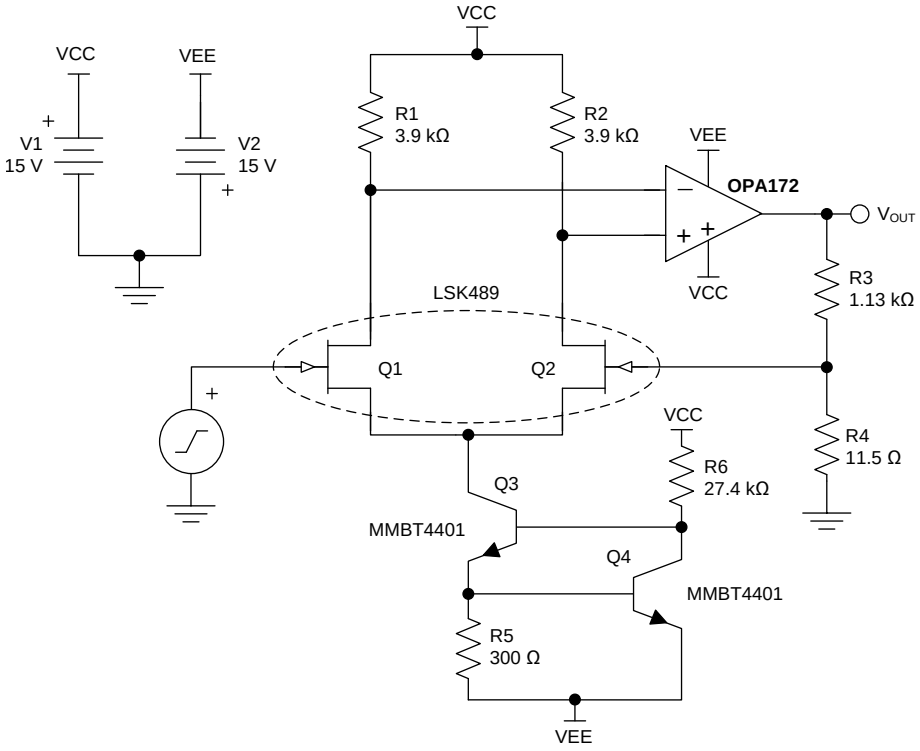


图 51. JFET-Input Low-Noise Amplifier

10 Power-Supply Recommendations

The OPA172 is specified for operation from 4.5 V to 36 V (±2.25 V to ±18 V); many specifications apply from –40°C to +125°C. Parameters that can exhibit significant variance with regard to operating voltage or temperature are presented in the *Typical Characteristics*.

CAUTION

Supply voltages larger than 40 V can permanently damage the device; see the *Absolute Maximum Ratings*.

Place 0.1-μF bypass capacitors close to the power-supply terminals to reduce errors coupling in from noisy or high-impedance power supplies. For more detailed information on bypass capacitor placement, see the *Layout* section.

11 Layout

11.1 Layout Guidelines

For best operational performance of the device, use good printed circuit board (PCB) layout practices, including:

- Noise can propagate into analog circuitry through the power pins of the circuit as a whole and op amp itself. Bypass capacitors are used to reduce the coupled noise by providing low-impedance power sources local to the analog circuitry.
  - Connect low-ESR, 0.1-µF ceramic bypass capacitors between each supply pin and ground, placed as close to the device as possible. A single bypass capacitor from V+ to ground is applicable for single-supply applications.
- Separate grounding for analog and digital portions of circuitry is one of the simplest and most-effective methods of noise suppression. One or more layers on multilayer PCBs are usually devoted to ground planes. A ground plane helps distribute heat and reduces EMI noise pickup. Make sure to physically separate digital and analog grounds paying attention to the flow of the ground current. For more detailed information refer to SLOA089, *Circuit Board Layout Techniques*.
- In order to reduce parasitic coupling, run the input traces as far away from the supply or output traces as possible. If these traces cannot be kept separate, crossing the sensitive trace perpendicular as opposed to in parallel with the noisy trace is preferable.
- Place the external components as close to the device as possible. As shown in 图 52, keeping RF and RG close to the inverting input minimizes parasitic capacitance.
- Keep the length of input traces as short as possible. Always remember that the input traces are the most sensitive part of the circuit.
- Consider a driven, low-impedance guard ring around the critical traces. A guard ring can significantly reduce leakage currents from nearby traces that are at different potentials.

11.2 Layout Example

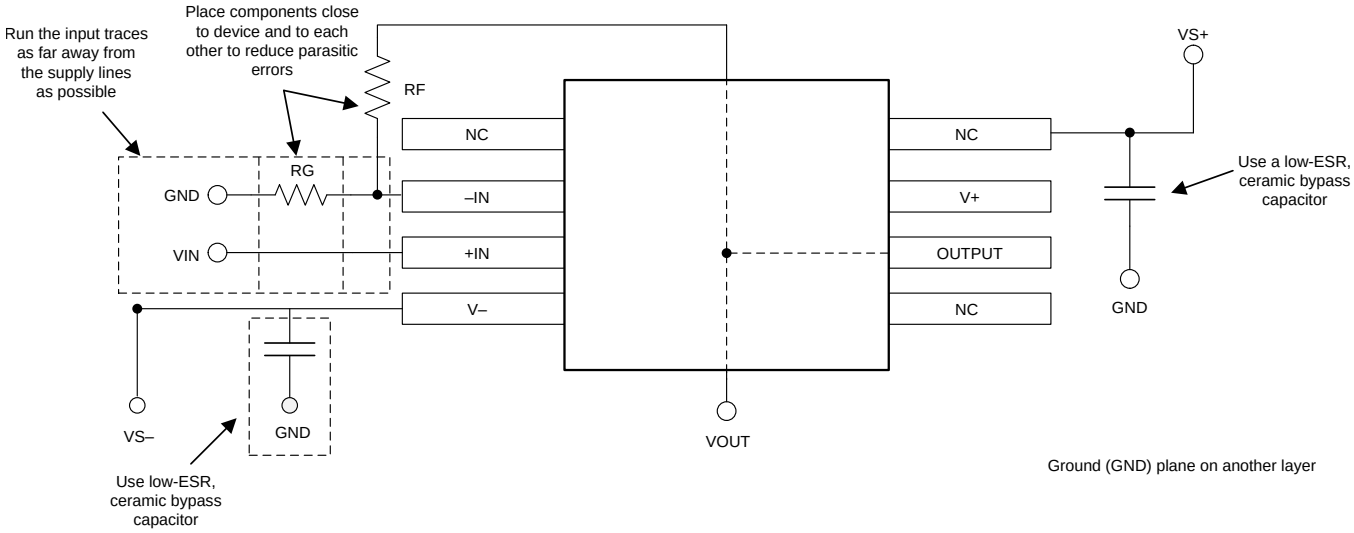


图 52. Operational Amplifier Board Layout for Noninverting Configuration

12 器件和文档支持

12.1 器件支持

12.1.1 开发支持

12.1.1.1 TINA-TI™（免费软件下载）

TINA™是一款简单、功能强大且易于使用的电路仿真程序，此程序基于 SPICE 引擎。TINA-TI 是 TINA 软件的一款免费全功能版本，除了一系列无源和有源模型外，此版本软件还预先载入了一个宏模型库。TINA-TI 提供所有传统的 SPICE 直流、瞬态和频域分析，以及其他设计功能。

TINA-TI 可从 Analog eLab Design Center（模拟电子实验室设计中心）免费下载，它提供全面的后续处理能力，使得用户能够以多种方式形成结果。虚拟仪器提供选择输入波形和探测电路节点、电压和波形的功能，从而创建一个动态的快速入门工具。

注

这些文件需要安装 TINA 软件（由 DesignSoft™提供）或者 TINA-TI 软件。请从 TINA-TI 文件夹 中下载免费的 TINA-TI 软件。

12.2 文档支持

12.2.1 相关文档

SBOA015 (AB-028) — *《反馈曲线图定义运算放大器交流性能》*。

SLOA089 — *《电路板布局布线技巧》*。

SLOD006 — *《适用于所有人的运算放大器》*。

SBOA128 — *《运算放大器的电磁干扰 (EMI) 抑制比》*。

TIPD128 — *《使用隔离电阻器实现的电容负载驱动解决方案》*。

12.3 相关链接

表 5 列出了快速访问链接。类别包括技术文档、支持与社区资源、工具和软件，以及申请样片或购买产品的快速链接。

表 **5.** 相关链接

器件	产品文件夹	样片与购买	技术文档	工具与软件	支持和社区
OPA172	单击此处	单击此处	单击此处	单击此处	单击此处
OPA2172	单击此处	单击此处	单击此处	单击此处	单击此处
OPA4172	单击此处	单击此处	单击此处	单击此处	单击此处

12.4 社区资源

下列链接提供到 TI 社区资源的连接。链接的内容由各个分销商“按照原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的 《使用条款》。

TI E2E™ 在线社区 ***TI 的工程师对工程师 (E2E) 社区。*** 此社区的创建目的在于促进工程师之间的协作。在 e2e.ti.com 中，您可以咨询问题、分享知识、拓展思路并与同行工程师一道帮助解决问题。

设计支持 ***TI 参考设计支持*** 可帮助您快速查找有帮助的 E2E 论坛、设计支持工具以及技术支持的联系信息。

12.5 商标

E2E is a trademark of Texas Instruments.
TINA-TI is a trademark of Texas Instruments, Inc and DesignSoft, Inc.
Bluetooth is a registered trademark of Bluetooth SIG, Inc.
TINA, DesignSoft are trademarks of DesignSoft, Inc.
All other trademarks are the property of their respective owners.

12.6 静电放电警告

ESD 可能会损坏该集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理措施和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。 精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

12.7 术语表

SLYZ022 — *TI 术语表*。

这份术语表列出并解释术语、缩写和定义。

13 机械、封装和可订购信息

以下页面包含机械、封装和可订购信息。这些信息是指定器件的最新可用数据。数据如有变更，恕不另行通知，且不会对此文档进行修订。如需获取此产品说明书的浏览器版本，请查阅左侧的导航栏。

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
OPA172ID	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OPA172	Samples
OPA172IDBVR	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OUWQ	Samples
OPA172IDBVT	ACTIVE	SOT-23	DBV	5	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OUWQ	Samples
OPA172IDCKR	ACTIVE	SC70	DCK	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	SIU	Samples
OPA172IDCKT	ACTIVE	SC70	DCK	5	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	SIU	Samples
OPA172IDR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OPA172	Samples
OPA2172ID	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	O2172A	Samples
OPA2172IDGK	ACTIVE	VSSOP	DGK	8	80	RoHS & Green	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	OVJQ	Samples
OPA2172IDGKR	ACTIVE	VSSOP	DGK	8	2500	RoHS & Green	NIPDAUAG | SN	Level-2-260C-1 YEAR	-40 to 125	OVJQ	Samples
OPA2172IDR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	O2172A	Samples
OPA2172IDRGR	ACTIVE	SON	DRG	8	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OP2172	Samples
OPA2172IDRGT	ACTIVE	SON	DRG	8	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OP2172	Samples
OPA4172ID	ACTIVE	SOIC	D	14	50	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 125	OPA4172	Samples
OPA4172IDR	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 125	OPA4172	Samples
OPA4172IPW	ACTIVE	TSSOP	PW	14	90	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OPA4172	Samples
OPA4172IPWR	ACTIVE	TSSOP	PW	14	2000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OPA4172	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

OTHER QUALIFIED VERSIONS OF OPA2172, OPA4172 :

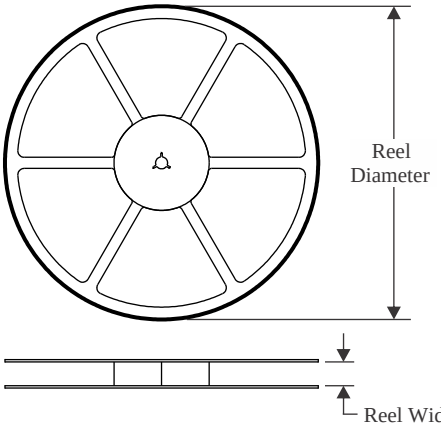
- Automotive : OPA2172-Q1, OPA4172-Q1

NOTE: Qualified Version Definitions:

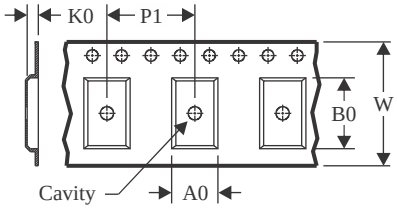
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

REEL DIMENSIONS

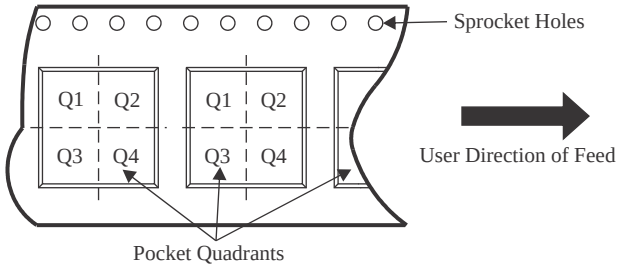


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

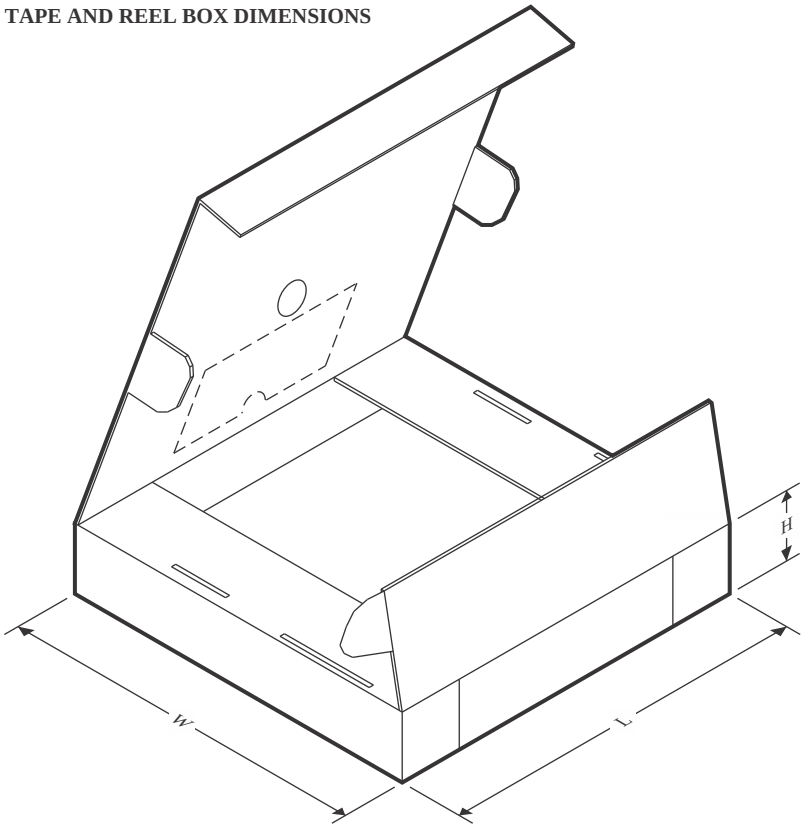
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
OPA172IDBVR	SOT-23	DBV	5	3000	180.0	8.4	3.23	3.17	1.37	4.0	8.0	Q3
OPA172IDBVT	SOT-23	DBV	5	250	180.0	8.4	3.23	3.17	1.37	4.0	8.0	Q3
OPA172IDCKR	SC70	DCK	5	3000	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
OPA172IDCKT	SC70	DCK	5	250	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
OPA172IDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
OPA2172IDGKR	VSSOP	DGK	8	2500	330.0	12.4	5.25	3.35	1.25	8.0	12.0	Q1
OPA2172IDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
OPA2172IDRGR	SON	DRG	8	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
OPA2172IDRGT	SON	DRG	8	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
OPA4172IDR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
OPA4172IPWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

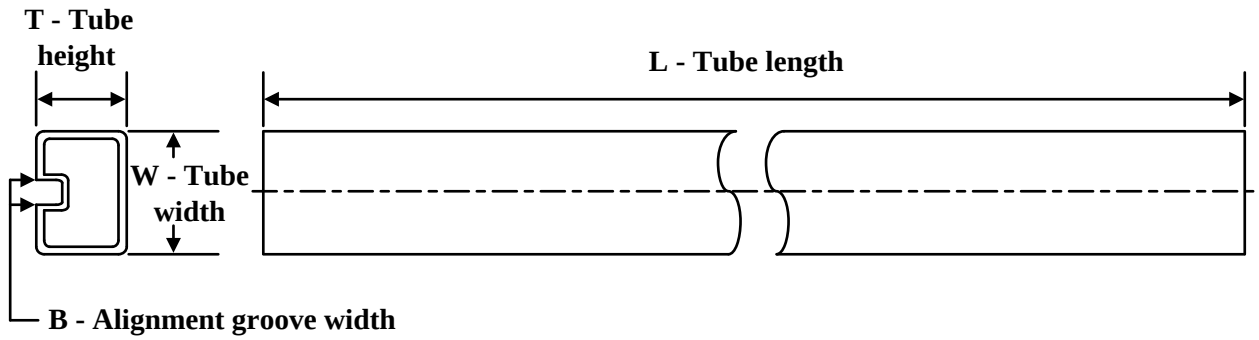
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
OPA172IDBVR	SOT-23	DBV	5	3000	223.0	270.0	35.0
OPA172IDBVT	SOT-23	DBV	5	250	223.0	270.0	35.0
OPA172IDCKR	SC70	DCK	5	3000	180.0	180.0	18.0
OPA172IDCKT	SC70	DCK	5	250	180.0	180.0	18.0
OPA172IDR	SOIC	D	8	2500	356.0	356.0	35.0
OPA2172IDGKR	VSSOP	DGK	8	2500	366.0	364.0	50.0
OPA2172IDR	SOIC	D	8	2500	356.0	356.0	35.0
OPA2172IDRGR	SON	DRG	8	3000	346.0	346.0	33.0
OPA2172IDRGT	SON	DRG	8	250	210.0	185.0	35.0
OPA4172IDR	SOIC	D	14	2500	356.0	356.0	35.0
OPA4172IPWR	TSSOP	PW	14	2000	356.0	356.0	35.0

TUBE



*All dimensions are nominal

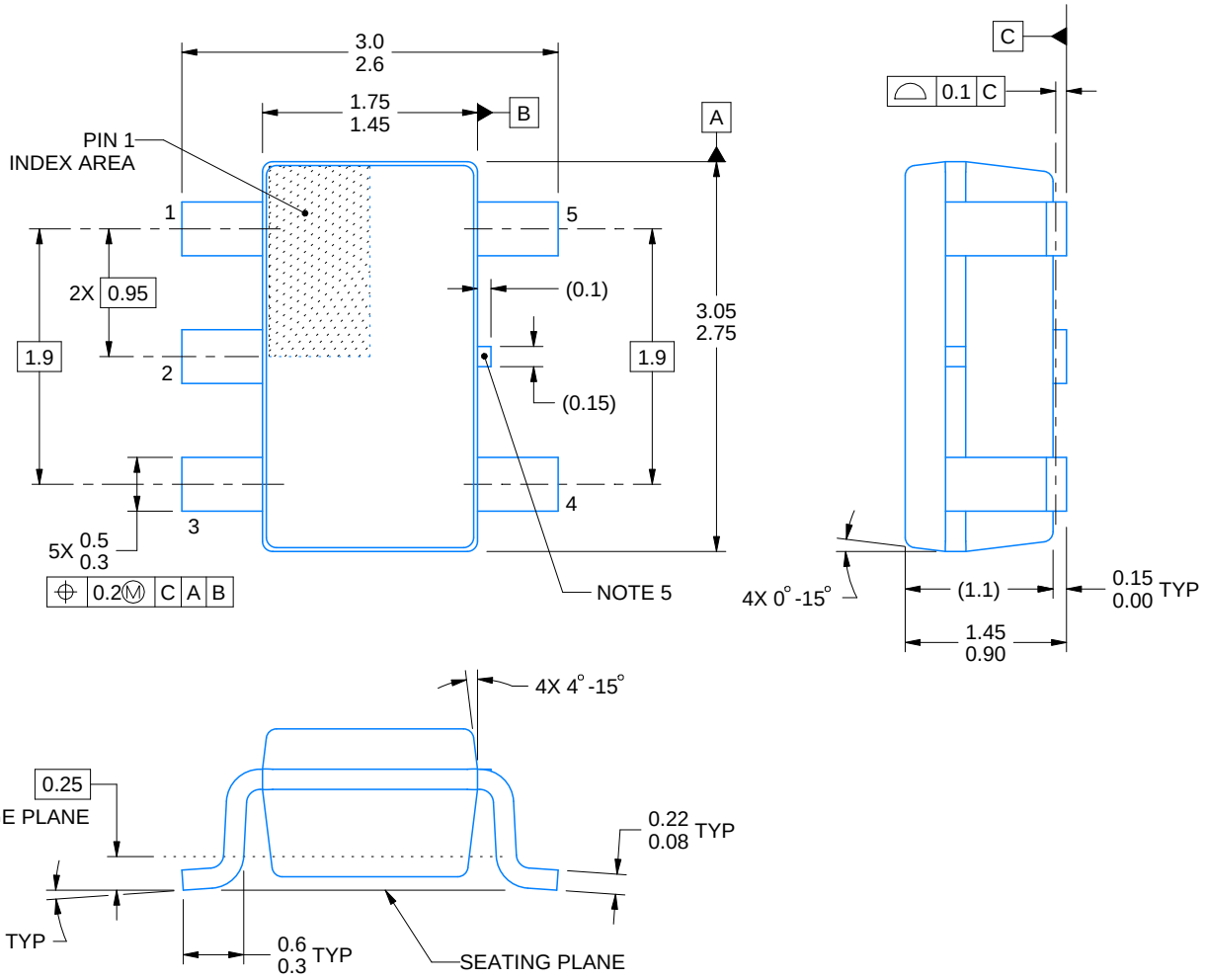
Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
OPA172ID	D	SOIC	8	75	506.6	8	3940	4.32
OPA2172ID	D	SOIC	8	75	506.6	8	3940	4.32
OPA2172IDGK	DGK	VSSOP	8	80	330	6.55	500	2.88
OPA4172ID	D	SOIC	14	50	506.6	8	3940	4.32
OPA4172IPW	PW	TSSOP	14	90	530	10.2	3600	3.5

PACKAGE OUTLINE

DBV0005A

SOT-23 - 1.45 mm max height

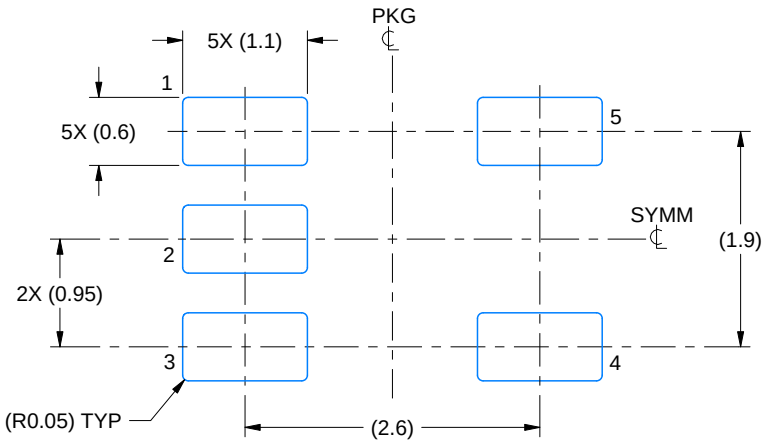
SMALL OUTLINE TRANSISTOR



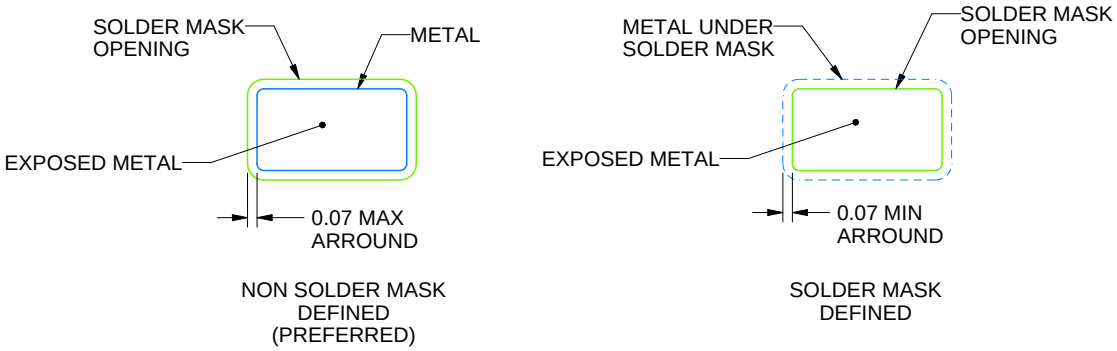
4214839/K 08/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.
5. Support pin may differ or may not be present.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

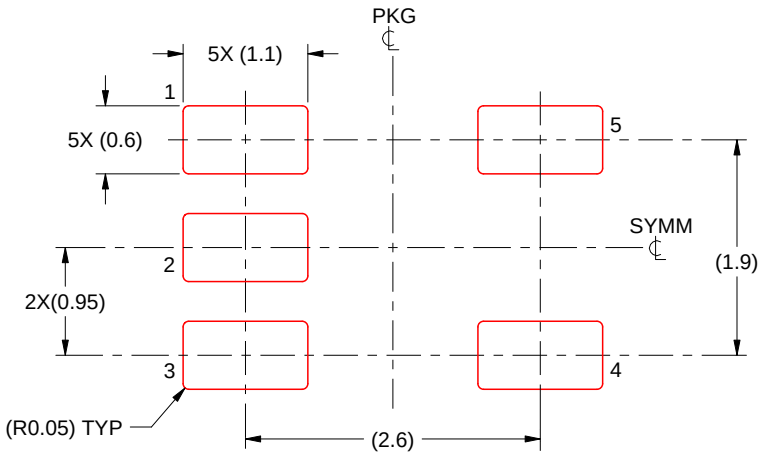


SOLDER MASK DETAILS

4214839/K 08/2024

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214839/K 08/2024

NOTES: (continued)

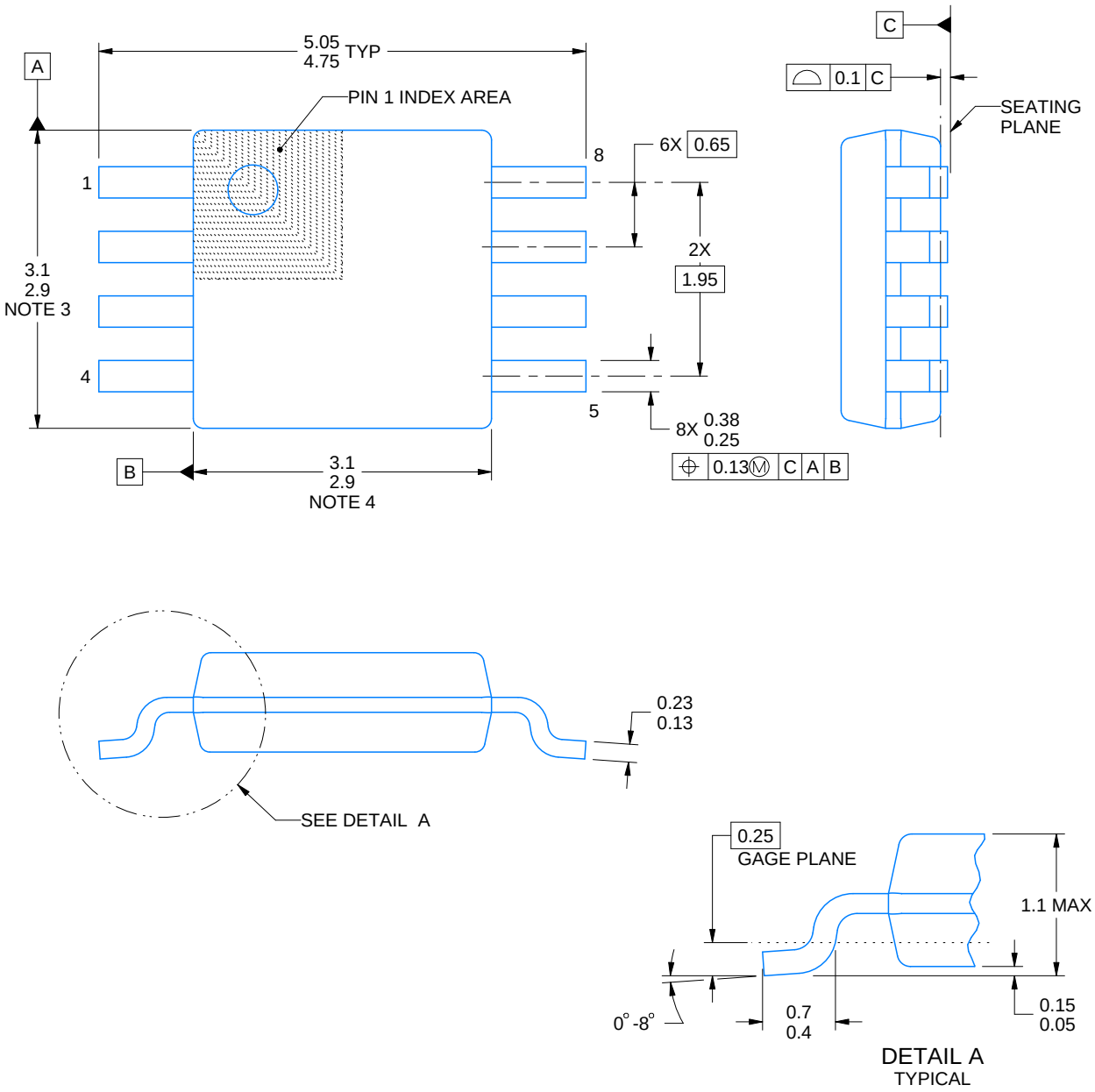
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

DGK0008A

VSSOP - 1.1 mm max height

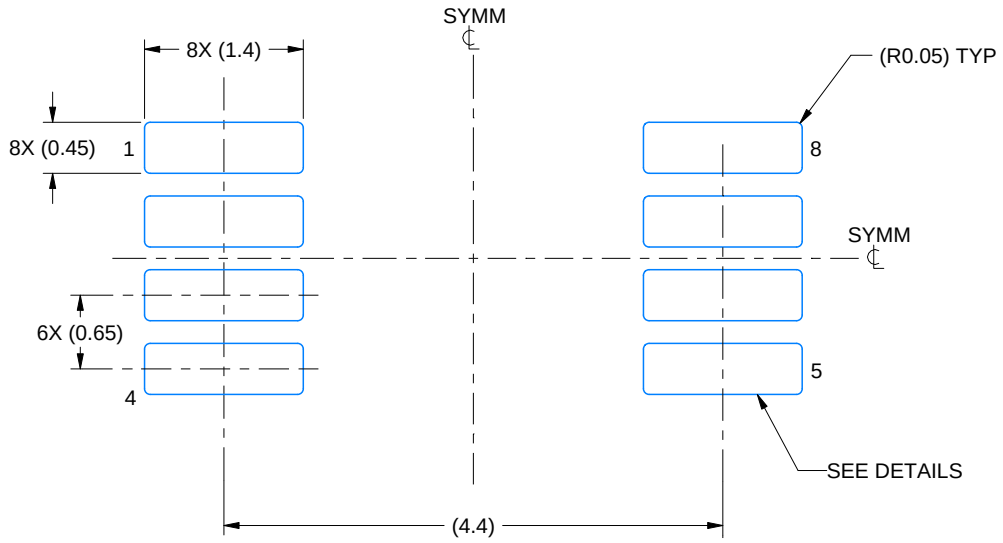
SMALL OUTLINE PACKAGE



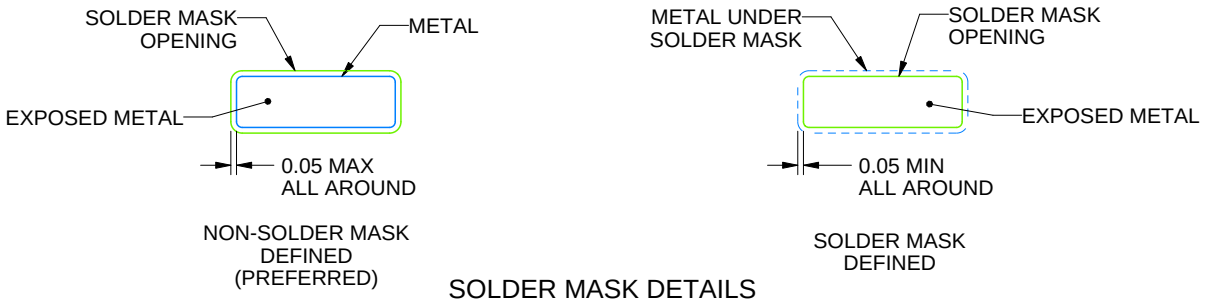
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X

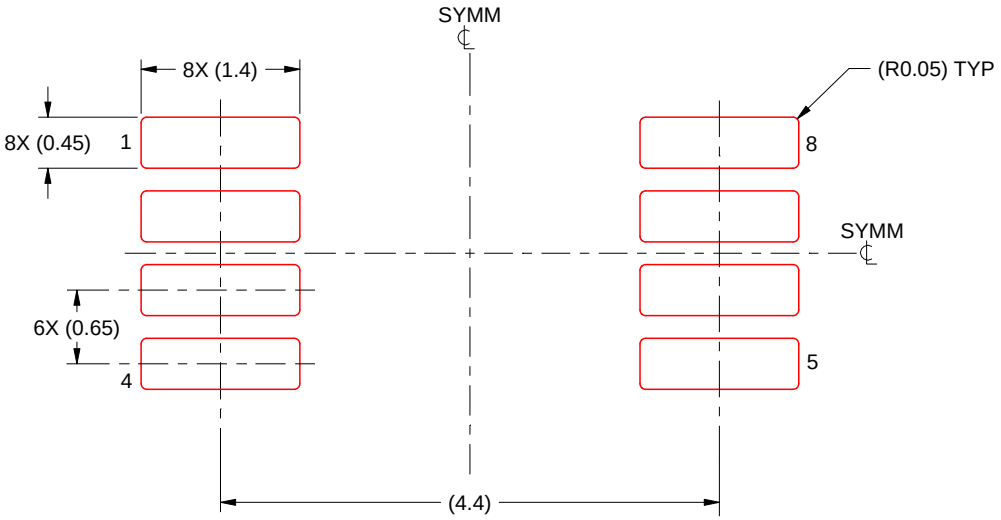


SOLDER MASK DETAILS

4214862/A 04/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.

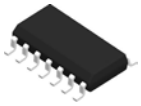


SOLDER PASTE EXAMPLE
SCALE: 15X

4214862/A 04/2023

NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

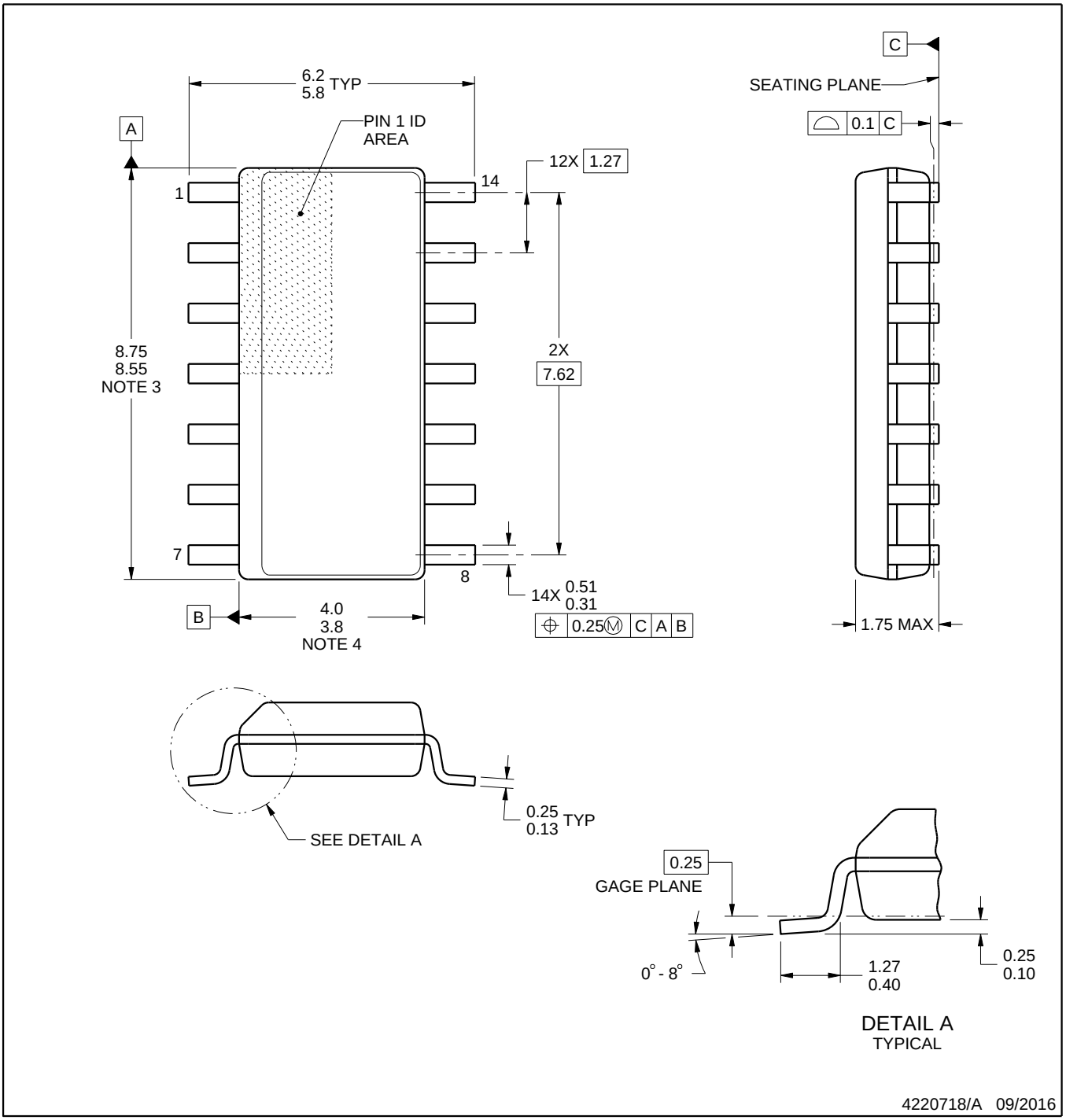


PACKAGE OUTLINE

D0014A

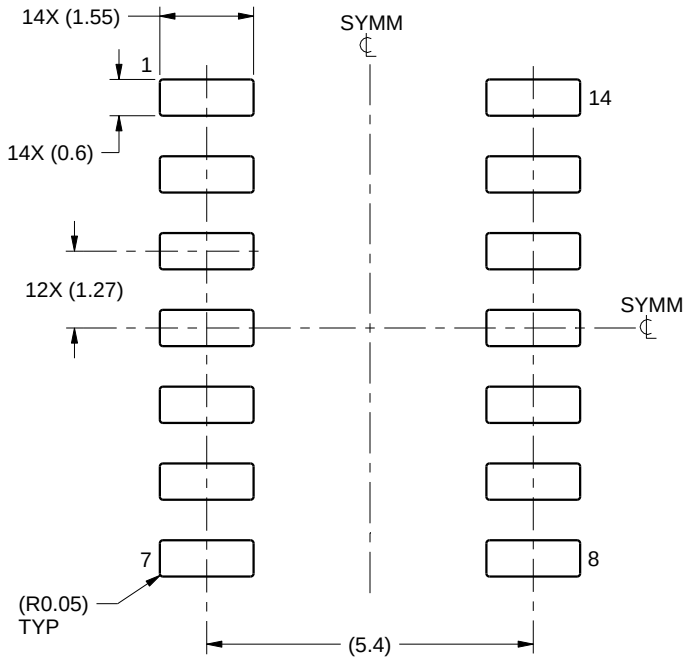
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

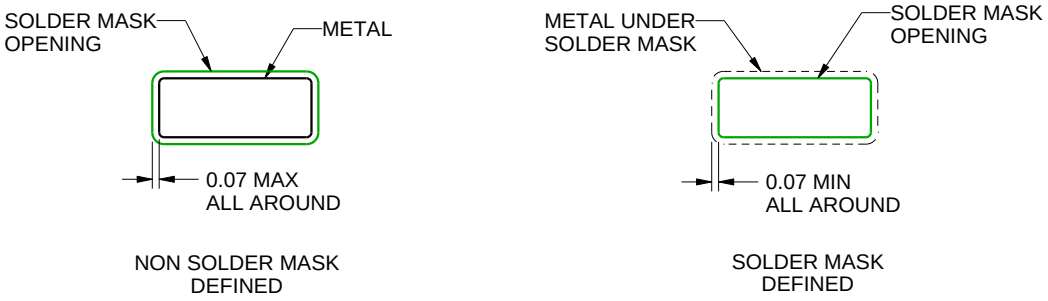


NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm, per side.
5. Reference JEDEC registration MS-012, variation AB.



LAND PATTERN EXAMPLE
SCALE:8X



SOLDER MASK DETAILS

4220718/A 09/2016

NOTES: (continued)

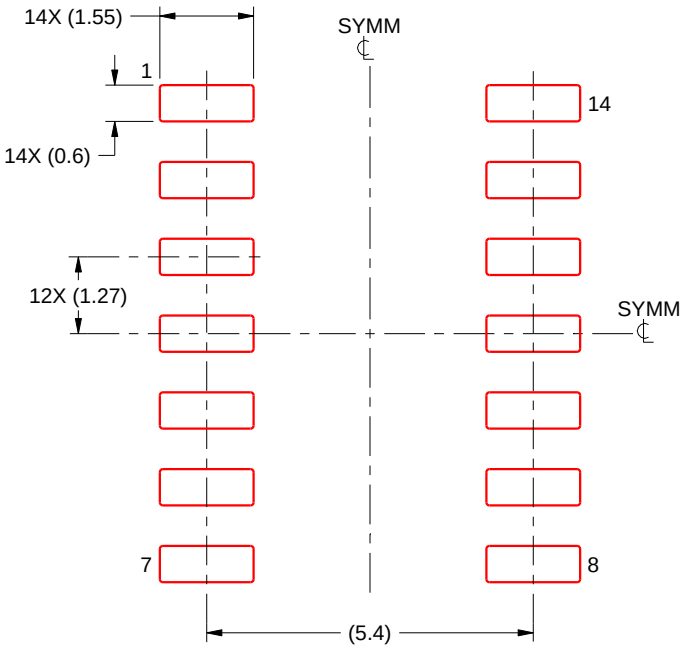
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:8X

4220718/A 09/2016

NOTES: (continued)

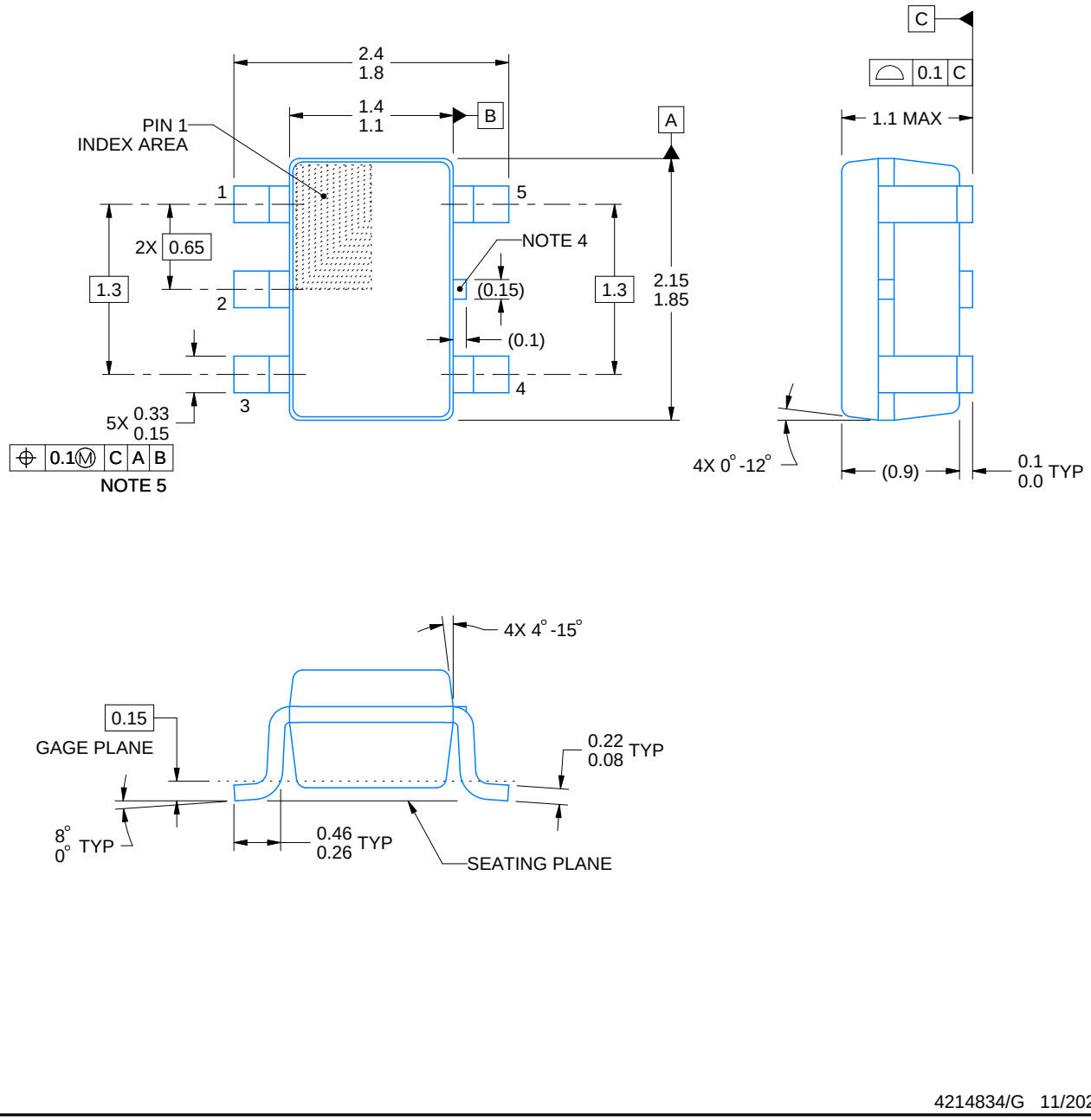
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

DCK0005A

SOT - 1.1 max height

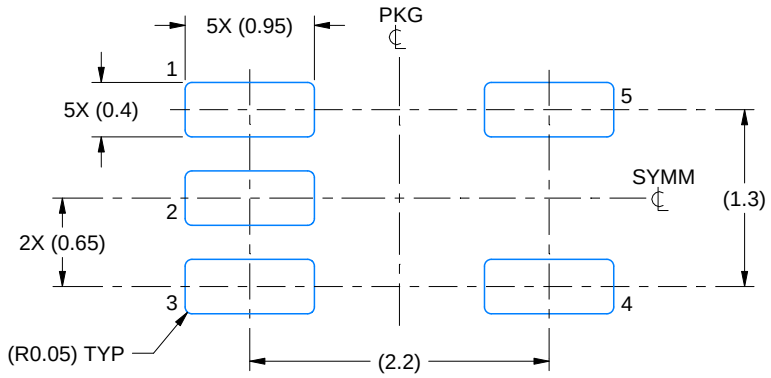
SMALL OUTLINE TRANSISTOR



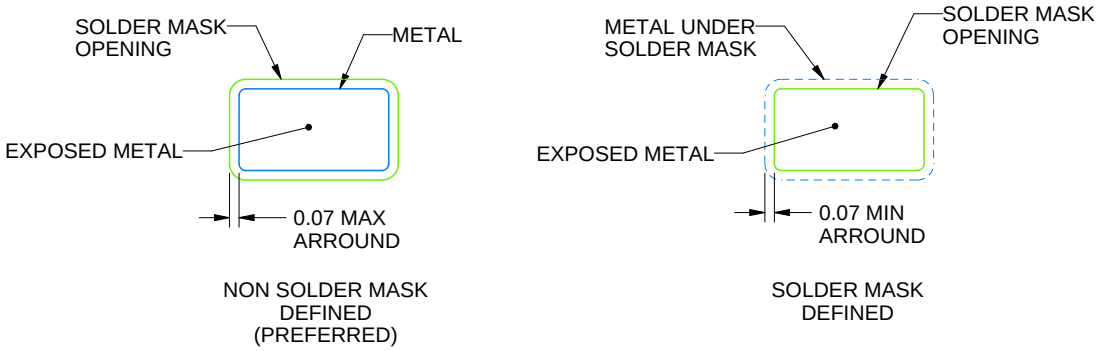
4214834/G 11/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-203.
4. Support pin may differ or may not be present.
5. Lead width does not comply with JEDEC.
6. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25mm per side



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:18X

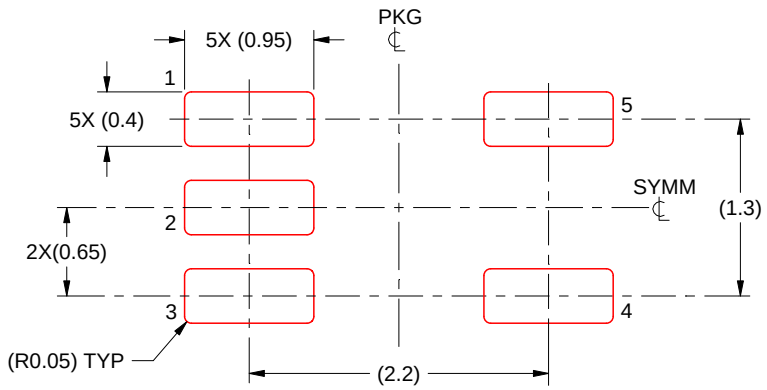


SOLDER MASK DETAILS

4214834/G 11/2024

NOTES: (continued)

7. Publication IPC-7351 may have alternate designs.
8. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

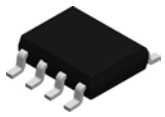


SOLDER PASTE EXAMPLE
BASED ON 0.125 THICK STENCIL
SCALE:18X

4214834/G 11/2024

NOTES: (continued)

9. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
10. Board assembly site may have different recommendations for stencil design.

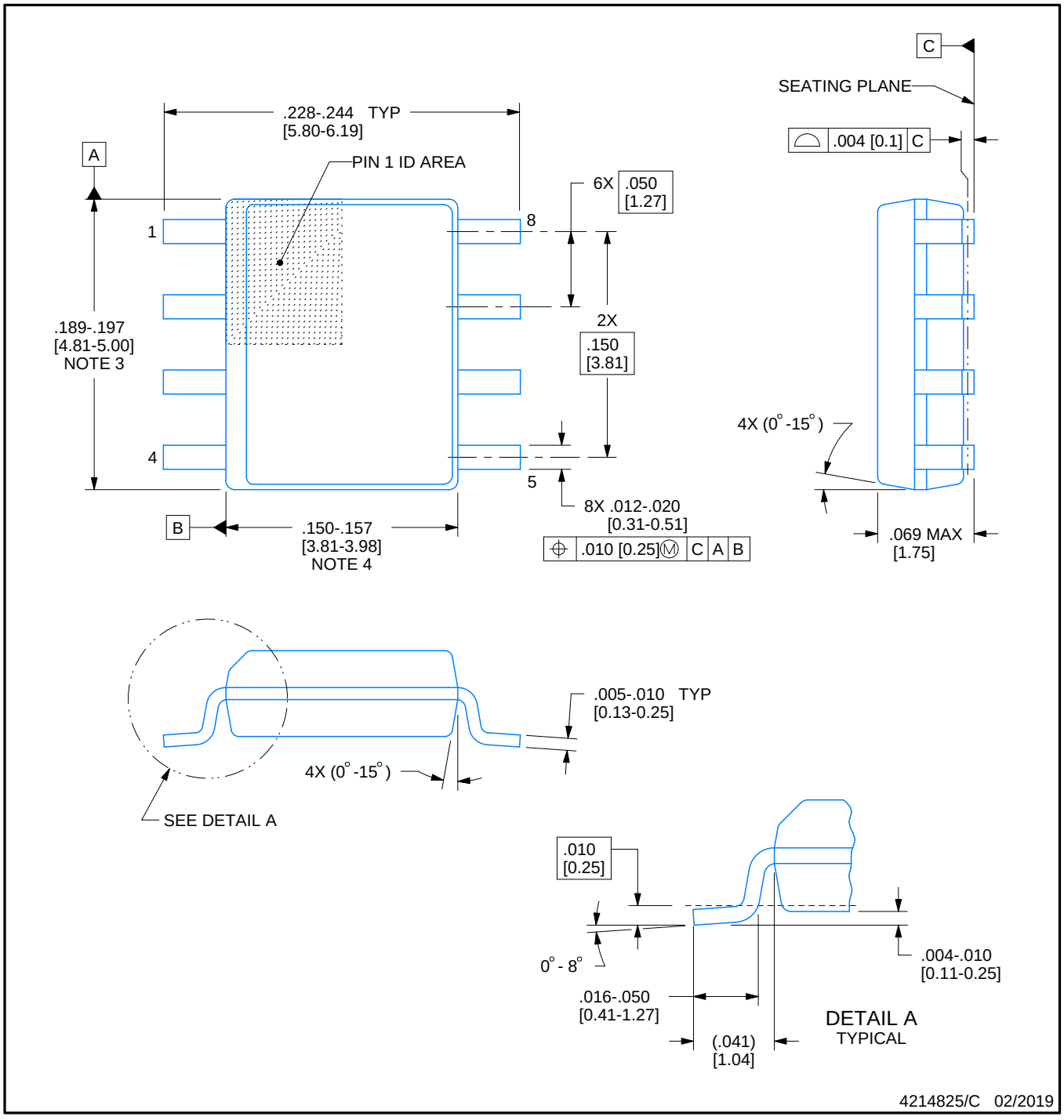


PACKAGE OUTLINE

D0008A

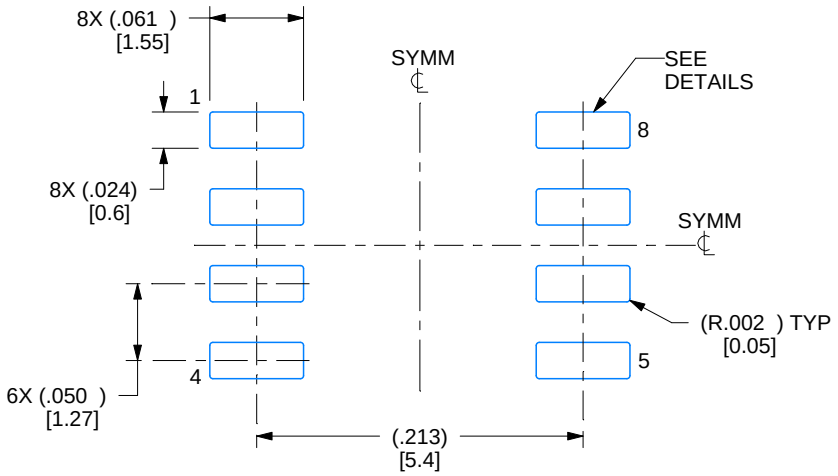
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

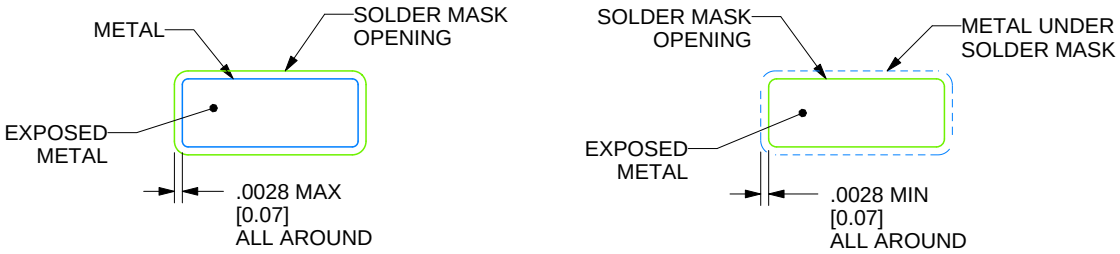


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

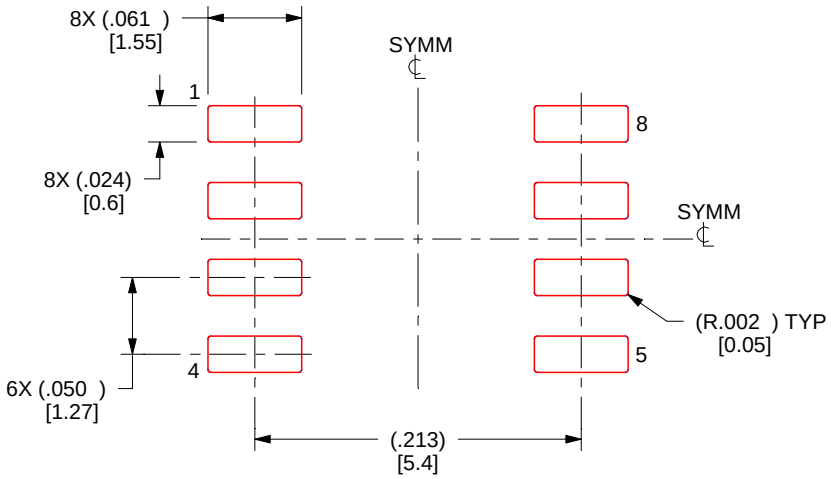
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



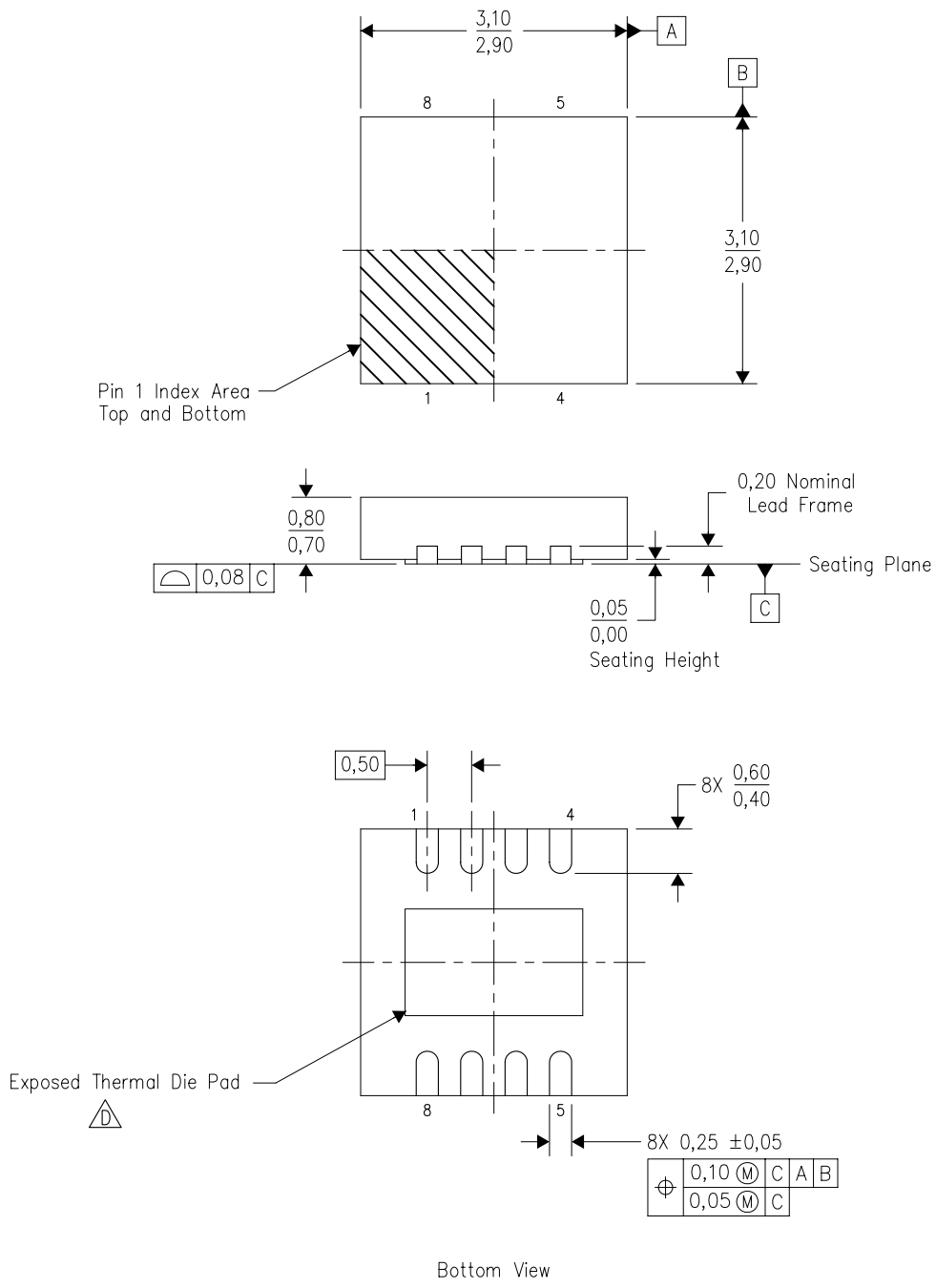
SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

DRG (S–PWSON–N8) PLASTIC SMALL OUTLINE NO–LEAD



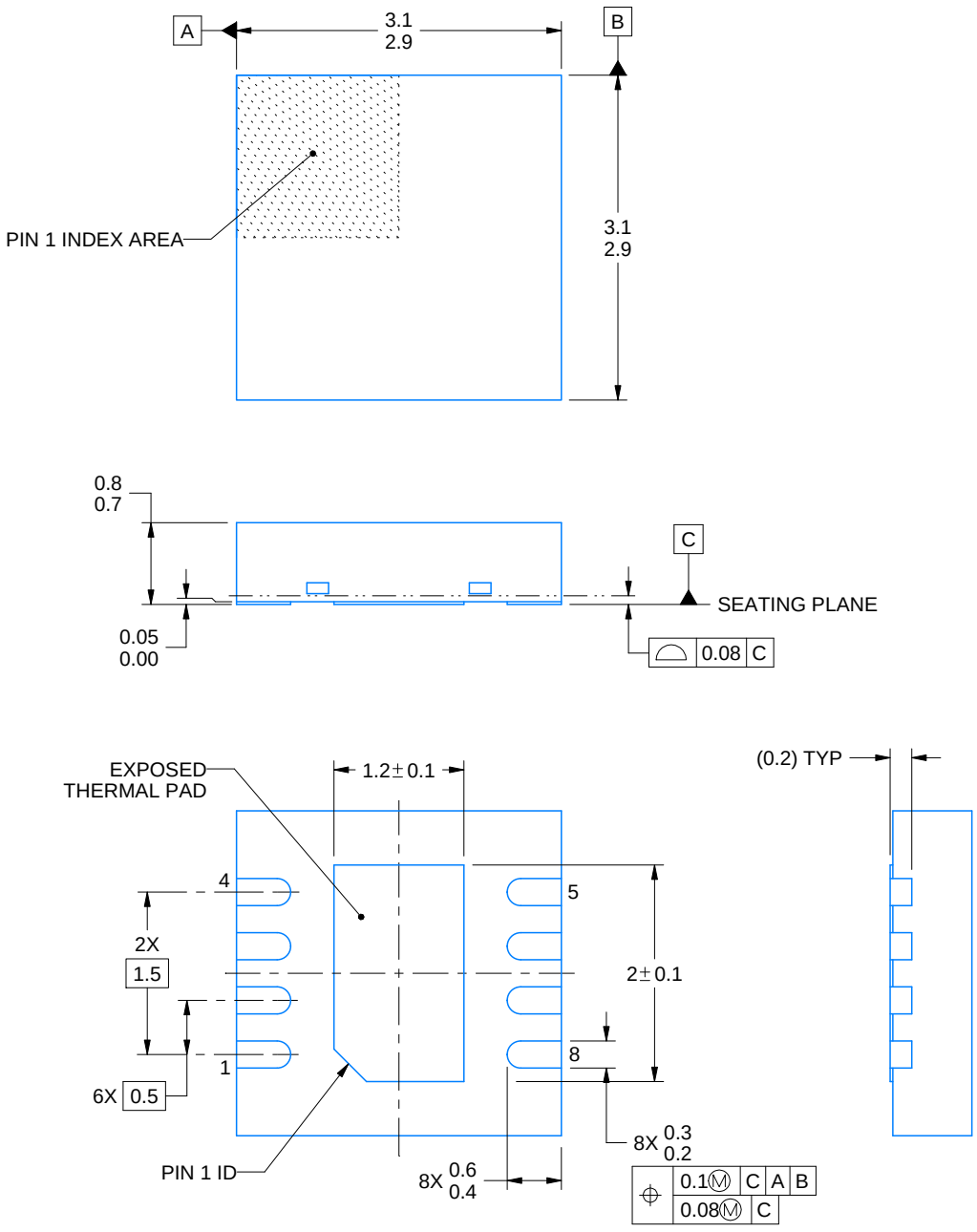
NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. SON (Small Outline No–Lead) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.
E. JEDEC MO–229 package registration pending.

PACKAGE OUTLINE

DRG0008A

WSON - 0.8 mm max height

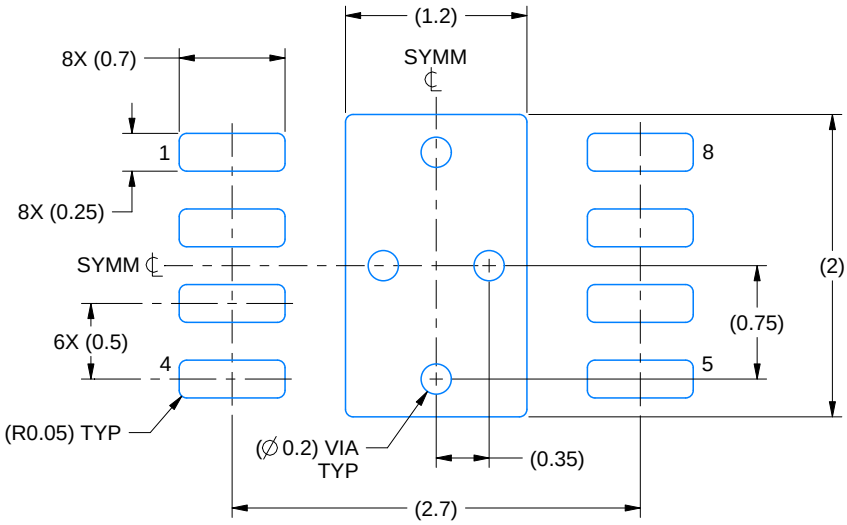
PLASTIC SMALL OUTLINE - NO LEAD



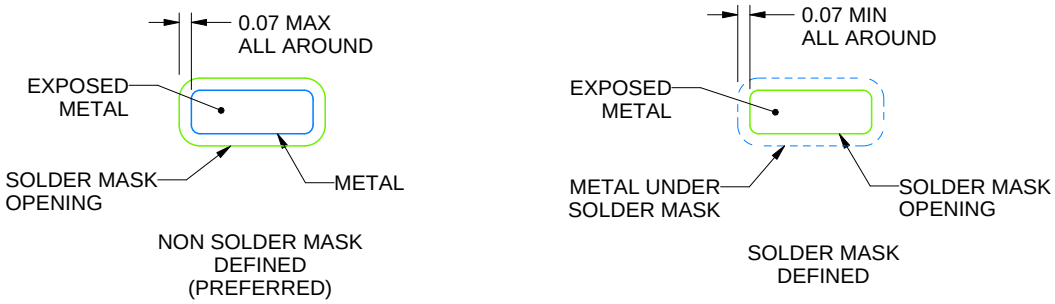
4218885/A 03/2020

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:20X

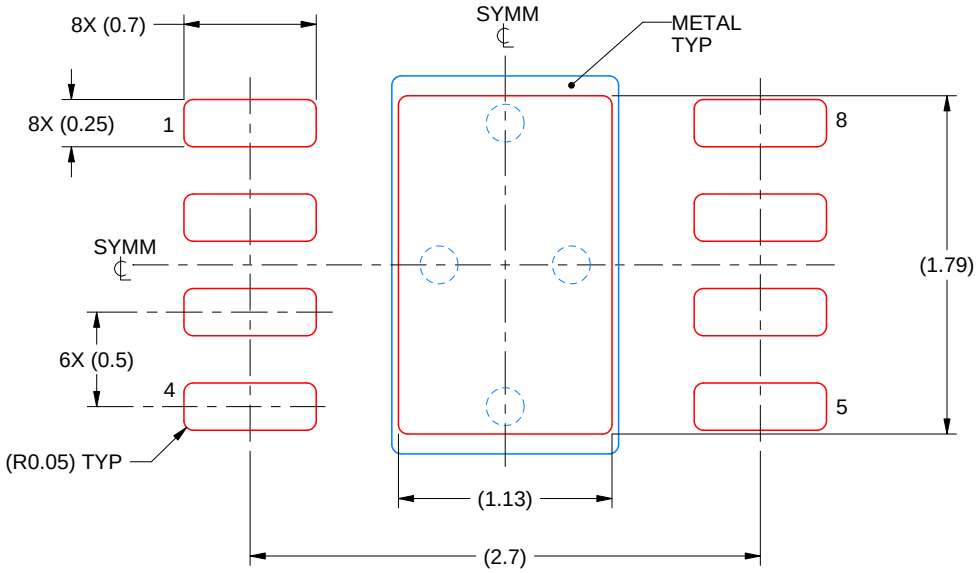


SOLDER MASK DETAILS

4218885/A 03/2020

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
84% PRINTED SOLDER COVERAGE BY AREA
SCALE:25X

4218885/A 03/2020

NOTES: (continued)

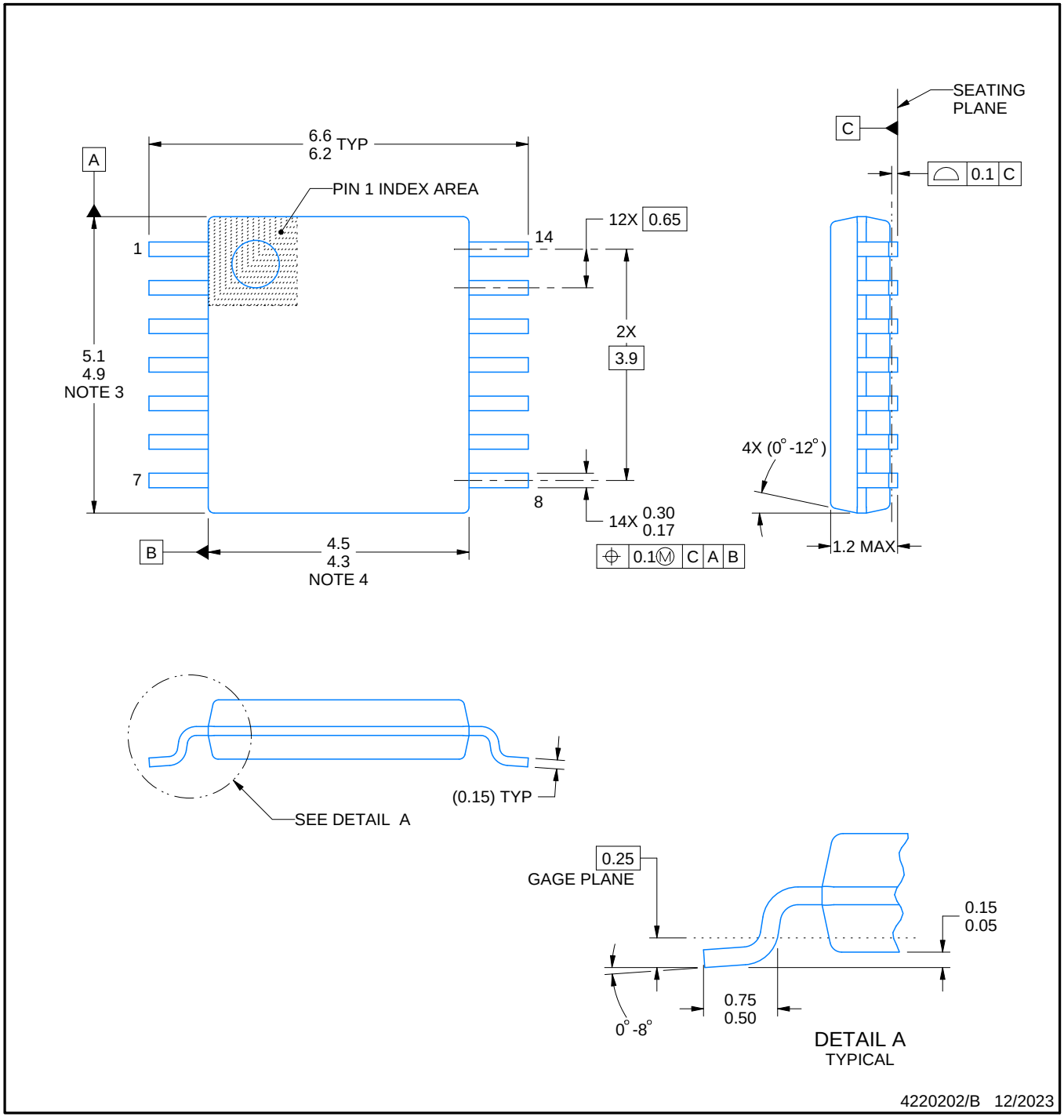
6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

PACKAGE OUTLINE

PW0014A

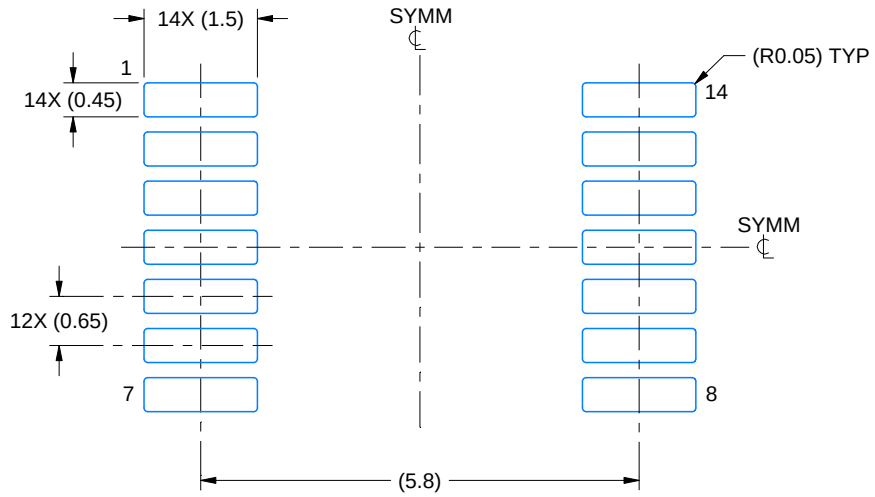
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

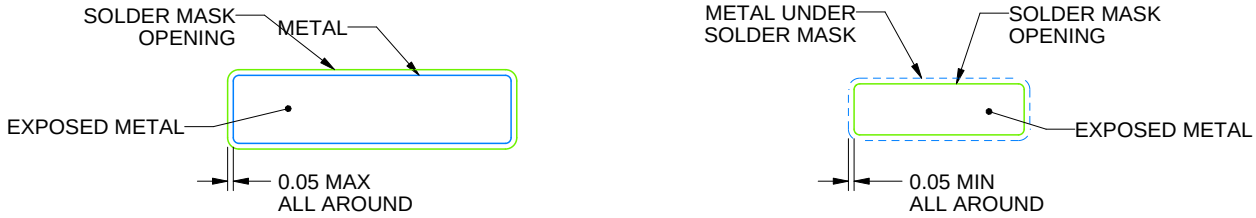


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

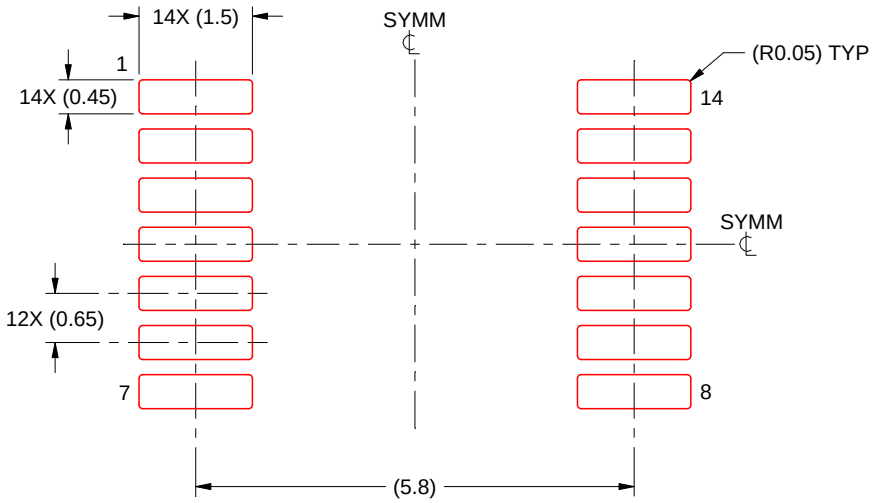


SOLDER MASK DETAILS

4220202/B 12/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220202/B 12/2023

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

重要通知和免责声明

TI“按原样”提供技术和可靠性数据（包括数据表）、设计资源（包括参考设计）、应用或其他设计建议、网络工具、安全信息和其他资源，不保证没有瑕疵且不做出任何明示或暗示的担保，包括但不限于对适销性、某特定用途方面的适用性或不侵犯任何第三方知识产权的暗示担保。

这些资源可供使用 TI 产品进行设计的熟练开发人员使用。您将自行承担以下全部责任：(1) 针对您的应用选择合适的 TI 产品，(2) 设计、验证并测试您的应用，(3) 确保您的应用满足相应标准以及任何其他功能安全、信息安全、监管或其他要求。

这些资源如有变更，恕不另行通知。TI 授权您仅可将这些资源用于研发本资源所述的 TI 产品的相关应用。 严禁以其他方式对这些资源进行复制或展示。您无权使用任何其他 TI 知识产权或任何第三方知识产权。您应全额赔偿因在这些资源的使用中对 TI 及其代表造成的任何索赔、损害、成本、损失和债务，TI 对此概不负责。

TI 提供的产品受 TI 的销售条款或 ti.com 上其他适用条款/TI 产品随附的其他适用条款的约束。TI 提供这些资源并不会扩展或以其他方式更改 TI 针对 TI 产品发布的适用的担保或担保免责声明。

TI 反对并拒绝您可能提出的任何其他或不同的条款。

邮寄地址：Texas Instruments, Post Office Box 655303, Dallas, Texas 75265