1MHz，微功耗，低噪声，轨到轨输出入输出 (RRIO)，1.8V CMOS 运算放大器
价值线系列

查询样品: OPA313, OPA2313, OPA4313

特性

- 低 I_Q：50μA/ch
- 宽电源电压：1.8V 至 5.5V
- 低噪声：1kHz 下为 25nV/√Hz
- 增益带宽：1MHz
- 低输入偏置电流：0.2pA
- 低偏移电压：0.5mV
- 单位增益稳定
- 内部射频 (RF) / 电磁干扰 (EMI) 滤波器
- 扩展温度范围：
  -40°C 至 +125°C

应用范围

- 电池供电仪器：
  - 消费类应用、工业应用、医疗应用
  - 笔记本电脑、便携式媒体播放器
- 传感器信号调节：
  - 回路供电类应用
  - 笔记本电脑、便携式媒体播放器
- 无线传感器：
  - 住所安全
  - 远程感测
  - 无线仪表

说明

OPA313 系列单通道、双通道和四通道运算放大器代表了新一代的低成本、通用、微功耗运算放大器。 轨到轨输入和输出摆幅，低静态电流（典型值 50μA）与 1MHz 的宽带宽和极低噪声（1kHz 时为 25nV/√Hz）组合在一起使得这个系列对于要求在成本和性能间达到很好平衡的多种电池供电类应用具有很大的吸引力。 低输入偏置电流支持那些在具有兆欧级源阻抗的应用中使用的运算放大器。

OPA313 器件的稳健耐用设计方便了电路设计人员的使用：负载电容高达 150pF 时单位增益稳定、一个集成的 RF/EMI 抑制滤波器、在过驱情况下无相位反转和高静电放电 (ESD) 保护（4kV 人体模型 (HBM)）。

这些器件针对低至 +1.8V (±0.9V) 和最高 +5.5V (±2.75V) 的低压运行进行了优化，并且在电压为 1.8V，3.3V 和 5V 时，其额定运行温度范围为 -40°C 至 +125°C 的完全扩展温度范围。

OPA313（单通道）采用 SC70-5 和小外形尺寸晶体管 (SOT)23-5 封装。 OPA2313（双通道）采用小外形尺寸 (SO)-8，微型小外形尺寸 (MSOP)-8 和四方扁平无引线 (DFN)-8 封装。 四通道 OPA4313 采用薄型小外形尺寸 (TSSOP)-14 封装。

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English Data Sheet: SBOS649

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

封装信息[1]

产品	封装-引线	封装指示符	额定温度范围	封装标识
OPA313	SC70-5	DCK	-40°C 至 125°C	SIE
	小外形尺寸晶体管封装 (SOT) 23-5	DBV	-40°C 至 125°C	SIF
OPA2313	SO-8	D	-40°C 至 125°C	OP2313
	MSOP-8	DGK	-40°C 至 125°C	OUSS
	DFN-8	DRG	-40°C 至 125°C	SDY
OPA4313	TSSOP-14	PW	-40°C 至 125°C	OPA4313

(1) 要获得最新的封装和订货信息，请参阅本文档末尾的封装选项附录，或者访问www.ti.com上的器件产品文件夹。

最大绝对额定值[1]

在自然通风温度范围内运行测得，除非另有说明。

		OPA313，OPA2313，OPA4313	单位
电源电压		7	V
单输入端子	电压[2]	(V-)-0.5 至 (V+)+0.5	V
	电流[2]	±10	mA
输出短路[3]		连续	mA
运行温度，T_A		-40 至 +150	°C
存储温度，T_{stg}		-65 至 +150	°C
结温，T_J		+150	°C
静电放电 (ESD) 额定值	人体模型 (HBM)	4000	V
	充电器件模型 (CDM)	1000	V
	机器模型 (MM)	200	V

(1) 超过这些额定值的应力有可能造成永久损坏。 长时间处于最大绝对额定情况下会降低设备的可靠性。 这些只是应力额定值，在这些值或者任何超过那些所标明的条件下的功能运行并未注明。
(2) 输入端子被二极管钳制至电源轨。 摆幅超过电源轨 0.5V 的输入信号的电流应该被限制在 10mA 或者更少。
(3) 短路至接地，每封装一个放大器。

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电气特性：V_S= +1.8V 至 +5.5V[1]

T_A=+25 °C 时，R_L=10kΩ 被连接至 V_S/2，并且 V_{CM}=V_{OUT}=V_S/2，除非另外注明。

参数		测试条件	OPA313，OPA2313，OPA4313			单位
			最小值	典型值	最大值	
偏移电压						
V_{OS}	输入偏移电压			0.5	2.5	mV
dV_{OS}/dT	与温度间的关系	T_A=-40°C 至 +125°C		2		μV/°C
电源抑制比 (PSRR)	与电源的关系	T_A=-40°C 至 +125°C	74	90		dB
	通道分离，直流	在直流		10		μV/V 时
输入电压范围						
V_{CM}	共模电压范围	无相位反向，轨到轨输入	(V-)-0.2		(V+)+0.2	V
CMRR	共模抑制比	T_A=-40°C 至 +125°C 时，(V_S-)-0.2V<V_{CM}<(V_S+)-1.3V	70	85		dB
		V_S=1.8V，V_{CM}=-0.2V 至 +1.8V	58	73		dB
		T_A=-40°C 至 +125°C 时，V_S=1.8V，V_{CM}=-0.2V 至 +1.6V	58	70		dB
		T_A=-40°C 至 +125°C 时, V_S=5.5V，V_{CM}=-0.2V 至 5.7V[2]	64	80		dB
输入偏置电流						
I_B	输入偏置电流			±0.2	±10	pA
		T_A=-40°C 至 +85°C			±50	pA
		T_A=-40°C 至 +125°C			±600	pA
I_{OS}	输入偏移电流			±0.2	±10	pA
		T_A=-40°C 至 +85°C			±50	pA
		T_A=-40°C 至 +125°C			±600	pA
噪声						
	输入电压噪声（峰值至峰值）	f=0.1Hz 至 10Hz		6		$μV_{PP}$
e_n	输入电压噪声密度	f=10kHz		22		nV/√Hz
		f=1kHz		25		nV/√Hz
i_n	输入电流噪声密度	f=1kHz		5		fA/√Hz
输入电容						
C_{IN}	差分电压			1		pF
	共模			5		pF
开环增益						
A_{OL}	开环电压增益	T_A=-40°C 至 +125°C 时 V_S=1.8V，0.1V<V_O<(V+)-0.1V	90	110		dB
		T_A=-40°C 至 +125°C 时 V_S=5.5V，0.1V<V_O<(V+)-0.1V	104	116		dB
		T_A=-40°C 至 +125°C 时 V_S=1.8V，0.3V<V_O<(V+)-0.3V，R_L=2kΩ[2]	90	100		dB
		T_A=-40°C 至 +125°C 时 V_S=5.5V，0.3V<V_O<(V+)-0.3V，R_L=2kΩ[2]	100	110		dB
	相位裕量	V_S=5.0V，G=+1		65		度

(1) 最小或最大额定限值参数在 +25ºC 时经 100% 生产测试，除非另外注明。 温度范围内的限值基于特性和统计分析。
(2) 由设计和特性指定；未经生产测试。

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电气特性：V_S= +1.8V 至 +5.5V[1] (continued)

T_A=+25 °C 时，R_L=10kΩ 被连接至 V_S/2，并且 V_{CM}=V_{OUT}=V_S/2，除非另外注明。

参数		测试条件	OPA313，OPA2313，OPA4313			单位
			最小值	典型值	最大值	
频率响应						
GBW	带宽增益产品	V_S=1.8V，C_L=10pF		0.9		MHz
		V_S=5.0V，C_L=10pF		1		MHz
SR	转换率	V_S=1.8V，G=+1		0.45		V/μs
		V_S=5.0V，G=+1		0.5		V/μs
t_S	稳定时间	到 0.1%，V_S=5.0V，2V 阶跃，G=+1 时的稳定时间		5		μs
		到 0.01%，V_S=5.0V，2V 阶跃，G=+1 时的稳定时间		6		μs
	过载恢复时间	V_S=5.0V，V_{IN}× 增益 > V_S		3		μs
THD+N	总谐波失真 + 噪声[3]	V_S=5.0V，V_O=1V_{RMS}，G=+1，f=1kHz		0.0045 %		
输出						
V_O	自电源轨的输出电压摆幅	V_S=1.8V，R_L=100kΩ[4]		5	15	mV
		V_S=5.5V，R_L=100kΩ[4]		5	20	mV
		T_A=-40°C 至 +125°C，R_L=100 kΩ[4]			30	mV
		V_S=1.8V，R_L=2kΩ[4]		25	50	mV
		V_S=5.5V，R_L=2kΩ[4]		75	100	mV
		T_A=-40°C 至 +125°C，R_L=2kΩ			125	mV
I_{SC}	短路电流	V_S=1.8V		±6		mA
		V_S=5.5V		±15		mA
		T_A=-40°C 至 +125°C，V_S=5.5V		±12		mA
R_O	开环输出阻抗			2300		Ω
电源						
V_S	额定电压范围		1.8 (±0.9)		5.5 (±2.75)	V
I_Q	每个放大器的静态电流	I_O=0mA		50	60	μA
		T_A=-40°C 至 +125°C，V_S=5.0V，I_O=0mA			85	μA
	加电时间	V_S=0V 至 5V，达到 90% I_Q水平		10		μs
温度						
	额定温度		-40		+125	°C
	工作范围		-40		+150	°C
	储存温度		-65		+150	°C

(3) 三阶滤波器；-3dB 时的带宽 = 80kHz。
(4) 由设计和特性指定；未经生产测试。

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热性能信息：OPA313

热度量[1]		OPA313 DBV (SOT23) 5 引脚	OPA313 DCK (SC70) 5 引脚	单位
θ_{JA}	结到环境热阻	228.5	281.4	°C/W
$\theta_{JC(top)}$	结至芯片外壳（顶部）热阻	99.1	91.6	
θ_{JB}	结至电路板热阻	54.6	59.6	
ψ_{JT}	结至顶部的特征参数	7.7	1.5	
ψ_{JB}	结至电路板的特征参数	53.8	58.8	
$\theta_{JC(bottom)}$	结至芯片外壳（底部）热阻	不可用	不可用	

(1) 有关传统和新的热 度量的更多信息，请参阅*IC 封装热度量*应用报告， SPRA953。

热性能信息：OPA2313

热度量[1]		OPA2313 D (SO) 8 引脚	OPA2313 DGK (MSOP) 8 引脚	OPA2313 DRG (DFN) 8 引脚	单位
θ_{JA}	结到环境热阻	138.4	191.2	53.8	°C/W
$\theta_{JC(top)}$	结至芯片外壳（顶部）热阻	89.5	61.9	69.2	
θ_{JB}	结至电路板热阻	78.6	111.9	20.1	
ψ_{JT}	结至顶部的特征参数	29.9	5.1	3.8	
ψ_{JB}	结至电路板的特征参数	78.1	110.2	20.0	
$\theta_{JC(bottom)}$	结至芯片外壳（底部）热阻	不可用	不可用	11.6	

(1) 有关传统和新的热 度量的更多信息，请参阅*IC 封装热度量*应用报告， SPRA953。

热性能信息：OPA4313

热度量[1]		OPA4313 PW (TSSOP) 14 引脚	单位
θ_{JA}	结到环境热阻	121.0	°C/W
$\theta_{JC(top)}$	结至芯片外壳（顶部）热阻	49.4	
θ_{JB}	结至电路板热阻	62.8	
ψ_{JT}	结至顶部的特征参数	5.9	
ψ_{JB}	结至电路板的特征参数	62.2	
$\theta_{JC(bottom)}$	结至芯片外壳（底部）热阻	不可用	

(1) 有关传统和新的热 度量的更多信息，请参阅*IC 封装热度量*应用报告， SPRA953。

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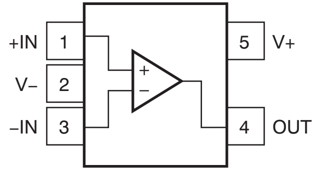
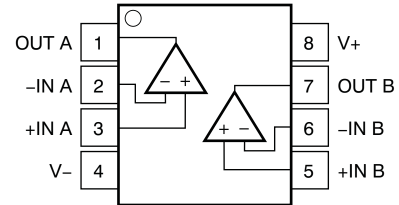
引脚配置

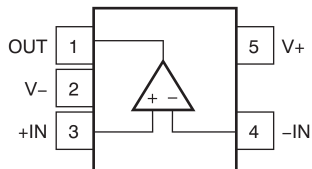
DCK 封装
SC70-5
（顶视图）



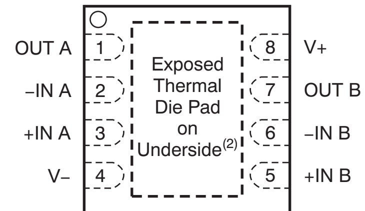
D，DGK 封装
SO-8，MSOP-8
（顶视图）



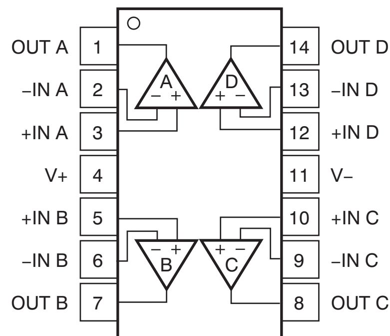
DBV 封装
小外形尺寸晶体管封装 (SOT) 23-5
（顶视图）



DRG 封装(1)
DFN-8
（顶视图）



PW 封装
TSSOP-14
（顶视图）



(1) 焊球间距：0.65mm

(2) 将散热垫连接至 V-。 散热垫尺寸：1.8mm x 1.5mm。

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典型特征

Table 1. 特征性能测量

标题	图表
开环增益和相位与频率间的关系	Figure 1
开环增益与温度间的关系	Figure 2
静态电流与电源电压间的关系	Figure 3
静态电流与温度间的关系	Figure 4
偏移电压产品分布	Figure 5
偏移电压漂移分布	Figure 6
偏移电压与共模电压间的关系（最大电源）	Figure 7
偏移电压与温度间的关系	Figure 8
CMRR 和电源抑制比 (PSRR) 与频率间的关系 (RTI)	Figure 9
CMRR 和 PSRR 温度间的关系	Figure 10
0.1Hz 至 10Hz 输入电压噪声 (5.5V)	Figure 11
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输入电压噪声与共模电压间的关系 (5.5V)	Figure 13
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最大输出电压与频率和电源电压间的关系	Figure 16
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小信号阶跃响应，非反相 (5.5V)	Figure 23
大信号阶跃响应，非反相 (1.8V)	Figure 24
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THD+N 与频率间的关系 (0.5V_{RMS}，G=+1，2kΩ，10kΩ)	Figure 32
电磁干扰抑制比 (EMIRR) IN+ 与频率间的关系	Figure 33

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典型特征

T_A=+25 °C 时，R_L =10kΩ 被连接至 $V_S/2$，并且 $V_{CM}=V_{OUT}=V_S/2$，除非另外注明。

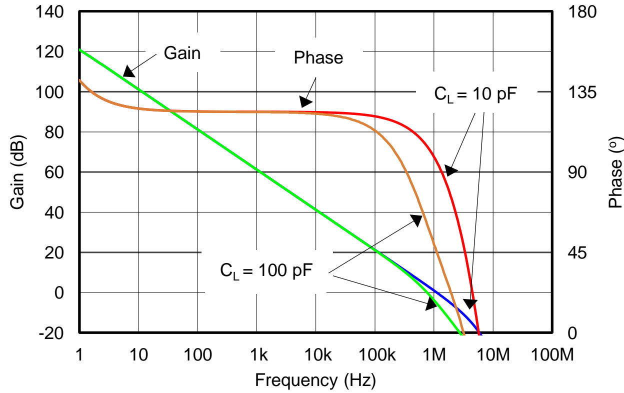

Figure 1. 开环增益和相位与频率间的关系

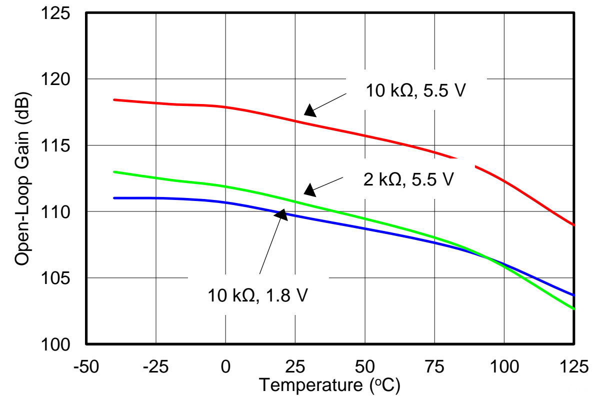

Figure 2. 开环增益与温度间的关系

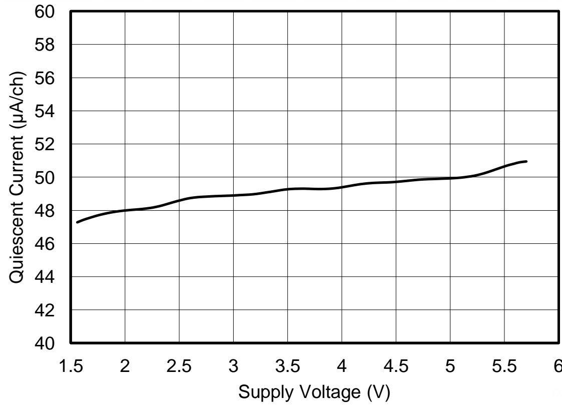

Figure 3. 静态电流与电源间的关系

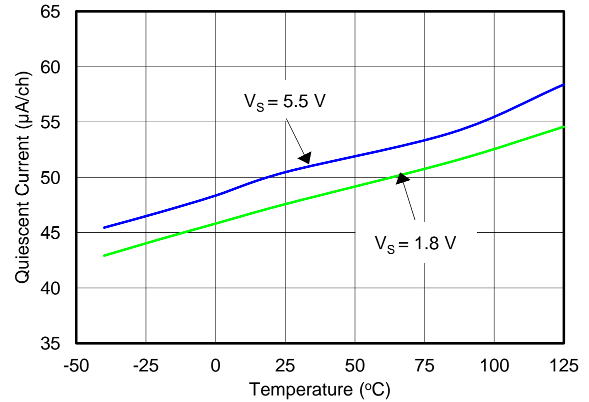

Figure 4. 静态电流与温度间的关系

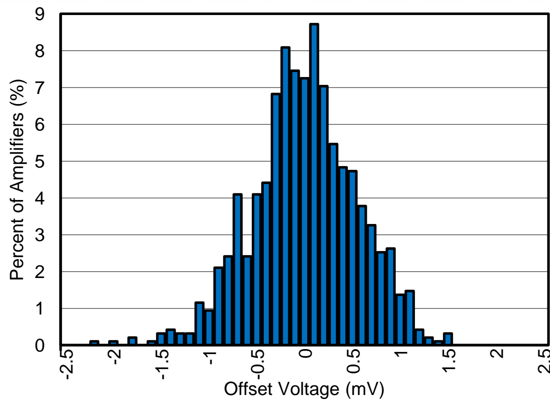

Figure 5. 偏移电压产品分布

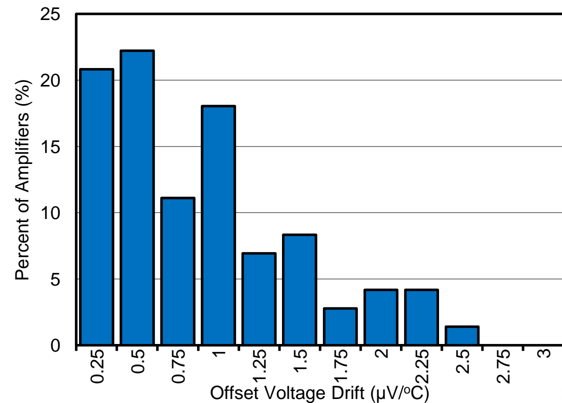

Figure 6. 偏移电压漂移分布

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典型特征 (continued)

T_A=+25 °C 时，R_L =10kΩ 被连接至 V_S/2，并且 V_{CM}=V_{OUT}=V_S/2，除非另外注明。

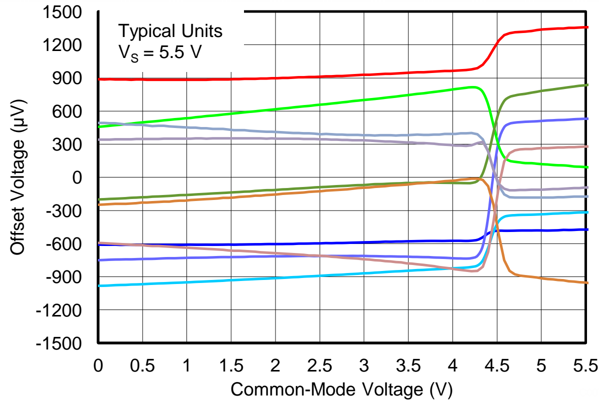

Figure 7. 偏移电压与共模电压间的关系

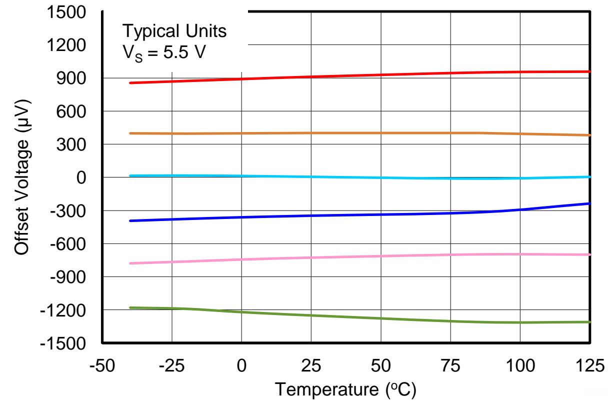

Figure 8. 偏移电压与温度间的关系

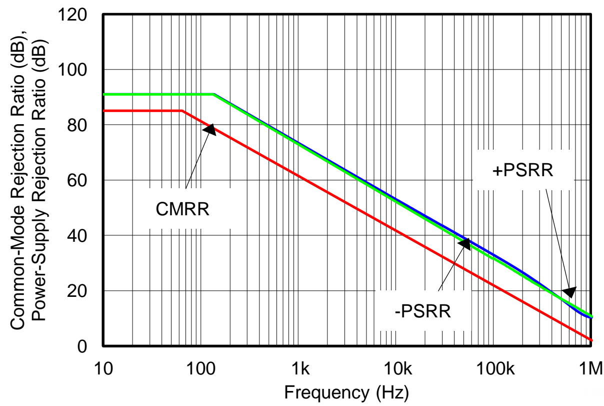

Figure 9. CMRR 和 PSRR 与频率间的关系（以输入为基准）

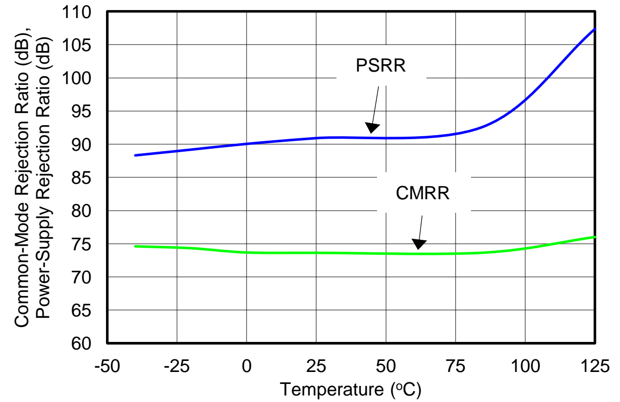

Figure 10. CMRR 和 PSRR 与温度间的关系

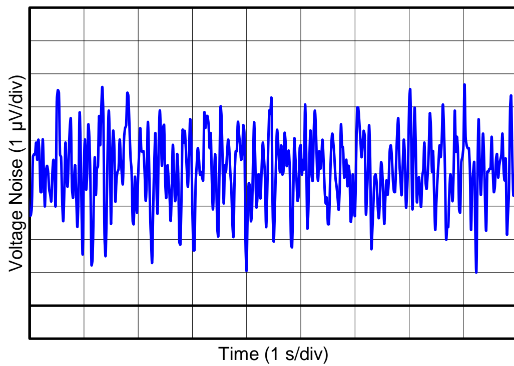

Figure 11. 0.1Hz 至 10Hz 输入电压噪声

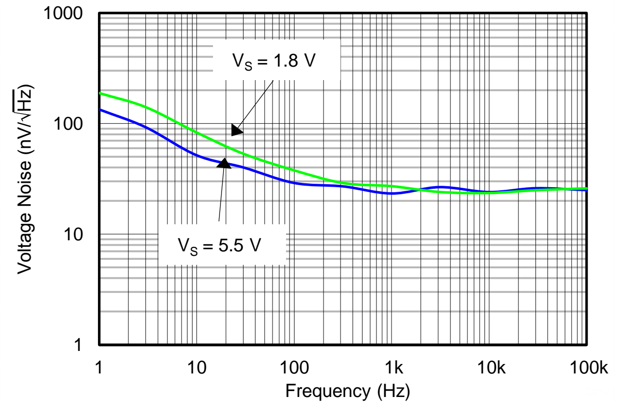

Figure 12. 输入电压噪声频谱密度与频率间的关系

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典型特征 (continued)

T_A=+25 °C 时，R_L =10kΩ 被连接至 $V_S/2$，并且 $V_{CM}=V_{OUT}=V_S/2$，除非另外注明。

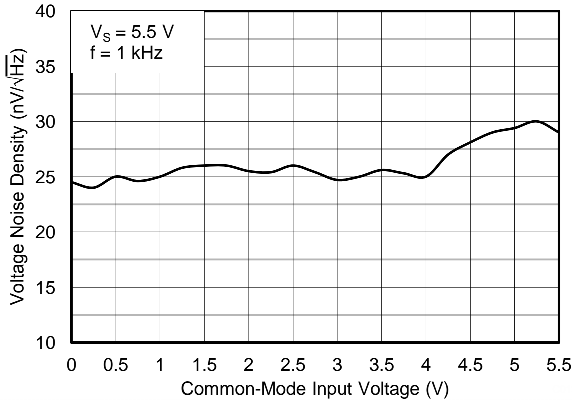

Figure 13. 电压噪声与共模电压间的关系

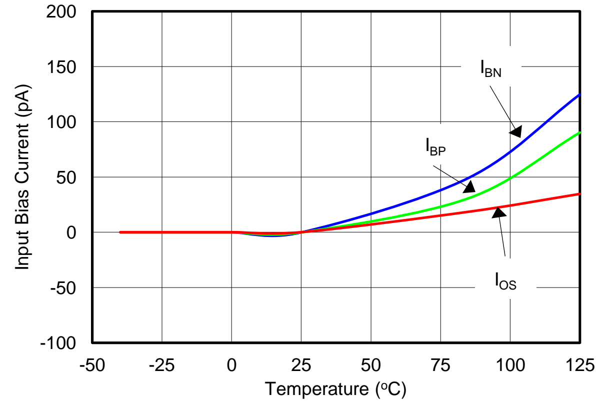

Figure 14. 输入偏置和偏移电流与温度间的关系

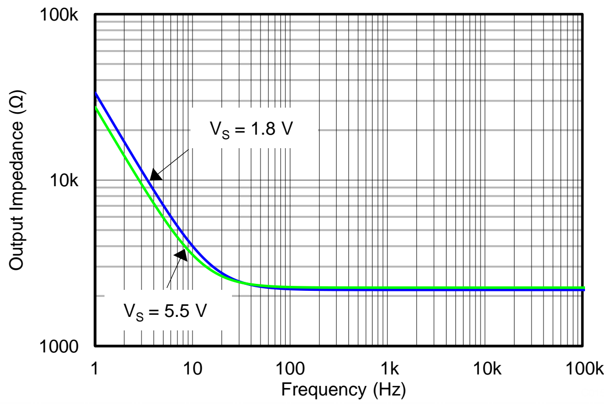

Figure 15. 开环输出阻抗与频率间的关系

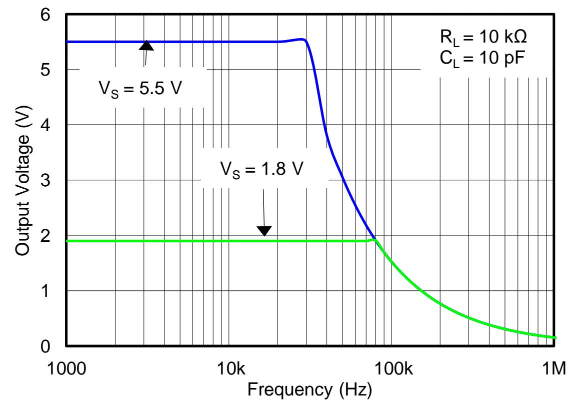

Figure 16. 最大输出电压与频率和电源电压间的关系

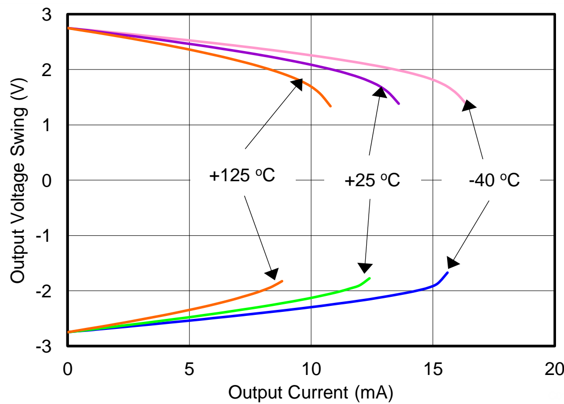

Figure 17. 输出电压摆幅与输出电流间的关系（温度范围内）

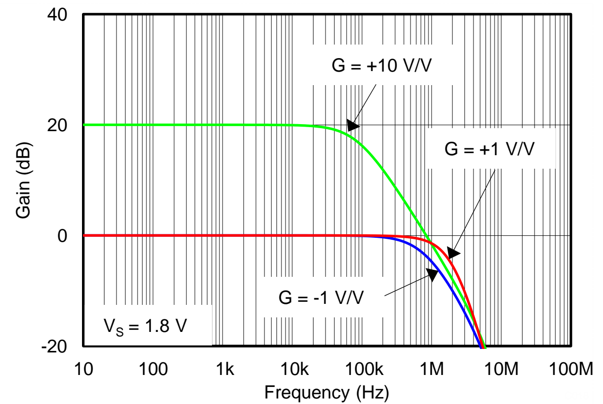

Figure 18. 闭环增益与频率间的关系（最小电源）

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典型特征 (continued)

T_A=+25 °C 时，R_L =10kΩ 被连接至 V_S/2，并且 V_{CM}=V_{OUT}=V_S/2，除非另外注明。

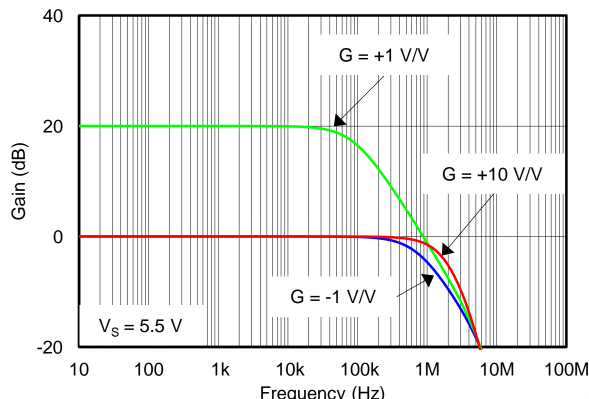

Figure 19. 闭环增益与频率间的关系（最大电源）

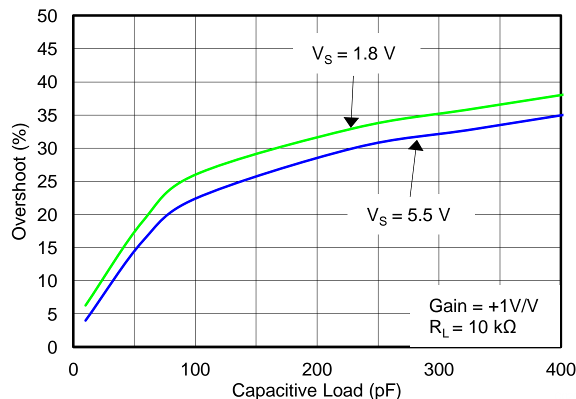

Figure 20. 小信号过冲与负载电容间的关系

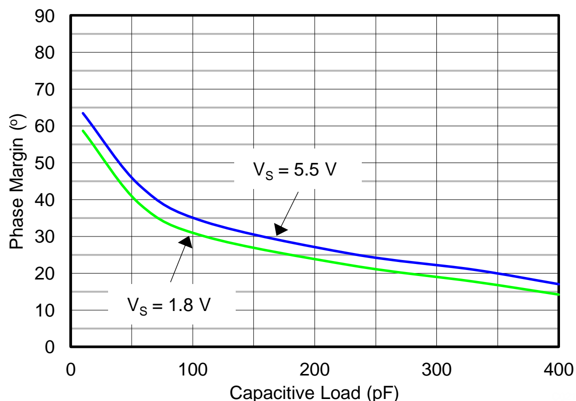

Figure 21. 相位裕量与电容负载间的关系

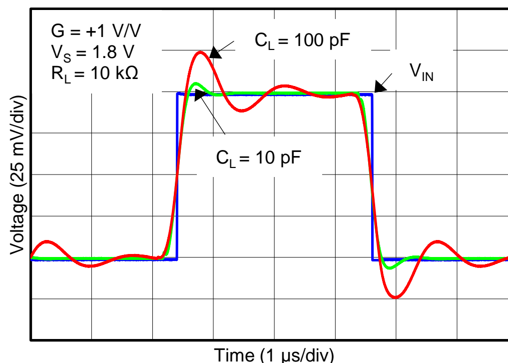

Figure 22. 小信号脉冲响应（最小电源）

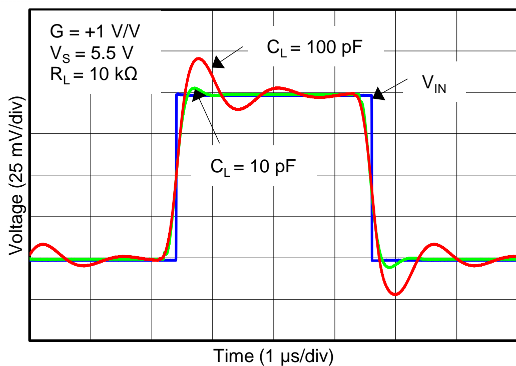

Figure 23. 小信号脉冲响应（最大电源）

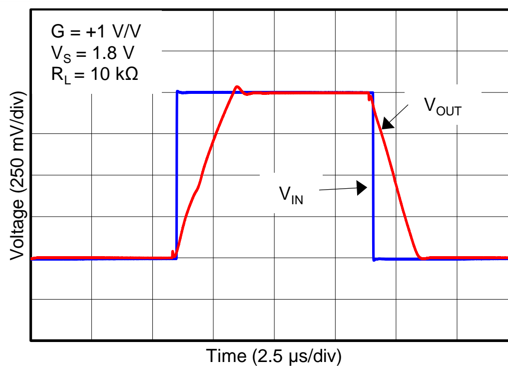

Figure 24. 大信号脉冲响应（最小电源）

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典型特征 (continued)

T_A=+25 °C 时，R_L =10kΩ 被连接至 $V_S/2$，并且 $V_{CM}=V_{OUT}=V_S/2$，除非另外注明。

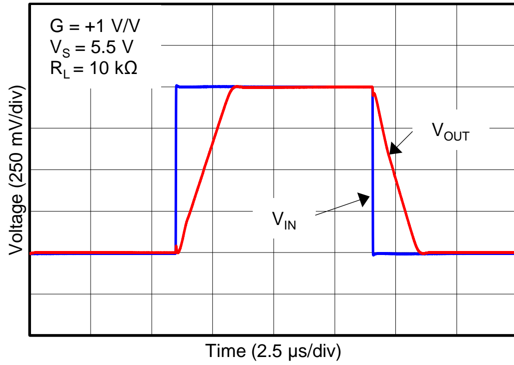

Figure 25. 大信号脉冲响应（最大电源）

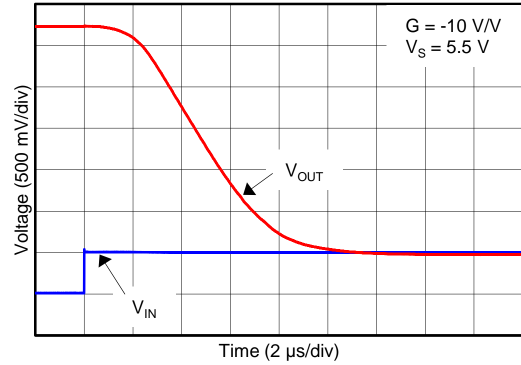

Figure 26. 正过载恢复

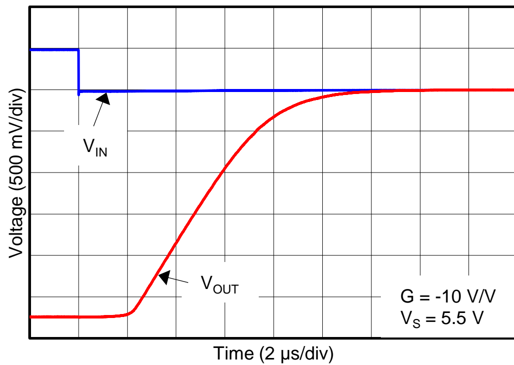

Figure 27. 负过载恢复

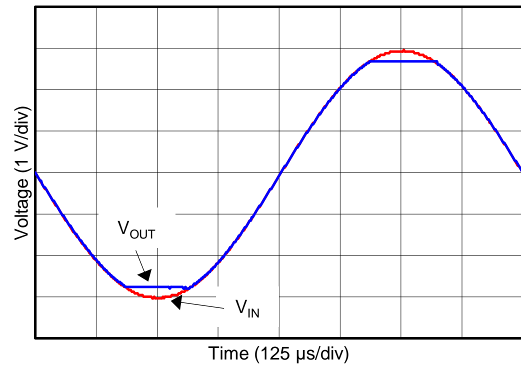

Figure 28. 无相位反转

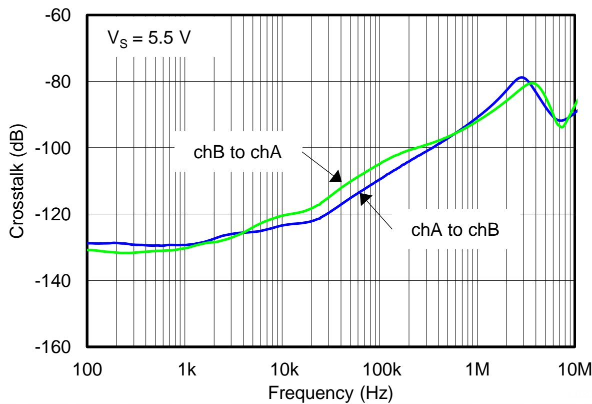

Figure 29. 通道分离与频率间的关系

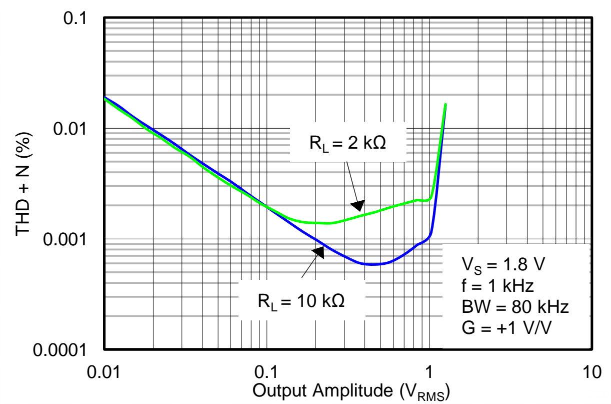

Figure 30. THD+N 与输出摆幅间的关系（最小电源）

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典型特征 (continued)

T_A=+25 °C 时，R_L =10kΩ 被连接至 $V_S/2$，并且 $V_{CM}=V_{OUT}=V_S/2$，除非另外注明。

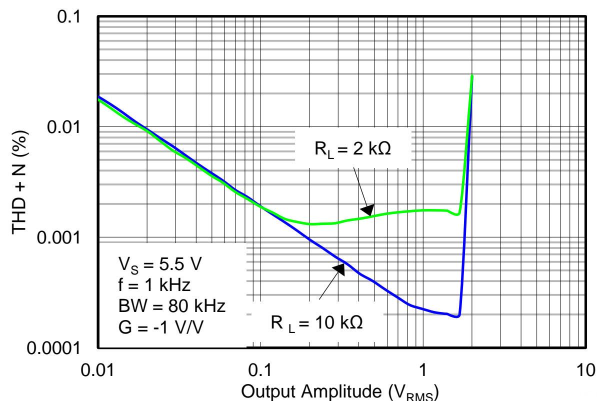

Figure 31. THD+N 与输出摆幅间的关系（最大电源）

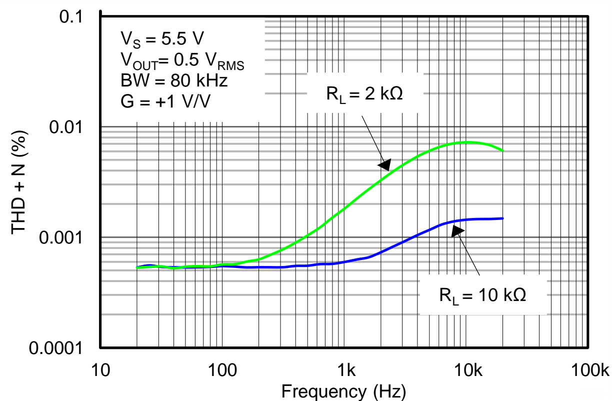

Figure 32. THD+N 与频率间的关系

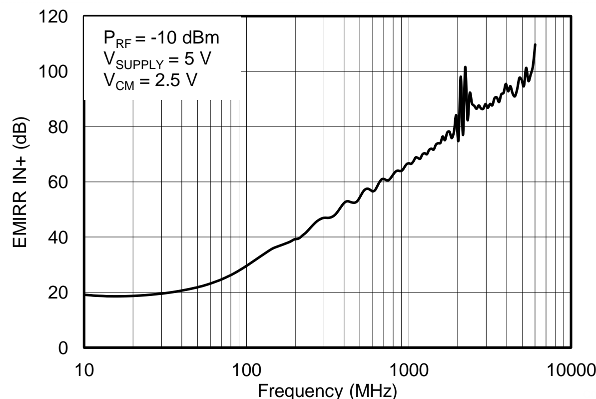

Figure 33. EMIRR IN+ 与频率间的关系

应用信息

OPA313 是一款专门为便携式应用而设计的低功耗、轨到轨输入和输出运算放大器。 这些器件的运行电压介于 1.8V 至 5.5V，单位增益稳定，并且非常适合于大范围的通用应用。 AB 类输出级能够驱动被连接至 V+ 和接地间任一点的小于等于 10kΩ 的负载。 输入共模电压范围包括两个电源轨并且可在实际上实现 OPA313 系列在任一单电源应用中的使用。 轨到轨输入和输出摆幅大大增加了动态范围，特别是在低电源应用中，并且使得此类产品非常适合于驱动采样模数转换器 (ADC)。

OPA313 特有 1MHz 带宽和 0.5V/μs 转换率，每通道电源电流只有 50μA，从而在极低功耗下提供非常好的交流性能。 在 1kHz 时为 DC 应用提供 25nV/√Hz的 极低输入噪声电压，低输入偏置电流 (0.2pA)，和一个 0.5mV（典型值）的输入偏移电压。 典型电压漂移为 2μV/°C；在整个温度范围内，输入偏移电压变化只有 200μV（0.5mV 至 0.7mV）。

工作电压

OPA313 系列运算放大器在 +1.8V 至 +5.5V 额定电压范围内可保证运行。此外，很多应用可应用于 -40°C 至 +125°C 温度范围内。 随工作电压或温度大幅变化的参数显示在 典型特征图中。 应使用 0.01μF 陶瓷电容器将电源引脚旁通。

轨到轨输入

OPA313 系列的输入共模电压范围将电源轨扩展 200mV。 此性能由一个互补输入级实现：与一个 P 通道差分对并联的 N 通道输入差分对，如Figure 34中所示。 N 通道对对于靠近正电源轨的输入电压有效，通常比正电源高 (V+)-1.3V 至 200mV，而 P 通道对针对低于负电源轨 200mV 至大约 (V+)1.3V 间的输入打开。有一个小转换区域，通常介于 (V+)-1.4V 至 (V+)-1.2V 之间，在这个区间内两个对都打开。 借助于过程变化，这个 200mV 转换区域的变化可高达 300mV。 因此，此转换区域（两个级都打开）在低端上的范围介于 (V+)-1.7V 至 (V+)-1.5V 之间，在高端上的范围高达 (V+)-1.1V 至 (V+)-0.9V 之间。 在这个转换区域内，相对于这个区域外的器件运行，PSRR，CMRR，偏移电压，偏移漂移和 THD 有可能降级。

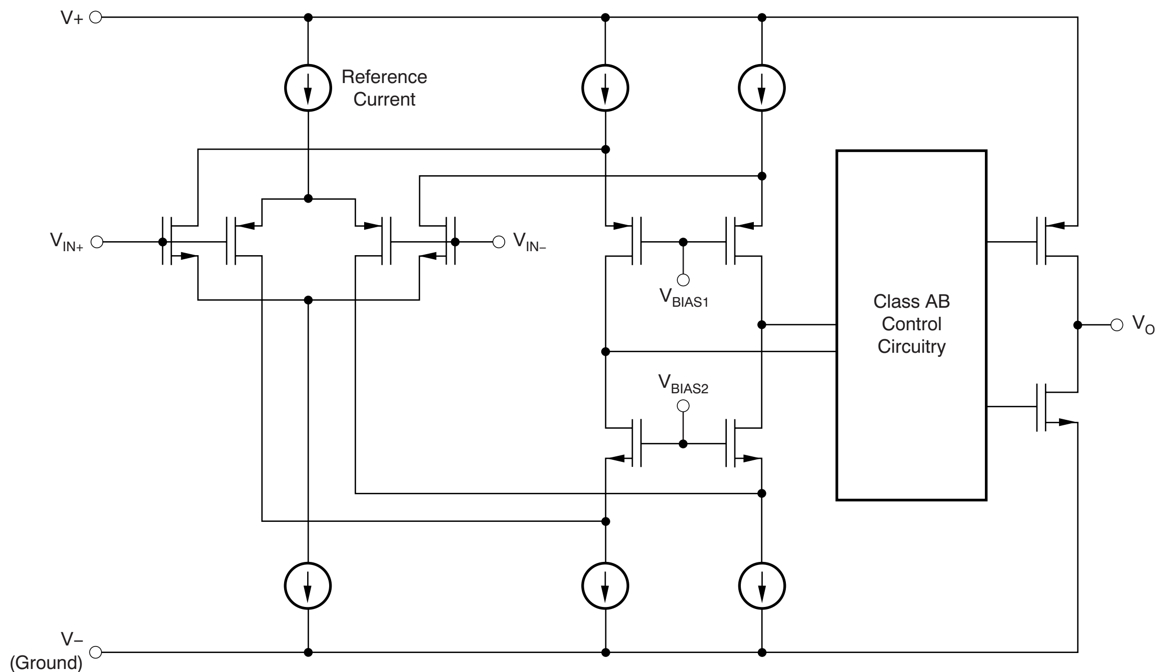

Figure 34. 简化电路原理图

输入和静电放电 (ESD) 保护

OPA313 系列在所有引脚上包含有内部静电放电 (ESD) 保护。 在输入和输出引脚的情况下，这个保护主要包括连接在输入和电源引脚间的电流转向二极管。 只要电流被限制在 绝对最大额定值中所述的 10mA 内，这些 ESD 保护二极管还提供电路内、输入过驱保护。Figure 35显示了如何将一个串联输入电阻器添加至被驱动的输入来限制输入电流。 这个增加的二极管在放大器输入上增加了热噪声并且它的值应该在噪声敏感应用中被保持在最小值。

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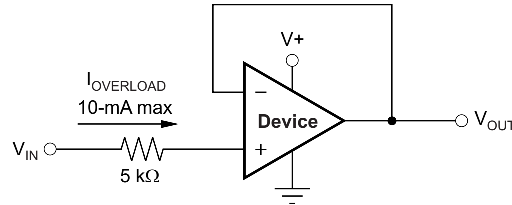

Figure 35. 输入电流保护

共模抑制比 (CMRR)

针对 OPA313 的 CMRR 用几种不同的方法指定，这样对于一个给定的应用，可找到最佳的匹配；请见 电气特性。首先，给出了低于转换区域 [V_{CM}<(V+)-1.3V] 的共模范围内器件的 CMRR。 当应用需要使用差分输入对中的一个时，这个技术规格是器件功能的最好指示。 其次，整个共模范围内的 CMRR 在（V_{CM}=-0.2V 至 5.7V）上指定。这个最终值包括转换区域内可见的变化（请见Figure 7）。

EMI 磁化率和输入过滤

运算放大器随着器件对于电磁干扰 (EMI) 的磁化率而发生变化。 如果被传导的 EMI 进入运算放大器，放大器输出上观察到的 dc 偏移当 EMI 出现时有可能偏离其标称值。 这个偏离是由与内部半导体结相关的信号修整引起的。虽然 EMI 会影响所有运算放大器引脚功能，但是信号输入引脚最有可能受到影响。 OPA313 运算放大器系列包含一个减少放大器对 EMI 响应的内部输入低通滤波器。 这个滤波器提供共模和差分模式滤波。 此滤波器针对大约 35MHz (-3dB) 的截止频率而设计，具有每十倍频 20dB 的下降率。

德州仪器 (TI) 已经开发出在 10MHz 至 6GHz 扩展宽频谱范围内准确测量和量化运算放大器抗扰度的功能。 EMI 抑制比 (EMIRR) 度量可实现运算放大器与 EMI 抗扰度的直接比较。Figure 33图示了在 OPA313 系列上进行这个测试所得到的结果。 也可在应用报告中找到详细信息，*运算放大器的 EMI 抑制比*(SBOA128)，可从www.ti.com内下载。

轨至轨输出

被设计成微功耗、低噪声运算放大器，OPA313 提供可靠耐用的输出驱动能力。 一个具有共源晶体管 AB 类输出级被用于实现完全轨到轨输出摆幅功能。 对于高达 10kΩ 的电阻负载，无论施加的电源电压是多少，输出摆幅通常在两个电源轨的 5mV 以内。 不同的负载情况改变放大器摆动靠近电源轨的能力；请参考典型特征图， *输出电压摆幅与输出电流间的关系*。

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电容负载和稳定性

OPA313 被设计用于需要驱动电容负载的应用中。 但与所有运算放大器一起工作时，有具体的实例表明 OPA313 会变得不稳定。 当确定放大器是否在运行中保持稳定时，需要考虑特定运算放大器电路配置、布局布线、增益和输出负载等因素。 相对于运行在较高噪声增益上的放大器，一个用单位增益 (+1V/V) 配置来驱动电容负载的的运算放大器不稳定的可能性更大。 与运算放大器输出电阻结合在一起的电容负载在反馈环路内生成一个使相位裕量降级的极点。 相位裕量的降级随着负载电容的增加而增加。 当运行在单位增益配置中时，OPA313 在纯电容负载达到大约 1nF 时仍然保持稳定。 某些超大电容器（C_L大于 1μF）的等效串联电阻足够改变反馈环路内的相位特性，从而使放大器保持稳定。 增加放大器闭环增益使得放大器能够驱动更大的电容。 当在更高电压增益上观察放大器的过冲响应时，这个增加的驱动能力会十分明显。 请见典型特征图，*小信号过冲与电容负载间的关系*。

一个增加运行在单位增益配置中的放大器电容负载驱动能力的技巧是插入一个小电阻器，通常为 10Ω 至 20Ω，与输出串联，如Figure 36中所示。 这个电阻器大大减少了与大电容负载相关的过冲和振铃。 然而，这个技巧的一个可能问题是这个增加的串联电阻和任一与负载电容并联的连接电阻会生成一个分压器。 此电压分压器在输出上引入一个减少输出摆幅的增益错误。

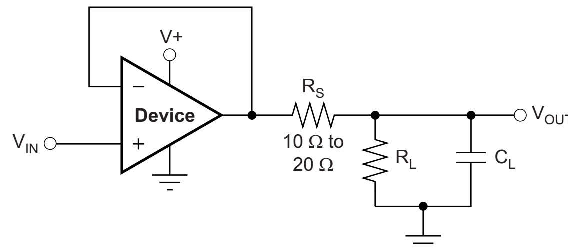

Figure 36. 改进电容负载驱动

DFN 封装

OPA2313（双通道版本）使用 DFN 类型封装（也称为小外形尺寸无引线 (SON) 封装）；这个封装是只在封装底部两侧有接触点的四方扁平无引线 (QFN) 封装。 这个无引线封装大大增加了印刷电路板 (PCB) 尺寸并且通过一个外露散热垫来提高散热和电气特性。 DFN 封装的一个主要优势是其 0.9mm 的低高度。 DFN 封装物理尺寸小，具有更小的走线面积、改进的散热性能、减少的电气寄生，并且使用一个与其它诸如小外形尺寸 (SO) 和微型小外形尺寸 (MSOP) 等常见封装一致的引脚分配机制。 此外，无外部引线也消除了引线弯曲问题的出现。

DFN 封装可使用标准 PCB 组装技巧轻松安装。 请见应用说明，*QFN/SON PCB 附件* (SLUA271) 和应用报告，*四方扁平无引线逻辑封装* (SCBA017)，都可以从www.ti.com内下载。

NOTE

DFN 封装底部的外露引线框下垫板应该被连接至最低负电压 (V-)。

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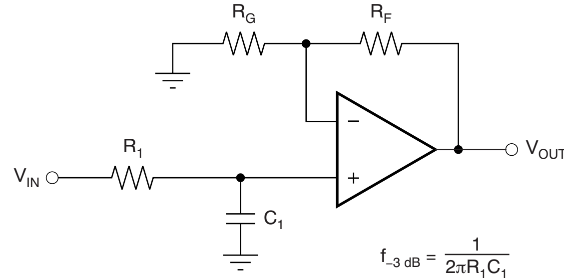
应用示例

常用配置

当接收到低电平信号时，经常需要限制即将进入系统的信号的带宽。 建立这个受限带宽的最简单的方法是在放大器的非反相端子上放置一个 RC 滤波器，如Figure 37中所示。



$$\frac{V_{OUT}}{V_{IN}} = \left(1 + \frac{R_F}{R_G}\right)\left(\frac{1}{1 + sR_1C_1}\right)$$

Figure 37. 单极点低通滤波器

如果需要更多的衰减，需要多个极点滤波器。 Sallen-Key 滤波器可被用于完成此项工作，如Figure 38所示。 为了获得最佳结果，放大器应该有一个 8 倍或 10 倍于滤波器频率带宽的带宽。 不遵守这一原则会导致放大器的相位偏移。

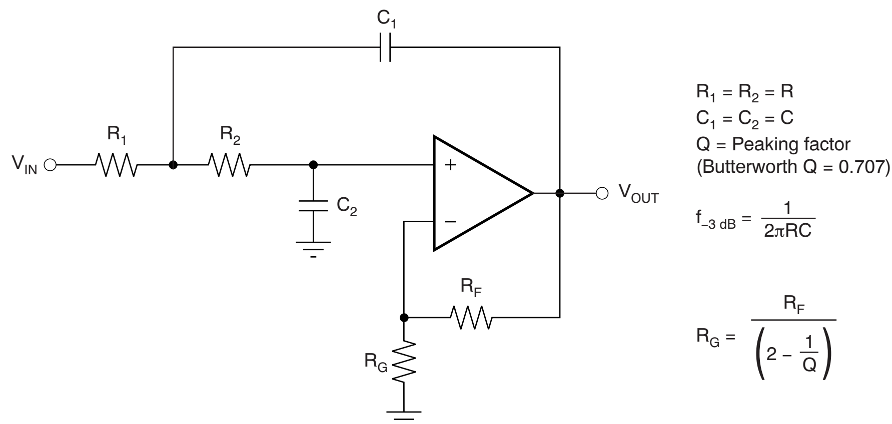


Figure 38. 两极点低通 Sallen-Key 滤波器

修订历史记录

请注意：前一修订版的页码可能与当前版本的页码不同。

Changes from Original (September 2012) to Revision A	Page
• 将产品预览改为生产数据	1

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
OPA2313ID	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OP2313	Samples
OPA2313IDGK	ACTIVE	VSSOP	DGK	8	80	RoHS & Green	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	OUSS	Samples
OPA2313IDGKR	ACTIVE	VSSOP	DGK	8	2500	RoHS & Green	NIPDAUAG | SN	Level-2-260C-1 YEAR	-40 to 125	OUSS	Samples
OPA2313IDR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OP2313	Samples
OPA2313IDRGR	ACTIVE	SON	DRG	8	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	SDY	Samples
OPA2313IDRGT	ACTIVE	SON	DRG	8	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	SDY	Samples
OPA313IDBVR	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	SIE	Samples
OPA313IDBVT	ACTIVE	SOT-23	DBV	5	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	SIE	Samples
OPA313IDCKR	ACTIVE	SC70	DCK	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	SIF	Samples
OPA313IDCKT	ACTIVE	SC70	DCK	5	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	SIF	Samples
OPA4313IPW	ACTIVE	TSSOP	PW	14	90	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OPA4313	Samples
OPA4313IPWR	ACTIVE	TSSOP	PW	14	2000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OPA4313	Samples

[1] The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

[2] **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

[3] MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

[4] There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

[5] Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

[6] Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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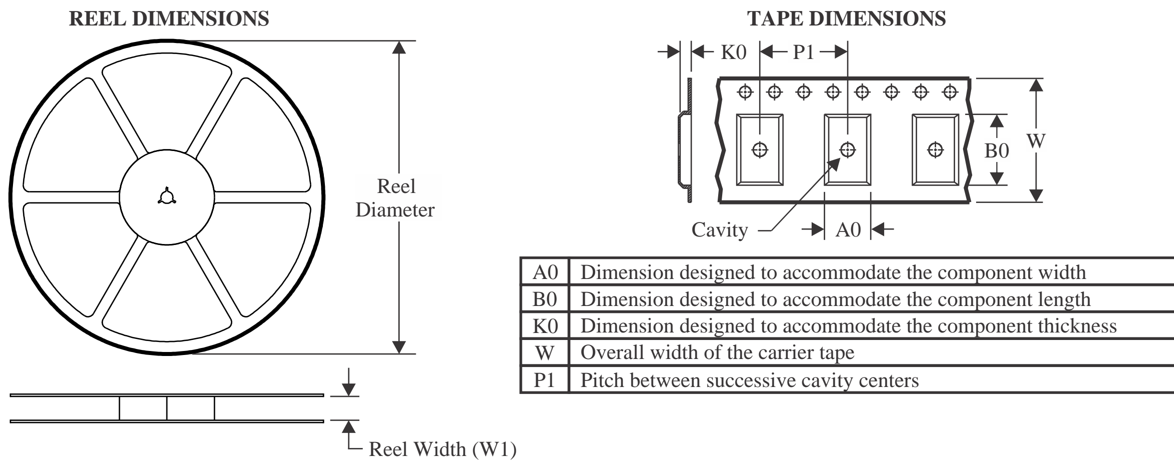
OTHER QUALIFIED VERSIONS OF OPA2313 :

- Automotive : OPA2313-Q1

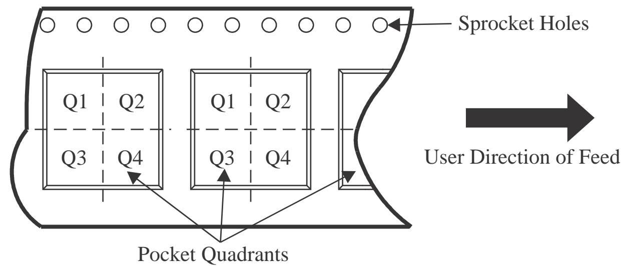
NOTE: Qualified Version Definitions:

- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION



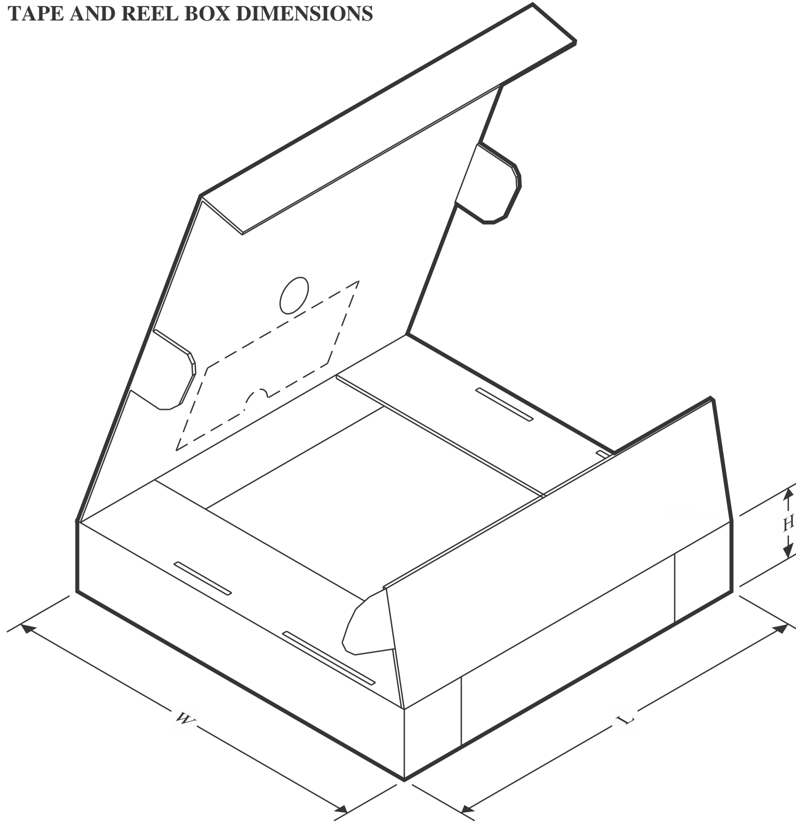
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
OPA2313IDGKR	VSSOP	DGK	8	2500	330.0	12.4	5.25	3.35	1.25	8.0	12.0	Q1
OPA2313IDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
OPA2313IDRGR	SON	DRG	8	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
OPA2313IDRGT	SON	DRG	8	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
OPA313IDBVR	SOT-23	DBV	5	3000	178.0	9.0	3.3	3.2	1.4	4.0	8.0	Q3
OPA313IDBVT	SOT-23	DBV	5	250	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
OPA313IDCKR	SC70	DCK	5	3000	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
OPA4313IPWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

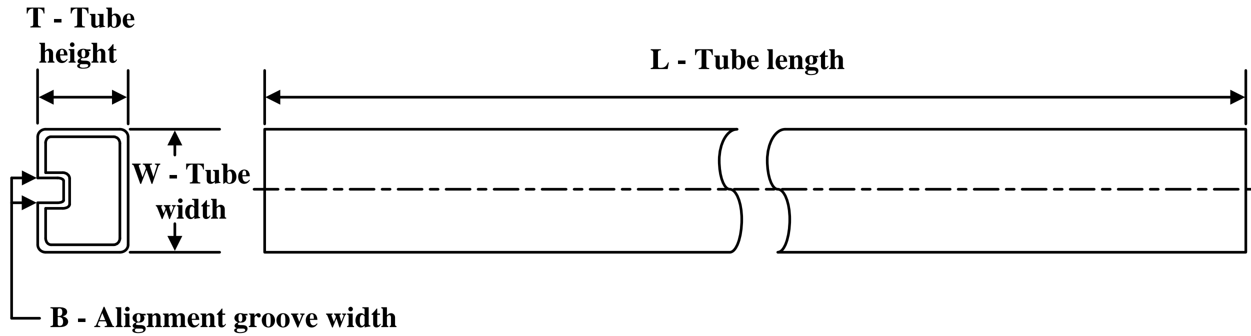
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
OPA2313IDGKR	VSSOP	DGK	8	2500	366.0	364.0	50.0
OPA2313IDR	SOIC	D	8	2500	353.0	353.0	32.0
OPA2313IDRGR	SON	DRG	8	3000	346.0	346.0	33.0
OPA2313IDRGT	SON	DRG	8	250	210.0	185.0	35.0
OPA313IDBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
OPA313IDBVT	SOT-23	DBV	5	250	180.0	180.0	18.0
OPA313IDCKR	SC70	DCK	5	3000	180.0	180.0	18.0
OPA4313IPWR	TSSOP	PW	14	2000	356.0	356.0	35.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
OPA2313ID	D	SOIC	8	75	507	8	3940	4.32
OPA2313IDGK	DGK	VSSOP	8	80	330	6.55	500	2.88
OPA4313IPW	PW	TSSOP	14	90	530	10.2	3600	3.5

C

SEATING PLANE

.004 [0.1] C

.228-.244 TYP
[5.80-6.19]

A

PIN 1 ID AREA

6X .050
[1.27]

1

8

.189-.197
[4.81-5.00]
NOTE 3

2X
.150
[3.81]

4X (0° -15°)

4

5

8X .012-.020
[0.31-0.51]

.010 [0.25] Ⓜ C A B

B

.150-.157
[3.81-3.98]
NOTE 4

.069 MAX
[1.75]

.005-.010 TYP
[0.13-0.25]

4X (0° -15°)

SEE DETAIL A

.010
[0.25]

0° - 8°

.004-.010
[0.11-0.25]

.016-.050
[0.41-1.27]

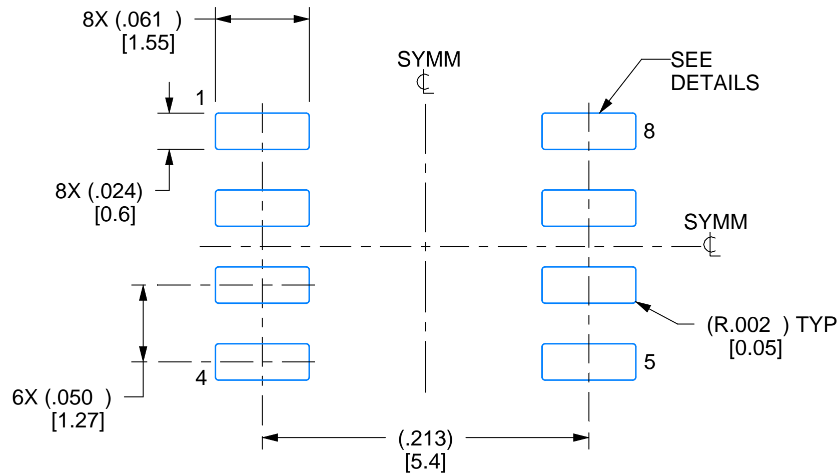
(.041)
[1.04]

DETAIL A
TYPICAL

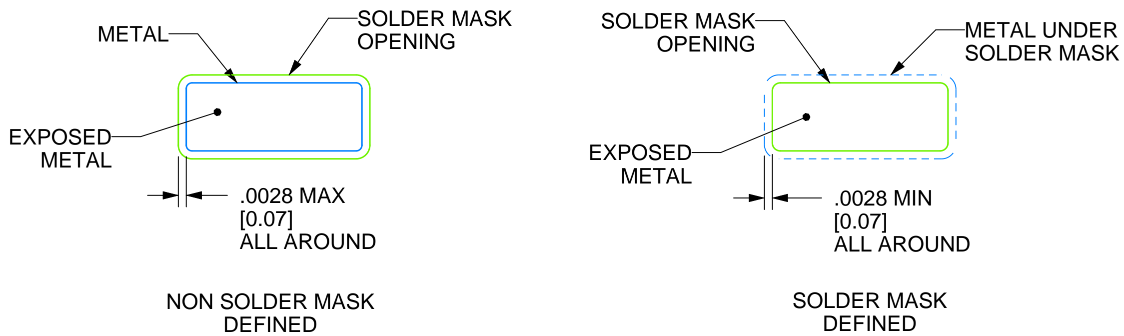
4214825/C 02/2019

NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X

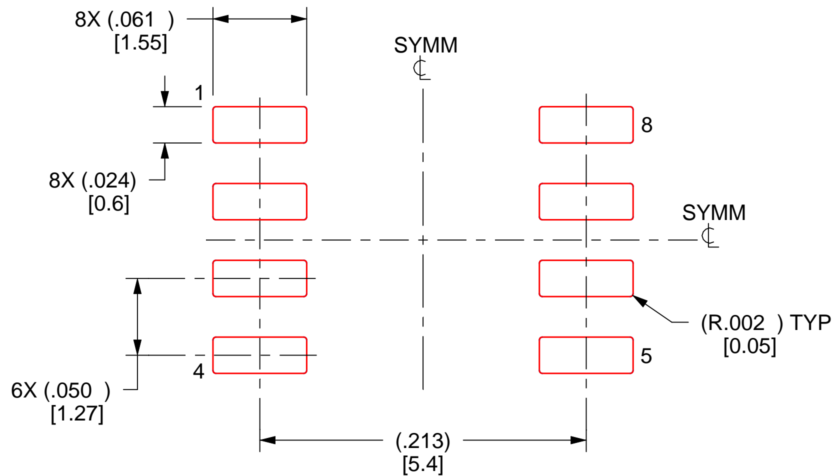


SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PIN 1 INDEX AREA

2.4
1.8

1.4
1.1

B

A

C

0.1 C

1.1 MAX

1 2 3 4 5

2X 0.65

1.3

NOTE 4

(0.15)

(0.1)

1.3

2.15
1.85

5X 0.33
0.15

0.1 Ⓜ C A B

NOTE 5

4X 0°-12°

(0.9)

0.1
0.0 TYP

4X 4°-14°

0.15

GAGE PLANE

0.22
0.08 TYP

8°
0° TYP

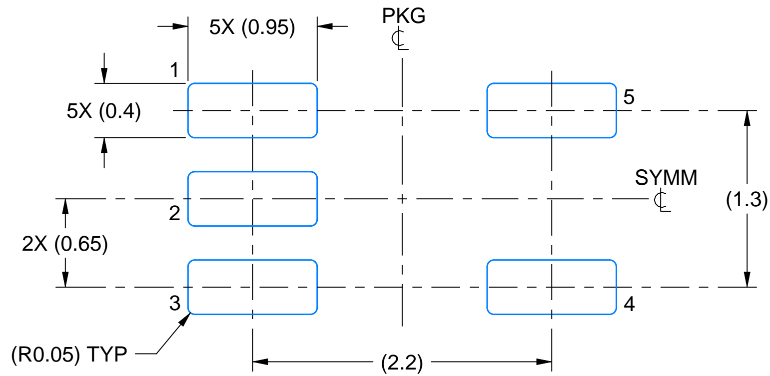
0.46
0.26 TYP

SEATING PLANE

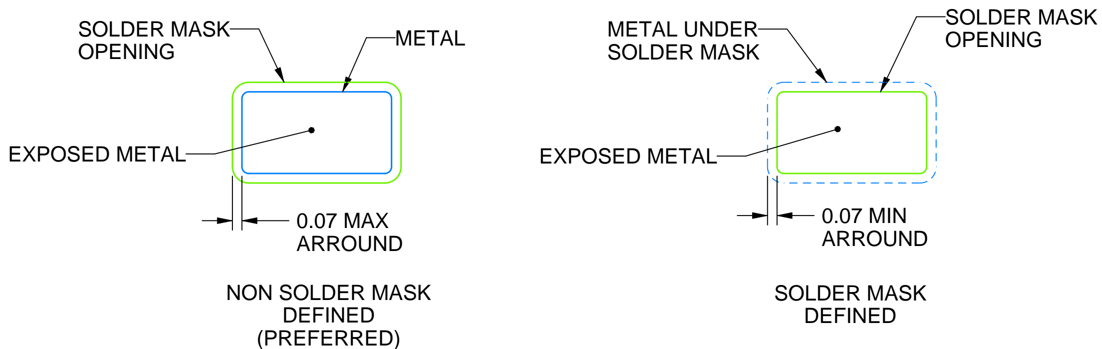
4214834/F 08/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-203.
4. Support pin may differ or may not be present.
5. Lead width does not comply with JEDEC.
6. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25mm per side



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:18X

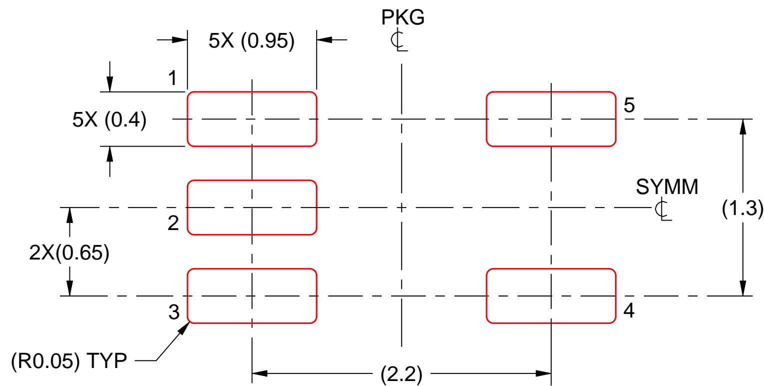


SOLDER MASK DETAILS

4214834/F 08/2024

NOTES: (continued)

7. Publication IPC-7351 may have alternate designs.
8. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



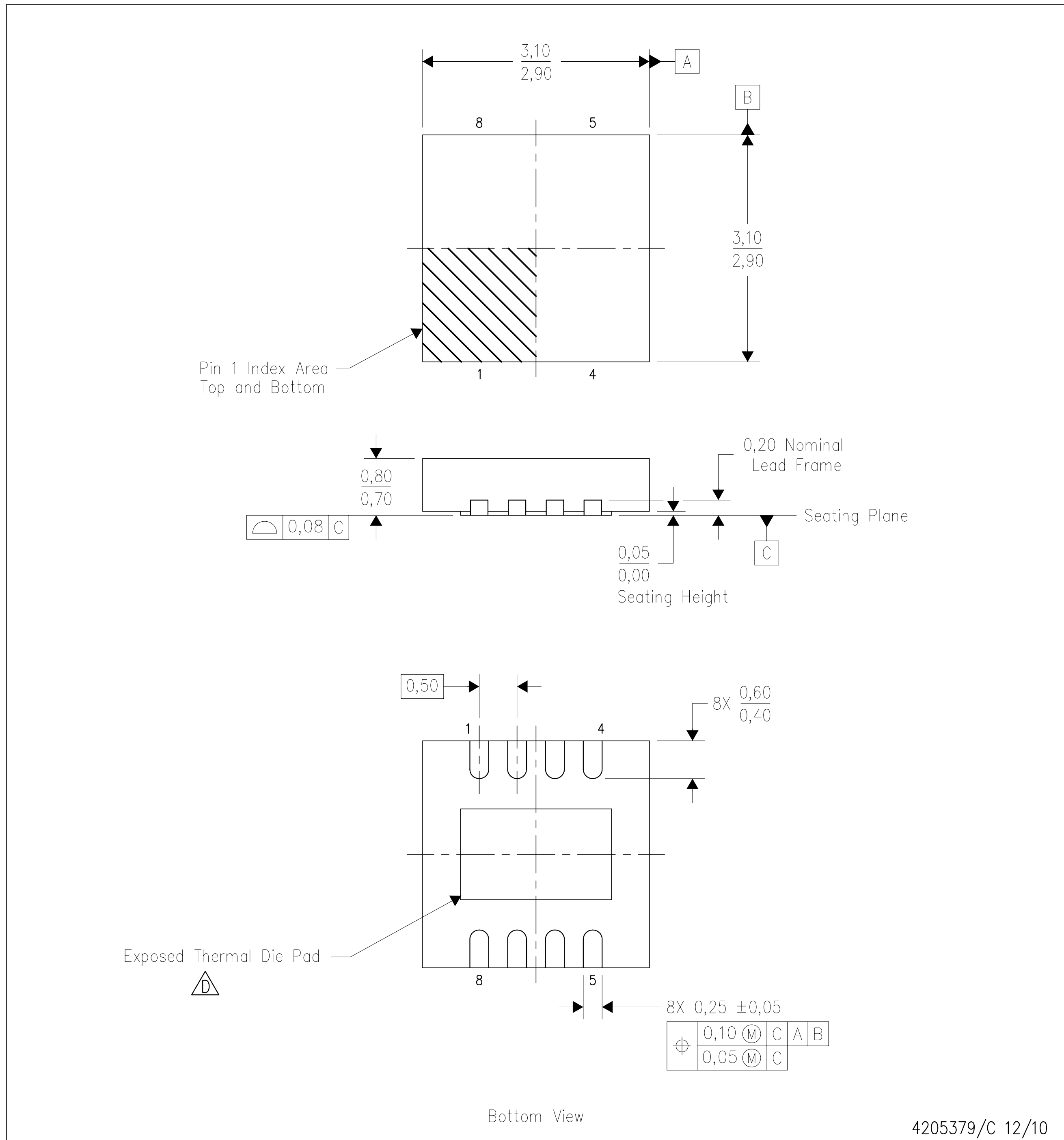
SOLDER PASTE EXAMPLE
BASED ON 0.125 THICK STENCIL
SCALE:18X

4214834/F 08/2024

NOTES: (continued)

9. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
10. Board assembly site may have different recommendations for stencil design.

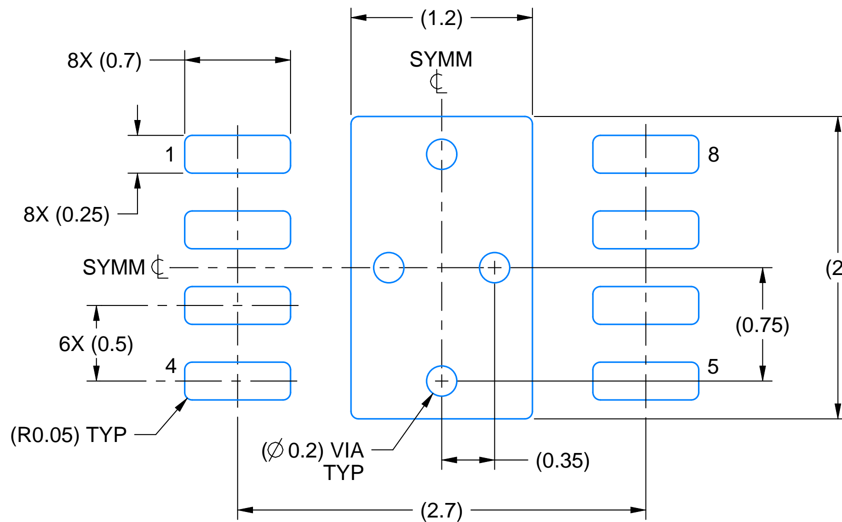
DRG (S-PWSON-N8) PLASTIC SMALL OUTLINE NO-LEAD



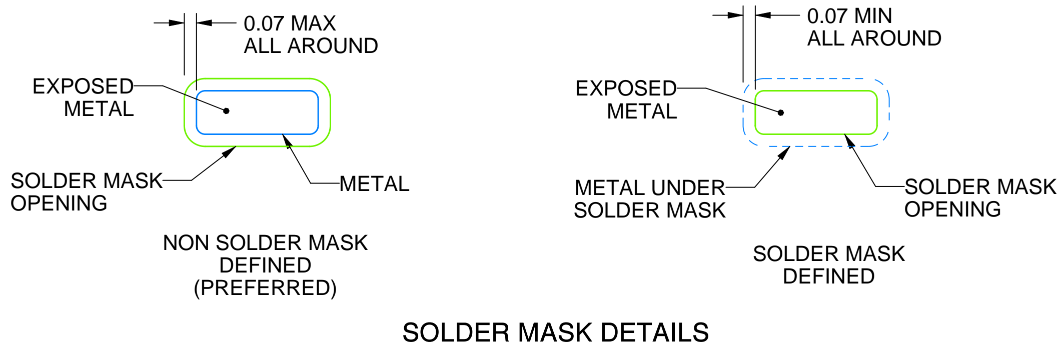
NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
- B. This drawing is subject to change without notice.
- C. SON (Small Outline No–Lead) package configuration.
- D. The package thermal pad must be soldered to the board for thermal and mechanical performance. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.
- E. JEDEC MO–229 package registration pending.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:20X



NON SOLDER MASK DEFINED (PREFERRED)

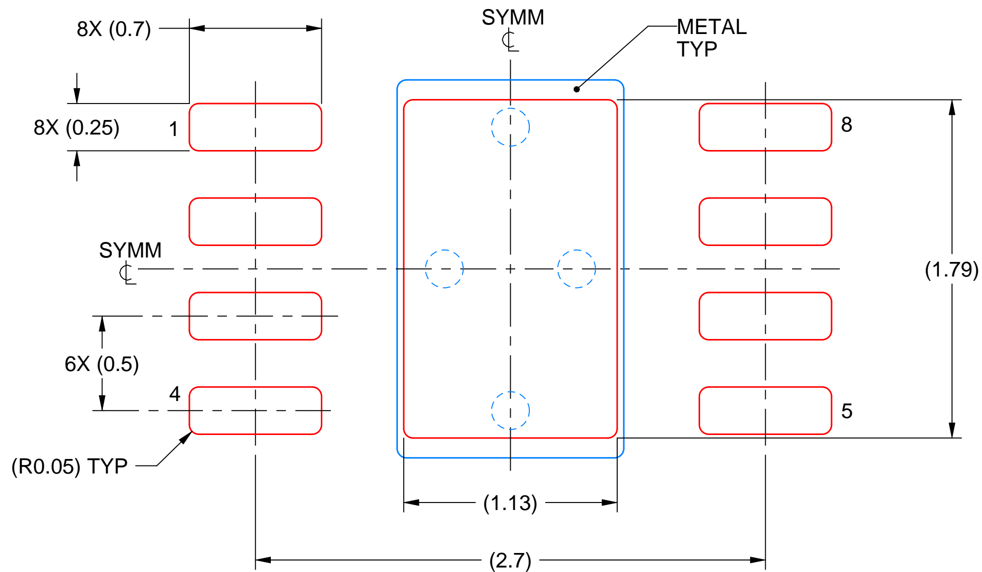
SOLDER MASK DEFINED

SOLDER MASK DETAILS

4218885/A 03/2020

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



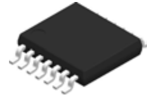
SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
84% PRINTED SOLDER COVERAGE BY AREA
SCALE:25X

4218885/A 03/2020

NOTES: (continued)

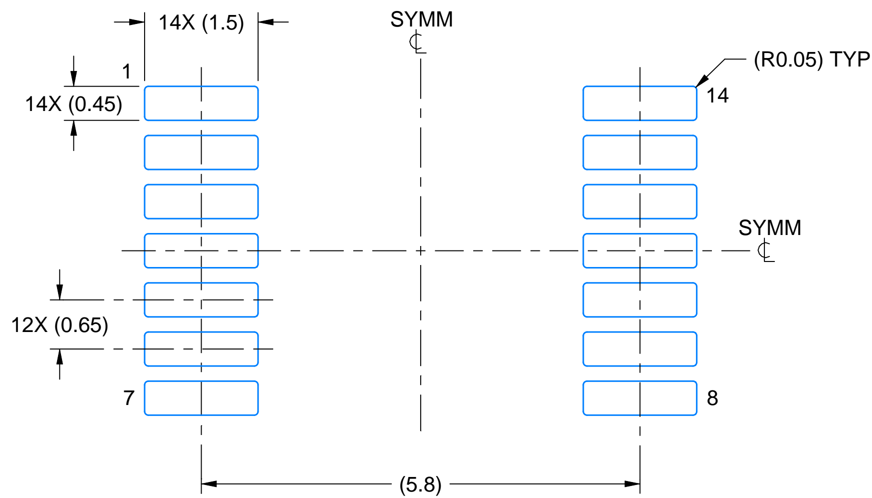
6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.



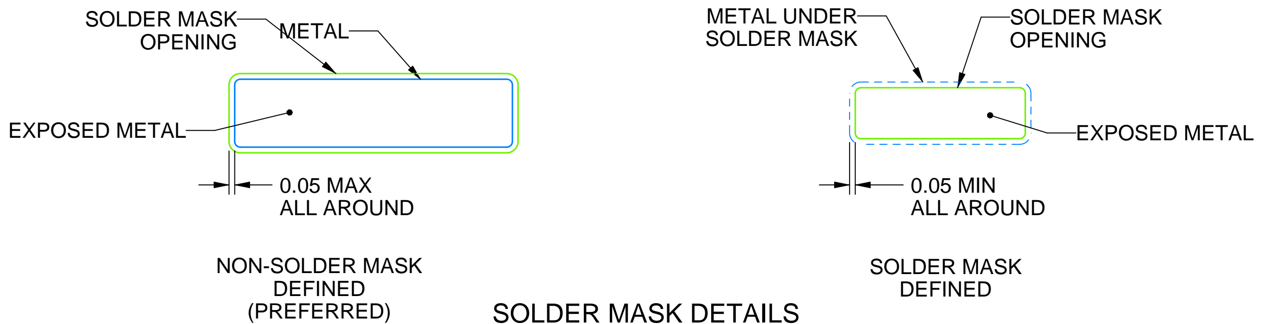
4220202/B 12/2023

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

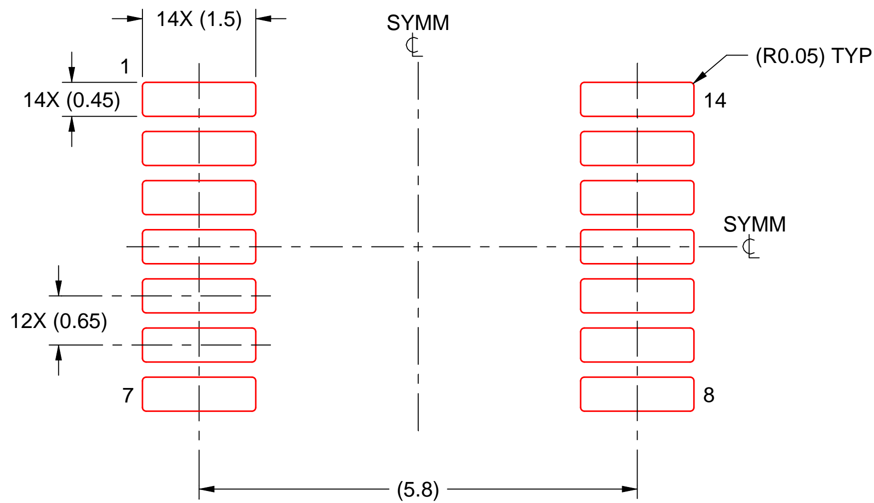


SOLDER MASK DETAILS

4220202/B 12/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220202/B 12/2023

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

3.0
2.6

1.75
1.45

B

A

C

0.1 C

PIN 1
INDEX AREA

1

5

2X 0.95

1.9

2

(0.1)

(0.15)

1.9

3.05
2.75

3

4

5X 0.5
0.3

0.2 Ⓜ C A B

NOTE 5

4X 0° -15°

(1.1)

0.15
0.00 TYP

1.45
0.90

4X 4° -15°

0.25
GAGE PLANE

0.22
0.08 TYP

8°
0° TYP

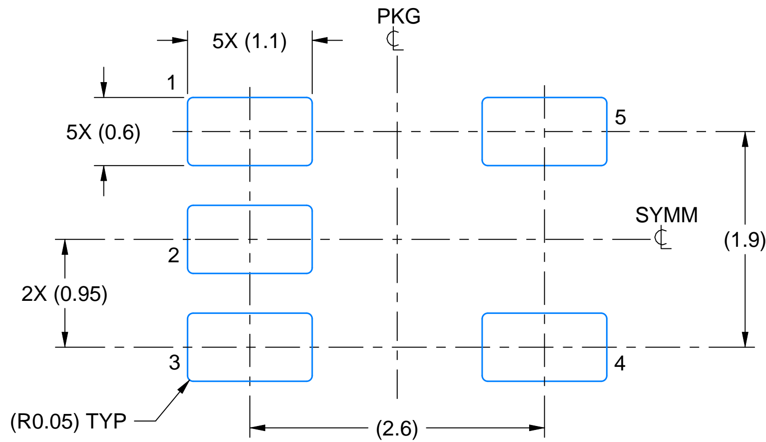
0.6
0.3 TYP

SEATING PLANE

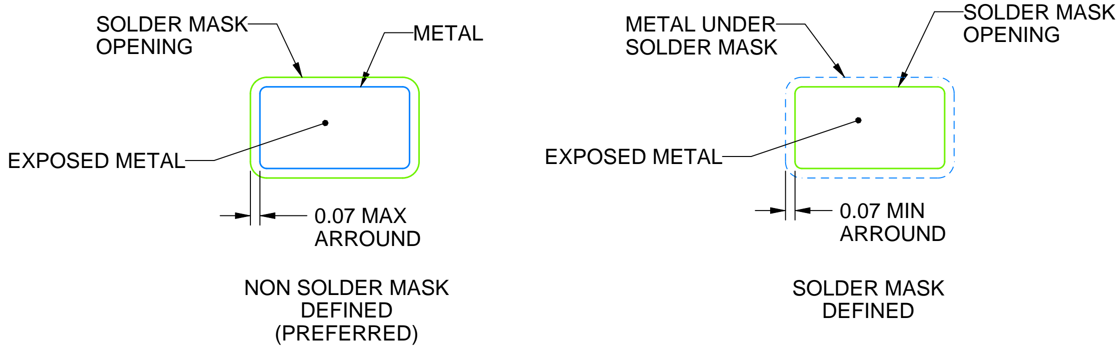
4214839/K 08/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.
5. Support pin may differ or may not be present.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

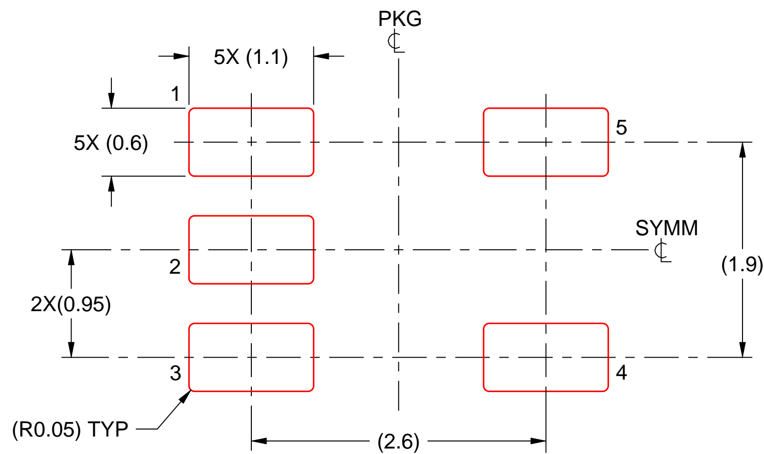


SOLDER MASK DETAILS

4214839/K 08/2024

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214839/K 08/2024

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

A
5.05
4.75 TYP
PIN 1 INDEX AREA
C
0.1 C
SEATING PLANE
1
8
6X 0.65
3.1
2.9
NOTE 3
2X
1.95
4
5
8X 0.38
0.25
0.13 Ⓜ C A B
B
3.1
2.9
NOTE 4

0.23
0.13
SEE DETAIL A

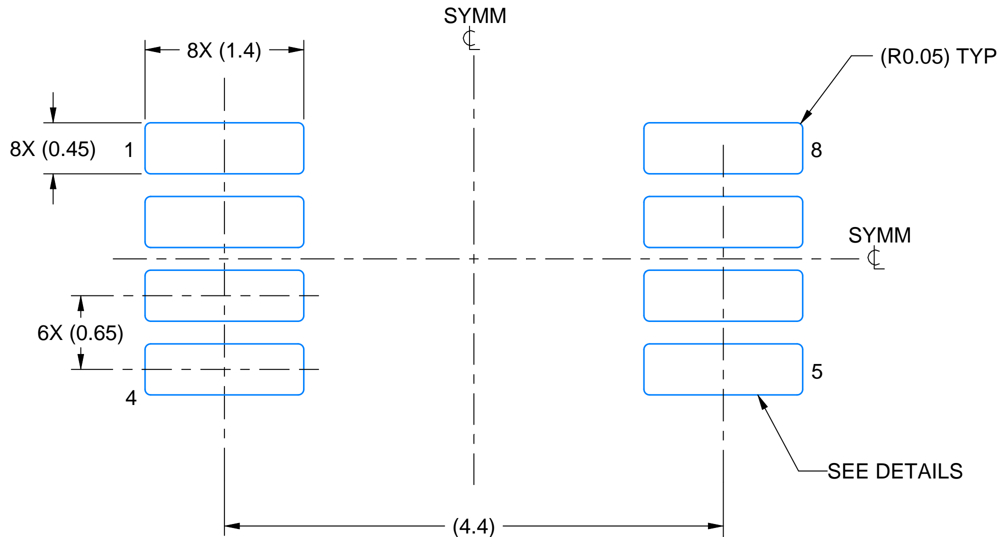
0.25
GAGE PLANE
1.1 MAX
0°-8°
0.7
0.4
0.15
0.05
DETAIL A
TYPICAL

4214862/A 04/2023

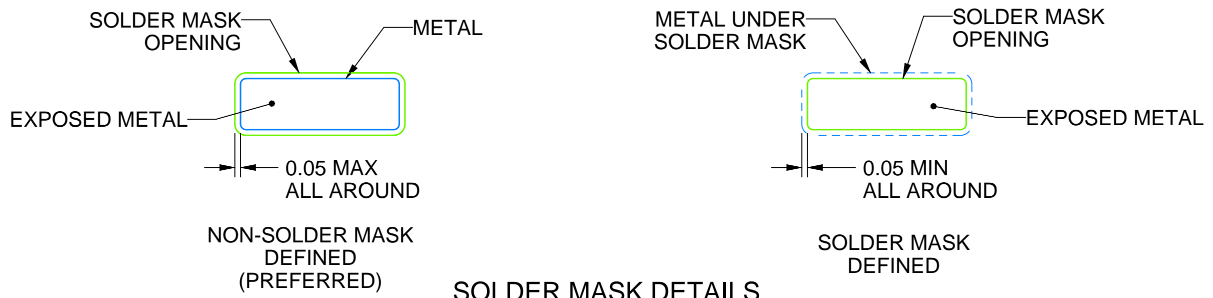
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X



SOLDER MASK DETAILS

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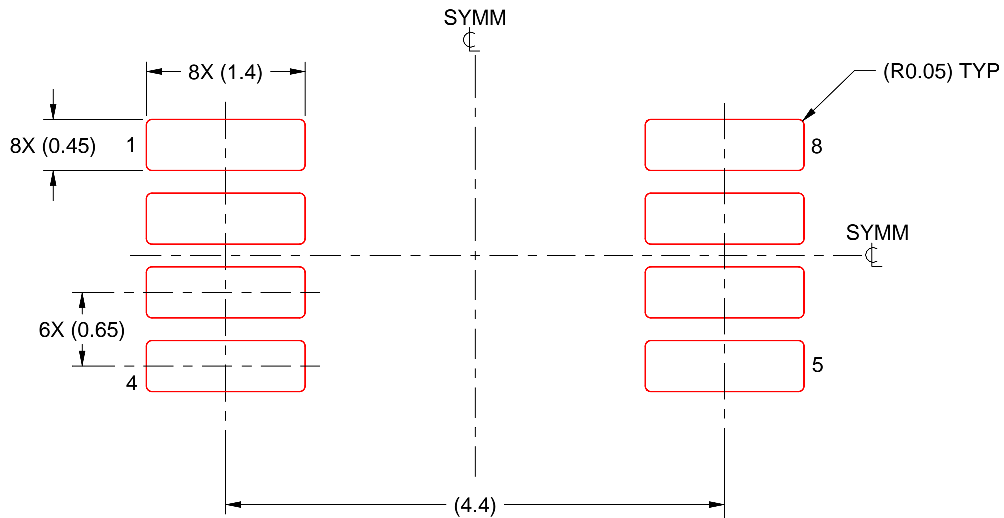
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.



SOLDER PASTE EXAMPLE
SCALE: 15X

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NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

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