

用于 I²C 总线的 PCF8574 远程 8 位 I/O 扩展器

1 特性

- 低待机功耗，最大值为 10 μ A
- I²C 至并行端口扩展器
- 开漏中断输出
- 兼容大多数微控制器
- 具有高电流驱动能力的锁存输出，用于直接驱动 LED
- 闩锁性能超过 100mA，符合 JESD 78 II 类规范的要求

2 应用

- 电信方舱：滤波器单元
- 服务器
- 路由器（电信交换设备）
- 个人计算机
- 个人电子产品
- 工业自动化
- 采用 GPIO 受限处理器的产品

3 说明

这款面向两线制双向总线 (I²C) 的 8 位输入/输出 (I/O) 扩展器设计为在 2.5V 至 6V V_{CC} 下运行。

PCF8574 器件通过 I²C 接口 [串行时钟 (SCL)、串行数据 (SDA)] 为大多数微控制器系列提供通用远程 I/O 扩展。

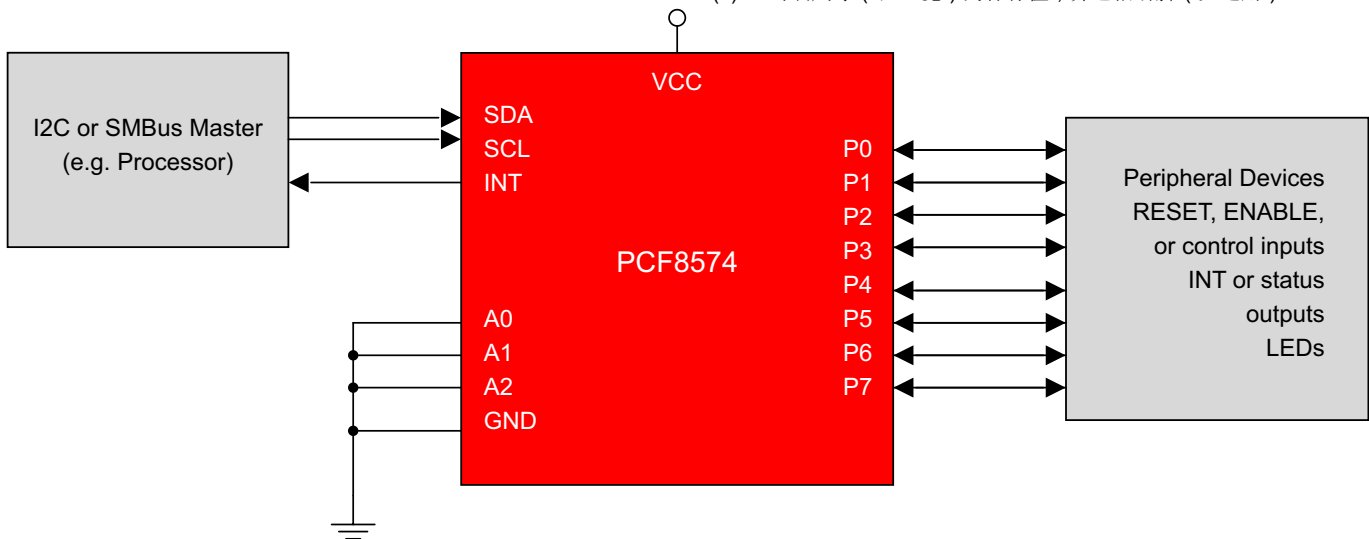
该器件具有一个 8 位准双向 I/O 端口 (P0 - P7)，其中包括具有高电流驱动能力的锁存输出，用于直接驱动 LED。每个准双向 I/O 都可以用作输入或输出（无需使用数据方向控制信号）。在上电时，这些 I/O 处于高电平。在该模式下，仅有一个连接到 V_{CC} 的电流源处于活动状态。

封装信息

器件型号	封装 ⁽¹⁾	封装尺寸 ⁽²⁾
PCF8574	TVSOP (DGV, 20)	5mm × 6.40mm
	SOIC (DW, 16)	10.3mm × 10.3mm
	PDIP (N, 16)	19.3mm × 9.4mm
	TSSOP (PW, 20)	6.5mm × 6.4mm
	VQFN (RGT, 16)	3mm × 3mm
	VQFN (RGY, 20)	4.5mm × 3.5mm

(1) 有关更多信息，请参阅节 11。

(2) 封装尺寸（长 × 宽）为标称值，并包括引脚（如适用）。



简化原理图



Table of Contents

1 特性	1	7.3 Feature Description.....	14
2 应用	1	7.4 Device Functional Modes.....	15
3 说明	1	8 Application and Implementation	17
4 Pin Configuration and Functions	3	8.1 Application Information.....	17
5 Specifications	4	8.2 Typical Application.....	17
5.1 Absolute Maximum Ratings.....	4	8.3 Power Supply Recommendations.....	19
5.2 ESD Ratings.....	4	8.4 Layout.....	21
5.3 Recommended Operating Conditions.....	4	9 Device and Documentation Support	23
5.4 Thermal Information.....	4	9.1 Documentation Support.....	23
5.5 Electrical Characteristics.....	6	9.2 Receiving Notification of Documentation Updates....	23
5.6 I ² C Interface Timing Requirements.....	6	9.3 支持资源.....	23
5.7 Switching Characteristics.....	7	9.4 Trademarks.....	23
5.8 Typical Characteristics.....	8	9.5 静电放电警告.....	23
6 Parameter Measurement Information	10	9.6 术语表.....	23
7 Detailed Description	13	10 Revision History	23
7.1 Overview.....	13	11 Mechanical, Packaging, and Orderable Information	24
7.2 Functional Block Diagram.....	13		

4 Pin Configuration and Functions

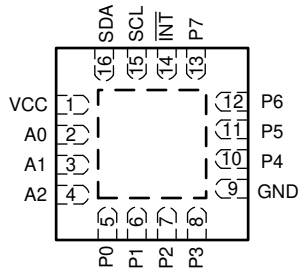


图 4-1. RGT Package, 16 Pins (Top View)

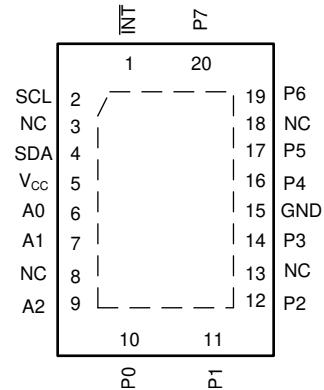


图 4-2. RGY Package, 20 Pins (Top View)

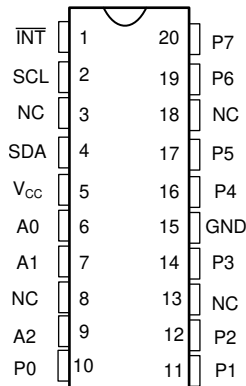


图 4-3. DGV or PW Package, 20 Pins (Top View)

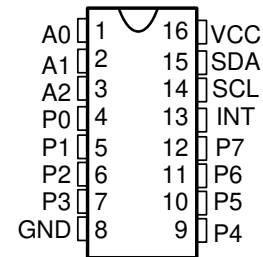


图 4-4. DW or N Package, 20 Pins, Top View

表 4-1. Pin Functions

NAME	PIN				TYPE	DESCRIPTION
	RGT	RGY	DGV or PW	DW or N		
A [0..2]	2, 3, 4	6, 7, 9	6, 7, 9	1, 2, 3	I	Address inputs 0 through 2. Connect directly to V _{CC} or ground. Pullup resistors are not needed.
GND	9	15	15	8	—	Ground
INT	14	1	1	13	O	Interrupt output. Connect to V _{CC} through a pullup resistor.
NC	-	3, 8, 13, 18	3, 8, 13, 18	-	—	Do not connect
P[0..7]	5, 6, 7, 8, 10, 11, 12, 13	10, 11, 12, 14, 16, 17, 19, 20	10, 11, 12, 14, 16, 17, 19, 20	4, 5, 6, 7, 9, 10, 11, 12	I/O	P-port input/output. Push-pull design structure.
SCL	15	2	2	14	I	Serial clock line. Connect to V _{CC} through a pullup resistor
SDA	16	4	4	15	I/O	Serial data line. Connect to V _{CC} through a pullup resistor.
V _{CC}	1	5	5	16	—	Voltage supply

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

		MIN	MAX	UNIT
V _{CC}	Supply voltage range	- 0.5	6.5	V
V _I	Input voltage range ⁽²⁾	- 0.5	V _{CC} + 0.5	V
V _O	Output voltage range ⁽²⁾	- 0.5	V _{CC} + 0.5	V
I _{IK}	Input clamp current	V _I < 0	- 20	mA
I _{OK}	Output clamp current	V _O < 0	- 20	mA
I _{OK}	Input/output clamp current	V _O < 0 or V _O > V _{CC}	±400	μA
I _{OL}	Continuous output low current	V _O = 0 to V _{CC}	50	mA
I _{OH}	Continuous output high current	V _O = 0 to V _{CC}	- 4	mA
	Continuous current through V _{CC} or GND		±100	mA
T _J	Junction temperature		150	°C
T _{stg}	Storage temperature range	- 65	150	°C

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under [Section 5.3](#) is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.

5.2 ESD Ratings

			VALUE	UNIT
V _(ESD)	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾	1500	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101 ⁽²⁾	2000	

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 500-V HBM is possible with the necessary precautions.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 250-V CDM is possible with the necessary precautions.

5.3 Recommended Operating Conditions

		MIN	MAX	UNIT
V _{CC}	Supply voltage	2.5	6	V
V _{IH}	High-level input voltage	0.7 × V _{CC}	V _{CC} + 0.5	V
V _{IL}	Low-level input voltage	- 0.5	0.3 × V _{CC}	V
I _{OH}	High-level output current		- 1	mA
I _{OL}	Low-level output current		25	mA
T _A	Operating free-air temperature	- 40	85	°C

5.4 Thermal Information

THERMAL METRIC ⁽¹⁾		PCF8574						UNIT
		DGV	DW	N	PW	RGT	RGY	
		20 PINS	16 PINS	16 PINS	20 PINS	16 PINS	20 PINS	
R _{θJA}	Junction-to-ambient thermal resistance	92	76.7	73.1	94.8	56.0	52.2	°C/W
R _{θJC(top)}	Junction-to-case (top) thermal resistance	-	45.1	51.9	40.2	67.4	50.6	°C/W
R _{θJB}	Junction-to-board thermal resistance	-	45.8	48.3	58.5	31.2	29.2	°C/W
ψ _{JT}	Junction-to-top characterization parameter	-	17.2	29.8	2.8	3.9	3.3	°C/W
ψ _{JB}	Junction-to-board characterization parameter	-	45.2	47.9	58.0	31.1	29.1	°C/W

THERMAL METRIC ⁽¹⁾		PCF8574						UNIT
		DGV	DW	N	PW	RGT	RGY	
		20 PINS	16 PINS	16 PINS	20 PINS	16 PINS	20 PINS	
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	-	n/a	n/a	n/a	15.1	16.0	°C/W

- (1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC package thermal metrics application report](#).

5.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

		TEST CONDITIONS	VCC	MIN	TYP ⁽¹⁾	MAX	UNIT
V _{IK}	Input diode clamp voltage	I _I = -18 mA	2.5 V to 6 V	-1.2			V
V _{POR}	Power-on reset voltage	V _I = V _{CC} or GND, I _O = 0	6 V		1.3	2.4	V
I _{OH}	P port	V _O = GND	2.5 V to 6 V	-310		-30	μA
I _{OHT}	P port transient pullup current	High during acknowledge, V _{OH} = GND	2.5 V		-1		mA
I _{OL}	SDA	V _O = 0.4 V	2.5 V to 6 V		3		mA
	P port	V _O = 1 V	5 V		10	25	
	INT	V _O = 0.4 V	2.5 V to 6 V		1.6		
I _I	SCL, SDA	V _I = V _{CC} or GND	2.5 V to 6 V			±5	μA
	INT					±5	
	A0, A1, A2					±5	
I _{IHL}	P port	-250mV < V _i < GND	2.5 V to 6 V			±400	μA
I _{CC}	Operating mode	V _I = V _{CC} or GND, I _O = 0, f _{SCL} = 100 kHz	6 V		40	100	μA
	Standby mode	V _I = V _{CC} or GND, I _O = 0			2.5	10	
C _i	SCL	V _I = V _{CC} or GND	2.5 V to 6 V		1.5	7	pF
C _{io}	SDA	V _{IO} = V _{CC} or GND	2.5 V to 6 V		3	7	pF
	P port				4	10	

(1) All typical values are at V_{CC} = 5 V, T_A = 25°C.

5.6 I²C Interface Timing Requirements

over recommended operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
f _{scl}	I ² C clock frequency		100	kHz
t _{sch}	I ² C clock high time	4		μs
t _{scl}	I ² C clock low time	4.7		μs
t _{sp}	I ² C spike time		70	ns
t _{eds}	I ² C serial data setup time	250		ns
t _{sdh}	I ² C serial data hold time	0		ns
t _{icr}	I ² C input rise time		1	μs
t _{icf}	I ² C input fall time		0.3	μs
t _{ocf}	I ² C output fall time (10-pF to 400-pF bus)		300	ns
t _{buf}	I ² C bus free time between stop and start	4.7		μs
t _{sts}	I ² C start or repeated start condition setup	4.7		μs
t _{sth}	I ² C start or repeated start condition hold	4		μs
t _{sps}	I ² C stop condition setup	4		μs
t _{vd}	Valid data time		3.4	μs
C _b	I ² C bus capacitive load		400	pF

5.7 Switching Characteristics

over recommended operating free-air temperature range, $C_L \leq 100$ pF (unless otherwise noted)

PARAMETER		FROM (INPUT)	TO (OUTPUT)	MIN	MAX	UNIT
t_{pv}	Output data valid	SCL	P port		4	μ s
t_{su}	Input data setup time	P port	SCL	0		μ s
t_h	Input data hold time	P port	SCL	4		μ s
t_{iv}	Interrupt valid time	P port	INT		4	μ s
t_{ir}	Interrupt reset delay time	SCL	INT		4	μ s

5.8 Typical Characteristics

$T_A = 25^\circ\text{C}$ (unless otherwise noted)

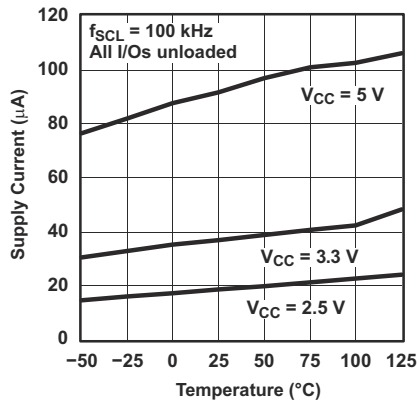


图 5-1. Supply Current vs Temperature

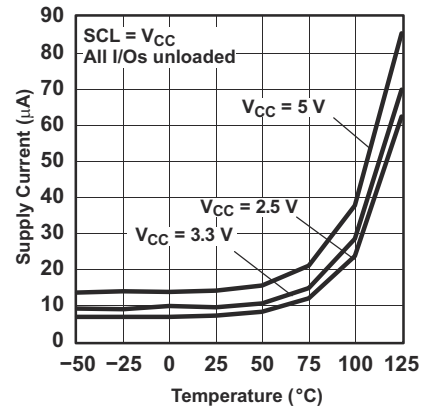


图 5-2. Standby Supply Current vs Temperature

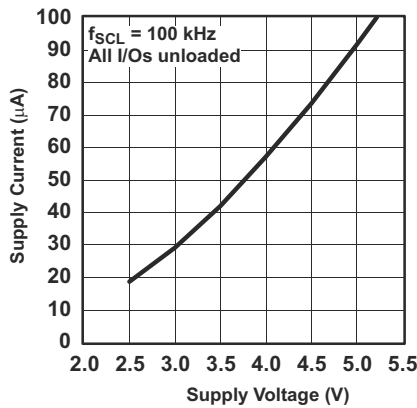


图 5-3. Supply Current vs Supply Voltage

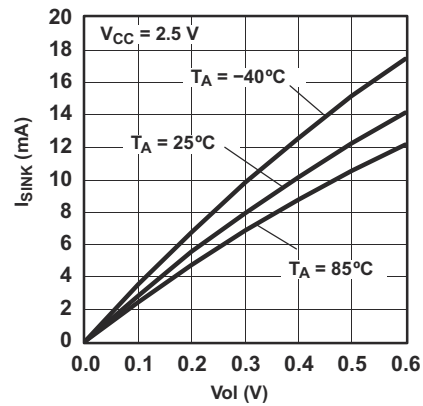


图 5-4. I/O Sink Current vs Output Low Voltage

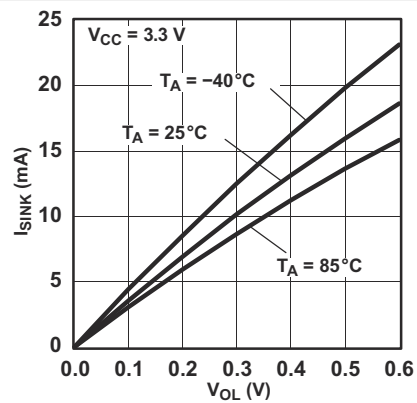


图 5-5. I/O Sink Current vs Output Low Voltage

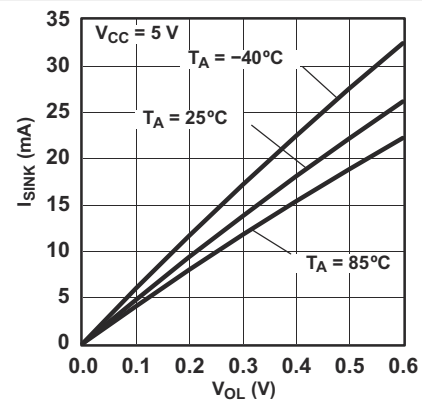


图 5-6. I/O Sink Current vs Output Low Voltage

5.8 Typical Characteristics (continued)

$T_A = 25^\circ\text{C}$ (unless otherwise noted)

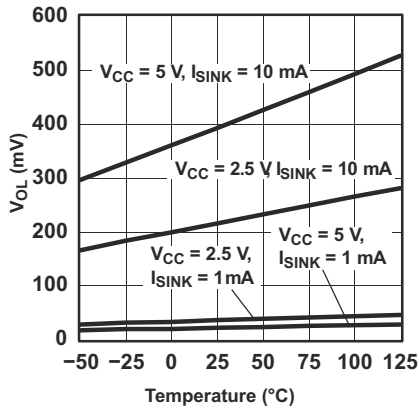


图 5-7. I/O Output Low Voltage vs Temperature

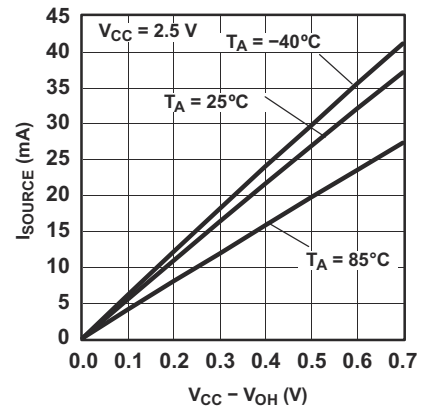


图 5-8. I/O Source Current vs Output High Voltage

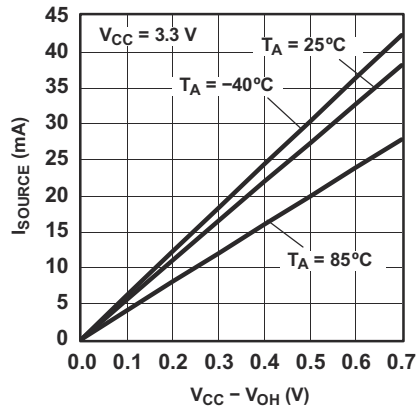


图 5-9. I/O Source Current vs Output High Voltage

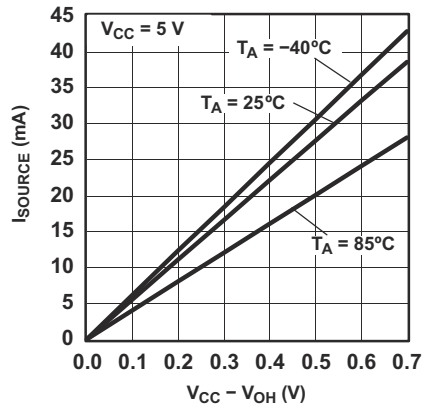


图 5-10. I/O Source Current vs Output High Voltage

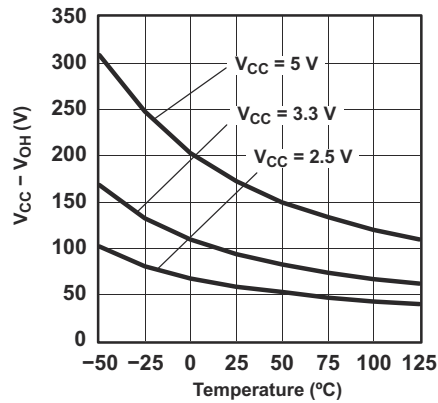


图 5-11. I/O High Voltage vs Temperature

6 Parameter Measurement Information

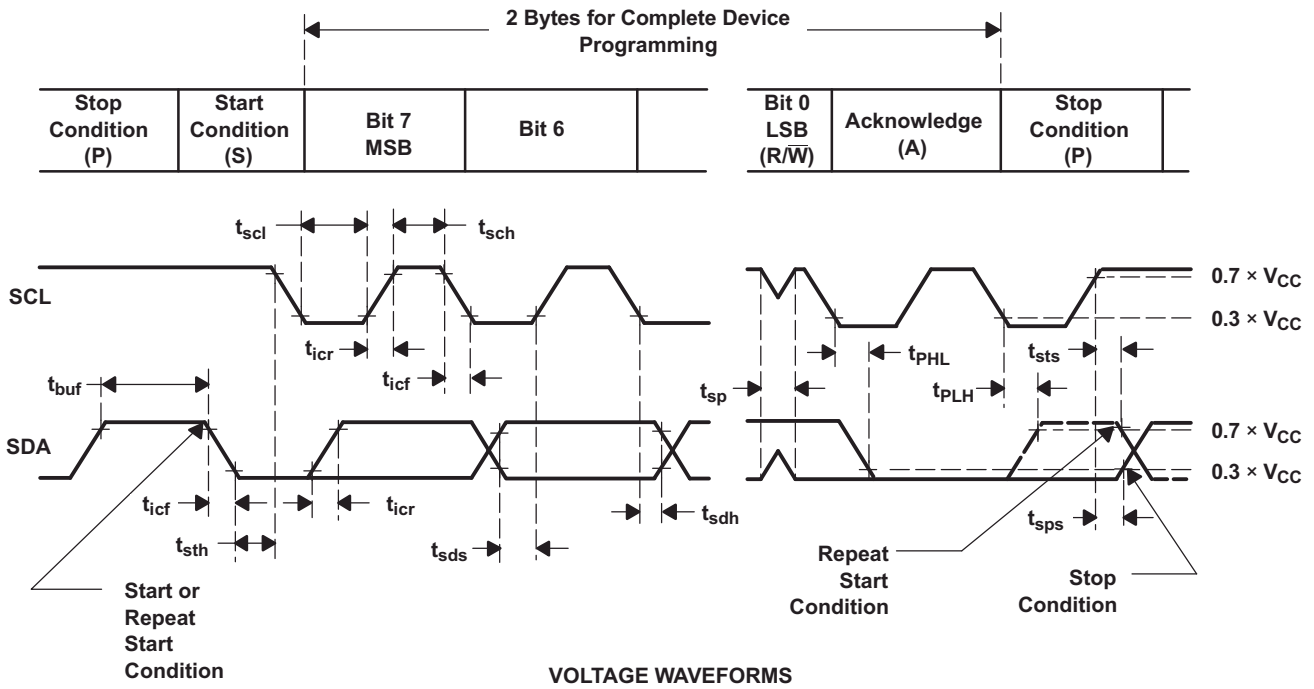
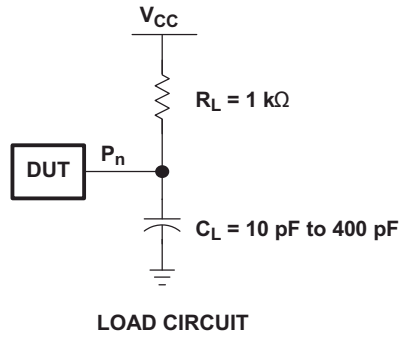


图 6-1. I²C Interface Load Circuit and Voltage Waveforms

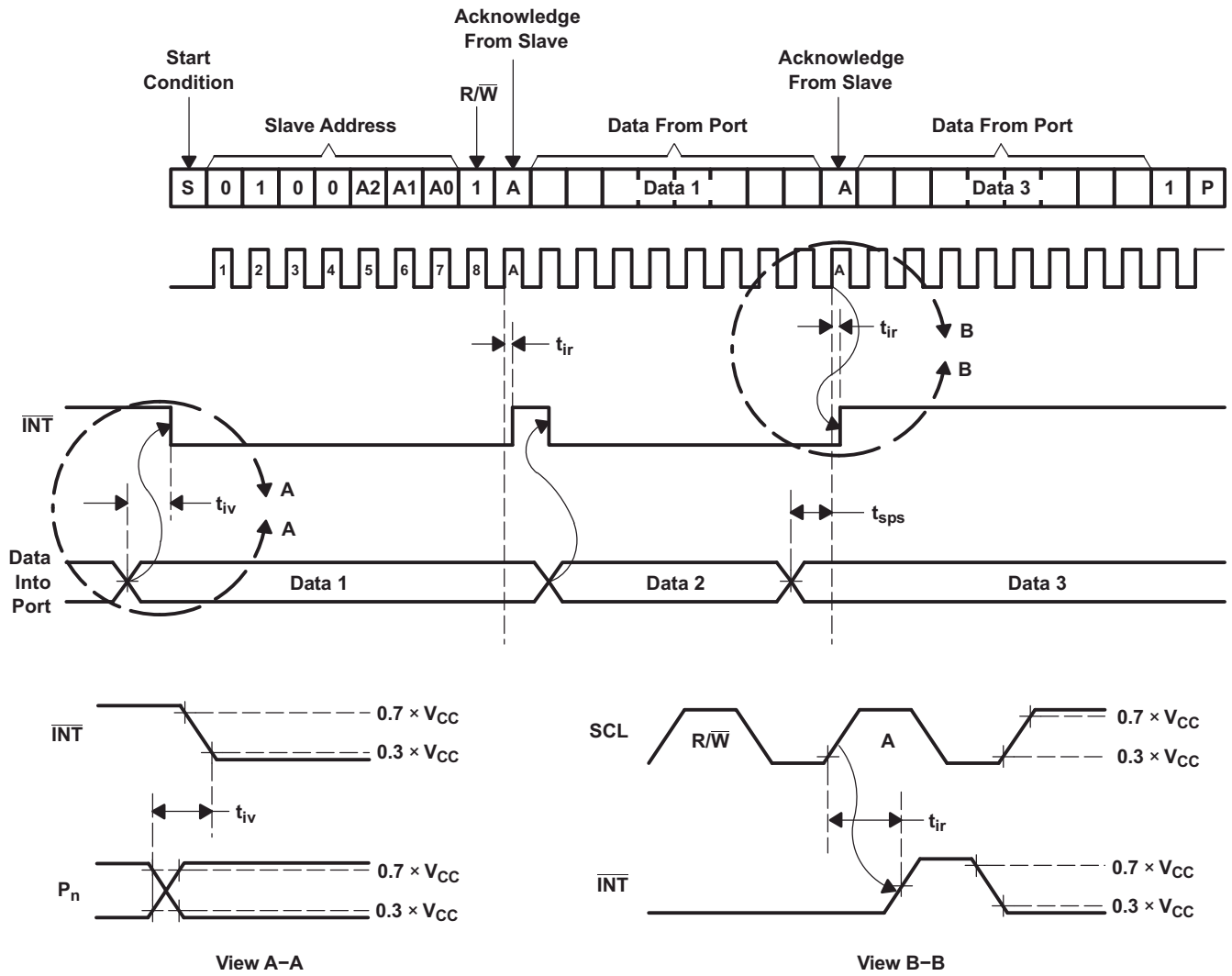


图 6-2. Interrupt Voltage Waveforms

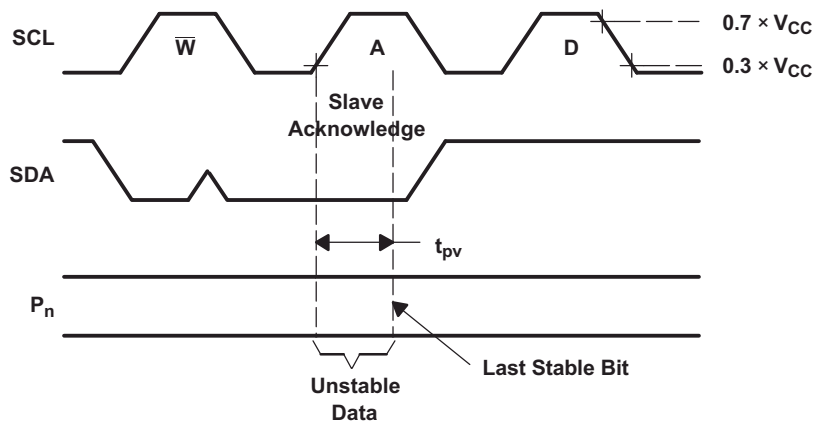


图 6-3. I²C Write Voltage Waveforms

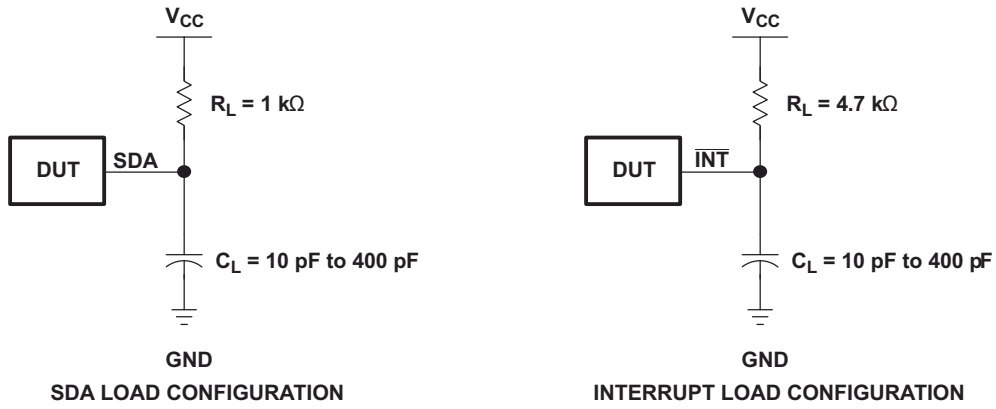


图 6-4. Load Circuits

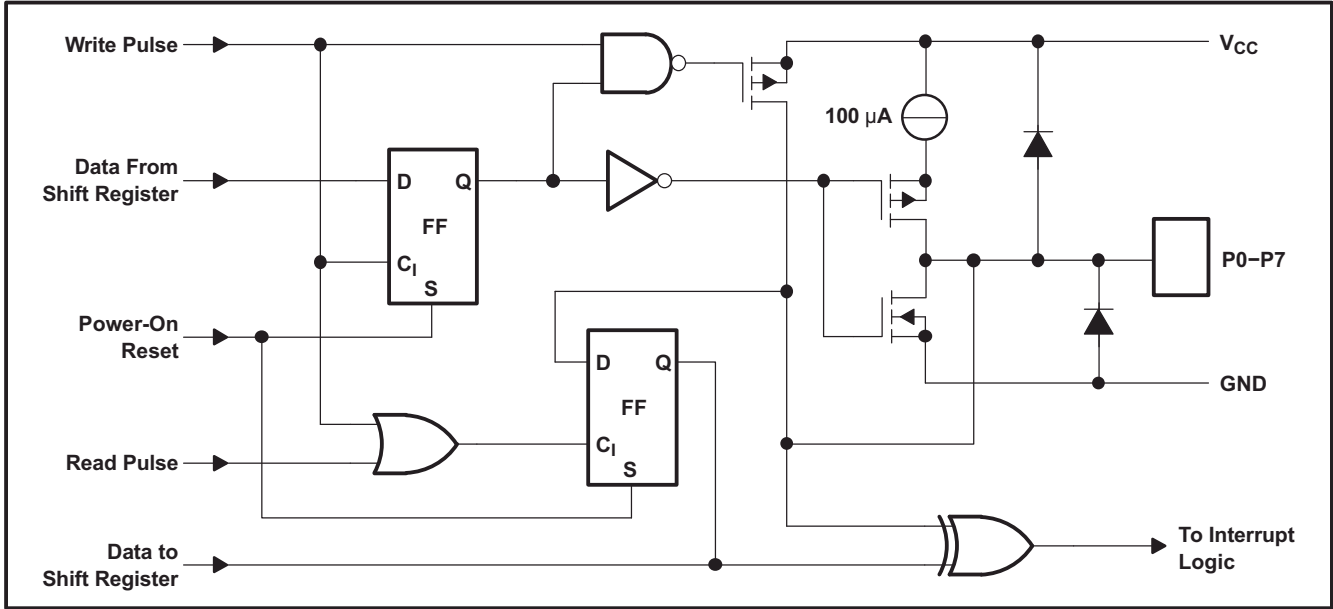


图 7-2. Simplified Schematic Diagram of Each P-Port Input or Output

7.3 Feature Description

7.3.1 I²C Interface

I²C communication with this device is initiated by a controller sending a start condition, a high-to-low transition on the SDA I/O while the SCL input is high. After the start condition, the device address byte is sent, most-significant bit (MSB) first, including the data direction bit (R/\bar{W}). This device does not respond to the general call address. After receiving the valid address byte, this device responds with an acknowledge, a low on the SDA I/O during the high of the acknowledge-related clock pulse. The address inputs (A0 - A2) of the target device must not be changed between the start and the stop conditions.

The data byte follows the address acknowledge. If the R/\bar{W} bit is high, the data from this device are the values read from the P port. If the R/\bar{W} bit is low, the data are from the controller, to be output to the P port. The data byte is followed by an acknowledge sent from this device. If other data bytes are sent from the controller, following the acknowledge, they are ignored by this device. Data are output only if complete bytes are received and acknowledged. The output data will be valid at time, t_{pv} , after the low-to-high transition of SCL and during the clock cycle for the acknowledge.

A stop condition, which is a low-to-high transition on the SDA I/O while the SCL input is high, is sent by the controller.

7.3.2 Interface Definition

BYTE	BIT							
	7 (MSB)	6	5	4	3	2	1	0 (LSB)
I ² C target address	L	H	L	L	A2	A1	A0	R/\bar{W}
I/O data bus	P7	P6	P5	P4	P3	P2	P1	P0

7.3.3 Address Reference

INPUTS			I ² C BUS TARGET 8-BIT READ ADDRESS	I ² C BUS TARGET 8-BIT WRITE ADDRESS
A2	A1	A0		
L	L	L	65 (decimal), 41 (hexadecimal)	64 (decimal), 40 (hexadecimal)
L	L	H	67 (decimal), 43 (hexadecimal)	66 (decimal), 42 (hexadecimal)
L	H	L	69 (decimal), 45 (hexadecimal)	68 (decimal), 44 (hexadecimal)
L	H	H	71 (decimal), 47 (hexadecimal)	70 (decimal), 46 (hexadecimal)
H	L	L	73 (decimal), 49 (hexadecimal)	72 (decimal), 48 (hexadecimal)
H	L	H	75 (decimal), 4B (hexadecimal)	74 (decimal), 4A (hexadecimal)
H	H	L	77 (decimal), 4D (hexadecimal)	76 (decimal), 4C (hexadecimal)
H	H	H	79 (decimal), 4F (hexadecimal)	78 (decimal), 4E (hexadecimal)

7.4 Device Functional Modes

图 7-3 和 图 7-4 显示写和读模式的地址和时序图，分别。

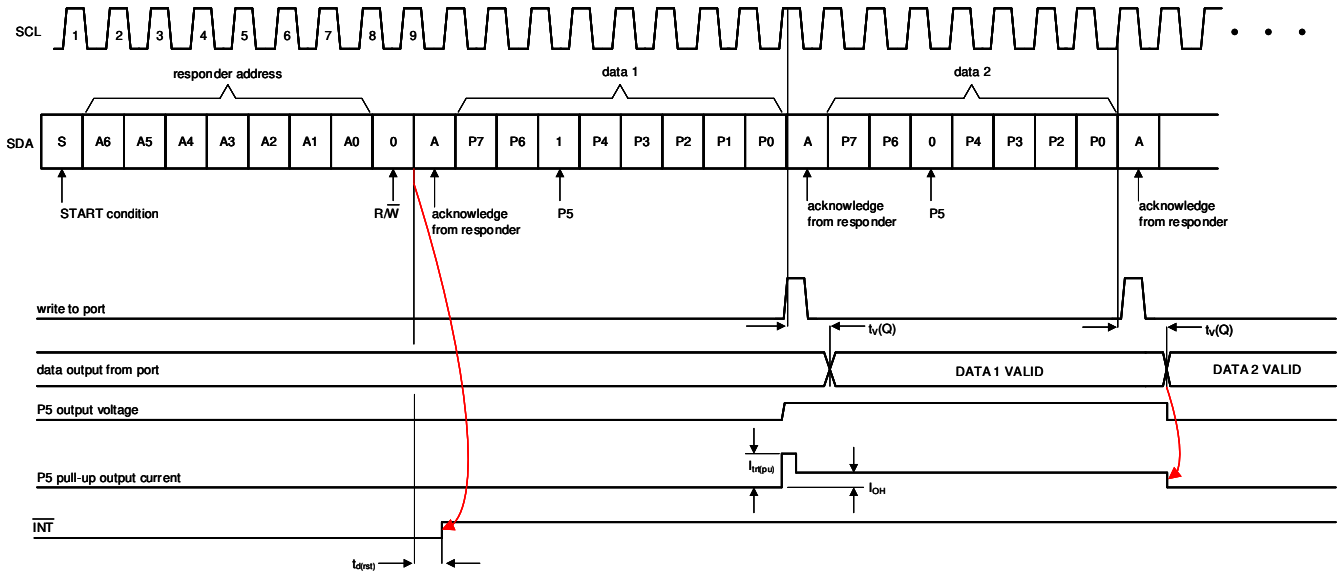
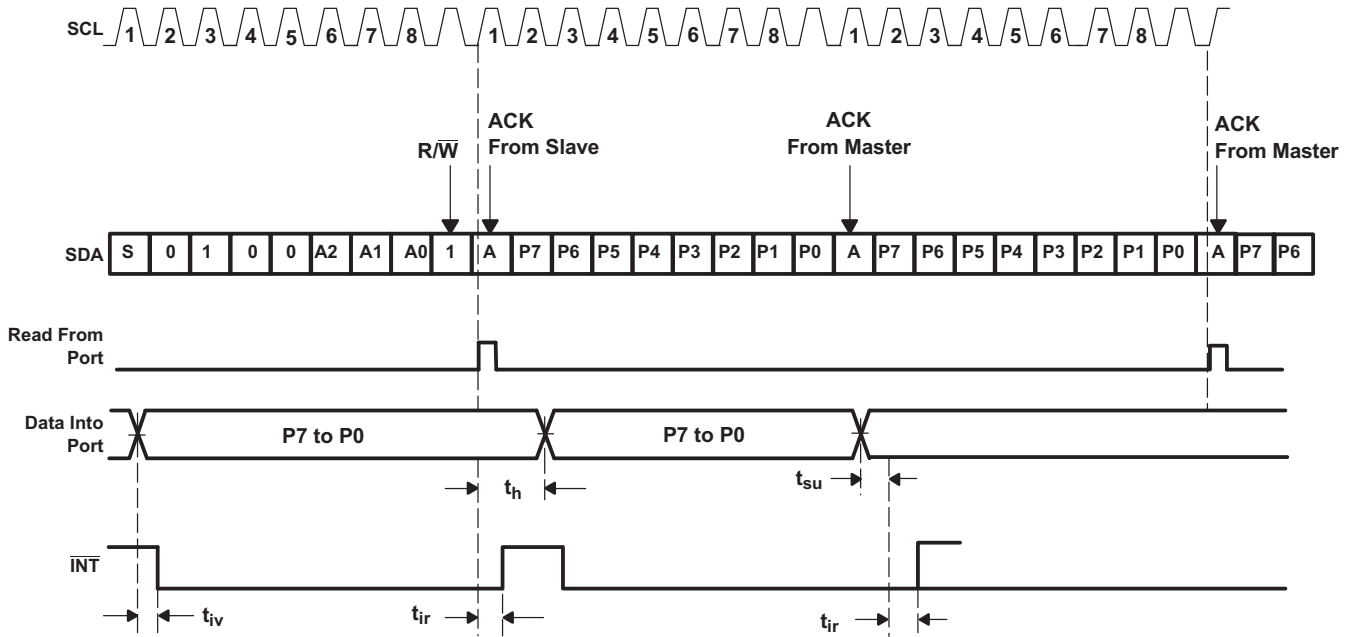


图 7-3. Write Mode (Output)



- A. A low-to-high transition of SDA while SCL is high is defined as the stop condition (P). The transfer of data can be stopped at any moment by a stop condition. When this occurs, data present at the latest ACK phase is valid (output mode). Input data is lost.

图 7-4. Read Mode (Input)

8 Application and Implementation

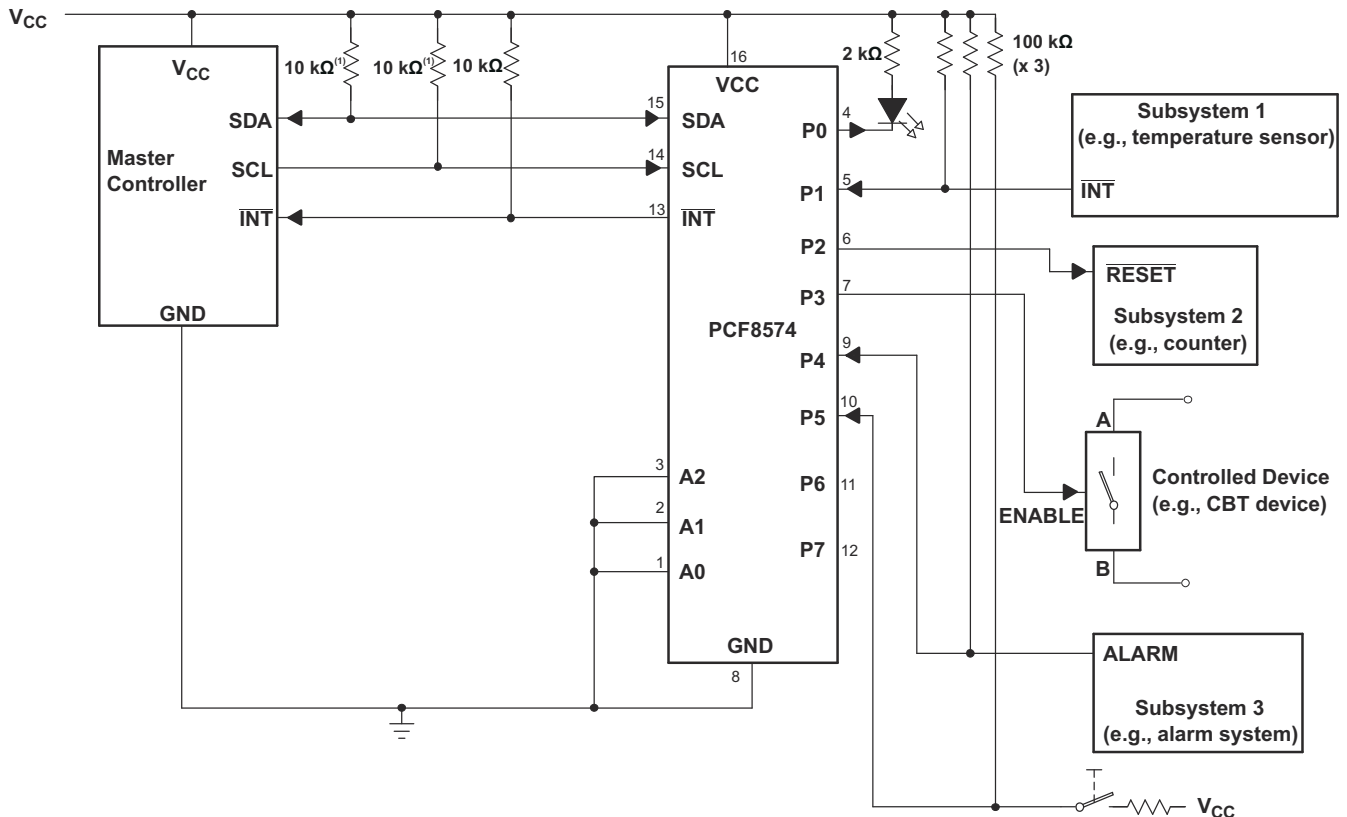
备注

以下应用部分中的信息不属于 TI 器件规格的范围，TI 不担保其准确性和完整性。TI 的客户应负责确定器件是否适用于其应用。客户应验证并测试其设计，以确保系统功能。

8.1 Application Information

图 8-1 shows an application in which the PCF8574 device can be used.

8.2 Typical Application



- The SCL and SDA pins must be tied directly to V_{CC} because if SCL and SDA are tied to an auxiliary power supply that could be powered on while V_{CC} is powered off, then the supply current, I_{CC} , will increase as a result.
- Device address is configured as 0100000 for this example.
- P0, P2, and P3 are configured as outputs.
- P1, P4, and P5 are configured as inputs.
- P6 and P7 are not used and must be configured as outputs.

图 8-1. Application Schematic

8.2.1 Design Requirements

8.2.1.1 Minimizing I_{CC} When I/Os Control LEDs

When the I/Os are used to control LEDs, normally they are connected to V_{CC} through a resistor as shown in 图 8-1. For a P-port configured as an input, I_{CC} increases as V_I becomes lower than V_{CC} . The LED is a diode, with threshold voltage V_T , and when a P-port is configured as an input the LED will be off but V_I is a V_T drop below V_{CC} .

For battery-powered applications, it is essential that the voltage of P-ports controlling LEDs is greater than or equal to V_{CC} when the P-ports are configured as input to minimize current consumption. 图 8-2 shows a high-value resistor in parallel with the LED. 图 8-3 shows V_{CC} less than the LED supply voltage by at least V_T . Both of these methods maintain the I/O V_I at or above V_{CC} and prevents additional supply current consumption when the P-port is configured as an input and the LED is off.

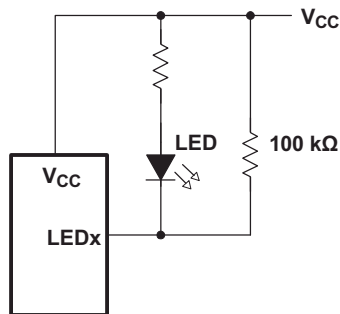


图 8-2. High-Value Resistor in Parallel With LED

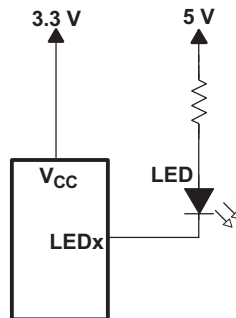


图 8-3. Device Supplied by a Lower Voltage

8.2.2 Detailed Design Procedure

The pull-up resistors, R_p , for the SCL and SDA lines need to be selected appropriately and take into consideration the total capacitance of all targets on the I²C bus. The minimum pull-up resistance is a function of V_{CC} , $V_{OL(max)}$, and I_{OL} :

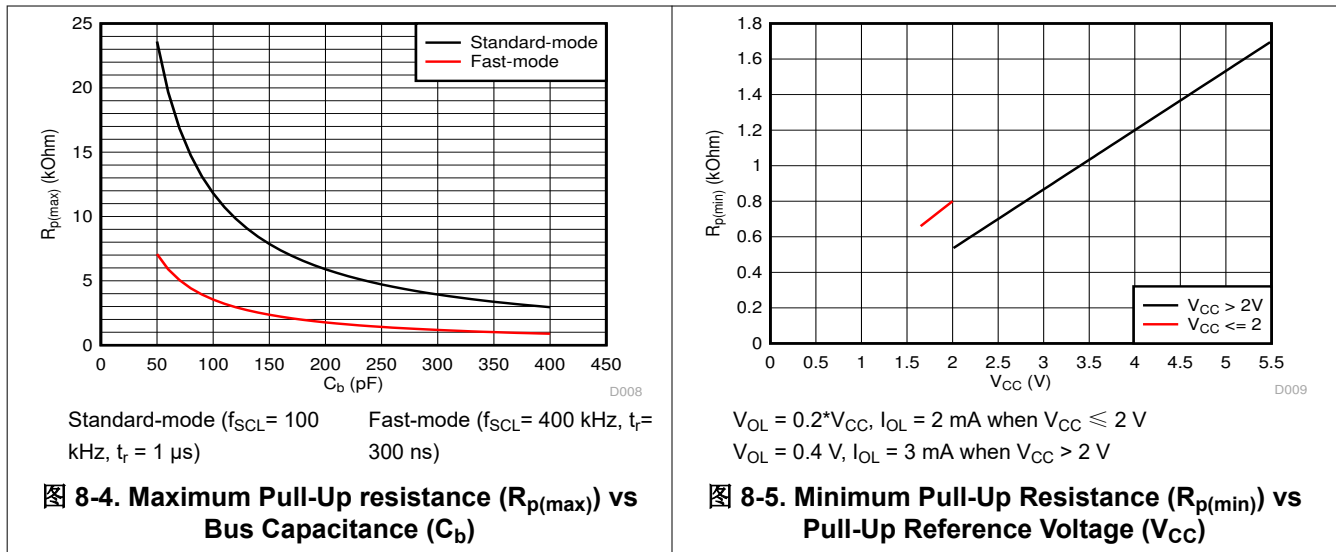
$$R_{p(min)} = \frac{V_{CC} - V_{OL(max)}}{I_{OL}} \quad (1)$$

The maximum pull-up resistance is a function of the maximum rise time, t_r (300 ns for fast-mode operation, $f_{SCL} = 400$ kHz) and bus capacitance, C_b :

$$R_{p(max)} = \frac{t_r}{0.8473 \times C_b} \quad (2)$$

The maximum bus capacitance for an I²C bus must not exceed 400 pF for standard-mode or fast-mode operation. The bus capacitance can be approximated by adding the capacitance of the PCF8574 device, C_i for SCL or C_{io} for SDA, the capacitance of wires/connections/traces, and the capacitance of additional targets on the bus.

8.2.3 Application Curves



8.3 Power Supply Recommendations

8.3.1 Power-On Reset Requirements

In the event of a glitch or data corruption, the PCF8574 device can be reset to its default conditions by using the power-on reset feature. Power-on reset requires that the device go through a power cycle to be completely reset. This reset also happens when the device is powered on for the first time in an application.

The two types of power-on reset are shown in 图 8-6 and 图 8-7.

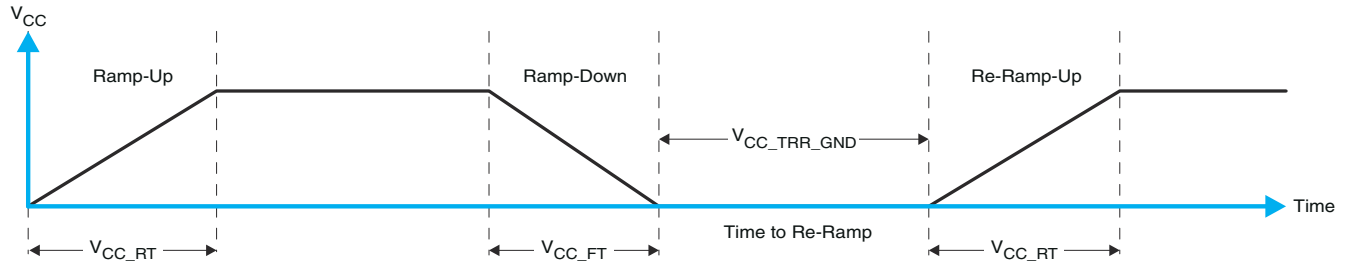


图 8-6. V_{CC} is Lowered Below 0.2 V or 0 V and Then Ramped Up to V_{CC}

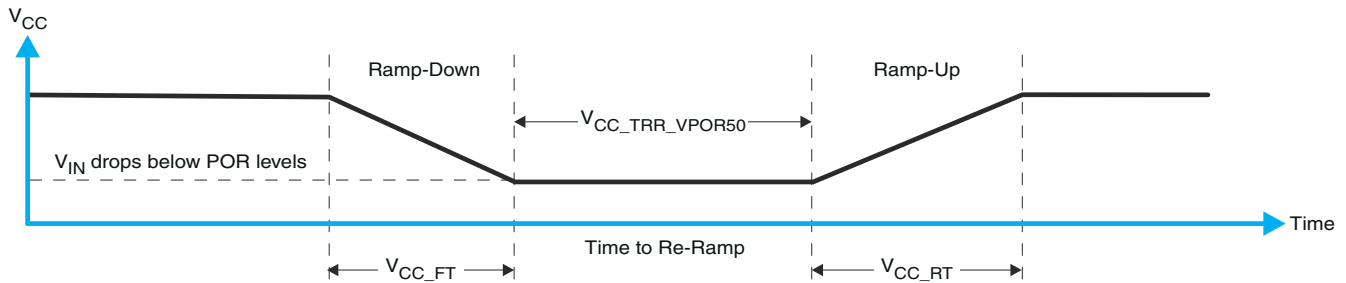


图 8-7. V_{CC} is Lowered Below the POR Threshold, Then Ramped Back Up to V_{CC}

表 8-1 specifies the performance of the power-on reset feature for PCF8574 for both types of power-on reset.

表 8-1. Recommended Supply Sequencing and Ramp Rates ⁽¹⁾

PARAMETER			MIN	TYP	MAX	UNIT
V_{CC_FT}	Fall rate	See 图 8-6	1		100	ms
V_{CC_RT}	Rise rate	See 图 8-6	0.01		100	ms
$V_{CC_TRR_GND}$	Time to re-ramp (when V_{CC} drops to GND)	See 图 8-6	0.001			ms
$V_{CC_TRR_POR50}$	Time to re-ramp (when V_{CC} drops to $V_{POR_MIN} - 50$ mV)	See 图 8-7	0.001			ms
V_{CC_GH}	Level that V_{CCP} can glitch down to, but not cause a functional disruption when $V_{CCX_GW} = 1$ μ s	See 图 8-8			1.2	V
V_{CC_GW}	Glitch width that will not cause a functional disruption when $V_{CCX_GH} = 0.5 \times V_{CCx}$	See 图 8-8				μ s
V_{PORF}	Voltage trip point of POR on falling V_{CC}		0.99		1.28	V
V_{PORR}	Voltage trip point of POR on rising V_{CC}		1.190		1.410	V

(1) $T_A = -40^\circ\text{C}$ to 85°C (unless otherwise noted)

Glitches in the power supply can also affect the power-on reset performance of this device. The glitch width (V_{CC_GW}) and height (V_{CC_GH}) are dependent on each other. The bypass capacitance, source impedance, and device impedance are factors that affect power-on reset performance. 图 8-8 and 表 8-1 provide more information on how to measure these specifications.

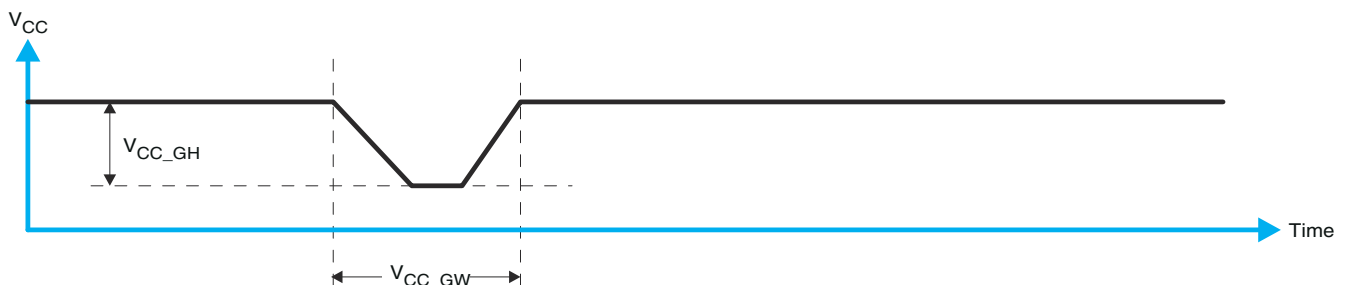


图 8-8. Glitch Width and Glitch Height

V_{POR} is critical to the power-on reset. V_{POR} is the voltage level at which the reset condition is released and all the registers and the I²C/SMBus state machine are initialized to their default states. The value of V_{POR} differs based on the V_{CC} being lowered to or from 0. 图 8-9 and 表 8-1 provide more details on this specification.

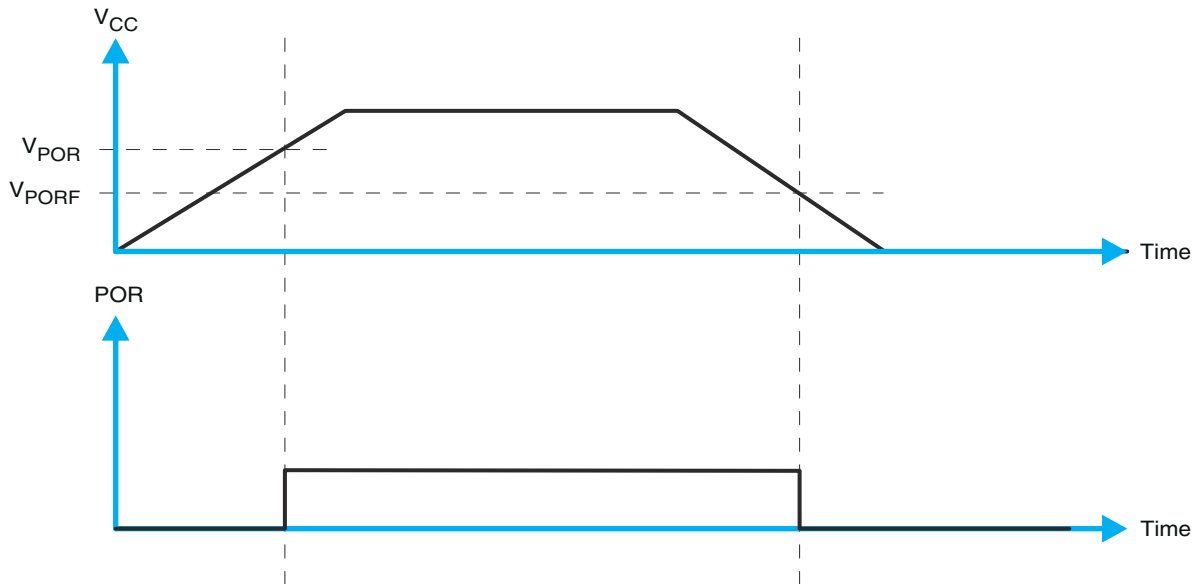


图 8-9. V_{POR}

8.4 Layout

8.4.1 Layout Guidelines

For printed circuit board (PCB) layout of the PCF8574 device, common PCB layout practices should be followed but additional concerns related to high-speed data transfer such as matched impedances and differential pairs are not a concern for I2C signal speeds.

In all PCB layouts, it is a best practice to avoid right angles in signal traces, to fan out signal traces away from each other upon leaving the vicinity of an integrated circuit (IC), and to use thicker trace widths to carry higher amounts of current that commonly pass through power and ground traces. By-pass and de-coupling capacitors are commonly used to control the voltage on the VCC pin, using a larger capacitor to provide additional power in the event of a short power supply glitch and a smaller capacitor to filter out high-frequency ripple. These capacitors should be placed as close to the PCF8574 device as possible. These best practices are shown in 图 8-10.

For the layout example provided in 图 8-10, it would be possible to fabricate a PCB with only 2 layers by using the top layer for signal routing and the bottom layer as a split plane for power (VCC) and ground (GND). However, a 4 layer board is preferable for boards with higher density signal routing. On a 4 layer PCB, it is common to route signals on the top and bottom layer, dedicate one internal layer to a ground plane, and dedicate the other internal layer to a power plane. In a board layout using planes or split planes for power and ground, vias are placed directly next to the surface mount component pad which needs to attach to VCC or GND and the via is connected electrically to the internal layer or the other side of the board. Vias are also used when a signal trace needs to be routed to the opposite side of the board, but this technique is not demonstrated in 图 8-10.

8.4.2 Layout Example

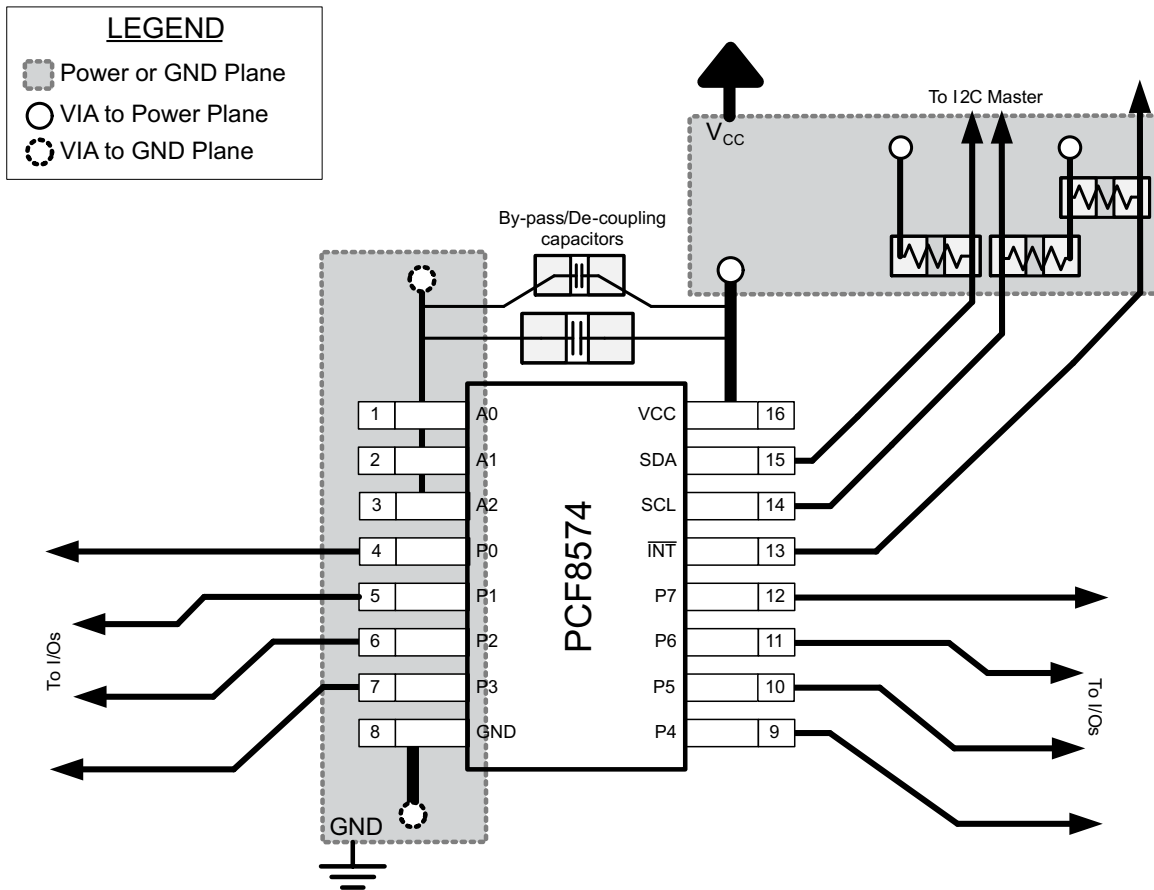


图 8-10. Layout Example for PCF8574

9 Device and Documentation Support

9.1 Documentation Support

9.1.1 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms and definitions.

9.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

9.3 支持资源

[TI E2E™ 中文支持论坛](#)是工程师的重要参考资料，可直接从专家处获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题，获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的[使用条款](#)。

9.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.

所有商标均为其各自所有者的财产。

9.5 静电放电警告



静电放电 (ESD) 会损坏这个集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

9.6 术语表

[TI 术语表](#) 本术语表列出并解释了术语、首字母缩略词和定义。

10 Revision History

Changes from Revision J (March 2016) to Revision K (September 2024)	Page
• 将提到 I ² C 的旧术语实例通篇更改为控制器和目标.....	1
• 将“器件信息”表更改为封装信息表.....	1
• Update <i>Absolute Max Voltage</i> from 7V to 6.5V.....	4
• Update <i>Thermal Information</i> for RGY, PW, RGT, N and DW packages.....	4
• Update I _{OH} polarity and increase limit from -300 μA to -310 μA.....	6
• Removed footnote #2 from <i>Electrical Characteristics</i>	6
• Updated I _{IHL} test condition.....	6
• Changed Spike filter limit from 100ns to 70ns max.....	6
• Changed 图 7-3	15
• Updated VPORF and VPORR values.....	19

Changes from Revision I (November 2015) to Revision J (March 2016)	Page
• 更正了 器件信息 表中的器件型号.....	1

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser based versions of this data sheet, refer to the left hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
PCF8574DGVR	Active	Production	TVSOP (DGV) 20	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	PF574
PCF8574DGVR.A	Active	Production	TVSOP (DGV) 20	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	PF574
PCF8574DW	Obsolete	Production	SOIC (DW) 16	-	-	Call TI	Call TI	-40 to 85	PCF8574
PCF8574DWR	Active	Production	SOIC (DW) 16	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	PCF8574
PCF8574DWR.A	Active	Production	SOIC (DW) 16	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	PCF8574
PCF8574DWR1G4	Active	Production	SOIC (DW) 16	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	PCF8574
PCF8574DWR1G4.A	Active	Production	SOIC (DW) 16	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	PCF8574
PCF8574DWRG4	Obsolete	Production	SOIC (DW) 16	-	-	Call TI	Call TI	-40 to 85	PCF8574
PCF8574N	Active	Production	PDIP (N) 16	25 TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	PCF8574N
PCF8574N.A	Active	Production	PDIP (N) 16	25 TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	PCF8574N
PCF8574NE4	Active	Production	PDIP (N) 16	25 TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	PCF8574N
PCF8574PW	Obsolete	Production	TSSOP (PW) 20	-	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	PF574
PCF8574PWR	Active	Production	TSSOP (PW) 20	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	PF574
PCF8574PWR.A	Active	Production	TSSOP (PW) 20	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	PF574
PCF8574PWRG4	Active	Production	TSSOP (PW) 20	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	PF574
PCF8574PWRG4.A	Active	Production	TSSOP (PW) 20	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	PF574
PCF8574RGTR	Active	Production	VQFN (RGT) 16	3000 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	ZWJ
PCF8574RGTR.A	Active	Production	VQFN (RGT) 16	3000 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	ZWJ
PCF8574RGTRG4	Active	Production	VQFN (RGT) 16	3000 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	ZWJ
PCF8574RGTRG4.A	Active	Production	VQFN (RGT) 16	3000 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	ZWJ
PCF8574RGYR	Active	Production	VQFN (RGY) 20	3000 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	PF574
PCF8574RGYR.A	Active	Production	VQFN (RGY) 20	3000 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	PF574
PCF8574RGYRG4	Active	Production	VQFN (RGY) 20	3000 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	PF574
PCF8574RGYRG4.A	Active	Production	VQFN (RGY) 20	3000 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	PF574

(1) **Status:** For more details on status, see our [product life cycle](#).

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer:The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

GENERIC PACKAGE VIEW

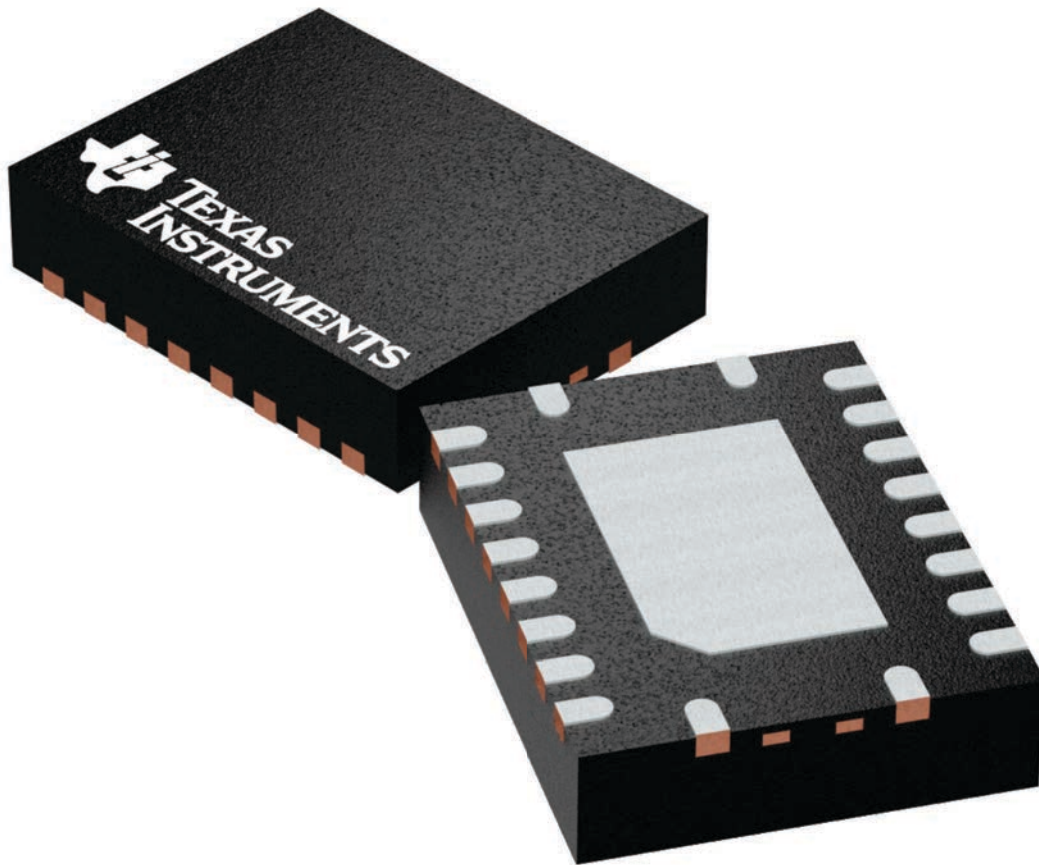
RGY 20

VQFN - 1 mm max height

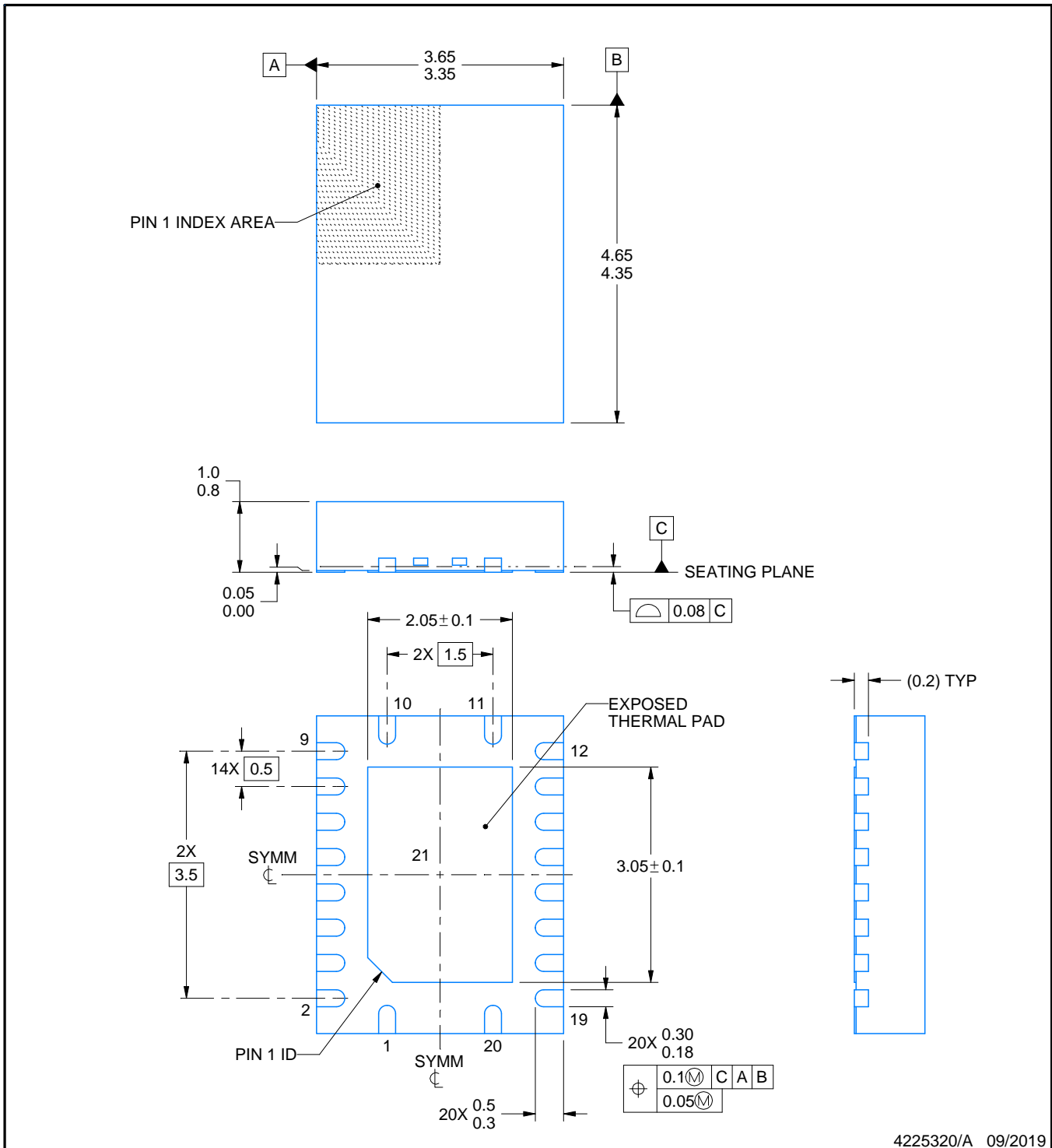
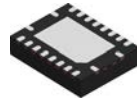
3.5 x 4.5, 0.5 mm pitch

PLASTIC QUAD FGLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4225264/A



4225320/A 09/2019

NOTES:

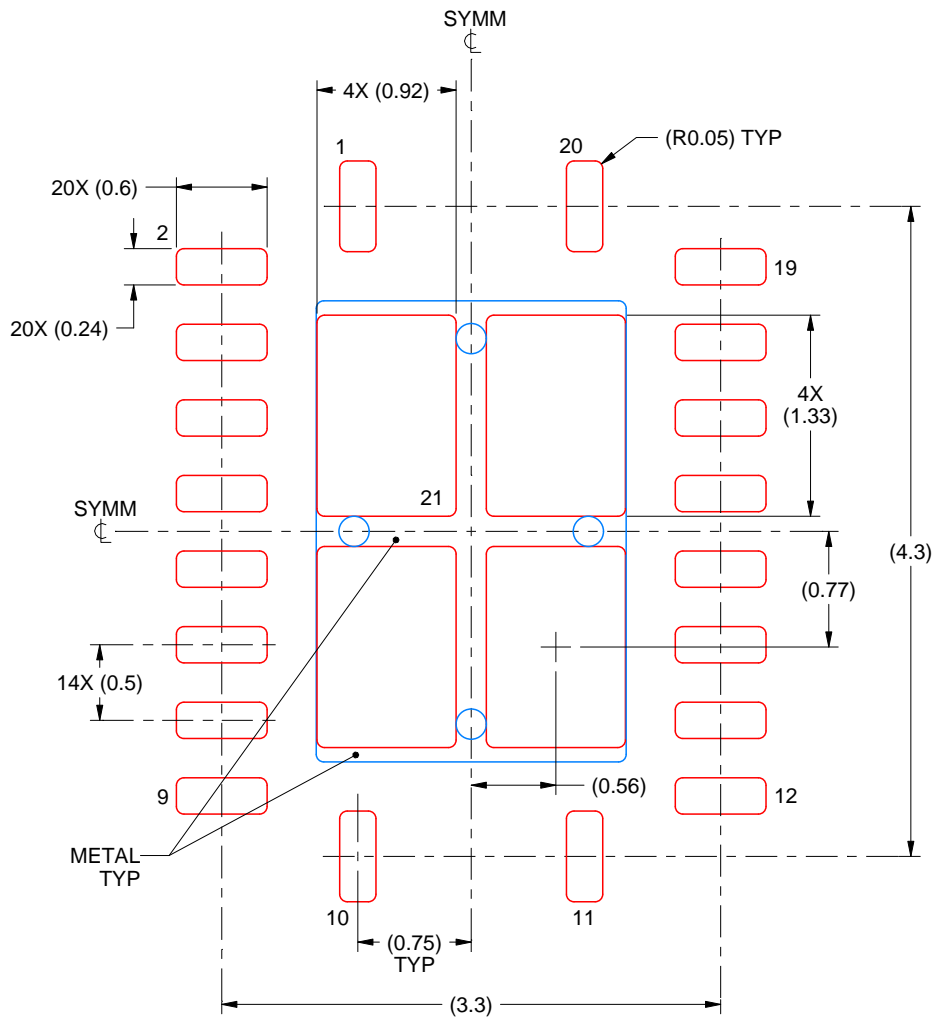
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

EXAMPLE STENCIL DESIGN

RGY0020A

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



SOLDER PASTE EXAMPLE
 BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 21
 78% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
 SCALE:20X

4225320/A 09/2019

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

GENERIC PACKAGE VIEW

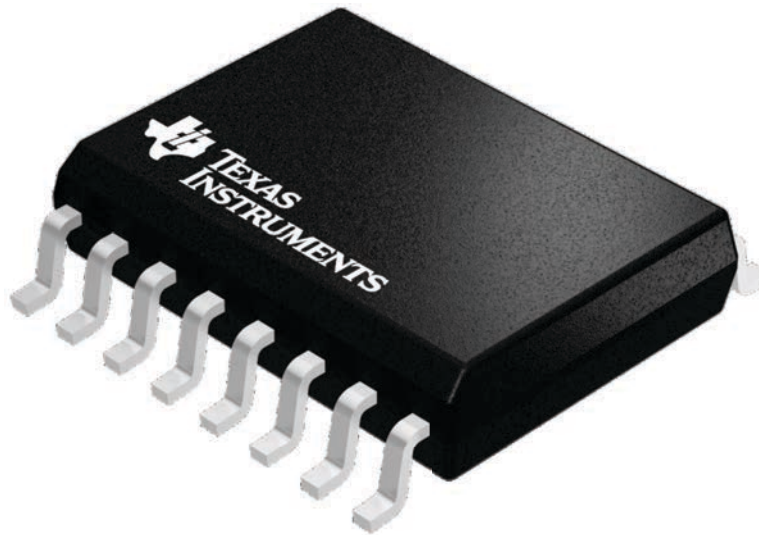
DW 16

SOIC - 2.65 mm max height

7.5 x 10.3, 1.27 mm pitch

SMALL OUTLINE INTEGRATED CIRCUIT

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4224780/A

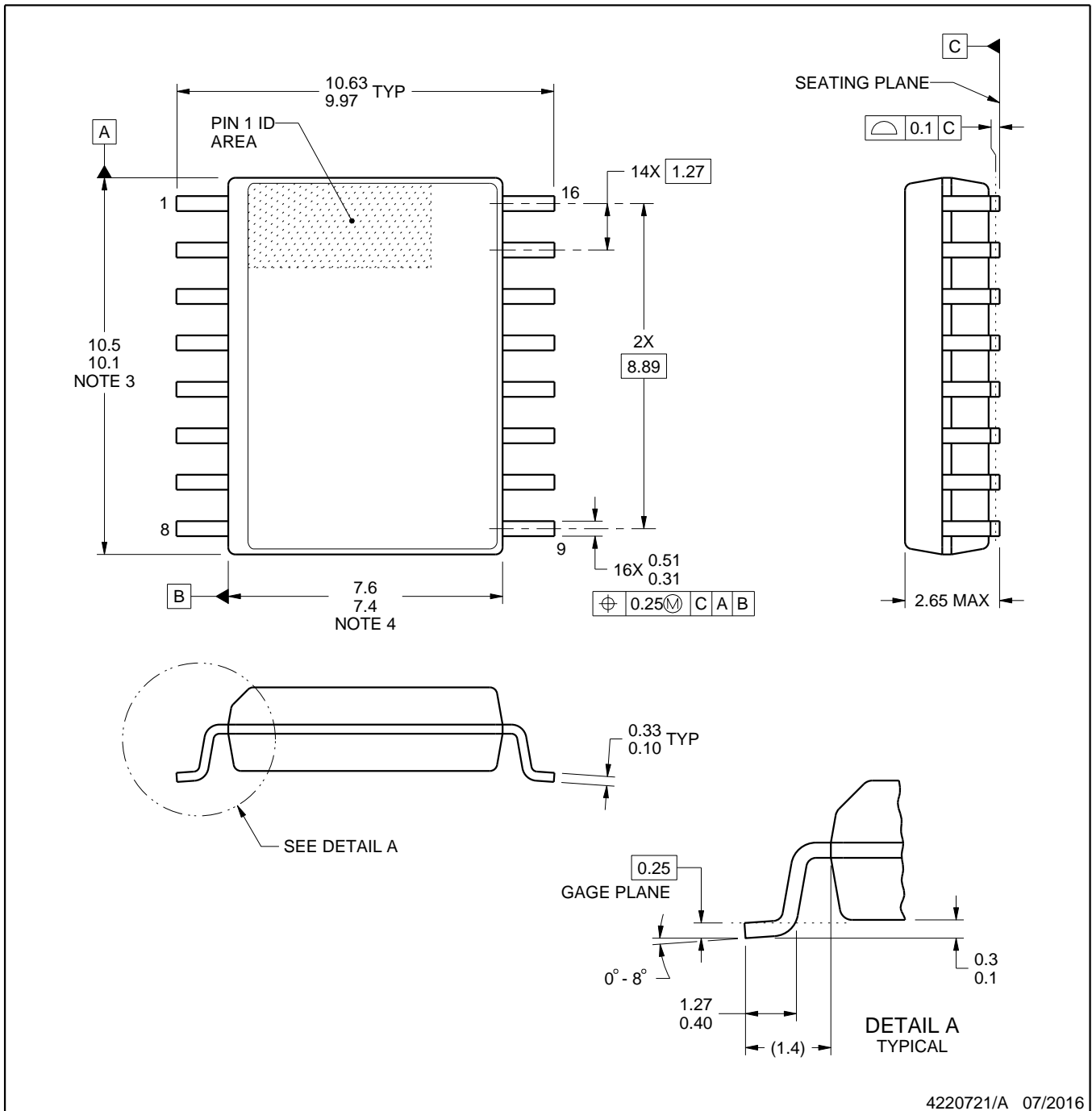


DW0016A

PACKAGE OUTLINE

SOIC - 2.65 mm max height

SOIC



4220721/A 07/2016

NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.
5. Reference JEDEC registration MS-013.

EXAMPLE BOARD LAYOUT

DW0016A

SOIC - 2.65 mm max height

SOIC



LAND PATTERN EXAMPLE
SCALE:7X



SOLDER MASK DETAILS

4220721/A 07/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DW0016A

SOIC - 2.65 mm max height

SOIC



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:7X

4220721/A 07/2016

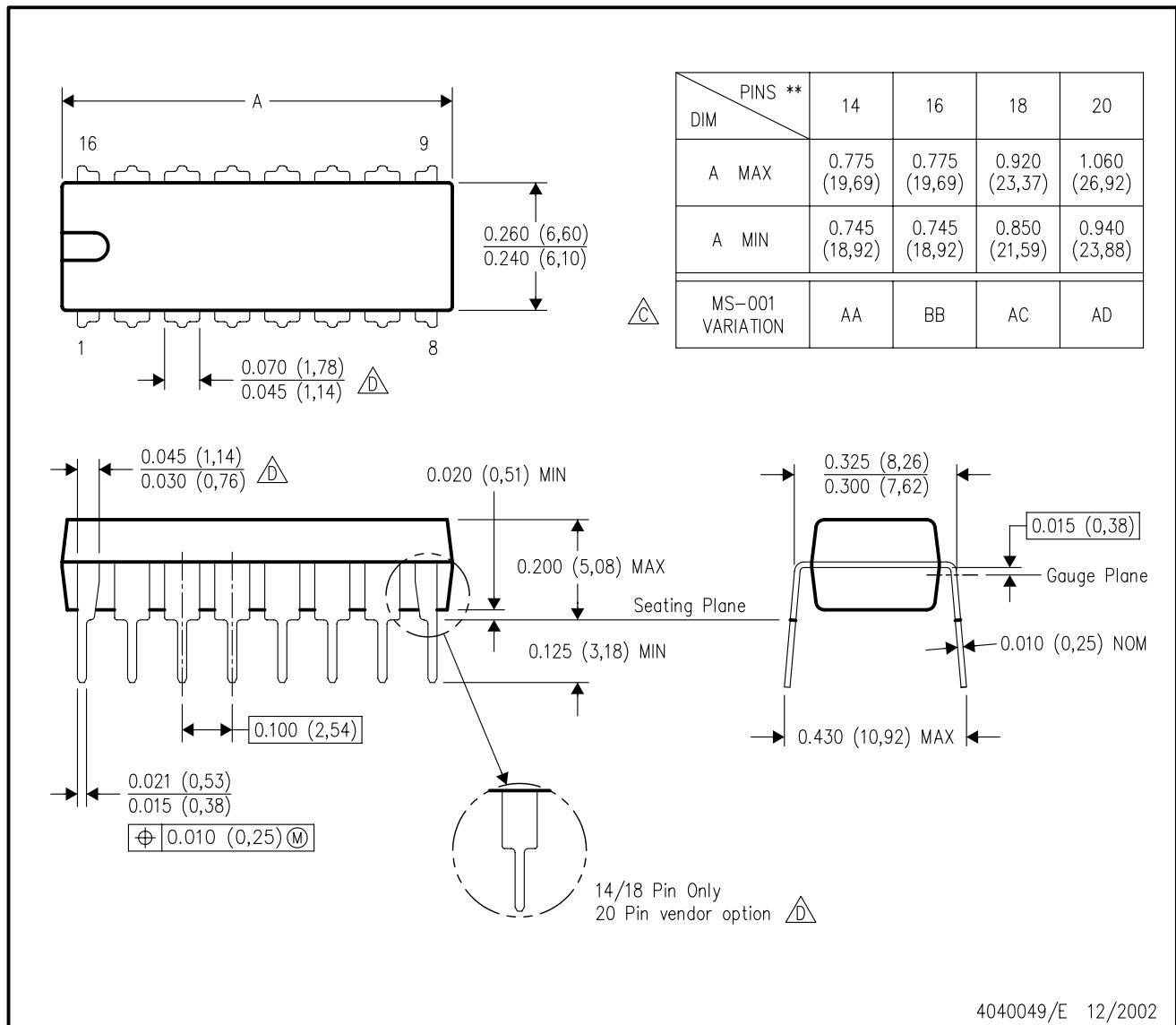
NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

N (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE

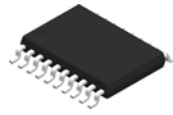
16 PINS SHOWN



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - $\triangle C$ Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
 - $\triangle D$ The 20 pin end lead shoulder width is a vendor option, either half or full width.

4040049/E 12/2002

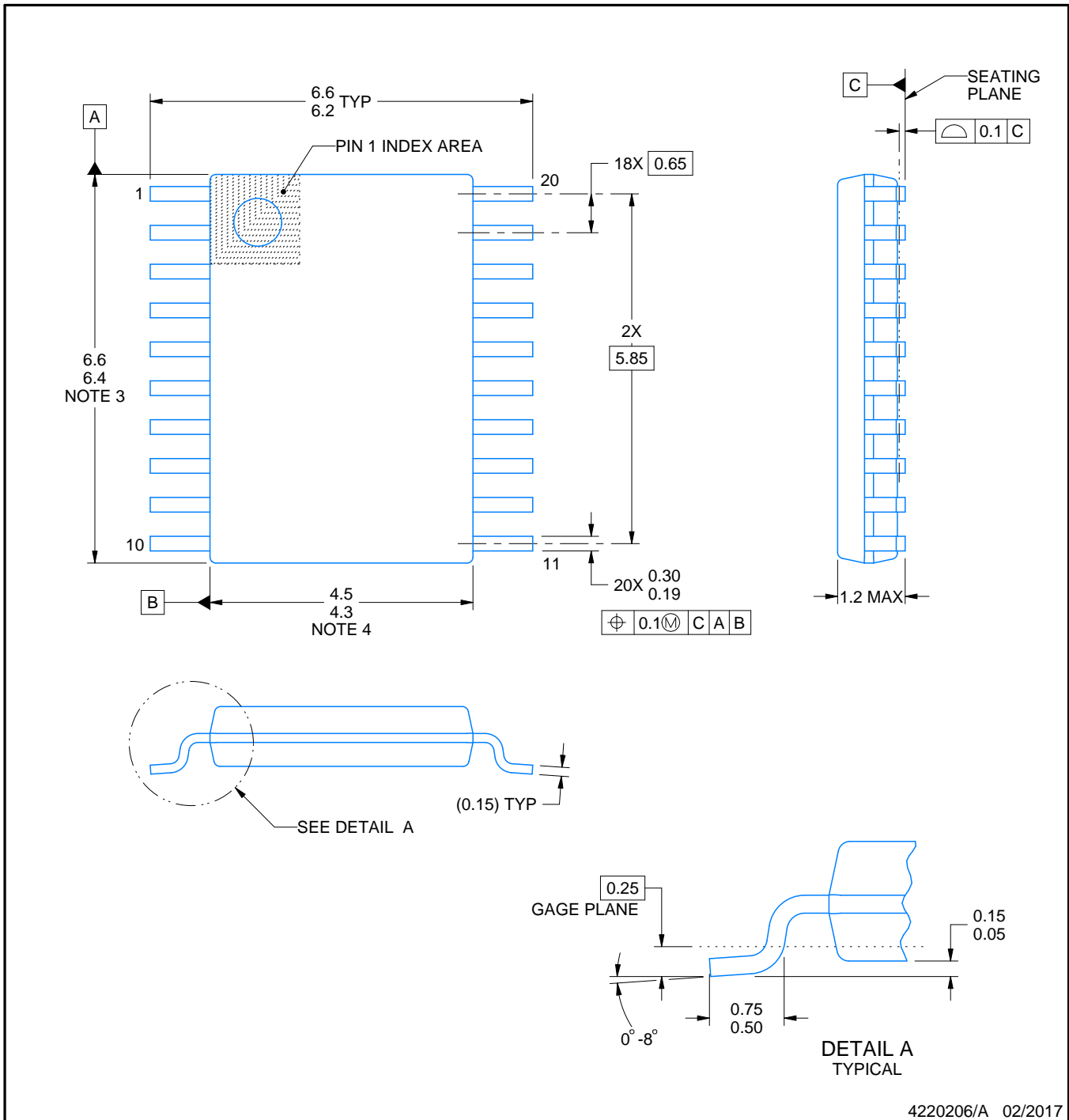
PW0020A



PACKAGE OUTLINE

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



4220206/A 02/2017

NOTES:

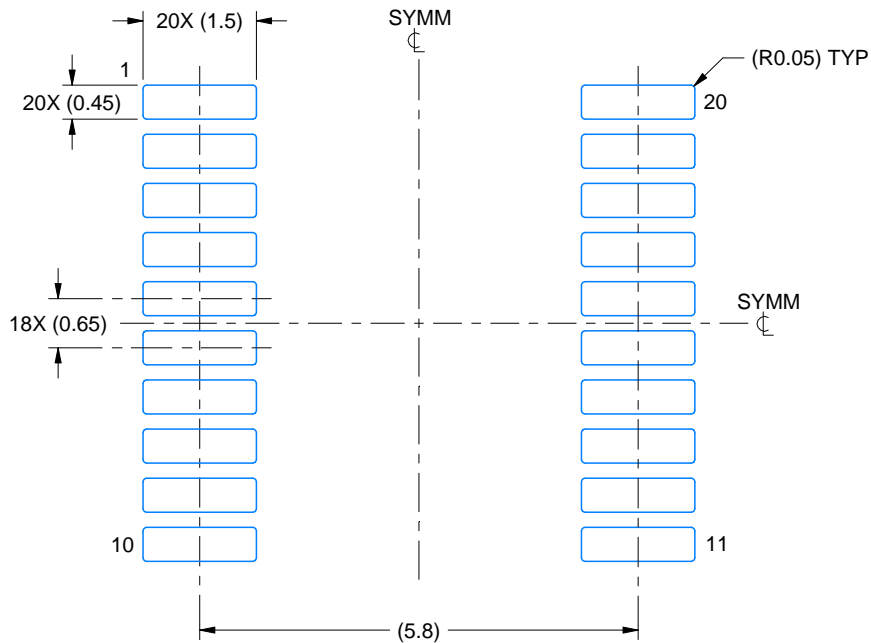
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

EXAMPLE BOARD LAYOUT

PW0020A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



SOLDER MASK DETAILS

4220206/A 02/2017

NOTES: (continued)

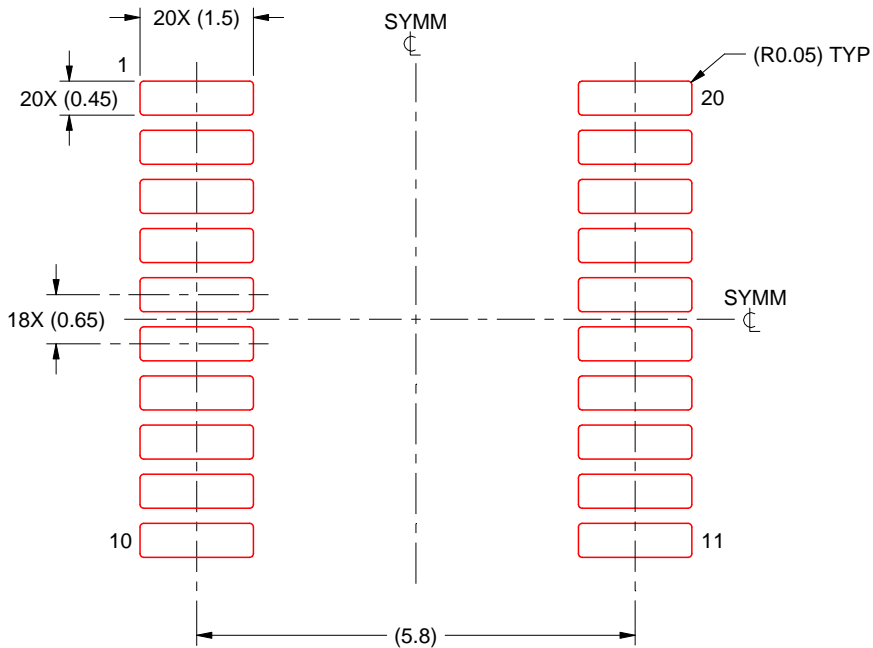
- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

PW0020A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220206/A 02/2017

NOTES: (continued)

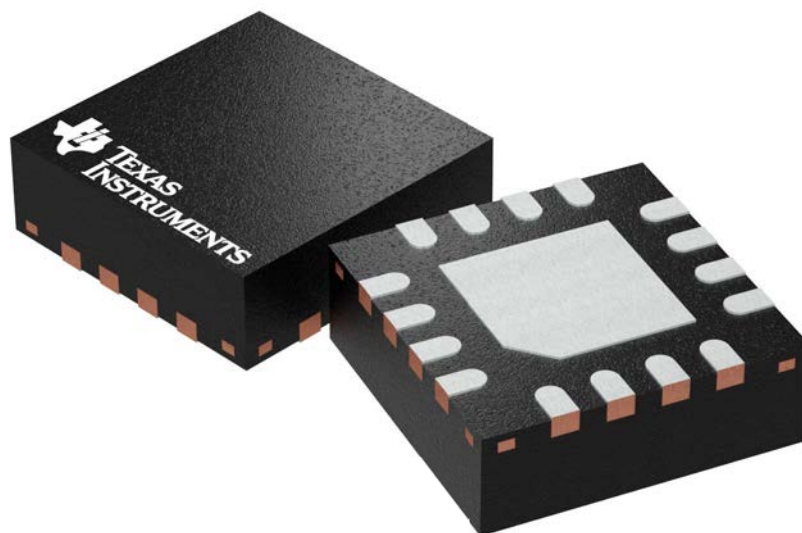
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

RGT 16

GENERIC PACKAGE VIEW

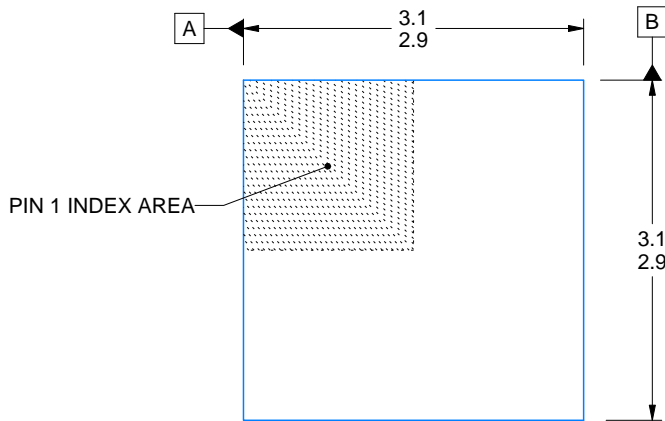
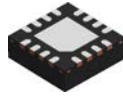
VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

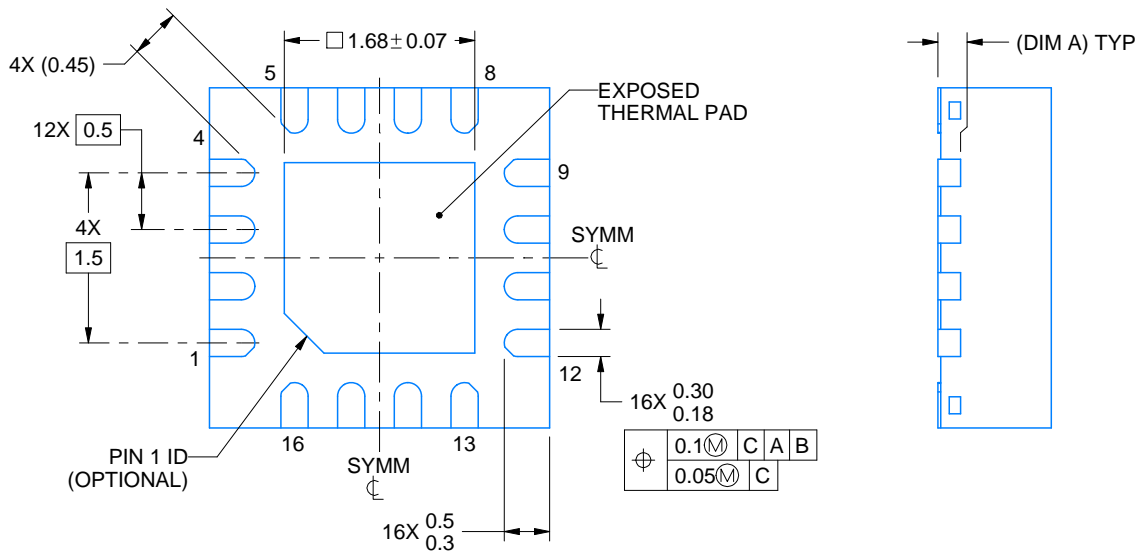
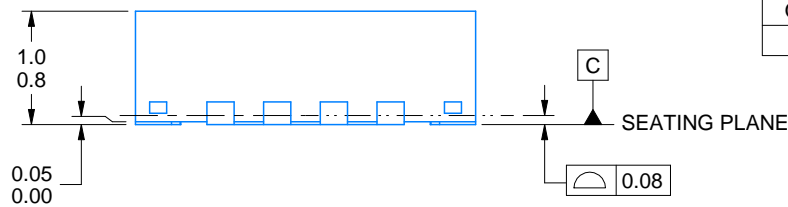


Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

4203495/1



SIDE WALL METAL THICKNESS DIM A	
OPTION 1	OPTION 2
0.1	0.2



4222419/E 07/2025

NOTES:

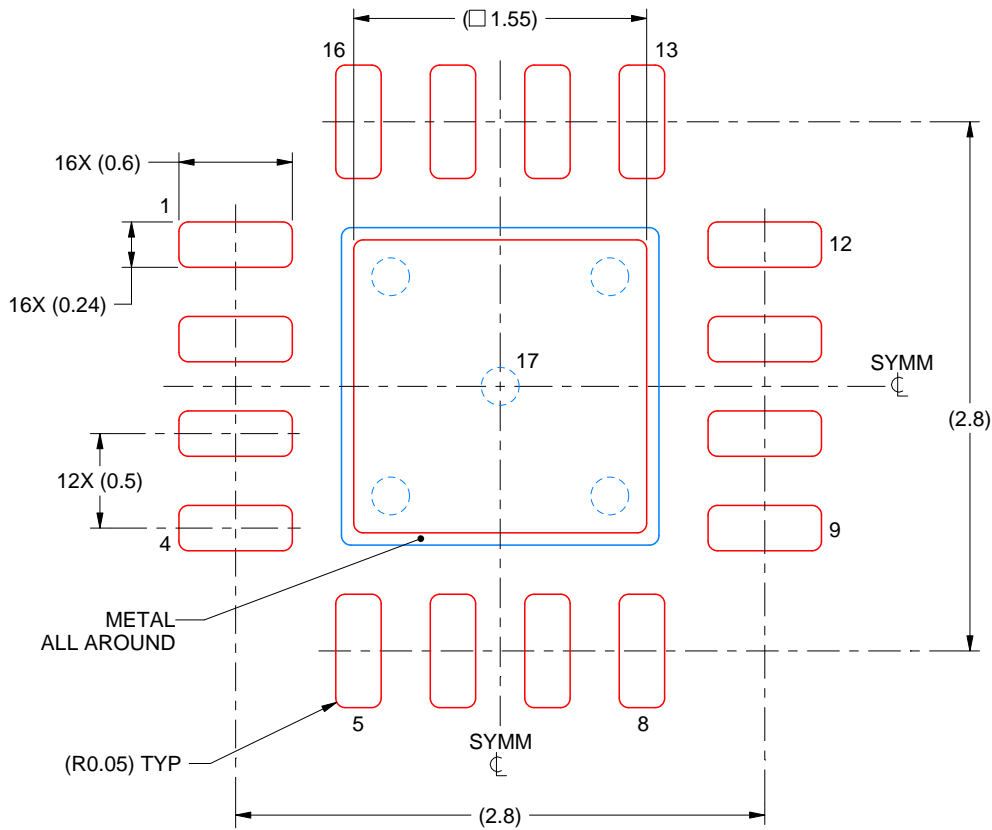
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

EXAMPLE STENCIL DESIGN

RGT0016C

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 17:
85% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:25X

4222419/E 07/2025

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

重要通知和免责声明

TI“按原样”提供技术和可靠性数据（包括数据表）、设计资源（包括参考设计）、应用或其他设计建议、网络工具、安全信息和其他资源，不保证没有瑕疵且不做任何明示或暗示的担保，包括但不限于对适销性、与某特定用途的适用性或不侵犯任何第三方知识产权的暗示担保。

这些资源可供使用 TI 产品进行设计的熟练开发人员使用。您将自行承担以下全部责任：(1) 针对您的应用选择合适的 TI 产品，(2) 设计、验证并测试您的应用，(3) 确保您的应用满足相应标准以及任何其他安全、安保法规或其他要求。

这些资源如有变更，恕不另行通知。TI 授权您仅可将这些资源用于研发本资源所述的 TI 产品的相关应用。严禁以其他方式对这些资源进行复制或展示。您无权使用任何其他 TI 知识产权或任何第三方知识产权。对于因您对这些资源的使用而对 TI 及其代表造成的任何索赔、损害、成本、损失和债务，您将全额赔偿，TI 对此概不负责。

TI 提供的产品受 [TI 销售条款](#)、[TI 通用质量指南](#) 或 [ti.com](#) 上其他适用条款或 TI 产品随附的其他适用条款的约束。TI 提供这些资源并不会扩展或以其他方式更改 TI 针对 TI 产品发布的适用的担保或担保免责声明。除非德州仪器 (TI) 明确将某产品指定为定制产品或客户特定产品，否则其产品均为按确定价格收入目录的标准通用器件。

TI 反对并拒绝您可能提出的任何其他或不同的条款。

版权所有 © 2026，德州仪器 (TI) 公司

最后更新日期：2025 年 10 月