PCF8575 具有中断输出的远程 16 位 I²C 和 SMBus I/O 扩展器

1 特性

- I²C 至并行端口扩展器
- 开漏中断输出
- 低待机流耗，最大值为 10 µA
- 兼容大多数微控制器
- 400kHz 快速 I²C 总线
- 可通过 3 个硬件地址引脚设置地址，从而可在总线上连接多达 8 个器件
- 具有高电流驱动能力的锁存输出，用于直接驱动 LED
- 连接到 V_{CC} 的电流源，用于主动在输出端驱动高电平
- 闩锁性能超过 100mA，符合 JESD 78 II 类规范的要求
- ESD 保护性能超过 JESD 22 规范要求
  - 2000V 人体放电模型
  - 200V 机器放电模型
  - 1000V 充电器件模型

2 应用

- 电信方舱：滤波器单元
- 服务器
- 路由器（电信交换设备）
- 个人计算机
- 个人电子产品
- 工业自动化
- 具有较少 GPIO 的产品

3 说明

这款面向两线制双向总线 (I²C) 的 16 位 I/O 扩展器设计为在 2.5V 至 5.5V V_{CC} 下运行。

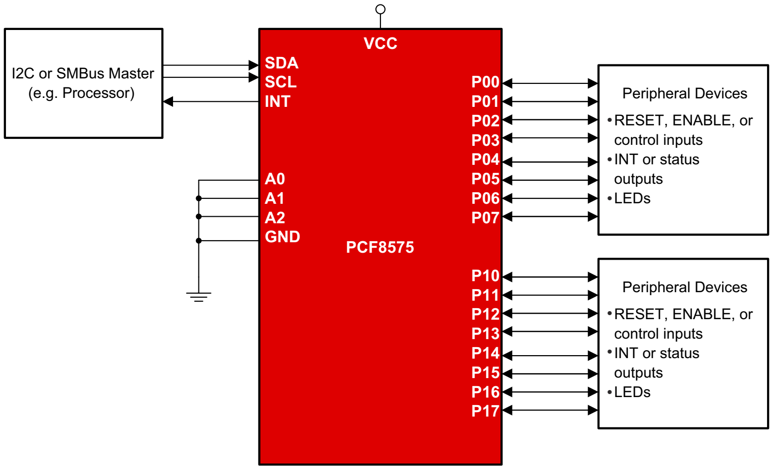
PCF8575 器件通过 I²C 接口 [串行时钟 (SCL)、串行数据 (SDA)] 为大多数微控制器系列提供通用远程 I/O 扩展。

该器件具有一个 16 位准双向输入/输出 (I/O) 端口（P07 – P00、P17 – P10），其中包括具有高电流驱动能力的锁存输出，用于直接驱动 LED。每个准双向 I/O 都可以用作输入或输出（无需使用数据方向控制信号）。在上电时，这些 I/O 处于高电平。在该模式下，仅有一个连接到 V_{CC} 的电流源处于活动状态。

封装信息

器件型号	封装(1)	封装尺寸(2)
PCF8575	SSOP（DB，24）	8.2mm × 7.8mm
	SSOP（DBQ，24）	8.65mm × 6mm
	TVSOP（DGV，24）	5mm × 6.4mm
	SOIC（DW，24）	15.5mm × 10.3mm
	TSSOP（PW，24）	7.8mm × 6.4mm
	VQFN（RGV，24）	4mm × 4mm

(1) 有关可用封装，请参阅节 12。
(2) 封装尺寸（长 × 宽）为标称值，并包括引脚（如适用）。



简化原理图

English Data Sheet: SCPS121

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4 Pin Configuration and Functions

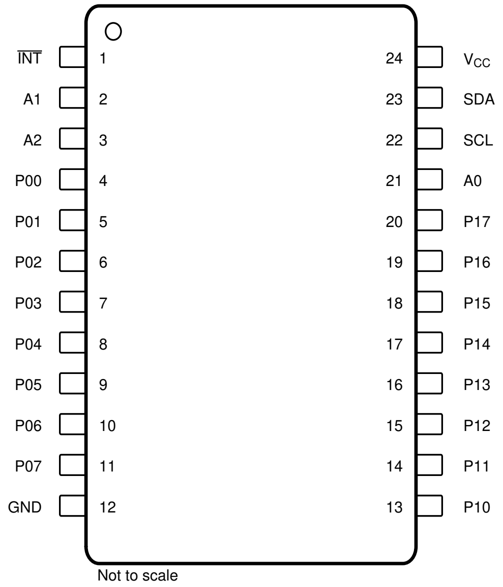


图 4-1. DB, DBQ, DGV, DW, or PW Package SSOP, TVSOP, SOIC, TSSOP (Top View)

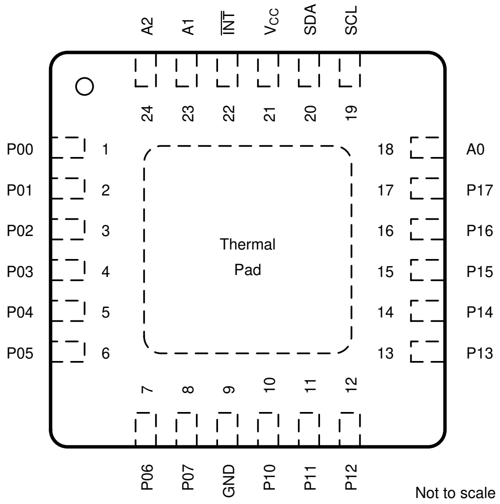


图 4-2. RGE Package VQFN (Top View)

PIN			TYPE	DESCRIPTION
NAME	DB, DBQ, DGV, DW, AND PW	RGE		
A0	21	18	I	Address input 0. Connect directly to V_{CC} or ground. Pull-up resistors are not needed.
A1	2	23	I	Address input 1. Connect directly to V_{CC} or ground. Pull-up resistors are not needed.
A2	3	24	I	Address input 2. Connect directly to V_{CC} or ground. Pull-up resistors are not needed.
$\overline{\text{INT}}$	1	22	O	Interrupt output. Connect to V_{CC} through a pull-up resistor.
P00	4	1	I/O	P-port input/output. Push-pull design structure.
P01	5	2	I/O	P-port input/output. Push-pull design structure.
P02	6	3	I/O	P-port input/output. Push-pull design structure.
P03	7	4	I/O	P-port input/output. Push-pull design structure.
P04	8	5	I/O	P-port input/output. Push-pull design structure.
P05	9	6	I/O	P-port input/output. Push-pull design structure.
P06	10	7	I/O	P-port input/output. Push-pull design structure.
P07	11	8	I/O	P-port input/output. Push-pull design structure.
GND	12	9	—	Ground
P10	13	10	I/O	P-port input/output. Push-pull design structure.
P11	14	11	I/O	P-port input/output. Push-pull design structure.
P12	15	12	I/O	P-port input/output. Push-pull design structure.
P13	16	13	I/O	P-port input/output. Push-pull design structure.
P14	17	14	I/O	P-port input/output. Push-pull design structure.
P15	18	15	I/O	P-port input/output. Push-pull design structure.
P16	19	16	I/O	P-port input/output. Push-pull design structure.
P17	20	17	I/O	P-port input/output. Push-pull design structure.
SCL	22	19	I	Serial clock line. Connect to V_{CC} through a pull-up resistor
SDA	23	20	I/O	Serial data line. Connect to V_{CC} through a pull-up resistor.
V_{CC}	24	21	—	Supply voltage

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1)

			MIN	MAX	UNIT
V_{CC}	Supply voltage range		– 0.5	6.5	V
V_I	Input voltage range (2)		– 0.5	V_{CC} + 0.5	V
V_O	Output voltage range (2)		– 0.5	V_{CC} + 0.5	V
I_{IK}	Input clamp current	$V_I < 0$		– 20	mA
I_{OK}	Output clamp current	$V_O < 0$		– 20	mA
I_{OK}	Input/output clamp current	$V_O < 0$ or $V_O > V_{CC}$		– 20	mA
I_{OL}	Continuous output low current	V_O = 0 to V_{CC}		50	mA
I_{OH}	Continuous output high current	V_O = 0 to V_{CC}		– 4	mA
	Continuous current through V_{CC} or GND			±100	mA
T_{stg}	Storage temperature range			150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under 节 5.3is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins	2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins	1000	

5.3 Recommended Operating Conditions

		MIN	MAX	UNIT
V_{CC}	Supply voltage	2.5	5.5	V
V_{IH}	High-level input voltage	0.7 × V_{CC}	V_{CC} + 0.5	V
V_{IL}	Low-level input voltage	– 0.5	0.3 × V_{CC}	V
I_{OH}	P-port high-level output current		– 1	mA
I_{OHT}	P-port transient pullup current		– 10	mA
I_{OL}	P-port low-level output current		25	mA
T_A	Operating free-air temperature	– 40	85	°C

5.4 Thermal Information

THERMAL METRIC (1)		PCF8575						UNIT
		DB	DBQ	DGV	DW	PW	RGE	
		24 PINS						
$R_{\theta JA}$	Junction-to-ambient thermal resistance	87.8	61	86	75.6	99.7	53.6	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	51.9			47.9	42.5	50.8	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	56.8			50.1	66.1	31.5	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	14.3			21.1	2.7	3.4	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	56.2			49.7	65.5	31.4	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	-			-	-	14.8	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

5.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP(1)	MAX	UNIT
V_{IK}	Input diode clamp voltage	$I_I = -18$ mA	2.5 V to 5.5 V	-1.2			V
V_{POR}	Power-on reset voltage	$V_I = V_{CC}$ or GND, $I_O = 0$	V_{POR}		1.2	1.8	V
I_{OH}	P port	V_O = GND	2.5 V to 5.5 V	-30		-300	μA
I_{OHT}	P-port transient pullup current	High during ACK, V_{OH} = GND	2.5 V	-0.5	-1		mA
I_{OL}	SDA	V_{OL} = 0.4 V	2.5 V to 5.5 V	3			mA
	P port	V_{OL} = 0.4 V		5	15		
		V_{OL} = 1 V		10	25		
	$\overline{INT}$	V_{OL} = 0.4 V		1.6			
I_I	SCL, SDA	$V_I = V_{CC}$ or GND	2.5 V to 5.5 V			±5	μA
	A0, A1, A2					±1	
I_{IHL}	P port	-250mV < Vi < GND	2.5 V to 5.5 V			±400	μA
I_{CC}	Operating mode	$V_I = V_{CC}$ or GND, $I_O = 0$, f_{scl} = 400 kHz	5.5 V		100	200	μA
			3.6 V		30	75	
			2.7 V		20	50	
	Standby mode	$V_I = V_{CC}$ or GND, $I_O = 0$, f_{scl} = 0 kHz	5.5 V		2.5	10	
			3.6 V		2.5	10	
			2.7 V		2.5	10	
ΔI_{CC}	Supply current increase	One input at V_{CC} – 0.6 V, Other inputs at V_{CC} or GND	2.5 V to 5.5 V			200	μA
C_I	SCL	$V_I = V_{CC}$ or GND	2.5 V to 5.5 V		3	7	pF
C_{io}	SDA	$V_{IO} = V_{CC}$ or GND	2.5 V to 5.5 V		3	7	pF
	P port				4	10	

(1) All typical values are at nominal supply voltage (2.5-V, 3.3-V, or 5-V V_{CC}) and T_A = 25°C.

5.6 I^{2}C Interface Timing Requirements

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 6-1)

			MIN	MAX	UNIT
f_{scl}	I^{2}C clock frequency			400	kHz
t_{sch}	I^{2}C clock high time		0.6		μs
t_{scl}	I^{2}C clock low time		1.3		μs
t_{sp}	I^{2}C spike time			50	ns
t_{sds}	I^{2}C serial data setup time		100		ns
t_{sdh}	I^{2}C serial data hold time		0		ns
t_{icr}	I^{2}C input rise time		20 + 0.1C_b (1)	300	ns
t_{icf}	I^{2}C input fall time		20 + 0.1C_b (1)	300	ns
t_{ocf}	I^{2}C output fall time	10-pF to 400-pF bus		300	ns
t_{buf}	I^{2}C bus free time between Stop and Start		1.3		μs
t_{sts}	I^{2}C start or repeated Start condition setup		0.6		μs
t_{sth}	I^{2}C start or repeated Start condition hold		0.6		μs
t_{sps}	I^{2}C Stop condition setup		0.6		μs
t_{vd}	Valid-data time	SCL low to SDA output valid		1.2	μs
C_b	I^{2}C bus capacitive load			400	pF

(1) C_b = total bus capacitance of one bus line in pF

5.7 Switching Characteristics

over recommended operating free-air temperature range, $C_L \leqslant 100$ pF (unless otherwise noted) (see Figure 6-2 and Figure 6-3)

PARAMETER		FROM (INPUT)	TO (OUTPUT)	MIN	MAX	UNIT
t_{iv}	Interrupt valid time	P port	$\overline{\text{INT}}$		4	µs
t_{ir}	Interrupt reset delay time	SCL	$\overline{\text{INT}}$		4	µs
t_{pv}	Output data valid	SCL	P port		4	µs
t_{su}	Input data setup time	P port	SCL	0		µs
t_h	Input data hold time	P port	SCL	4		µs

6 Typical Characteristics

T_A = 25°C (unless otherwise noted)

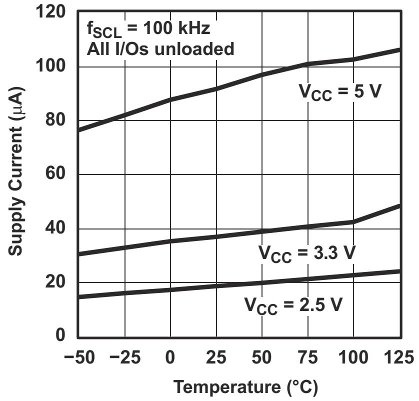


图 6-1. Supply Current vs Temperature

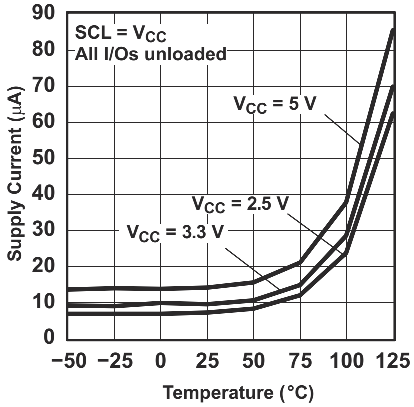


图 6-2. Standby Supply Current vs Temperature

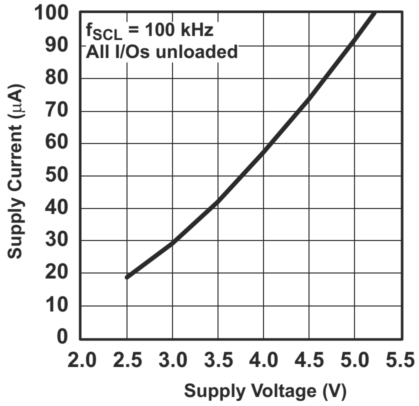


图 6-3. Supply Current vs Supply Voltage

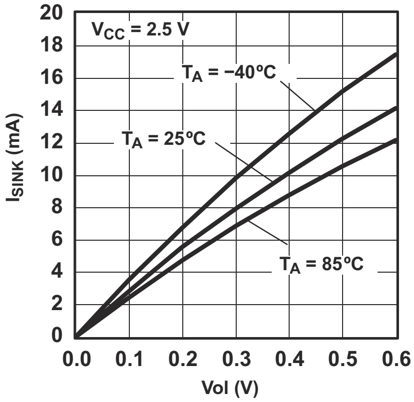


图 6-4. I/O Sink Current vs Output Low Voltage

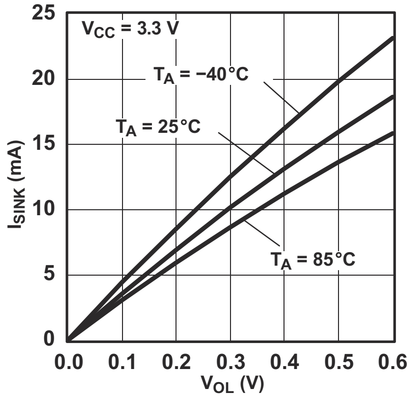


图 6-5. I/O Sink Current vs Output Low Voltage

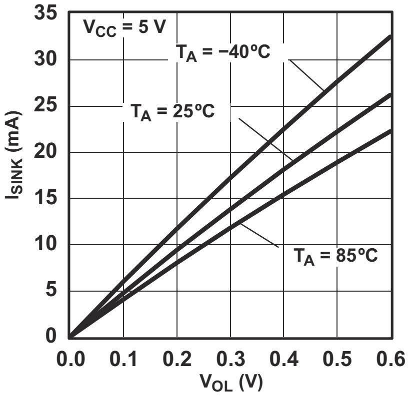


图 6-6. I/O Sink Current vs Output Low Voltage

6 Typical Characteristics (continued)

T_A = 25°C (unless otherwise noted)

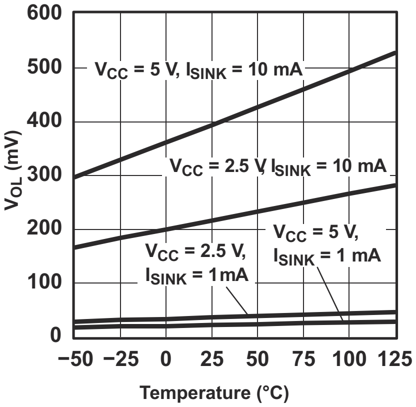


图 6-7. I/O Output Low Voltage vs Temperature

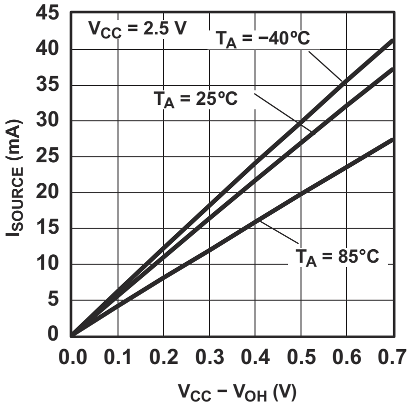


图 6-8. I/O Source Current vs Output High Voltage

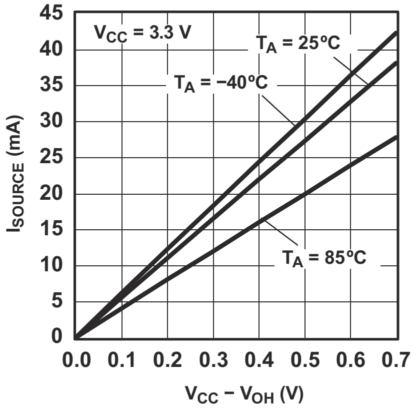


图 6-9. I/O Source Current vs Output High Voltage

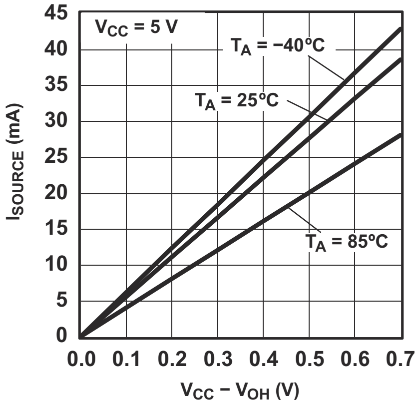


图 6-10. I/O Source Current vs Output High Voltage

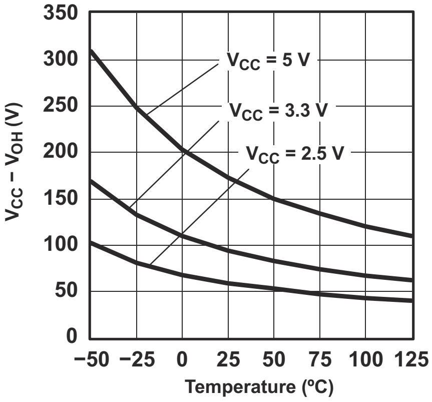
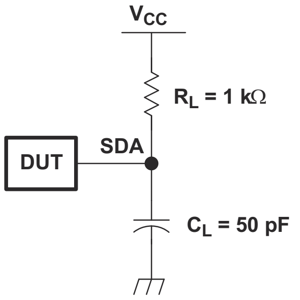
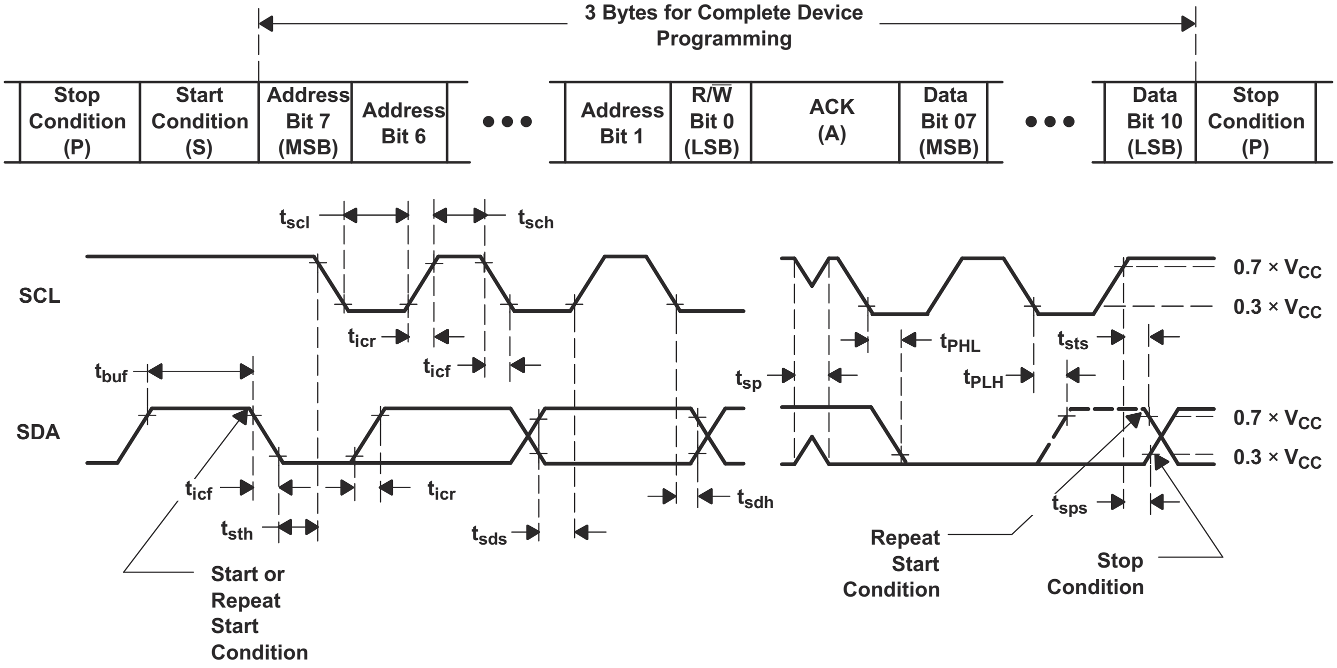


图 6-11. I/O High Voltage vs Temperature

7 Parameter Measurement Information



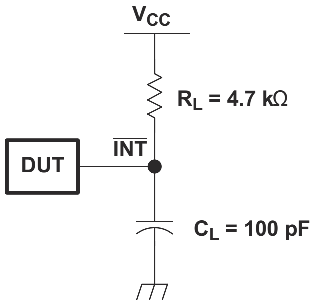
SDA LOAD CONFIGURATION



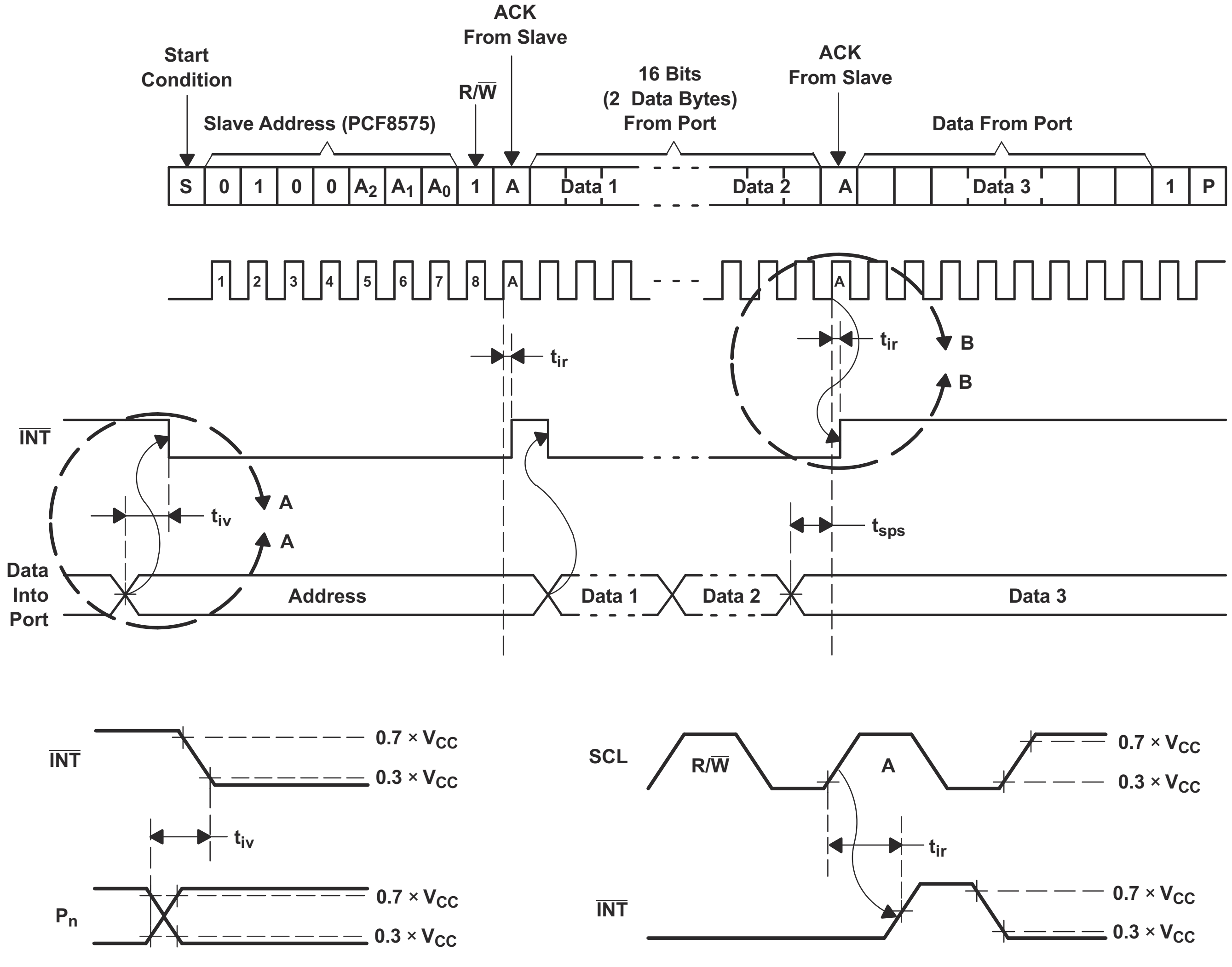
VOLTAGE WAVEFORMS

BYTE	DESCRIPTION
1	I^2C address
2, 3	P-port data

图 7-1. I^2C Interface Load Circuit and Voltage Waveforms



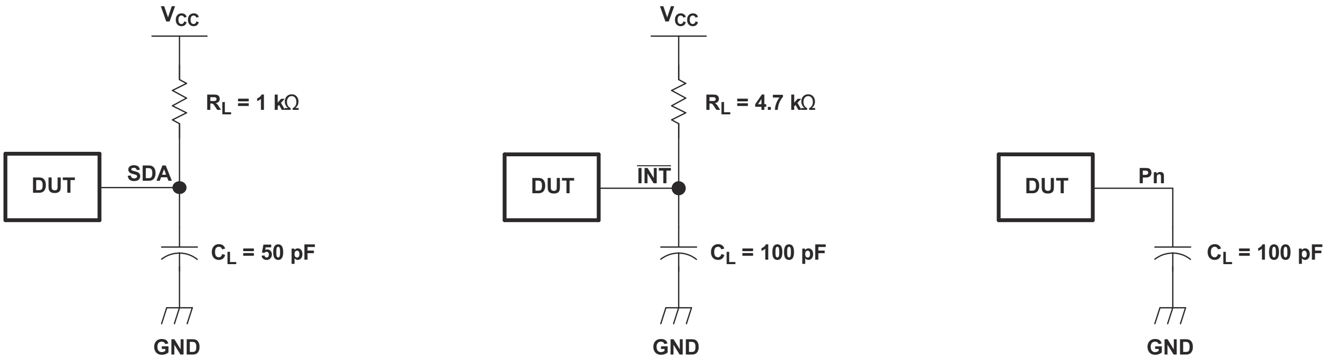
INTERRUPT LOAD CONFIGURATION



View A−A

View B−B

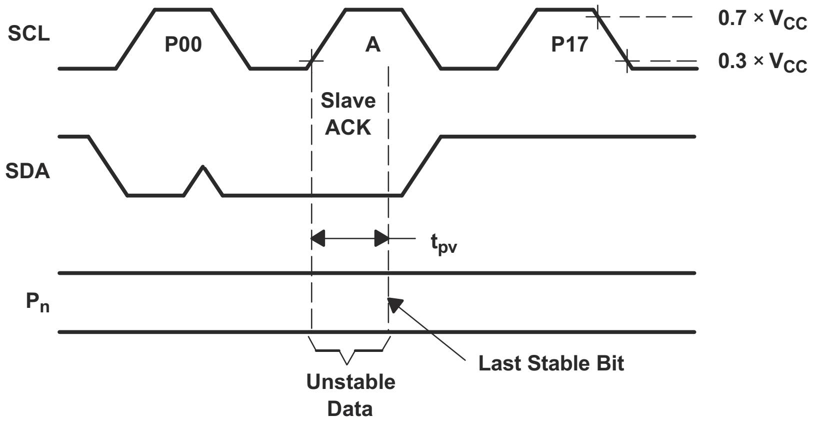
图 7-2. Interrupt Load Circuit and Voltage Waveforms



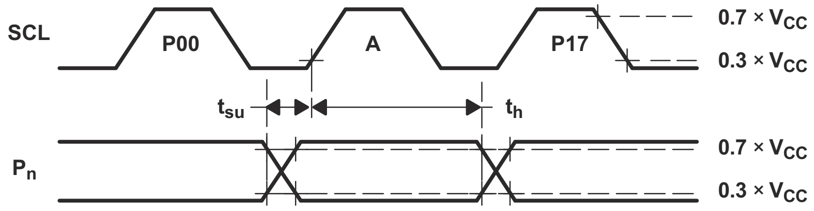
SDA LOAD CONFIGURATION

INTERRUPT LOAD CONFIGURATION

P-PORT LOAD CONFIGURATION



Write-Mode Timing ($R/\overline{W}$ = 0)



Read-Mode Timing ($R/\overline{W}$ = 1)

图 7-3. P-Port Load Circuits and Voltage Waveforms

8 Detailed Description

8.1 Overview

The PCF8575 provides general-purpose remote I/O expansion for most microcontroller families via the I^2C interface serial clock (SCL) and serial data (SDA).

The device features a 16-bit quasi-bidirectional input/output (I/O) port (P07 – P00, P17 – P10), including latched outputs with high-current drive capability for directly driving LEDs. Each quasi-bidirectional I/O can be used as an input or output without the use of a data-direction control signal. At power on, the I/Os are high. In this mode, only a current source (I_{OH}) to V_{CC} is active. An additional strong pullup to V_{CC} (I_{OHT}) allows fast-rising edges into heavily loaded outputs. This device turns on when an output is written high and is switched off by the negative edge of SCL. The I/Os should be high before being used as inputs. After power on, as all the I/Os are set high, all of them can be used as inputs. Any change in setting of the I/Os as either input or outputs can be done with the write mode. If a high is applied externally to an I/O that has been written earlier to low, a large current (I_{OL}) will flow to GND.

The PCF8575 provides an open-drain interrupt ($\overline{INT}$) output, which can be connected to the interrupt input of a microcontroller. An interrupt is generated by any rising or falling edge of the port inputs in the input mode. After time, t_{iv}, the signal $\overline{INT}$ is valid. Resetting and reactivating the interrupt circuit is achieved when data on the port is changed to the original setting, or data is read from or written to the port that generated the interrupt. Resetting occurs in the read mode at the acknowledge (ACK) bit after the rising edge of the SCL signal or in the write mode at the ACK bit after the falling edge of the SCL signal. Interrupts that occur during the ACK clock pulse can be lost (or be very short), due to the resetting of the interrupt during this pulse. Each change of the I/Os after resetting is detected and is transmitted as $\overline{INT}$. Reading from or writing to another device does not affect the interrupt circuit. This device does not have internal configuration or status registers. Instead, read or write to the device I/Os directly after sending the device address (see 图 8-6 and 图 8-7).

By sending an interrupt signal on this line, the remote I/O can inform the microcontroller if there is incoming data on its ports, without having to communicate via the I^2C bus. Thus, the PCF8575 can remain a simple target device.

Every data transmission to or from the PCF8575 must consist of an even number of bytes. The first data byte in every pair refers to port 0 (P07 – P00), and the second data byte in every pair refers to port 1 (P17 – P10). To write to the ports (output mode), the controller first addresses the target device, setting the last bit of the byte containing the target address to logic 0. The PCF8575 acknowledges, and the controller sends the first data byte for P07 – P00. After the first data byte is acknowledged by the PCF8575, the second data byte (P17 – P10) is sent by the controller. Once again, the PCF8575 acknowledges the receipt of the data, after which this 16-bit data is presented on the port lines.

The number of data bytes that can be sent successively is not limited. After every two bytes, the previous data is overwritten. When the PCF8575 receives the pairs of data bytes, the first byte is referred to as P07 – P00 and the second byte as P17 – P10. The third byte is referred to as P07 – P00, the fourth byte as P17 – P10, and so on.

Before reading from the PCF8575, all ports desired as input should be set to logic 1. To read from the ports (input mode), the controller first addresses the target device, setting the last bit of the byte containing the target address to logic 1. The data bytes that follow on the SDA are the values on the ports. If the data on the input port changes faster than the controller can read, this data may be lost.

When power is applied to V_{CC}, an internal power-on reset holds the PCF8575 in a reset state until V_{CC} has reached V_{POR}. At that time, the reset condition is released, and the device I^2C-bus state machine initializes the bus to its default state.

The hardware pins (A0, A1, and A2) are used to program and vary the fixed I^2C address and allow up to eight devices to share the same I^2C bus or SMBus. The fixed I^2C address of the PCF8575 is the same as the PCF8575C, PCF8574, PCA9535, and PCA9555, allowing up to eight of these devices, in any combination, to share the same I^2C bus or SMBus.

8.2 Functional Block Diagram

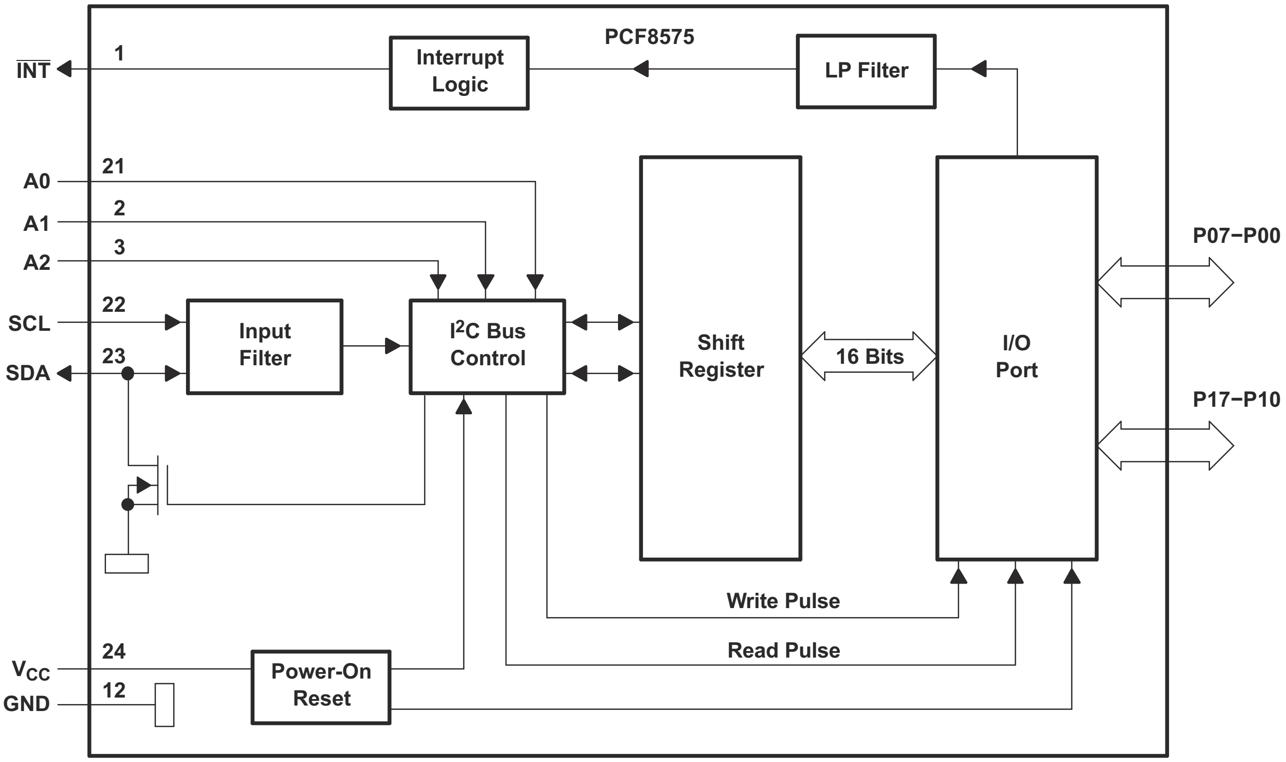


图 8-1. Logic Diagram (Positive Logic)

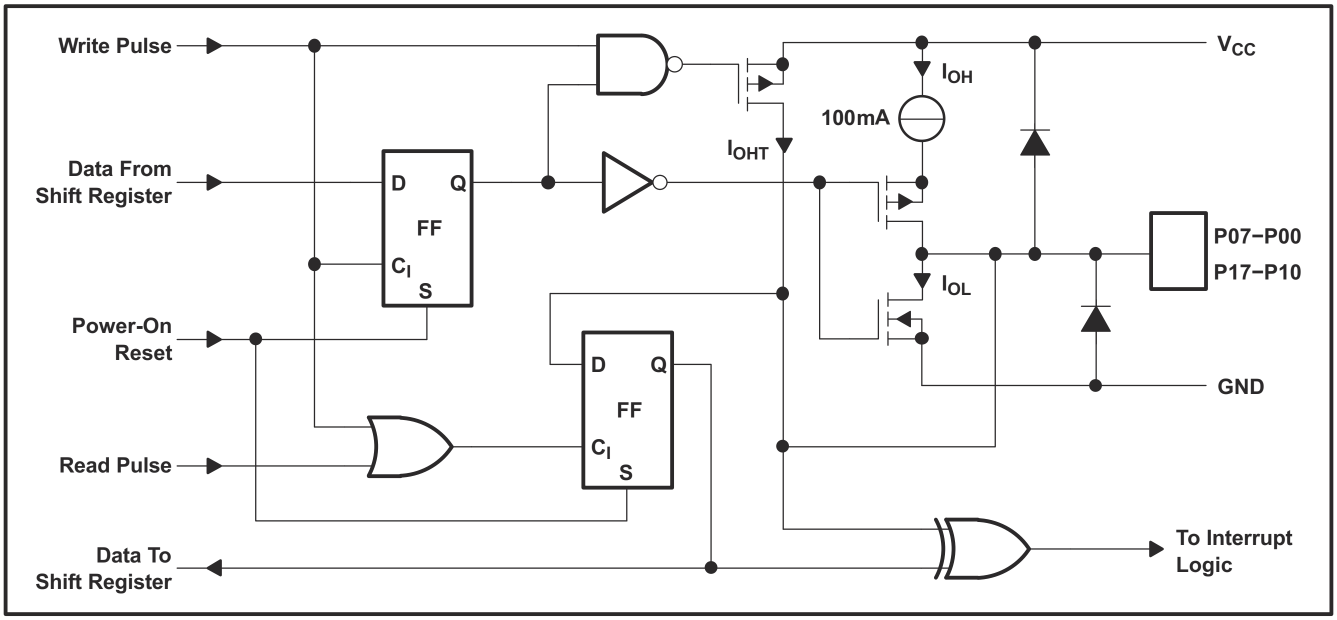


图 8-2. Simplified Schematic Diagram of Each P-Port Input or Output

8.3 Feature Description

8.3.1 I²C Interface

The bidirectional I²C bus consists of the serial clock (SCL) and serial data (SDA) lines. Both lines must be connected to a positive supply via a pullup resistor when connected to the output stages of a device. Data transfer may be initiated only when the bus is not busy.

I²C communication with this device is initiated by a controller sending a Start condition, a high-to-low transition on the SDA input/output while the SCL input is high (see 图 8-3). After the Start condition, the device address byte is sent, most significant bit (MSB) first, including the data direction bit (R/ $\overline{\text{W}}$). This device does not respond to the general call address. After receiving the valid address byte, this device responds with an ACK, a low on the SDA input/output during the high of the ACK-related clock pulse. The address inputs (A2 – A0) of the target device must not be changed between the Start and Stop conditions.

The data byte follows the address ACK. If the R/ $\overline{\text{W}}$ bit is high, the data from this device are the values read from the P port. If the R/ $\overline{\text{W}}$ bit is low, the data are from the controller, to be output to the P port. The data byte is followed by an ACK sent from this device. If other data bytes are sent from the controller, following the ACK, they are ignored by this device. Data are output only if complete bytes are received and acknowledged. The output data is valid at time (t_{pv}) after the low-to-high transition of SCL, during the clock cycle for the ACK.

On the I²C bus, only one data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the high pulse of the clock period, as changes in the data line at this time are interpreted as control commands (Start or Stop) (see 图 8-4).

A Stop condition, a low-to-high transition on the SDA input/output while the SCL input is high, is sent by the controller (see 图 8-3).

The number of data bytes transferred between the Start and Stop conditions from transmitter to receiver is not limited. Each byte of eight bits is followed by one ACK bit. The transmitter must release the SDA line before the receiver can send an ACK bit.

A target receiver that is addressed must generate an ACK after the reception of each byte. Also, a controller must generate an ACK after the reception of each byte that has been clocked out of the target transmitter. The device that acknowledges has to pull down the SDA line during the ACK clock pulse so that the SDA line is stable low during the high pulse of the ACK-related clock period (see 图 8-5). Setup and hold times must be taken into account.

A controller receiver must signal an end of data to the transmitter by not generating an acknowledge (NACK) after the last byte that has been clocked out of the target. This is done by the controller receiver by holding the SDA line high. In this event, the transmitter must release the data line to enable the controller to generate a Stop condition.

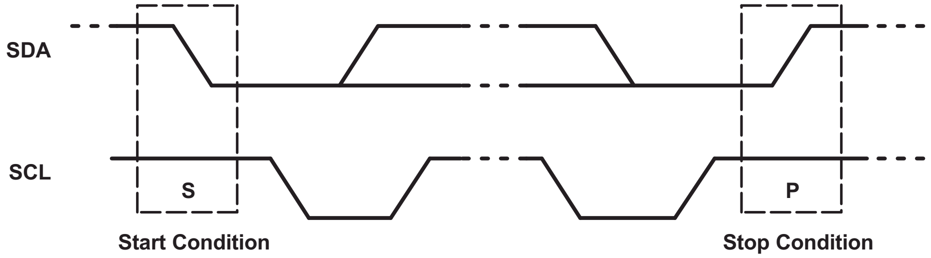


图 8-3. Definition of Start and Stop Conditions

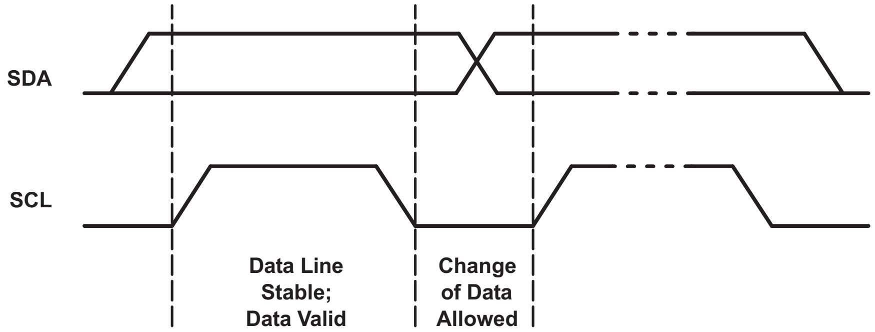


图 8-4. Bit Transfer

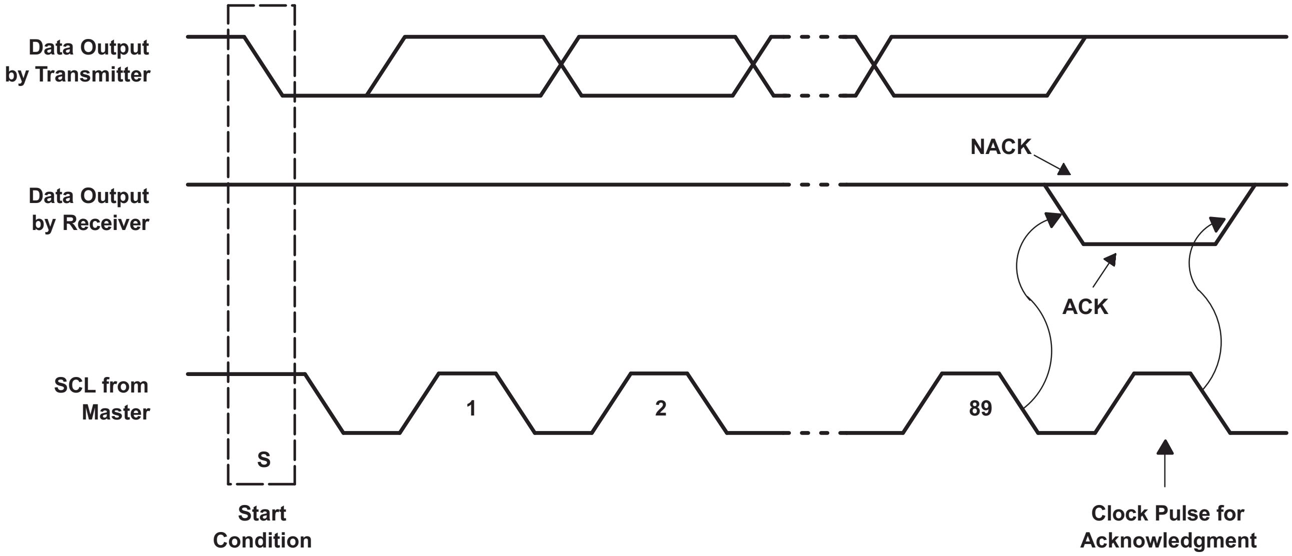


图 8-5. Acknowledgment on I²C Bus

8.3.2 Interface Definition

BYTE	BIT							
	7 (MSB)	**6**	**5**	**4**	**3**	**2**	**1**	**0 (LSB)**
I²C target address	L	H	L	L	A2	A1	A0	R/ $\overline{W}$
P0x I/O data bus	P07	P06	P05	P04	P03	P02	P01	P00
P1x I/O data bus	P17	P16	P15	P14	P13	P12	P11	P10

8.3.3 Address Reference

INPUTS			I²C BUS TARGET 8-BIT READ ADDRESS	I²C BUS TARGET 8-BIT WRITE ADDRESS
A2	A1	A0		
L	L	L	65 (decimal), 41 (hexadecimal)	64 (decimal), 40 (hexadecimal)
L	L	H	67 (decimal), 43 (hexadecimal)	66 (decimal), 42 (hexadecimal)
L	H	L	69 (decimal), 45 (hexadecimal)	68 (decimal), 44 (hexadecimal)
L	H	H	71 (decimal), 47 (hexadecimal)	70 (decimal), 46 (hexadecimal)
H	L	L	73 (decimal), 49 (hexadecimal)	72 (decimal), 48 (hexadecimal)
H	L	H	75 (decimal), 4B (hexadecimal)	74 (decimal), 4A (hexadecimal)
H	H	L	77 (decimal), 4D (hexadecimal)	76 (decimal), 4C (hexadecimal)
H	H	H	79 (decimal), 4F (hexadecimal)	78 (decimal), 4E (hexadecimal)

8.4 Device Functional Modes

图 8-6 and 图 8-7 show the address and timing diagrams for the write and read modes, respectively.

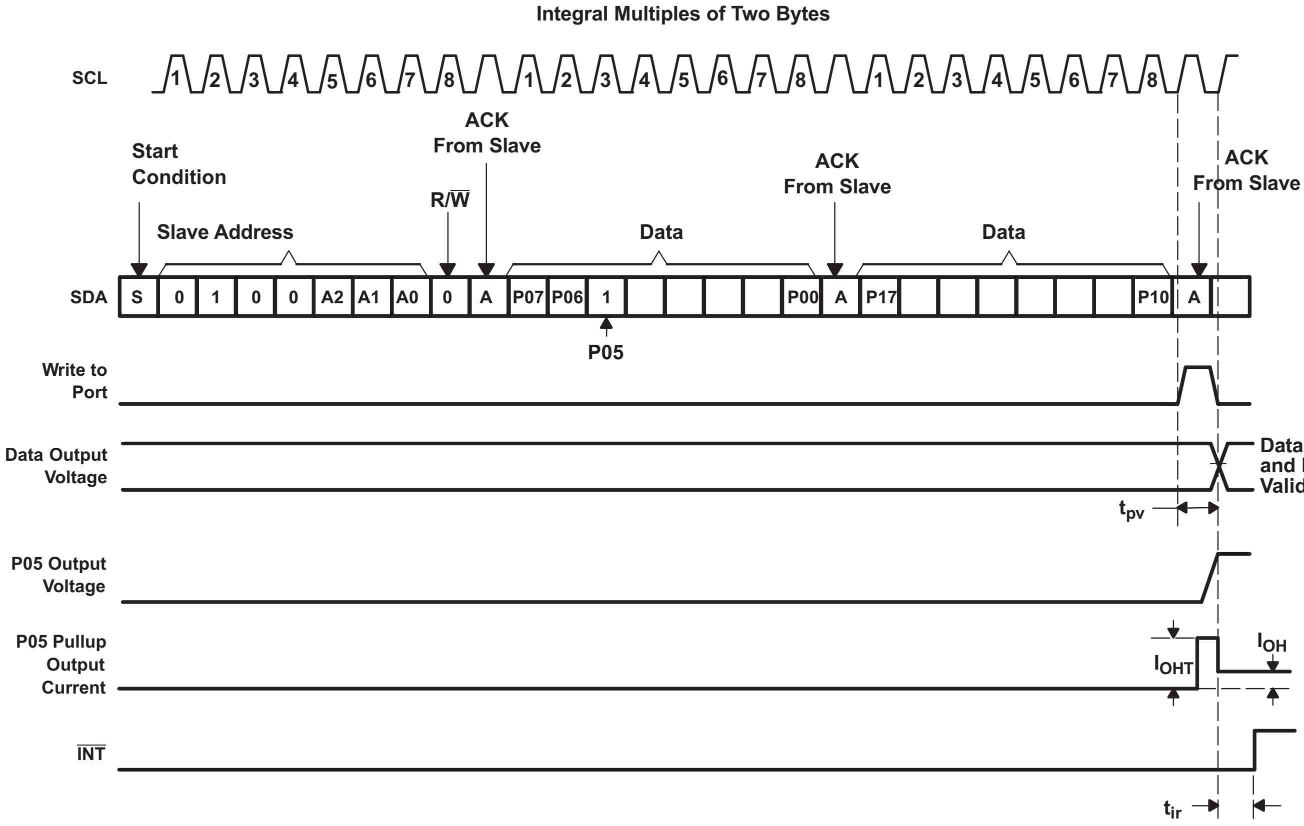


图 8-6. Write Mode (Output)

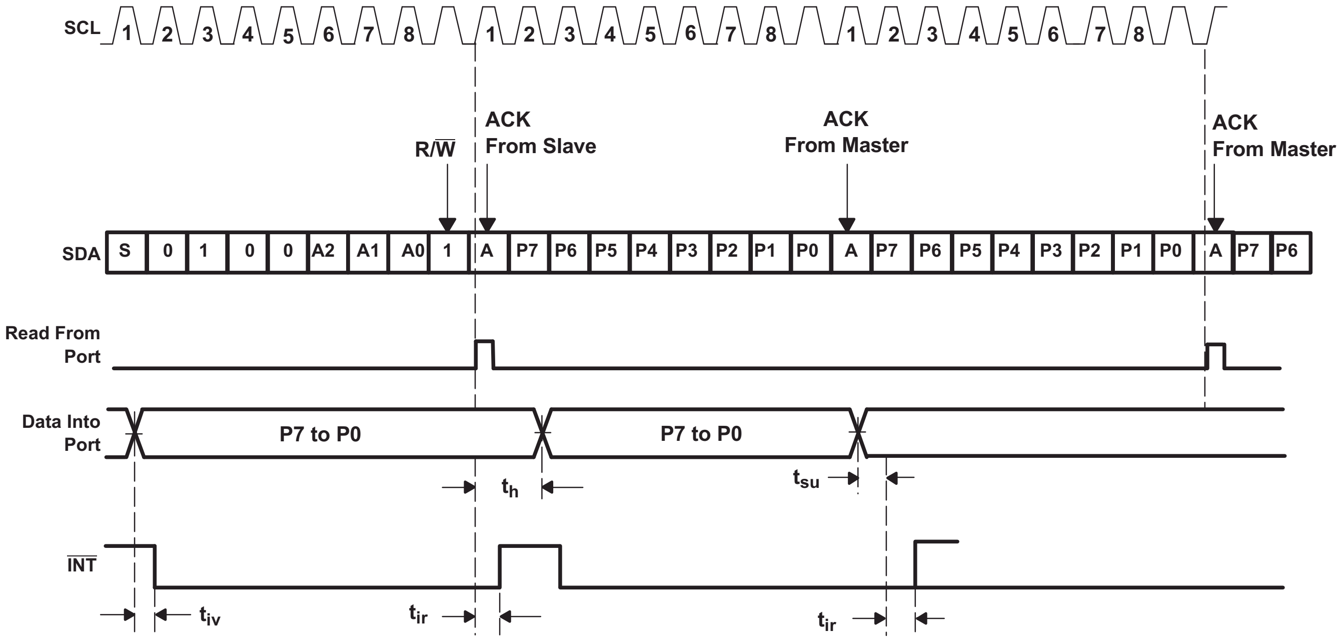


图 8-7. Read Mode (Input)

9 Application and Implementation

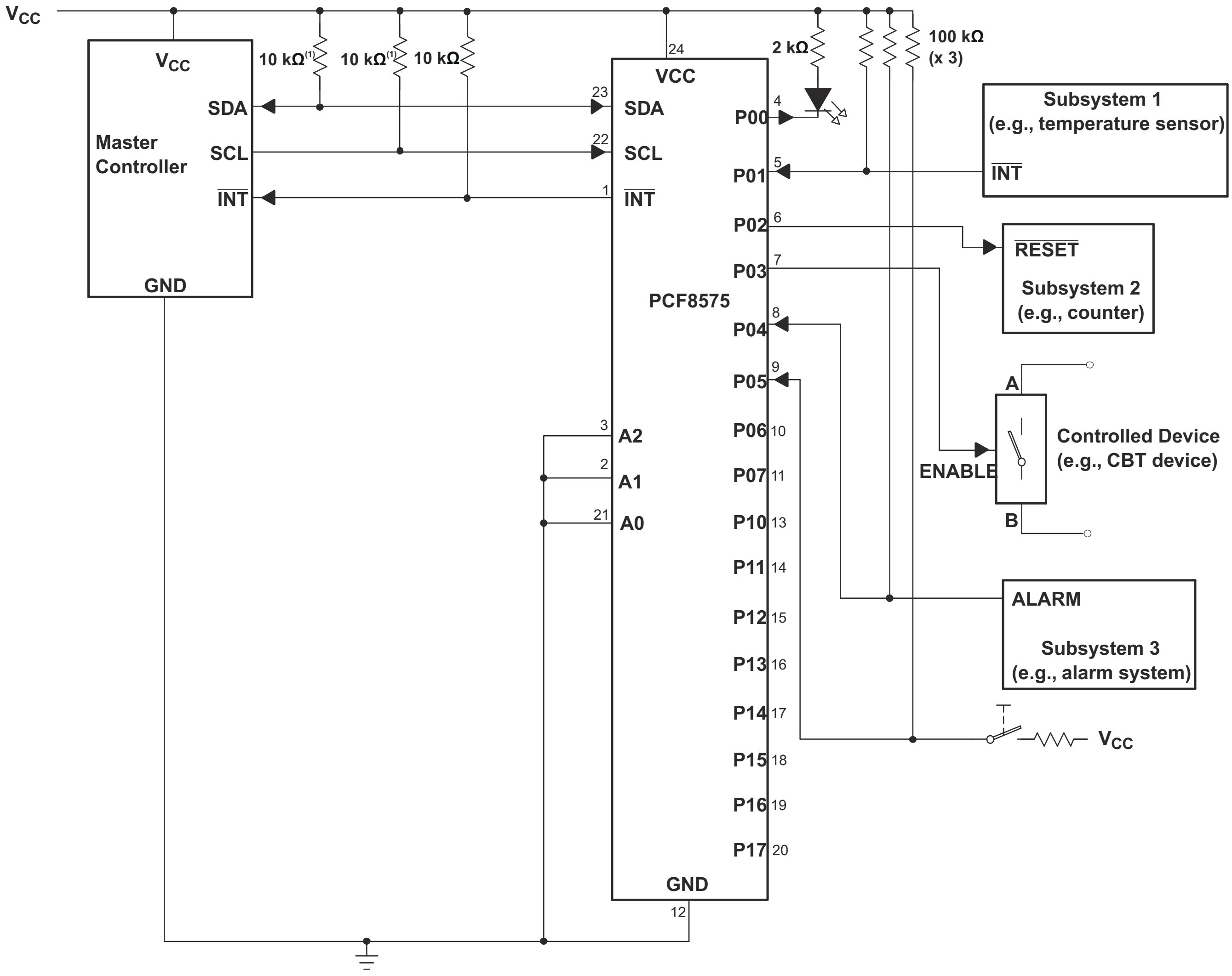
备注

以下应用部分中的信息不属于 TI 器件规格的范围，TI 不担保其准确性和完整性。TI 的客 户应负责确定器件是否适用于其应用。客户应验证并测试其设计，以确保系统功能。

9.1 Application Information

图 9-1 shows an application in which PCF8575 can be used.

9.2 Typical Application



A. The SCL and SDA pins must be tied directly to VCC because if SCL and SDA are tied to an auxiliary power supply that could be powered on while VCC is powered off, then the supply current, ICC, will increase as a result.
B. Device address is configured as 0100000 for this example.
C. P0, P2, and P3 are configured as outputs.
D. P1, P4, and P5 are configured as inputs.
E. P6 and P7 are not used and must be configured as outputs.

图 9-1. Application Schematic

9.2.1 Design Requirements

9.2.1.1 Minimizing I_{CC} When I/Os Control LEDs

When the I/Os are used to control LEDs, normally they are connected to V_{CC} through a resistor as shown in 图 9-1. For a P-port configured as an input, I_{CC} increases as V_I becomes lower than V_{CC}. The LED is a diode, with threshold voltage V_T, and when a P-port is configured as an input the LED will be off but V_I is a V_T drop below V_{CC}.

For battery-powered applications, it is essential that the voltage of P-ports controlling LEDs is greater than or equal to V_{CC} when the P-ports are configured as input to minimize current consumption. 图 9-2 shows a high-value resistor in parallel with the LED. 图 9-3 shows V_{CC} less than the LED supply voltage by at least V_T. Both of these methods maintain the I/O V_I at or above V_{CC} and prevents additional supply current consumption when the P-port is configured as an input and the LED is off.

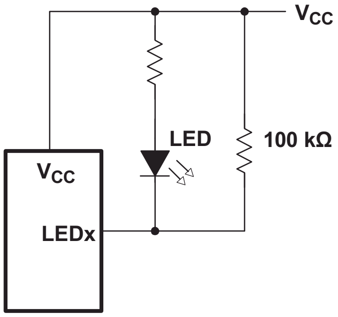


图 9-2. High-Value Resistor in Parallel With LED

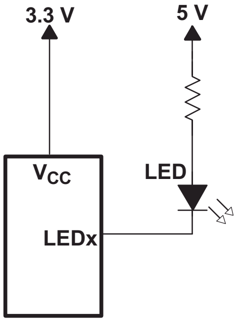


图 9-3. Device Supplied by a Lower Voltage

9.2.2 Detailed Design Procedure

The pull-up resistors, R_P, for the SCL and SDA lines need to be selected appropriately and take into consideration the total capacitance of all targets on the I^2C bus. The minimum pull-up resistance is a function of V_{CC}, $V_{OL,(max)}$, and I_{OL}:

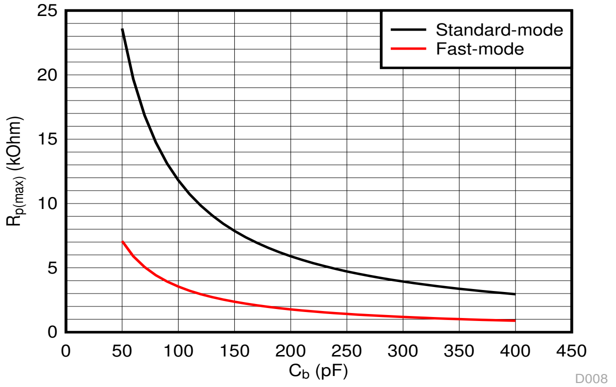
$$R_{p(min)} = \frac{V_{CC} - V_{OL(max)}}{I_{OL}} \tag{1}$$

The maximum pull-up resistance is a function of the maximum rise time, t_r (300 ns for fast-mode operation, f_{SCL} = 400 kHz) and bus capacitance, C_b:

$$R_{p(max)} = \frac{t_r}{0.8473 \times C_b} \tag{2}$$

The maximum bus capacitance for an I^2C bus must not exceed 400 pF for standard-mode or fast-mode operation. The bus capacitance can be approximated by adding the capacitance of the PCF8575, C_i for SCL or C_{io} for SDA, the capacitance of wires/connections/traces, and the capacitance of additional targets on the bus.

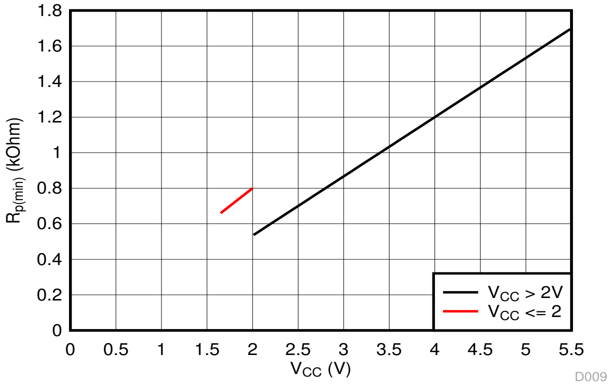
9.2.3 Application Curves



Standard-mode (f_{SCL}= 100 kHz, t_r = 1 μs)

Fast-mode (f_{SCL}= 400 kHz, t_r= 300 ns)

图 9-4. Maximum Pull-Up Resistance ($R_{p(max)}$) vs Bus Capacitance (C_b)



V_{OL} = 0.2*V_{CC}, I_{OL} = 2 mA
when $V_{CC} \leqslant 2$ V
V_{OL} = 0.4 V, I_{OL} = 3 mA
when V_{CC} > 2 V

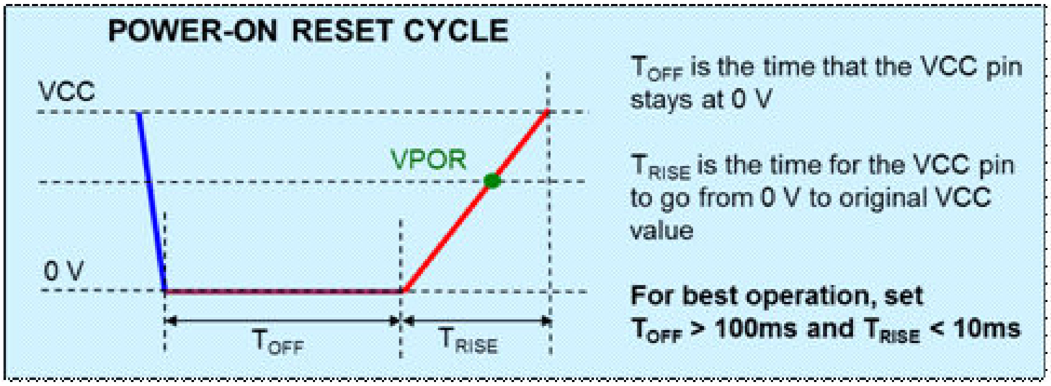
图 9-5. Minimum Pull-Up Resistance ($R_{p(min)}$) vs Pull-Up Reference Voltage (V_{CC})

9.3 Power Supply Recommendations

The operating power-supply voltage range of the PCF8575 is 2.5 V to 5.5 V applied at the VCC pin. When the PCF8575 is powered on for the first time or anytime the device needs to be reset by cycling the power supply, the power-on reset requirements must be followed to ensure the I^2C bus logic is initialized properly.

9.3.1 Power-On Reset

A power-on reset condition can be missed if the VCC ramps are outside specification listed below.



9.3.2 System Impact

If ramp conditions are outside timing allowances above, POR condition can be missed, causing the device to lock up.

9.4 Layout

9.4.1 Layout Guidelines

For printed circuit board (PCB) layout of the PCF8575 device, common PCB layout practices should be followed but additional concerns related to high-speed data transfer such as matched impedances and differential pairs are not a concern for I^2C signal speeds.

In all PCB layouts, it is a best practice to avoid right angles in signal traces, to fan out signal traces away from each other upon leaving the vicinity of an integrated circuit (IC), and to use thicker trace widths to carry higher amounts of current that commonly pass through power and ground traces. By-pass and de-coupling capacitors are commonly used to control the voltage on the V_{CC} pin, using a larger capacitor to provide additional power in the event of a short power supply glitch and a smaller capacitor to filter out high-frequency ripple. These capacitors should be placed as close to the PCF8575 as possible. These best practices are shown in 图 9-6.

For the layout example provided in 图 9-6, it would be possible to fabricate a PCB with only 2 layers by using the top layer for signal routing and the bottom layer as a split plane for power (V_{CC}) and ground (GND). However, a 4 layer board is preferable for boards with higher density signal routing. On a 4 layer PCB, it is common to route signals on the top and bottom layer, dedicate one internal layer to a ground plane, and dedicate the other internal layer to a power plane. In a board layout using planes or split planes for power and ground, vias are placed directly next to the surface mount component pad which needs to attach to V_{CC} or GND and the via is connected electrically to the internal layer or the other side of the board. Vias are also used when a signal trace needs to be routed to the opposite side of the board, but this technique is not demonstrated in 图 9-6.

9.4.2 Layout Example

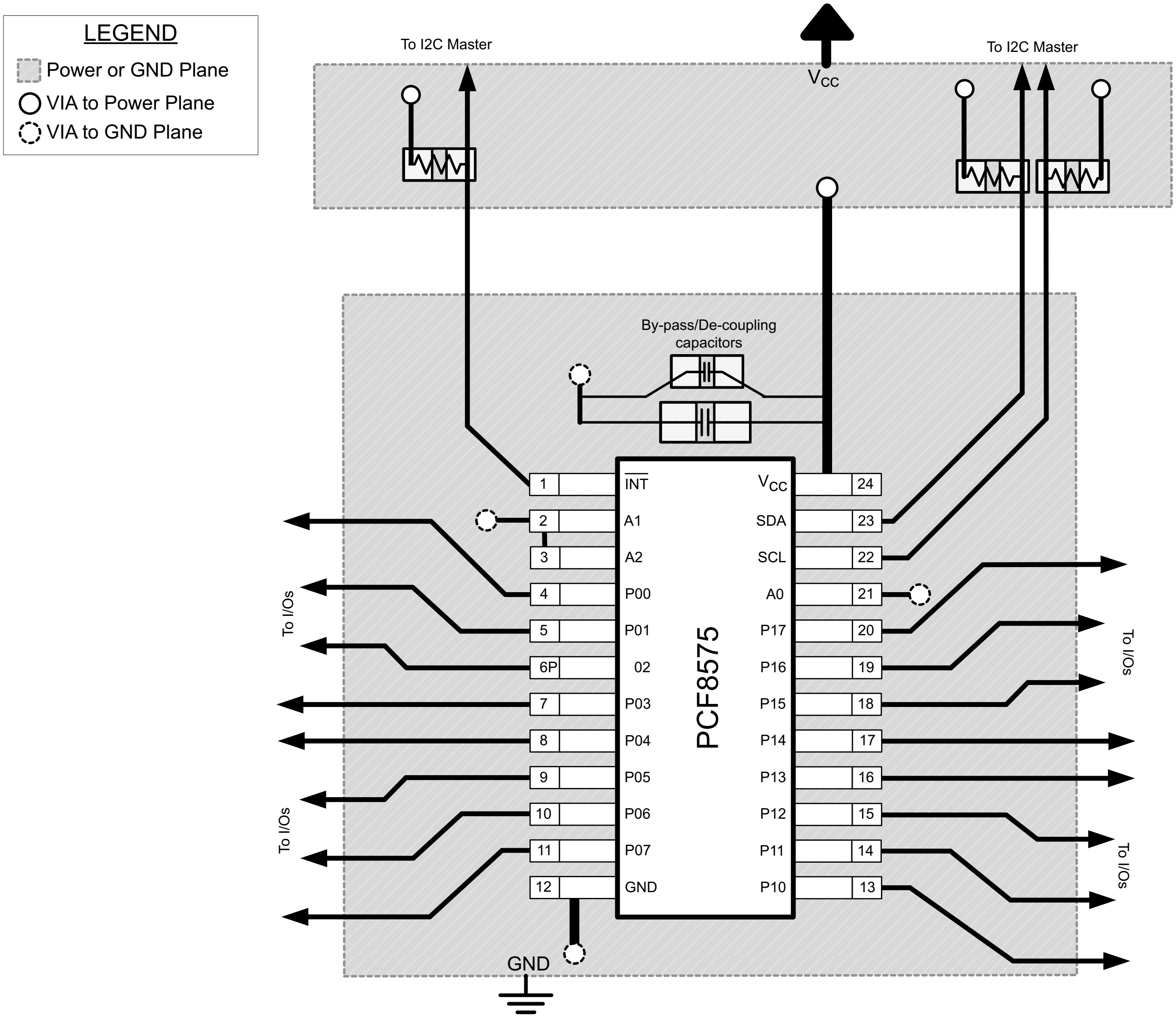


图 9-6. Layout Example for PCF8575

10 Device and Documentation Support

10.1 Device Support

10.2 Documentation Support

10.3 接收文档更新通知

要接收文档更新通知，请导航至 ti.com 上的器件产品文件夹。点击*通知* 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

10.4 支持资源

TI E2E™ 中文支持论坛是工程师的重要参考资料，可直接从专家处获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题，获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的使用条款。

10.5 Trademarks

TI E2E™ is a trademark of Texas Instruments.
所有商标均为其各自所有者的财产。

10.6 静电放电警告

静电放电 (ESD) 会损坏这个集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

10.7 术语表

TI 术语表	本术语表列出并解释了术语、首字母缩略词和定义。

11 Revision History

注：以前版本的页码可能与当前版本的页码不同

Changes from Revision H (February 2020) to Revision I (August 2024) **Page**

- 将提到 I^2C 的旧术语实例通篇更新为控制器和目标.......... 1
- 将“器件信息”表更新为*封装信息* 表.......... 1
- Updated Thermal Information.......... 4
- Removed footnote #2 from Electrical Characteristics.......... 5
- Updated I_{IHL} test condition.......... 5

Changes from Revision G (August 2018) to Revision H (February 2020) **Page**

- Updated 图 8-6 16

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
PCF8575DBQR	ACTIVE	SSOP	DBQ	24	2500	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	PCF8575	Samples
PCF8575DBR	ACTIVE	SSOP	DB	24	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	PF575	Samples
PCF8575DGVR	ACTIVE	TVSOP	DGV	24	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	PF575	Samples
PCF8575DW	OBSOLETE	SOIC	DW	24		TBD	Call TI	Call TI	-40 to 85	PCF8575	
PCF8575DWR	ACTIVE	SOIC	DW	24	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	PCF8575	Samples
PCF8575PW	OBSOLETE	TSSOP	PW	24		TBD	Call TI	Call TI	-40 to 85	PF575	
PCF8575PWR	ACTIVE	TSSOP	PW	24	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	PF575	Samples
PCF8575PWRE4	ACTIVE	TSSOP	PW	24	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	PF575	Samples
PCF8575RGER	ACTIVE	VQFN	RGE	24	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	PF575 Q1	Samples

[1] The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

[2] **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

[3] MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

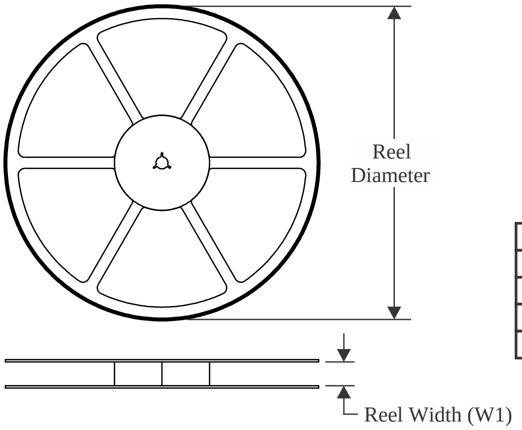
[4] There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

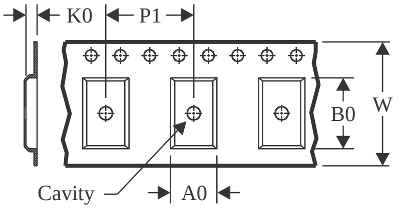
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

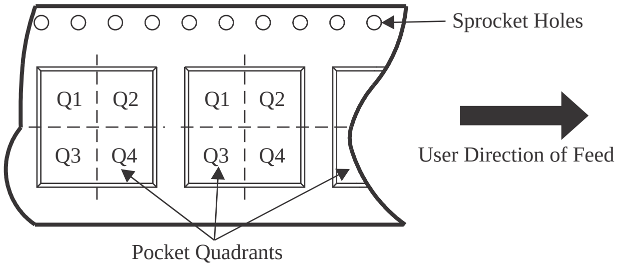


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

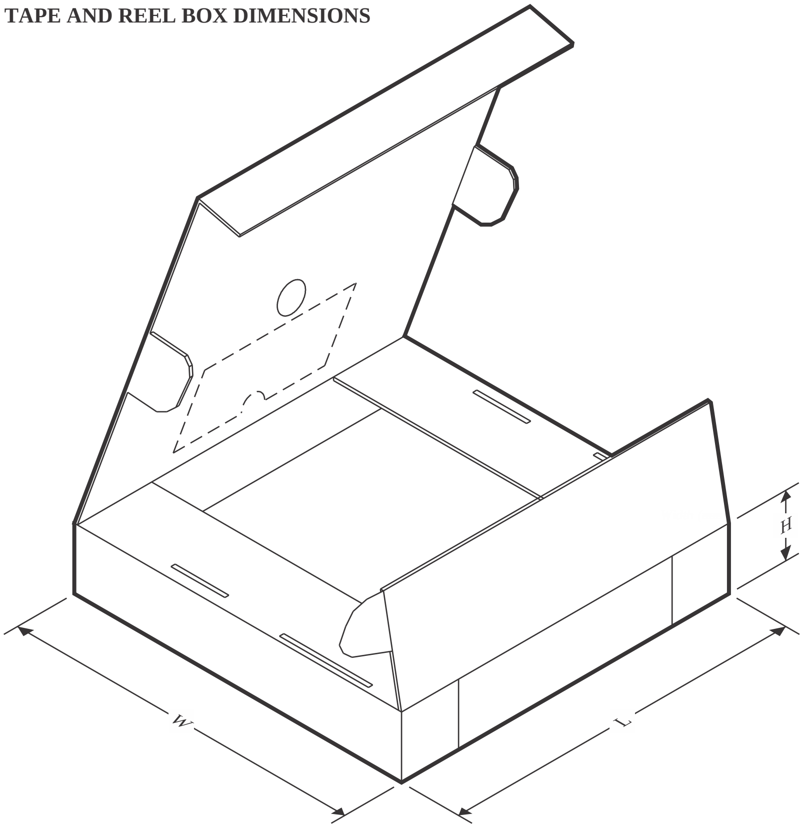
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
PCF8575DBQR	SSOP	DBQ	24	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
PCF8575DBR	SSOP	DB	24	2000	330.0	16.4	8.2	8.8	2.5	12.0	16.0	Q1
PCF8575DBR	SSOP	DB	24	2000	330.0	16.4	8.2	8.8	2.5	12.0	16.0	Q1
PCF8575DGVR	TVSOP	DGV	24	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
PCF8575DWR	SOIC	DW	24	2000	330.0	24.4	10.75	15.7	2.7	12.0	24.0	Q1
PCF8575PWR	TSSOP	PW	24	2000	330.0	16.4	6.95	8.3	1.6	8.0	16.0	Q1
PCF8575RGER	VQFN	RGE	24	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2

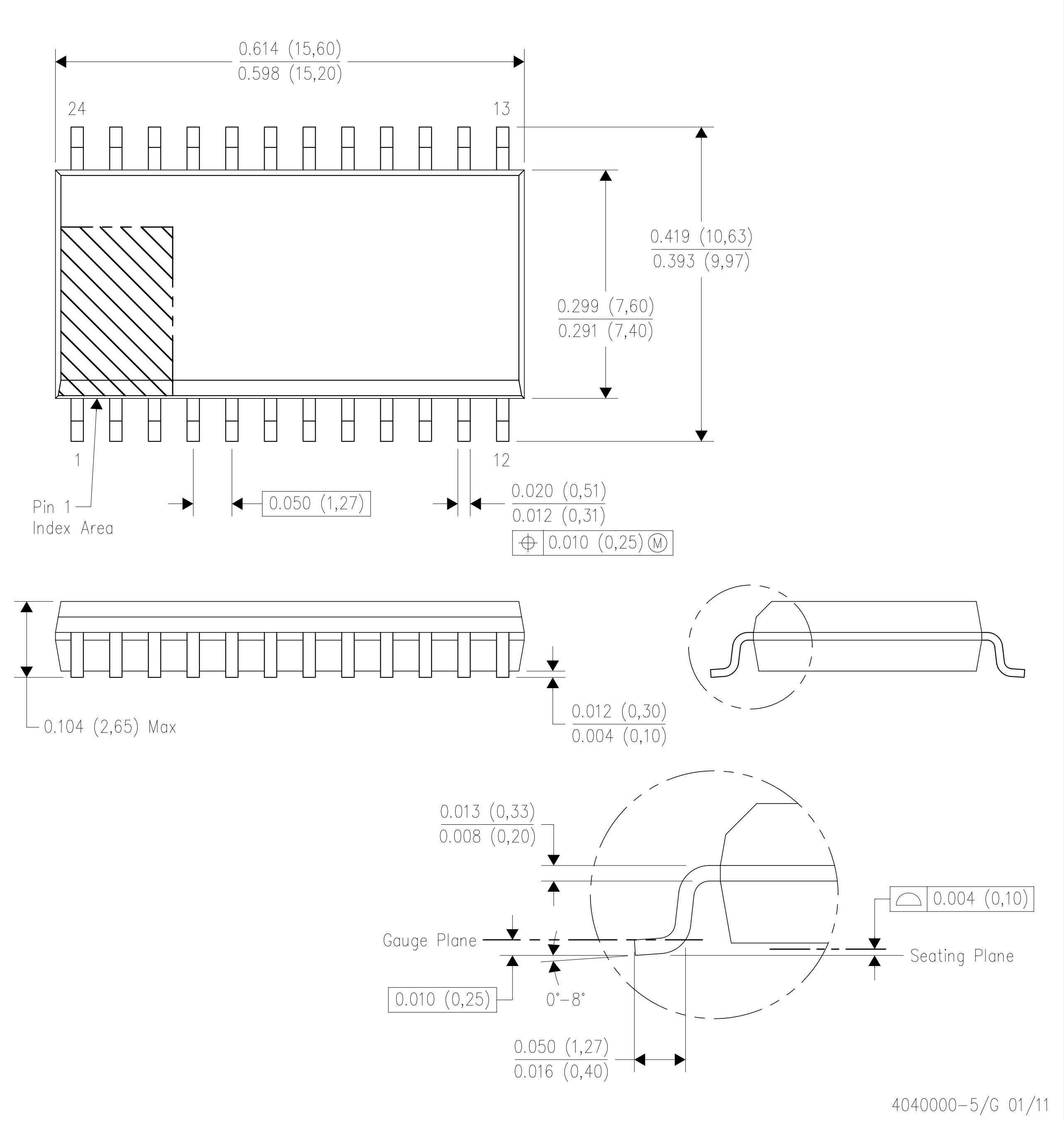
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

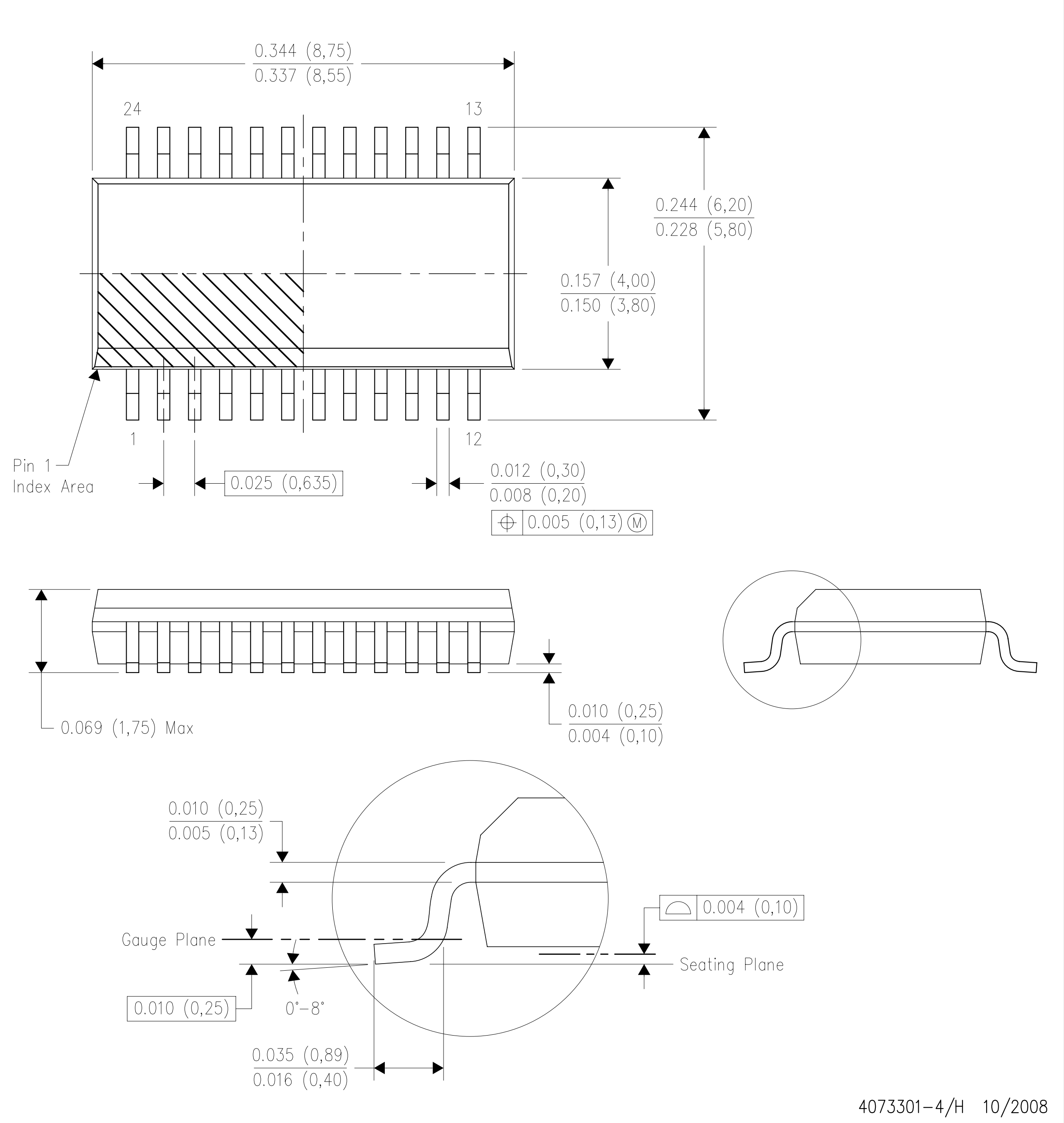
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
PCF8575DBQR	SSOP	DBQ	24	2500	356.0	356.0	35.0
PCF8575DBR	SSOP	DB	24	2000	356.0	356.0	35.0
PCF8575DBR	SSOP	DB	24	2000	356.0	356.0	35.0
PCF8575DGVR	TVSOP	DGV	24	2000	356.0	356.0	35.0
PCF8575DWR	SOIC	DW	24	2000	350.0	350.0	43.0
PCF8575PWR	TSSOP	PW	24	2000	356.0	356.0	35.0
PCF8575RGER	VQFN	RGE	24	3000	356.0	356.0	35.0

DW (R–PDSO–G24) PLASTIC SMALL OUTLINE

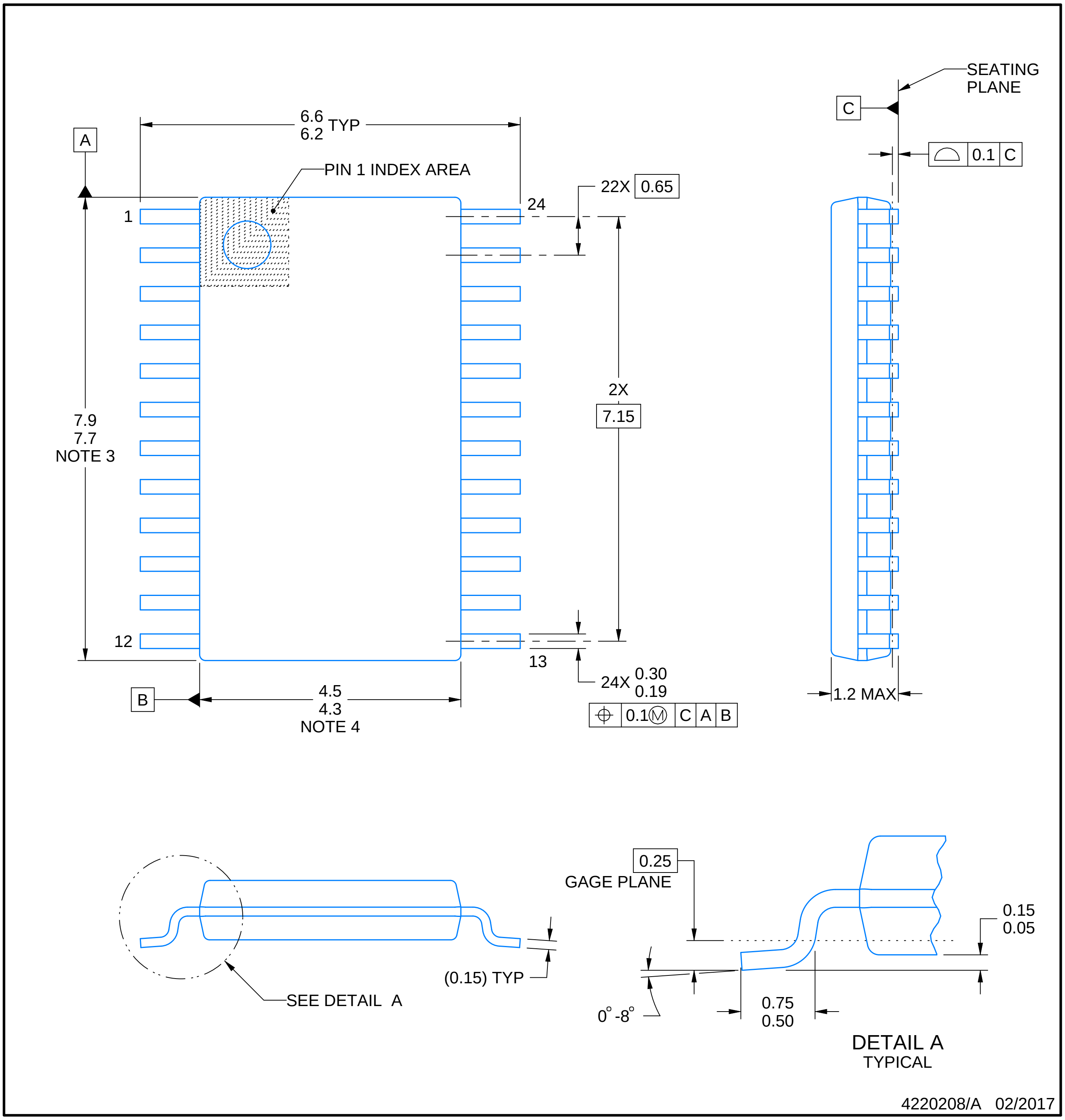


NOTES:
- A. All linear dimensions are in inches (millimeters). Dimensioning and tolerancing per ASME Y14.5M–1994.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
- D. Falls within JEDEC MS–013 variation AD.

DBQ (R–PDSO–G24) PLASTIC SMALL–OUTLINE PACKAGE

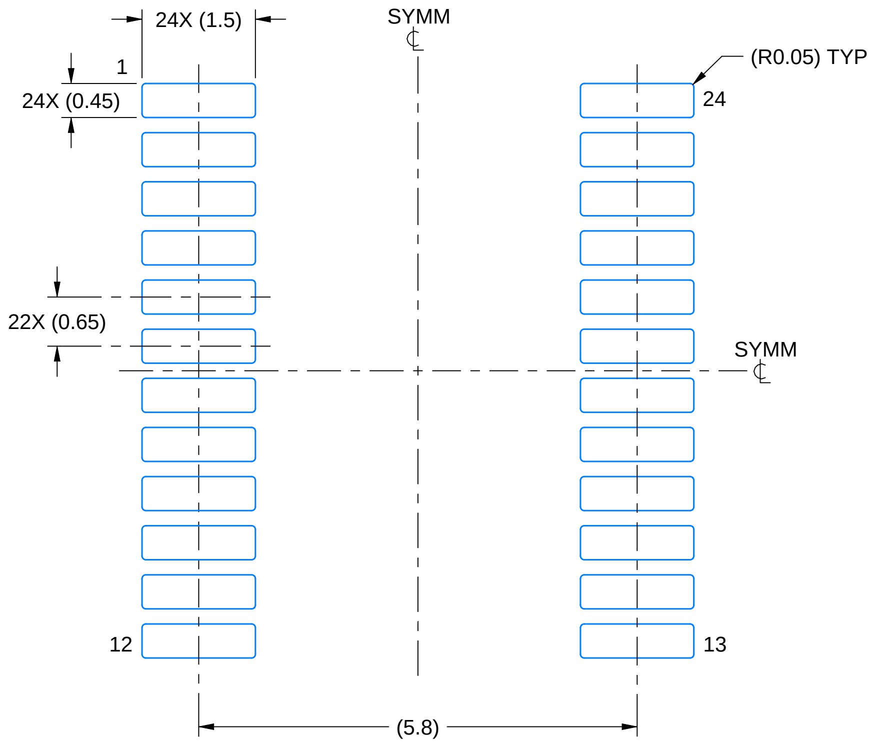


NOTES:
- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15) per side.
- D. Falls within JEDEC MO–137 variation AE.

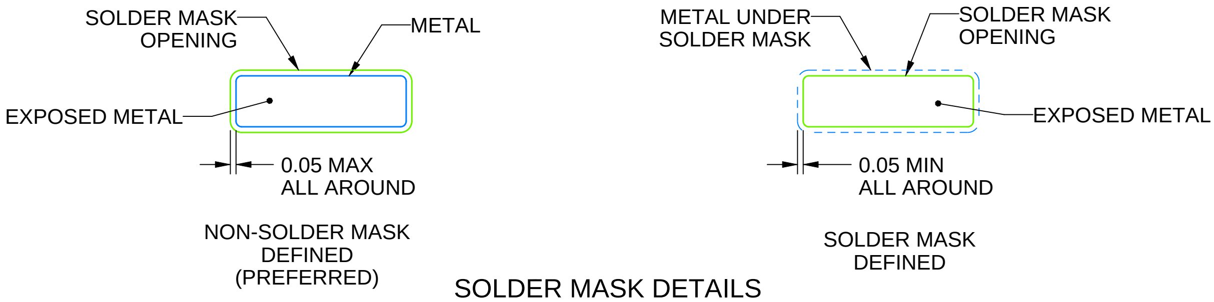


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

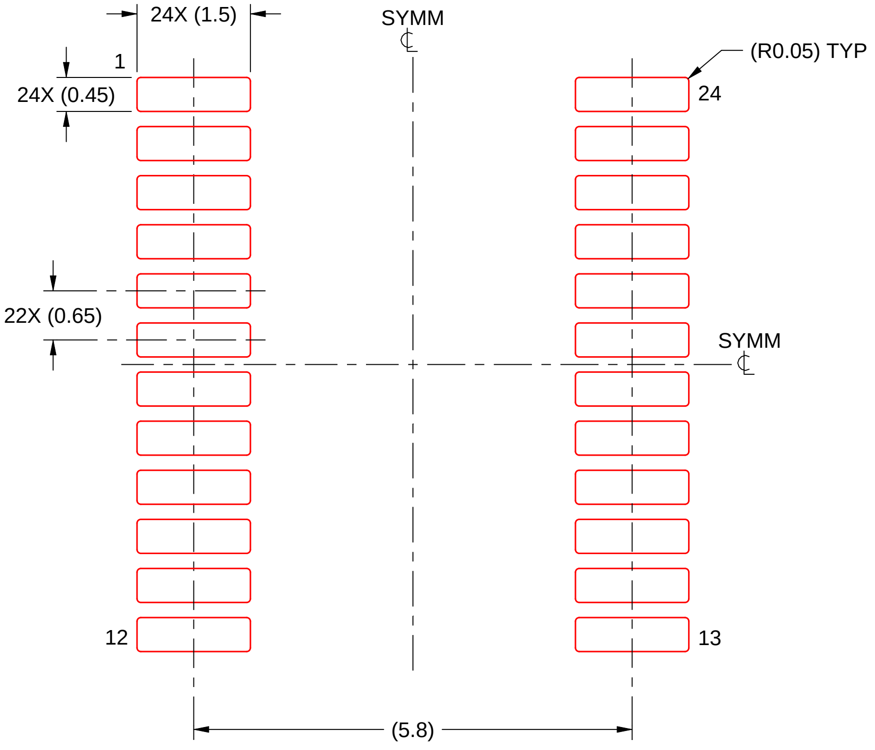


SOLDER MASK DETAILS

4220208/A 02/2017

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

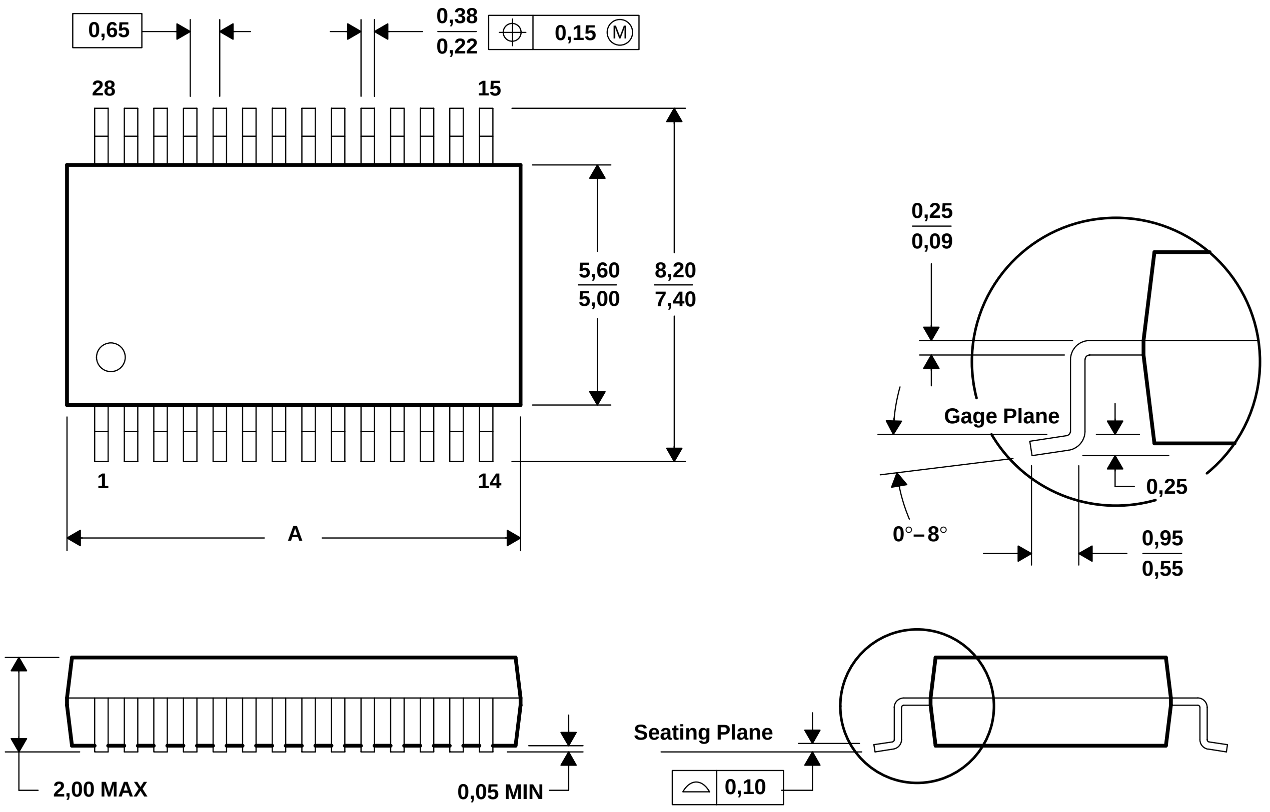
4220208/A 02/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

DB (R-PDSO-G**) PLASTIC SMALL-OUTLINE

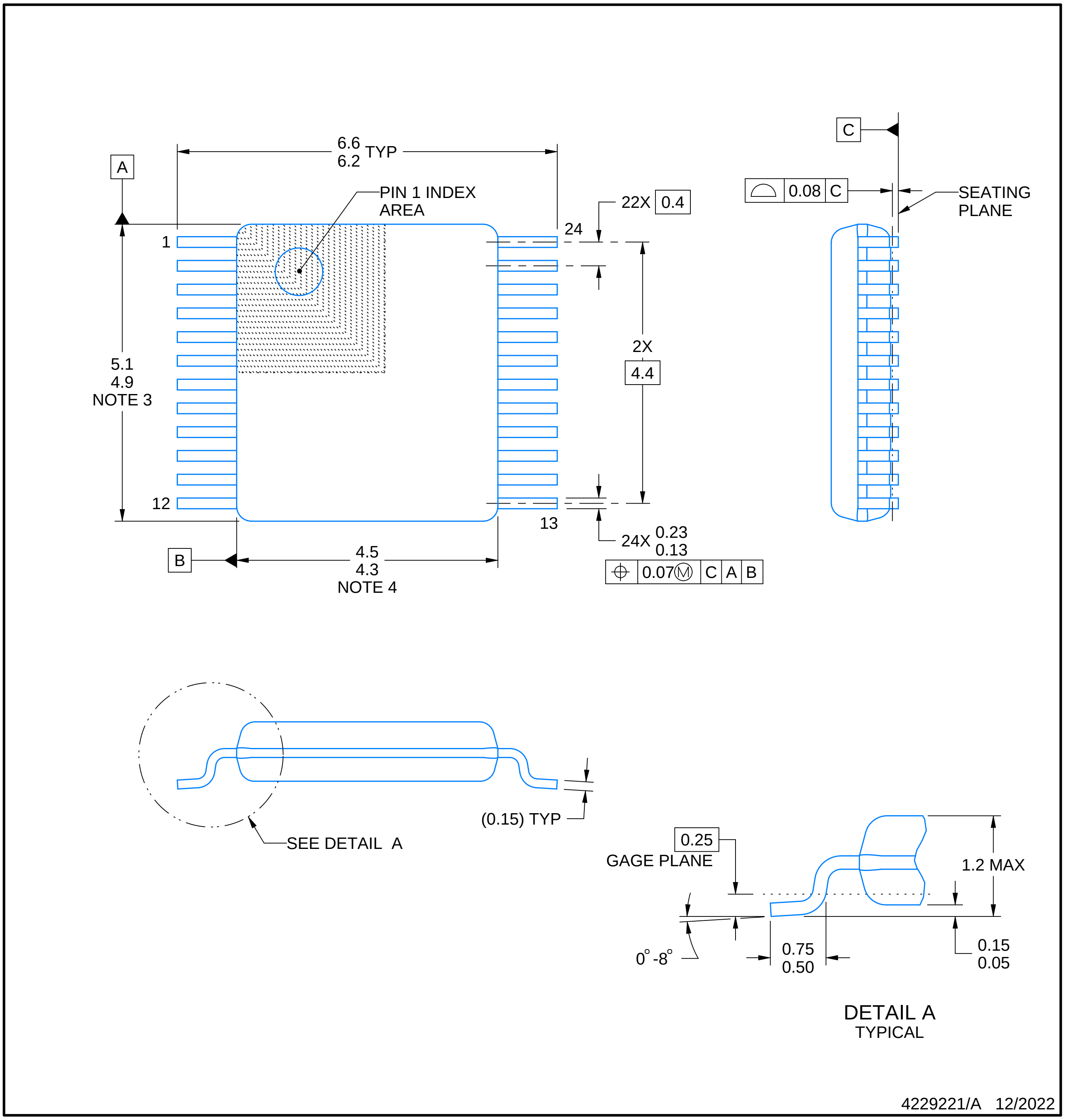
28 PINS SHOWN



PINS ** / DIM	14	16	20	24	28	30	38
A MAX	6,50	6,50	7,50	8,50	10,50	10,50	12,90
A MIN	5,90	5,90	6,90	7,90	9,90	9,90	12,30

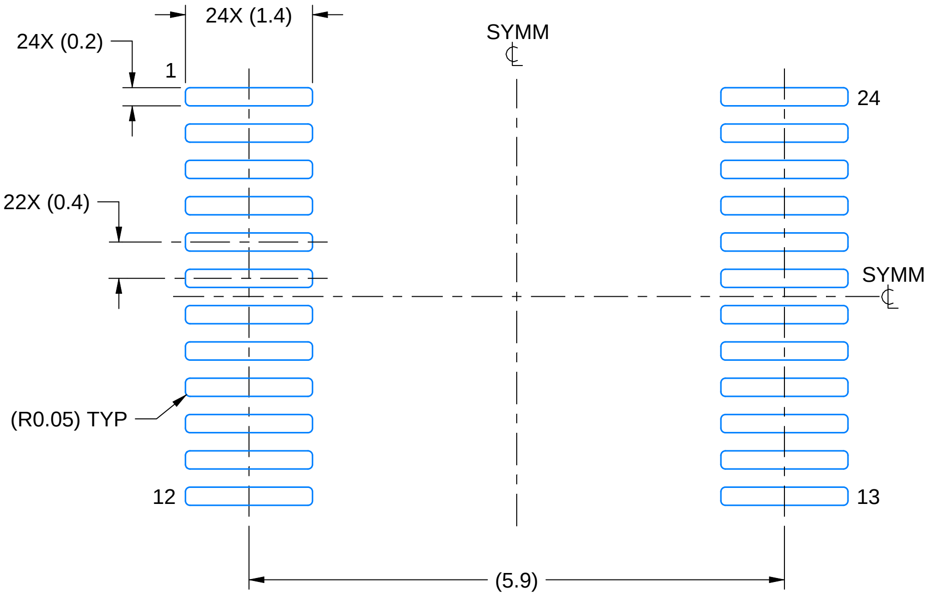
4040065 /E 12/01

NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
- D. Falls within JEDEC MO-150

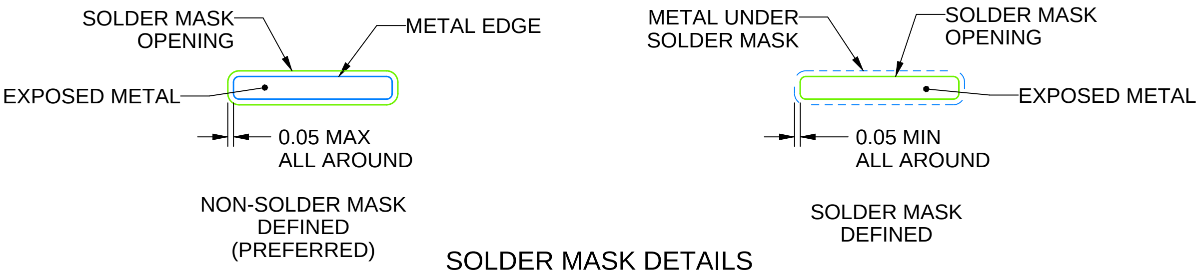


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 12X

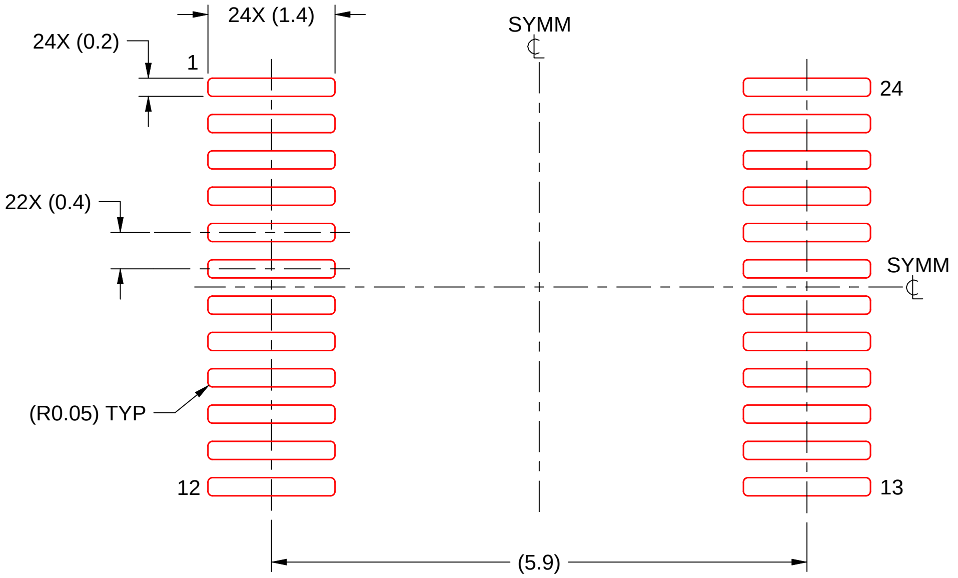


SOLDER MASK DETAILS

4229221/A 12/2022

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 12X

4229221/A 12/2022

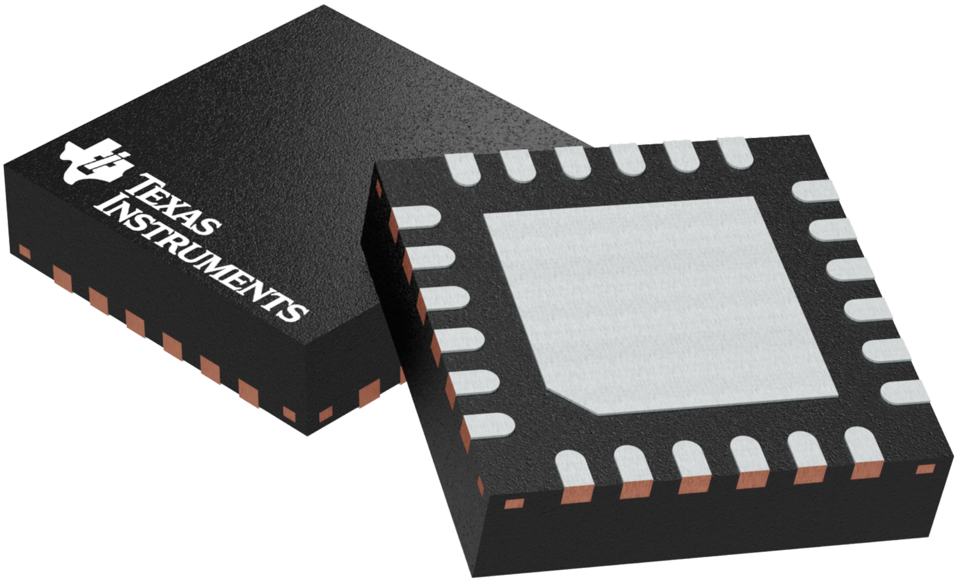
NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

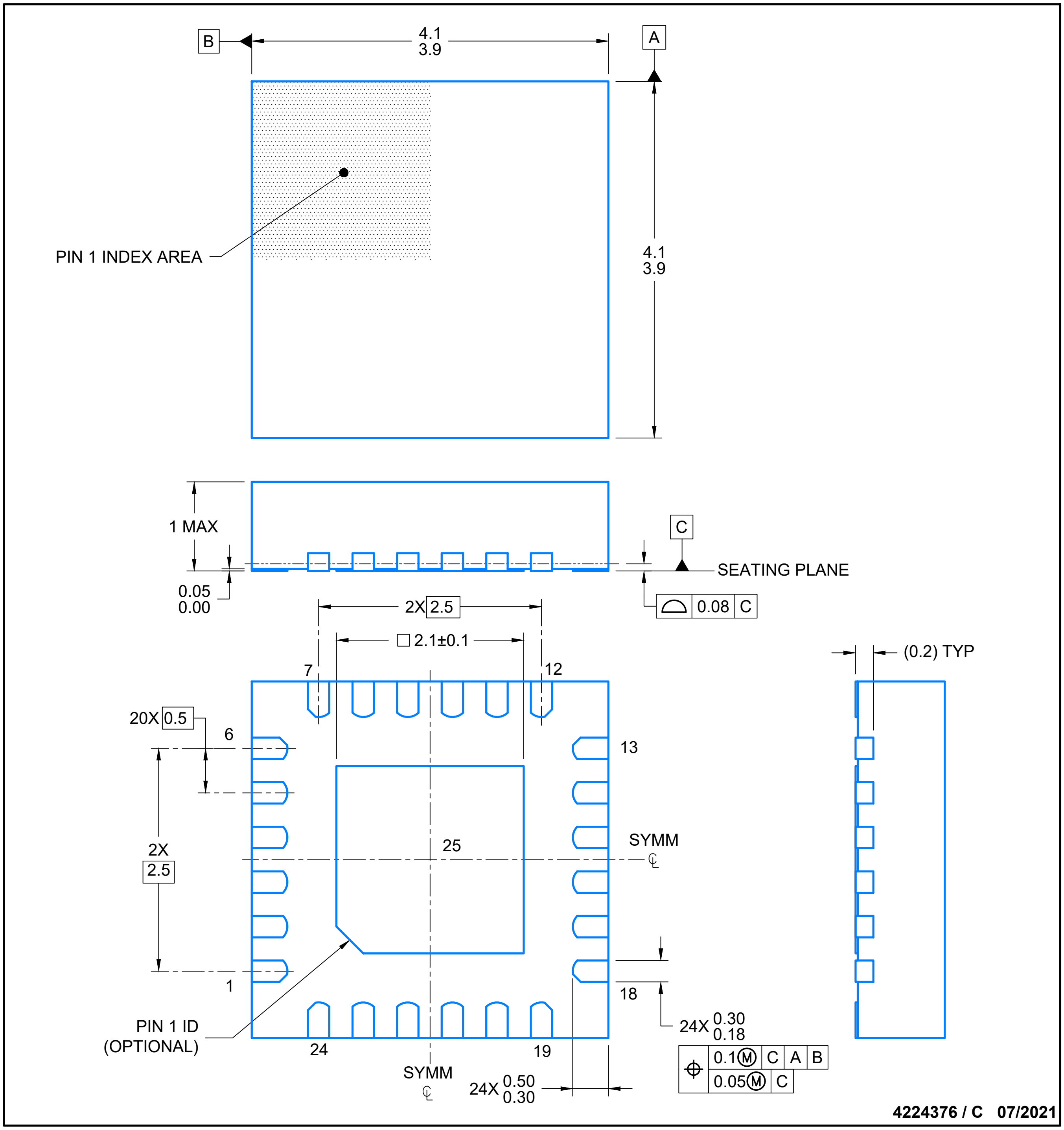
RGE 24

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



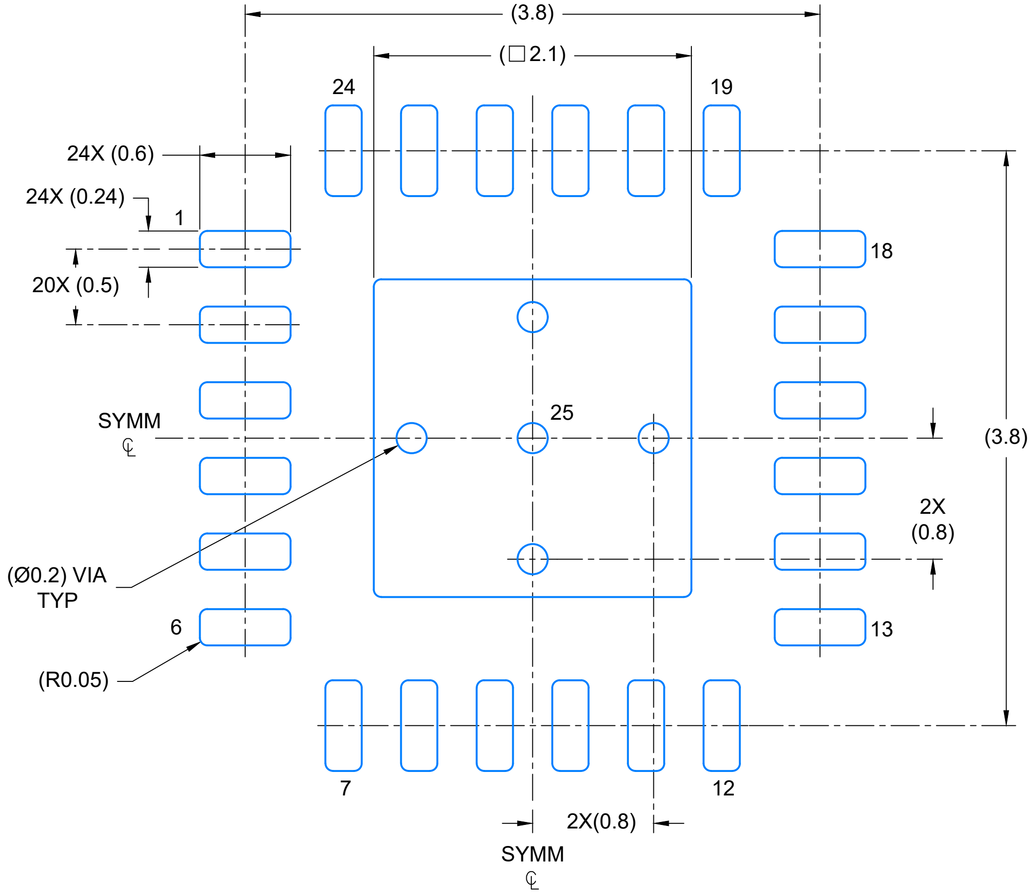
Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



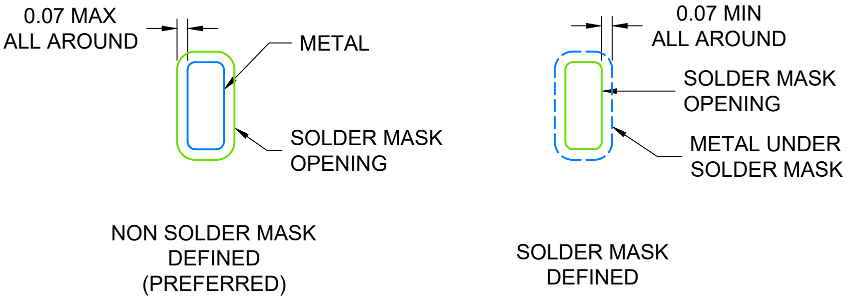
4224376 / C 07/2021

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
SCALE: 20X



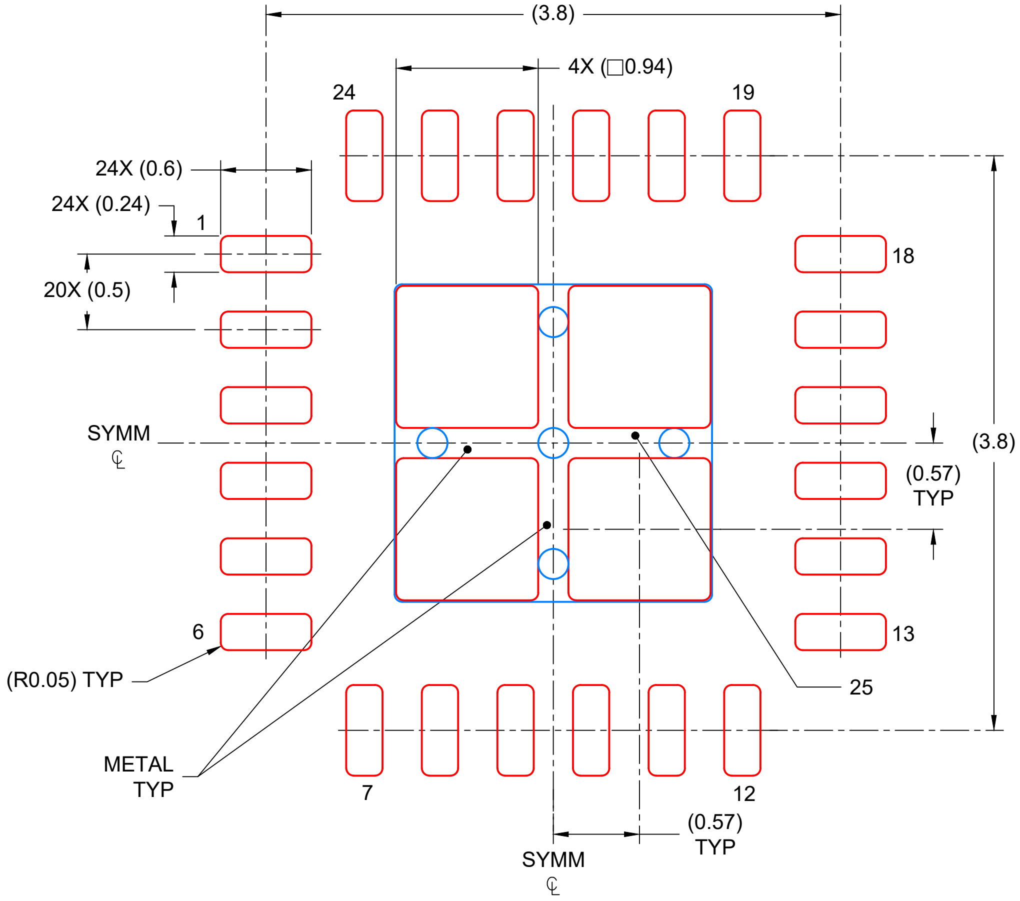
NON SOLDER MASK
DEFINED
(PREFERRED)

SOLDER MASK
DEFINED

SOLDER MASK DETAILS

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
80% PRINTED COVERAGE BY AREA
SCALE: 20X

NOTES: (continued)

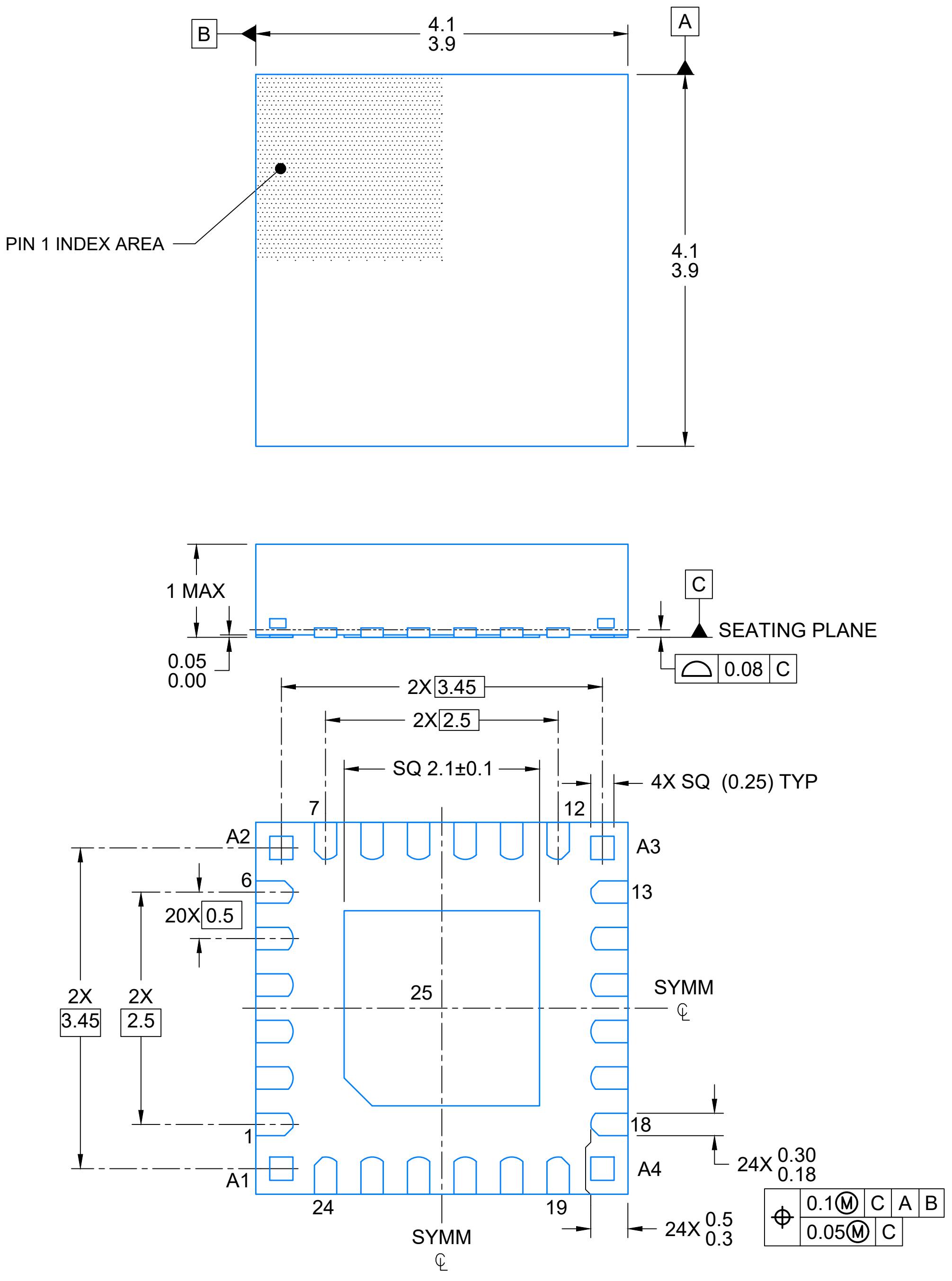
6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations..

PACKAGE OUTLINE

RGE0024R

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK-NO LEAD

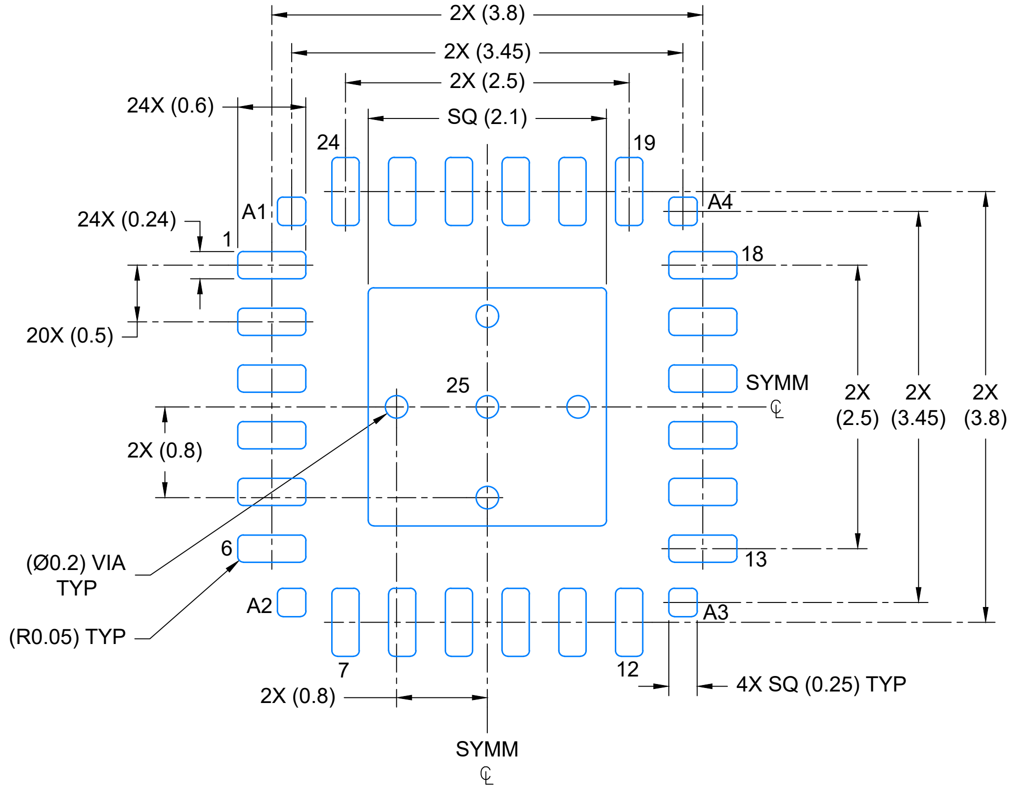


4225246/A 08/2019

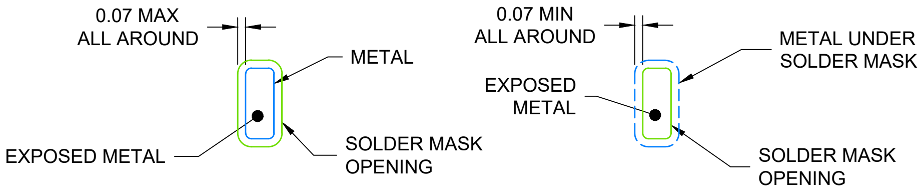
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.

EXAMPLE BOARD LAYOUT



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X



NON SOLDER MASK
DEFINED
(PREFERRED)

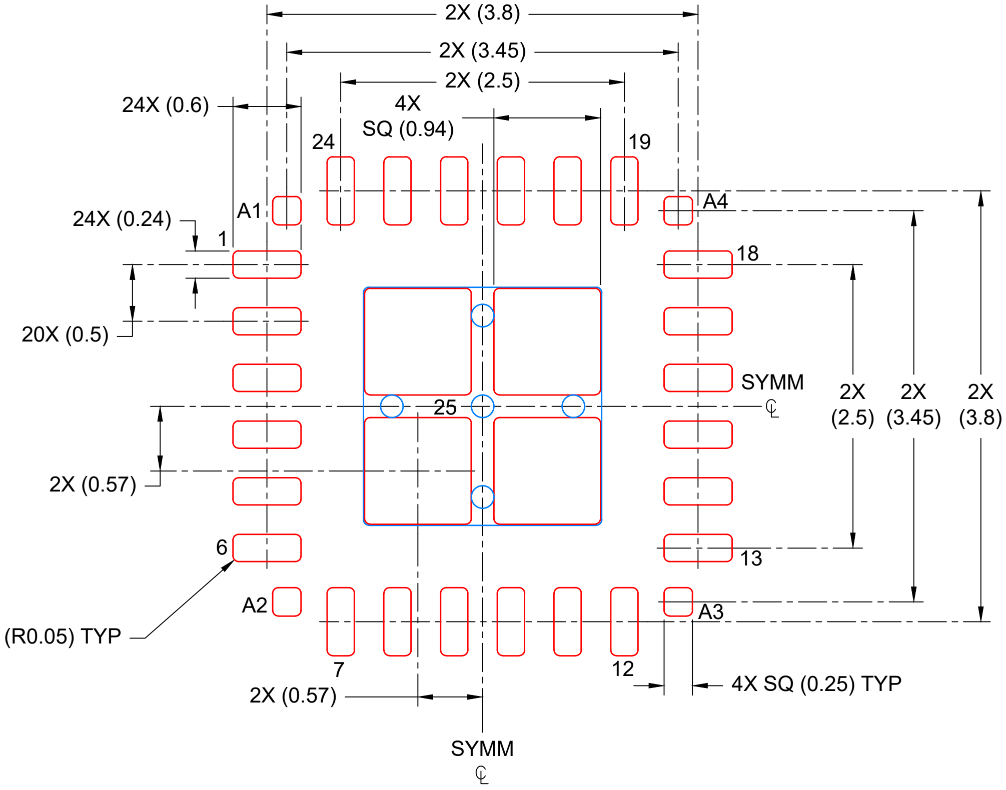
SOLDER MASK
DEFINED

SOLDER MASK DETAILS

4225246/A 08/2019

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
80% PRINTED COVERAGE BY AREA
SCALE: 15X

4225246/A 08/2019

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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