

## PCM3070 具有嵌入式 miniDSP 的立体声音频编解码器

### 1 特性

- 信噪比 (SNR) 为 100dB 的立体声音频数模转换器 (DAC)
- SNR 为 93dB 的立体声音频模数转换器 (ADC)
- 丰富的信号处理选项
- 嵌入式 miniDSP
- 6 个单端或 3 个全差分模拟输入
- 立体声双耳式耳机输出
- 立体声线路输出
- 超低噪声可编程增益放大器 (PGA)
- 模拟旁路模式
- 可编程锁相环 (PLL)
- 集成型低压降稳压器 (LDO)
- 5mm x 5mm、32 引脚四方扁平无引线 (QFN) 封装

### 2 应用

- 条形音箱
- 平板电视
- MP3 坞站
- 蜂窝电话坞站
- 其他立体声或 2.1 家用音频系统

### 3 说明

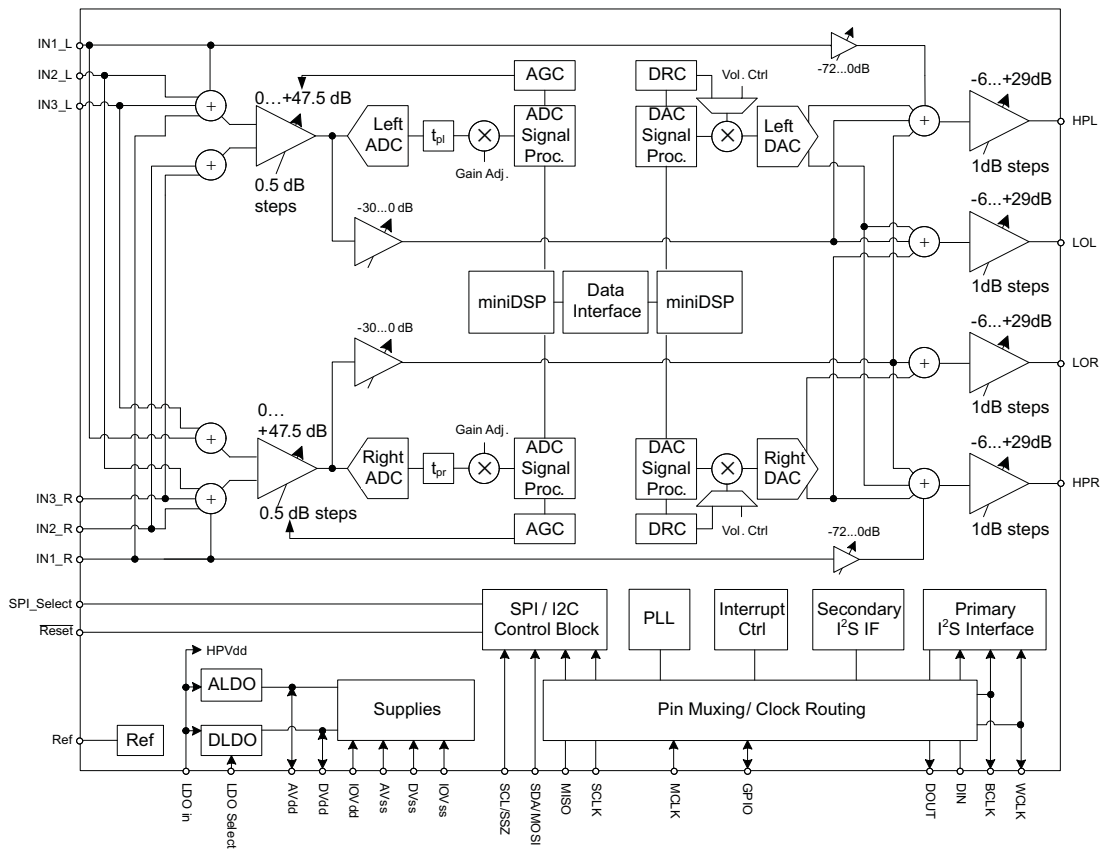
PCM3070 是一款灵活的立体声音频编解码器，配有可编程输入和输出、完全可编程 miniDSP、固定式预定义和可参数化信号处理块、集成式 PLL、集成式 LDO 以及灵活的数字接口。

器件信息(1)

| 器件型号    | 封装                    | 封装尺寸 (标称值)      |
|---------|-----------------------|-----------------|
| PCM3070 | 超薄四方扁平无引线 (VQFN) (32) | 5.00mm x 5.00mm |

(1) 要了解所有可用封装，请见数据表末尾的可订购产品附录。

### 4 LP38690 的



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## 5 修订历史记录

### Changes from Original (February 2011) to Revision A

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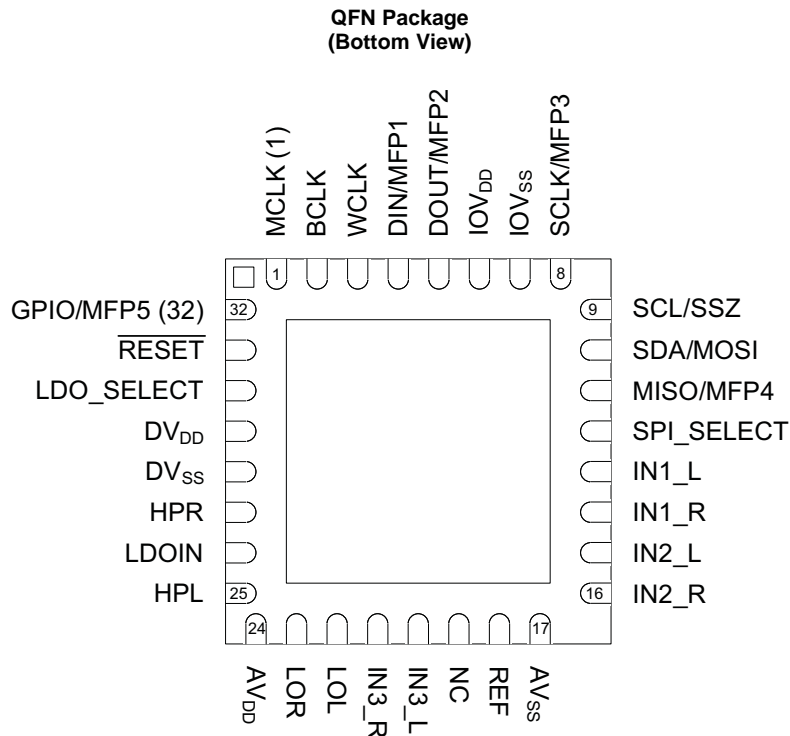
|   |   |          |
|---|---|----------|
| • | 已添加引脚配置和功能部分, 处理额定值表, 特性描述部分, 器件功能模式, 应用和实现部分, 电源相关建议部分, 布局部分, 器件和文档支持部分以及机械、封装和可订购信息部分 ..... | <b>1</b> |
|---|---|----------|

## 6 Device Comparison Table

| PART NUMBER             | DESCRIPTION                              |
|-------------------------|--|
| <a href="#">PCM3070</a> | Stereo audio codec with embedded miniDSP |

## 7 Pin Configuration and Functions

This document describes signals that take on different names depending on how they are configured. In such cases, the different names are placed together and separated by slash (/) characters. For example, "SCL/SS". Active low signals are represented by overbars.



### Pin Functions

| PIN | NAME              | TYPE <sup>(1)</sup> | DESCRIPTION  |
|-----|-------------------|---------------------|--|
| 1   | MCLK              | DI                  | Master Clock Input   |
| 2   | BCLK              | DIO                 | Audio serial data bus (primary) bit clock  |
| 3   | WCLK              | DIO                 | Audio serial data bus (primary) word clock   |
| 4   | DIN<br>MFP1       | DI                  | Primary function:<br>Audio serial data bus data input<br>Secondary function:<br>General Purpose Clock Input<br>General Purpose Input   |
| 5   | DOUT<br>MFP2      | DO                  | Primary function:<br>Audio serial data bus data output<br>Secondary function:<br>General Purpose Output<br>Clock Output<br>INT1 Output<br>INT2 Output<br>Audio serial data bus (secondary) bit clock output<br>Audio serial data bus (secondary) word clock output |
| 6   | IOV <sub>DD</sub> | Power               | IO voltage supply 1.1V – 3.6V  |
| 7   | IOV <sub>SS</sub> | Ground              | IO ground supply   |

(1) DI (Digital Input), DO (Digital Output), DIO (Digital Input/Output), AI (Analog Input), AO (Analog Output), AIO (Analog Input/Output)

**Pin Functions (continued)**

| PIN | NAME              | TYPE <sup>(1)</sup> | DESCRIPTION  |
|-----|-------------------|---------------------|--|
| 8   | SCLK<br>/<br>MFP3 | DI                  | Primary function: (SPI_Select = 1)<br>SPI serial clock<br>Secondary function: (SPI_Select = 0)<br>Audio serial data bus (secondary) bit clock input<br>Audio serial data bus (secondary) DAC or common word clock input<br>Audio serial data bus (secondary) ADC word clock input<br>Audio serial data bus (secondary) data input<br>General Purpose Input                                       |
| 9   | SCL/SS            | DI                  | I <sup>2</sup> C interface serial clock (SPI_Select = 0)<br>SPI interface mode chip-select signal (SPI_Select = 1)   |
| 10  | SDA/MOSI          | DI                  | I <sup>2</sup> C interface mode serial data input (SPI_Select = 0)<br>SPI interface mode serial data input (SPI_Select = 1)  |
| 11  | MISO<br>/<br>MFP4 | DO                  | Primary function: (SPI_Select = 1)<br>Serial data output<br>Secondary function: (SPI_Select = 0)<br>General purpose output<br>CLKOUT output<br>INT1 output<br>INT2 output<br>Audio serial data bus (primary) ADC word clock output<br>Audio serial data bus (secondary) data output<br>Audio serial data bus (secondary) bit clock output<br>Audio serial data bus (secondary) word clock output |
| 12  | SPI_SELECT        | DI                  | Control mode select pin ( 1 = SPI, 0 = I <sup>2</sup> C )  |
| 13  | IN1_L             | AI                  | Multifunction Analog Input,<br>or Single-ended configuration: Line 1 left<br>or Differential configuration: Line right, negative   |
| 14  | IN1_R             | AI                  | Multifunction Analog Input,<br>or Single-ended configuration: or Line 1 right<br>or Differential configuration: Line right, positive   |
| 15  | IN2_L             | AI                  | Multifunction Analog Input,<br>or Single-ended configuration: Line 2 left<br>or Differential configuration: Line left, positive  |
| 16  | IN2_R             | AI                  | Multifunction Analog Input,<br>or Single-ended configuration: Line 2 right<br>or Differential configuration: Line left, negative   |
| 17  | AV <sub>SS</sub>  | Ground              | Analog ground supply   |
| 18  | REF               | AO                  | Reference voltage output for filtering   |
| 19  | NC                | --                  | NC, do not connect   |
| 20  | IN3_L             | AI                  | Multifunction Analog Input,<br>or Single-ended configuration: Line 3 left,<br>or Differential configuration: Line left, positive,<br>or Differential configuration: Line right, negative   |
| 21  | IN3_R             | AI                  | Multifunction Analog Input,<br>or Single-ended configuration: Line 3 right,<br>or Differential configuration: Line left, negative,<br>or Differential configuration: Line right, positive  |
| 22  | LOL               | AO                  | Left line output   |
| 23  | LOR               | AO                  | Right line output  |
| 24  | AV <sub>DD</sub>  | Power               | Analog voltage supply 1.5V–1.95V<br>Input when A-LDO disabled,<br>Filtering output when A-LDO enabled  |
| 25  | HPL               | AO                  | Left high power output driver  |
| 26  | LDOIN/HPVDD       | Power               | LDO Input supply and Headphone Power supply 1.9V– 3.6V   |

**Pin Functions (continued)**

| PIN         | NAME                      | TYPE <sup>(1)</sup> | DESCRIPTION   |
|-------------|---------------------------|---------------------|---|
| 27          | HPR                       | AO                  | Right high power output driver  |
| 28          | DV <sub>SS</sub>          | Ground              | Digital Ground and Chip-substrate   |
| 29          | DV <sub>DD</sub>          | Power               | If LDO_SELECT Pin = 0 (D-LDO disabled)<br>Digital voltage supply 1.26V – 1.95V<br>If LDO_SELECT Pin = 1 (D-LDO enabled)<br>Digital voltage supply filtering output  |
| 30          | LDO_SELECT                | DI                  | D-LDO enable signal (1 = D-LDO enable, 0 = D-LDO disabled)  |
| 31          | $\overline{\text{RESET}}$ | DI                  | Reset (active low)  |
| 32          | GPIO<br><br>MFP5          | DI                  | Primary function:<br>General Purpose digital IO<br>Secondary function:<br>CLKOUT Output<br>INT1 Output<br>INT2 Output<br>Audio serial data bus ADC word clock output<br>Audio serial data bus (secondary) bit clock output<br>Audio serial data bus (secondary) word clock output |
| Thermal Pad | Thermal Pad               | N/A                 | Connect to PCB ground plane. Not internally connected.  |

## 8 Specifications

### 8.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) <sup>(1)</sup>

|   |  | MIN  | MAX                     | UNIT |
|---|--|------|-------------------------|------|
| Input voltage                             | AV <sub>DD</sub> to AV <sub>SS</sub>   | -0.3 | 2.2                     | V    |
|   | DV <sub>DD</sub> to DV <sub>SS</sub>   | -0.3 | 2.2                     | V    |
|   | IOV <sub>DD</sub> to IOV <sub>SS</sub> | -0.3 | 3.9                     | V    |
|   | LDOIN to AV <sub>SS</sub>              | -0.3 | 3.9                     | V    |
| Digital Input voltage                     |  |      | IOV <sub>DD</sub> + 0.3 | V    |
| Analog input voltage                      |  |      | AV <sub>DD</sub> + 0.3  | V    |
| Operating temperature range               |  | -40  | 85                      | °C   |
| Junction temperature (T <sub>J</sub> Max) |  |      | 105                     | °C   |

(1) Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

### 8.2 Handling Ratings

|                    |                           | MIN  | MAX | UNIT |
|--------------------|---------------------------|--|-----|------|
| T <sub>stg</sub>   | Storage temperature range | -55  | 125 | °C   |
| V <sub>(ESD)</sub> | Electrostatic discharge   | Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins <sup>(1)</sup>              |     | kV   |
|                    |                           | Charged device model (CDM), per JEDEC specification JESD22-C101, all pins <sup>(2)</sup> |     | V    |

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

### 8.3 Recommended Operating Conditions

|  |                                 | MIN   | NOM | MAX   | UNIT              |      |
|--|---------------------------------|---|-----|---|-------------------|------|
| LDOIN  | Power Supply Voltage Range      | Referenced to AV <sub>SS</sub> <sup>(1)</sup>                                 |     | 1.9   | 3.6               |      |
| AV <sub>DD</sub>   |                                 | 1.5   | 1.8 | 1.95  | V                 |      |
| IOV <sub>DD</sub>  |                                 | Referenced to IOV <sub>SS</sub> <sup>(1)</sup>                                |     | 1.5   |                   | 3.6  |
| DV <sub>DD</sub> <sup>(2)</sup>  |                                 | Referenced to DV <sub>SS</sub> <sup>(1)</sup>                                 |     | 1.8   |                   | 1.95 |
| PLL Input Frequency  |                                 | Clock divider uses fractional divide (D > 0), P = 1, DV <sub>DD</sub> ≥ 1.65V |     | 10  |                   | 20   |
|  |                                 | Clock divider uses integer divide (D = 0), P = 1, DV <sub>DD</sub> ≥ 1.65V    |     | 0.512   | 20                |      |
| MCLK   | Master Clock Frequency          | MCLK; Master Clock Frequency; DV <sub>DD</sub> ≥ 1.65V                        |     |   | 50                |      |
|  |                                 | MCLK; Master Clock Frequency; DV <sub>DD</sub> ≥ 1.26V                        |     |   | 25                |      |
| SCL  | SCL Clock Frequency             |   |     | 400   | kHz               |      |
| Audio input max ac signal swing (IN1_L, IN1_R, IN2_L, IN2_R, IN3_L, IN3_R) |                                 | CM = 0.75 V   |     | 0   | 0.530             |      |
|  |                                 | CM = 0.9 V  |     | 0   | 0.707             |      |
|  |                                 |   |     | 0.75 or AV <sub>DD</sub> -0.75 <sup>(3)</sup> | V <sub>peak</sub> |      |
|  |                                 |   |     | 0.9 or AV <sub>DD</sub> -0.9 <sup>(3)</sup>   | V <sub>peak</sub> |      |
| C <sub>Lout</sub>  | Digital output load capacitance |   |     | 10  | pF                |      |
| T <sub>OPR</sub>   | Operating Temperature Range     |   |     | -40   | 85                |      |
|  |                                 |   |     |   | °C                |      |

(1) All grounds on board are tied together to prevent voltage differences of more than 0.2V maximum for any combination of ground signals.

(2) At DV<sub>DD</sub> values lower than 1.65V, the PLL does not function. Refer to the *Maximum PCM3070 Clock Frequencies* table in the *PCM3070 Application Reference Guide (SLAU332)* for details on maximum clock frequencies.

(3) Whichever is smaller.

## 8.4 Thermal Information

| THERMAL METRIC <sup>(1)</sup> |  | PCM3070   | UNIT |
|-------------------------------|--|-----------|------|
|                               |  | RHB (QFN) |      |
|                               |  | 32 PINS   |      |
| R <sub>θJA</sub>              | Junction-to-ambient thermal resistance       | 31.4      | °C/W |
| R <sub>θJCTop</sub>           | Junction-to-case (top) thermal resistance    | 21.4      |      |
| R <sub>θJB</sub>              | Junction-to-board thermal resistance         | 5.4       |      |
| ψ <sub>JT</sub>               | Junction-to-top characterization parameter   | 0.2       |      |
| ψ <sub>JB</sub>               | Junction-to-board characterization parameter | 5.4       |      |
| R <sub>θJCbott</sub>          | Junction-to-case (bottom) thermal resistance | 0.9       |      |

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report (SPRA953).

## 8.5 Electrical Characteristics, ADC

| PARAMETER                |   | TEST CONDITIONS  | MIN   | TYP | MAX | UNIT             |
|--------------------------|---|--|-------|-----|-----|------------------|
| <b>AUDIO ADC</b>         |   |  |       |     |     |                  |
| Input signal level (0dB) |   | Single-ended, CM = 0.9V  | 0.5   |     |     | V <sub>RMS</sub> |
| Device Setup             |   | 1kHz sine wave input, Single-ended Configuration<br>IN1_R to Right ADC and IN1_L to Left ADC,<br>R <sub>in</sub> = 20k, f <sub>s</sub> = 48kHz,<br>AOSR = 128, MCLK = 256 x f <sub>s</sub> ,<br>PLL Disabled; AGC = OFF, Channel Gain = 0dB,<br>Processing Block = PRB_R1,   |       |     |     |                  |
| SNR                      | Signal-to-noise ratio, A-weighted <sup>(1)(2)</sup> | Inputs ac-shortened to ground  | 80    | 93  |     | dB               |
|                          |   | IN2_R, IN3_R routed to Right ADC and ac-shortened to ground<br>IN2_L, IN3_L routed to Left ADC and ac-shortened to ground  | 93    |     |     |                  |
| DR                       | Dynamic range A-weighted <sup>(1)(2)</sup>          | –60dB full-scale, 1-kHz input signal   | 92    |     |     | dB               |
| THD+N                    | Total Harmonic Distortion plus Noise                | –3 dB full-scale, 1-kHz input signal   | –85   |     | –70 | dB               |
|                          |   | IN2_R, IN3_R routed to Right ADC<br>IN2_L, IN3_L routed to Left ADC<br>–3dB full-scale, 1-kHz input signal   | –85   |     |     |                  |
| <b>AUDIO ADC</b>         |   |  |       |     |     |                  |
| Input signal level (0dB) |   | Single-ended, CM = 0.75V, AV <sub>DD</sub> = 1.5V  | 0.375 |     |     | V <sub>RMS</sub> |
| Device Setup             |   | 1kHz sine wave input, Single-ended Configuration<br>IN1_R, IN2_R, IN3_R routed to Right ADC<br>IN1_L, IN2_L, IN3_L routed to Left ADC<br>R <sub>in</sub> = 20kΩ, f <sub>s</sub> = 48kHz,<br>AOSR = 128, MCLK = 256 x f <sub>s</sub> ,<br>PLL Disabled, AGC = OFF, Channel Gain = 0dB,<br>Processing Block = PRB_R1 |       |     |     |                  |
| SNR                      | Signal-to-noise ratio, A-weighted <sup>(1)(2)</sup> | Inputs ac-shortened to ground  | 91    |     |     | dB               |
| DR                       | Dynamic range A-weighted <sup>(1)(2)</sup>          | –60dB full-scale, 1-kHz input signal   | 90    |     |     | dB               |
| THD+N                    | Total Harmonic Distortion plus Noise                | –3dB full-scale, 1-kHz input signal  | –80   |     |     | dB               |

- (1) Ratio of output level with 1kHz full-scale sine wave input, to the output level with the inputs short circuited, measured A-weighted over a 20Hz to 20kHz bandwidth using an audio analyzer.
- (2) All performance measured with 20kHz low-pass filter and, where noted, A-weighted filter. Failure to use such a filter may result in higher THD+N and lower SNR and dynamic range readings than shown in the Electrical Characteristics. The low-pass filter removes out-of-band noise, which, although not audible, may affect dynamic specification values.



**Electrical Characteristics, ADC (continued)**

| PARAMETER        |  | TEST CONDITIONS   | MIN | TYP   | MAX | UNIT              |
|------------------|--|---|-----|-------|-----|-------------------|
| <b>AUDIO ADC</b> |  |   |     |       |     |                   |
|                  | Input signal level (0dB)                         | Differential Input, CM = 0.9V   |     | 10    |     | mV                |
|                  | Device Setup                                     | 1kHz sine wave input, Differential configuration<br>IN1_L and IN1_R routed to Right ADC<br>IN2_L and IN2_R routed to Left ADC<br>R <sub>in</sub> = 10K, f <sub>s</sub> = 48kHz, AOSR = 128<br>MCLK = 256* f <sub>s</sub> PLL Disabled<br>AGC = OFF, Channel Gain = 40dB Processing Block = PRB_R1,  |     |       |     |                   |
| ICN              | Idle-Channel Noise, A-weighted <sup>(1)(2)</sup> | Inputs ac-short to ground, input referred noise   |     | 2     |     | μV <sub>RMS</sub> |
| <b>AUDIO ADC</b> |  |   |     |       |     |                   |
|                  | Gain Error                                       | 1kHz sine wave input , Single-ended configuration<br>R <sub>in</sub> = 20kΩ f <sub>s</sub> = 48kHz, AOSR = 128,<br>MCLK = 256 x f <sub>s</sub> , PLL Disabled<br>AGC = OFF, Channel Gain = 0dB<br>Processing Block = PRB_R1,  |     | -0.05 |     | dB                |
|                  | Input Channel Separation                         | 1kHz sine wave input at -3dBFS<br>Single-ended configuration<br>IN1_L routed to Left ADC<br>IN1_R routed to Right ADC, R <sub>in</sub> = 20kΩ<br>AGC = OFF, AOSR = 128,<br>Channel Gain = 0dB, CM = 0.9V  |     | 108   |     | dB                |
|                  | Input Pin Crosstalk                              | 1kHz sine wave input at -3dBFS on IN2_L, IN2_L internally not routed.<br>IN1_L routed to Left ADC<br>ac-coupled to ground<br>1kHz sine wave input at -3dBFS on IN2_R,<br>IN2_R internally not routed.<br>IN1_R routed to Right ADC<br>ac-coupled to ground<br>Single-ended configuration R <sub>in</sub> = 20kΩ,<br>AOSR = 128 Channel, Gain = 0dB, CM = 0.9V |     | 115   |     | dB                |
|                  | PSRR   | 217Hz, 100mVpp signal on AV <sub>DD</sub> ,<br>Single-ended configuration, R <sub>in</sub> = 20kΩ,<br>Channel Gain = 0dB; CM = 0.9V   |     | 55    |     | dB                |
|                  | ADC programmable gain amplifier gain             | Single-Ended, R <sub>in</sub> = 10kΩ, PGA gain set to 0dB   |     | 0     |     | dB                |
|                  |  | Single-Ended, R <sub>in</sub> = 10kΩ, PGA gain set to 47.5dB  |     | 47.5  |     | dB                |
|                  |  | Single-Ended, R <sub>in</sub> = 20kΩ, PGA gain set to 0dB   |     | -6    |     | dB                |
|                  |  | Single-Ended, R <sub>in</sub> = 20kΩ, PGA gain set to 47.5dB  |     | 41.5  |     | dB                |
|                  |  | Single-Ended, R <sub>in</sub> = 40kΩ, PGA gain set to 0dB   |     | -12   |     | dB                |
|                  |  | Single-Ended, R <sub>in</sub> = 40kΩ, PGA gain set to 47.5dB  |     | 35.5  |     | dB                |
|                  | ADC programmable gain amplifier step size        | 1-kHz tone  |     | 0.5   |     | dB                |

## 8.6 Electrical Characteristics, Bypass Outputs

| PARAMETER  |                           | TEST CONDITIONS  | MIN | TYP  | MAX | UNIT              |
|--|---------------------------|--|-----|------|-----|-------------------|
| <b>ANALOG BYPASS TO HEADPHONE AMPLIFIER, DIRECT MODE</b> |                           |  |     |      |     |                   |
| Device Setup   |                           | Load = 16Ω (single-ended), 50pF;<br>Input and Output CM = 0.9V;<br>Headphone Output on LDOIN Supply;<br>IN1_L routed to HPL and IN1_R routed to HPR;<br>Channel Gain = 0dB   |     |      |     |                   |
| Gain Error   |                           |  |     | -0.8 |     | dB                |
| Noise, A-weighted <sup>(1)</sup>                         |                           | Idle Channel, IN1_L and IN1_R ac-shortcd to ground   |     | 3    |     | μV <sub>RMS</sub> |
| THD  | Total Harmonic Distortion | 446mV <sub>rms</sub> , 1kHz input signal   |     | -89  |     | dB                |
| <b>ANALOG BYPASS TO LINE-OUT AMPLIFIER, PGA MODE</b>     |                           |  |     |      |     |                   |
| Device Setup   |                           | Load = 10kΩ (single-ended), 56pF;<br>Input and Output CM = 0.9V;<br>LINE Output on LDOIN Supply;<br>IN1_L routed to ADCPGA_L and IN1_R routed to ADCPGA_R; R <sub>in</sub> = 20kΩ<br>ADCPGA_L routed to LOL and ADCPGA_R routed to LOR; Channel Gain = 0dB |     |      |     |                   |
| Gain Error   |                           |  |     | 0.6  |     | dB                |
| Noise, A-weighted <sup>(1)</sup>                         |                           | Idle Channel, IN1_L and IN1_R ac-shortcd to ground   |     | 7    |     | μV <sub>RMS</sub> |
|  |                           | Channel Gain = 40dB,<br>Input Signal (0dB) = 5mV <sub>rms</sub><br>Inputs ac-shortcd to ground, Input Referred   |     | 3.4  |     | μV <sub>RMS</sub> |

(1) All performance measured with 20kHz low-pass filter and, where noted, A-weighted filter. Testing without such a filter may result in higher THD+N and lower SNR and dynamic range readings than shown in the Electrical Characteristics. The low-pass filter removes out-of-band noise, which, although not audible, may affect dynamic specification values.

## 8.7 Electrical Characteristics, Audio DAC Outputs

| PARAMETER   |   | TEST CONDITIONS  | MIN | TYP   | MAX | UNIT             |
|---|---|--|-----|-------|-----|------------------|
| <b>AUDIO DAC – STEREO SINGLE-ENDED LINE OUTPUT</b>      |   |  |     |       |     |                  |
| Device Setup  |   | Load = 10k $\Omega$ (single-ended), 56pF<br>Line Output on AV <sub>DD</sub> Supply<br>Input and Output CM = 0.9V<br>DOSR = 128, MCLK = 256 x f <sub>s</sub> ,<br>Channel Gain = 0dB, word length = 16 bits,<br>Processing Block = PRB_P1,                |     |       |     |                  |
|   | Full scale output voltage (0dB)                     |  |     | 0.5   |     | V <sub>RMS</sub> |
| SNR   | Signal-to-noise ratio A-weighted <sup>(1)(2)</sup>  | All zeros fed to DAC input   | 87  | 100   |     | dB               |
| DR  | Dynamic range, A-weighted <sup>(1)(2)</sup>         | –60dB 1kHz input full-scale signal, Word length = 20 bits  |     | 100   |     | dB               |
| THD+N   | Total Harmonic Distortion plus Noise                | –3dB full-scale, 1kHz input signal   |     | –83   | –70 | dB               |
|   | DAC Gain Error                                      | 0 dB, 1kHz input full scale signal   |     | 0.3   |     | dB               |
|   | DAC Mute Attenuation                                | Mute   |     | 119   |     | dB               |
|   | DAC channel separation                              | –1 dB, 1kHz signal, between left and right HP out  |     | 113   |     | dB               |
| DAC PSRR  |   | 100mVpp, 1kHz signal applied to AV <sub>DD</sub>   |     | 73    |     | dB               |
|   |   | 100mVpp, 217Hz signal applied to AV <sub>DD</sub>  |     | 77    |     | dB               |
| <b>AUDIO DAC – STEREO SINGLE-ENDED LINE OUTPUT</b>      |   |  |     |       |     |                  |
| Device Setup  |   | Load = 10k $\Omega$ (single-ended), 56pF<br>Line Output on AV <sub>DD</sub> Supply<br>Input and Output CM = 0.75V; AV <sub>DD</sub> = 1.5V<br>DOSR = 128<br>MCLK = 256 * fs<br>Channel Gain = –2dB<br>word length = 20 bits<br>Processing Block = PRB_P1 |     |       |     |                  |
|   | Full scale output voltage (0dB)                     |  |     | 0.375 |     | V <sub>RMS</sub> |
| SNR   | Signal-to-noise ratio, A-weighted <sup>(1)(2)</sup> | All zeros fed to DAC input   |     | 99    |     | dB               |
| DR  | Dynamic range, A-weighted <sup>(1)(2)</sup>         | –60dB 1 kHz input full-scale signal  |     | 97    |     | dB               |
| THD+N   | Total Harmonic Distortion plus Noise                | –1 dB full-scale, 1-kHz input signal   |     | –85   |     | dB               |
| <b>AUDIO DAC – STEREO SINGLE-ENDED HEADPHONE OUTPUT</b> |   |  |     |       |     |                  |
| Device Setup  |   | Load = 16 $\Omega$ (single-ended), 50pF<br>Headphone Output on AV <sub>DD</sub> Supply,<br>Input and Output CM = 0.9V, DOSR = 128,<br>MCLK = 256 * f <sub>s</sub> , Channel Gain = 0dB<br>word length = 16 bits;<br>Processing Block = PRB_P1            |     |       |     |                  |
|   | Full scale output voltage (0dB)                     |  |     | 0.5   |     | V <sub>RMS</sub> |
| SNR   | Signal-to-noise ratio, A-weighted <sup>(1)(2)</sup> | All zeros fed to DAC input   | 87  | 100   |     | dB               |
| DR  | Dynamic range, A-weighted <sup>(1)(2)</sup>         | –60dB 1kHz input full-scale signal, Word Length = 20 bits  |     | 99    |     | dB               |
| THD+N   | Total Harmonic Distortion plus Noise                | –3dB full-scale, 1kHz input signal   |     | –83   | –70 | dB               |
|   | DAC Gain Error                                      | 0dB, 1kHz input full scale signal  |     | –0.3  |     | dB               |
|   | DAC Mute Attenuation                                | Mute   |     | 122   |     | dB               |
|   | DAC channel separation                              | –1dB, 1kHz signal, between left and right HP out   |     | 110   |     | dB               |
| DAC PSRR  |   | 100mVpp, 1kHz signal applied to AV <sub>DD</sub>   |     | 73    |     | dB               |
|   |   | 100mVpp, 217Hz signal applied to AV <sub>DD</sub>  |     | 78    |     | dB               |

- (1) Ratio of output level with 1kHz full-scale sine wave input, to the output level with the inputs short circuited, measured A-weighted over a 20Hz to 20kHz bandwidth using an audio analyzer.
- (2) All performance measured with 20kHz low-pass filter and, where noted, A-weighted filter. Testing without such a filter may result in higher THD+N and lower SNR and dynamic range readings than shown in the Electrical Characteristics. The low-pass filter removes out-of-band noise, which, although not audible, may affect dynamic specification values

**Electrical Characteristics, Audio DAC Outputs (continued)**

| PARAMETER   |   | TEST CONDITIONS  | MIN | TYP   | MAX | UNIT       |
|---|---|--|-----|-------|-----|------------|
| Power Delivered   |   | $R_L = 16\Omega$ , Output Stage on $AV_{DD} = 1.8V$<br>THDN < 1%, Input CM = 0.9V,<br>Output CM = 0.9V   |     | 15    |     | mW         |
|   |   | $R_L = 16\Omega$ Output Stage on LDOIN = 3.3V,<br>THDN < 1% Input CM = 0.9V,<br>Output CM = 1.65V  |     | 64    |     |            |
| <b>AUDIO DAC – STEREO SINGLE-ENDED HEADPHONE OUTPUT</b> |   |  |     |       |     |            |
| Device Setup  |   | Load = $16\Omega$ (single-ended), 50pF,<br>Headphone Output on $AV_{DD}$ Supply,<br>Input and Output CM = 0.75V; $AV_{DD} = 1.5V$ ,<br>DOSR = 128, MCLK = $256 * f_s$ ,<br>Channel Gain = -2dB, word length = 20-bits;<br>Processing Block = PRB_P1,   |     |       |     |            |
|   | Full scale output voltage (0dB)                     |  |     | 0.375 |     | $V_{RMS}$  |
| SNR   | Signal-to-noise ratio, A-weighted <sup>(1)(2)</sup> | All zeros fed to DAC input   |     | 99    |     | dB         |
| DR  | Dynamic range, A-weighted <sup>(1)(2)</sup>         | -60dB 1kHz input full-scale signal   |     | 98    |     | dB         |
| THD+N   | Total Harmonic Distortion plus Noise                | -1dB full-scale, 1kHz input signal   |     | -83   |     | dB         |
| <b>AUDIO DAC – MONO DIFFERENTIAL HEADPHONE OUTPUT</b>   |   |  |     |       |     |            |
| Device Setup  |   | Load = $32\Omega$ (differential), 50pF,<br>Headphone Output on LDOIN Supply<br>Input CM = 0.75V, Output CM = 1.5V,<br>$AV_{DD} = 1.8V$ , LDOIN = 3.0V, DOSR = 128<br>MCLK = $256 * f_s$ , Channel (headphone driver)<br>Gain = 5dB for full scale output signal,<br>word length = 16 bits,<br>Processing Block = PRB_P1, |     |       |     |            |
|   | Full scale output voltage (0dB)                     |  |     | 1778  |     | $mV_{RMS}$ |
| SNR   | Signal-to-noise ratio, A-weighted <sup>(1)(2)</sup> | All zeros fed to DAC input   |     | 98    |     | dB         |
| DR  | Dynamic range, A-weighted <sup>(1)(2)</sup>         | -60dB 1kHz input full-scale signal   |     | 96    |     | dB         |
| THD   | Total Harmonic Distortion                           | -3dB full-scale, 1kHz input signal   |     | -82   |     | dB         |
| Power Delivered   |   | $R_L = 32\Omega$ , Output Stage on LDOIN = 3.3V,<br>THDN < 1%, Input CM = 0.9V,<br>Output CM = 1.65V   |     | 136   |     | mW         |
|   |   | $R_L = 32\Omega$ Output Stage on LDOIN = 3.0V,<br>THDN < 1% Input CM = 0.9V,<br>Output CM = 1.5V   |     | 114   |     | mW         |

## 8.8 Electrical Characteristics, LDO

over operating free-air temperature range (unless otherwise noted)

| PARAMETER                                      | TEST CONDITIONS                                    | MIN | TYP  | MAX | UNIT |
|--|--|-----|------|-----|------|
| <b>LOW DROPOUT REGULATOR (AV<sub>DD</sub>)</b> |  |     |      |     |      |
| Output Voltage                                 | LDO <sub>Mode</sub> = 1, LDO <sub>IN</sub> > 1.95V |     | 1.67 |     | V    |
|  | LDO <sub>Mode</sub> = 0, LDO <sub>IN</sub> > 2.0V  |     | 1.72 |     |      |
|  | LDO <sub>Mode</sub> = 2, LDO <sub>IN</sub> > 2.05V |     | 1.77 |     |      |
| Output Voltage Accuracy                        |  |     | ±2%  |     |      |
| Load Regulation                                | Load current range 0 to 50mA                       |     | 15   |     | mV   |
| Line Regulation                                | Input Supply Range 1.9V to 3.6V                    |     | 5    |     | mV   |
| Decoupling Capacitor                           |  | 1   |      |     | μF   |
| Bias Current                                   |  |     | 60   |     | μA   |

## 8.9 Electrical Characteristics, Misc.

| PARAMETER                             | TEST CONDITIONS   | MIN | TYP  | MAX | UNIT              |
|---------------------------------------|---|-----|------|-----|-------------------|
| <b>REFERENCE</b>                      |   |     |      |     |                   |
| Reference Voltage Settings            | CMM <sub>Mode</sub> = 0 (0.9V)  |     | 0.9  |     | V                 |
|                                       | CMM <sub>Mode</sub> = 1 (0.75V)   |     | 0.75 |     |                   |
| Reference Noise                       | CM = 0.9V, A-weighted, 20Hz to 20kHz bandwidth, C <sub>ref</sub> = 10μF   |     | 1    |     | μV <sub>RMS</sub> |
| Decoupling Capacitor                  |   | 1   | 10   |     | μF                |
| <b>miniDSP<sup>(1)</sup></b>          |   |     |      |     |                   |
| Maximum miniDSP clock frequency - ADC | DV <sub>DD</sub> = 1.65V  |     | 55.3 |     | MHz               |
| Maximum miniDSP clock frequency - DAC | DV <sub>DD</sub> = 1.65V  |     | 55.3 |     | MHz               |
| <b>Shutdown Current</b>               |   |     |      |     |                   |
| Device Setup                          | Coarse AV <sub>DD</sub> supply turned off, LDO <sub>select</sub> held at ground, No external digital input is toggled |     |      |     |                   |
| I(DV <sub>DD</sub> )                  |   |     | 0.9  |     | μA                |
| I(IOV <sub>DD</sub> )                 |   |     | 13   |     | nA                |

(1) miniDSP clock speed is specified by design and not tested in production.

## 8.10 Electrical Characteristics, Logic Levels<sup>(1)</sup>

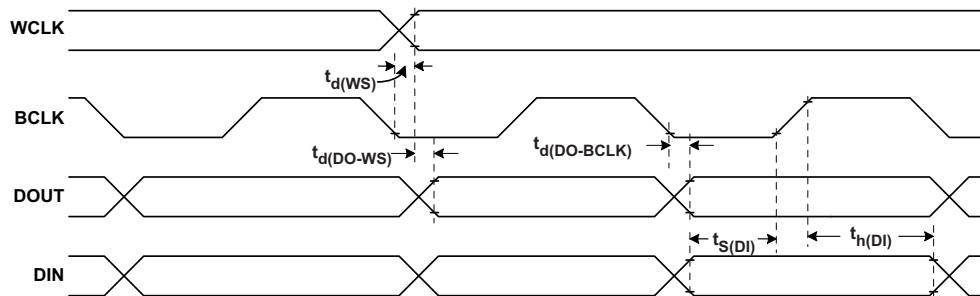
At 25°C, AV<sub>DD</sub>, DV<sub>DD</sub>, IOV<sub>DD</sub> = 1.8V

| PARAMETER                   | TEST CONDITIONS  | MIN                     | TYP                     | MAX | UNIT |
|-----------------------------|--|-------------------------|-------------------------|-----|------|
| <b>LOGIC FAMILY</b>         |  |                         |                         |     |      |
| <b>CMOS</b>                 |  |                         |                         |     |      |
| V <sub>IH</sub> Logic Level | I <sub>IH</sub> = 5 μA, IOV <sub>DD</sub> > 1.6V       | 0.7 × IOV <sub>DD</sub> |                         |     | V    |
|                             | I <sub>IH</sub> = 5μA, 1.2V ≤ IOV <sub>DD</sub> < 1.6V | 0.9 × IOV <sub>DD</sub> |                         |     | V    |
|                             | I <sub>IH</sub> = 5μA, IOV <sub>DD</sub> < 1.2V        | IOV <sub>DD</sub>       |                         |     | V    |
| V <sub>IL</sub>             | I <sub>IL</sub> = 5 μA, IOV <sub>DD</sub> > 1.6V       | −0.3                    | 0.3 × IOV <sub>DD</sub> |     | V    |
|                             | I <sub>IL</sub> = 5μA, 1.2V ≤ IOV <sub>DD</sub> < 1.6V |                         | 0.1 × IOV <sub>DD</sub> |     | V    |
|                             | I <sub>IL</sub> = 5μA, IOV <sub>DD</sub> < 1.2V        |                         | 0                       |     | V    |
| V <sub>OH</sub>             | I <sub>OH</sub> = 2 TTL loads                          | 0.8 × IOV <sub>DD</sub> |                         |     | V    |
| V <sub>OL</sub>             | I <sub>OL</sub> = 2 TTL loads                          |                         | 0.1 × IOV <sub>DD</sub> |     | V    |
| Capacitive Load             |  |                         | 10                      |     | pF   |

(1) Applies to all DI, DO, and DIO pins shown in [Pin Configuration and Functions](#).

**8.11 I<sup>2</sup>S LJF and RJF Timing in Master Mode (see Figure 1)**

|                  |  | IOVDD = 1.8V |     | IOVDD = 3.3V |     | UNIT |
|------------------|--|--------------|-----|--------------|-----|------|
|                  |  | MIN          | MAX | MIN          | MAX |      |
| $t_{d(WS)}$      | WCLK delay                             |              | 30  |              | 20  | ns   |
| $t_{d(DO-WS)}$   | WCLK to DOUT delay (For LJF Mode only) |              | 20  |              | 20  | ns   |
| $t_{d(DO-BCLK)}$ | BCLK to DOUT delay                     |              | 22  |              | 20  | ns   |
| $t_{s(DI)}$      | DIN setup                              | 8            |     | 8            |     | ns   |
| $t_{h(DI)}$      | DIN hold                               | 8            |     | 8            |     | ns   |
| $t_r$            | Rise time                              |              | 24  |              | 12  | ns   |
| $t_f$            | Fall time                              |              | 24  |              | 12  | ns   |



All specifications at 25°C, DVdd = 1.8V

**Figure 1. I<sup>2</sup>S LJF and RJF Timing in Master Mode**

8.12 I<sup>2</sup>S LJF and RJF Timing in Slave Mode (see Figure 2)

|                         |  | IOVDD = 1.8V |     | IOVDD = 3.3V |     | UNIT |
|-------------------------|--|--------------|-----|--------------|-----|------|
|                         |  | MIN          | MAX | MIN          | MAX |      |
| t <sub>H(BCLK)</sub>    | BCLK high period                       | 35           |     | 35           |     | ns   |
| t <sub>L(BCLK)</sub>    | BCLK low period                        | 35           |     | 35           |     | ns   |
| t <sub>s(WS)</sub>      | WCLK setup                             | 8            |     | 8            |     | ns   |
| t <sub>h(WS)</sub>      | WCLK hold                              | 8            |     | 8            |     | ns   |
| t <sub>d(DO-WS)</sub>   | WCLK to DOUT delay (For LJF mode only) |              | 20  |              | 20  | ns   |
| t <sub>d(DO-BCLK)</sub> | BCLK to DOUT delay                     |              | 22  |              | 22  | ns   |
| t <sub>s(DI)</sub>      | DIN setup                              | 8            |     | 8            |     | ns   |
| t <sub>h(DI)</sub>      | DIN hold                               | 8            |     | 8            |     | ns   |
| t <sub>r</sub>          | Rise time                              |              | 4   |              | 4   | ns   |
| t <sub>f</sub>          | Fall time                              |              | 4   |              | 4   | ns   |

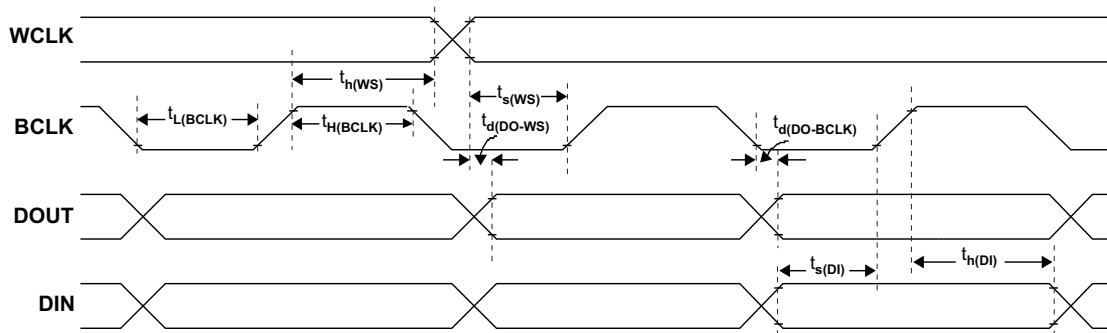
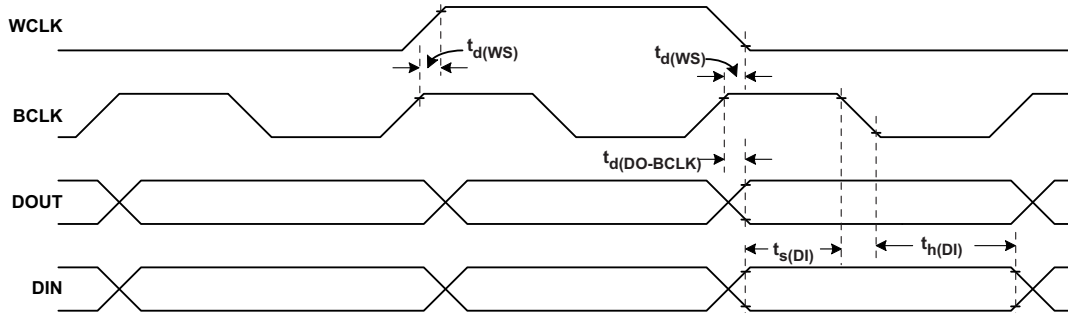


Figure 2. I<sup>2</sup>S LJF and RJF Timing in Slave Mode

**8.13 DSP Timing in Master Mode (see Figure 3)**

|                  |                    | IOVDD = 1.8V |     | IOVDD = 3.3V |     | UNIT |
|------------------|--------------------|--------------|-----|--------------|-----|------|
|                  |                    | MIN          | MAX | MIN          | MAX |      |
| $t_{d(WCLK)}$    | WCLK delay         |              | 30  |              | 20  | ns   |
| $t_{d(DO-BCLK)}$ | BCLK to DOUT delay |              | 22  |              | 20  | ns   |
| $t_{s(DI)}$      | DIN setup          | 8            |     | 8            |     | ns   |
| $t_{h(DI)}$      | DIN hold           | 8            |     | 8            |     | ns   |
| $t_r$            | Rise time          |              | 24  |              | 12  | ns   |
| $t_f$            | Fall time          |              | 24  |              | 12  | ns   |



All specifications at 25°C, DVdd = 1.8V

**Figure 3. DSP Timing in Master Mode**



8.14 DSP Timing in Slave Mode (see Figure 4)

|                  |                    | IOVDD = 1.8V |     | IOVDD = 3.3V |     | UNIT |
|------------------|--------------------|--------------|-----|--------------|-----|------|
|                  |                    | MIN          | MAX | MIN          | MAX |      |
| $t_{H(BCLK)}$    | BCLK high period   | 35           |     | 35           |     | ns   |
| $t_{L(BCLK)}$    | BCLK low period    | 35           |     | 35           |     | ns   |
| $t_{s(WS)}$      | WCLK setup         | 8            |     | 8            |     | ns   |
| $t_{h(WS)}$      | WCLK hold          | 8            |     | 8            |     | ns   |
| $t_{d(DO-BCLK)}$ | BCLK to DOUT delay |              | 22  |              | 22  | ns   |
| $t_{s(DI)}$      | DIN setup          | 8            |     | 8            |     | ns   |
| $t_{h(DI)}$      | DIN hold           | 8            |     | 8            |     | ns   |
| $t_r$            | Rise time          |              | 4   |              | 4   | ns   |
| $t_f$            | Fall time          |              | 4   |              | 4   | ns   |

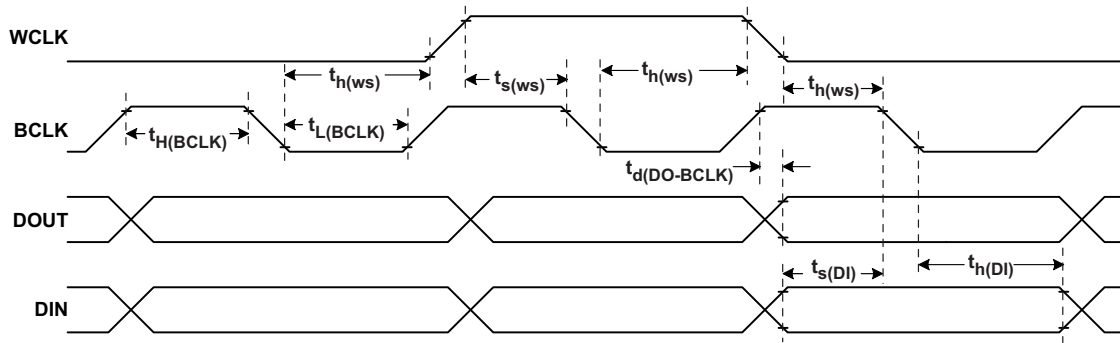


Figure 4. DSP Timing in Slave Mode

## 8.15 I<sup>2</sup>C Interface Timing

|              |  | Standard-Mode |     |      | Fast-Mode   |     |     | UNIT    |
|--------------|--|---------------|-----|------|-------------|-----|-----|---------|
|              |  | MIN           | TYP | MAX  | MIN         | TYP | MAX |         |
| $f_{SCL}$    | SCL clock frequency  | 0             |     | 100  | 0           |     | 400 | kHz     |
| $t_{HD;STA}$ | Hold time (repeated) START condition. After this period, the first clock pulse is generated. | 4.0           |     |      | 0.8         |     |     | $\mu$ s |
| $t_{LOW}$    | LOW period of the SCL clock  | 4.7           |     |      | 1.3         |     |     | $\mu$ s |
| $t_{HIGH}$   | HIGH period of the SCL clock   | 4.0           |     |      | 0.6         |     |     | $\mu$ s |
| $t_{SU;STA}$ | Setup time for a repeated START condition  | 4.7           |     |      | 0.8         |     |     | $\mu$ s |
| $t_{HD;DAT}$ | Data hold time: For I2C bus devices  | 0             |     | 3.45 | 0           |     | 0.9 | $\mu$ s |
| $t_{SU;DAT}$ | Data set-up time   | 250           |     |      | 100         |     |     | ns      |
| $t_r$        | SDA and SCL Rise Time  |               |     | 1000 | $20+0.1C_b$ |     | 300 | ns      |
| $t_f$        | SDA and SCL Fall Time  |               |     | 300  | $20+0.1C_b$ |     | 300 | ns      |
| $t_{SU;STO}$ | Set-up time for STOP condition   | 4.0           |     |      | 0.8         |     |     | $\mu$ s |
| $t_{BUF}$    | Bus free time between a STOP and START condition   | 4.7           |     |      | 1.3         |     |     | $\mu$ s |
| $C_b$        | Capacitive load for each bus line  |               |     | 400  |             |     | 400 | pF      |

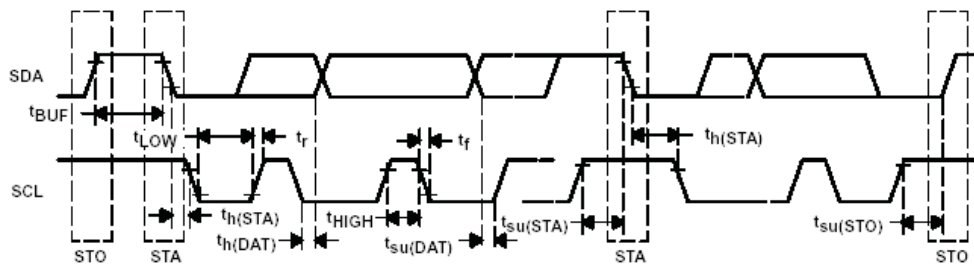


Figure 5. I<sup>2</sup>C Interface Timing

8.16 SPI Interface Timing (See Figure 6)

|                |                            | IOVDD = 1.8V |     |     | IOVDD = 3.3V |     |     | UNIT |
|----------------|----------------------------|--------------|-----|-----|--------------|-----|-----|------|
|                |                            | MIN          | TYP | MAX | MIN          | TYP | MAX |      |
| $t_{sck}$      | SCLK Period <sup>(1)</sup> | 100          |     |     | 50           |     |     | ns   |
| $t_{sckh}$     | SCLK Pulse width High      | 50           |     |     | 25           |     |     | ns   |
| $t_{sckl}$     | SCLK Pulse width Low       | 50           |     |     | 25           |     |     | ns   |
| $t_{lead}$     | Enable Lead Time           | 30           |     |     | 20           |     |     | ns   |
| $t_{trail}$    | Enable Trail Time          | 30           |     |     | 20           |     |     | ns   |
| $t_{d;seqxfr}$ | Sequential Transfer Delay  | 40           |     |     | 20           |     |     | ns   |
| $t_a$          | Slave DOUT access time     |              |     | 40  |              |     | 20  | ns   |
| $t_{dis}$      | Slave DOUT disable time    |              |     | 40  |              |     | 20  | ns   |
| $t_{su}$       | DIN data setup time        | 15           |     |     | 10           |     |     | ns   |
| $t_{h(DIN)}$   | DIN data hold time         | 15           |     |     | 10           |     |     | ns   |
| $t_{v(DOUT)}$  | DOUT data valid time       |              |     | 25  |              |     | 18  | ns   |
| $t_r$          | SCLK Rise Time             |              |     | 4   |              |     | 4   | ns   |
| $t_f$          | SCLK Fall Time             |              |     | 4   |              |     | 4   | ns   |

(1) These parameters are based on characterization and are not tested in production.

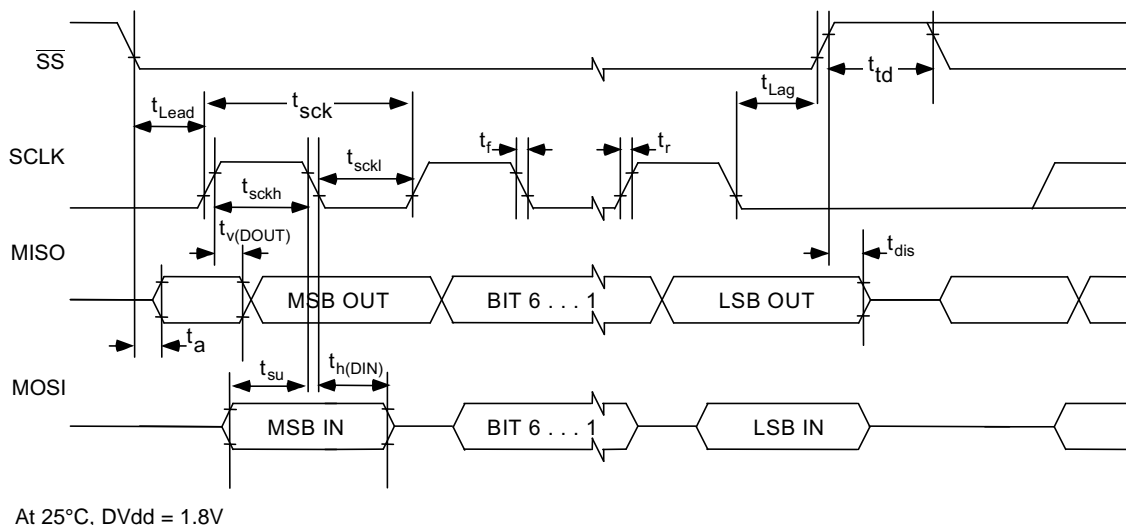


Figure 6. SPI Interface Timing Diagram

## 8.17 Typical Characteristics

### 8.17.1 Typical Performance

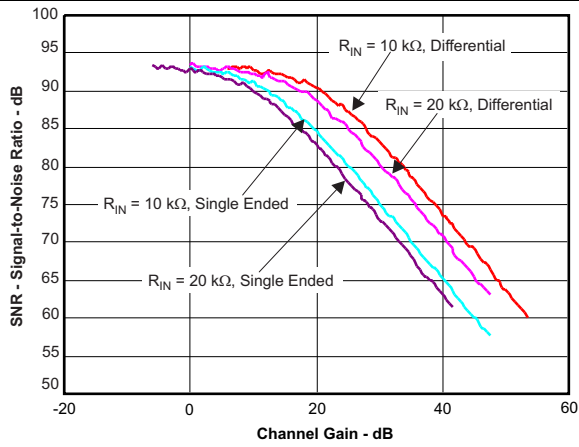


Figure 7. ADC SNR vs Channel Gain

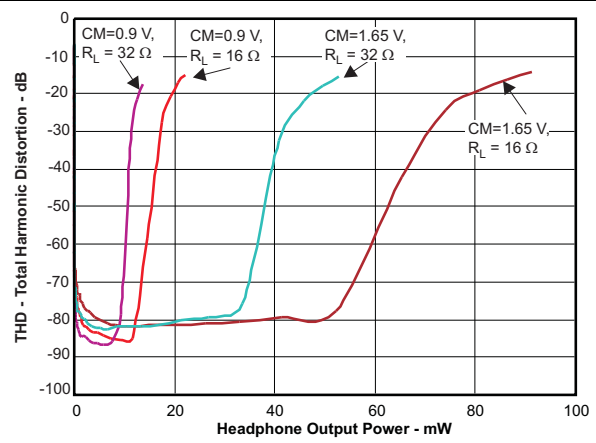


Figure 8. Total Harmonic Distortion vs Headphone Output Power

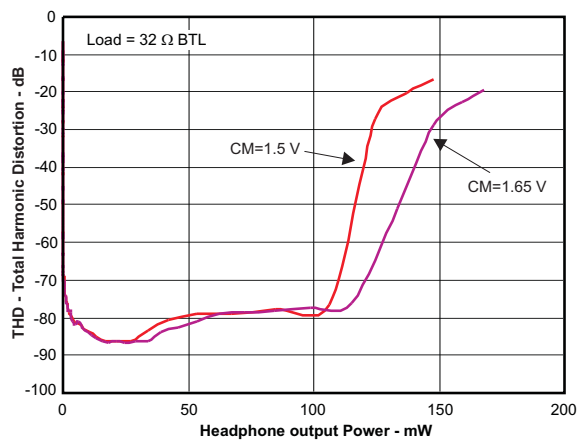


Figure 9. Total Harmonic Distortion vs Headphone Output Power

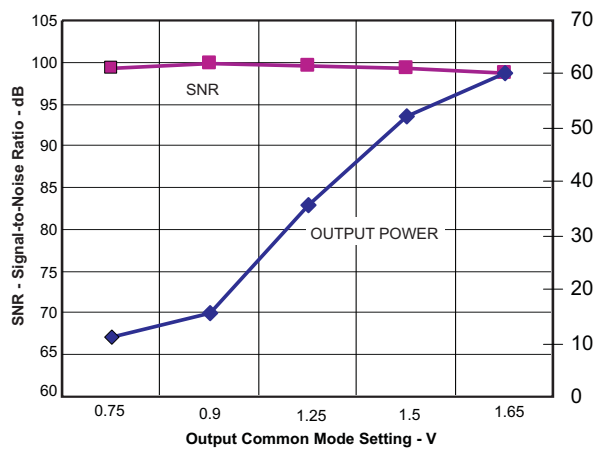


Figure 10. Headphone SNR and Output Power vs Output Common Mode Setting

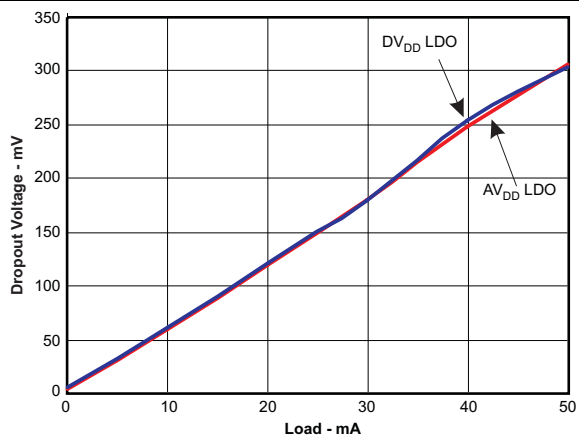


Figure 11. LDO Dropout Voltage vs Load Current

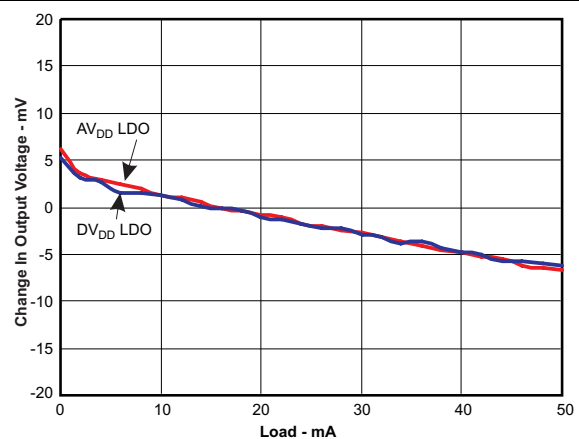
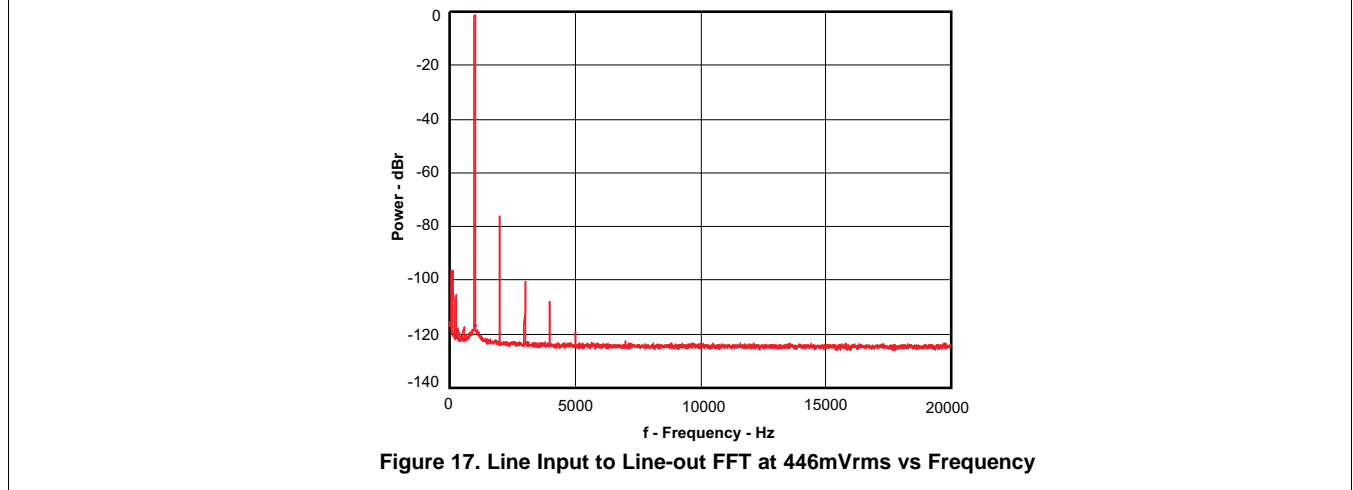
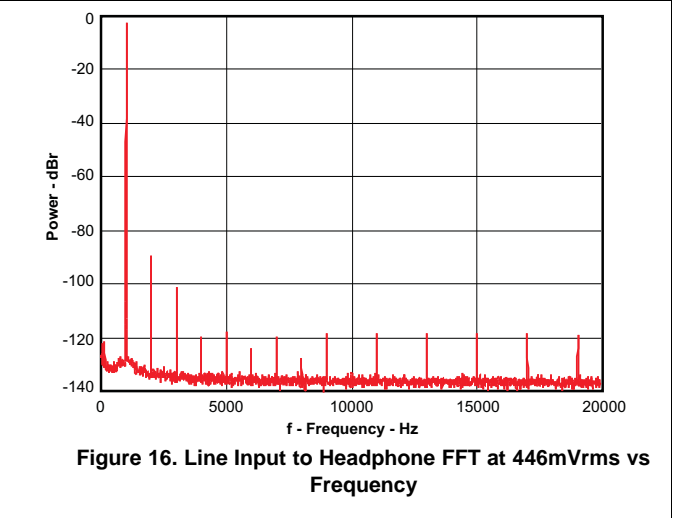
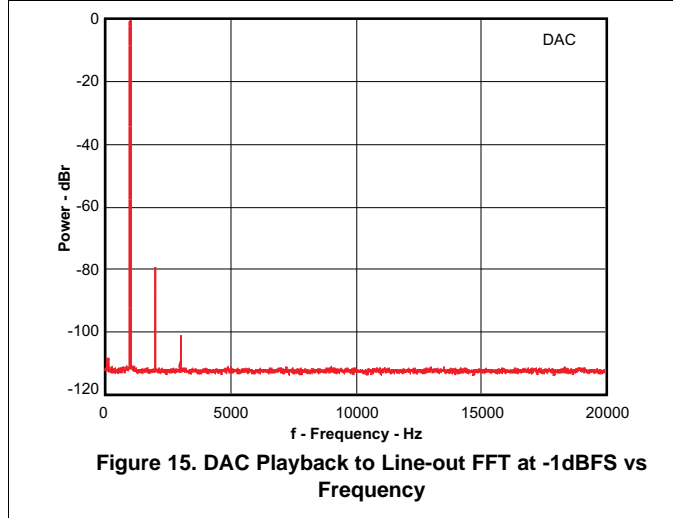
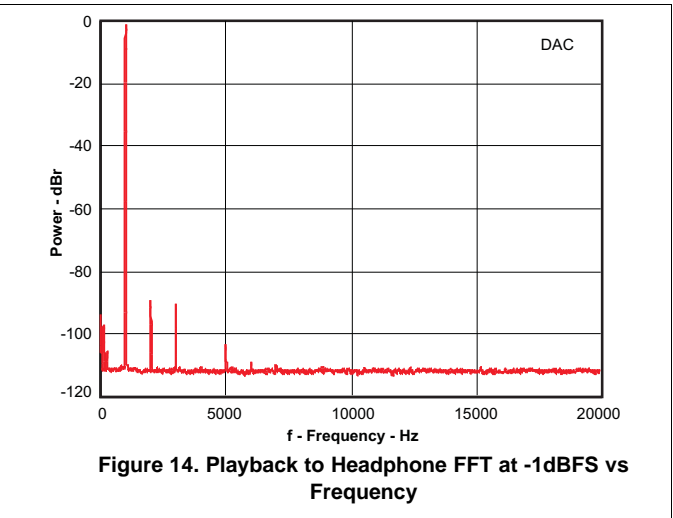
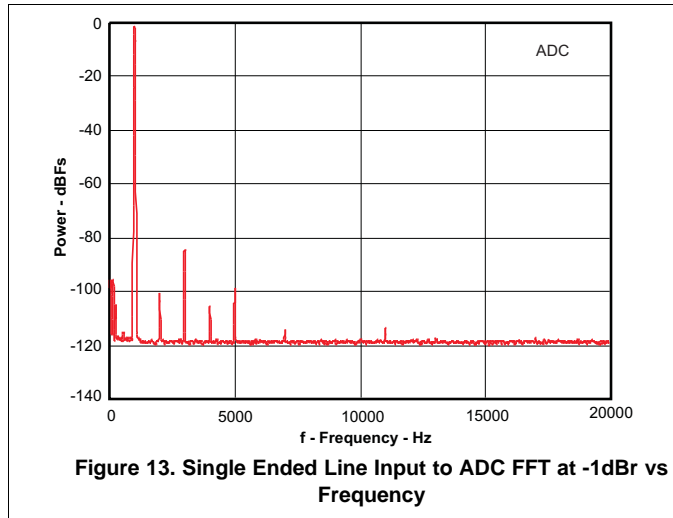


Figure 12. LDO Load Response

8.17.2 Typical Characteristics, FFT



## 9 Parameter Measurement Information

All parameters are measured according to the conditions described in the [Specifications](#) section.

## 10 Detailed Description

### 10.1 Overview

The PCM3070 features two fully-programmable miniDSP cores that support application-specific algorithms in the record and/or the playback path of the device. The miniDSP cores are fully software controlled. Target algorithms, like speaker EQ, Crossovers, Dynamic Range Controls, Intelligent volume controls and other post-processing algorithms are loaded into the device after power-up.

Extensive register-based control of input/output channel configuration, gains, effects, pin-multiplexing and clocks is included, allowing the device to be precisely targeted to its application.

The record path of the PCM3070 covers operations from 8kHz mono to 192kHz stereo recording, and contains programmable input channel configurations covering single-ended and differential setups, as well as floating or mixed input signals.

The playback path offers signal-processing blocks for filtering and effects, and supports flexible mixing of DAC and analog input signals as well as programmable volume controls. The playback path contains two high-power output drivers as well as two fully-differential outputs. The high-power outputs can be configured in multiple ways, including stereo and mono BTL.

The voltage supply range for the PCM3070 for analog is 1.5V–1.95V, and for digital it is 1.26V–1.95V. To ease system-level design, LDOs are integrated to generate the appropriate analog or digital supply from input voltages ranging from 1.8V to 3.6V. Digital I/O voltages are supported in the range of 1.5V–3.6V.

The required internal clock of the PCM3070 can be derived from multiple sources, including the MCLK pin, the BCLK pin, the GPIO pin or the output of the internal PLL, where the input to the PLL again can be derived from the MCLK pin, the BCLK or GPIO pins. The PLL is highly programmable and can accept available input clocks in the range of 512kHz to 50MHz.

## 10.2 Functional Block Diagram

Figure 18 shows the basic functional blocks of the device.

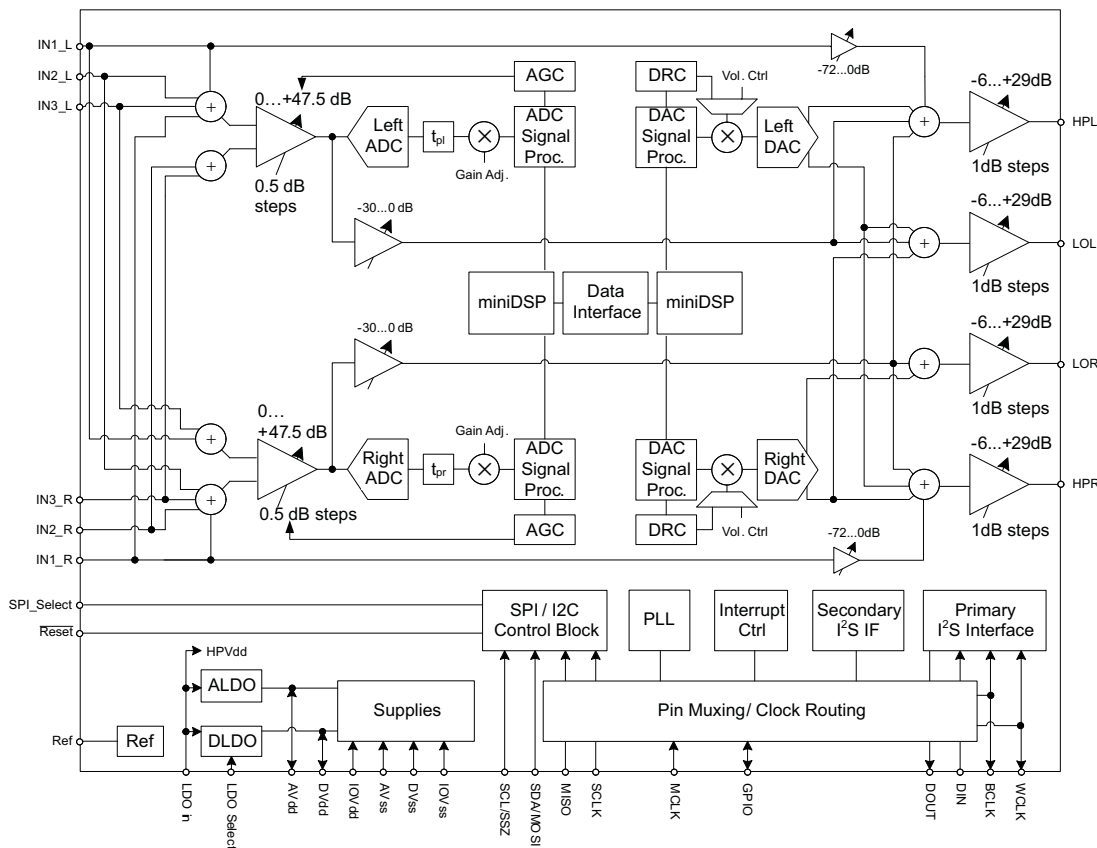


Figure 18. Block Diagram

## 10.3 Feature Description

### 10.3.1 Device Connections

#### 10.3.1.1 Digital Pins

Only a small number of digital pins are dedicated to a single function; whenever possible, the digital pins have a default function, and also can be reprogrammed to cover alternative functions for various applications.

The fixed-function pins are  $\overline{\text{Reset}}$  and the  $\text{SPI\_Select}$  pin, which are HW control pins. Depending on the state of  $\text{SPI\_Select}$ , the two control-bus pins  $\text{SCL}/\overline{\text{SS}}$  and  $\text{SDA}/\text{MOSI}$  are configured for either  $\text{I}^2\text{C}$  or SPI protocol.

Other digital IO pins can be configured for various functions via register control. An overview of available functionality is given in [Multifunction Pins](#).

## Feature Description (continued)

### 10.3.1.1.1 Multifunction Pins

Table 1 shows the possible allocation of pins for specific functions. The PLL input, for example, can be programmed to be any of 4 pins (MCLK, BCLK, DIN, GPIO).

**Table 1. Multifunction Pin Assignments**

|   |                                       | 1                                | 2                | 3    | 4           | 5            | 6             | 7             | 8                |
|---|---------------------------------------|----------------------------------|------------------|------|-------------|--------------|---------------|---------------|------------------|
|   | Pin Function                          | MCLK                             | BCLK             | WCLK | DIN<br>MFP1 | DOUT<br>MFP2 | MFP3/<br>SCLK | MFP4/<br>MISO | GPIO<br>MFP5     |
| A | PLL Input                             | S <sup>(1)</sup>                 | S <sup>(2)</sup> |      | E           |              |               |               | S <sup>(3)</sup> |
| B | Codec Clock Input                     | S <sup>(1),D<sup>(4)</sup></sup> | S <sup>(2)</sup> |      |             |              |               |               | S <sup>(3)</sup> |
| C | I <sup>2</sup> S BCLK input           |                                  | S,D              |      |             |              |               |               |                  |
| D | I <sup>2</sup> S BCLK output          |                                  | E <sup>(5)</sup> |      |             |              |               |               |                  |
| E | I <sup>2</sup> S WCLK input           |                                  |                  | E, D |             |              |               |               |                  |
| F | I <sup>2</sup> S WCLK output          |                                  |                  | E    |             |              |               |               |                  |
| G | I <sup>2</sup> S ADC word clock input |                                  |                  |      |             |              | E             |               | E                |
| H | I <sup>2</sup> S ADC WCLK out         |                                  |                  |      |             |              |               | E             | E                |
| I | I <sup>2</sup> S DIN                  |                                  |                  |      | E, D        |              |               |               |                  |
| J | I <sup>2</sup> S DOUT                 |                                  |                  |      |             | E, D         |               |               |                  |
| K | General Purpose Output I              |                                  |                  |      |             | E            |               |               |                  |
| K | General Purpose Output II             |                                  |                  |      |             |              |               | E             |                  |
| K | General Purpose Output III            |                                  |                  |      |             |              |               |               | E                |
| L | General Purpose Input I               |                                  |                  |      | E           |              |               |               |                  |
| L | General Purpose Input II              |                                  |                  |      |             |              | E             |               |                  |
| L | General Purpose Input III             |                                  |                  |      |             |              |               |               | E                |
| M | INT1 output                           |                                  |                  |      |             | E            |               | E             | E                |
| N | INT2 output                           |                                  |                  |      |             | E            |               | E             | E                |
| Q | Secondary I <sup>2</sup> S BCLK input |                                  |                  |      |             |              | E             |               | E                |
| R | Secondary I <sup>2</sup> S WCLK in    |                                  |                  |      |             |              | E             |               | E                |
| S | Secondary I <sup>2</sup> S DIN        |                                  |                  |      |             |              | E             |               | E                |
| T | Secondary I <sup>2</sup> S DOUT       |                                  |                  |      |             |              |               | E             |                  |
| U | Secondary I <sup>2</sup> S BCLK OUT   |                                  |                  |      |             | E            |               | E             | E                |
| V | Secondary I <sup>2</sup> S WCLK OUT   |                                  |                  |      |             | E            |               | E             | E                |
| W | Reserved                              |                                  |                  |      |             |              |               |               |                  |
| X | Aux Clock Output                      |                                  |                  |      |             | E            |               | E             | E                |

(1) S<sup>(1)</sup>: The MCLK pin can drive the PLL and Codec Clock inputs **simultaneously**.

(2) S<sup>(2)</sup>: The BCLK pin can drive the PLL and Codec Clock and audio interface bit clock inputs **simultaneously**.

(3) S<sup>(3)</sup>: The GPIO/MFP5 pin can drive the PLL and Codec Clock inputs simultaneously.

(4) D: Default Function

(5) E: The pin is **exclusively** used for this function, no other function can be implemented with the same pin. (If GPIO/MFP5 has been allocated for General Purpose Output, it cannot be used as the INT1 output at the same time.)

### 10.3.1.2 Analog Pins

Analog functions can also be configured to a large degree. Analog blocks are powered down by default. The blocks can be powered up with fine granularity according to the application needs.



### 10.3.2 Analog Audio I/O

The analog IO path of the PCM3070 features a large set of options for signal conditioning as well as signal routing:

- 6 analog inputs which can be mixed and-or multiplexed in single-ended and-or differential configuration
- 2 programmable gain amplifiers (PGA) with a range of 0 to +47.5dB
- 2 mixer amplifiers for analog bypass
- 2 low power analog bypass channels
- Mute function
- Automatic gain control (AGC)
- Channel-to-channel phase adjustment
- Fast charge of ac-coupling capacitors
- Anti thump

#### 10.3.2.1 Analog Bypass

The PCM3070 offers two analog-bypass modes. In either of the modes, an analog input signal can be routed from an analog input pin to an amplifier driving an analog output pin. Neither the ADC nor the DAC resources are required for such operation.

In analog low-power bypass mode, line-level signals can be routed directly from the analog inputs INL to the left headphone amplifier (HPL) and INR to HPR.

#### 10.3.2.2 ADC Bypass Using Mixer Amplifiers

In addition to the analog bypass mode, another bypass mode uses the programmable gain amplifiers of the input stage in conjunction with a mixer amplifier. With this mode, low-level signals can be amplified and routed to the line or headphone outputs, fully bypassing the ADC and DAC.

To enable this mode, the mixer amplifiers are powered on via software command.

#### 10.3.2.3 Headphone Output

The stereo headphone drivers on pins HPL and HPR can drive loads with impedances down to 16Ω in single-ended AC-coupled headphone configurations, or loads down to 32Ω in differential mode, where a speaker is connected between HPL and HPR. In single-ended drive configuration these drivers can drive up to 15mW power into each headphone channel while operating from 1.8V analog supplies. While running from the AVdd supply, the output common-mode of the headphone driver is set by the common-mode setting of analog inputs in Page 1 / Register 10, Bit D6, to allow maximum utilization of the analog supply range while simultaneously providing a higher output-voltage swing. In cases when higher output-voltage swing is required, the headphone amplifiers can run directly from the higher supply voltage on LDOIN input (up to 3.6V). To use the higher supply voltage for higher output signal swing, the output common-mode can be adjusted to either 1.25V, 1.5V or 1.65V by configuring Page 1 / Register 10, Bits D5-D4. When the common-mode voltage is configured at 1.65V and LDOIN supply is 3.3V, the headphones can each deliver up to 40mW power into a 16Ω load.

The headphone drivers are capable of driving a mixed combination of DAC signal and bypass from analog input INL and INR by configuring Page 1 / Register 12 and Page 1 / Register 13 respectively. The analog input signals can be attenuated up to 72dB before routing by configuring Page 1 / Register 22 and 23. The level of the DAC signal can be controlled using the digital volume control of the DAC in Page 0, Reg 65 and 66. To control the output-voltage swing of headphone drivers, the digital volume control provides a range of –6.0dB to +29.0dB(6) in steps of 1dB. These can be configured by programming Page 1 / Register 16 and 17. These level controls are not meant to be used as dynamic volume control, but more to set output levels during initial device configuration.

#### 10.3.2.4 Line Outputs

The stereo line level drivers on LOL and LOR pins can drive a wide range of line level resistive impedances in the range of 600Ω to 10kΩ. The output common modes of line level drivers can be configured to equal either the analog input common-mode setting, or 1.65V. With output common-mode setting of 1.65V and DRVdd\_HP supply at 3.3V the line-level drivers can drive up to 1Vrms output signal. The line-level drivers can drive out a mixed combination of DAC signal and attenuated ADC PGA signal. Signal mixing is register-programmable.

### 10.3.3 ADC

The PCM3070 includes a stereo audio ADC, which uses a delta-sigma modulator with a programmable oversampling ratio, followed by a digital decimation filter. The stereo recording path can be powered up one channel at a time, to support the case where only mono record capability is required.

The ADC path of the PCM3070 features a large set of options for signal conditioning as well as signal routing:

- Two ADCs
- Six analog inputs which can be mixed and-or multiplexed in single-ended and-or differential configuration
- Two programmable gain amplifiers (PGA) with a range of 0 to +47.5dB
- Two mixer amplifiers for analog bypass
- Two analog bypass channels
- Fine gain adjustment of digital channels with 0.1dB step size
- Digital volume control with a range of -12 to +20dB
- Mute function
- Automatic gain control (AGC)

In addition to the standard set of ADC features the PCM3070 also offers the following special functions:

- Channel-to-channel phase adjustment
- Fast charge of ac-coupling capacitors
- Anti thump
- Adaptive filter mode

#### 10.3.3.1 ADC Processing

The PCM3070 offers a range of processing blocks which implement various signal processing capabilities along with decimation filtering. These processing blocks give users the choice of how much and what type of signal processing they may use and which decimation filter is applied.

##### 10.3.3.1.1 ADC Processing Blocks

The PCM3070 offers a range of processing blocks which implement various signal processing capabilities along with decimation filtering. These processing blocks give users the choice of how much and what type of signal processing they may use and which decimation filter is applied.

[表 2](#) gives an overview of the available processing blocks and their properties.

The signal processing blocks available are:

- First-order IIR
- Scalable number of biquad filters
- Variable-tap FIR filter
- AGC

The processing blocks are tuned for common cases and can achieve high anti-alias filtering or low group delay in combination with various signal processing effects such as audio effects and frequency shaping. The available first order IIR, BiQuad and FIR filters have fully user-programmable coefficients. The Resource Class Column (RC) gives an approximate indication of power consumption.

**表 2. ADC Processing Blocks**

| Processing Blocks     | Channel | Decimation Filter | 1st Order IIR Available | Number BiQuads | FIR    | Required AOSR Value | Resource Class |
|-----------------------|---------|-------------------|-------------------------|----------------|--------|---------------------|----------------|
| PRB_R1 <sup>(1)</sup> | Stereo  | A                 | Yes                     | 0              | No     | 128,64              | 6              |
| PRB_R2                | Stereo  | A                 | Yes                     | 5              | No     | 128,64              | 8              |
| PRB_R3                | Stereo  | A                 | Yes                     | 0              | 25-Tap | 128,64              | 8              |
| PRB_R4                | Right   | A                 | Yes                     | 0              | No     | 128,64              | 3              |
| PRB_R5                | Right   | A                 | Yes                     | 5              | No     | 128,64              | 4              |
| PRB_R6                | Right   | A                 | Yes                     | 0              | 25-Tap | 128,64              | 4              |
| PRB_R7                | Stereo  | B                 | Yes                     | 0              | No     | 64                  | 3              |
| PRB_R8                | Stereo  | B                 | Yes                     | 3              | No     | 64                  | 4              |
| PRB_R9                | Stereo  | B                 | Yes                     | 0              | 20-Tap | 64                  | 4              |
| PRB_R10               | Right   | B                 | Yes                     | 0              | No     | 64                  | 2              |
| PRB_R11               | Right   | B                 | Yes                     | 3              | No     | 64                  | 2              |
| PRB_R12               | Right   | B                 | Yes                     | 0              | 20-Tap | 64                  | 2              |
| PRB_R13               | Stereo  | C                 | Yes                     | 0              | No     | 32                  | 3              |
| PRB_R14               | Stereo  | C                 | Yes                     | 5              | No     | 32                  | 4              |
| PRB_R15               | Stereo  | C                 | Yes                     | 0              | 25-Tap | 32                  | 4              |
| PRB_R16               | Right   | C                 | Yes                     | 0              | No     | 32                  | 2              |
| PRB_R17               | Right   | C                 | Yes                     | 5              | No     | 32                  | 2              |
| PRB_R18               | Right   | C                 | Yes                     | 0              | 25-Tap | 32                  | 2              |

(1) Default

For more detailed information see the PCM3070 Application Reference Guide, [SLAU332](#).

### 10.3.4 DAC

The PCM3070 includes a stereo audio DAC supporting data rates from 8kHz to 192kHz. Each channel of the stereo audio DAC consists of a signal-processing engine with fixed processing blocks, a programmable miniDSP, a digital interpolation filter, multi-bit digital delta-sigma modulator, and an analog reconstruction filter. The DAC is designed to provide enhanced performance at low sampling rates through increased oversampling and image filtering, thereby keeping quantization noise generated within the delta-sigma modulator and signal images strongly suppressed within the audio band to beyond 20kHz. To handle multiple input rates and optimize performance, the PCM3070 allows the system designer to program the oversampling rates over a wide range from 1 to 1024. The system designer can choose higher oversampling ratios for lower input data rates and lower oversampling ratios for higher input data rates.

The PCM3070 DAC channel includes a built-in digital interpolation filter to generate oversampled data for the sigma-delta modulator. The interpolation filter can be chosen from three different types depending on required frequency response, group delay and sampling rate.

The DAC path of the PCM3070 features many options for signal conditioning and signal routing:

- 2 headphone amplifiers
  - Usable in single-ended or differential mode
  - Analog volume setting with a range of -6 to +29dB
- 2 line-out amplifiers
  - Usable in single-ended or differential mode
  - Analog volume setting with a range of -6 to +29dB
- Digital volume control with a range of -63.5 to +24dB
- Mute function
- Dynamic range compression (DRC)

In addition to the standard set of DAC features the PCM3070 also offers the following special features:

- Built in sine wave generation (beep generator)
- Digital auto mute
- Adaptive filter mode

### 10.3.4.1 DAC Processing Blocks — Overview

The PCM3070 implements signal processing capabilities and interpolation filtering via processing blocks. These fixed processing blocks give users the choice of how much and what type of signal processing they may use and which interpolation filter is applied.

表 3 gives an overview over all available processing blocks of the DAC channel and their properties. The Resource Class Column (RC) gives an approximate indication of power consumption.

The signal processing blocks available are:

- First-order IIR
- Scalable number of biquad filters
- 3D – Effect
- Beep Generator

The processing blocks are tuned for typical cases and can achieve high image rejection or low group delay in combination with various signal processing effects such as audio effects and frequency shaping. The available first-order IIR and biquad filters have fully user-programmable coefficients. The Resource Class Column (RC) gives an approximate indication of power consumption.

**表 3. Overview – DAC Predefined Processing Blocks**

| Processing Block No.  | Interpolation Filter | Channel | 1st Order IIR Available | Num. of Biquads | DRC | 3D  | Beep Generator |
|-----------------------|----------------------|---------|-------------------------|-----------------|-----|-----|----------------|
| PRB_P1 <sup>(1)</sup> | A                    | Stereo  | No                      | 3               | No  | No  | No             |
| PRB_P2                | A                    | Stereo  | Yes                     | 6               | Yes | No  | No             |
| PRB_P3                | A                    | Stereo  | Yes                     | 6               | No  | No  | No             |
| PRB_P4                | A                    | Left    | No                      | 3               | No  | No  | No             |
| PRB_P5                | A                    | Left    | Yes                     | 6               | Yes | No  | No             |
| PRB_P6                | A                    | Left    | Yes                     | 6               | No  | No  | No             |
| PRB_P7                | B                    | Stereo  | Yes                     | 0               | No  | No  | No             |
| PRB_P8                | B                    | Stereo  | No                      | 4               | Yes | No  | No             |
| PRB_P9                | B                    | Stereo  | No                      | 4               | No  | No  | No             |
| PRB_P10               | B                    | Stereo  | Yes                     | 6               | Yes | No  | No             |
| PRB_P11               | B                    | Stereo  | Yes                     | 6               | No  | No  | No             |
| PRB_P12               | B                    | Left    | Yes                     | 0               | No  | No  | No             |
| PRB_P13               | B                    | Left    | No                      | 4               | Yes | No  | No             |
| PRB_P14               | B                    | Left    | No                      | 4               | No  | No  | No             |
| PRB_P15               | B                    | Left    | Yes                     | 6               | Yes | No  | No             |
| PRB_P16               | B                    | Left    | Yes                     | 6               | No  | No  | No             |
| PRB_P17               | C                    | Stereo  | Yes                     | 0               | No  | No  | No             |
| PRB_P18               | C                    | Stereo  | Yes                     | 4               | Yes | No  | No             |
| PRB_P19               | C                    | Stereo  | Yes                     | 4               | No  | No  | No             |
| PRB_P20               | C                    | Left    | Yes                     | 0               | No  | No  | No             |
| PRB_P21               | C                    | Left    | Yes                     | 4               | Yes | No  | No             |
| PRB_P22               | C                    | Left    | Yes                     | 4               | No  | No  | No             |
| PRB_P23               | A                    | Stereo  | No                      | 2               | No  | Yes | No             |
| PRB_P24               | A                    | Stereo  | Yes                     | 5               | Yes | Yes | No             |
| PRB_P25               | A                    | Stereo  | Yes                     | 5               | Yes | Yes | Yes            |

(1) Default

For more detailed information see the PCM3070 Application Reference Guide, [SLAU332](#).

### 10.3.5 Digital Audio IO Interface

Audio data is transferred between the host processor and the PCM3070 via the digital audio data serial interface, or audio bus. The audio bus on this device is very flexible, including left or right-justified data options, support for I2S or PCM protocols, programmable data length options, a TDM mode for multichannel operation, very flexible master/slave configurability for each bus clock line, and the ability to communicate with multiple devices within a system directly.

The audio bus of the PCM3070 can be configured for left or right-justified, I2S, DSP, or TDM modes of operation, where communication with standard PCM interfaces is supported within the TDM mode. These modes are all MSB-first, with data width programmable as 16, 20, 24, or 32 bits by configuring Page 0, Register 27, D(5:4). In addition, the word clock and bit clock can be independently configured in either Master or Slave mode, for flexible connectivity to a wide variety of processors. The word clock is used to define the beginning of a frame, and may be programmed as either a pulse or a square-wave signal. The frequency of this clock corresponds to the maximum of the selected ADC and DAC sampling frequencies.

The bit clock is used to clock in and clock out the digital audio data across the serial bus. When in Master mode, this signal can be programmed to generate variable clock pulses by controlling the bit-clock divider in Page 0, Register 30. The number of bit-clock pulses in a frame may need adjustment to accommodate various word-lengths as well as to support the case when multiple PCM3070s may share the same audio bus.

The PCM3070 also includes a feature to offset the position of start of data transfer with respect to the word-clock. This offset can be controlled in terms of number of bit-clocks and can be programmed in Page 0, Register 28.

The PCM3070 also has the feature of inverting the polarity of the bit-clock used for transferring the audio data as compared to the default clock polarity used. This feature can be used independently of the mode of audio interface chosen. This can be configured via Page 0, Register 29, D(3).

The PCM3070 further includes programmability (Page 0, Register 27, D0) to place the DOUT line into a hi-Z (3-state) condition during all bit clocks when valid data is not being sent. By combining this capability with the ability to program at what bit clock in a frame the audio data begins, time-division multiplexing (TDM) can be accomplished, enabling the use of multiple codecs on a single audio serial data bus. When the audio serial data bus is powered down while configured in master mode, the pins associated with the interface are put into a hi-Z output condition.

By default when the word-clocks and bit-clocks are generated by the PCM3070, these clocks are active only when the codec (ADC, DAC or both) are powered up within the device. This is done to save power. However, it also supports a feature when both the word clocks and bit-clocks can be active even when the codec in the device is powered down. This is useful when using the TDM mode with multiple codecs on the same bus, or when word-clock or bit-clocks are used in the system as general-purpose clocks.

### 10.3.6 Clock Generation and PLL

The PCM3070 supports a wide range of options for generating clocks for the ADC and DAC sections as well as interface and other control blocks. The clocks for ADC and DAC require a source reference clock. This clock can be provided on variety of device pins such as MCLK, BCLK or GPIO pins. The CODEC\_CLKIN can then be routed through highly-flexible clock dividers to generate the various clocks required for ADC, DAC and the miniDSP sections. In the event that the desired audio or miniDSP clocks cannot be generated from the reference clocks on MCLK BCLK or GPIO, the PCM3070 also provides the option of using the on-chip PLL which supports a wide range of fractional multiplication values to generate the required clocks. Starting from CODEC\_CLKIN the PCM3070 provides several programmable clock dividers to help achieve a variety of sampling rates for ADC, DAC and clocks for the miniDSP.

For more detailed information see the PCM3070 Application Reference Guide, [SLAU332](#).

### 10.3.7 Control Interfaces

The PCM3070 control interface supports SPI or I<sup>2</sup>C communication protocols, with the protocol selectable using the SPI\_SELECT pin. For SPI, SPI\_SELECT should be tied high; for I<sup>2</sup>C, SPI\_SELECT should be tied low. Changing the state of SPI\_SELECT during device operation is not recommended.

### 10.3.7.1 I<sup>2</sup>C Control

The PCM3070 supports the I<sup>2</sup>C control protocol, and will respond to the I<sup>2</sup>C address of 0011000. I<sup>2</sup>C is a two-wire, open-drain interface supporting multiple devices and masters on a single bus. Devices on the I<sup>2</sup>C bus only drive the bus lines LOW by connecting them to ground; they never drive the bus lines HIGH. Instead, the bus wires are pulled HIGH by pullup resistors, so the bus wires are HIGH when no device is driving them LOW. This circuit prevents two devices from conflicting; if two devices drive the bus simultaneously, there is no driver contention.

### 10.3.7.2 SPI Control

In the SPI control mode, the PCM3070 uses the pins SCL/ $\overline{SS}$  as  $\overline{SS}$ , SCLK as SCLK, MISO as MISO, SDA/MOSI as MOSI; a standard SPI port with clock polarity setting of 0 (typical microprocessor SPI control bit CPOL = 0). The SPI port allows full-duplex, synchronous, serial communication between a host processor (the master) and peripheral devices (slaves). The SPI master (in this case, the host processor) generates the synchronizing clock (driven onto SCLK) and initiates transmissions. The SPI slave devices (such as the PCM3070) depend on a master to start and synchronize transmissions. A transmission begins when initiated by an SPI master. The byte from the SPI master begins shifting in on the slave MOSI pin under the control of the master serial clock (driven onto SCLK). As the byte shifts in on the MOSI pin, a byte shifts out on the MISO pin to the master shift register.

For more detailed information see the PCM3070 Application Reference Guide, [SLAU332](#).

## 10.4 Device Functional Modes

The following special functions are available to support advanced system requirements:

- Interrupt generation
- Flexible pin multiplexing

For more detailed information see the PCM3070 Application Reference Guide, [SLAU332](#).

### 10.4.1 MiniDSP

The PCM3070 features two miniDSP cores. The first miniDSP core is tightly coupled to the ADC, the second miniDSP core is tightly coupled to the DAC. The fully programmable algorithms for the miniDSP must be loaded into the device after power up. The miniDSPs have direct access to the digital stereo audio stream on the ADC and on the DAC side, offering the possibility for advanced, very-low group delay DSP algorithms. Each miniDSP can run up to 1152 instructions on every audio sample at a 48kHz sample rate. The two cores can run fully synchronized and can exchange data.

### 10.4.2 Software

Software development for the PCM3070 is supported through TI's comprehensive PurePath Studio Development Environment; a powerful, easy-to-use tool designed specifically to simplify software development on the PCM3070 miniDSP audio platform. The Graphical Development Environment consists of a library of common audio functions that can be dragged-and-dropped into an audio signal flow and graphically connected together. The DSP code can then be assembled from the graphical signal flow with the click of a mouse.

Please visit the PCM3070 product folder on [www.ti.com](http://www.ti.com) to learn more about PurePath Studio and the latest status on available, ready-to-use DSP algorithms.



## 10.5 Register Map

### 10.5.1 Register Map Summary

**Table 4. Summary of Register Map**

| Decimal  |          | Hex      |           | DESCRIPTION   |
|----------|----------|----------|-----------|---|
| PAGE NO. | REG. NO. | PAGE NO. | REG. NO.  |   |
| 0        | 0        | 0x00     | 0x00      | Page Select Register  |
| 0        | 1        | 0x00     | 0x01      | Software Reset Register                                       |
| 0        | 2        | 0x00     | 0x02      | Reserved Register   |
| 0        | 3        | 0x00     | 0x03      | Reserved Register   |
| 0        | 4        | 0x00     | 0x04      | Clock Setting Register 1, Multiplexers                        |
| 0        | 5        | 0x00     | 0x05      | Clock Setting Register 2, PLL P&R Values                      |
| 0        | 6        | 0x00     | 0x06      | Clock Setting Register 3, PLL J Values                        |
| 0        | 7        | 0x00     | 0x07      | Clock Setting Register 4, PLL D Values (MSB)                  |
| 0        | 8        | 0x00     | 0x08      | Clock Setting Register 5, PLL D Values (LSB)                  |
| 0        | 9-10     | 0x00     | 0x09-0x0A | Reserved Register   |
| 0        | 11       | 0x00     | 0x0B      | Clock Setting Register 6, NDAC Values                         |
| 0        | 12       | 0x00     | 0x0C      | Clock Setting Register 7, MDAC Values                         |
| 0        | 13       | 0x00     | 0x0D      | DAC OSR Setting Register 1, MSB Value                         |
| 0        | 14       | 0x00     | 0x0E      | DAC OSR Setting Register 2, LSB Value                         |
| 0        | 15       | 0x00     | 0x0F      | miniDSP_D Instruction Control Register 1                      |
| 0        | 16       | 0x00     | 0x10      | miniDSP_D Instruction Control Register 2                      |
| 0        | 17       | 0x00     | 0x11      | miniDSP_D Interpolation Factor Setting Register               |
| 0        | 18       | 0x00     | 0x12      | Clock Setting Register 8, NADC Values                         |
| 0        | 19       | 0x00     | 0x13      | Clock Setting Register 9, MADC Values                         |
| 0        | 20       | 0x00     | 0x14      | ADC Oversampling (AOSR) Register                              |
| 0        | 21       | 0x00     | 0x15      | miniDSP_A Instruction Control Register 1                      |
| 0        | 22       | 0x00     | 0x16      | miniDSP_A Instruction Control Register 2                      |
| 0        | 23       | 0x00     | 0x17      | miniDSP_A Decimation Factor Setting Register                  |
| 0        | 24       | 0x00     | 0x18      | Reserved Register   |
| 0        | 25       | 0x00     | 0x19      | Clock Setting Register 10, Multiplexers                       |
| 0        | 26       | 0x00     | 0x1A      | Clock Setting Register 11, CLKOUT M divider value             |
| 0        | 27       | 0x00     | 0x1B      | Audio Interface Setting Register 1                            |
| 0        | 28       | 0x00     | 0x1C      | Audio Interface Setting Register 2, Data offset setting       |
| 0        | 29       | 0x00     | 0x1D      | Audio Interface Setting Register 3                            |
| 0        | 30       | 0x00     | 0x1E      | Clock Setting Register 12, BCLK N Divider                     |
| 0        | 31       | 0x00     | 0x1F      | Audio Interface Setting Register 4, Secondary Audio Interface |
| 0        | 32       | 0x00     | 0x20      | Audio Interface Setting Register 5                            |
| 0        | 33       | 0x00     | 0x21      | Audio Interface Setting Register 6                            |
| 0        | 34       | 0x00     | 0x22      | Digital Interface Misc. Setting Register                      |
| 0        | 35       | 0x00     | 0x23      | Reserved Register   |
| 0        | 36       | 0x00     | 0x24      | ADC Flag Register   |
| 0        | 37       | 0x00     | 0x25      | DAC Flag Register 1   |
| 0        | 38       | 0x00     | 0x26      | DAC Flag Register 2   |
| 0        | 39-41    | 0x00     | 0x27-0x29 | Reserved Register   |
| 0        | 42       | 0x00     | 0x2A      | Sticky Flag Register 1  |
| 0        | 43       | 0x00     | 0x2B      | Interrupt Flag Register 1                                     |
| 0        | 44       | 0x00     | 0x2C      | Sticky Flag Register 2  |
| 0        | 45       | 0x00     | 0x2D      | Sticky Flag Register 3  |

**Register Map (continued)**
**Table 4. Summary of Register Map (continued)**

| Decimal  |          | Hex      |           | DESCRIPTION                                       |
|----------|----------|----------|-----------|---|
| PAGE NO. | REG. NO. | PAGE NO. | REG. NO.  |   |
| 0        | 46       | 0x00     | 0x2E      | Interrupt Flag Register 2                         |
| 0        | 47       | 0x00     | 0x2F      | Interrupt Flag Register 3                         |
| 0        | 48       | 0x00     | 0x30      | INT1 Interrupt Control Register                   |
| 0        | 49       | 0x00     | 0x31      | INT2 Interrupt Control Register                   |
| 0        | 50-51    | 0x00     | 0x32-0x33 | Reserved Register                                 |
| 0        | 52       | 0x00     | 0x34      | GPIO/MFP5 Control Register                        |
| 0        | 53       | 0x00     | 0x35      | DOUT/MFP2 Function Control Register               |
| 0        | 54       | 0x00     | 0x36      | DIN/MFP1 Function Control Register                |
| 0        | 55       | 0x00     | 0x37      | MISO/MFP4 Function Control Register               |
| 0        | 56       | 0x00     | 0x38      | SCLK/MFP3 Function Control Register               |
| 0        | 57-59    | 0x00     | 0x39-0x3B | Reserved Registers                                |
| 0        | 60       | 0x00     | 0x3C      | DAC Signal Processing Block Control Register      |
| 0        | 61       | 0x00     | 0x3D      | ADC Signal Processing Block Control Register      |
| 0        | 62       | 0x00     | 0x3E      | miniDSP_A and miniDSP_D Configuration Register    |
| 0        | 63       | 0x00     | 0x3F      | DAC Channel Setup Register 1                      |
| 0        | 64       | 0x00     | 0x40      | DAC Channel Setup Register 2                      |
| 0        | 65       | 0x00     | 0x41      | Left DAC Channel Digital Volume Control Register  |
| 0        | 66       | 0x00     | 0x42      | Right DAC Channel Digital Volume Control Register |
| 0        | 67       | 0x00     | 0x43      | Headset Detection Configuration Register          |
| 0        | 68       | 0x00     | 0x44      | DRC Control Register 1                            |
| 0        | 69       | 0x00     | 0x45      | DRC Control Register 2                            |
| 0        | 70       | 0x00     | 0x46      | DRC Control Register 3                            |
| 0        | 71       | 0x00     | 0x47      | Beep Generator Register 1                         |
| 0        | 72       | 0x00     | 0x48      | Beep Generator Register 2                         |
| 0        | 73       | 0x00     | 0x49      | Beep Generator Register 3                         |
| 0        | 74       | 0x00     | 0x4A      | Beep Generator Register 4                         |
| 0        | 75       | 0x00     | 0x4B      | Beep Generator Register 5                         |
| 0        | 76       | 0x00     | 0x4C      | Beep Generator Register 6                         |
| 0        | 77       | 0x00     | 0x4D      | Beep Generator Register 7                         |
| 0        | 78       | 0x00     | 0x4E      | Beep Generator Register 8                         |
| 0        | 79       | 0x00     | 0x4F      | Beep Generator Register 9                         |
| 0        | 80       | 0x00     | 0x50      | Reserved Register                                 |
| 0        | 81       | 0x00     | 0x51      | ADC Channel Setup Register                        |
| 0        | 82       | 0x00     | 0x52      | ADC Fine Gain Adjust Register                     |
| 0        | 83       | 0x00     | 0x53      | Left ADC Channel Volume Control Register          |
| 0        | 84       | 0x00     | 0x54      | Right ADC Channel Volume Control Register         |
| 0        | 85       | 0x00     | 0x55      | ADC Phase Adjust Register                         |
| 0        | 86       | 0x00     | 0x56      | Left Channel AGC Control Register 1               |
| 0        | 87       | 0x00     | 0x57      | Left Channel AGC Control Register 2               |
| 0        | 88       | 0x00     | 0x58      | Left Channel AGC Control Register 3               |
| 0        | 89       | 0x00     | 0x59      | Left Channel AGC Control Register 4               |
| 0        | 90       | 0x00     | 0x5A      | Left Channel AGC Control Register 5               |
| 0        | 91       | 0x00     | 0x5B      | Left Channel AGC Control Register 6               |
| 0        | 92       | 0x00     | 0x5C      | Left Channel AGC Control Register 7               |
| 0        | 93       | 0x00     | 0x5D      | Left Channel AGC Control Register 8               |



**Register Map (continued)**
**Table 4. Summary of Register Map (continued)**

| Decimal  |          | Hex      |           | DESCRIPTION   |
|----------|----------|----------|-----------|---|
| PAGE NO. | REG. NO. | PAGE NO. | REG. NO.  |   |
| 0        | 94       | 0x00     | 0x5E      | Right Channel AGC Control Register 1                            |
| 0        | 95       | 0x00     | 0x5F      | Right Channel AGC Control Register 2                            |
| 0        | 96       | 0x00     | 0x60      | Right Channel AGC Control Register 3                            |
| 0        | 97       | 0x00     | 0x61      | Right Channel AGC Control Register 4                            |
| 0        | 98       | 0x00     | 0x62      | Right Channel AGC Control Register 5                            |
| 0        | 99       | 0x00     | 0x63      | Right Channel AGC Control Register 6                            |
| 0        | 100      | 0x00     | 0x64      | Right Channel AGC Control Register 7                            |
| 0        | 101      | 0x00     | 0x65      | Right Channel AGC Control Register 8                            |
| 0        | 102      | 0x00     | 0x66      | DC Measurement Register 1                                       |
| 0        | 103      | 0x00     | 0x67      | DC Measurement Register 2                                       |
| 0        | 104      | 0x00     | 0x68      | Left Channel DC Measurement Output Register 1                   |
| 0        | 105      | 0x00     | 0x69      | Left Channel DC Measurement Output Register 2                   |
| 0        | 106      | 0x00     | 0x6A      | Left Channel DC Measurement Output Register 3                   |
| 0        | 107      | 0x00     | 0x6B      | Right Channel DC Measurement Output Register 1                  |
| 0        | 108      | 0x00     | 0x6C      | Right Channel DC Measurement Output Register 2                  |
| 0        | 109      | 0x00     | 0x6D      | Right Channel DC Measurement Output Register 3                  |
| 0        | 110-127  | 0x00     | 0x6E-0x7F | Reserved Register   |
| 1        | 0        | 0x01     | 0x00      | Page Select Register  |
| 1        | 1        | 0x01     | 0x01      | LDO Control Register  |
| 1        | 2        | 0x01     | 0x02      | Power Configuration Register 2                                  |
| 1        | 3        | 0x01     | 0x03      | Playback Configuration Register 1                               |
| 1        | 4        | 0x01     | 0x04      | Playback Configuration Register 2                               |
| 1        | 5-8      | 0x01     | 0x05-0x08 | Reserved Register   |
| 1        | 9        | 0x01     | 0x09      | Output Driver Power Control Register                            |
| 1        | 10       | 0x01     | 0x0A      | Common Mode Control Register                                    |
| 1        | 11       | 0x01     | 0x0B      | Over Current Protection Configuration Register                  |
| 1        | 12       | 0x01     | 0x0C      | HPL Routing Selection Register                                  |
| 1        | 13       | 0x01     | 0x0D      | HPR Routing Selection Register                                  |
| 1        | 14       | 0x01     | 0x0E      | LOL Routing Selection Register                                  |
| 1        | 15       | 0x01     | 0x0F      | LOR Routing Selection Register                                  |
| 1        | 16       | 0x01     | 0x10      | HPL Driver Gain Setting Register                                |
| 1        | 17       | 0x01     | 0x11      | HPR Driver Gain Setting Register                                |
| 1        | 18       | 0x01     | 0x12      | LOL Driver Gain Setting Register                                |
| 1        | 19       | 0x01     | 0x13      | LOR Driver Gain Setting Register                                |
| 1        | 20       | 0x01     | 0x14      | Headphone Driver Startup Control Register                       |
| 1        | 21       | 0x01     | 0x15      | Reserved Register   |
| 1        | 22       | 0x01     | 0x16      | IN1L to HPL Volume Control Register                             |
| 1        | 23       | 0x01     | 0x17      | IN1R to HPR Volume Control Register                             |
| 1        | 24       | 0x01     | 0x18      | Mixer Amplifier Left Volume Control Register                    |
| 1        | 25       | 0x01     | 0x19      | Mixer Amplifier Right Volume Control Register                   |
| 1        | 26-50    | 0x01     | 0x1A-0x32 | Reserved Register   |
| 1        | 51       | 0x01     | 0x33      | Reserved. Do Not Use  |
| 1        | 52       | 0x01     | 0x34      | Left PGA Positive Terminal Input Routing Configuration Register |
| 1        | 53       | 0x01     | 0x35      | Reserved Register   |
| 1        | 54       | 0x01     | 0x36      | Left PGA Negative Terminal Input Routing Configuration Register |

**Register Map (continued)**
**Table 4. Summary of Register Map (continued)**

| Decimal  |          | Hex       |           | DESCRIPTION  |
|----------|----------|-----------|-----------|--|
| PAGE NO. | REG. NO. | PAGE NO.  | REG. NO.  |  |
| 1        | 55       | 0x01      | 0x37      | Right PGA Positive Terminal Input Routing Configuration Register |
| 1        | 56       | 0x01      | 0x38      | Reserved Register  |
| 1        | 57       | 0x01      | 0x39      | Right PGA Negative Terminal Input Routing Configuration Register |
| 1        | 58       | 0x01      | 0x3A      | Floating Input Configuration Register                            |
| 1        | 59       | 0x01      | 0x3B      | Left PGA Volume Control Register                                 |
| 1        | 60       | 0x01      | 0x3C      | Right PGA Volume Control Register                                |
| 1        | 61       | 0x01      | 0x3D      | Reserved. Do Not Use   |
| 1        | 62       | 0x01      | 0x3E      | ADC Analog Volume Control Flag Register                          |
| 1        | 63       | 0x01      | 0x3F      | DAC Analog Gain Control Flag Register                            |
| 1        | 64-70    | 0x01      | 0x40-0x46 | Reserved Register  |
| 1        | 71       | 0x01      | 0x47      | Analog Input Quick Charging Configuration Register               |
| 1        | 72-122   | 0x01      | 0x48-0x7A | Reserved Register  |
| 1        | 123      | 0x01      | 0x7B      | Reference Power-up Configuration Register                        |
| 1        | 124-127  | 0x01      | 0x7C-0x7F | Reserved Register  |
| 8        | 0        | 0x08      | 0x00      | Page Select Register   |
| 8        | 1        | 0x08      | 0x01      | ADC Adaptive Filter Configuration Register                       |
| 8        | 2-7      | 0x08      | 0x02-0x07 | Reserved   |
| 8        | 8-127    | 0x08      | 0x08-0x7F | ADC Coefficients Buffer-A C(0:29)                                |
| 9-16     | 0        | 0x09-0x10 | 0x00      | Page Select Register   |
| 9-16     | 1-7      | 0x09-0x10 | 0x01-0x07 | Reserved   |
| 9-16     | 8-127    | 0x09-0x10 | 0x08-0x7F | ADC Coefficients Buffer-A C(30:255)                              |
| 26-34    | 0        | 0x1A-0x22 | 0x00      | Page Select Register   |
| 26-34    | 1-7      | 0x1A-0x22 | 0x01-0x07 | Reserved.  |
| 26-34    | 8-127    | 0x1A-0x22 | 0x08-0x7F | ADC Coefficients Buffer-B C(0:255)                               |
| 44       | 0        | 0x2C      | 0x00      | Page Select Register   |
| 44       | 1        | 0x2C      | 0x01      | DAC Adaptive Filter Configuration Register                       |
| 44       | 2-7      | 0x2C      | 0x02-0x07 | Reserved   |
| 44       | 8-127    | 0x2C      | 0x08-0x7F | DAC Coefficients Buffer-A C(0:29)                                |
| 45-52    | 0        | 0x2D-0x34 | 0x00      | Page Select Register   |
| 45-52    | 1-7      | 0x2D-0x34 | 0x01-0x07 | Reserved.  |
| 45-52    | 8-127    | 0x2D-0x34 | 0x08-0x7F | DAC Coefficients Buffer-A C(30:255)                              |
| 62-70    | 0        | 0x3E-0x46 | 0x00      | Page Select Register   |
| 62-70    | 1-7      | 0x3E-0x46 | 0x01-0x07 | Reserved.  |
| 62-70    | 8-127    | 0x3E-0x46 | 0x08-0x7F | DAC Coefficients Buffer-B C(0:255)                               |
| 80-114   | 0        | 0x50-0x72 | 0x00      | Page Select Register   |
| 80-114   | 1-7      | 0x50-0x72 | 0x01-0x07 | Reserved.  |
| 80-114   | 8-127    | 0x50-0x72 | 0x08-0x7F | miniDSP_A Instructions   |
| 152-186  | 0        | 0x98-0xBA | 0x00      | Page Select Register   |
| 152-186  | 1-7      | 0x98-0xBA | 0x01-0x07 | Reserved.  |
| 152-186  | 8-127    | 0x98-0xBA | 0x08-0x7F | miniDSP_D Instructions   |

## 11 Application and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

### 11.1 Application Information

The PCM3070 is a highly integrated stereo audio codec with integrated miniDSP and flexible digital audio interface options. It enables many different types of audio platforms having a need for stereo audio record and playback and needing to interface with other devices in the system over a digital audio interface.

### 11.2 Typical Application

图 19 shows a typical circuit configuration for a system using the PCM3070.

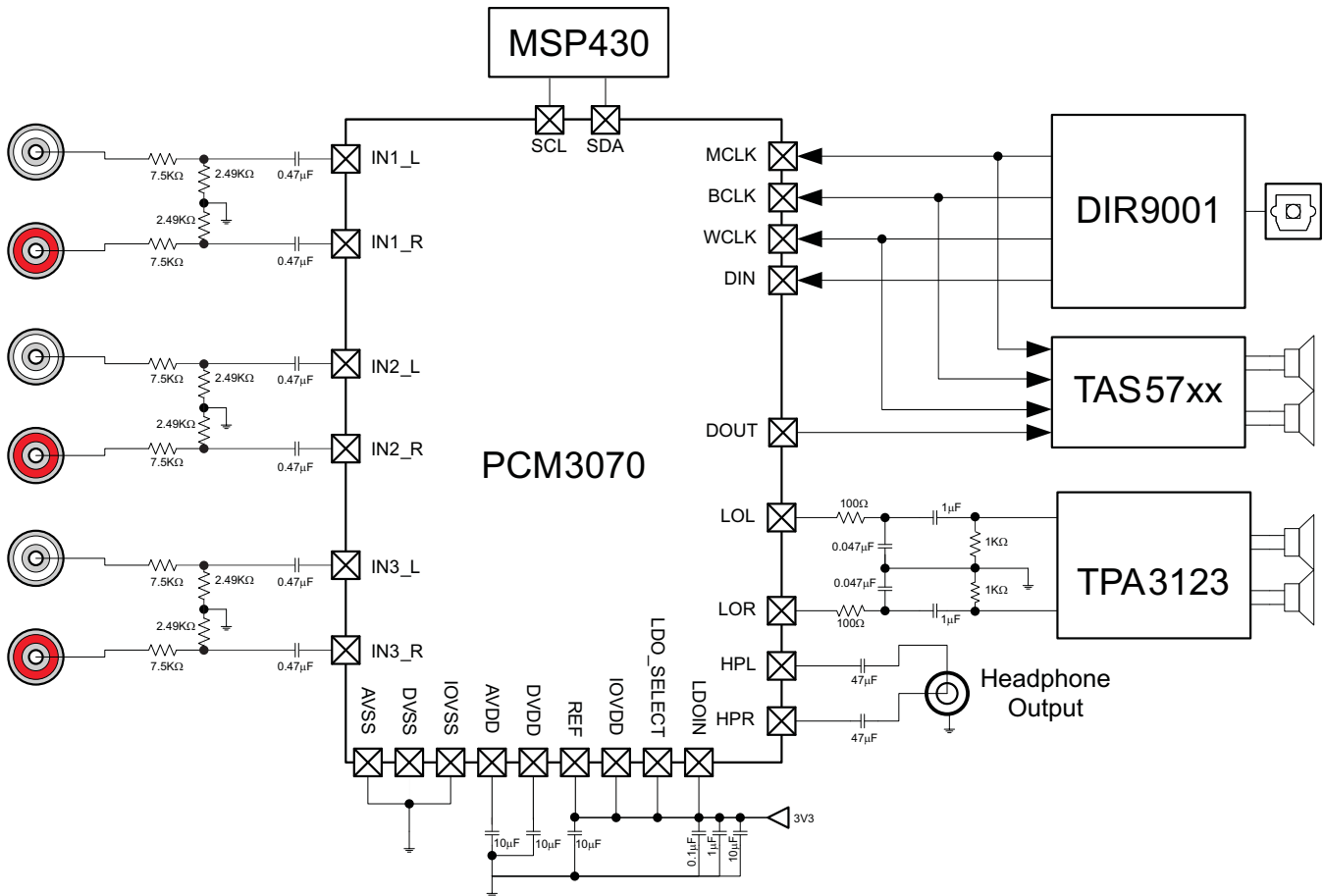


图 19. Typical Circuit Configuration

## Typical Application (接下页)

### 11.2.1 Design Requirements

#### 11.2.1.1 Reference Filtering Capacitor

The PCM3070 has a built-in bandgap used to generate reference voltages and currents for the device. To achieve high SNR, the reference voltage on REF should be filtered using a 10- $\mu$ F capacitor from REF terminal to ground.

### 11.2.2 Detailed Design Procedures

#### 11.2.2.1 Analog Input Connection

The analog inputs to PCM3070 should be ac-coupled to the device terminals to allow decoupling of signal source's common mode voltage with that of PCM3070's common mode voltage. The input coupling capacitor in combination with the selected input impedance of PCM3070 forms a high-pass filter.

$$F_c = 1/(2 \times \pi \times R_{eq} C_c) \quad (1)$$

$$C_c = 1/(2 \times \pi \times R_{eq} F_c) \quad (2)$$

For high fidelity audio recording application it is desirable to keep the cutoff frequency of the high pass filter as low as possible. For single-ended input mode, the equivalent input resistance  $R_{eq}$  can be calculated as

$$R_{eq} = R_{in} \times (1 + 2g)/(1+g) \quad (3)$$

where  $g$  is the analog PGA gain calculated in linear terms.

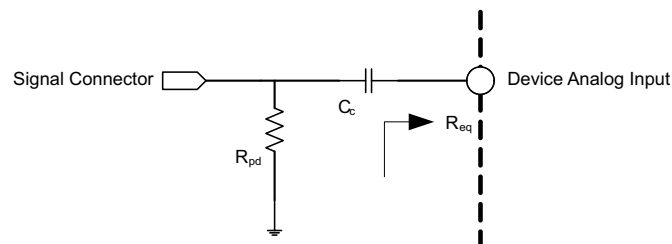
$$g = 10000 \times 2^{\text{floor}(G/6)}/R_{in} \quad (4)$$

where  $G$  is the analog PGA gain programmed in P1\_R59-R60 (in dB) and  $R_{in}$  is the value of the resistor programmed in P1\_R52-R57 and assumes  $R_{in} = R_{cm}$  (as defined in P1\_R52-R57).

For differential input mode,  $R_{eq}$  of the half circuit can be calculated as:

$$R_{eq} = R_{in} \quad (5)$$

where  $R_{in}$  is the value of the resistor programmed in P1\_R52-R57, assuming symmetrical inputs.



**图 20. Analog Input Connection With Pull-down Resistor**

When the analog signal is connected to the system through a connector such as audio jack, it is recommended to put a pull-down resistor on the signal as shown in 图 20. The pulldown resistor helps keep the signal grounded and helps improve noise immunity when no source is connected to the connector. The pulldown resistor value should be chosen large enough to avoid loading of signal source.

Each analog input of the PCM3070 is capable of handling signal amplitude of 0.5 Vrms. If the input signal source can drive signals higher than the maximum value, an external resistor divider network as shown in 图 21 should be used to attenuate the signal to less than 0.5Vrms before connecting the signal to the device. The resistor values of the network should be chosen to provide desired attenuation as well as 公式 6.

$$R_1 \parallel R_2 \ll R_{eq} \quad (6)$$

Typical Application (接下页)

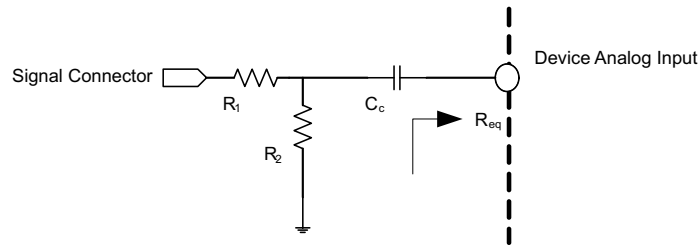


图 21. Analog Input Connection With Resistor Divider Network

Whenever any of the analog input terminals IN1\_L, IN2\_L, IN3\_L, IN1\_R, IN2\_R or IN3\_R are not used in an application, it is recommended to short the unused input terminals together (if convenient) and connect them to ground using a small capacitor (example 0.1 μF).

11.2.2.2 Analog Output Connection

The line outputs of the PCM3070 drive a signal biased around the device common mode voltage. To avoid loading the common mode with the load, it is recommended to connect the single-ended load through an ac-coupling capacitor. The ac-coupling capacitor in combination with the load impedance forms a high pass filter.

$$F_c = 1/(2 \times \pi \times R_L C_c) \tag{7}$$

$$C_c = 1/(2 \times \pi \times R_L F_c) \tag{8}$$

For high fidelity playback, the cutoff frequency of the resultant high-pass filter should be kept low. For example with  $R_L$  of 10 kΩ, using 1-μF coupling capacitor results in a cut-off frequency of 8 Hz.

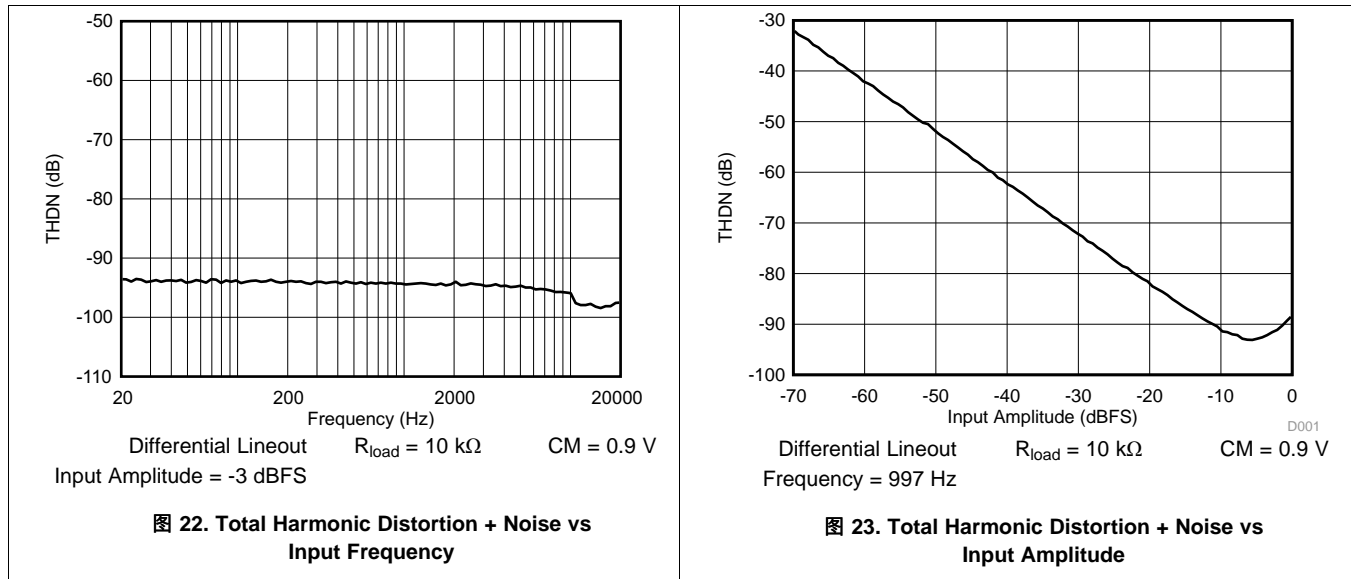
For differential lineout configurations, the load should be directly connected between the differential outputs, with no coupling capacitor.

Whenever any of the analog output terminals LOL, LOR, HPL or HPR are not used in an application, they should be left open or not connected.

**Typical Application (接下页)**
**11.2.3 Application Curves**

图 22 shows the excellent low-distortion performance of the PCM3070 in a system over the 20-Hz to 20-kHz audio spectrum.

图 23 shows the distortion performance of the PCM3070 in a system over the input amplitude range.



## 12 Power Supply Recommendations

To power up the device, a 3.3V system rail (1.9V to 3.6V) can be used. The IOVDD voltage can be in the range of 1.1V – 3.6V. Internal LDOs can generate the appropriate digital and analog core voltages when configured to do so. For maximum flexibility, the respective voltages can also be supplied externally, bypassing the built-in LDOs. To support high-output drive capabilities, the output stages of the output amplifiers can be driven from the analog core voltage or the 1.9...3.6V rail used for the LDO inputs (LDO\_in).

The AVDD and LDOIN power inputs are used to power the analog circuits including analog to digital converters, digital to analog converters, programmable gain amplifiers, headphone amplifiers, etc. The analog blocks in PCM3070 have high power supply rejection ratio, however it is recommended that these supplies be powered by well regulated power supplies like low dropout regulators (LDO) for optimal performance. When these power terminals are driven from a common power source, the current drawn from the source will depend upon blocks enabled inside the device. However as an example when all the internal blocks powered are enabled the source should be able to deliver 150mA of current.

The DVDD powers the digital core of PCM3070, including the miniDSP, the audio serial interface, control interfaces (SPI or I2C), clock generation and PLL. The DVDD power can be driven by high efficiency switching regulators or low drop out regulators. When the miniDSP\_A and miniDSP\_D are enabled in programmable mode and operated at peak frequencies, the supply source should be able to deliver approx 100mA of current. When the PRB modes are used instead of programmable miniDSP mode, then the peak current load on DVDD supply source could be approximately 20 mA.

The IOVDD powers the digital input and digital output buffers of PCM3070. The current consumption of this power depends on configuration of digital terminals as inputs or outputs. When the digital terminals are configured as outputs, the current consumption would depend on switching frequency of the signal and the load on the output terminal, which depends on board design and input capacitance of other devices connected to the signal.

Refer to [图 19](#) for recommendations on decoupling capacitors.

For more detailed information see the PCM3070 Application Reference Guide, [SLAU332](#).

## 13 Layout

### 13.1 Layout Guidelines

Each system design and PCB layout is unique. The layout should be carefully reviewed in the context of a specific PCB design. However, the following guidelines can optimize PCM3070 performance:

- Connect the thermal pad to ground.
- The decoupling capacitors for the power supplies should be placed close to the device terminals. [图 19](#) shows the recommended decoupling capacitors for the PCM3070.
- The PCM3070 internal voltage references must be filtered using external capacitors. Place the filter capacitors on REF near the device terminals for optimal performance.
- For analog differential audio signals, the signals should be routed differentially on the PCB for better noise immunity. Avoid crossing of digital and analog signals to avoid undesirable crosstalk.

### 13.2 Layout Example

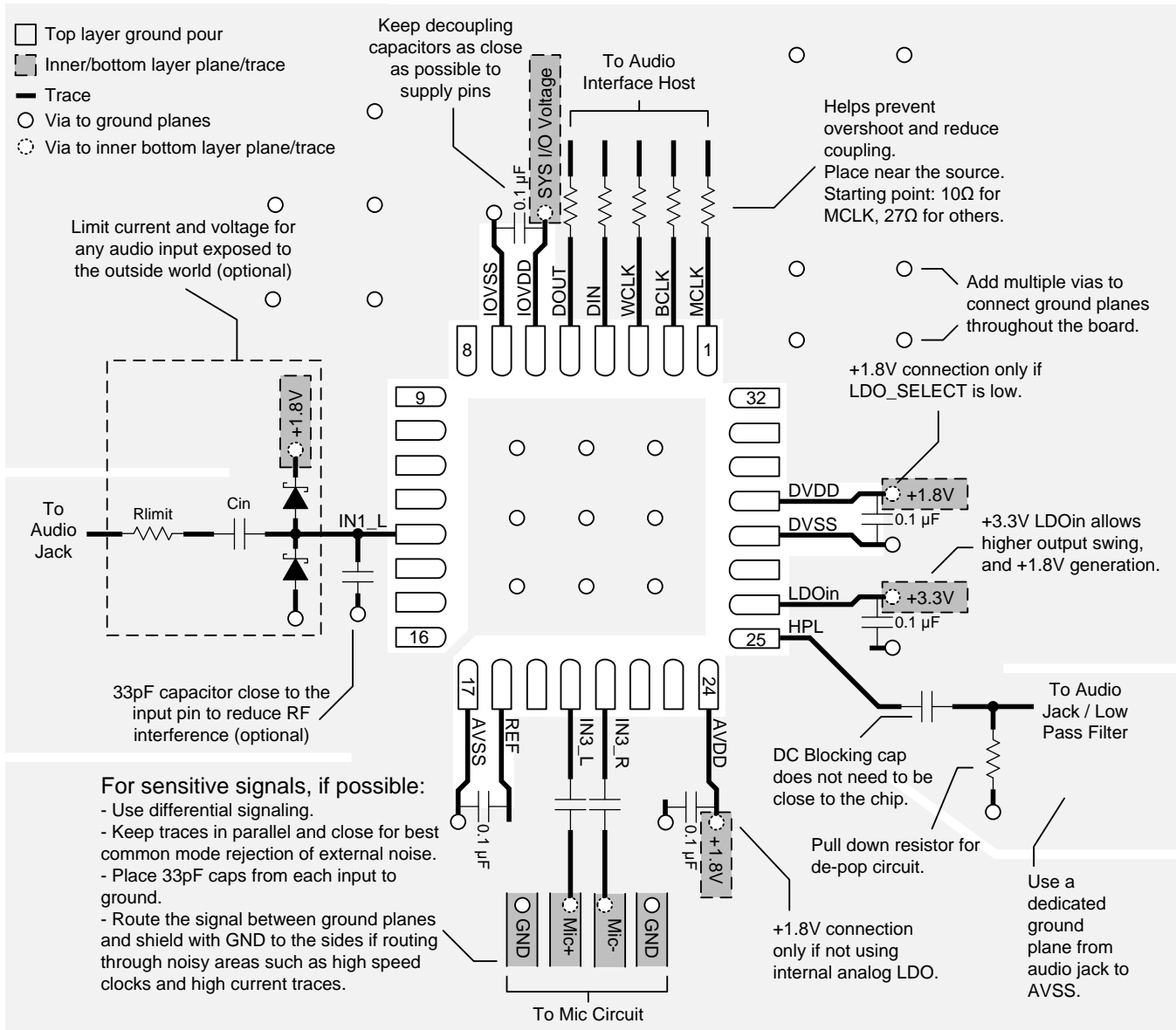


图 24. Layout

Example layout views can be found in the EVM User Guide:

- <http://www.ti.com/tool/PCM3070RHBEVM-K>



## 14 器件和文档支持

### 14.1 文档支持

#### 14.1.1 相关文档

《PCM3070 应用参考指南》，[SLAU332](#)。

### 14.2 商标

All trademarks are the property of their respective owners.

### 14.3 静电放电警告



这些装置包含有限的内置 ESD 保护。存储或装卸时，应将导线一起截短或将装置放置于导电泡棉中，以防止 MOS 门极遭受静电损伤。

### 14.4 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

## 15 机械封装和可订购信息

以下页中包括机械封装和可订购信息。这些信息是针对指定器件可提供的最新数据。这些数据会在无通知且不对本文档进行修订的情况下发生改变。欲获得该数据表的浏览器版本，请查阅左侧的导航栏。

**PACKAGING INFORMATION**

| Orderable Device | Status<br>(1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan<br>(2) | Lead finish/<br>Ball material<br>(6) | MSL Peak Temp<br>(3) | Op Temp (°C) | Device Marking<br>(4/5) | Samples                 |
|------------------|---------------|--------------|-----------------|------|-------------|-----------------|--------------------------------------|----------------------|--------------|-------------------------|-------------------------|
| PCM3070IRHBR     | ACTIVE        | VQFN         | RHB             | 32   | 3000        | RoHS & Green    | NIPDAU                               | Level-1-260C-UNLIM   | -40 to 85    | PCM3070<br>             | <a href="#">Samples</a> |
| PCM3070IRHBT     | ACTIVE        | VQFN         | RHB             | 32   | 250         | RoHS & Green    | NIPDAU                               | Level-1-260C-UNLIM   | -40 to 85    | PCM3070<br>             | <a href="#">Samples</a> |

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

| Device       | Package Type | Package Drawing | Pins | SPQ  | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|--------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| PCM3070IRHBR | VQFN         | RHB             | 32   | 3000 | 330.0              | 12.4               | 5.3     | 5.3     | 1.1     | 8.0     | 12.0   | Q2            |
| PCM3070IRHBT | VQFN         | RHB             | 32   | 250  | 180.0              | 12.4               | 5.3     | 5.3     | 1.1     | 8.0     | 12.0   | Q2            |

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

| Device       | Package Type | Package Drawing | Pins | SPQ  | Length (mm) | Width (mm) | Height (mm) |
|--------------|--------------|-----------------|------|------|-------------|------------|-------------|
| PCM3070IRHBR | VQFN         | RHB             | 32   | 3000 | 346.0       | 346.0      | 33.0        |
| PCM3070IRHBT | VQFN         | RHB             | 32   | 250  | 210.0       | 185.0      | 35.0        |

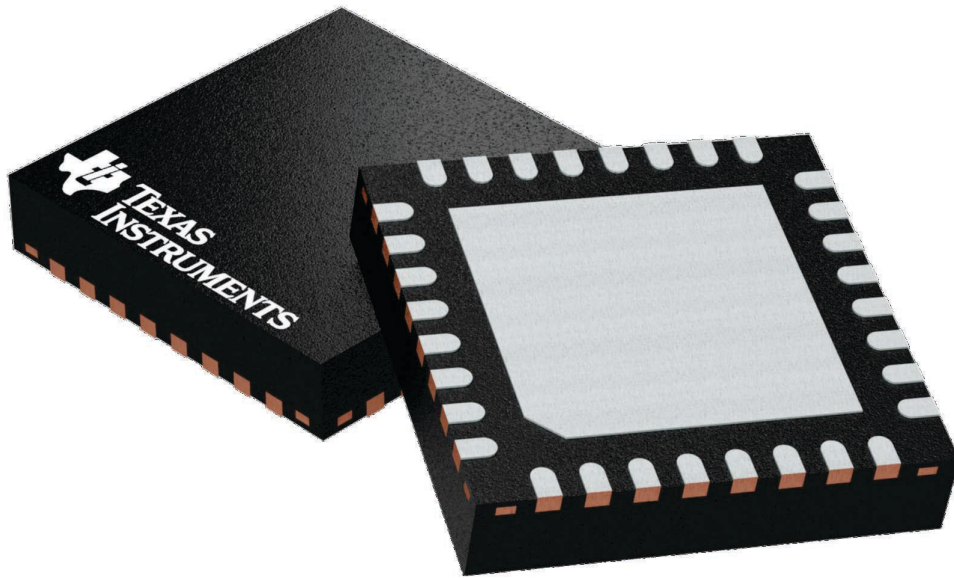
## GENERIC PACKAGE VIEW

**RHB 32**

**VQFN - 1 mm max height**

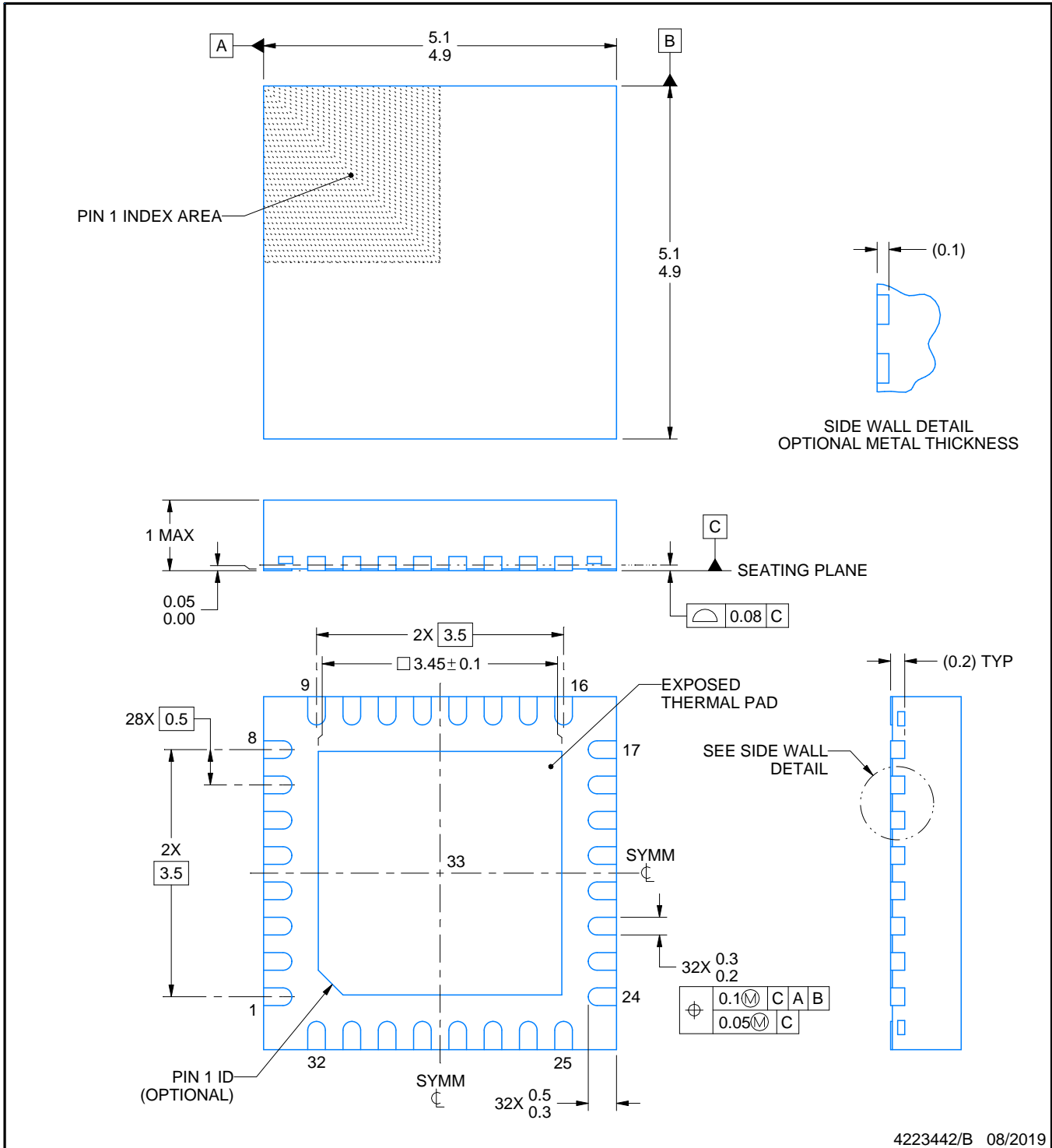
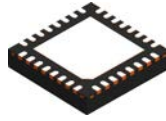
5 x 5, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD



Images above are just a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.

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NOTES:

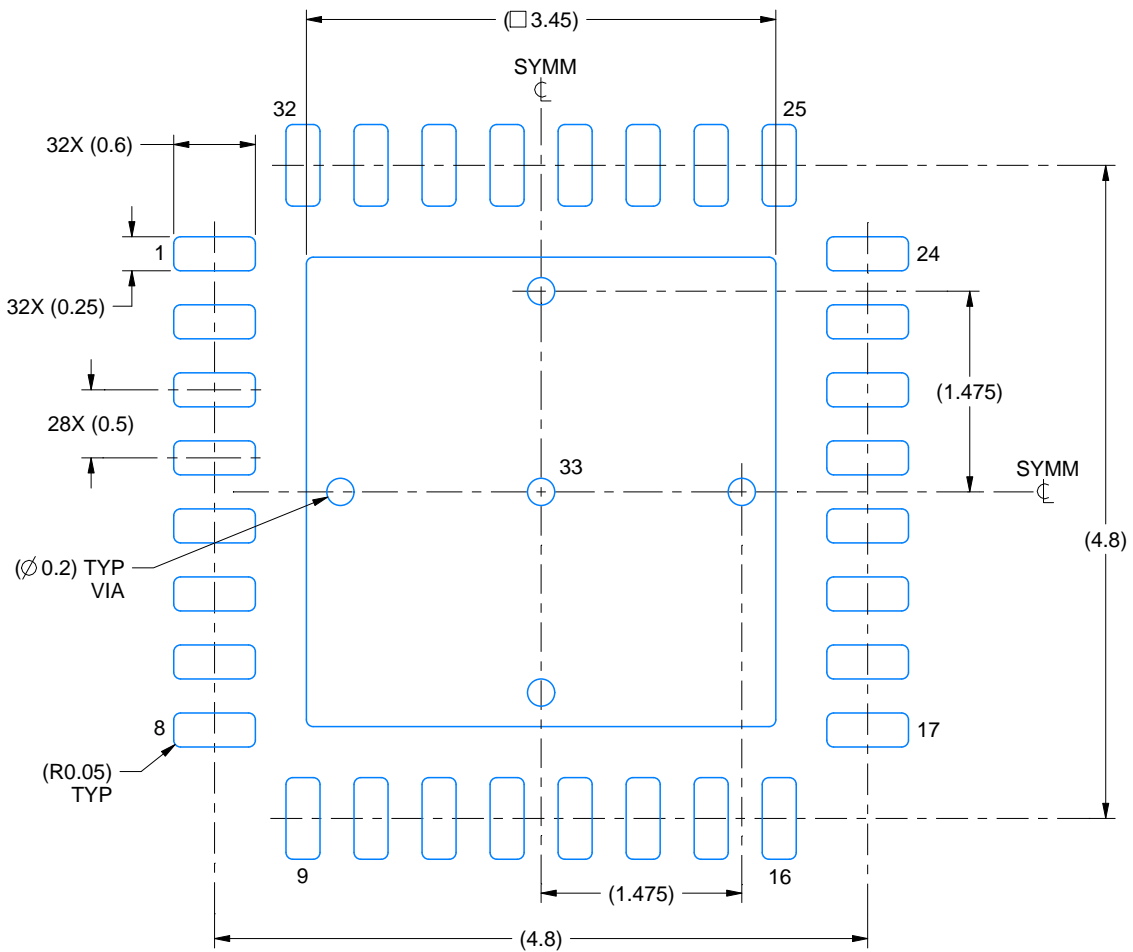
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

# EXAMPLE BOARD LAYOUT

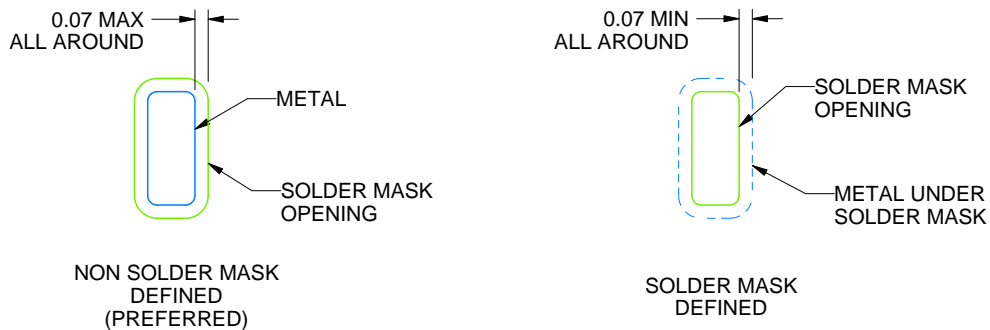
RHB0032E

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



LAND PATTERN EXAMPLE  
SCALE:18X



SOLDER MASK DETAILS

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NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 ([www.ti.com/lit/slua271](http://www.ti.com/lit/slua271)).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

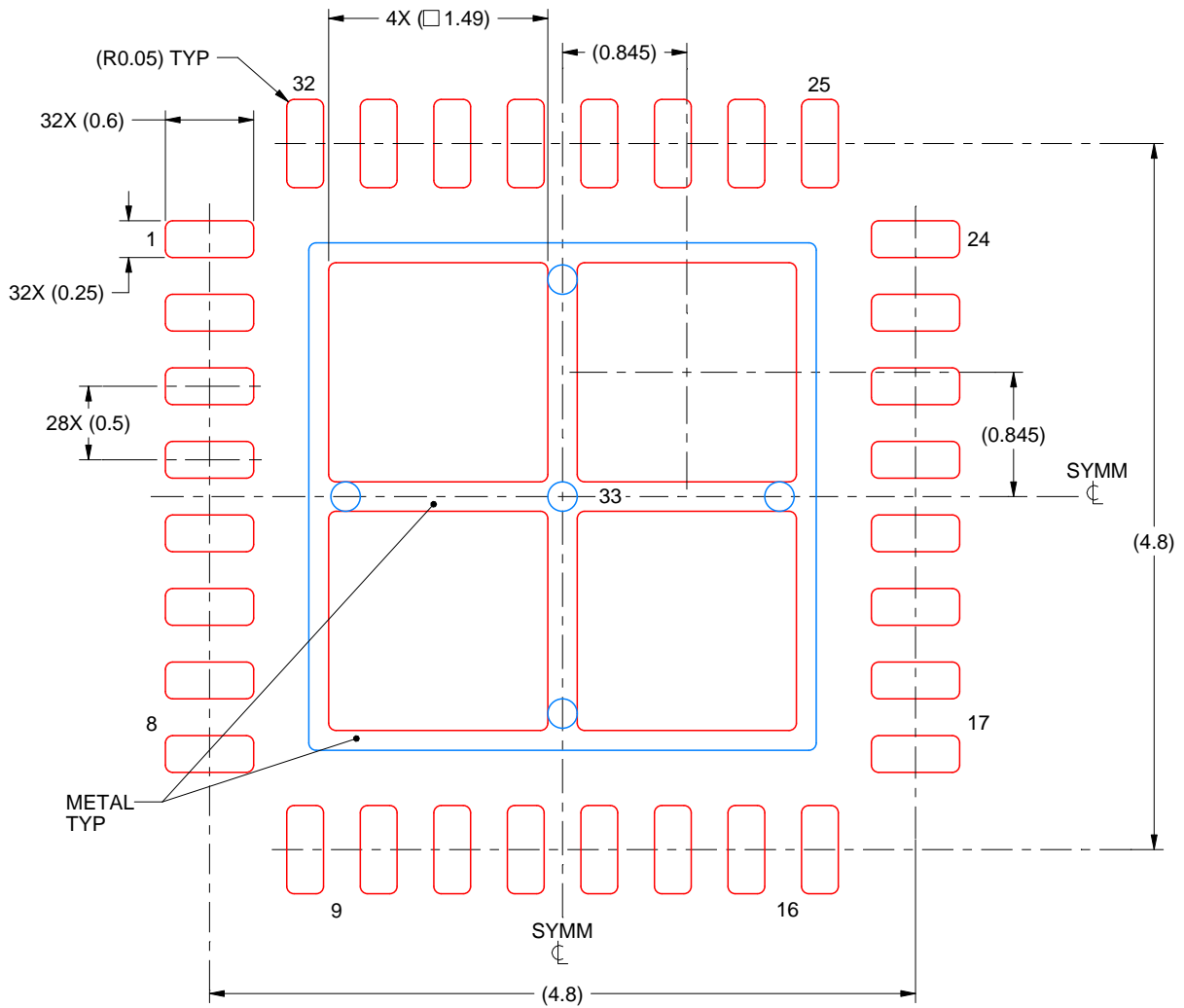


# EXAMPLE STENCIL DESIGN

RHB0032E

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



**SOLDER PASTE EXAMPLE**  
 BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 33:  
 75% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE  
 SCALE:20X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

## 重要声明和免责声明

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