

2V_{RMS} DirectPath™, 具有 32 位, 384kHz 脉冲编码调制 (PCM) 接口的 112, 106, 100dB 音频立体声数模转换器 (DAC)

 查询样品: [PCM5100A-Q1](#), [PCM5101A-Q1](#), [PCM5102A-Q1](#)

特性

- 符合汽车应用要求
- 具有符合 **AEC-Q100** 的下列结果:
 - 器件温度 1 级: **-40°C 至 125°C** 的环境运行温度范围
 - 器件人体模型 (HBM) 静电放电 (ESD) 分类等级 **H2**
 - 器件充电器件模型 (CDM) ESD 分类等级 **C4B**
- 市场领先的低带外噪声
- 可选数字滤波器延迟与性能
- 无需隔离直流电流的电容器
- 集成的负电荷泵
- 用于采样率变化或者时钟暂停的内部无爆音控制
- 智能静噪系统: 针对带有无爆音操作的 **120dB** 静噪信噪比 (SNR) 的软上升或下降斜坡和模拟静噪 (AMUTE)
- 具有对于内部生成 **SCK** 的 **BCK** 基准的集成高性能音频锁相环路 (PLL)
- 支持 **1.8V** 数字输入接口
- 小型 **20** 引脚薄型小外形尺寸 (TSSOP) 封装
- 接受 **16, 24** 和 **32** 位音频数据
- PCM** 数据格式: **I²S**, 左对齐

- 当 **LRCK** 和 **BCK** 被置为无效时, 自动进入省电模式
- 1.8V** 或 **3.3V** 故障安全低压互补金属氧化物半导体 (LVCMOS) 数字输入
- 硬件配置
- 单电源运行:
 - 3.3V** 模拟, **1.8V** 或 **3.3V** 数字
- 集成型加电复位

应用范围

- 汽车应用
- 车用信息娱乐
- 音频视频 (A/V) 接收器
- 数字多用途光盘 (DVD), 蓝光光盘 (BD) 播放器
- 高清电视 (HDTV) 接收器
- 需要 **2V_{RMS}** 音频输出的应用

说明

PCM510xA-Q1 是单片互补金属氧化物半导体 (CMOS) 集成电路系列产品, 此产品包括一个立体声数模转换器和小型薄型小外形尺寸 (TSSOP) 封装内的附加支持电路。PCM510xA-Q1 使用 TI 的高级分段数模转换器 (DAC) 架构的新一代产品来实现出色的动态性能并提升了对于时钟抖动的耐受度。

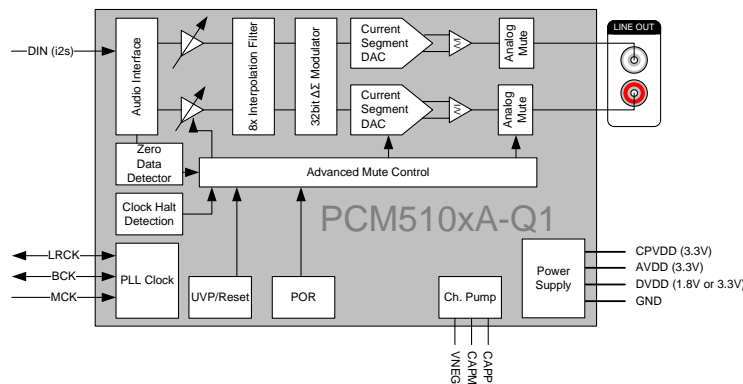


图 1. PCM510xA-Q1 功能方框图



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This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

Typical Performance (3.3-V Power Supply)

Parameter	PCM5102A-Q1	PCM5101A-Q1	PCM5100A-Q1
SNR	112	106	100 dB
Dynamic Range	112	106	100 dB
Total Harmonic Distortion + Noise (THD+N) at -1 dBFS	-93	-92	-90 dB
Full Scale Output	2.1 V _{RMS} (GND center)		
Normal 8 × Oversampling Digital Filter Latency:	20 t _S		
Low Latency 8 × Oversampling Digital Filter Latency:	3.5 t _S		
Sampling Frequency:	8 kHz to 384 kHz		
System Clock Multiples (f _{SCK}):	64, 128, 192, 256, 384, 512, 768, 1024, 1152, 1536, 2048, 3072; up to 50 MHz		

DESCRIPTION (CONTINUED)

The PCM510xA-Q1 provides 2.1-V_{RMS} ground centered outputs, allowing designers to eliminate DC blocking capacitors on the output, as well as external muting circuits traditionally associated with single supply line drivers.

The integrated line driver surpasses all other charge-pump based line drivers by supporting loads down to 1 kΩ. By supporting loads down to 1 kΩ, the PCM510xA-Q1 can essentially drive up to 10 products in parallel. For instance, liquid crystal display television (LCD TV), DVD-R, A/V Receivers, and so forth.

The integrated PLL on the device removes the requirement for a system clock (commonly known as master clock), allowing a 3-wire I²S connection and reducing system electromagnetic interference (EMI).

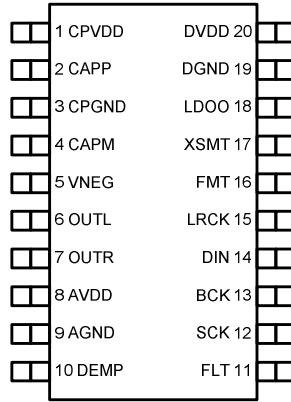
Intelligent clock error and PowerSense undervoltage protection utilizes a two level mute system for pop-free performance. Upon clock error or system power failure, the device digitally attenuates the data (or last known good data), then mutes the analog circuit

Compared with existing DAC technology, the PCM510xA-Q1 family offers up to 20-dB lower out-of-band noise, reducing EMI and aliasing in downstream amplifiers and analog-to-digital converters (ADCs) from traditional 100-kHz OBN measurements all the way to 3 MHz.

The PCM510xA-Q1 accepts industry-standard audio data formats with 16- to 32-bit data. Sample rates up to 384 kHz are supported.

Table 1. Differences Between PCM510xA-Q1 Devices

T _A	Orderable Part Number	Dynamic Range	SNR	THD	TOP-SIDE MARKING
-40°C to 125°C	PCM5100AQPWRQ1	100 dB	100 dB	-90 dB	P5100AQ1
	PCM5101AQPWRQ1	106 dB	106 dB	-92 dB	Preview
	PCM5102AQPWRQ1	112 dB	112 dB	-93 dB	Preview

DEVICE INFORMATION
PIN FUNCTIONS, PCM510xA-Q1
**PCM510xA-Q1
(Top View)**

PIN FUNCTIONS, PCM510xA-Q1

PIN		I/O	DESCRIPTION
NAME	NO.		
CPVDD	1	—	Charge pump power supply, 3.3 V
CAPP	2	O	Charge pump flying capacitor terminal for positive rail
CPGND	3	—	Charge pump ground
CAPM	4	O	Charge pump flying capacitor terminal for negative rail
VNEG	5	O	Negative charge pump rail terminal for decoupling, –3.3 V
OUTL	6	O	Analog output from DAC left channel
OUTR	7	O	Analog output from DAC right channel
AVDD	8	—	Analog power supply, 3.3 V
AGND	9	—	Analog ground
DEMP	10	I	De-emphasis control for 44.1-kHz sampling rate ⁽¹⁾ : Off (Low), On (High)
FLT	11	I	Filter select: Normal latency (Low), Low latency (High)
SCK	12	I	System clock input ⁽¹⁾
BCK	13	I	Audio data bit clock input ⁽¹⁾
DIN	14	I	Audio data input ⁽¹⁾
LRCK	15	I	Audio data word clock input ⁽¹⁾
FMT	16	I	Audio format selection: I ² S (Low), Left justified (High)
XSMT	17	I	Soft mute control ⁽¹⁾ : Soft mute (Low), soft un-mute (High)
LDOO	18	—	Internal logic supply rail terminal for decoupling, or external 1.8-V supply terminal
DGND	19	—	Digital ground
DVDD	20	—	Digital power supply, 1.8 V or 3.3 V

(1) Failsafe LVCMOS Schmitt trigger input

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
Supply Voltage	AVDD, CPVDD, DVDD	-0.3	3.9	V
	LDOO with DVDD at 1.8 V (See Figure 40 and Figure 42)	-0.3	2.25	
Digital Input Voltage	DVDD at 1.8 V	-0.3	2.25	
	DVDD at 3.3 V	-0.3	3.9	
Analog Input Voltage		-0.3	3.9	
Operating Temperature Range		-25	125	°C
Storage Temperature Range		-65	150	
Electrostatic Discharge (ESD) Rating	Human Body Model (HBM) AEC-Q100 Classification Level H2		2	kV
	Charged Device Model (CDM) AEC-Q100 Classification Level C4B		750	V

THERMAL CHARACTERISTICS

over operating free-air temperature range (unless otherwise noted)

THERMAL METRIC ⁽¹⁾		PCM5100A-Q1	UNIT
		(20 PINS)	
θ_{JA}	Junction-to-ambient thermal resistance	91.2	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	1	
Ψ_{JB}	Junction-to-board characterization parameter	41.5	
$\theta_{JC(top)}$	Junction-to-case(top) thermal resistance	25.3	
θ_{JB}	Junction-to-board thermal resistance	42	

(1) For more information about traditional and new thermal metrics, see the IC Package Thermal Metrics application report, [SPRA953](#).

ELECTRICAL CHARACTERISTICS

All specifications at $T_A = -40$ to 125°C , $AV_{DD} = CPV_{DD} = DV_{DD} = 3.3$ V, $f_S = 48$ kHz, system clock = $512 f_S$ and 24-bit data unless otherwise noted.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Resolution		16	24	32	Bits
Data Format (PCM Mode)					
Audio data interface format		I ² S, left justified			
Audio data bit length		16, 24, 32-bit acceptable			
Audio data format		MSB First, 2s Complement			
$f_S^{(1)}$	Sampling frequency	8		384	kHz
	System clock frequency	64, 128, 192, 256, 384, 512, 768, 1024, 1152, 1536, 2048, or 3072 f_{SCK} , up to 50 MHz			
Digital Input/Output					
Logic Family: 3.3-V LVCMOS compatible					
V_{IH}	Input logic level	$0.7 \times DV_{DD}$			V
V_{IL}		$0.3 \times DV_{DD}$			
I_{IH}	Input logic current	$V_{IN} = V_{DD}$	10		μA
I_{IL}		$V_{IN} = 0$ V	-10		
V_{OH}	Output logic level	$I_{OH} = -4$ mA	$0.8 \times DV_{DD}$		V
V_{OL}		$I_{OL} = 4$ mA	$0.22 \times DV_{DD}$		
Logic Family 1.8-V LVCMOS compatible					
V_{IH}	Input logic level	$0.7 \times DV_{DD}$			V
V_{IL}		$0.3 \times DV_{DD}$			

(1) One sample time is defined as the reciprocal of the sampling frequency. $1 t_S = 1 / f_S$

ELECTRICAL CHARACTERISTICS (continued)

All specifications at $T_A = -40$ to 125°C , $AV_{DD} = CPV_{DD} = DV_{DD} = 3.3\text{ V}$, $f_S = 48\text{ kHz}$, system clock = $512 f_S$ and 24-bit data unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{IH}	Input logic current	$V_{IN} = V_{DD}$			10	μA
I_{IL}		$V_{IN} = 0\text{ V}$			-10	

ELECTRICAL CHARACTERISTICS (continued)

All specifications at $T_A = -40$ to 125°C , $AV_{DD} = CPV_{DD} = DV_{DD} = 3.3\text{ V}$, $f_S = 48\text{ kHz}$, system clock = $512 f_S$ and 24-bit data unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH}	Output logic level	$I_{OH} = -2\text{ mA}$	$0.8 \times DV_{DD}$		$0.22 \times DV_{DD}$	V
V_{OL}		$I_{OL} = 2\text{ mA}$				
Dynamic Performance (PCM Mode)⁽²⁾⁽³⁾⁽⁴⁾						
THD+N at $-1\text{ dBFS}^{(3)}$	$f_S = 48\text{ kHz}$		-93, -92, -90	-83, -82, -80	dB	
	$f_S = 96\text{ kHz}$		-93, -92, -90			
	$f_S = 192\text{ kHz}$		-93, -92, -90			
Dynamic range ⁽³⁾	EIAJ, A-weighted, $f_S = 48\text{ kHz}$		106, 100, 95	112, 106, 100	dB	
	EIAJ, A-weighted, $f_S = 96\text{ kHz}$			112, 106, 100		
	EIAJ, A-weighted, $f_S = 192\text{ kHz}$			112, 106, 100		
SNR Signal-to-noise ratio ⁽³⁾	EIAJ, A-weighted, $f_S = 48\text{ kHz}$			112, 106, 100	dB	
	EIAJ, A-weighted, $f_S = 96\text{ kHz}$			112, 106, 100		
	EIAJ, A-weighted, $f_S = 192\text{ kHz}$			112, 106, 100		
Signal-to-noise ratio with AMUTE ⁽³⁾⁽⁵⁾	EIAJ, A-weighted, $f_S = 48\text{ kHz}$		113	123	dB	
	EIAJ, A-weighted, $f_S = 96\text{ kHz}$			123		
	EIAJ, A-weighted, $f_S = 192\text{ kHz}$			123		
Channel separation	$f_S = 48\text{ kHz}$		100, 95, 90	109, 103, 97	dB	
	$f_S = 96\text{ kHz}$			109, 103, 97		
	$f_S = 192\text{ kHz}$			109, 103, 97		
Analog Output						
Output voltage				2.1		V_{RMS}
Gain error			-7	± 2	7	% of FSR
Gain mismatch, channel-to-channel			-7	± 2	7	% of FSR
Bipolar zero (BPZ) error		At BPZ	-5	± 1	5	mV
Load impedance			1			k Ω
Filter Characteristics–1: Normal						
Pass band					$0.45 f_S$	
Stop band			$0.55 f_S$			
Stop band attenuation			-60			dB
Pass-band ripple					± 0.02	
Delay time				$20 t_S$		s
Filter Characteristics–2: Low Latency						
Pass band					$0.47 f_S$	
Stop band			$0.55 f_S$			
Stop band attenuation			-52			dB
Pass-band ripple					± 0.0001	
Delay time				$3.5 t_S$		s

(2) Filter condition: THD+N: 20-Hz HPF, 20-kHz AES17 LPF. Dynamic range: 20-Hz HPF, 20-kHz AES17 LPF. A-weighted SNR: 20-Hz HPF, 20-kHz AES17 LPF. A-weighted Channel Separation: 20-Hz HPF, 20-kHz AES17 LPF. Analog performance specifications are measured using the System Two Cascade™ audio measurement system by Audio Precision™ in the record management system (RMS) mode.

(3) Output load is 10 k Ω , with 470- Ω output resistor and a 2.2-nF shunt capacitor (see recommended output filter).

(4) Values shown for three devices PCM5102A-Q1, PCM5101A-Q1, PCM5100A-Q1, respectively.

(5) Assert XSMT or both left-channel and right-channel PCM data are BPZ.

ELECTRICAL CHARACTERISTICS (continued)

All specifications at $T_A = -40$ to 125°C , $AV_{DD} = CPV_{DD} = DV_{DD} = 3.3\text{ V}$, $f_S = 48\text{ kHz}$, system clock = $512 f_S$ and 24-bit data unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Power Supply Requirements						
DV_{DD}	Digital supply voltage	Target $DV_{DD} = 1.8\text{ V}$	1.65	1.8	1.95	VDC
DV_{DD}	Digital supply voltage	Target $DV_{DD} = 3.3\text{ V}$	3	3.3	3.6	VDC
AV_{DD}	Analog supply voltage		3	3.3	3.6	
CPV_{DD}	Charge-pump supply voltage		3	3.3	3.6	
I_{DD}	DV_{DD} supply current at $1.8\text{ V}^{(6)}$	$f_S = 48\text{ kHz}$		7		
		$f_S = 96\text{ kHz}$		8		
		$f_S = 192\text{ kHz}$		9		
I_{DD}	DV_{DD} supply current at $1.8\text{ V}^{(7)}$	$f_S = 48\text{ kHz}$		7		mA
		$f_S = 96\text{ kHz}$		8		
		$f_S = 192\text{ kHz}$		9		
I_{DD}	DV_{DD} supply current at $1.8\text{ V}^{(8)}$			0.3		mA
I_{DD}	DV_{DD} supply current at $3.3\text{ V}^{(6)}$	$f_S = 48\text{ kHz}$		7	12	mA
		$f_S = 96\text{ kHz}$		8		
		$f_S = 192\text{ kHz}$		9		
I_{DD}	DV_{DD} supply current at $3.3\text{ V}^{(7)}$	$f_S = 48\text{ kHz}$		8	13	mA
		$f_S = 96\text{ kHz}$		9		
		$f_S = 192\text{ kHz}$		10		
I_{DD}	DV_{DD} supply current at $3.3\text{ V}^{(8)}$			0.5	0.8	mA
I_{CC}	AV_{DD} / CPV_{DD} Supply Current ⁽⁶⁾	$f_S = 48\text{ kHz}$		11	16	mA
		$f_S = 96\text{ kHz}$		11		
		$f_S = 192\text{ kHz}$		11		
I_{CC}	AV_{DD} / CPV_{DD} Supply Current ⁽⁷⁾	$f_S = 48\text{ kHz}$		22	32	mA
		$f_S = 96\text{ kHz}$		22		
		$f_S = 192\text{ kHz}$		22		
I_{CC}	AV_{DD} / CPV_{DD} Supply Current ⁽⁸⁾	$f_S = \text{n/a}$		0.2	0.4	mA
	Power Dissipation, $DV_{DD} = 1.8\text{ V}^{(6)}$	$f_S = 48\text{ kHz}$		48.9	185	mW
		$f_S = 96\text{ kHz}$		50.7		
		$f_S = 192\text{ kHz}$		52.5		
	Power Dissipation, $DV_{DD} = 1.8\text{ V}^{(7)}$	$f_S = 48\text{ kHz}$		85.2	187	mW
		$f_S = 96\text{ kHz}$		87		
		$f_S = 192\text{ kHz}$		88.8		
	Power Dissipation, $DV_{DD} = 1.8\text{ V}^{(8)}$	$f_S = \text{n/a}$ (power down mode)		1.2		mW
	Power Dissipation, $DV_{DD} = 3.3\text{ V}^{(6)}$	$f_S = 48\text{ kHz}$		59.4	92.4	mW
		$f_S = 96\text{ kHz}$		62.7		
		$f_S = 192\text{ kHz}$		66		
	Power Dissipation, $DV_{DD} = 3.3\text{ V}^{(7)}$	$f_S = 48\text{ kHz}$		99	148.5	mW
		$f_S = 96\text{ kHz}$		102.3		
		$f_S = 192\text{ kHz}$		105.6		
	Power Dissipation, $DV_{DD} = 3.3\text{ V}^{(8)}$	$f_S = \text{n/a}$ (power down mode)		2.3	4	mW

(6) Input is BPZ data.

(7) Input is 1 kHz - 1 dBFS data

(8) Power down mode

TYPICAL CHARACTERISTICS

All specifications at $T_A = 25^\circ\text{C}$, $AV_{DD} = CPV_{DD} = DV_{DD} = 3.3\text{ V}$, $f_S = 48\text{ kHz}$, system clock = $512 f_S$ and 24-bit data unless otherwise noted.

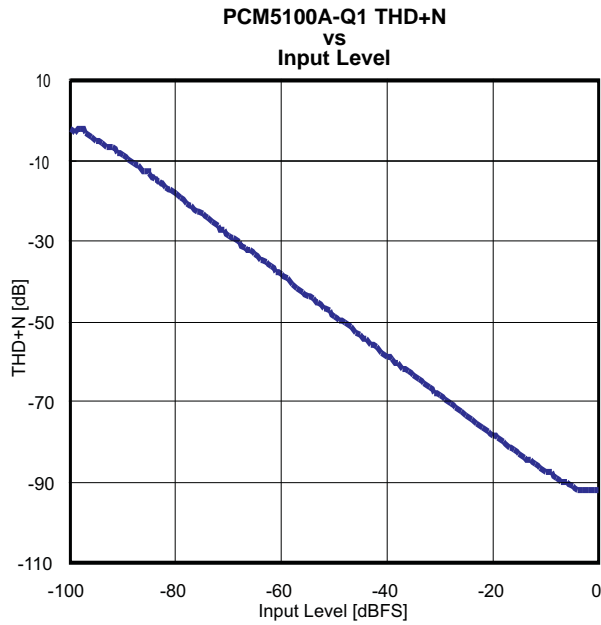


Figure 2.

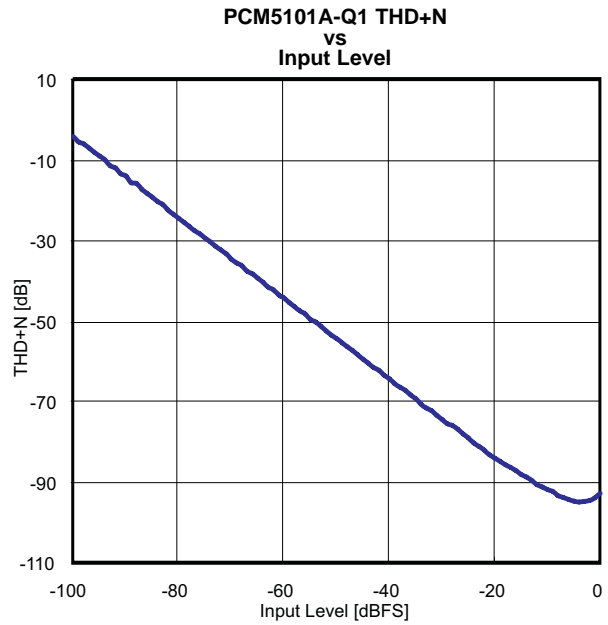


Figure 3.

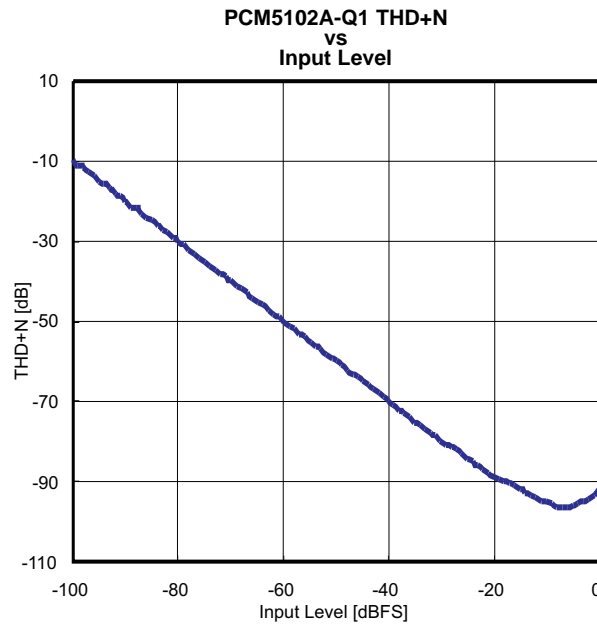


Figure 4.

TYPICAL CHARACTERISTICS (continued)

All specifications at $T_A = 25^\circ\text{C}$, $AV_{DD} = CPV_{DD} = DV_{DD} = 3.3\text{ V}$, $f_S = 48\text{ kHz}$, system clock = $512 f_S$ and 24-bit data unless otherwise noted.

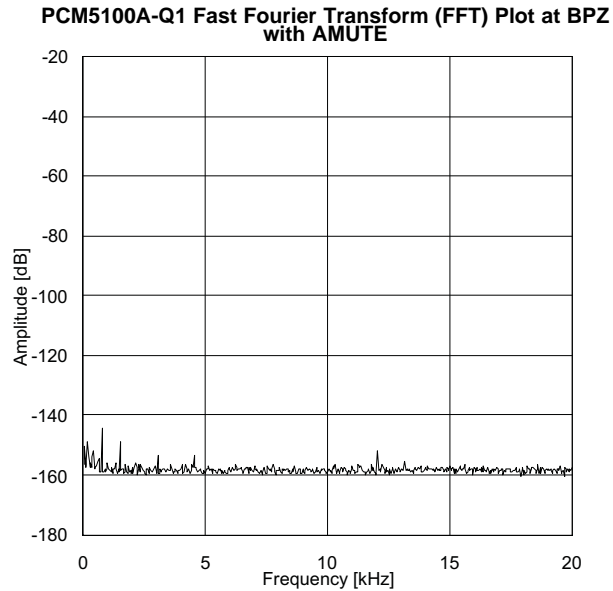


Figure 5.

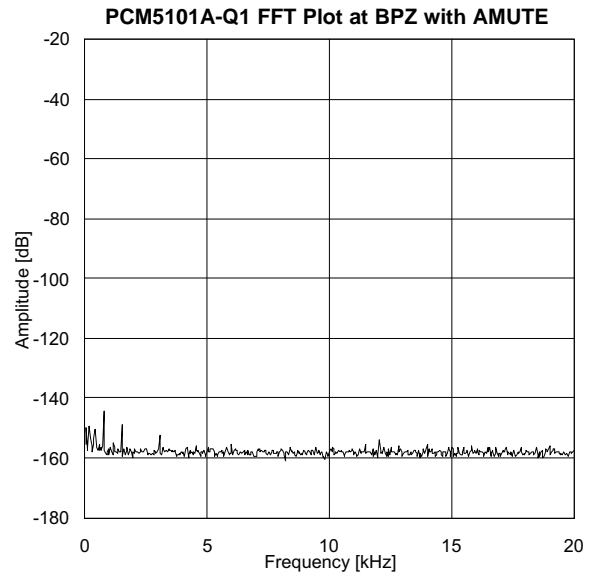


Figure 6.

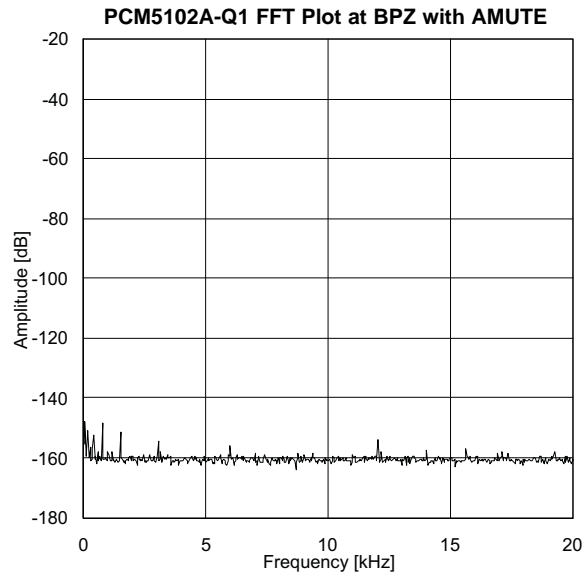


Figure 7.

TYPICAL CHARACTERISTICS (continued)

All specifications at $T_A = 25^\circ\text{C}$, $AV_{DD} = CPV_{DD} = DV_{DD} = 3.3\text{ V}$, $f_S = 48\text{ kHz}$, system clock = $512 f_S$ and 24-bit data unless otherwise noted.

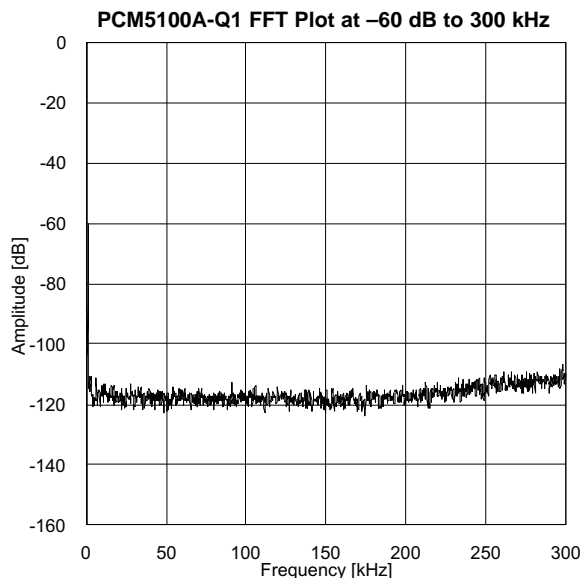


Figure 8.

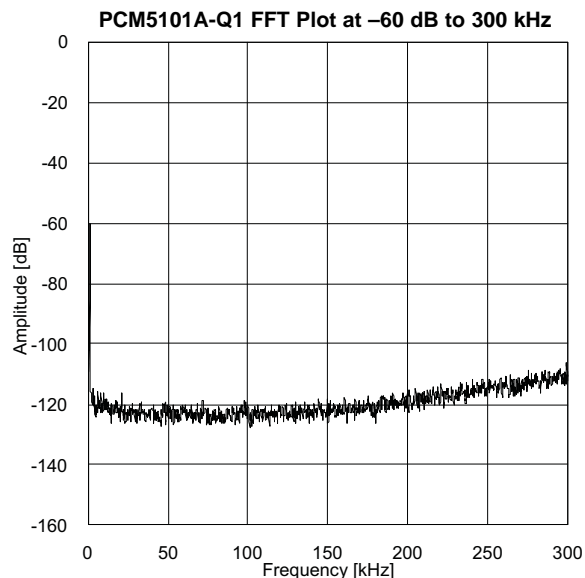


Figure 9.

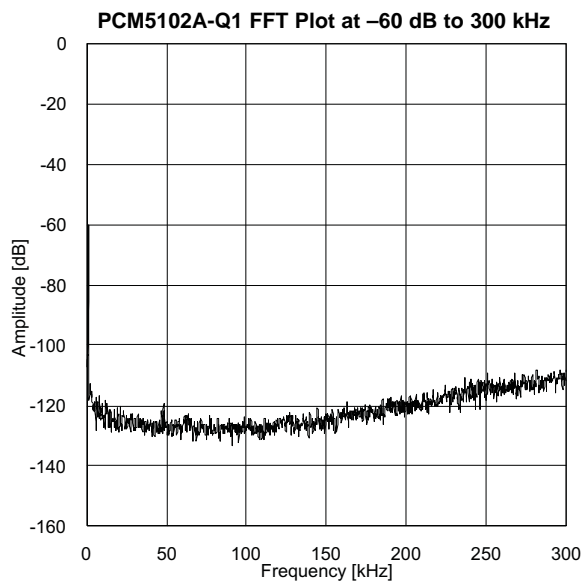


Figure 10.

APPLICATION INFORMATION

Reset and System Clock Functions

Power-On Reset Function

Power-On Reset, Digital Power Supply Voltage 3.3-V Supply

The PCM510xA-Q1 includes a power-on reset function shown in Figure 11. With supply voltage greater than 2.8 V, the power-on reset function is enabled. After the initialization period, the PCM510xA-Q1 is set to its default reset state.

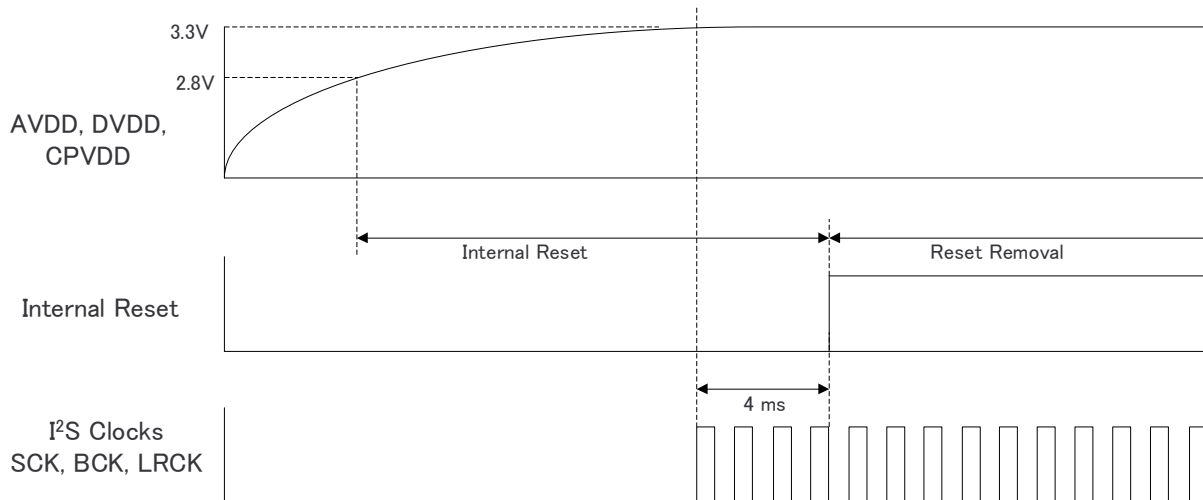


Figure 11. Power-On Reset Timing, $DV_{DD} = 3.3\text{ V}$

Power-On Reset, Digital Power Supply Voltage 1.8-V Supply

The PCM510xA-Q1 includes a power-on reset function shown in Figure 12 operating at $DV_{DD} = 1.8\text{ V}$. With analog power supply voltage greater than approximately 2.8 V, charge-pump power supply voltage greater than approximately 2.8 V, and digital power supply voltage greater than approximately 1.5 V, the power-on reset function is enabled. After the initialization period, the PCM510xA-Q1 is set to its default reset state.

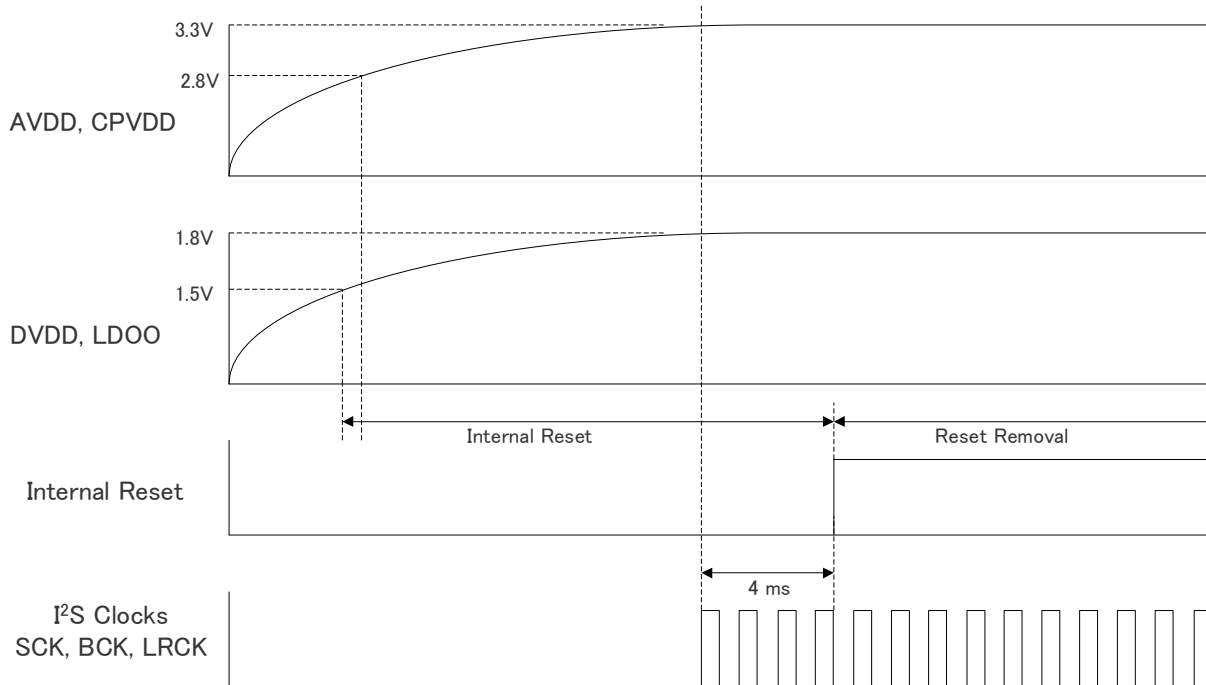


Figure 12. Power-On Reset Timing, $DV_{DD} = 1.8\text{ V}$

System Clock Input

The PCM510xA-Q1 requires a system clock to operate the digital interpolation filters and advanced segment DAC modulators. The system clock is applied at the SCK input (pin 12) and supports up to 50 MHz. The PCM510xA-Q1 system-clock detection circuit automatically senses the system-clock frequency. Common audio sampling frequencies in the bands of 8 kHz, 16 kHz, (32 kHz – 44.1 kHz – 48 kHz), (88.2 kHz – 96 kHz), (176.4 kHz – 192 kHz), and 384 kHz with $\pm 4\%$ tolerance are supported. Values in the parentheses are grouped when detected, for example, 88.2 kHz and 96 kHz are detected as double rate, 32 kHz, 44.1 kHz and 48 kHz is detected as a single rate.

The sampling frequency detector sets the clock for the digital filter, delta sigma modulator (DSM) and the negative charge pump (NCP) automatically. Table 2 shows examples of system clock frequencies for common audio sampling rates.

SCK rates that are not common to standard audio clocks, between 1 MHz and 50 MHz, are only supported in software mode, available only in the PCM512x and PCM514x devices, by configuring various PLL and clock-divider registers. This programmability allows the device to become a clock master and drive the host serial port with LRCK and BCK, from a non-audio related clock (for example, using 12 MHz to generate 44.1 kHz (LRCK) and 2.8224 MHz (BCK)).

Figure 13 shows the timing requirements for the system clock input. For optimal performance, use a clock source with low phase jitter and noise.

Table 2. System Master Clock Inputs for Audio Related Clocks

Sampling Frequency	System Clock Frequency (f_{SCK}) (MHz)											
	64 f_S	128 f_S	192 f_S	256 f_S	384 f_S	512 f_S	768 f_S	1024 f_S	1152 f_S	1536 f_S	2048 f_S	3072 f_S
8 kHz	– ⁽¹⁾	1.0240 ⁽²⁾	1.5360 ⁽²⁾	2.0480	3.0720	4.0960	6.1440	8.1920	9.2160	12.2880	16.3840	24.5760
16 kHz	– ⁽¹⁾	2.0480 ⁽²⁾	3.0720 ⁽²⁾	4.0960	6.1440	8.1920	12.2880	16.3840	18.4320	24.5760	36.8640	49.1520
32 kHz	– ⁽¹⁾	4.0960 ⁽²⁾	6.1440 ⁽²⁾	8.1920	12.2880	16.3840	24.5760	32.7680	36.8640	49.1520	– ⁽¹⁾	– ⁽¹⁾
44.1 kHz	– ⁽¹⁾	5.6488 ⁽²⁾	8.4672 ⁽²⁾	11.2896	16.9344	22.5792	33.8688	45.1584	– ⁽¹⁾	– ⁽¹⁾	– ⁽¹⁾	– ⁽¹⁾
48 kHz	– ⁽¹⁾	6.1440 ⁽²⁾	9.2160 ⁽²⁾	12.2880	18.4320	24.5760	36.8640	49.1520	– ⁽¹⁾	– ⁽¹⁾	– ⁽¹⁾	– ⁽¹⁾
88.2 kHz	– ⁽¹⁾	11.2896 ⁽²⁾	16.9344	22.5792	33.8688	45.1584	– ⁽¹⁾	– ⁽¹⁾	– ⁽¹⁾	– ⁽¹⁾	– ⁽¹⁾	– ⁽¹⁾
96 kHz	– ⁽¹⁾	12.2880 ⁽²⁾	18.4320	24.5760	36.8640	49.1520	– ⁽¹⁾	– ⁽¹⁾	– ⁽¹⁾	– ⁽¹⁾	– ⁽¹⁾	– ⁽¹⁾
176.4 kHz	– ⁽¹⁾	22.5792	33.8688	45.1584	– ⁽¹⁾	– ⁽¹⁾	– ⁽¹⁾	– ⁽¹⁾	– ⁽¹⁾	– ⁽¹⁾	– ⁽¹⁾	– ⁽¹⁾
192 kHz	– ⁽¹⁾	24.5760	36.8640	49.1520	– ⁽¹⁾	– ⁽¹⁾	– ⁽¹⁾	– ⁽¹⁾	– ⁽¹⁾	– ⁽¹⁾	– ⁽¹⁾	– ⁽¹⁾
384 kHz	24.5760	49.1520	– ⁽¹⁾	– ⁽¹⁾	– ⁽¹⁾	– ⁽¹⁾	– ⁽¹⁾	– ⁽¹⁾	– ⁽¹⁾	– ⁽¹⁾	– ⁽¹⁾	– ⁽¹⁾

(1) This system clock rate is not supported for the given sampling frequency.

(2) This system clock rate is supported by PLL mode.

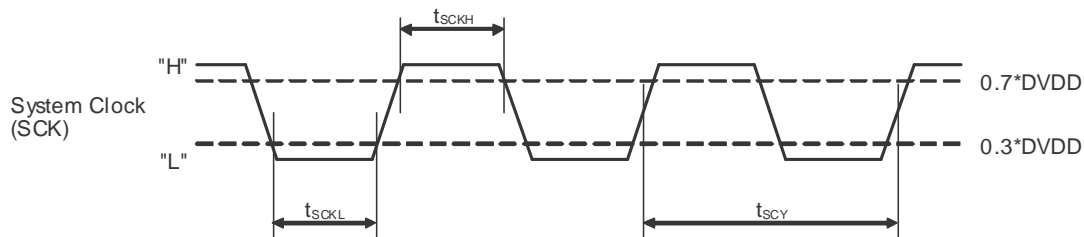


Figure 13. Timing Requirements for SCK Input

Table 3. Timing Requirements for SCK Input

	Parameters	Min	Max	Unit
t_{SCY}	System clock pulse cycle time	20	1000	ns
t_{SCKH}	System clock pulse width, High	$DV_{DD} = 1.8\text{ V}$	8	ns
		$DV_{DD} = 3.3\text{ V}$	9	
t_{SCKL}	System clock pulse width, Low	$DV_{DD} = 1.8\text{ V}$	8	ns
		$DV_{DD} = 3.3\text{ V}$	9	

System Clock PLL Mode

The system clock PLL mode allows designers to use a simple 3-wire I²S audio source when driving the output. The 3-wire source reduces the need for a high frequency SCK, making printed circuit board (PCB) layout easier, and reduces high frequency EMI.

The device starts up requiring an external SCK input, but if BCK and LRCK start correctly while SCK remains at ground level for 16 successive LRCK periods, then the internal PLL starts, automatically generating an internal SCK from the BCK reference. The PCM510xA-Q1 disables the internal PLL when an external SCK is supplied; specific BCK rates are required to generate an appropriate master clock. Table 4 describes the minimum and maximum BCK per LRCK for the integrated PLL to automatically generate an internal SCK.

Table 4. BCK Rates (MHz) by LRCK Sample Rate for PCM510xA-Q1 PLL Operation

Sample f (kHz)	BCK (f _s)	
	32	64
8	–	–
16	–	1.024
32	1.024	2.048
44.1	1.4112	2.8224
48	1.536	3.072
96	3.072	6.144
192	6.144	12.288
384	12.288	24.576

Audio Data Interface

Audio Serial Interface

The audio interface port is a 3-wire serial port, including LRCK (pin 15), BCK (pin 13), and DIN (pin 14). BCK is the serial audio bit clock, used to clock the serial data present on DIN into the serial shift register of the audio interface. Serial data is clocked into the PCM510xA-Q1 on the rising edge of BCK. LRCK is the serial audio left and right word clock.

Table 5. PCM510xA-Q1 Audio Data Formats, Bit Depths and Clock Rates

CONTROL MODE	FORMAT	DATA BITS	MAX LRCK FREQUENCY [f _s]	SCK RATE [x f _s]	BCK RATE [x f _s]
Hardware Control	I ² S or LJ	32, 24, 20, 16	Up to 192 kHz	128 – 3072 (≤ 50 MHz)	64, 48, 32
			384 kHz	64, 128	64, 48, 32

The PCM510xA-Q1 requires the synchronization of LRCK and system clock, but does not need a specific phase relation between LRCK and system clock.

If the relationship between LRCK and system clock changes more than ±5 SCK, internal operation is initialized within one sample period and analog outputs are forced to the BPZ level until resynchronization between LRCK and system clock is completed.

If the relationship between LRCK and BCK are invalid more than four LRCK periods, internal operation is initialized within one sample period and analog outputs are forced to the BPZ level until resynchronization between LRCK and BCK is completed.

PCM Audio Data Formats and Timing

The PCM510xA-Q1 supports industry-standard audio data formats, including standard I²S and left-justified. Data formats are selected using the FMT (pin 16), Low for I²S, and high for left-justified.

All formats require binary 2s complement, MSB-first audio data. Figure 14 shows a detailed timing diagram for the serial audio interface.

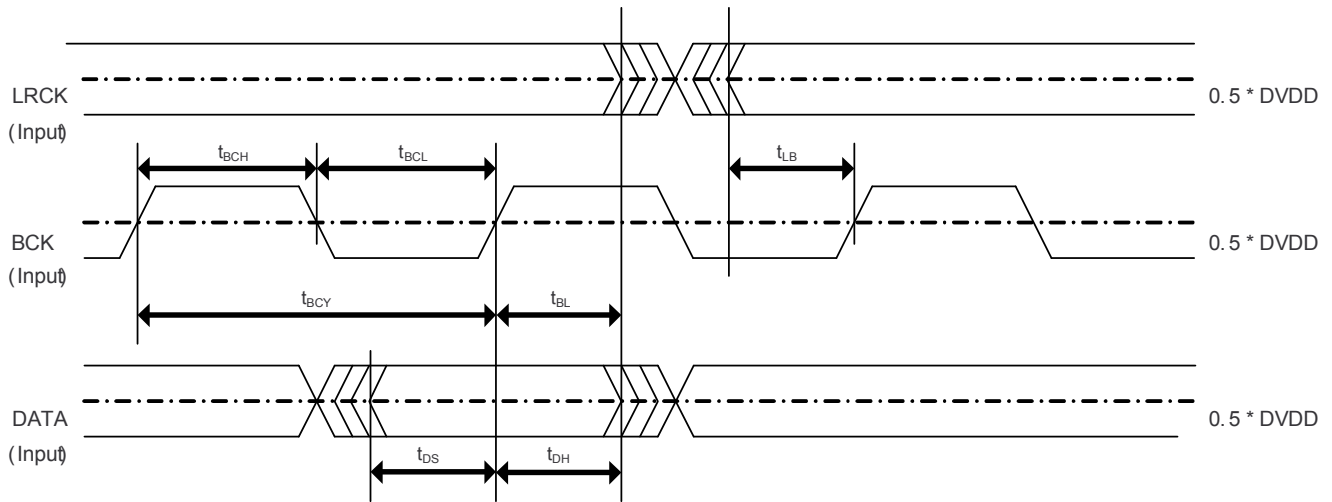


Figure 14. PCM510xA-Q1 Serial Audio Timing - Slave

Table 6. Audio Interface Slave Timing

	Parameters	Min	Max	Units
t_{BCY}	BCK Pulse Cycle Time	40		ns
t_{BCL}	BCK Pulse Width LOW	16		ns
t_{BCH}	BCK Pulse Width HIGH	16		ns
t_{BL}	BCK Rising Edge to LRCK Edge	8		ns
t_{LB}	LRCK Edge to BCK Rising Edge	8		ns
t_{DS}	DATA Set Up Time	8		ns
t_{DH}	DATA Hold Time	8		ns
f_{BCK}	BCK frequency at $DV_{DD} = 3.3\text{ V}$		24.576	MHz
f_{BCK}	BCK frequency at $DV_{DD} = 1.8\text{ V}$		12.288	MHz

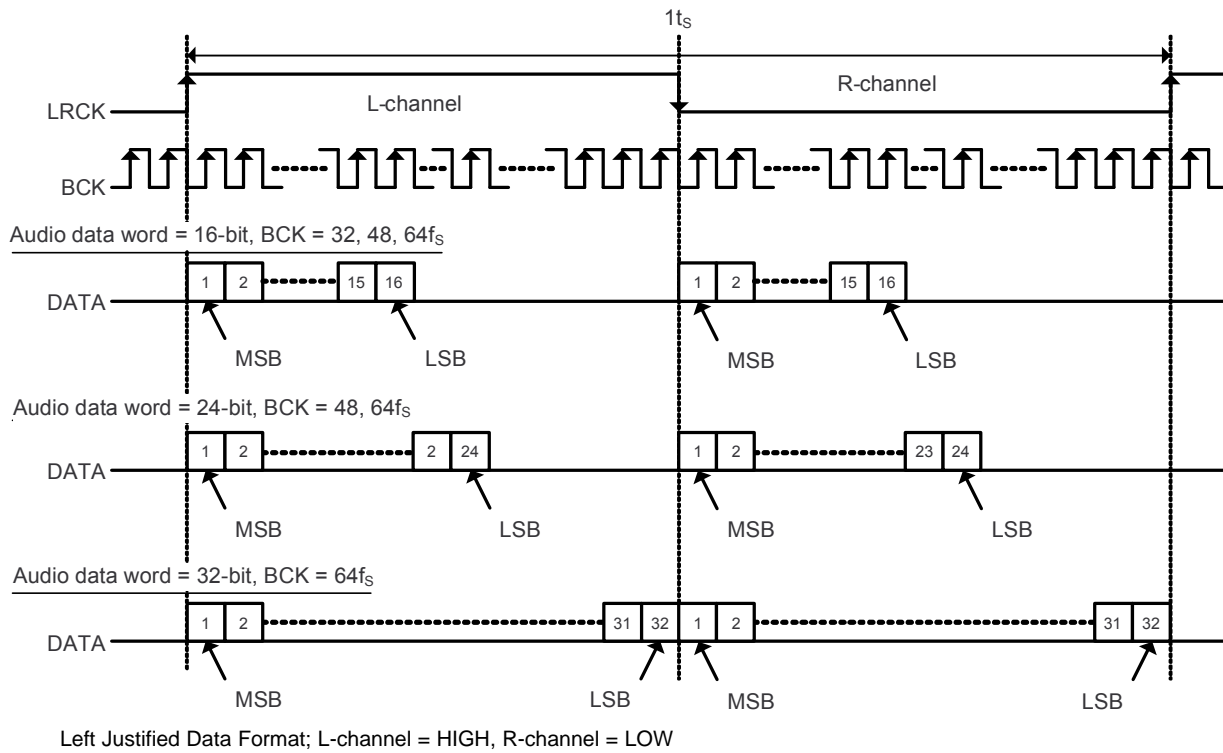


Figure 15. Left Justified Audio Data Format

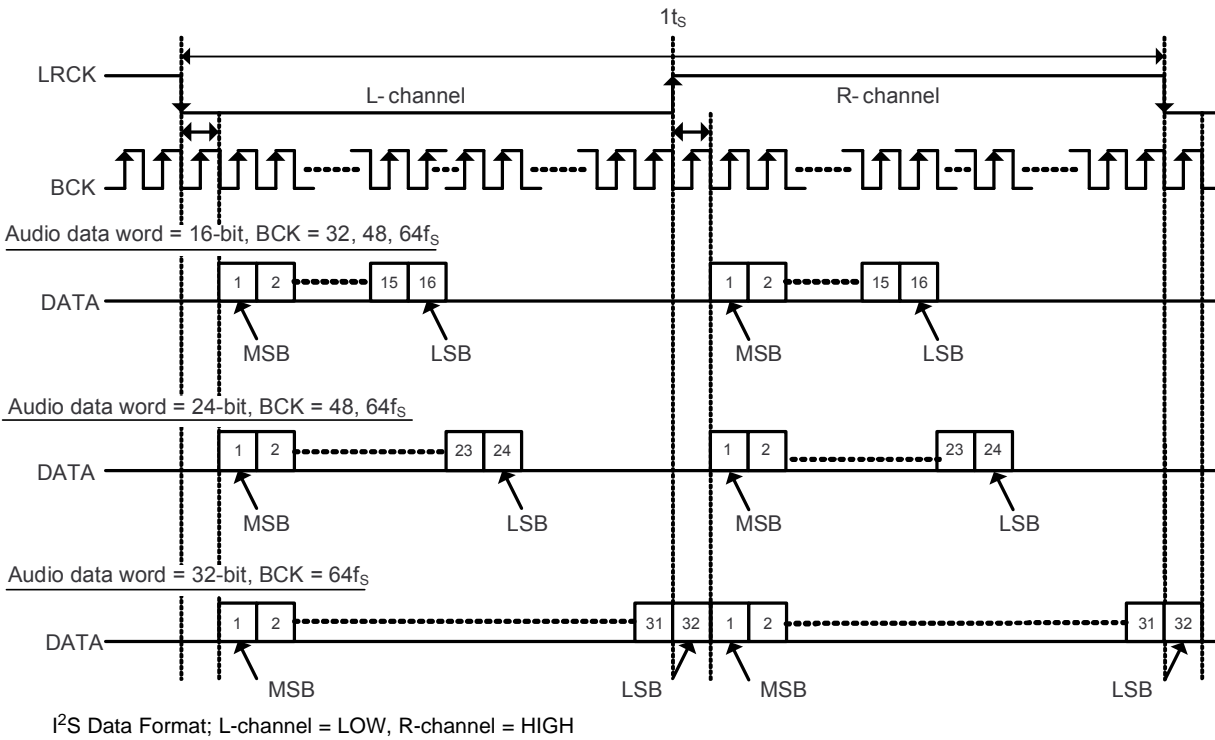


Figure 16. I²S Audio Data Format

Function Descriptions

Interpolation Filter

The PCM510xA-Q1 provides two types of interpolation filter. Users can select which filter to use by using the FLT (pin 11)

Table 7. Digital Interpolation Filter Options

FLT Pin	Description
0	FIR Normal x8 / x4 / x2 / x1 Interpolation Filters
1	IIR Low Latency x8 / x4 / x2 / x1 Interpolation Filters

The normal x8 / x4 / x2 / x1 (bypass) interpolation filter is programmed in 256 cycles in one sample time (t_s) for sample rates from 8 kHz to 384 kHz.

Table 8. Normal x8 Interpolation Filter

Parameter	Condition	Value (Typ)	Value (Max)	Units
Filter Gain Pass Band	0 0.45 f_s		± 0.02	dB
Filter Gain Stop Band	0.55 f_s 7.455 f_s	-60		dB
Filter Group Delay		22 t_s		s

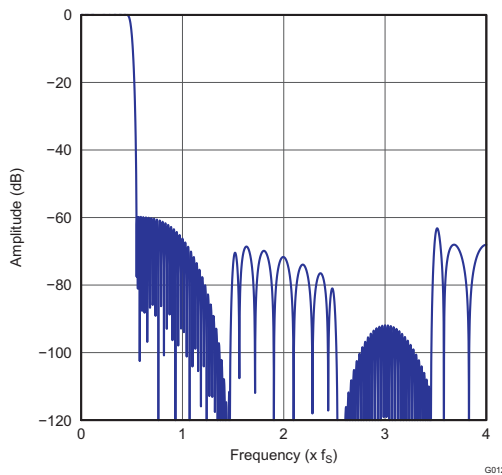


Figure 17. Normal x8 Interpolation Filter Frequency Response

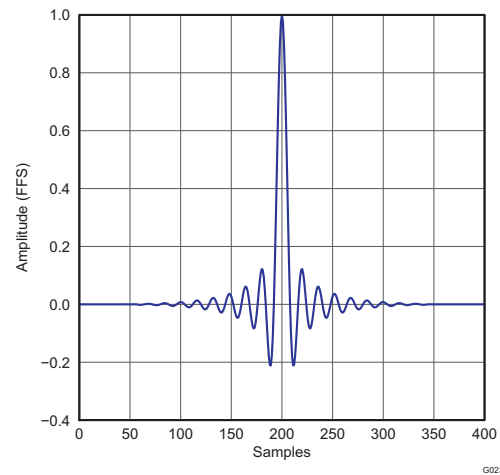


Figure 18. Normal x8 Interpolation Filter Impulse Response

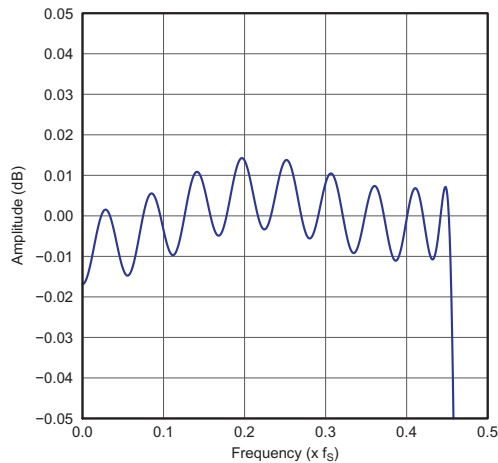


Figure 19. Normal x8 Interpolation Filter Passband Ripple

The normal x4 / x2 / x1 (bypass) interpolation filter is programmed in 256 cycles in one t_S for sample rates from 8 kHz to 384 kHz.

Table 9. Normal x4 Interpolation Filter

Parameter	Condition	Value (Typ)	Value (Max)	Units
Filter Gain Pass Band	0 0.45 f_S		± 0.02	dB
Filter Gain Stop Band	0.55 f_S 7.455 f_S	-60		dB
Filter Group Delay		22 t_S		s

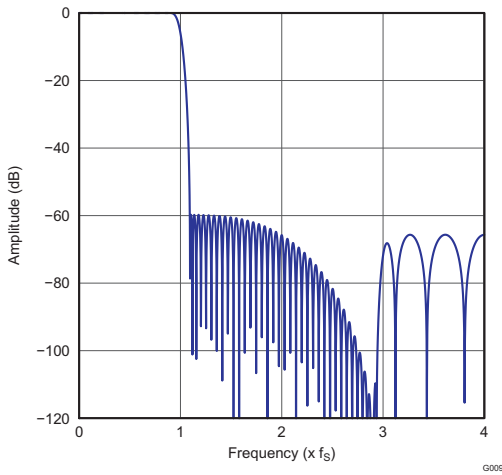


Figure 20. Normal x4 Interpolation Filter Frequency Response

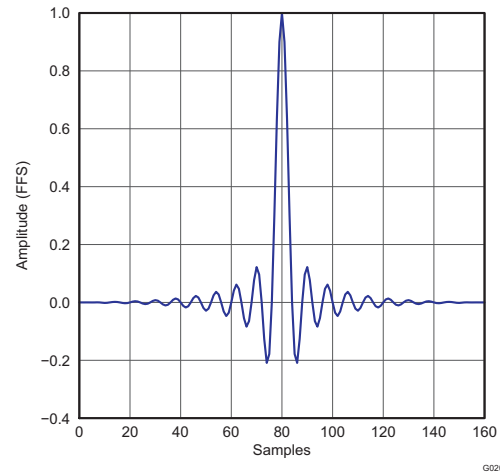


Figure 21. Normal x4 Interpolation Filter Impulse Response

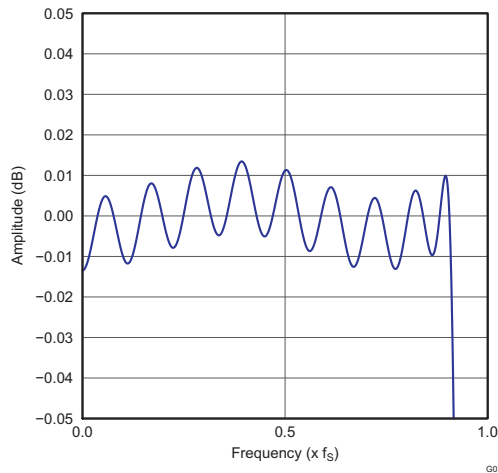


Figure 22. Normal x4 Interpolation Filter Passband Ripple

Normal x2 / x1 (bypass) interpolation filter is programmed in 256 cycles in one t_S for sample rates from 8 kHz to 384 kHz.

Table 10. Normal x2 Interpolation Filter

Parameter	Condition	Value (Typ)	Value (Max)	Units
Filter Gain Pass Band	0 0.45 f_S		± 0.02	dB
Filter Gain Stop Band	0.55 f_S 7.455 f_S	-60		dB
Filter Group Delay		22 t_S		s

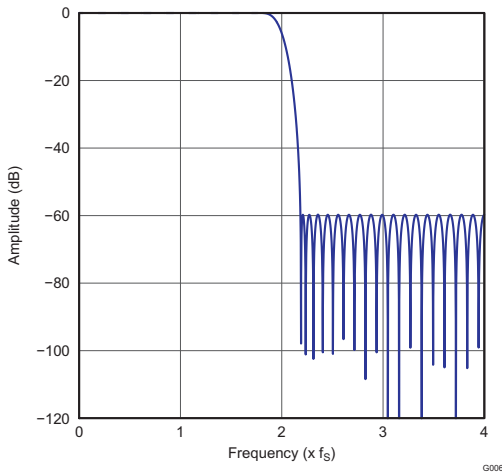


Figure 23. Normal x2 Interpolation Filter Frequency Response

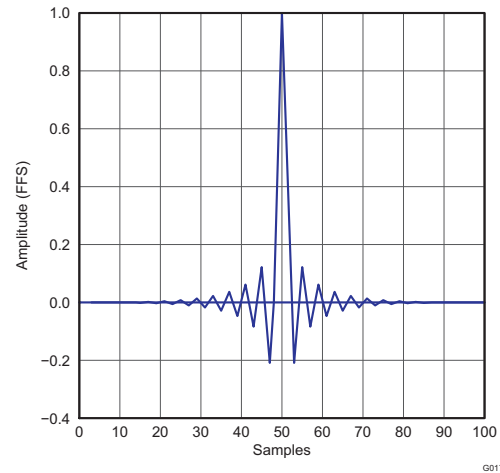


Figure 24. Normal x2 Interpolation Filter Impulse Response

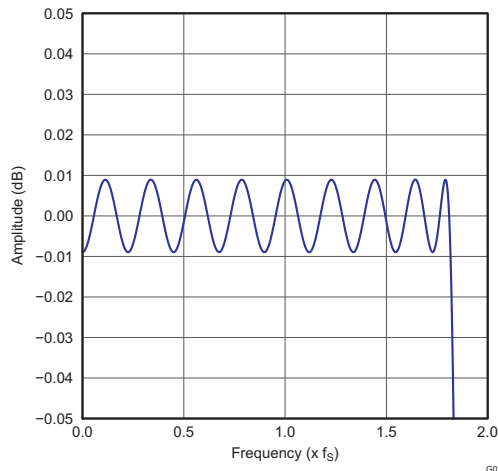


Figure 25. Normal x2 Interpolation Filter Passband Ripple

The low-latency x8 / x4 / x2 / x1 (bypass) interpolation filter is programmed in 256 cycles one t_S for sample rates from 8 kHz to 384 kHz.

Table 11. Low latency x8 Interpolation Filter

Parameter	Condition	Value (Typ)	Units
Filter Gain Pass Band	0 0.45 f_S	± 0.0001	dB
Filter Gain Stop Band	0.55 f_S 7.455 f_S	-52	dB
Filter Group Delay		3.5 t_S	s

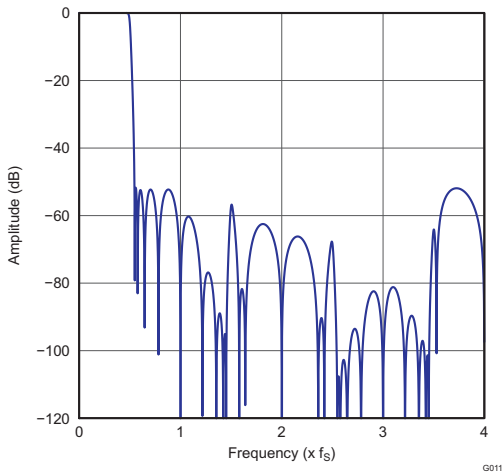


Figure 26. Low latency x8 Interpolation Filter Frequency Response

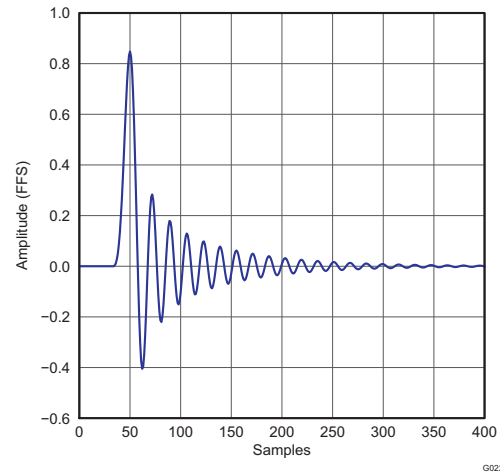


Figure 27. Low latency x8 Interpolation Filter Impulse Response

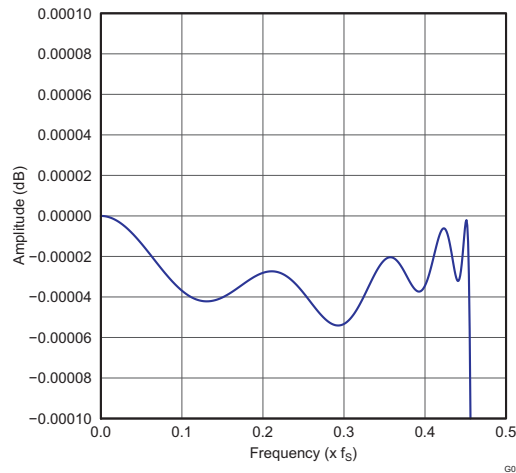


Figure 28. Low latency x8 Interpolation Filter Passband Ripple

Table 12. Low latency x4 Interpolation Filter

Parameter	Condition	Value (Typ)	Units
Filter Gain Pass Band	0 0.45 f_s	± 0.0001	dB
Filter Gain Stop Band	0.55 f_s 3.455 f_s	-52	dB
Filter Group Delay		3.5 t_s	s

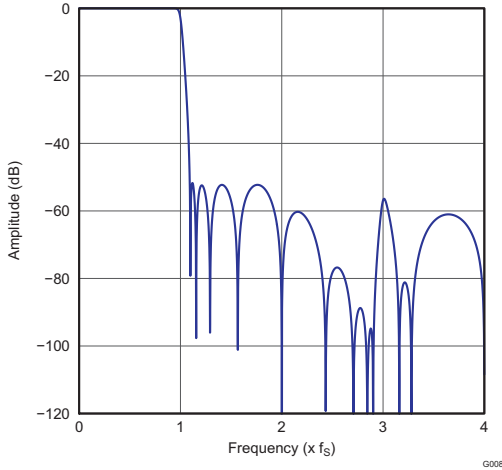


Figure 29. Low latency x4 Interpolation Filter Frequency Response

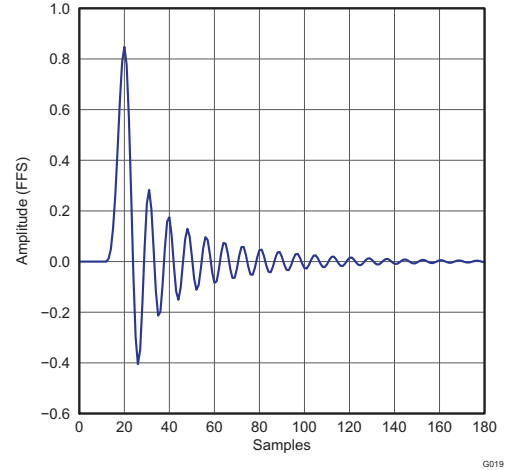


Figure 30. Low latency x4 Interpolation Filter Impulse Response

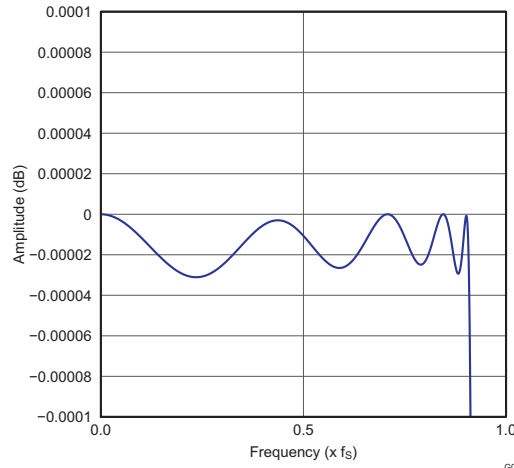


Figure 31. Low latency x4 Interpolation Filter Passband Ripple

Table 13. Low latency x2 Interpolation Filter

Parameter	Condition	Value (Typ)	Units
Filter Gain Pass Band	0 0.45 f_s	± 0.0001	dB
Filter Gain Stop Band	0.55 f_s 1.455 f_s	-52	dB
Filter Group Delay		3.5 t_s	s

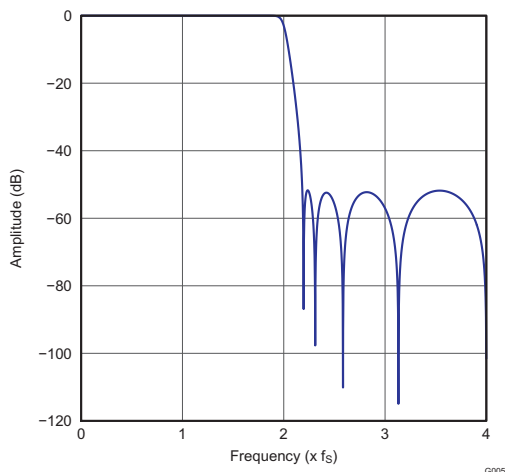


Figure 32. Low latency x2 Interpolation Filter Frequency Response

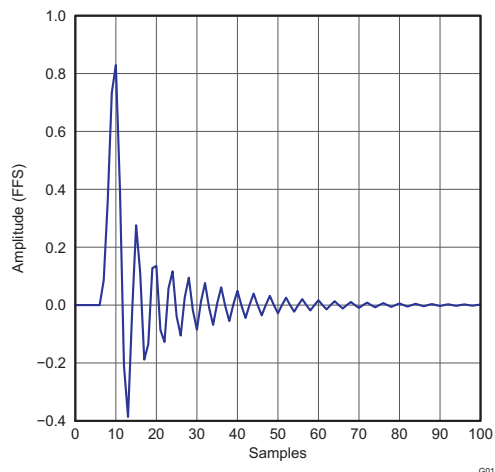


Figure 33. Low latency x2 Interpolation Filter Impulse Response

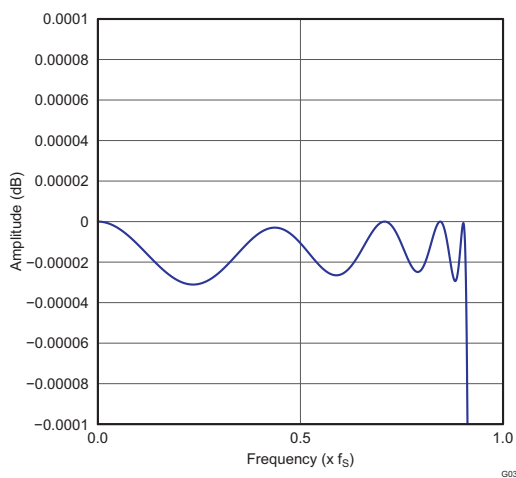


Figure 34. Low latency x2 Interpolation Filter Passband Ripple

Zero Data Detect

The PCM510xA-Q1 has a zero-data detect function. When the device detects continuous zero data, it enters a full AMUTE condition.

The PCM510xA-Q1 counts zero data over 1024LRCKs (21 ms at 48 kHz) before setting AMUTE.

Power Save Mode

When any kind of clock error (SCK, BCK, and LRCK) or clock halt is detected, the PCM510xA-Q1 enters stand-by mode automatically. The current-segment DAC and line driver are also powered down.

When BCK and LRCK halt to a low level for more than one second, the PCM510xA-Q1 enters power-down mode automatically. Power-down mode includes the negative charge pump and bias or reference circuit power-down in addition to stand-by.

Whenever expected audio clocks (SCK, BCK, LRCK) are applied to the PCM510xA-Q1, the device starts its power-up sequence automatically.

XSMT Pin (Soft Mute and Soft Un-Mute)

For external digital control of the PCM510xA-Q1, the XSMT pin must be driven by an external digital host with a specific minimum rise time (t_r) and fall time (t_f) for soft mute and soft un-mute. The PCM510xA-Q1 requires rise and fall times of less than 20 ns. In the majority of applications, this should not be a problem, however, traces with high capacitance may have issues.

When the XSMT pin is shifted from high to low (3.3 V to 0 V), a soft digital attenuation ramp is started, -1 dB attenuation is applied every $1 t_s$ from 0 dBFS to $-\infty$. This attenuation takes 104 sample times.

When the XSMT pin is shifted from low to high (0 V to 3.3 V), a soft digital un-mute is started, 1 dB gain steps are applied every t_s from $-\infty$ to 0 dBFS. This ramp-up takes 104 sample times.

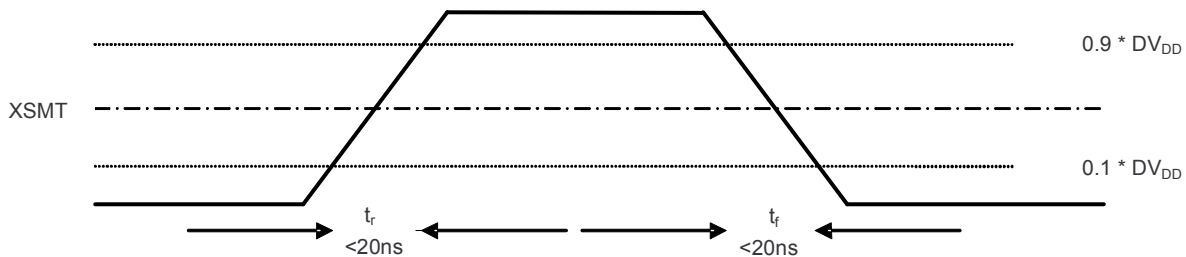


Figure 35. XSMT Timing for Soft Mute and Soft Un-Mute

Table 14. XSMT Timing Parameters

Parameters	Min	Max	Unit
Rise time (t_r)		20	ns
Fall time (t_f)		20	ns

External Power Sense Undervoltage Protection Mode (Supported Only When $DV_{DD} = 3.3$ V)

The XSMT pin can also be used to monitor a system voltage, such as the $24-V_{DC}$ LCD TV backlight, or $12-V_{DC}$ system supply using a potential divider created with two resistors. (See Figure 36)

- If the XSMT pin makes a transition from 1 to 0 over 6 ms or more, the device switches into external undervoltage protection mode. In this mode, two trigger levels are used.
- When XSMT pin level reaches 2 V, soft mute process begins.
- When XSMT pin level reaches 1.2 V, AMUTE engages, regardless of digital audio level, and analog shut down begins. For example, DAC circuitry powers down.

A timing diagram to show this is shown in Figure 37.

NOTE

The XSMT input pins voltage range is from -0.3 V to $DV_{DD} + 0.3\text{ V}$. The ratio of external resistors must be considered within this input range. Any increase in power supply (such as power supply positive noise or ripple) can pull the XSMT pin higher than $DV_{DD} + 0.3\text{ V}$.

For example, if the PCM510xA-Q1 is monitoring a 12-V input, and dividing the voltage by four, then the voltage at XSMT during ideal power supply conditions is 3 V. If the voltage spikes any higher than 14.4 V, then XSMT sees a voltage in excess of 3.6 V ($DV_{DD} + 0.3$), potentially damaging the device.

Providing the divider is set appropriately, any DC voltage can be monitored.

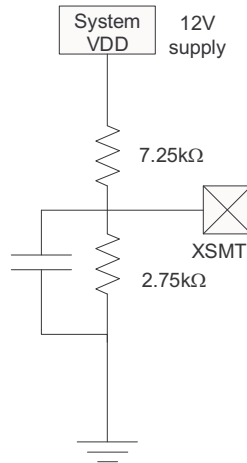


Figure 36. XSMT in External UVP Mode

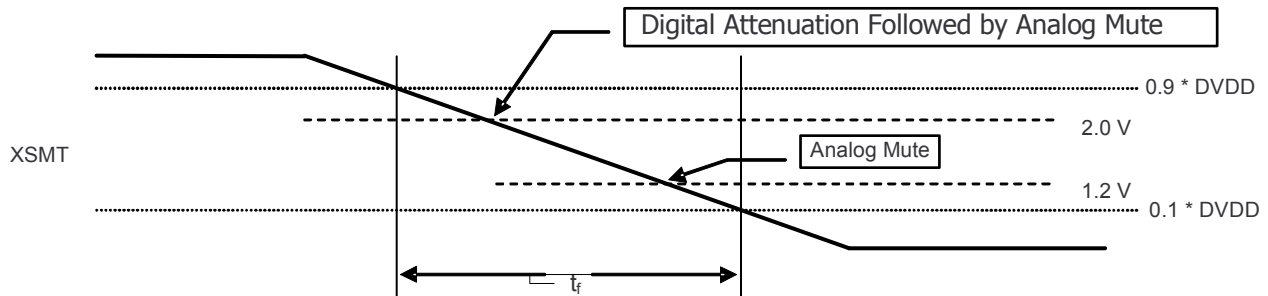


Figure 37. XSMT Timing for Undervoltage Protection

Recommended Powerdown Sequence

With inadequate system design, the PCM510xA-Q1 can exhibit some pop on power down. Pops are caused by the device not having enough time to detect power loss and start the muting process.

The PCM510xA-Q1 evaluation board avoids audible pop with an electrolytic decoupling capacitor. This capacitor provides enough time between data loss from universal serial bus (USB) or S/PDIF and power supply loss for the muting process to take place.

The PCM510xA-Q1 has two auto-mute functions to mute the device upon power loss (intentional or unintentional).

XSMT = 0

When the XSMT pin is pulled low, the incoming PCM data is attenuated to 0, closely followed by a hard AMUTE. This process takes $150 t_s + 0.2\text{ mS}$.

Because this digital power supply voltage mute time is mainly dominated by the sampling frequency, systems sampling at 192 kHz mutes much faster than a 48-kHz system.

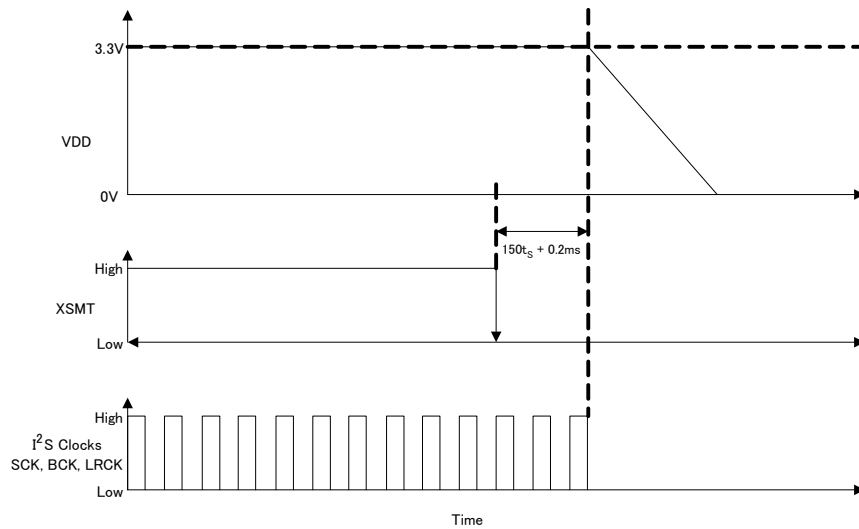
Clock Error Detect

When clock error is detected on the incoming data clock, the PCM510xA-Q1 family switches to an internal oscillator, and continues to drive the output, while attenuating the data from the last known value. Once this process is complete, the PCM510xA-Q1 outputs are hard muted to ground.

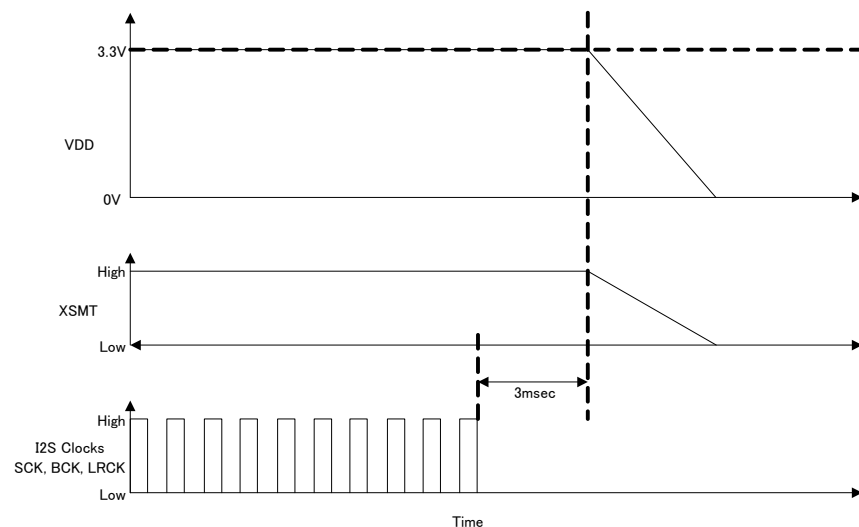
Planned Shutdown

These auto-muting processes can be manipulated by system designs to mute before power loss in the following ways:

1. Assert XSMT low 150 t_S + 0.2 ms before power is removed.



2. Stop I²S clocks (SCK, BCK, LRCK) 3 ms before power down as shown below:



Unplanned Shutdown

Many systems use a low-noise regulator to provide an analog power supply voltage 3.3-V supply for the DAC. The XSMT pin can take advantage of such a feature to measure the pre-regulated output from the system switched mode power supply (SMPS) to mute the output before the entire SMPS discharges. [Figure 38](#) shows how to configure such a system to use the XSMT pin. The XSMT pin can also be used in parallel with a GPIO pin from the system microcontroller or digital signal processor (DSP), or Power Supply.

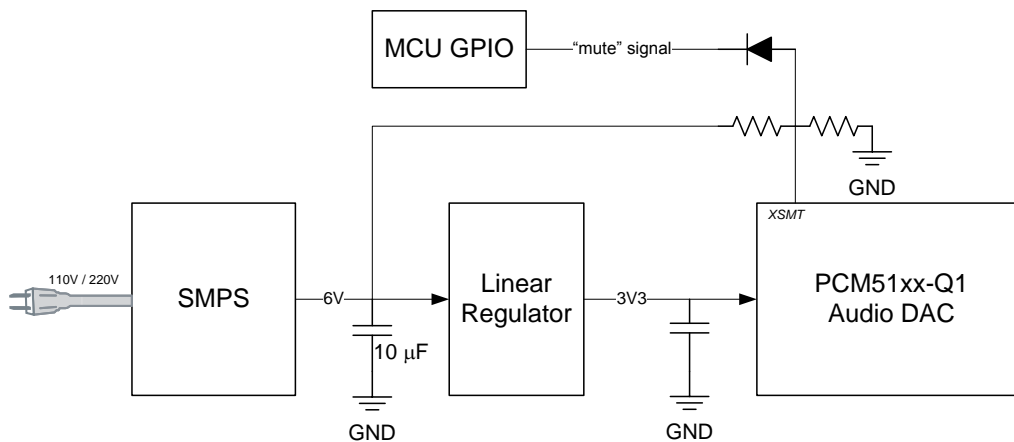


Figure 38. Using the XSMT Pin

Typical Application Circuits

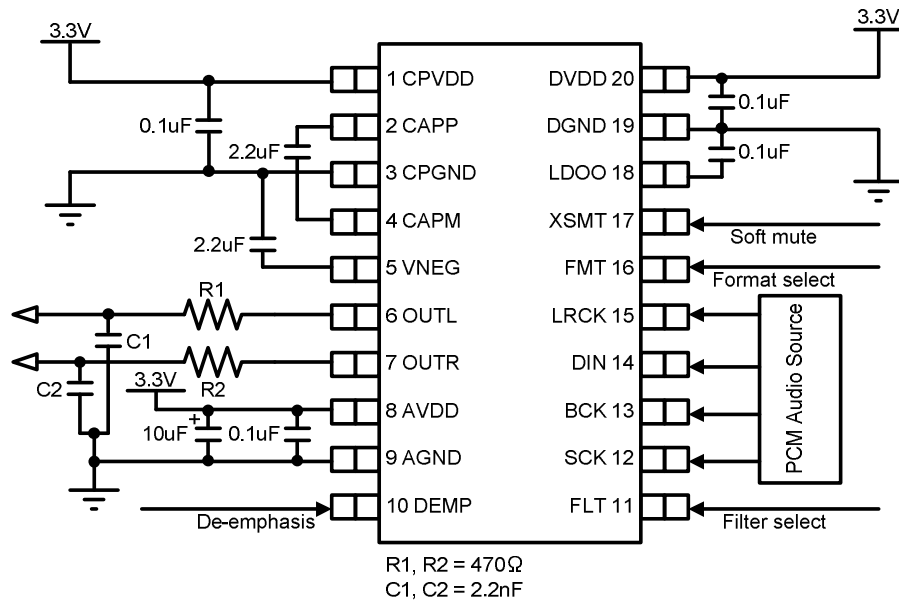


Figure 39. PCM510xA-Q1 Standard PCM Audio Operation, 3.3 V

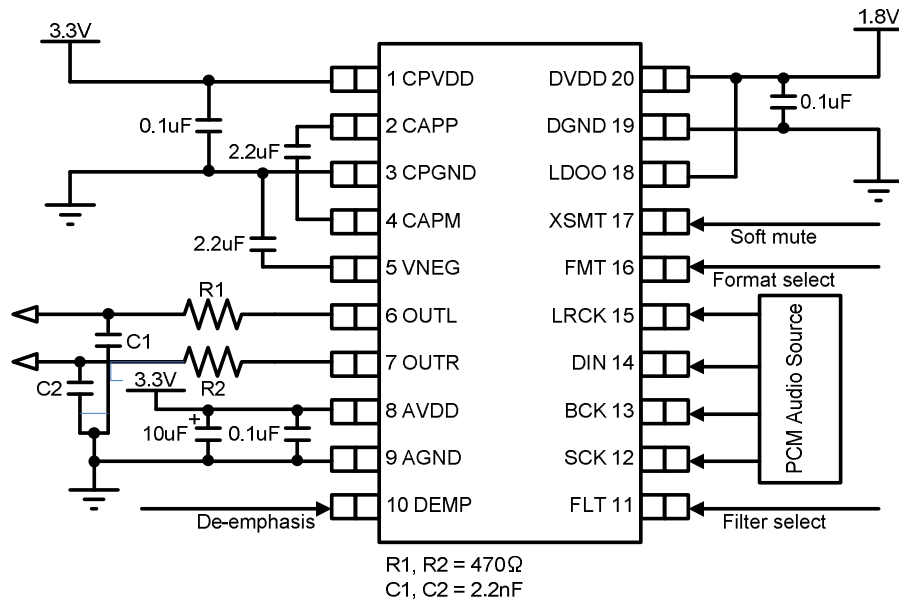


Figure 40. PCM510xA-Q1 Standard PCM Audio Operation, 1.8 V

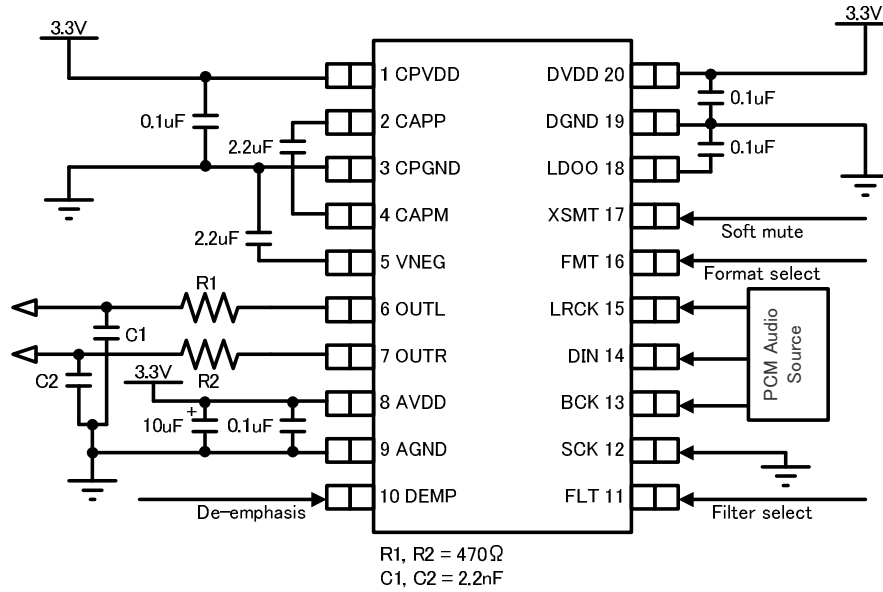


Figure 41. PCM510xA-Q1 PLL Operation, 3.3 V

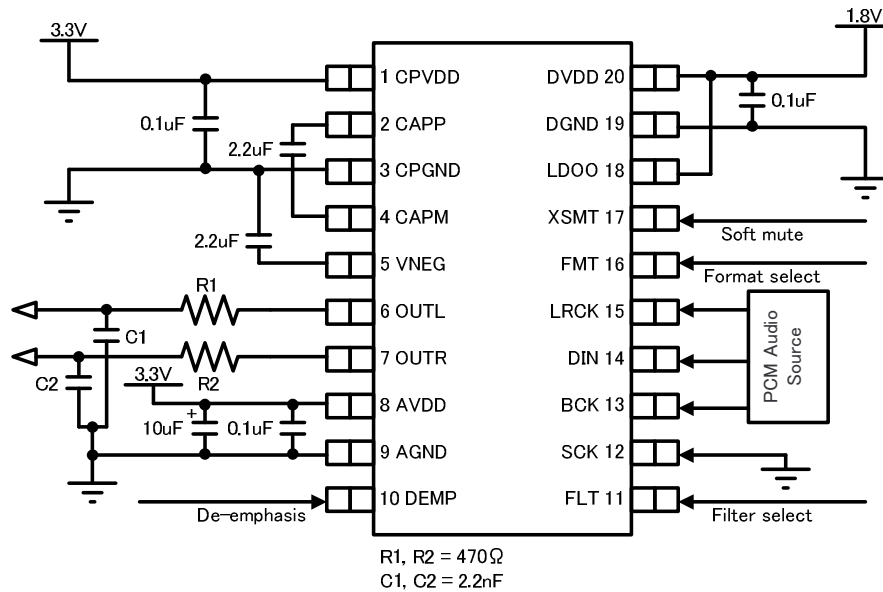


Figure 42. PCM510xA-Q1 PLL Operation, 1.8 V

Recommended Output Filter for the PCM510xA-Q1

The diagram in [Figure 43](#) shows the recommended output filter for the PCM510xA-Q1. The new PCM510xA-Q1 next generation current segment architecture offers excellent out of band noise, making a traditional 20-kHz low pass filter unnecessary.

The RC settings below offer a -3 -dB filter point at 153 kHz (approximately), giving the DAC the ability to reproduce virtually all frequencies through to its maximum sampling rate of 384 kHz.

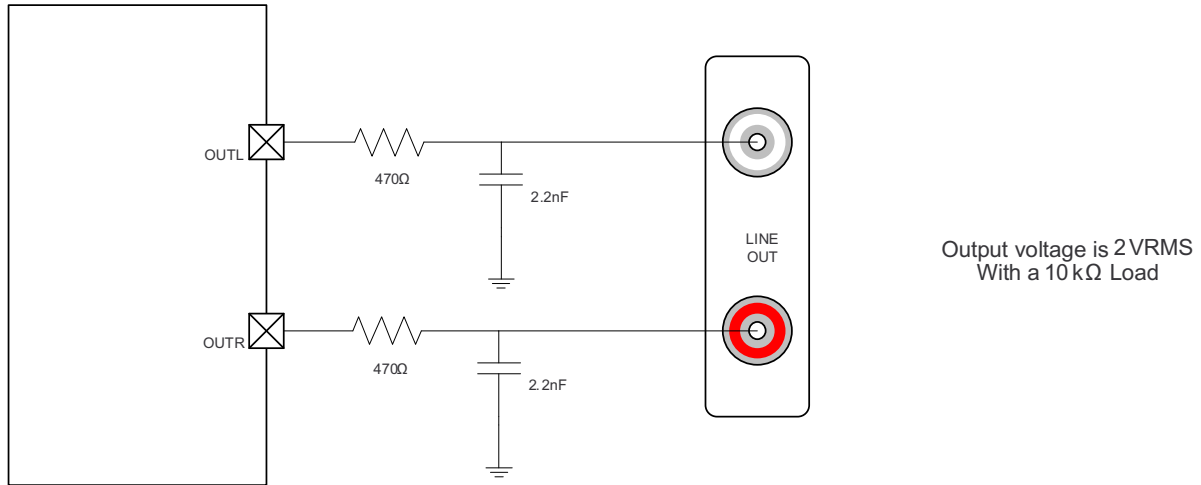


Figure 43. Recommended Output Lowpass Filter for 10-kΩ Operation

REVISION HISTORY

Changes from Original (September 2013) to Revision A	Page
• Changed 文档状态从产品预览改为生成数据	1
• Added T_A to <i>Differences Between PCM510xA-Q1 Devices</i> table	2
• Changed generic part number to orderable part number in <i>Differences Between PCM510xA-Q1 Devices</i> table	2
• Added top-side marking to <i>Differences Between PCM510xA-Q1 Devices</i> table	2
• Changed <i>THERMAL CHARACTERISTICS</i> table to provide more information on Thermal Metrics	4
• Changed $T_A = 25^\circ\text{C}$ to temperature range in condition statement of <i>ELECTRICAL CHARACTERISTICS</i> table	4
• Changed $T_A = 25^\circ\text{C}$ to temperature range in condition statement of <i>ELECTRICAL CHARACTERISTICS</i> table	5
• Changed $T_A = 25^\circ\text{C}$ to temperature range in condition statement of <i>ELECTRICAL CHARACTERISTICS</i> table	6
• Changed min and max values from -6 and $+6$ to -7 and $+7$ for the Gain error parameter under Analog Output in the <i>ELECTRICAL CHARACTERISTICS</i> table	6
• Changed min and max values from -6 and $+6$ to -7 and $+7$ for the Gain mismatch parameter under Analog Output in the <i>ELECTRICAL CHARACTERISTICS</i> table	6
• Changed $T_A = 25^\circ\text{C}$ to temperature range in condition statement of <i>ELECTRICAL CHARACTERISTICS</i> table	7

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
PCM5100AQPWRQ1	ACTIVE	TSSOP	PW	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	P5100AQ1	Samples
PCM5101AQPWRQ1	ACTIVE	TSSOP	PW	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	P5101AQ1	Samples
PCM5102AQPWRQ1	ACTIVE	TSSOP	PW	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	P5102AQ1	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
PCM5100AQPWRQ1	TSSOP	PW	20	2000	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1
PCM5101AQPWRQ1	TSSOP	PW	20	2000	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1
PCM5102AQPWRQ1	TSSOP	PW	20	2000	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
PCM5100AQPWRQ1	TSSOP	PW	20	2000	350.0	350.0	43.0
PCM5101AQPWRQ1	TSSOP	PW	20	2000	350.0	350.0	43.0
PCM5102AQPWRQ1	TSSOP	PW	20	2000	350.0	350.0	43.0

PW0020A



PACKAGE OUTLINE

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



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NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

EXAMPLE BOARD LAYOUT

PW0020A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



SOLDER MASK DETAILS

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NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

PW0020A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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