

SM320VC5421-EP Fixed-Point Digital Signal Processor

Data Manual

Literature Number: SGUS047
July 2003

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.



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1 SM320VC5421-EP Features

- **Controlled Baseline**
 - One Assembly/Test Site, One Fabrication Site
- **Extended Temperature Performance of –40°C to 85°C**
- **Enhanced Diminishing Manufacturing Sources (DMS) Support**
- **Enhanced Product-Change Notification**
- **Qualification Pedigree†**
- **200-MIPS Dual-Core DSP Consisting of Two Independent Subsystems**
- **Each Core Has an Advanced Multibus Architecture With Three Separate 16-Bit Data Memory Buses and One Program Bus**
- **40-Bit Arithmetic Logic Unit (ALU) Including a 40-Bit Barrel-Shifter and Two 40-Bit Accumulators Per Core**
- **Each Core Has a 17-Bit × 17-Bit Parallel Multiplier Coupled to a 40-Bit Adder for Non-Pipelined Single-Cycle Multiply/Accumulate (MAC) Operations**
- **Each Core Has a Compare, Select, and Store Unit (CSSU) for the Add/Compare Selection of the Viterbi Operator**
- **Each Core Has an Exponent Encoder to Compute an Exponent Value of a 40-Bit Accumulator Value in a Single Cycle**
- **Each Core Has Two Address Generators With Eight Auxiliary Registers and Two Auxiliary Register Arithmetic Units (ARAUs)**
- **16-Bit Data Bus With Data Bus Holder Feature**
- **512K-Word × 16-Bit Extended Program Address Space**
- **Total of 256K-Word × 16-Bit Dual- and Single-Access On-Chip RAM (128K-Word × 16-Bit Two-Way Shared Memory)**
- **Single-Instruction Repeat and Block-Repeat Operations**
- **Instructions With 32-Bit-Long Word Operands**
- **Instructions With Two or Three Operand Reads**
- **Fast Return From Interrupts**
- **Arithmetic Instructions With Parallel Store and Parallel Load**
- **Conditional Store Instructions**
- **Output Control of CLKOUT**
- **Output Control of TOUT**
- **Power Consumption Control With IDLE1, IDLE2, and IDLE3 Instructions**
- **Dual 1.8-V (Core) and 3.3-V (I/O) Power Supplies for Low-Power, Fast Operations**
- **10-ns Single-Cycle Fixed-Point Instruction**
- **Interprocessor Communication via Two Internal 8-Element FIFOs**
- **Twelve Channels of Direct Memory Access (DMA) for Data Transfers With No CPU Loading (Six Channels Per Subsystem With External Access)**
- **Six Multichannel Buffered Serial Ports (McBSPs) With 128-Channel Selection Capability (Three McBSPs per Subsystem)**
- **16-Bit Host-Port Interface (HPI) Multiplexed With External Memory Interface Pins**
- **Software-Programmable Phase-Locked Loop (APLL) Provides Several Clocking Options (Requires External Oscillator)**
- **On-Chip Scan-Based Emulation Logic, IEEE Standard 1149-1‡ (JTAG) Boundary-Scan Logic**
- **Two Software-Programmable Timers (One Per Subsystem)**
- **Software-Programmable Wait-State Generator (14 Wait States Maximum)**
- **Provided in 144-pin Low-Profile Quad Flatpack (LQFP) (PGE Suffix) Package**

† Component qualification in accordance with JEDEC and industry standards to ensure reliable operation over an extended temperature range. This includes, but is not limited to, Highly Accelerated Stress Test (HAST) or biased 85/85, temperature cycle, autoclave or unbiased HAST, electromigration, bond intermetallic life, and mold compound life. Such qualification testing should not be viewed as justifying use of this component beyond specified performance and environmental limits.

‡ IEEE Standard 1149.1-1990 Standard-Test-Access Port and Boundary Scan Architecture.

2 Introduction

This section describes the main features, gives a brief functional overview of the SM320VC5421-EP, lists the pin assignments, and provides a signal description table. This data manual also provides a detailed description section, electrical specifications, parameter measurement information, and mechanical data about the available packaging.

NOTE: This data manual is designed to be used in conjunction with the *TMS320C54x™ DSP Functional Overview* (literature number SPRU307).

2.1 Description

The 320VC5421 fixed-point digital signal processor (DSP) is a dual-core solution running at 200-MIPS performance. The 5421 consists of two DSP subsystems capable of core-to-core communications and a 128K-word zero-wait-state on-chip program memory shared by the two DSP subsystems. Each subsystem consists of one 54x DSP core, 32K-word program/data DARAM, 32K-word data SARAM, 2K-word ROM, three multichannel serial interfaces, xDMA logic, one timer, one APLL, and other miscellaneous circuitry.

The 5421 also contains a host-port interface (HPI) that allows the 5421 to be viewed as a memory-mapped peripheral to a host processor. The 5421 is pin-compatible with the TMS320VC5420.

Each subsystem has its separate program and data spaces, allowing simultaneous accesses to program instructions and data. Two read operations and one write operation can be performed in one cycle. Instructions with parallel store and application-specific instructions can fully utilize this architecture. Furthermore, data can be transferred between program and data spaces. Such parallelism supports a powerful set of arithmetic, logic, and bit-manipulation operations that can all be performed in a single machine cycle. The 5421 includes the control mechanisms to manage interrupts, repeated operations, and function calls. In addition, the 5421 has 128K words of on-chip program memory that can be shared between the two subsystems.

The 5421 is intended as a high-performance, low-cost, high-density DSP for remote data access or voice-over IP subsystems. It is designed to maintain the current modem architecture with minimal hardware and software impacts, thus maximizing reuse of existing modem technologies and development efforts.

2.2 Migration From the 5420 to the 5421

Customers migrating from the 5420 to the 5421 need to take into account the following:

- The memory structure of the 5421 has been changed to incorporate 128K x 16-bit words of two-way shared memory.
- The DMA of the 5421 has been enhanced to provide access to external, as well as internal memory.
- The HPI and DMA memory maps have been changed to incorporate the new memory 5421.
- 2K x 16-bit words of ROM have been added to the 5421 for bootloading purposes only.
- The VCO pin on the 5420 has been replaced with the $\overline{\text{HOLDA}}$ pin on the 5421 and the $\overline{\text{HOLD}}$ pin was added to the 5421 at a previously unused pin location.
- The McBSPs have been updated with a new mode that allows 128-channel selection capability.
- McBSP CLKX/R pins can be used as inputs to internal clock rate generator for CLKS-like function without the penalty of extra pins.
- The SELA/B pin on 5421 is changed to type I/O/Z for added functionality.

NOTE:

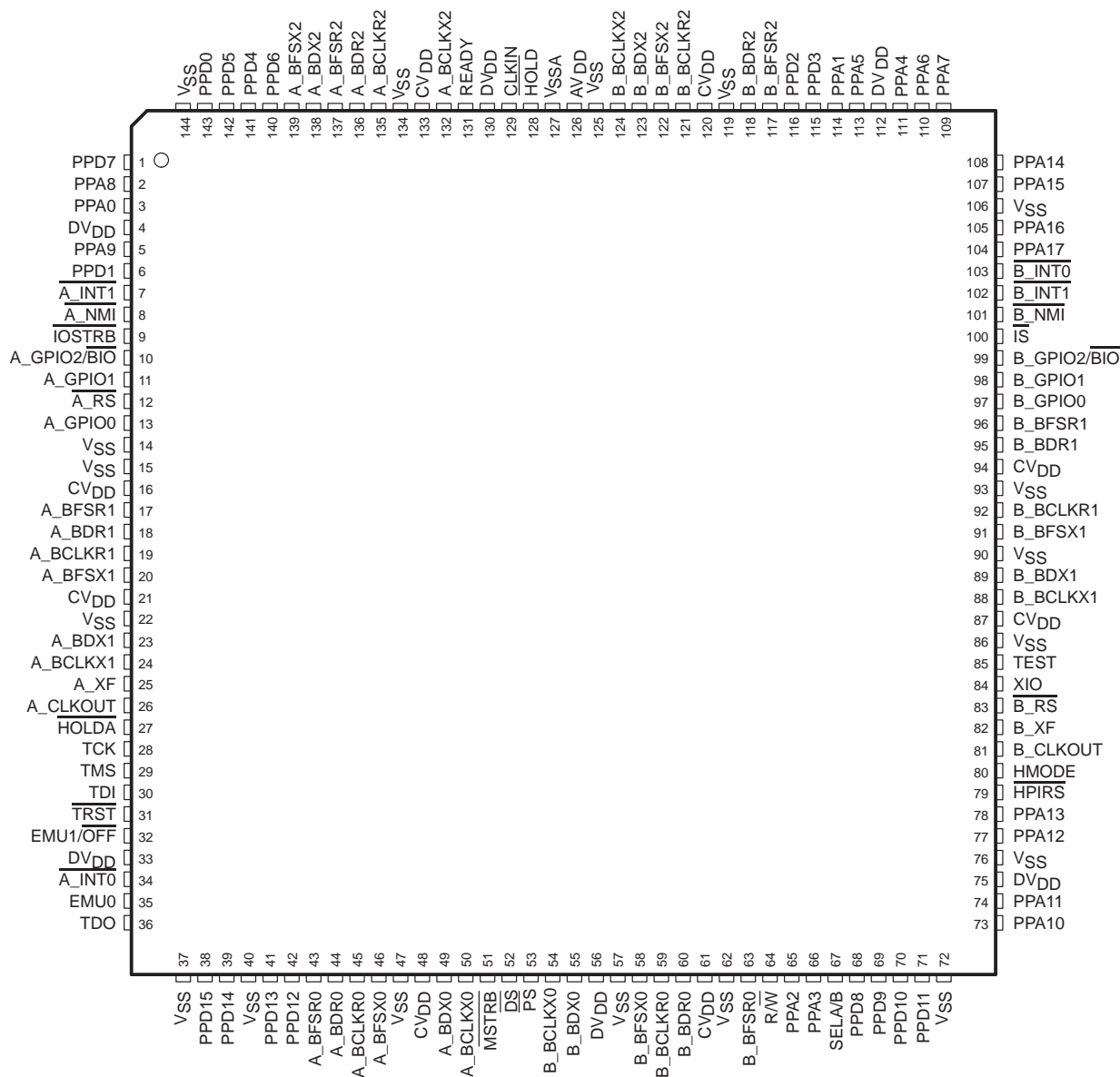
For additional information, see *TMS320VC5420 to TMS320VC5421 DSP Migration* (literature number SPRA621).

2.3 Pin Assignments

Figure 2–1 provides the pin assignments for the 144-pin low-profile quad flatpack (LQFP) package.

2.3.1 Pin Assignments for the PGE Package

The SM320VC5421PGE-EP 144-pin low-profile quad flatpack (LQFP) is footprint- and pin-compatible with the 5420. Table 2–1 lists the pin number and associated signal name for both the multiplexed mode and the nonmultiplexed mode.



NOTES: A. DVDD is the power supply for the I/O pins while CVDD is the power supply for the core CPU. VSS is the ground for both the I/O pins and the core CPU.

B. Pin configuration shown for nonmultiplexed mode only. See the pin assignments table for the 320VC5421PGE for multiplexed functions of specific pins and for specific pin numbers.

Figure 2–1. 144-Pin Low-Profile Flatpack Pin Assignments (PGE – Top View)

Table 2–1. Pin Assignments for the 144-Pin Low-Profile Quad Flatpack

| SIGNAL NAME (NONMULTIPLEXED) | SIGNAL NAME (MULTIPLEXED) | PIN NO. | SIGNAL NAME (NONMULTIPLEXED) | SIGNAL NAME (MULTIPLEXED) | PIN NO. |
|---------------------------------|------------------------------|------------|---------------------------------|------------------------------|------------|
| PPD7 | HD7 | 1 | PPA8 | HA8 | 2 |
| PPA0 | $\overline{A_HINT/HA0}$ | 3 | DV _{DD} | | 4 |
| PPA9 | HA9 | 5 | PPD1 | HD1 | 6 |
| $\overline{A_INT1}$ | | 7 | $\overline{A_NMI}$ | | 8 |
| \overline{IOSTRB} | A_GPIO3/A_TOUT | 9 | A_GPIO2/ \overline{BIO} | | 10 |
| A_GPIO1 | | 11 | $\overline{A_RS}$ | | 12 |
| A_GPIO0 | A_ROMEN | 13 | V _{SS} | | 14 |
| V _{SS} | | 15 | CV _{DD} | | 16 |
| A_BFSR1 | | 17 | A_BDR1 | | 18 |
| A_BCLKR1 | | 19 | A_BFSX1 | | 20 |
| CV _{DD} | | 21 | V _{SS} | | 22 |
| A_BDX1 | | 23 | A_BCLKX1 | | 24 |
| A_XF | | 25 | A_CLKOUT | | 26 |
| \overline{HOLDA} | | 27 | TCK | | 28 |
| TMS | | 29 | TDI | | 30 |
| \overline{TRST} | | 31 | EMU1/ \overline{OFF} | | 32 |
| DV _{DD} | | 33 | $\overline{A_INT0}$ | | 34 |
| EMU0 | | 35 | TDO | | 36 |
| V _{SS} | | 37 | PPD15 | HD15 | 38 |
| PPD14 | HD14 | 39 | V _{SS} | | 40 |
| PPD13 | HD13 | 41 | PPD12 | HD12 | 42 |
| A_BFSR0 | | 43 | A_BDR0 | | 44 |
| A_BCLKR0 | | 45 | A_BFSX0 | | 46 |
| V _{SS} | | 47 | CV _{DD} | | 48 |
| A_BDX0 | | 49 | A_BCLKX0 | | 50 |
| \overline{MSTRB} | \overline{HCS} | 51 | \overline{DS} | $\overline{HDS2}$ | 52 |
| \overline{PS} | $\overline{HDS1}$ | 53 | B_BCLKX0 | | 54 |
| B_BDX0 | | 55 | DV _{DD} | | 56 |
| V _{SS} | | 57 | B_BFSX0 | | 58 |
| B_BCLKR0 | | 59 | B_BDR0 | | 60 |
| CV _{DD} | | 61 | V _{SS} | | 62 |
| B_BFSR0 | | 63 | R/ \overline{W} | $\overline{HR/W}$ | 64 |
| PPA2 | HCNTL1/HA2 | 65 | PPA3 | HCNTL0/HA3 | 66 |
| SELA/B | PPA18 | 67 | PPD8 | HD8 | 68 |
| PPD9 | HD9 | 69 | PPD10 | HD10 | 70 |
| PPD11 | HD11 | 71 | V _{SS} | | 72 |
| PPA10 | HA10 | 73 | PPA11 | HA11 | 74 |
| DV _{DD} | | 75 | V _{SS} | | 76 |
| PPA12 | HA12 | 77 | PPA13 | HA13 | 78 |
| \overline{HPIRS} | | 79 | HMODE | | 80 |
| B_CLKOUT | | 81 | B_XF | | 82 |
| $\overline{B_RS}$ | | 83 | XIO | | 84 |
| TEST | | 85 | V _{SS} | | 86 |

Table 2–1. Pin Assignments for the 144-Pin Low-Profile Quad Flatpack (Continued)

| SIGNAL NAME (NONMULTIPLEXED) | SIGNAL NAME (MULTIPLEXED) | PIN NO. | SIGNAL NAME (NONMULTIPLEXED) | SIGNAL NAME (MULTIPLEXED) | PIN NO. |
|----------------------------------|------------------------------------|------------|---------------------------------|--|------------|
| CVDD | | 87 | B_BCLKX1 | | 88 |
| B_BDX1 | | 89 | VSS | | 90 |
| B_BFSX1 | | 91 | B_BCLKR1 | | 92 |
| VSS | | 93 | CVDD | | 94 |
| B_BDR1 | | 95 | B_BFSR1 | | 96 |
| B_GPIO0 | B_ROMEN | 97 | B_GPIO1 | | 98 |
| B_GPIO2/ $\overline{\text{BIO}}$ | | 99 | $\overline{\text{IS}}$ | B_GPIO3/B_TOUT | 100 |
| $\overline{\text{B_NMI}}$ | | 101 | $\overline{\text{B_INT1}}$ | | 102 |
| $\overline{\text{B_INT0}}$ | | 103 | PPA17 | HA17 | 104 |
| PPA16 | HA16 | 105 | VSS | | 106 |
| PPA15 | HA15 | 107 | PPA14 | HA14 | 108 |
| PPA7 | HA7 | 109 | PPA6 | HA6 | 110 |
| PPA4 | $\overline{\text{HAS}}/\text{HA4}$ | 111 | DVDD | | 112 |
| PPA5 | HA5 | 113 | PPA1 | $\overline{\text{B_HINT}}/\text{HA1}$ | 114 |
| PPD3 | HD3 | 115 | PPD2 | HD2 | 116 |
| B_BFSR2 | | 117 | B_BDR2 | | 118 |
| VSS | | 119 | CVDD | | 120 |
| B_BCLKR2 | | 121 | B_BFSX2 | | 122 |
| B_BDX2 | | 123 | B_BCLKX2 | | 124 |
| VSS | | 125 | AVDD | | 126 |
| VSSA | | 127 | $\overline{\text{HOLD}}$ | | 128 |
| CLKIN | | 129 | DVDD | | 130 |
| READY | HRDY | 131 | A_BCLKX2 | | 132 |
| CVDD | | 133 | VSS | | 134 |
| A_BCLKR2 | | 135 | A_BDR2 | | 136 |
| A_BFSR2 | | 137 | A_BDX2 | | 138 |
| A_BFSX2 | | 139 | PPD6 | HD6 | 140 |
| PPD4 | HD4 | 141 | PPD5 | HD5 | 142 |
| PPD0 | HD0 | 143 | VSS | | 144 |

2.4 Signal Descriptions

Table 2–2 lists each signal, function, and operating mode(s) grouped by function. See pin assignments section for exact pin locations based on package type.

Table 2–2. Signal Descriptions

| PIN NAME | TYPE† | DESCRIPTION |
|---|--------|--|
| DATA SIGNALS | | |
| PPA18 (MSB) PPA17 PPA16 PPA15 PPA14 PPA13 PPA12 PPA11 PPA10 PPA9 PPA8 PPA7 PPA6 PPA5 PPA4‡§ PPA3 PPA2 PPA1 PPA0 (LSB) | I/O/Z | <p>Parallel port address bus. The DSP can access the external memory locations by way of the external memory interface using PPA[18:0] in external memory interface (EMIF) mode when the XIO pin is logic high. PPA18 is a secondary output function of the SELA/B pin.</p> <p>The PPA[17:0] pins are also multiplexed with the HPI interface. In HPI mode (XIO pin is low), the external address pins PPA[17:0] are used by a host processor for access to the memory map by way of the on-chip HPI. Refer to the Host-Port Interface (HPI) Signals section of this table for details on the secondary functions of these pins.</p> <p>These pins are placed into the high-impedance state when $\overline{\text{OFF}}$ is low.</p> |
| PPD15 (MSB) PPD14 PPD13 PPD12 PPD11 PPD10 PPD9 PPD8 PPD7 PPD6 PPD5 PPD4 PPD3 PPD2 PPD1 PPD0 (LSB) | I/O/Z¶ | <p>Parallel port data bus. The DSP uses this bidirectional data bus to access external memory when the device is in external memory interface (EMIF) mode (the XIO pin is logic high).</p> <p>This data bus is also multiplexed with the 16-bit HPI data bus. When in HPI mode, the bus is used to transfer data between the host processor and internal DSP memory via the HPI. Refer to the HPI section of this table for details on the secondary functions of these pins.</p> <p>The data bus includes bus holders to reduce power dissipation caused by floating, unused pins. The bus holders also eliminate the need for external pullup resistors on unused pins. When the data bus is not being driven by the 5421, the bus holders keep data pins at the last driven logic level. The data bus keepers are disabled at reset and can be enabled/disabled via the BH bit of the BSCR register.</p> <p>These pins are placed into high-impedance state when $\overline{\text{OFF}}$ is low.</p> |

† I = Input, O = Output, S = Supply, Z = High Impedance

‡ This pin has an internal pullup resistor.

§ These pins are Schmitt triggered inputs.

¶ This pin has an internal bus holder controlled by way of the BSCR register in 54x cLEAD core of DSP subsystem A.

This pin is used by Texas Instruments for device testing and should be left unconnected.

|| This pin has an internal pulldown resistor.

Table 2–2. Signal Descriptions (Continued)

| PIN NAME | TYPE† | DESCRIPTION | |
|--|-------|---|---|
| DATA SIGNALS (CONTINUED) | | | |
| A_INT0‡ B_INT0‡ A_INT1‡ B_INT1‡ | I | External user interrupts. A_INT0–B_INT0 are prioritized and are maskable by the interrupt mask register (IMR) and the interrupt mode bit. A_INT1–B_INT1 can be polled and reset by way of the interrupt flag register (IFR). | |
| INITIALIZATION, INTERRUPT, AND RESET OPERATIONS | | | |
| A_NMI§ B_NMI§ | I | Nonmaskable interrupt. NMI is an external interrupt that cannot be masked by way of the INTM or the IMR. When NMI is activated, the processor traps to the appropriate vector location. | |
| A_RS§ B_RS§ | I | Reset. RS causes the digital signal processor (DSP) to terminate execution and causes a reinitialization of the CPU and peripherals. When RS is brought to a high level, execution begins at location 0FF80h of program memory. RS affects various registers and status bits. | |
| XIO | I | The XIO pin is used to configure the parallel port as a host-port interface (HPI mode when XIO pin is low), or as an asynchronous memory interface (EMIF mode when XIO pin is high). NOTE: Because the XIO signal is asynchronous, caution must be taken when changing the state of the XIO pin to ensure the current cycle is properly ended. At device reset, the XIO pin level determines the initialization value of the MP/MC bit (a bit in the processor mode status (PMST) register). Refer to the memory section for details. | |
| GENERAL-PURPOSE I/O PINS | | | |
| A_XF B_XF | O/Z | External flag output (latched software-programmable output-only signal). Bit-addressable. A_XF and B_XF are placed into the high-impedance state when OFF is low. | |
| A_GPIO0 B_GPIO0 | I/O/Z | A_ROMEN B_ROMEN | I General-purpose I/O pins. The secondary function of these pins. In XIO mode, the ROM enable (ROMEN) pins are used to enable the applicable on-chip ROM after reset. |
| A_GPIO1 B_GPIO1 | I/O/Z | General-purpose I/O pins (software-programmable I/O signal). Values can be latched (output) by writing into the GPIO register. The states of GPIO pins (inputs) can be read by reading the GPIO register. The GPIO direction is also programmable by way of the DIRn field in the GPIO register. | |
| A_GPIO2/BIO B_GPIO2/BIO | I/O/Z | General-purpose I/O. These pins can be configured like GPIO0–GPIO1; however, as an input, the pins operate as the traditional branch control bit (BIO). If application code does not perform BIO-conditional instructions, these pins operate as general inputs. | |
| A_GPIO3 (A_TOUT) B_GPIO3 (B_TOUT) | I/O/Z | PRIMARY IOSTRB IS | O When the device is in HPI mode and HMODE = 0 (multiplexed), these pins act according to the general-purpose I/O control register. TOUT bit must be set to “1” to drive the timer output on the pin. IF TOUT = 0, then these pins are general-purpose I/Os. In EMIF mode (XIO = 1), these signals are active during I/O space accesses. |

† I = Input, O = Output, S = Supply, Z = High Impedance

‡ This pin has an internal pullup resistor.

§ These pins are Schmitt triggered inputs.

¶ This pin has an internal bus holder controlled by way of the BSCR register in 54x cLEAD core of DSP subsystem A.

This pin is used by Texas Instruments for device testing and should be left unconnected.

|| This pin has an internal pulldown resistor.

Table 2–2. Signal Descriptions (Continued)

| PIN NAME | TYPE† | DESCRIPTION |
|--|-------|--|
| MEMORY CONTROL SIGNALS | | |
| $\overline{\text{PS}}\ddagger\S$ $\overline{\text{DS}}\ddagger\S$ $\overline{\text{IS}}$ | O/Z | Program space select signal. The $\overline{\text{PS}}$ signal is asserted during external program space accesses. This pin is placed into the high-impedance state when $\overline{\text{OFF}}$ is low. |
| | | This pin is also multiplexed with the HPI, and functions as the $\overline{\text{HDS1}}$ data strobe input signal in HPI mode. Refer to the HPI section of this table for details on the secondary function of this pin. |
| | | Data space select signal. The $\overline{\text{DS}}$ signal is asserted during external data space accesses. This pin is placed into the high-impedance state when $\overline{\text{OFF}}$ is low. |
| | | This pin is also multiplexed with the HPI, and functions as the $\overline{\text{HDS2}}$ data strobe input signal in HPI mode. Refer to the HPI section of this table for details on the secondary function of this pin. |
| $\overline{\text{IOSTRB}}\ddagger\S$ | O/Z | I/O space select signal. The $\overline{\text{IS}}$ signal is asserted during external I/O space accesses. This pin is placed into the high-impedance state when $\overline{\text{OFF}}$ is low. |
| | | This pin is also multiplexed with the general-purpose I/O feature, and functions as the B_GPIO3 (B_TOUT) input/output signal in HPI mode. Refer to the General-Purpose I/O section of this table for details on the secondary function of this pin. |
| $\overline{\text{MSTRB}}\ddagger\S$ | O/Z | Program and data memory strobe (active in EMIF mode). This pin is placed into the high-impedance state when $\overline{\text{OFF}}$ is low. |
| READY | I | Data-ready input signal. READY indicates that the external device is prepared for a bus transaction to be completed. If the device is not ready (READY = 0), the processor waits one cycle and checks READY again. The processor performs the READY detection if at least two software wait states are programmed. |
| $\overline{\text{R/W}}$ | O/Z | This pin is also multiplexed with the HPI, and functions as the host-port data ready (output) in HPI mode. Refer to the HPI section of this table for details on the secondary function of this pin. |
| | | Read/write output signal. $\overline{\text{R/W}}$ indicates transfer direction during communication to an external device. $\overline{\text{R/W}}$ is normally in the read mode (high), unless it is asserted low when the DSP performs a write operation. |
| $\overline{\text{IOSTRB}}$ | O/Z | This pin is placed into the high-impedance state when $\overline{\text{OFF}}$ is low. |
| | | I/O space memory strobe. External I/O space is accessible by the CPU and not the direct memory access (DMA) controller. The DMA has its own dedicated I/O space that is not accessible by the CPU. |
| $\overline{\text{IOSTRB}}$ | O/Z | This pin is also multiplexed with the general-purpose I/O feature, and functions as the A_GPIO3 (A_TOUT) signal in HPI mode. Refer to the General Purpose I/O section of this table for details on the secondary function of this pin. |
| | | This pin is placed into the high-impedance state when $\overline{\text{OFF}}$ is low. |

† I = Input, O = Output, S = Supply, Z = High Impedance

‡ This pin has an internal pullup resistor.

§ These pins are Schmitt triggered inputs.

¶ This pin has an internal bus holder controlled by way of the BSCR register in 54x cLEAD core of DSP subsystem A.

This pin is used by Texas Instruments for device testing and should be left unconnected.

|| This pin has an internal pulldown resistor.

Table 2–2. Signal Descriptions (Continued)

| PIN NAME | TYPE† | DESCRIPTION | |
|--|-------|---|---|
| MEMORY CONTROL SIGNALS (CONTINUED) | | | |
| PPA18 | O/Z | PRIMARY | |
| | | SELA/B | I |
| | | <p>For HPI access (XIO=0), SELA/B is an input. See Table 3–3 for a truth table of SELA/B, HMODE, and XIO pins and functionality.</p> <p>For external memory accesses (XIO=1), SELA/B is multiplexed as output PPA18. See the PPA signal descriptions. These pins are placed into the high-impedance state when $\overline{\text{OFF}}$ is low.</p> | |
| $\overline{\text{HOLD}}\ddagger$ | I | Hold. $\overline{\text{HOLD}}$ is asserted to request control of the address, data, and control lines. When acknowledged, these lines go into the high-impedance state. | |
| $\overline{\text{HOLDA}}$ | O/Z | Hold acknowledge. $\overline{\text{HOLDA}}$ indicates to the external circuitry that the processor is in a hold state and that the address, data, and control lines are in the high-impedance state, allowing them to be available to the external circuitry. $\overline{\text{HOLDA}}$ also goes into the high-impedance state when $\overline{\text{OFF}}$ is low. | |
| CLOCKING SIGNALS | | | |
| A_CLKOUT B_CLKOUT | O/Z | Master clock output signal. CLKOUT cycles at the machine-cycle rate of the CPU. The internal machine cycle is bounded by the falling edges of this signal. The CLKOUT pin can be turned off by writing a "1" to the CLKOFF bit of the PMST register. CLKOUT goes into the high-impedance state when EMU1/ $\overline{\text{OFF}}$ is low. | |
| CLKIN§ | I | Input clock to the device. CLKIN connects to an oscillator circuit/device (PLL). | |
| MULTICHANNEL BUFFERED SERIAL PORT 0, 1, AND 2 SIGNALS | | | |
| A_BCLKR0‡§ B_BCLKR0‡§ A_BCLKR1‡§ B_BCLKR1‡§ A_BCLKR2‡§ B_BCLKR2‡§ | I/O/Z | <p>Receive clocks. BCLKR serves as the serial shift clock for the buffered serial-port receiver. Input from an external clock source for clocking data into the McBSP. When not being used as a clock, these pins can be used as general-purpose I/O by setting RIOEN = 1.</p> <p>BCLKR can be configured as an output by the way of the CLKRM bit in the PCR register. These pins are placed into the high-impedance state when $\overline{\text{OFF}}$ is low.</p> | |
| A_BCLKX0‡§ B_BCLKX0‡§ A_BCLKX1‡§ B_BCLKX1‡§ A_BCLKX2‡§ B_BCLKX2‡§ | I/O/Z | <p>Transmit clocks. Clock signal used to clock data from the transmit register. This pin can also be configured as an input by setting the CLKXM = 0 in the PCR register. BCLKX can be sampled as an input by way of the IN1 bit in the SPC register. When not being used as a clock, these pins can be used as general-purpose I/O by setting XIOEN = 1.</p> <p>These pins are placed into the high-impedance state when $\overline{\text{OFF}}$ is low.</p> | |
| A_BDR0 B_BDR0 A_BDR1 B_BDR1 A_BDR2 B_BDR2 | I | Buffered serial data receive (input) pin. When not being used as data-receive pins, these pins can be used as general-purpose I/O by setting RIOEN = 1. | |

† I = Input, O = Output, S = Supply, Z = High Impedance

‡ This pin has an internal pullup resistor.

§ These pins are Schmitt triggered inputs.

¶ This pin has an internal bus holder controlled by way of the BSCR register in 54x cLEAD core of DSP subsystem A.

This pin is used by Texas Instruments for device testing and should be left unconnected.

|| This pin has an internal pulldown resistor.

Table 2–2. Signal Descriptions (Continued)

| PIN NAME | TYPE† | DESCRIPTION | |
|--|-------|---|-------|
| MULTICHANNEL BUFFERED SERIAL PORT 0, 1, AND 2 SIGNALS (CONTINUED) | | | |
| A_BDX0 B_BDX0 A_BDX1 B_BDX1 A_BDX2 B_BDX2 | O/Z | Buffered serial-port transmit (output) pin. When not being used as data-transmit pins, these pins can be used as general-purpose I/O by setting XIOEN = 1. These pins are placed into the high-impedance state when $\overline{\text{OFF}}$ is low. | |
| A_BFSR0 B_BFSR0 A_BFSR1 B_BFSR1 A_BFSR2 B_BFSR2 | I/O/Z | Frame synchronization pin for buffered serial-port input data. The BFSR pulse initiates the receive-data process over the BDR pin. When not being used as data-receive synchronization pins, these pins can be used as general-purpose I/O by setting RIOEN = 1. These pins are placed into the high-impedance state when $\overline{\text{OFF}}$ is low. | |
| A_BFSX0 B_BFSX0 A_BFSX1 B_BFSX1 A_BFSX2 B_BFSX2 | I/O/Z | Buffered serial-port frame synchronization pin for transmitting data. The BFSX pulse initiates the transmit-data process over the BDX pin. If $\overline{\text{RS}}$ is asserted when BFSX is configured as output, then BFSX is turned into input mode by the reset operation. When not being used as data-transmit synchronization pins, these pins can be used as general-purpose I/O by setting XIOEN = 1. These pins are placed into the high-impedance state when $\overline{\text{OFF}}$ is low. | |
| HOST-PORT INTERFACE (HPI) SIGNALS | | | |
| HA[17:0] | I | PRIMARY | |
| | | PPA[17:0] | O/Z |
| <p>These pins are multiplexed with the external interface pins and are used by the HPI when the subsystem is in HPI mode (XIO = 0, MP/MC = 0). See the PPA signal descriptions. These pins are placed into the high-impedance state when $\overline{\text{OFF}}$ is low.</p> <p>NOTE: HA4 has a pullup and a Schmitt trigger buffer.</p> | | | |
| HD[15:0] | I/O/Z | PRIMARY | |
| | | PPD[15:0] | I/O/Z |
| <p>Parallel bidirectional data bus. These pins are multiplexed with the external interface pins and are used as an HPI interface when XIO = 0.</p> <p>These pins include bus holders to reduce power dissipation caused by floating, unused inputs. The bus holders also eliminate the need for external pullup resistors on unused inputs. In multiplexed address/data mode (HMODE = 0), when the data bus is not being driven by the 5421, the bus holders keep the multiplexed address inputs on these pins at the last logic level driven by the host. The data bus holders are disabled at reset and can be enabled/disabled via the BH bit of the BSCR register.</p> <p>See the PPD signal descriptions. These pins are placed into the high-impedance state when $\overline{\text{OFF}}$ is low.</p> | | | |

† I = Input, O = Output, S = Supply, Z = High Impedance

‡ This pin has an internal pullup resistor.

§ These pins are Schmitt triggered inputs.

¶ This pin has an internal bus holder controlled by way of the BSCR register in 54x cLEAD core of DSP subsystem A.

This pin is used by Texas Instruments for device testing and should be left unconnected.

|| This pin has an internal pulldown resistor.

Table 2–2. Signal Descriptions (Continued)

| PIN NAME | TYPE† | DESCRIPTION | | |
|--|-------|--|-----|--|
| HOST-PORT INTERFACE (HPI) SIGNALS (CONTINUED) | | | | |
| HCNTL0 HCNTL1 | I | PPA3 PPA2 | O/Z | HPI control inputs. Use PPA3 and PPA2 for the HCNTL0 and HCNTL1 values during the HPI HPIC, HPIA, and HPID reads/writes. Only used in multiplexed address/data mode (HMODE = 0). These pins are shared with the external memory interface and are only used by the HPI when the interface is in HPI mode (XIO pin is low). These pins are placed into the high-impedance state when $\overline{\text{OFF}}$ is low. |
| $\overline{\text{HAS}}\ddagger$ | I | PPA4‡§ | O/Z | Address strobe input. Hosts with multiplexed address and data pins require $\overline{\text{HAS}}$ to latch the address in the HPIA register. This signal is only used in HPI multiplexed address/data mode (HMODE pin is low). This pin is shared with the external memory interface and is only used by the HPI when the interface is in HPI mode (XIO pin is low). This pin is placed into the high-impedance state when $\overline{\text{OFF}}$ is low. |
| $\overline{\text{HCS}}\ddagger$ | I | $\overline{\text{MSTRB}}\ddagger$ | O/Z | HPI chip-select signal. This signal must be active during HPI transfers, and can remain active between concurrent transfers. This pin is shared with the external memory interface and is only used by the HPI when the interface is in HPI mode (XIO pin is low). This pin is placed into the high-impedance state when $\overline{\text{OFF}}$ is low. |
| $\overline{\text{HDS1}}\ddagger$ $\overline{\text{HDS2}}\ddagger$ | I | $\overline{\text{PS}}\ddagger$ $\overline{\text{DS}}\ddagger$ | O/Z | HPI data strobes. $\overline{\text{HDS1}}$ and $\overline{\text{HDS2}}$ are driven by the host read and write strobes to control HPI transfers. These pins are shared with the external memory interface and are only used by the HPI when the interface is in HPI mode (XIO pin is low). These pins are placed into the high-impedance state when $\overline{\text{OFF}}$ is low. |
| HR/ $\overline{\text{W}}$ | I | R/ $\overline{\text{W}}$ | O/Z | HPI read/write signal. This signal is used by the host to control the direction of an HPI transfer. This pin is shared with the external memory interface and is only used by the HPI when the interface is in HPI mode (XIO pin is low). This pin is placed into the high-impedance state when $\overline{\text{OFF}}$ is low. |
| HRDY | O/Z | READY | I | HPI data-ready output. The ready output informs the host when the HPI is ready for the next transfer. This pin is shared with the external memory interface and is only used by the HPI when the interface is in HPI mode (XIO pin is low). HRDY is placed into the high-impedance state when $\overline{\text{OFF}}$ is low. |
| $\overline{\text{A_HINT}}$ $\overline{\text{B_HINT}}$ | O/Z | PRIMARY PPA0 PPA1 | O/Z | Host interrupt pin. HPI can interrupt the host by asserting this low. The host can clear this interrupt by writing a "1" to the $\overline{\text{HINT}}$ bit of the HPIC register. Only supported in HPI multiplexed address/data mode (HMODE pin is low). These pins are placed into the high-impedance state when $\overline{\text{OFF}}$ is low. |
| HPIRS§ | I | Host-port interface (HPI) reset pin. This signal resets the host port interface and both subsystems. | | |

† I = Input, O = Output, S = Supply, Z = High Impedance

‡ This pin has an internal pullup resistor.

§ These pins are Schmitt triggered inputs.

¶ This pin has an internal bus holder controlled by way of the BSCR register in 54x cLEAD core of DSP subsystem A.

This pin is used by Texas Instruments for device testing and should be left unconnected.

|| This pin has an internal pulldown resistor.

Table 2–2. Signal Descriptions (Continued)

| PIN NAME | TYPE† | DESCRIPTION |
|--|-------|--|
| HOST-PORT INTERFACE (HPI) SIGNALS (CONTINUED) | | |
| HMODE | I | Host mode select. When this pin is low, it selects the HPI multiplexed address/data mode. The multiplexed address/data mode allows hosts with multiplexed address/data lines access to the HPI registers HPIC, HPIA, and HPID. Host-to-DSP and DSP-to-host interrupts are supported in this mode. When HMODE is high, it selects the HPI nonmultiplexed mode. HPI nonmultiplexed mode allows hosts with separate address/data buses to access the HPI address range by way of the 18-bit address bus and the HPI data (HPID) register via the 16-bit data bus. Host-to-DSP and DSP-to-host interrupts are not supported in this mode. |
| SUPPLY PINS | | |
| AV _{DD} | S | Dedicated power supply that powers the PLL. AV _{DD} = 1.8 V. AV _{DD} can be connected to CV _{DD} . |
| CV _{DD} | S | Dedicated “clean” power supply that powers the core CPUs. CV _{DD} = 1.8 V |
| DV _{DD} | S | Dedicated “dirty” power supply that powers the I/O pins. DV _{DD} = 3.3 V |
| V _{SS} | S | Digital ground. Dedicated ground plane for the device. |
| V _{SSA} | S | Analog ground. Dedicated ground for the PLL. V _{SSA} can be connected to V _{SS} if digital and analog grounds are not separated. |
| TEST PIN | | |
| TEST# | | No connection |
| EMULATION/TEST PINS | | |
| TCK‡§ | I | Standard test clock. This is normally a free-running clock signal with a 50% duty cycle. Changes on the test access port (TAP) of input signals TMS and TDI are clocked into the TAP controller, instruction register, or selected test-data register on the rising edge of TCK. Changes at the TAP output signal (TDO) occur on the falling edge of TCK. |
| TDI‡ | I | Test data input. Pin with an internal pullup device. TDI is clocked into the selected register (instruction or data) on a rising edge of TCK. |
| TDO | O/Z | Test data output. The contents of the selected register is shifted out of TDO on the falling edge of TCK. TDO is in high-impedance state except <u>when</u> the scanning of data is in progress. These pins are placed into high-impedance state when <u>OFF</u> is low. |
| TMS‡ | I | Test mode select. Pin with internal pullup device. This serial control input is clocked into the TAP controller on the rising edge of TCK. |
| <u>TRST</u> | I | Test reset. When high, <u>TRST</u> gives the scan system control of the operations of the device. If <u>TRST</u> is driven low, the device operates in its functional mode and the IEEE 1149.1 signals are ignored. Pin with internal pulldown device. |

† I = Input, O = Output, S = Supply, Z = High Impedance

‡ This pin has an internal pullup resistor.

§ These pins are Schmitt triggered inputs.

¶ This pin has an internal bus holder controlled by way of the BSCR register in 54x cLEAD core of DSP subsystem A.

This pin is used by Texas Instruments for device testing and should be left unconnected.

|| This pin has an internal pulldown resistor.

Table 2-2. Signal Descriptions (Continued)

| PIN NAME | TYPE† | DESCRIPTION |
|--|-------|--|
| EMULATION/TEST PINS (CONTINUED) | | |
| EMU0 | I/O/Z | Emulator interrupt 0 pin. When $\overline{\text{TRST}}$ is driven low, EMU0 must be high for the activation of the EMU1/ $\overline{\text{OFF}}$ condition. When $\overline{\text{TRST}}$ is driven high, EMU0 is used as an interrupt to or from the emulator system and is defined as I/O. |
| EMU1/ $\overline{\text{OFF}}$ | I/O/Z | Emulator interrupt 1 pin. When $\overline{\text{TRST}}$ is driven high, EMU1/ $\overline{\text{OFF}}$ is used as an interrupt to or from the emulator system and is defined as I/O. When $\overline{\text{TRST}}$ transitions from high to low, then EMU1 operates as $\overline{\text{OFF}}$. EMU/ $\overline{\text{OFF}}$ = 0 puts all output drivers into the high-impedance state. Note that $\overline{\text{OFF}}$ is used exclusively for testing and emulation purposes (and not for multiprocessing applications). Therefore, for the $\overline{\text{OFF}}$ condition, the following conditions apply: $\overline{\text{TRST}} = 0$, EMU0 = 1, EMU1 = 0 |

† I = Input, O = Output, S = Supply, Z = High Impedance

‡ This pin has an internal pullup resistor.

§ These pins are Schmitt triggered inputs.

¶ This pin has an internal bus holder controlled by way of the BSCR register in 54x cLEAD core of DSP subsystem A.

This pin is used by Texas Instruments for device testing and should be left unconnected.

|| This pin has an internal pulldown resistor.

3 Functional Overview

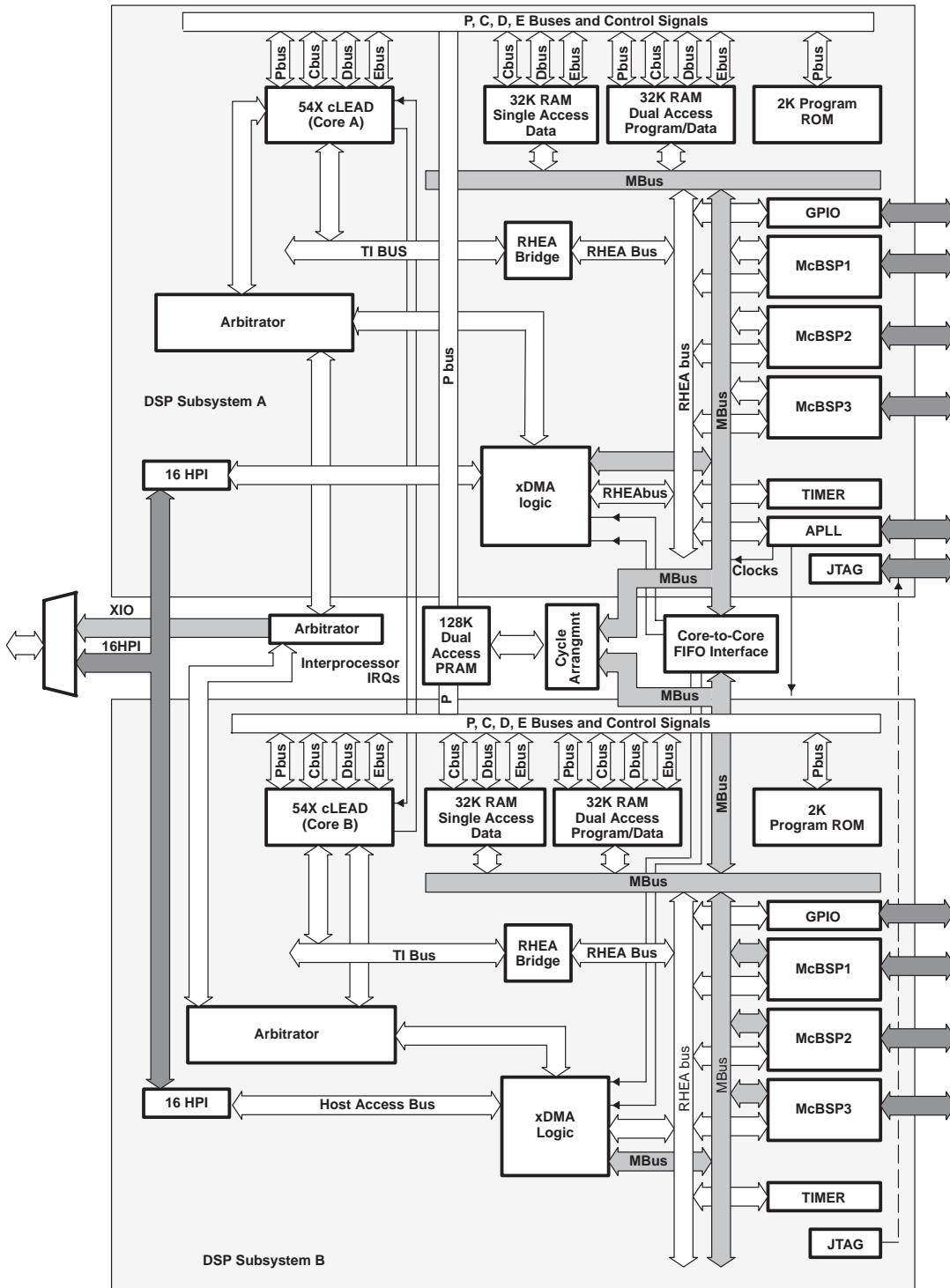


Figure 3–1. 320VC5421 Functional Block Diagram

3.1 Memory

Each 5421 DSP subsystem maintains the peripheral register memory map and interrupt location/priorities of the standard 5420. Figure 3–2 shows the size of the required memory blocks and their link map within the program and data space of the cLEAD core. The total on-chip memory for the 5421 devices is 256K-word data/program.

| Hex | Data | Hex | Program Page 0 | Hex | Program Page 1 | Hex | Program Page 2 | Hex | Program Page 3 | Hex | Program Page n |
|---------|---|---------|--|---------|--|---------|--|---------|--|---------|-----------------------|
| 00 0000 | Memory-Mapped Registers | 00 0000 | Reserved | 01 0000 | Reserved | 02 0000 | Reserved | 03 0000 | Reserved | 0n 0000 | Reserved |
| 00 005F | On-Chip DARAM A/B [§] (32K Words) Prog/Data | 00 005F | On-Chip DARAM A/B [§] (32K Words) Prog/Data (OVLY=1) External (OVLY=0) | 01 005F | On-Chip DARAM A/B [§] (32K Words) Prog/Data (OVLY=1) External (OVLY=0) | 02 005F | On-Chip DARAM A/B [§] (32K Words) Prog/Data (OVLY=1) External (OVLY=0) | 03 005F | On-Chip DARAM A/B [§] (32K Words) Prog/Data (OVLY=1) External (OVLY=0) | 0n 005F | External [‡] |
| 00 0060 | | 00 0060 | | 01 0060 | | 02 0060 | | 03 0060 | | 0n 0060 | |
| 00 7FFF | On-Chip SARAM A/B (32K Words) Data Only (DROM=1) External (DROM=0) | 00 7FFF | On-Chip two-way shared DARAM 0 [¶] (24K Words) Prog Only Shared 0 | 01 7FFF | On-Chip two-way shared DARAM 1 [¶] (32K Words) Prog Only Shared 1 | 02 7FFF | On-Chip two-way shared DARAM 2 [#] (32K Words) Prog Only Shared 2 | 03 7FFF | On-Chip two-way shared DARAM 3 [#] (32K Words) Prog Only Shared 3 | 0n 7FFF | External [‡] |
| 00 8000 | | 00 8000 | | 01 8000 | | 02 8000 | | 03 8000 | | 0n 8000 | |
| 00 DFFF | | 00 DFFF | Reserved | | | | | | | | |
| 00 E000 | | 00 E000 | | | | | | | | | |
| 00 F7FF | | 00 F7FF | | | | | | | | | |
| 00 F800 | | 00 F800 | ROM (ROMEN=1) [†] | | | | | | | | |
| 00 FFFF | | 00 FFFF | | 01 FFFF | | 02 FFFF | | 03 FFFF | | 0n FFFF | |

† ROM enabled after reset.
 ‡ When CPU PMST register bit MP/MC=0 and an address is generated outside the on-chip memory bound or the address reach, i.e., XPC > 3h, access is always external, if XIO = 1. Pages 8–127 are mapped over pages 4–7. When XIO = 1 and MP/MC = 1, program pages 0, 1, 2, and 3 are external. Pages 4–127 are mapped over pages 0–3.
 § On-chip DARAM A and SARAM A are for subsystem A. Likewise, on-chip DARAM B and SARAM B are for subsystem B.
 ¶ On-chip DRAM 0 and DRAM 1 are owned by subsystem A and shared with subsystem B.
 # On-chip DRAM 2 and DRAM 3 are owned by subsystem B and shared with subsystem A.
 NOTES: A. Clearing the ROMEN bit (GPIO[7]) enables an 8K-word block (0E000h – 0FFFFh) of DARAM .
 B. All external accesses require the XIO pin to be high.
 C. CPU I/O space is a single page of 64K words. Access is always external.
 D. All internal memory is divided into 8K blocks.

Figure 3–2. Memory Map Relative to CPU Subsystems A and B

3.1.1 On-Chip Dual-Access RAM (DARAM)

The 5421 subsystems A and B each have 32K 16-bit words of on-chip DARAM (4 blocks of 8K words). Each of these DARAM blocks can be accessed twice per machine cycle. This memory is intended primarily to store data values; however, it can be used to store program as well. At reset, the DARAM is mapped into data memory space. The DARAM can be mapped into program/data memory space by setting the OVLY bit in the processor-mode status (PMST) register of the 54x CPU in each DSP subsystem.

3.1.2 On-Chip Single-Access RAM (SARAM)

The 5421 subsystems A and B each have 32K 16-bit words of on-chip SARAM (4 blocks of 8K words). Each of these SARAM blocks can be accessed once per machine cycle. This memory is intended to store data values only. At reset, the SARAM is disabled. The SARAM can be enabled in data memory space by setting the DROM bit in the PMST register.

3.1.3 On-Chip Two-Way Shared RAM (DARAM)

The 5421 has 128K 16-bit words of on-chip DARAM (16 blocks of 8K words) that is shared between the two DSP subsystems. This memory is intended to store program only. Each subsystem is able to make one instruction fetch from any location in two-way shared memory each cycle. Neither subsystem CPU can write to the two-way shared memory as only the DMA can write to two-way shared memory.

3.1.4 On-Chip Boot ROM

The 5421 subsystems A and B each have 2K 16-bit words of on-chip ROM. This ROM is used for bootloading functions only. Enabling the ROM maps out one 8K-word block of the shared program memory. The ROM can be disabled by clearing bit 7 (ROMEN) of the general-purpose I/O (GPIO) register. Table 3–1 shows the XIO/ROMEN modes. The ROM is enabled or disabled at reset for each subsystem depending on the state of the GPIO0 pin for that subsystem.

Table 3–1. XIO/ROMEN Modes

| XIO | ROMEN/GPIO0 | MODE |
|-----|-------------|-------------------------|
| 0 | x | Fetch internal from RAM |
| 1 | 0 | Fetch external |
| 1 | 1 | ROM enabled |

3.1.5 Extended Program Memory

The program memory space on the 5421 device addresses up to 512K 16-bit words. The 5421 device uses a paged extended memory scheme in program space to allow access of up to 512K of program memory. This extended program memory (each subsystem) is organized into eight pages (0–7), pages 0–3 are internal, pages 4–7 are external, each 64K in length. (Pages 8–127 as defined by the program counter extension register (XPC) are aliases for pages 4–7.) Access to the extended program memory is similar to the 5420. To implement the extended program memory scheme, the 5421 device includes the following feature:

- Two 54x instructions are extended to use the additional two bits in the 5421 device.
 - READA – Read program memory addressed by accumulator A and store in data memory
 - WRITA – Write data to program memory addressed by accumulator A
(Writes not allowed for CPUs to shared program memory)

3.1.6 Program Memory

The program memory is accessible on multiple pages, depending on the XPC value. Within these pages, memory is accessible, depending on the address range.

- Access in the lower 32K of each page is dependent on the state of OVLY.
 - OVLY = 0 – Program memory is accessed externally for all values of XPC.
 - OVLY = 1 – Program memory is accessed from local data/program DARAM for all values of XPC.
- Access in the upper 32K of each page is dependent on the state of MP/ \overline{MC} and the value of XPC.
 - MP/ \overline{MC} = 0 – Program memory is accessed internally from two-way shared DARAM for XPC = 0–3. Program memory is accessed externally for XPC = 4–127.
 - MP/ \overline{MC} = 1 – Program memory is accessed externally for all values of XPC.

3.1.7 Data Memory

The data memory space is a single page of 64K. Access is dependent on the address range. Access in the lower 32K of data memory is always from local DARAM.

Access in the upper 32K of data memory is dependent on the state of DROM.

- DROM = 0 – Data memory is accessed externally
- DROM = 1 – Data memory is accessed internally from local SARAM

3.1.8 I/O Memory

The I/O space is a single page of 64K. Access is always external.

When XIO = 0 and an access to external memory is attempted, any write is ignored and any read is an unknown value.

3.2 Multicore Reset Signals

The 5421 device includes three reset signals: $\overline{A_RS}$, $\overline{B_RS}$, and \overline{HPIRS} . The $\overline{A_RS}$ and $\overline{B_RS}$ pins function as the CPU reset signal for subsystem A and subsystem B, respectively. These signals reset the state of the CPU registers and upon release, initiate the reset function. Additionally, the $\overline{A_RS}$ signal resets the on-chip PLL and initializes the CLKMD register to bypass mode.

The HPI reset signal (\overline{HPIRS}) places the HPI peripheral into a reset state. It is necessary to wait three clock cycles after the rising edge of \overline{HPIRS} before performing an HPI access. The \overline{HPIRS} signal also resets the PLL by turning off the PLL and initializing the CLKMD register to bypass mode.

3.3 Bootloader

The on-chip bootloader is used to automatically transfer user code from an external source to anywhere in program memory after reset. The XIO pin is sampled during a hardware reset and the results indicate the operating mode as shown in Table 3–2.

Table 3–2. Bootloader Operating Modes

| XIO | AFTER RESET |
|-----|---|
| 0 | <p>HPI mode, bootload is controlled by host. The external host holds the 5421 in reset while it loads the on-chip memory of one or both subsystems as determined by the SELA/B pin.</p> <p>The host can release the 5421 from reset by either of the following methods:</p> <ol style="list-style-type: none"> 1. If the $\overline{A_RS/B_RS}$ pins are held low while \overline{HPIRS} transitions from low to high, the subsystem cores reset will be controlled by the $\overline{A_RS/B_RS}$ pins. When the host has finished downloading code, it drives $\overline{A_RS/B_RS}$ high to release the cores from reset. 2. If the $\overline{A_RS/B_RS}$ pins are held high while \overline{HPIRS} transitions from low to high, the subsystems stay in reset until a HPI data write to address 0x2F occurs. This means the host can download code to subsystem A and then release core A from reset by writing any data to core A address 0x2F via the HPI. The host can then repeat the sequence for core B. This mode allows the host to control the 5421 reset without additional hardware. |
| 1 | XIO mode. ROM is mapped in, if ROMEN pin = 1 during reset. |

The 5421 bootloader provides the following options for the source of code to download:

- Parallel from 8-bit or 16-bit-wide EPROM
- Serial boot from McBSPs, 8-bit mode

GPIO register bit 7 (ROMEN) is used to enable/disable the ROM after reset. The ROMEN bit reflects the status of the ROMEN/GPIO0 pin for each core. ROMEN = 1 indicates that the ROM and the 8K-word program memory block (00 E000h–00 FFFFh) are not available for a CPU write. When ROMEN = 0, this 8K-word program memory is available and the ROM is disabled.

A combination of interrupt flags and the bit values of an external memory location determine the selection of the various boot options.

3.4 External Interface (XIO)

The external interface (XIO) supports the 5421 master boot modes and other external accesses. Its features include:

- Multiplexed with the HPI pins
- Selection of XIO or HPI mode is determined by a dedicated pin (XIO)
- Provides 512K words of external program space, 64K words of external data space, and 64K words of external I/O space.
- Different boot modes are selectable by the XIO, HMODE, and $\overline{A_RS/B_RS}$ pins.
- After reset, the control register bit ROMEN is always preset to 1.

While XIO = 0 during reset, host HPI mode is on, the host sees all RAM, and ROM is disabled. A host write to 002Fh releases the CPUs from reset; the 002Fh write by the host clears the ROMEN bit in the GPIO register.

While XIO = 1 and ROMEN = 1 during reset, the CPU starts from ROM (0FF80h) to do boot selection. After branching to non-ROM area, the code changes the ROMEN bit to enable the RAM area occupied by ROM. While XIO = 1 and ROMEN = 0 during reset, the CPU starts from external (0FF80h) to do boot selection.

Table 3–3 provides a complete description of HMODE, SELA/B, and XIO pin functionality.

Table 3–3. XIO/HPI Modes

| HMODE | SELA/B | HPI MODES (XIO = 0) | XIO MODES (XIO = 1) |
|-------|--------|--|--|
| 0 | 0 | HPI muxed address/data subsystem A slave to host | SELA/B pin is multiplexed as PPA18 output. |
| 0 | 1 | HPI muxed address/data subsystem B slave to host | SELA/B pin is multiplexed as PPA18 output. |
| 1 | 0 | HPI non-muxed address/data subsystem A slave to host | SELA/B pin is multiplexed as PPA18 output. |
| 1 | 1 | HPI non-muxed address/data subsystem B slave to host | SELA/B pin is multiplexed as PPA18 output. |

3.5 On-Chip Peripherals

All the 54x devices have the same CPU structure; however, they have different on-chip peripherals connected to their CPUs. The on-chip peripheral options provided are:

- Software-programmable wait-state generator
- Programmable bank-switching
- Parallel I/O ports
- Multichannel buffered serial ports (McBSPs)
- A hardware timer
- A software-programmable clock generator using a phase-locked loop (PLL)

3.5.1 Software-Programmable Wait-State Generators

The software-programmable wait-state generator can be used to extend external bus cycles up to fourteen machine cycles to interface with slower off-chip memory and I/O devices. The software wait-state register (SWWSR) controls the operation of the wait-state generator. The SWWSR of a particular DSP subsystem (A or B) is used for the external memory interface, depending on the state of the xDMA/XIO arbitration logic (see Direct Memory Access (DMA) Controller section 3.8 and Table 3–4. The 14 least significant bits (LSBs) of the SWWSR specify the number of wait states (0–7) to be inserted for external memory accesses to five separate address ranges. This allows a different number of wait states for each of the five address ranges.

Additionally, the software wait-state multiplier (SWSM) bit of the software wait-state control register (SWCR) defines a multiplication factor of 1 or 2 for the number of wait states. At reset, the wait-state generator is initialized to provide seven wait states on all external memory accesses. The SWWSR bit fields are shown in Figure 3–3 and described in Table 3–4.

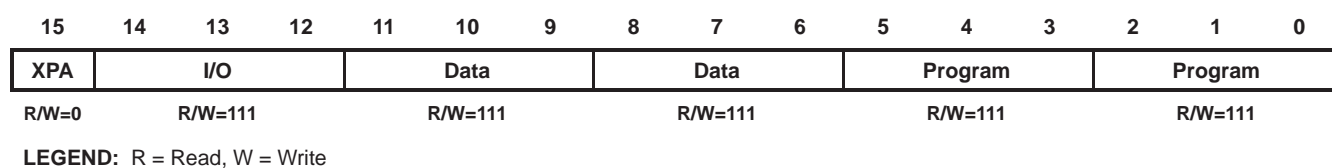
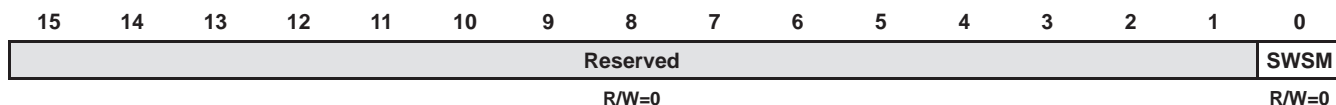


Figure 3–3. Software Wait-State Register (SWWSR) [Memory-Mapped Register (MMR) Address 0028h]

Table 3–4. Software Wait-State Register (SWWSR) Bit Fields

| BIT NO. | BIT NAME | RESET VALUE | FUNCTION |
|---------|----------|-------------|---|
| 15 | XPA | 0 | Extended program address control bit. XPA is used in conjunction with the program space fields (bits 0 through 5) to select the address range for program space wait states. |
| 14–12 | I/O | 1 | I/O space. The field value (0–7) corresponds to the base number of wait states for I/O space accesses within addresses 0000–FFFFh. The SWSM bit of the SWCR defines a multiplication factor of 1 or 2 for the base number of wait states. |
| 11–9 | Data | 1 | Upper data space. The field value (0–7) corresponds to the base number of wait states for external data space accesses within addresses 8000–FFFFh. The SWSM bit of the SWCR defines a multiplication factor of 1 or 2 for the base number of wait states. |
| 8–6 | Data | 1 | Lower data space. The field value (0–7) corresponds to the base number of wait states for external data space accesses within addresses 0000–7FFFh. The SWSM bit of the SWCR defines a multiplication factor of 1 or 2 for the base number of wait states. |
| 5–3 | Program | 1 | Upper program space. The field value (0–7) corresponds to the base number of wait states for external program space accesses within the following addresses: <input type="checkbox"/> XPA = 0: x8000–xFFFFh <input type="checkbox"/> XPA = 1: The upper program space bit field has no effect on wait states. The SWSM bit of the SWCR defines a multiplication factor of 1 or 2 for the base number of wait states. |
| 2–0 | Program | 1 | Program space. The field value (0–7) corresponds to the base number of wait states for external program space accesses within the following addresses: <input type="checkbox"/> XPA = 0: x0000–x7FFFh <input type="checkbox"/> XPA = 1: 00000–3FFFFh The SWSM bit of the SWCR defines a multiplication factor of 1 or 2 for the base number of wait states. |

The software wait-state multiplier bit of the software wait-state control register (SWCR) is used to extend the base number of wait states selected by the SWWSR. The SWCR bit fields are shown in Figure 3–4 and described in Table 3–5.



LEGEND: R = Read, W = Write

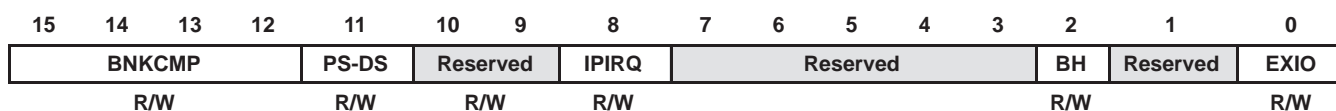
Figure 3–4. Software Wait-State Control Register (SWCR) [MMR Address 002Bh]

Table 3–5. Software Wait-State Control Register (SWCR) Bit Fields

| PIN NO. | PIN NAME | RESET VALUE | FUNCTION |
|---------|----------|-------------|--|
| 15–1 | Reserved | 0 | These bits are reserved and are unaffected by writes. |
| 0 | SWSM | 0 | Software wait-state multiplier. Used to multiply the number of wait states defined in the SWWSR by a factor of 1 or 2. <input type="checkbox"/> SWSM = 0: wait-state base values are unchanged (multiplied by 1). <input type="checkbox"/> SWSM = 1: wait-state base values are multiplied by 2 for a maximum of 14 wait states. |

3.5.2 Programmable Bank-Switching

Programmable bank-switching can be used to insert one cycle automatically when crossing memory-bank boundaries inside program memory or data memory space. One cycle can also be inserted when crossing from program-memory space to data-memory space (54x) or one program memory page to another program memory page. This extra cycle allows memory devices to release the bus before other devices start driving the bus, thereby avoiding bus contention. The size of the memory bank for the bank-switching is defined by the bank-switching control register (BSCR), as shown in Figure 3–5. The BSCR of a particular DSP subsystem (A or B) is used for the external memory interface based on the xDMA/XIO arbitration logic. The BSCR bit fields are described in Table 3–6.



LEGEND: R = Read, W = Write

Figure 3–5. BSCR Register Bit Layout for Each DSP Subsystem

Table 3–6. BSCR Register Bit Functions for Each DSP Subsystem

| BIT NO. | BIT NAME | RESET VALUE | FUNCTION |
|---------|----------|-------------|--|
| 15–12 | BNKCMP | 1111 | Bank compare. BNKCMP determines the external memory-bank size. BNKCMP is used to mask the four most significant bits (MSBs) of an address. For example, if BNKCMP = 1111b, the four MSBs (bits 12–15) are compared, resulting in a bank size of 4K words. Bank sizes of 4K words to 64K words are allowed. |
| 11 | PS-DS | 1 | Program read – data read access. PS-DS inserts an extra cycle between consecutive accesses of program read and data read or data read and program read. PS-DS = 0 No extra cycles are inserted by this feature. PS-DS = 1 One extra cycle is inserted between consecutive data and program reads. |
| 10–9 | Reserved | 0 | These bits are reserved and are unaffected by writes. |
| 8 | IPIRQ | 0 | The IPIRQ bit is used to send an interprocessor interrupt to the other subsystem. IPIRQ=1 sends the interrupt. IPIRQ must be cleared before subsequent interrupts can be made. Refer to the interrupts section for more details. |
| 7–3 | Reserved | 0 | These bits are reserved and are unaffected by writes. |
| 2 | BH | 0 | Bus holder. BH controls the bus holder feature: BH is cleared to 0 at reset. BH = 0 The bus holder is disabled. BH = 1 The bus holder is enabled. When not driven, PPD[15:0] pins are held at the previous logic level. |
| 1 | Reserved | 0 | This bit is reserved and is unaffected by writes. |
| 0 | EXIO | 0 | External bus interface off. The EXIO bit controls the external bus-off function. EXIO = 0 The external bus interface functions as usual. EXIO = 1 The address bus, data bus, and control signals become inactive after completing the current bus cycle. Note that the DROM, $\overline{MP/MC}$, and OVLY bits in the PMST and the HM bit of ST1 cannot be modified when the interface is disabled. |

3.5.3 Parallel I/O Ports

The 5421 has a total of 64K words of I/O port address space. These ports can be addressed by PORTR and PORTW. The \overline{IS} signal indicates the read/write access through an I/O port. The devices can interface easily with external devices through the I/O ports while requiring minimal off-chip address-decoding logic. The SELA/B pin selects which subsystem is accessing the external I/O space.

3.6 16-Bit Bidirectional Host-Port Interface (HPI16)

The HPI16 is an enhanced 16-bit version of the TMS320C54x™ DSP 8-bit host-port interface (HPI). The HPI16 is designed to allow a 16-bit host to access the DSP on-chip memory, with the host acting as the master of the interface.

3.6.1 HPI16 Memory Map

Figure 3–6 illustrates the available memory accessible by the HPI. Neither the CPU nor DMA I/O spaces can be accessed using the host-port interface.

| Hex | Page 0 | Hex | Page 1 | Hex | Page 2 | Hex | Page 3 |
|--------------------|--|--------------------|--|--------------------|--|--------------------|--|
| 00 0000 | Reserved | 01 0000 | | 02 0000 | Reserved | 03 0000 | |
| 00 001F 00 0020 | McBSP DXR/DRR MMRegs Only | | | 02 001F 02 0020 | McBSP DXR/DRR MMRegs Only | | |
| 00 005F 00 0060 | On-Chip DARAM A (32K Words) Prog/Data | | On-Chip Two-Way Shared DARAM 0 (32K Words) Program Only | 02 005F 02 0060 | On-Chip DARAM B (32K Words) Prog/Data | | On-Chip Two-Way Shared DARAM 2 (32K Words) Program Only |
| 00 7FFF 00 8000 | Subsystem A | 01 7FFF 01 8000 | Shared 0 | 02 7FFF 02 8000 | Subsystem B | 03 7FFF 03 8000 | Shared 2 |
| | On-Chip SARAM A (32K Words) Data Only | | On-Chip Two-Way Shared DARAM 1 (32K Words) Program Only | | On-Chip SARAM B (32K Words) Data Only | | On-Chip Two-Way Shared DARAM 3 (32K Words) Program Only |
| 00 FFFF | Subsystem A | 01 FFFF | Shared 1 | 02 FFFF | Subsystem B | 03 FFFF | Shared 3 |

- NOTES:
- A. All local memory is available to the HPI
 - B. The encoder maps CPU A Data Page 0 into the HPI Page 0. CPU B Data Page 0 is mapped into the HPI Page 2. Pages 1 and 3 are the on-chip shared program memory.
 - C. In pages 00 and 02, in the range of 0020–005F, only the following memory mapped registers are accessible: 20,21,30,31,40,41 (read only), 22,23,32,33,42,43 (write only).

Figure 3–6. Memory Map Relative to Host-Port Interface HPI16

3.6.2 HPI Features

Some of the features of the HPI16 include:

- 16-bit bidirectional data bus
- Multiple data strobes and control signals to allow glueless interfacing to a variety of hosts
- Multiplexed and nonmultiplexed address/data modes
- 18-bit address bus used in nonmultiplexed mode to allow access to all internal memory (including internal extended address pages)
- 18-bit address register used in multiplexed mode. Includes address autoincrement feature for faster accesses to sequential addresses
- Interface to on-chip DMA module to allow access to entire internal memory space
- HRDY signal to hold off host accesses due to DMA latency
- Control register available in multiplexed mode only. Accessible by either host or DSP to provide host/DSP interrupts, extended addressing, and data prefetch capability
- Maximum data rate of 33 megabytes per second (MBps) at 100-MHz DSP clock rate (no other DMA channels active)

The HPI16 acts as a slave to a 16-bit host processor and allows access to the on-chip memory of the DSP. There are two modes of operation as determined by the HMODE signal: *multiplexed* mode and *nonmultiplexed* mode.

3.6.3 HPI Multiplexed Mode

In *multiplexed* mode, HPI16 operation is very similar to that of the standard 8-bit HPI, which is available with other C54x™ DSP products. A host with a multiplexed address/data bus can access the HPI16 data register (HPID), address register (HPIA), or control register (HPIC) via the HD bidirectional data bus. The host initiates the access with the strobe signals ($\overline{\text{HDS1}}$, $\overline{\text{HDS2}}$, $\overline{\text{HCS}}$) and controls the type of access with the HCNTL, $\overline{\text{HR}/\overline{\text{W}}}$, and $\overline{\text{HAS}}$ signals. The DSP can interrupt the host via the $\overline{\text{HINT}}$ signal, and can stall host accesses via the HRDY signal.

3.6.4 Host/DSP Interrupts

In *multiplexed* mode, the HPI16 offers the capability for the host and DSP to interrupt each other through the HPIC register.

For host-to-DSP interrupts, the host must write a “1” to the DSPINT bit of the HPIC register. This generates an interrupt to the DSP. This interrupt can also be used to wake the DSP from any of the IDLE 1,2, or 3 states. Note that the DSPINT bit is always read as “0” by both the host and DSP. The DSP cannot write to this bit (see Figure 3–7).

For DSP-to-host interrupts, the DSP must write a “1” to the $\overline{\text{HINT}}$ bit of the HPIC register to interrupt the host via the $\overline{\text{HINT}}$ pin. The host acknowledges and clears this interrupt by also writing a “1” to the $\overline{\text{HINT}}$ bit of the HPIC register. Note that writing a “0” to the $\overline{\text{HINT}}$ bit by either host or DSP has no effect.

3.6.5 Emulation Considerations

The HPI16 can continue operation even when the DSP CPU is halted due to debugger breakpoints or other emulation events.

3.6.6 HPI Nonmultiplexed Mode

In *nonmultiplexed* mode, a host with separate address/data buses can access the HPI16 data register (HPID) via the HD 16-bit bidirectional data bus, and the address register (HPIA) via the 18-bit HA address bus. The host initiates the access with the strobe signals ($\overline{\text{HDS1}}$, $\overline{\text{HDS2}}$, $\overline{\text{HCS}}$) and controls the direction of the access with the $\overline{\text{HR}/\overline{\text{W}}}$ signal. The HPI16 can stall host accesses via the HRDY signal. Note that the HPIC register is not available in *nonmultiplexed* mode since there are no HCNTL signals available. All host accesses initiate a DMA read or write access. Figure 3–7 shows a block diagram of the HPI16 in *nonmultiplexed* mode.

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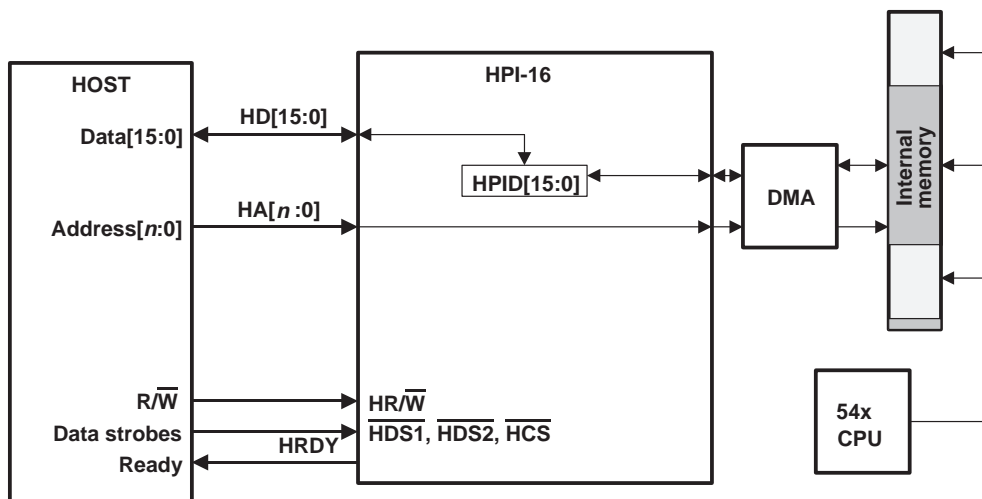


Figure 3–7. Interfacing to the HPI-16 in Non-Multiplexed Mode

3.6.7 Other HPI16 System Considerations

3.6.7.1 Operation During IDLE

The HPI16 can continue to operate during IDLE1 or IDLE2 by using special clock management logic that turns on relevant clocks to perform a synchronous memory access, and then turns the clocks back off to save power. The DSP CPU does not wake up from the IDLE mode during this process.

3.6.7.2 Downloading Code During Reset

The HPI16 can download code while the DSP is in reset. However, the system provides a pin ($\overline{\text{HPIRS}}$) that provides a way to take the HPI16 module out of reset while leaving the DSP in reset. The maximum HPI16 data rate is 33 MBps assuming no other DMA activity (100-MIPS DSP subsystem).

3.6.7.3 Performance Issues

On the 5421, the use of SELA/B is optional for access to all on-chip memory. However, with both the 5420 and 5421 implementation using two separate subsystems (subchips), the SELA/B pin is used to select the specific HPI16 used to access memory.

| SELA/B PIN | SUBSYSTEM |
|------------|-----------|
| 0 | A |
| 1 | B |

Accesses to memory contained inside the same subsystem as the selected HPI16 will be faster. For accesses to an HPI16 in a subsystem different than the memory being addressed, reads take an additional six cycles and writes an extra five cycles. Therefore, for performance reasons, it is best to additionally decode SELA/B.

3.7 Multichannel Buffered Serial Port (McBSP)

The 5421 device provides high-speed, full-duplex serial ports that allow direct interface to other C54x/LC54x devices, codecs, and other devices in a system. There are six multichannel buffered serial ports (McBSPs) on board (three per subsystem).

The McBSP provides:

- Full-duplex communication
- Double-buffer data registers, which allow a continuous data stream
- Independent framing and clocking for receive and transmit

In addition, the McBSP has the following capabilities:

- Direct interface to:
 - T1/E1 framers
 - MVIP switching-compatible and ST-BUS compliant devices
 - IOM-2 compliant device
 - AC97-compliant device
 - Serial peripheral interface (SPI)
- Multichannel transmit and receive of up to 128 channels
- A wide selection of data sizes, including: 8, 12, 16, 20, 24, or 32 bits
- μ -law and A-law companding
- Programmable polarity for both frame synchronization and data clocks
- Programmable internal clock and frame generation

The 5421 McBSPs have been enhanced to provide more flexibility in the choice of the sample rate generator input clock source. On previous TMS320C5000™ DSP platform devices, the McBSP sample rate input clock can be driven from one of two possible choices: the internal CPU clock, or the external CLKS pin. However, most C5000™ DSP devices have only the internal CPU clock as a possible source because the CLKS pin is not implemented on most device packages.

To accommodate applications that require an external reference clock for the sample rate generator, the 5421 McBSPs allow either the receive clock pin (BCLKR) or the transmit clock pin (BCLKX) to be configured as the input clock to the sample rate generator. This enhancement is enabled through two register bits: pin control register (PCR) bit 7 – enhanced sample clock mode (SCLKME), and sample rate generator register 2 (SRGR2) bit 13 – McBSP sample rate generator clock mode (CLKSM). SCLKME is an addition to the PCR contained in the McBSPs on previous C5000 devices. The new bit layout of the PCR is shown in Figure 3–8. For a description of the remaining bits, see *TMS320C54x DSP Reference Set, Volume 5: Enhanced Peripherals* (literature number SPRU302).

| | | | | | | | |
|----------|-----------|---------|---------|-------|-------|-------|-------|
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| Reserved | | XIOEN | RIOEN | FSXM | FSRM | CLKXM | CLKRM |
| R,+0 | | RW,+0 | RW,+0 | RW,+0 | RW,+0 | RW,+0 | RW,+0 |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| SCLKME | CLKS_STAT | DX_STAT | DR_STAT | FSXP | FSRP | CLKXP | CLKRP |
| RW,+0 | R,+0 | R,+0 | R,+0 | RW,+0 | RW,+0 | RW,+0 | RW,+0 |

Note: R = Read, W = Write, +0 = Value at reset

Figure 3–8. Pin Control Register (PCR)

The selection of the sample rate generator (SRG) clock input source is made by the combination of the CLKSM and SCLKME bit values as shown in Table 3–7.

Table 3–7. Sample Rate Generator Clock Source Selection

| SCLKME | CLKSM | SRG Clock Source |
|--------|-------|---------------------------------------|
| 0 | 0 | CLKS (not available as a pin on 5421) |
| 0 | 1 | CPU clock |
| 1 | 0 | BCLKR pin |
| 1 | 1 | BCLKX pin |

When either of the bidirectional pins, BCLKR or BCLKX, is configured as the clock input, its output buffer is automatically disabled. For example, with SCLKME = 1 and CLKSM = 0, the BCLKR pin is configured as the SRG input. In this case, both the transmitter and receiver circuits can be synchronized to the SRG output by setting the PCR bits (9:8) for CLKXM = 1 and CLKRM = 1. However, the SRG output is only driven onto the BCLKX pin because the BCLKR output is automatically disabled.

The McBSP supports independent selection of multiple channels for the transmitter and receiver. When multiple channels are selected, each frame represents a time-division multiplexed (TDM) data stream. In using time-division multiplexed data streams, the CPU may only need to process a few of them. Thus, to save memory and bus bandwidth, multichannel selection allows independent enabling of particular channels for transmission and reception. Up to a maximum of 128 channels in a bit stream can be enabled or disabled.

The 5421 McBSPs have two working modes that are selected by setting the RMCME and XMCME bits in the multichannel control registers (MCR1x and MCR2x, respectively). See Figure 3–9 and Figure 3–10. For a description of the remaining bits, see *TMS320C54x DSP Reference Set, Volume 5: Enhanced Peripherals* (literature number SPRU302).

- In the first mode, when RMCME = 0 and XMCME = 0, there are two partitions (A and B), with each containing 16 channels as shown in Figure 3–9 and Figure 3–10. This is compatible with the McBSPs used in the 5420, where only 32-channel selection is enabled (default).

| | | | | | | | | | | | | | | | |
|----------|----|-------|--------|--------|-------|---|---|---|---|---|---|---|---|-------|---|
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Reserved | | XMCME | XPBBLK | XPABLK | XCBLK | | | | | | | | | XMCM | |
| R,+0 | | RW,+0 | RW,+0 | RW,+0 | R,+0 | | | | | | | | | RW,+0 | |

Note: R = Read, W = Write, +0 = Value at reset; x = McBSP 0,1, or 2

Figure 3–9. Multichannel Control Register 2x (MCR2x)

| | | | | | | | | | | | | | | | |
|----------|----|----|----|----|-------|--------|-------|--------|-------|-------|------|---|------|-------|---|
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Reserved | | | | | RMCME | RPBBLK | | RPABLK | | RCBLK | | | RMCM | | |
| R,+0 | | | | | RW,+0 | | RW,+0 | | RW,+0 | | R,+0 | | | RW,+0 | |

Note: R = Read, W = Write, +0 = Value at reset; x = McBSP 0,1, or 2

Figure 3–10. Multichannel Control Register 1x (MCR1x)

- In the second mode, with RMCME = 1 and XMCME = 1, the McBSPs have 128 channel selection capability. Twelve new registers (RCERCx–RCERHx and XCERCx–XCERHx) are used to enable the 128 channel selection. The subaddresses of the new registers are shown in Table 3–21. These new registers, functionally equivalent to the RCERA0–RCERB1 and XCERA0–XCERB1 registers in the 5420, are used to enable/disable the transmit and receive of additional channel partitions (C,D,E,F,G, and H) in the 128 channel stream. For example, XCERH1 is the transmit enable for channel partition H (channels 112 to 127) of MCBSP1 for each DSP subsystem. See Figure 3–11, Table 3–8, Figure 3–12, and Table 3–9 for bit layout and function of the receive and transmit registers .

| | | | | | | | |
|----------|----------|----------|----------|----------|----------|---------|---------|
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RCERYz15 | RCERYz14 | RCERYz13 | RCERYz12 | RCERYz11 | RCERYz10 | RCERYz9 | RCERYz8 |
| RW,+0 | RW,+0 | RW,+0 | RW,+0 | RW,+0 | RW,+0 | RW,+0 | RW,+0 |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RCERYz7 | RCERYz6 | RCERYz5 | RCERYz4 | RCERYz3 | RCERYz2 | RCERYz1 | RCERYz0 |
| RW,+0 | RW,+0 | RW,+0 | RW,+0 | RW,+0 | RW,+0 | RW,+0 | RW,+0 |

Note: R = Read, W = Write, +0 = Value at reset; y = Partition A,B,C,D,E,F,G, or H; z = McBSP 0,1, or 2

Figure 3–11. Receive Channel Enable Registers Bit Layout for Partitions A to H

Table 3–8. Receive Channel Enable Registers for Partitions A to H

| Bit | Name | Function |
|------|--------------|---|
| 15–0 | RCERYz(15:0) | Receive Channel Enable Register |
| | RCERYz n = 0 | Disables reception of <i>n</i> th channel in partition <i>y</i> . |
| | RCERYz n = 1 | Enables reception of <i>n</i> th channel in partition <i>y</i> . |

Note: y = Partition A,B,C,D,E,F,G, or H; z = McBSP 0,1, or 2; n = bit 15–0

| | | | | | | | |
|----------|----------|----------|----------|----------|----------|---------|---------|
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| XCERYz15 | XCERYz14 | XCERYz13 | XCERYz12 | XCERYz11 | XCERYz10 | XCERYz9 | XCERYz8 |
| RW,+0 | RW,+0 | RW,+0 | RW,+0 | RW,+0 | RW,+0 | RW,+0 | RW,+0 |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| XCERYz7 | XCERYz6 | XCERYz5 | XCERYz4 | XCERYz3 | XCERYz2 | XCERYz1 | XCERYz0 |
| RW,+0 | RW,+0 | RW,+0 | RW,+0 | RW,+0 | RW,+0 | RW,+0 | RW,+0 |

Note: R = Read, W = Write, +0 = Value at reset; y = Partition A,B,C,D,E,F,G, or H; z = McBSP 0,1, or 2

Figure 3–12. Transmit Channel Enable Registers Bit Layout for Partitions A to H

Table 3–9. Transmit Channel Enable Registers for Partitions A to H

| Bit | Name | Function |
|------|--------------|---|
| 15–0 | XCERyz(15:0) | Transmit Channel Enable Register |
| | | XCERyz $n = 0$ Disables transmit of n th channel in partition y . |
| | | XCERyz $n = 1$ Enables transmit of n th channel in partition y . |

Note: y = Partition A,B,C,D,E,F,G, or H; z = McBSP 0,1, or 2; n = bit 15–0

The clock stop mode (CLKSTP) in the McBSP provides compatibility with the serial port interface (SPI) protocol. Clock stop mode works with only single-phase frames and one word per frame. The word sizes supported by the McBSP are programmable for 8-, 12-, 16-, 20-, 24-, or 32-bit operation. When the McBSP is configured to operate in SPI mode, both the transmitter and the receiver operate together as a master or as a slave.

The McBSP is fully static and operates at arbitrarily low clock frequencies. The maximum McBSP multichannel operating frequency on the 5421 is 9 MBps. Nonmultichannel operation is limited to 38 MBps.

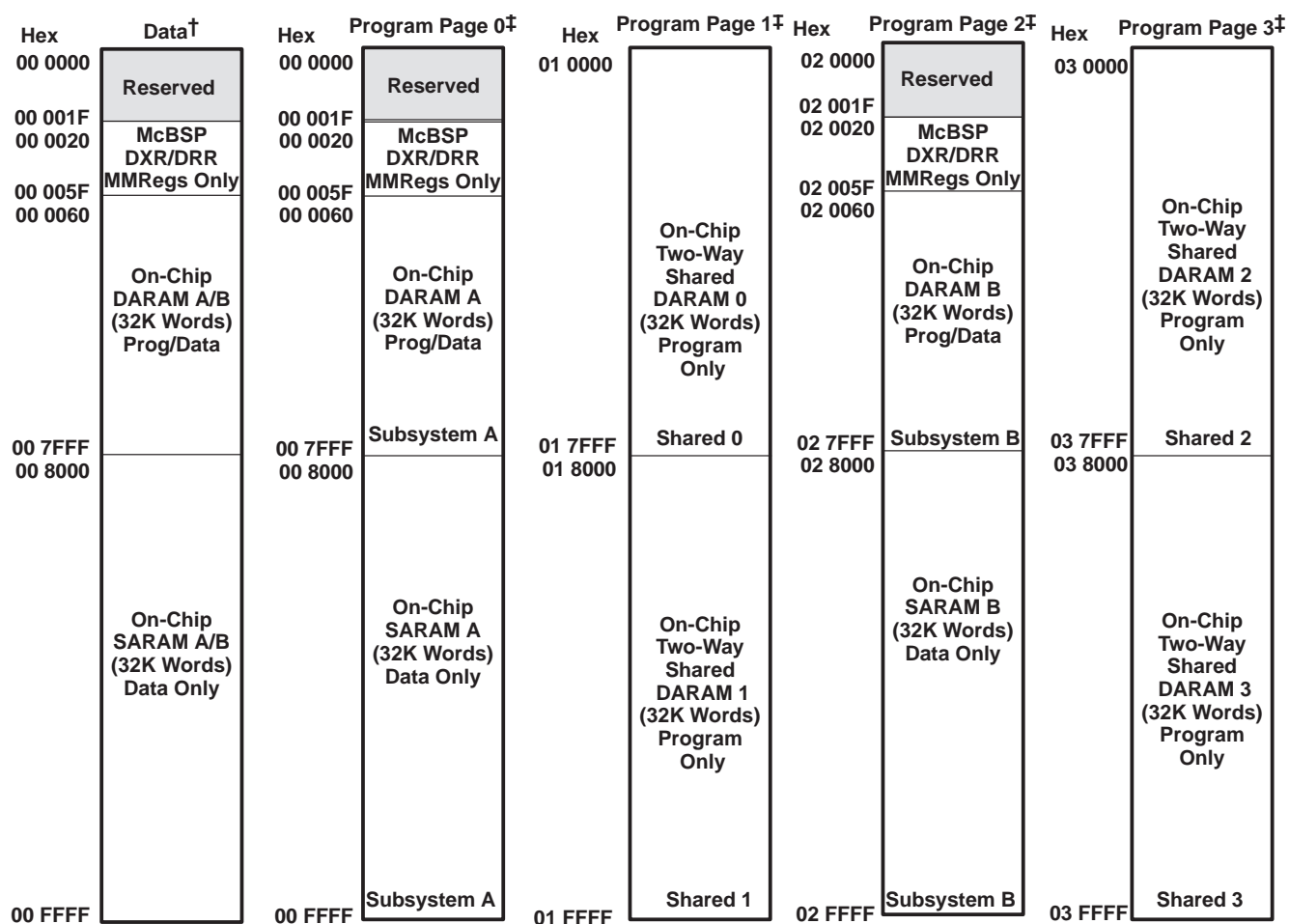
3.7.1 Emulation Considerations

The McBSP can continue operation even when the DSP CPU is halted due to debugger breakpoints or other emulation events.

3.8 Direct Memory Access (DMA) Controller

The 5421 includes two 6-channel direct memory access (DMA) controllers for performing data transfers independent of the CPU, one for each subsystem. The DMA controller controls accesses to off-chip program/data/IO and internal data/program memory. The primary function of the 5421 DMA controller is to provide code overlays and manage data transfers between on-chip memory, the peripherals, and off-chip memory.

In the background of CPU operation, the 5421 DMA allows movement of data between internal and external program/data memory, and internal peripherals, such as the McBSPs and the HPI. Each subsystem has its own independent DMA with six programmable channels, which allows for six different contexts for DMA operation. The HPI has a dedicated auxiliary DMA channel. Figure 3–13 illustrates the memory map accessible by the DMA.



† DMD/DMS = 01

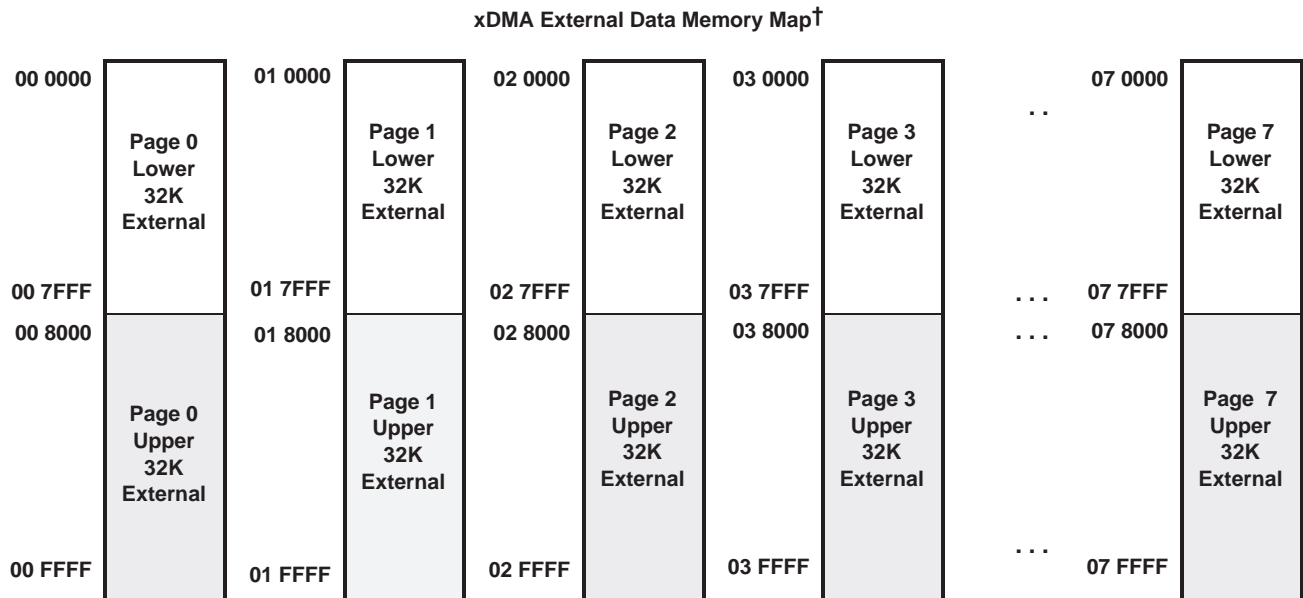
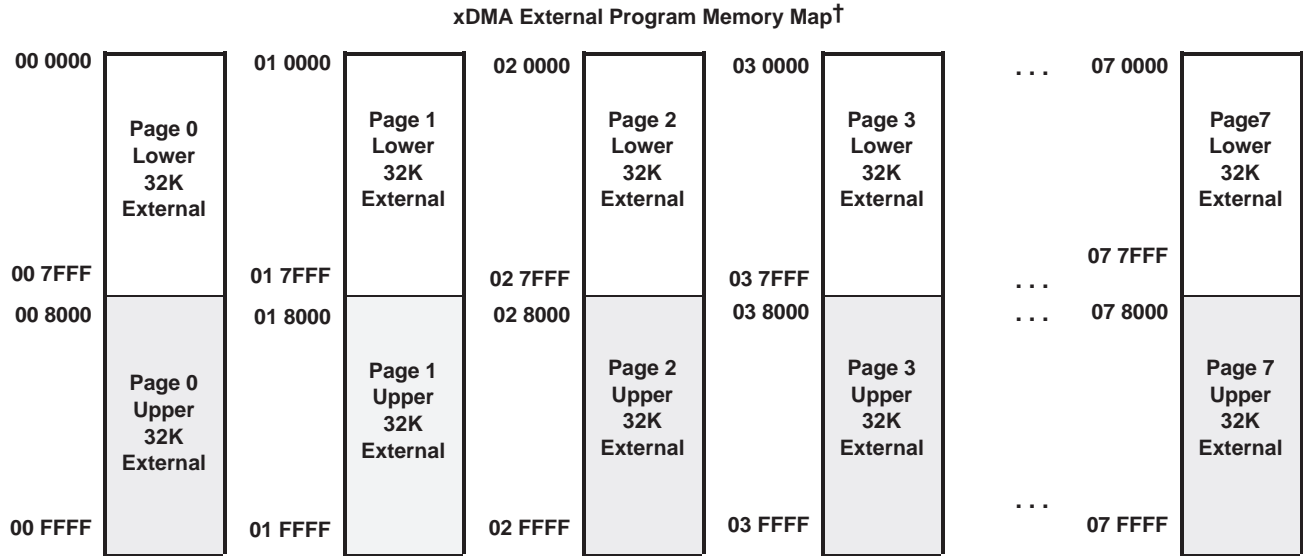
‡ DMD/DMS = 00

NOTES: A. All local memory is available to the DMA.

B. All I/O memory accesses by the DMA (DMD/DMS = 10) are mapped to the core-to-core FIFO.

C. In pages 00 and 02, in the range of 0020–005F, only the following memory mapped registers are accessible: 20,21,30,31,40,41 (read only), 22,23,32,33,42,43 (write only).

Figure 3–13. On-Chip Memory Map Relative to DMA (DLAXS/SLAXS = 0)



† Pages 8 – 127 are overlaid over pages 0 – 7.

Figure 3–14. DMA External Program Memory Map

3.8.1 DMA Controller Features

The 5421 DMA has the following features:

- The DMA operates independently of the CPU.
- The DMA has six channels. The DMA can keep track of the contexts of six independent block transfers.
- Two DMA channels are available for external accesses: one for reads and one for writes.
- The DMA has higher priority than the CPU for internal accesses.
- Each channel has independently programmable priorities.
- Each channel's source and destination address registers include configurable indexing modes. The address can be held constant, postincremented, postdecremented, or adjusted by a programmable value.
- For internal accesses, each read or write transfer can be initialized by selected events.
- Supports 32-bit transfers for internal accesses only.
- Single-word (16-bit) transfers are supported for external accesses.
- The DMA does not support transfers from peripherals to external memory.
- The DMA does not support transfers from external memory to the peripherals.
- The DMA does not support external to external transfers.

A 16-bit DMA transfer requires four CPU clock cycles to complete — two cycles for reads and two cycles for writes. This gives a maximum DMA throughput of 50 MBps. Since the DMA controller shares the DMA bus with the HPI module, the DMA access rate is reduced when the HPI is active.

3.8.2 DMA Accesses to External Memory

The 5421 DMA supports external accesses to extended program, extended data, and extended I/O memory. These overlay pages are only visible to the DMA controller. A maximum of two channels (one for reads, one for writes) per DMA can be used for external memory accesses. The DMA external accesses require 9 cycles (minimum) for external writes and 13 cycles (minimum) for external reads.

The control of the bus is arbitrated between the two CPUs and the two DMAs. While one DMA or CPU is in control of the external bus, the other three components will be held off (via wait-states) until the current transfer is complete. The DMA takes precedence over XIO requests. The $\overline{\text{HOLD}}/\text{HOLDA}$ feature of the 5421 affects external CPU transfers, as well as external DMA transfers. When an external processor asserts the $\overline{\text{HOLD}}$ pin to gain control of the memory interface, the $\overline{\text{HOLDA}}$ signal is not asserted until all pending DMA transfers are completed. To prevent a DMA from blocking out the CPUs or $\overline{\text{HOLD}}/\text{HOLDA}$ feature from accessing the external bus, uninterrupted burst transfers are **not** supported by the DMAs. Subsequently, CPU and DMA arbitration testing is performed for each external bus cycle, regardless of the bus activity. With the completion of each block, the highest priority will be swapped.

For arbitration at the DSP subsystem level, the DMA requests (DMA_REQ_A or DMA_REQ_B) from either DMA will be sent to both CPUs as shown in Figure 3–15. Regardless of which CPU controls the external pin interface (XIO), both CPUs must send a grant (GRANT_A, GRANT_B) for control of the bus to be released to the DMAs.

Arbitration between CPUs is done using a request/grant scheme. Prior to accessing XIO of one of the CPUs, software is responsible for asserting a request for access to the device pins and polling grant status until the pins are granted to the requestor. If both CPUs request the bus simultaneously, subsystem A is granted priority. For details on memory-mapped register bits pertaining to CPU XIO arbitration, see the general-purpose I/O control register bits [6:4] (CORE SEL, XIO GRANT, XIO REQ) in Table 3–14.

At reset, the default is that subsystem A has access to the device pins. Accesses without a grant will be allowed, but do not show up on the device pins.

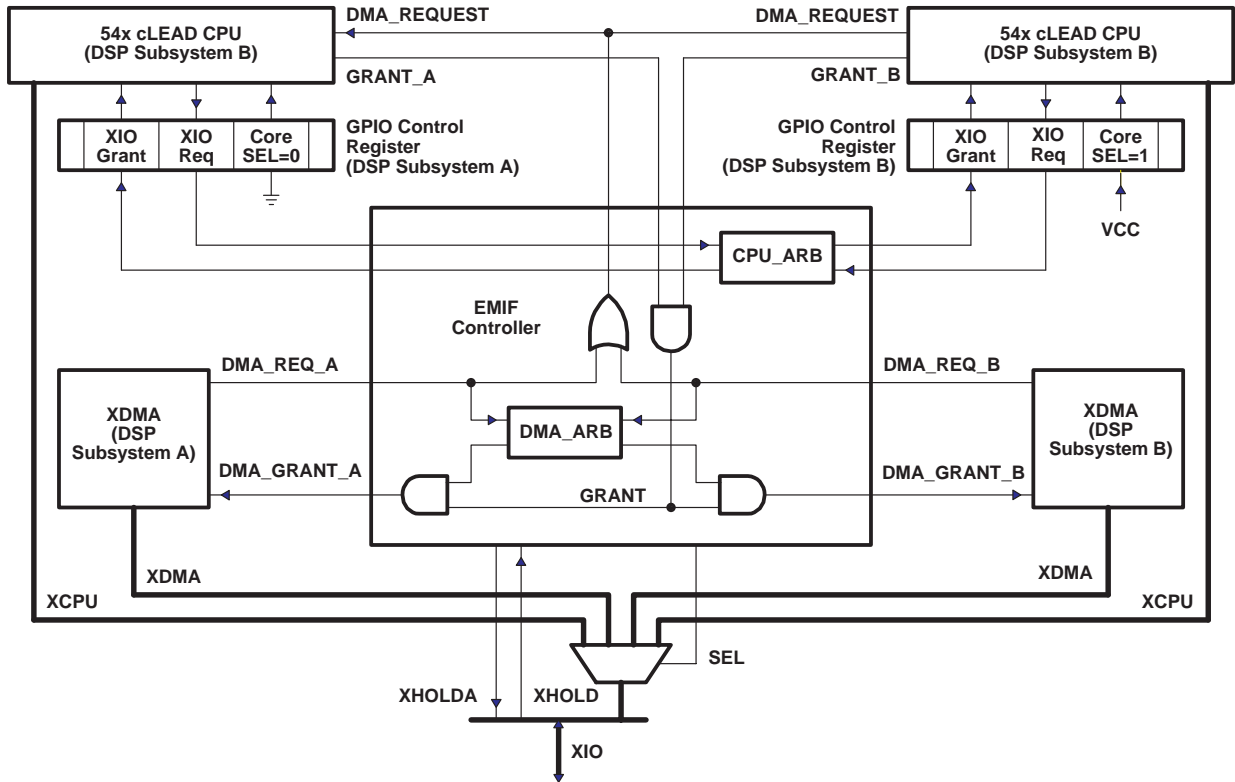


Figure 3-15. Arbitration Between XIO and xDMA for External Access

The HM bit in the ST1 indicates whether the processor continues internal execution when acknowledging an active HOLD signal.

- HM = 0, the processor continues execution from internal program memory but places its external interface in the high-impedance state.
- When HM = 1, the processor halts internal execution.

To ensure that proper arbitration occurs, the HM bit should be set to 0 in the memory-mapped ST1 registers for both CPUs.

To allow the DMA access to extended data pages, the SLAXS and DLAXS bits are added to the DMMCRn registers. For a description of the remaining bits, see *TMS320C54x DSP Reference Set, Volume 5: Enhanced Peripherals* (literature number SPRU302).

| | | | | | | | | | | | | | | | |
|-----------|------|------|--------|-------|------|---|-----|-------|---|------|---|---|---|-----|---|
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| AUTO INIT | DINM | IMOD | CT MOD | SLAXS | SIND | | DMS | DLAXS | | DIND | | | | DMD | |

Figure 3-16. DMA Transfer Mode Control Register (DMMCRn)

These new bit fields were created to allow the user to define the space-select for the DMA (internal/external). Also, a new extended destination data page (XDSTDP[6:0], subaddress 029h) and extended source data page (XSRCDP[6:0], subaddress 028h) have been created.

| | |
|---------------------------------|--|
| DLAXS(DMMCRn[5]) Destination | 0 = No external access (default internal) 1 = External access |
| SLAXS(DMMCRn[11]) Source | 0 = No external access (default internal) 1 = External access |

For the CPU external access, software can configure the memory cells to reside inside or outside the program address map. When the cells are mapped into program space, the device automatically accesses them when their addresses are within bounds. When the program address generation (PAGEN) logic generates an address outside its bounds, the device automatically generates an external access. All DMA I/O space accesses are mapped to the core-to-core FIFO.

3.8.3 DMA Controller Synchronization Events

The transfers associated with each DMA channel can be synchronized to one of several events. The DSYN bit field of the DMA channel x sync select and frame count (DMSFCx) register selects the synchronization event for a channel. The list of possible events and the DSYN values are shown in Table 3–10.

Table 3–10. DMA Synchronization Events

| DSYN VALUE | DMA SYNCHRONIZATION EVENT |
|---------------|-------------------------------------|
| 0000b | No synchronization used |
| 0001b | McBSP0 Receive Event |
| 0010b | McBSP0 Transmit Event |
| 0011b | McBSP2 Receive Event |
| 0100b | McBSP2 Transmit Event |
| 0101b | McBSP1 Receive Event |
| 0110b | McBSP1 Transmit Event |
| 0111b | FIFO Receive Buffer Not Empty Event |
| 1000b | FIFO Transmit Buffer Not Full Event |
| 1001b – 1111b | Reserved |

3.8.4 DMA Channel Interrupt Selection

The DMA controller can generate a CPU interrupt for each of the six channels. However, channels 0, 1, 2, and 3 are multiplexed with other interrupt sources. DMA channels 0 and 1 share an interrupt line with the receive and transmit portions of McBSP2 (IMR/IFR bits 6 and 7), and DMA channels 2 and 3 share an interrupt line with the receive and transmit portions of McBSP1 (IMR/IFR bits 10 and 11). When the 5421 is reset, the interrupts from these four DMA channels are deselected. The INTSEL bit field in the DMA channel priority and enable control (DMPREC) register can be used to select these interrupts, as shown in Table 3–11.

Table 3–11. DMA Channel Interrupt Selection

| INTSEL Value | IMR/IFR[6] | IMR/IFR[7] | IMR/IFR[10] | IMR/IFR[11] |
|--------------|------------|------------|-------------|-------------|
| 00b (reset) | BRINT2 | BXINT2 | BRINT1 | BXINT1 |
| 01b | BRINT2 | BXINT2 | DMAC2 | DMAC3 |
| 10b | DMAC0 | DMAC1 | DMAC2 | DMAC3 |
| 11b | Reserved | | | |

3.8.5 DMA in Autoinitialization Mode

The DMA can automatically reinitialize itself after completion of a block transfer. Some of the DMA registers can be preloaded for the next block transfer through the DMA global reload registers (DMGSA, DMGDA, DMGCR, and DMGFR). Autoinitialization allows:

- Continuous operation: Normally, the CPU would have to reinitialize the DMA immediately after the completion of the current block transfers, but with the global reload registers, it can reinitialize these values for the next block transfer any time after the current block transfer begins.
- Repetitive operation: The CPU does not preload the global reload register with new values for each block transfer but only loads them on the first block transfer.

The 5421 DMA has been enhanced to expand the DMA global reload register sets. Each DMA channel now has its own DMA global reload register set. For example, the DMA global reload register set for channel 0 has DMGSA0, DMGDA0, DMGCR0, and DMGFR0 while DMA channel 1 has DMGSA1, DMGDA1, DMGCR1, and DMGFR1, etc.

To utilize the additional DMA global reload registers, the AUTOIX bit is added to the DMPREC register as shown in Figure 3–17.

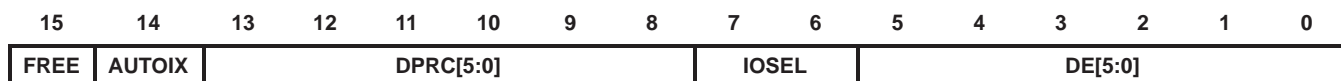


Figure 3–17. DMPREC Register

Table 3–12. DMA Global Reload Register Selection

| AUTOIX | DMA GLOBAL RELOAD REGISTER USAGE IN AUTO INIT MODE |
|-------------|--|
| 0 (default) | All DMA channels use DMGSA0, DMGDA0, DMGCR0 and DMGFR0 |
| 1 | Each DMA channel uses its own set of global reload registers |

3.8.6 Subsystem Communications

The 5421 device provides two options for efficient core-to-core communications:

- Core-to-core FIFO communications
- DMA global memory transfer

3.8.6.1 FIFO Data Communications

The subsystems’ FIFO communications interface is shown in the 5421 functional block diagram (Figure 3–1). Two unidirectional 8-word-deep FIFOs are available in the device for efficient interprocessor communication: one configured for core A-to-core B data transfers, and the other configured for core B-to-core A data transfers. Each subsystem, by way of DMA control, can write to its respective output data FIFO and read from its respective input data FIFO. The FIFOs are accessed using the DMAs I/O space, which is completely independent of the CPU I/O space. The DMA transfers to or from the FIFOs can be synchronized to “receive FIFO not empty” and “transmit FIFO not full” events, providing protection from overflow and underflow. Subsystems can interrupt each other to flag when the FIFOs are either full or empty. The interprocessor interrupt request bit (IPIRQ) (bit 8 in the BSCR register (BSCR.8)) is set to 1 to generate a PINT in the other subsystem’s IFR.14. See the *Interrupts* section (Section 3.13) for more information.

3.8.6.2 DMA Global Memory Transfers

The 5421 enables each subsystem to transfer data directly between the memories that are CPU local via DMA global memory transfers. The DMA global memory map is shown in Figure 3–13.

3.8.7 Chip Subsystem ID Register

The chip subsystem ID Register (CSIDR) is a read-only memory-mapped register located at 3Eh within each DSP subsystem. This register contains three elements for electrically readable device identification. The ChipID bits identify the type of 54x device (21h for 5421). The ChipRev bits contain the revision number of the device. Lastly, the SubSysID contains a unique subsystem identifier.

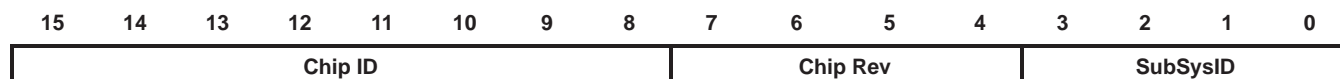


Figure 3–18. Chip Subsystem ID Register

Table 3–13. Chip Subsystem ID Register Bit Functions

| BIT NO. | BIT FIELD NAME | FUNCTION |
|---------|----------------|--|
| 15–8 | Chip ID | 54x device type. Contains 21h for 5421. |
| 7–4 | Chip Rev | Revision number of device (i.e., 0h for revision 0). |
| 3–0 | SubSysID | Identifier for DSP subsystem: A = 0h, B = 1h. |

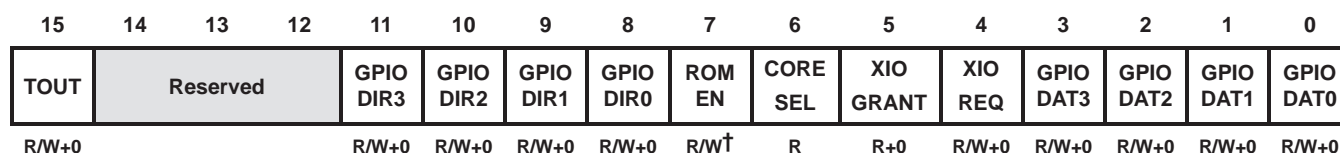
3.9 General-Purpose I/O

In addition to the A_XF and B_XF pins, the 5421 has eight general-purpose I/O pins. These pins are:

A_GPIO0, A_GPIO1, A_GPIO2, A_GPIO3

B_GPIO0, B_GPIO1, B_GPIO2, B_GPIO3

Four general-purpose I/O pins are available to each core. Each GPIO pin can be individually selected as either an input or an output. Additionally, the timer output is selectable on GPIO pin 3. At core reset, all GPIO pins are configured as inputs. GPIO data and control bits are accessible through a memory-mapped register at 3Ch with the format shown in Figure 3–19.



† 1 denotes XIO = 1, 0 denotes XIO = 0

Note: R = Read, W = Write, +0 = Value at reset

Figure 3–19. General-Purpose I/O Control Register

Table 3–14. General-Purpose I/O Control Register Bit Functions

| BIT NO. | BIT NAME | BIT VALUE | FUNCTION |
|---------|------------|-----------|---|
| 15 | TOUT | 0 | Timer output disable. Uses GPIO3 as general-purpose I/O. |
| | | 1 | Timer output enable. Overrides DIR3. Timer output is driven on GPIO3 and readable in DAT3. |
| 14-12 | Reserved | X | Register bit is reserved. Read 0, write has no effect. |
| 11–8 | GPIO DIRn† | 0 | GPIO pin is used as an input. |
| | | 1 | GPIO pin is used as an output. |
| 7 | ROMEN‡ | 0 | ROM is mapped out (value at reset if XIO = 0) |
| | | 1 | ROM is mapped in (value at reset if XIO = 1) |
| 6 | CORE SEL | 0 | cLEAD core A is selected for XIO REQ bit. DSP subsystem A is tied low internally for this bit. |
| | | 1 | cLEAD core B is selected for XIO REQ bit. DSP subsystem B is tied high internally for this bit. |
| 5 | XIO GRANT | 0 | EMIF is not available to the cLEAD core determined by the CORE SEL bit. |
| | | 1 | EMIF is granted to the cLEAD core determined by the CORE SEL bit. |
| 4 | XIO REQ | 0 | EMIF is not requested for the cLEAD core indicated by the CORE SEL bit. |
| | | 1 | Request EMIF for the cLEAD core indicated by the CORE SEL bit. |
| 3–0 | GPIO DATn† | 0 | GPIO pin is driven with a 0 (DIRn = 1). GPIO pin is read as 0 (DIRn = 0). |
| | | 1 | GPIO pin is driven with a 1 (DIRn = 1). GPIO pin is read as 1 (DIRn = 0). |

† n = 3, 2, 1, or 0

‡ 1 denotes XIO = 1, 0 denotes XIO = 0

Register bit 7 is used as ROMEN to enable and disable ROM space. In XIO mode, ROM enable (ROMEN) reflects the state of the A_GPIO0 and B_GPIO0 pins (GPIODAT0 input) to enable the applicable on-chip ROM after reset. Register bits (6:4) are used for XIO arbitration of external memory interface (EMIF) control between DSP subsystems. The timer out (TOUT) bit is used to multiplex the output of the timer and GPIO3. All GPIO pins are programmable as an input or output by the direction bit (DIRn). Data is either driven or read from the data bit field (DATn). DIR3 has no affect when TOUT = 1.

GPIO2 is a special case where the logic level determines the operation of $\overline{\text{BIO}}$ -conditional instructions on the CPU. GPIO2 is always mapped as a general-purpose I/O, but the $\overline{\text{BIO}}$ function exists when this pin is configured as an input.

3.9.1 Hardware Timer

The 54x devices feature a 16-bit timing circuit with a 4-bit prescaler. The timer counter decrements by one at every CLKOUT cycle. Each time the counter decrements to zero, a timer interrupt is generated. The timer can be stopped, restarted, reset, or disabled by specific status bits. The timer output pulse is driven on GPIO3 when the TOUT bit is set to one in the general-purpose I/O control register. The device must be in HPI mode (XIO = 0) to drive TOUT on the GPIO3 pin.

3.9.2 Software-Programmable Phase-Locked Loop (PLL)

The clock generator provides clocks to the 5421 device, and consists of a phase-locked loop (PLL) circuit. The clock generator requires a reference clock input, which must be provided by using an external clock source. The reference clock input is then divided by two (DIV mode) to generate clocks for the 5421 device. Alternately, the PLL circuit can be used (PLL mode) to generate the device clock by multiplying the reference clock frequency by a scale factor, allowing use of a clock source with a lower frequency than that of the CPU. Bypass (multiply by 1) is the default mode at reset. The PLL is an adaptive circuit that, once synchronized, locks onto and tracks an input clock signal. When the PLL is initially started, it enters a transitional mode during which the PLL acquires lock with the input signal. Once the PLL is locked, it continues to track and maintain synchronization with the input signal. Then, other internal clock circuitry allows the synthesis of new clock frequencies for use as master clock for the 5421 device. Only subsystem A controls the PLL. Subsystem B cannot access the PLL registers.

The software-programmable PLL features a high level of flexibility, and includes a clock scaler that provides various clock multiplier ratios, capability to directly enable and disable the PLL, and a PLL lock timer that can be used to delay switching to PLL clocking mode of the device until lock is achieved. Devices that have a built-in software-programmable PLL can be configured in one of two clock modes:

- PLL mode. The input clock (CLKIN) is multiplied by 1 of 31 possible ratios. These ratios are achieved using the PLL circuitry.
- DIV (divider) mode. The input clock is divided by 2 or 4. Note that when DIV mode is used, the PLL can be completely disabled in order to minimize power dissipation.

The software-programmable PLL is controlled using the 16-bit memory-mapped (address 0058h) clock mode register (CLKMD). The CLKMD register is used to define the clock configuration of the PLL clock module. Figure 3–20 shows the bit layout of the clock mode register and Table 3–15 describes the bit functions.

| | | | | | | | |
|---------------------|---------------------|-----------------------|----|---|------------------------|---------|--------|
| 15 | 12 | 11 | 10 | 3 | 2 | 1 | 0 |
| PLLMUL [†] | PLLDIV [†] | PLLCOUNT [†] | | | PLLON/OFF [†] | PLLNDIV | STATUS |
| R/W | R/W | R/W | | | R/W | R/W | R/W |

[†] When in DIV mode (PLLSTATUS is low), PLLMUL, PLLDIV, PLLCOUNT, and PLLON/OFF are don't cares, and their contents are indeterminate.

LEGEND: R = Read, W = Write

Figure 3–20. Clock Mode Register (CLKMD)

Table 3–15. Clock Mode Register (CLKMD) Bit Functions

| BIT NO. | BIT NAME | FUNCTION |
|---------|------------------------|---|
| 15–12 | PLLMUL [†] | PLL multiplier. PLLMUL defines the frequency multiplier in conjunction with PLLDIV and PLLNDIV. See Table 3–16. |
| 11 | PLLDIV [†] | PLL divider. PLLDIV defines the frequency multiplier in conjunction with PLLMUL and PLLNDIV. See Table 3–16. PLLDIV = 0 Means that an integer multiply factor is used PLLDIV = 1 Means that a noninteger multiply factor is used |
| 10–3 | PLLCOUNT [†] | PLL counter value. PLLCOUNT specifies the number of input clock cycles (in increments of 16 cycles) for the PLL lock timer to count before the PLL begins clocking the processor after the PLL is started. The PLL counter is a down-counter, which is driven by the input clock divided by 16; therefore, for every 16 input clocks, the PLL counter decrements by one. The PLL counter can be used to ensure that the processor is not clocked until the PLL is locked, so that only valid clock signals are sent to the device. |
| 2 | PLLON/OFF [†] | PLL on/off. PLLON/OFF enables or disables the PLL part of the clock generator in conjunction with the PLLNDIV bit (see Table 3–17). Note that PLLON/OFF and PLLNDIV can both force the PLL to run; when PLLON/OFF is high, the PLL runs independently of the state of PLLNDIV. |
| 1 | PLLNDIV | PLLNDIV configures PLL mode when high or DIV mode when low. PLLNDIV defines the frequency multiplier in conjunction with PLLDIV and PLLMUL. See Table 3–16. |
| 0 | STATUS | Indicates the PLL mode. STATUS = 0 Indicates DIV mode STATUS = 1 Indicates PLL mode |

[†] When in DIV mode (PLLSTATUS is low), PLLMUL, PLLDIV, PLLCOUNT, and PLLON/OFF are don't cares, and their contents are indeterminate.

Table 3–16. Multiplier Related to PLLNDIV, PLLDIV, and PLLMUL

| PLLNDIV | PLLDIV | PLLMUL | MULTIPLIER† |
|---------|--------|-----------|-------------------------|
| 0 | x | 0–14 | 0.5 |
| 0 | x | 15 | 0.25 |
| 1 | 0 | 0–14 | PLLMUL + 1 |
| 1 | 0 | 15 | bypass (multiply by 1)‡ |
| 1 | 1 | 0 or even | (PLLMUL + 1)/2 |
| 1 | 1 | odd | PLLMUL/4 |

† CLKOUT = CLKIN * Multiplier

‡ Indicates the default clock mode after reset

Table 3–17. VCO Truth Table

| PLLON/OFF | PLLNDIV | VCO STATE |
|-----------|---------|-----------|
| 0 | 0 | off |
| 1 | 0 | on |
| 0 | 1 | on |
| 1 | 1 | on |

3.9.3 PLL Clock Programmable Timer

During the lockup period, the PLL should not be used to clock the 5421. The PLLCOUNT programmable lock timer provides a convenient method of automatically delaying clocking of the device by the PLL until lock is achieved.

The PLL lock timer is a counter, loaded from the PLLCOUNT field in the CLKMD register, that decrements from its preset value to 0. The timer can be preset to any value from 0 to 255, and its input clock is CLKIN divided by 16. The resulting lockup delay can therefore be set from 0 to 255 × 16 CLKIN cycles.

The lock timer is activated when the operating mode of the clock generator is switched from DIV to PLL. During the lockup period, the clock generator continues to operate in DIV mode; after the PLL lock timer decrements to zero, the PLL begins clocking the 5421.

Accordingly, the value loaded into PLLCOUNT is chosen based on the following formula:

$$PLLCOUNT = \frac{\text{Lockup Time}}{16 \times T_{CLKIN}}$$

where T_{CLKIN} is the input reference clock period and lockup time is the required VCO lockup time, as shown in Table 3–18.

Table 3–18. VCO Lockup Time

| CLKOUT FREQUENCY (MHz) | LOCKUP TIME (µs) |
|------------------------|------------------|
| 5 | 23 |
| 10 | 17 |
| 20 | 16 |
| 40 | 19 |
| 60 | 24 |
| 80 | 29 |
| 100 | 35 |

3.10 Memory-Mapped Registers

The 5421 has 27 memory-mapped CPU registers, which are mapped in data memory space address 0h to 1Fh. Each 5421 device also has a set of memory-mapped registers associated with peripherals. Table 3–19 gives a list of CPU memory-mapped registers (MMRs) available. Table 3–20 shows additional peripheral MMRs associated with the 5421.

Table 3–19. Processor Memory-Mapped Registers for Each DSP Subsystem

| NAME | ADDRESS | | DESCRIPTION |
|------|---------|-----|----------------------------------|
| | DEC | HEX | |
| IMR | 0 | 0 | Interrupt Mask Register |
| IFR | 1 | 1 | Interrupt Flag Register |
| — | 2–5 | 2–5 | Reserved for testing |
| ST0 | 6 | 6 | Status Register 0 |
| ST1 | 7 | 7 | Status Register 1 |
| AL | 8 | 8 | Accumulator A Low Word (15–0) |
| AH | 9 | 9 | Accumulator A High Word (31–16) |
| AG | 10 | A | Accumulator A Guard Bits (39–32) |
| BL | 11 | B | Accumulator B Low Word (15–0) |
| BH | 12 | C | Accumulator B High Word (31–16) |
| BG | 13 | D | Accumulator B Guard Bits (39–32) |
| TREG | 14 | E | Temporary Register |
| TRN | 15 | F | Transition Register |
| AR0 | 16 | 10 | Auxiliary Register 0 |
| AR1 | 17 | 11 | Auxiliary Register 1 |
| AR2 | 18 | 12 | Auxiliary Register 2 |
| AR3 | 19 | 13 | Auxiliary Register 3 |
| AR4 | 20 | 14 | Auxiliary Register 4 |
| AR5 | 21 | 15 | Auxiliary Register 5 |
| AR6 | 22 | 16 | Auxiliary Register 6 |
| AR7 | 23 | 17 | Auxiliary Register 7 |
| SP | 24 | 18 | Stack Pointer |
| BK | 25 | 19 | Circular Buffer Size Register |
| BRC | 26 | 1A | Block-Repeat Counter |
| RSA | 27 | 1B | Block-Repeat Start Address |
| REA | 28 | 1C | Block-Repeat End Address |
| PMST | 29 | 1D | Processor Mode Status Register |
| XPC | 30 | 1E | Extended Program Counter |
| — | 31 | 1F | Reserved |

Table 3–20. Peripheral Memory-Mapped Registers for Each DSP Subsystem

| NAME | ADDRESS | | DESCRIPTION |
|--------|---------|-------|---|
| | DEC | HEX | |
| DRR20 | 32 | 20 | McBSP 0 Data Receive Register 2 |
| DRR10 | 33 | 21 | McBSP 0 Data Receive Register 1 |
| DXR20 | 34 | 22 | McBSP 0 Data Transmit Register 2 |
| DXR10 | 35 | 23 | McBSP 0 Data Transmit Register 1 |
| TIM | 36 | 24 | Timer Register |
| PRD | 37 | 25 | Timer Period Register |
| TCR | 38 | 26 | Timer Control Register |
| — | 39 | 27 | Reserved |
| SWWSR | 40 | 28 | Software Wait-State Register |
| BSCR | 41 | 29 | Bank-Switching Control Register |
| — | 42 | 2A | Reserved |
| SWCR | 43 | 2B | Software Wait-State Control Register |
| HPIC | 44 | 2C | HPI Control Register (HMODE=0 only) |
| — | 45–47 | 2D–2F | Reserved |
| DRR22 | 48 | 30 | McBSP 2 Data Receive Register 2 |
| DRR12 | 49 | 31 | McBSP 2 Data Receive Register 1 |
| DXR22 | 50 | 32 | McBSP 2 Data Transmit Register 2 |
| DXR12 | 51 | 33 | McBSP 2 Data Transmit Register 1 |
| SPSA2 | 52 | 34 | McBSP 2 Subbank Address Register† |
| SPSD2 | 53 | 35 | McBSP 2 Subbank Data Register† |
| — | 54–55 | 36–37 | Reserved |
| SPSA0 | 56 | 38 | McBSP 0 Subbank Address Register† |
| SPSD0 | 57 | 39 | McBSP 0 Subbank Data Register† |
| — | 58–59 | 3A–3B | Reserved |
| GPIO | 60 | 3C | General-Purpose I/O Register |
| — | 61 | 3D | Reserved |
| CSIDR | 62 | 3E | Chip Subsystem ID register |
| — | 63 | 3F | Reserved |
| DRR21 | 64 | 40 | McBSP 1 Data Receive Register 2 |
| DRR11 | 65 | 41 | McBSP 1 Data Receive Register 1 |
| DXR21 | 66 | 42 | McBSP 1 Data Transmit Register 2 |
| DXR11 | 67 | 43 | McBSP 1 Data Transmit Register 1 |
| — | 68–71 | 44–47 | Reserved |
| SPSA1 | 72 | 48 | McBSP 1 Subbank Address Register† |
| SPSD1 | 73 | 49 | McBSP 1 Subbank Data Register† |
| — | 74–83 | 4A–53 | Reserved |
| DMPREC | 84 | 54 | DMA Priority and Enable Control Register |
| DMSA | 85 | 55 | DMA Subbank Address Register‡ |
| DMSDI | 86 | 56 | DMA Subbank Data Register with Autoincrement‡ |
| DMSDN | 87 | 57 | DMA Subbank Data Register‡ |
| CLKMD | 88 | 58 | Clock Mode Register (CLKMD) |
| — | 89–95 | 59–5F | Reserved |

† See Table 3–21 for a detailed description of the McBSP control registers and their subaddresses.

‡ See Table 3–22 for a detailed description of the DMA subbank addressed registers.

3.11 McBSP Control Registers and Subaddresses

The control registers for the multichannel buffered serial port (McBSP) are accessed using the subbank addressing scheme. This allows a set or subbank of registers to be accessed through a single memory location. The McBSP subbank address register (SPSA) is used as a pointer to select a particular register within the subbank. The McBSP data register (SPSDx) is used to access (read or write) the selected register. Table 3–21 shows the McBSP control registers and their corresponding subaddresses.

Table 3–21. McBSP Control Registers and Subaddresses

| McBSP0 | | McBSP1 | | McBSP2 | | SUB-ADDRESS | DESCRIPTION |
|--------|---------|--------|---------|--------|---------|-------------|--|
| NAME | ADDRESS | NAME | ADDRESS | NAME | ADDRESS | | |
| SPCR10 | 39h | SPCR11 | 49h | SPCR12 | 35h | 00h | Serial port control register 1 |
| SPCR20 | 39h | SPCR21 | 49h | SPCR22 | 35h | 01h | Serial port control register 2 |
| RCR10 | 39h | RCR11 | 49h | RCR12 | 35h | 02h | Receive control register 1 |
| RCR20 | 39h | RCR21 | 49h | RCR22 | 35h | 03h | Receive control register 2 |
| XCR10 | 39h | XCR11 | 49h | XCR12 | 35h | 04h | Transmit control register 1 |
| XCR20 | 39h | XCR21 | 49h | XCR22 | 35h | 05h | Transmit control register 2 |
| SRGR10 | 39h | SRGR11 | 49h | SRGR12 | 35h | 06h | Sample rate generator register 1 |
| SRGR20 | 39h | SRGR21 | 49h | SRGR22 | 35h | 07h | Sample rate generator register 2 |
| MCR10 | 39h | MCR11 | 49h | MCR12 | 35h | 08h | Multichannel register 1 |
| MCR20 | 39h | MCR21 | 49h | MCR22 | 35h | 09h | Multichannel register 2 |
| RCERA0 | 39h | RCERA1 | 49h | RCERA2 | 35h | 0Ah | Receive channel enable register partition A |
| RCERB0 | 39h | RCERB1 | 49h | RCERB2 | 35h | 0Bh | Receive channel enable register partition B |
| XCERA0 | 39h | XCERA1 | 49h | XCERA2 | 35h | 0Ch | Transmit channel enable register partition A |
| XCERB0 | 39h | XCERB1 | 49h | XCERB2 | 35h | 0Dh | Transmit channel enable register partition B |
| PCR0 | 39h | PCR1 | 49h | PCR2 | 35h | 0Eh | Pin control register |
| RCERC0 | 39h | RCERC1 | 49h | RCERC2 | 35h | 010h | Receive channel enable register partition C |
| RCERD0 | 39h | RCERD1 | 49h | RCERD2 | 35h | 011h | Receive channel enable register partition D |
| XCERC0 | 39h | XCERC1 | 49h | XCERC2 | 35h | 012h | Transmit channel enable register partition C |
| XCERD0 | 39h | XCERD1 | 49h | XCERD2 | 35h | 013h | Transmit channel enable register partition D |
| RCERE0 | 39h | RCERE1 | 49h | RCERE2 | 35h | 014h | Receive channel enable register partition E |
| RCERF0 | 39h | RCERF1 | 49h | RCERF2 | 35h | 015h | Receive channel enable register partition F |
| XCERE0 | 39h | XCERE1 | 49h | XCERE2 | 35h | 016h | Transmit channel enable register partition E |
| XCERF0 | 39h | XCERF1 | 49h | XCERF2 | 35h | 017h | Transmit channel enable register partition F |
| RCERG0 | 39h | RCERG1 | 49h | RCERG2 | 35h | 018h | Receive channel enable register partition G |
| RCERH0 | 39h | RCERH1 | 49h | RCERH2 | 35h | 019h | Receive channel enable register partition H |
| XCERG0 | 39h | XCERG1 | 49h | XCERG2 | 35h | 01Ah | Transmit channel enable register partition G |
| XCERH0 | 39h | XCERH1 | 49h | XCERH2 | 35h | 01Bh | Transmit channel enable register partition H |

3.12 DMA Subbank Addressed Registers

The direct memory access (DMA) controller has several control registers associated with it. The main control register (DMPREC) is a standard memory-mapped register. However, the other registers are accessed using the subbank addressing scheme. This allows a set or subbank of registers to be accessed through a single memory location. The DMA subbank address (DMSA) register is used as a pointer to select a particular register within the subbank, while the DMA subbank data (DMSD) register or the DMA subbank data register with autoincrement (DMSDI) is used to access (read or write) the selected register.

When the DMSDI register is used to access the subbank, the subbank address is automatically postincremented so that a subsequent access affects the next register within the subbank. This autoincrement feature is intended for efficient, successive accesses to several control registers. If the autoincrement feature is not required, the DMSDN register should be used to access the subbank. Table 3–22 shows the DMA controller subbank addressed registers and their corresponding subaddresses.

Table 3–22. DMA Subbank Addressed Registers

| NAME | ADDRESS | SUB-ADDRESS | DESCRIPTION |
|--------|---------|-------------|---|
| DMSRC0 | 56h/57h | 00h | DMA channel 0 source address register |
| DMDST0 | 56h/57h | 01h | DMA channel 0 destination address register |
| DMCTR0 | 56h/57h | 02h | DMA channel 0 element count register |
| DMSFC0 | 56h/57h | 03h | DMA channel 0 sync event and frame count register |
| DMMCR0 | 56h/57h | 04h | DMA channel 0 transfer mode control register |
| DMSRC1 | 56h/57h | 05h | DMA channel 1 source address register |
| DMDST1 | 56h/57h | 06h | DMA channel 1 destination address register |
| DMCTR1 | 56h/57h | 07h | DMA channel 1 element count register |
| DMSFC1 | 56h/57h | 08h | DMA channel 1 sync event and frame count register |
| DMMCR1 | 56h/57h | 09h | DMA channel 1 transfer mode control register |
| DMSRC2 | 56h/57h | 0Ah | DMA channel 2 source address register |
| DMDST2 | 56h/57h | 0Bh | DMA channel 2 destination address register |
| DMCTR2 | 56h/57h | 0Ch | DMA channel 2 element count register |
| DMSFC2 | 56h/57h | 0Dh | DMA channel 2 sync event and frame count register |
| DMMCR2 | 56h/57h | 0Eh | DMA channel 2 transfer mode control register |
| DMSRC3 | 56h/57h | 0Fh | DMA channel 3 source address register |
| DMDST3 | 56h/57h | 10h | DMA channel 3 destination address register |
| DMCTR3 | 56h/57h | 11h | DMA channel 3 element count register |
| DMSFC3 | 56h/57h | 12h | DMA channel 3 sync event and frame count register |
| DMMCR3 | 56h/57h | 13h | DMA channel 3 transfer mode control register |
| DMSRC4 | 56h/57h | 14h | DMA channel 4 source address register |
| DMDST4 | 56h/57h | 15h | DMA channel 4 destination address register |
| DMCTR4 | 56h/57h | 16h | DMA channel 4 element count register |
| DMSFC4 | 56h/57h | 17h | DMA channel 4 sync event and frame count register |
| DMMCR4 | 56h/57h | 18h | DMA channel 4 transfer mode control register |
| DMSRC5 | 56h/57h | 19h | DMA channel 5 source address register |
| DMDST5 | 56h/57h | 1Ah | DMA channel 5 destination address register |
| DMCTR5 | 56h/57h | 1Bh | DMA channel 5 element count register |
| DMSFC5 | 56h/57h | 1Ch | DMA channel 5 sync event and frame count register |
| DMMCR5 | 56h/57h | 1Dh | DMA channel 5 transfer mode control register |
| DMSRCP | 56h/57h | 1Eh | DMA source program page address (common channel) |

Table 3–22. DMA Subbank Addressed Registers (Continued)

| NAME | ADDRESS | SUB-ADDRESS | DESCRIPTION |
|--------|---------|-------------|--|
| DMDSTP | 56h/57h | 1Fh | DMA destination program page address (common channel) |
| DMIDX0 | 56h/57h | 20h | DMA element index address register 0 |
| DMIDX1 | 56h/57h | 21h | DMA element index address register 1 |
| DMFRI0 | 56h/57h | 22h | DMA frame index register 0 |
| DMFRI1 | 56h/57h | 23h | DMA frame index register 1 |
| DMGSA0 | 56h/57h | 24h | DMA channel 0 global source address reload register |
| DMGDA0 | 56h/57h | 25h | DMA channel 0 global destination address reload register |
| DMGCR0 | 56h/57h | 26h | DMA channel 0 global count reload register |
| DMGFR0 | 56h/57h | 27h | DMA channel 0 global frame count reload register |
| XSRCDP | 56h/57h | 28h | DMA extended source data page |
| XDSTDP | 56h/57h | 29h | DMA extended destination data page |
| DMGSA1 | 56h/57h | 2Ah | DMA channel 1 global source address reload register |
| DMGDA1 | 56h/57h | 2Bh | DMA channel 1 global destination address reload register |
| DMGCR1 | 56h/57h | 2Ch | DMA channel 1 global count reload register |
| DMGFR1 | 56h/57h | 2Dh | DMA channel 1 global frame count reload register |
| DMGSA2 | 56h/57h | 2Eh | DMA channel 2 global source address reload register |
| DMGDA2 | 56h/57h | 2Fh | DMA channel 2 global destination address reload register |
| DMGCR2 | 56h/57h | 30h | DMA channel 2 global count reload register |
| DMGFR2 | 56h/57h | 31h | DMA channel 2 global frame count reload register |
| DMGSA3 | 56h/57h | 32h | DMA channel 3 global source address reload register |
| DMGDA3 | 56h/57h | 33h | DMA channel 3 global destination address reload register |
| DMGCR3 | 56h/57h | 34h | DMA channel 3 global count reload register |
| DMGFR3 | 56h/57h | 35h | DMA channel 3 global frame count reload register |
| DMGSA4 | 56h/57h | 36h | DMA channel 4 global source address reload register |
| DMGDA4 | 56h/57h | 37h | DMA channel 4 global destination address reload register |
| DMGCR4 | 56h/57h | 38h | DMA channel 4 global count reload register |
| DMGFR4 | 56h/57h | 39h | DMA channel 4 global frame count reload register |
| DMGSA5 | 56h/57h | 3Ah | DMA channel 5 global source address reload register |
| DMGDA5 | 56h/57h | 3Bh | DMA channel 5 global destination address reload register |
| DMGCR5 | 56h/57h | 3Ch | DMA channel 5 global count reload register |
| DMGFR5 | 56h/57h | 3Dh | DMA channel 5 global frame count reload register |

3.13 Interrupts

Vector-relative locations and priorities for all internal and external interrupts are shown in Table 3–23.

Table 3–23. 5421 Interrupt Locations and Priorities for Each DSP Subsystem

| NAME | LOCATION | | PRIORITY | FUNCTION |
|---------------|----------|-------|----------|--|
| | DECIMAL | HEX | | |
| RS, SINTR | 0 | 00 | 1 | Reset (Hardware and Software Reset) |
| NMI, SINT16 | 4 | 04 | 2 | Nonmaskable Interrupt |
| SINT17 | 8 | 08 | — | Software Interrupt #17 |
| SINT18 | 12 | 0C | — | Software Interrupt #18 |
| SINT19 | 16 | 10 | — | Software Interrupt #19 |
| SINT20 | 20 | 14 | — | Software Interrupt #20 |
| SINT21 | 24 | 18 | — | Software Interrupt #21 |
| SINT22 | 28 | 1C | — | Software Interrupt #22 |
| SINT23 | 32 | 20 | — | Software Interrupt #23 |
| SINT24 | 36 | 24 | — | Software Interrupt #24 |
| SINT25 | 40 | 28 | — | Software Interrupt #25 |
| SINT26 | 44 | 2C | — | Software Interrupt #26 |
| SINT27 | 48 | 30 | — | Software Interrupt #27 |
| SINT28 | 52 | 34 | — | Software Interrupt #28 |
| SINT29 | 56 | 38 | — | Software Interrupt #29 |
| SINT30 | 60 | 3C | — | Software Interrupt #30 |
| INT0, SINT0 | 64 | 40 | 3 | External User Interrupt #0 |
| INT1, SINT1 | 68 | 44 | 4 | External User Interrupt #1 |
| INT2, SINT2 | 72 | 48 | 5 | Reserved |
| TINT, SINT3 | 76 | 4C | 6 | External Timer Interrupt |
| BRINT0, SINT4 | 80 | 50 | 7 | BSP #0 Receive Interrupt |
| BXINT0, SINT5 | 84 | 54 | 8 | BSP #0 Transmit Interrupt |
| BRINT2, DMAC0 | 88 | 58 | 9 | BSP #2 Receive Interrupt or DMA Channel 0 |
| BXINT2, DMAC1 | 92 | 5C | 10 | BSP #2 Receive Interrupt or DMA Channel 1 |
| INT3, SINT8 | 96 | 60 | 11 | Reserved |
| HPINT, SINT9 | 100 | 64 | 12 | HPI Interrupt (from DSPINT in HPIC) |
| BRINT1, DMAC2 | 104 | 68 | 13 | BSP #1 Receive Interrupt or DMA Channel 2 |
| BXINT1, DMAC3 | 108 | 6C | 14 | BSP #1 transmit Interrupt or DMA channel 3 |
| DMAC4, SINT12 | 112 | 70 | 15 | DMA Channel 4 |
| DMAC5, SINT13 | 116 | 74 | 16 | DMA Channel 5 |
| IPINT, SINT14 | 120 | 78 | 17 | Interprocessor Interrupt |
| — | 124–127 | 7C–7F | — | Reserved |

The interprocessor interrupt (IPINT) bit of the interrupt mask register (IMR) and the interrupt flag register (IFR) allows the subsystem to perform interrupt service routines based on the other subsystem activity. Incoming IPINT interrupts are latched in IFR.14. Generating an interprocessor interrupt is performed by writing a “1” to the IPIRQ field of the bank-switching control register (BSCR). Subsequent interrupts must first clear the interrupt by writing “0” to the IPIRQ field. Figure 3–21 shows the bit layout of the IMR and the IFR. Table 3–24 describes the bit functions.

For example, if subsystem A is required to notify subsystem B of a completed task, subsystem A must write a “1” to the IPIRQ field to generate a IPINT interrupt on subsystem B. On subsystem B, the IPINT interrupt is latched in IFR.14. Figure 5 shows the bit layout of the BSCR and Table 6 describes the bit functions.

| | | | | | | | |
|----------------|----------------|-------|-------|----------------|----------------|-------|----------|
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| Reserved | IPINT | DMAC5 | DMAC4 | XINT1 or DMAC3 | RINT1 or DMAC2 | HPINT | Reserved |
| | R/W | | R/W | R/W | R/W | R/W | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| XINT2 or DMAC1 | RINT2 or DMAC0 | XINT0 | RINT0 | TINT | Reserved | INT1 | INT0 |
| R/W | R/W | R/W | R/W | R/W | | R/W | R/W |

LEGEND: R = Read, W = Write

Figure 3–21. Bit Layout of the IMR and IFR Registers for Subsystems A and B

Table 3–24. Bit Functions for IMR and IFR Registers for Each DSP Subsystem

| BIT NO. | BIT NAME | BIT VALUE | FUNCTION |
|---------|----------|-----------|--|
| 15 | Reserved | X | Register bit is reserved. |
| 14 | IPINT | 0 | IFR/IMR: Interprocessor IRQ has no interrupt pending/is disabled (masked). |
| | | 1 | IFR/IMR: Interprocessor IRQ has an interrupt pending/is enabled. |
| 13 | DMAC5 | 0 | IFR/IMR: DMA Channel 5 has no interrupt pending/is disabled (masked). |
| | | 1 | IFR/IMR: DMA Channel 5 has an interrupt pending/is enabled. |
| 12 | DMAC4 | 0 | IFR/IMR: DMA Channel 4 has no interrupt pending/is disabled (masked). |
| | | 1 | IFR/IMR: DMA Channel 4 has an interrupt pending/is enabled. |
| 11 | XINT1 | 0 | IFR/IMR: McBSP_1 has no transmit interrupt pending/is disabled (masked). |
| | | 1 | IFR/IMR: McBSP_1 has a transmit interrupt pending/is enabled. |
| | DMAC3 | 0 | IFR/IMR: DMA Channel 3 has no interrupt pending/is disabled (masked). |
| | | 1 | IFR/IMR: DMA Channel 3 has an interrupt pending/is enabled. |
| 10 | RINT1 | 0 | IFR/IMR: McBSP_1 has no receive interrupt pending/is disabled (masked). |
| | | 1 | IFR/IMR: McBSP_1 has a receive interrupt pending/is enabled. |
| | DMAC2 | 0 | IFR/IMR: DMA Channel 2 has no interrupt pending/is disabled (masked). |
| | | 1 | IFR/IMR: DMA Channel 2 has an interrupt pending/is enabled. |
| 9 | HPINT | 0 | IFR/IMR: Host-port interface has no DSPINT interrupt pending/is disabled (masked). |
| | | 1 | IFR/IMR: Host-port interface has an DSPINT interrupt pending/is enabled. |
| 8 | Reserved | X | Register bit is reserved. |
| 7 | XINT2 | 0 | IFR/IMR: McBSP_2 has no transmit interrupt pending/is disabled (masked). |
| | | 1 | IFR/IMR: McBSP_2 has a transmit interrupt pending/is enabled. |
| | DMAC1 | 0 | IFR/IMR: DMA Channel 1 has no interrupt pending/is disabled (masked). |
| | | 1 | IFR/IMR: DMA Channel 1 has an interrupt pending/is enabled. |
| 6 | RINT2 | 0 | IFR/IMR: McBSP_2 has no receive interrupt pending/is disabled (masked). |
| | | 1 | IFR/IMR: McBSP_2 has a receive interrupt pending/is enabled. |
| | DMAC0 | 0 | IFR/IMR: DMA Channel 0 has no interrupt pending/is disabled (masked). |
| | | 1 | IFR/IMR: DMA Channel 0 has an interrupt pending/is enabled. |
| 5 | XINT0 | 0 | IFR/IMR: McBSP_0 has no receive interrupt pending/is disabled (masked). |
| | | 1 | IFR/IMR: McBSP_0 has a receive interrupt pending/is enabled. |
| 4 | RINT0 | 0 | IFR/IMR: McBSP_0 has no receive interrupt pending/is disabled (masked). |
| | | 1 | IFR/IMR: McBSP_0 has a receive interrupt pending/is enabled. |

Table 3–24. Bit Functions for IMR and IFR Registers for Each DSP Subsystem (Continued)

| BIT NO. | BIT NAME | BIT VALUE | FUNCTION |
|---------|----------|-----------|--|
| 3 | TINT | 0 | IFR/IMR: Timer has no interrupt pending/is disabled (masked). |
| | | 1 | IFR/IMR: Timer has an interrupt pending/is enabled. |
| 2 | Reserved | X | Register bit is reserved. |
| 1 | INT1 | 0 | IFR/IMR: Ext user interrupt pin 1 has no interrupt pending/is disabled (masked). |
| | | 1 | IFR/IMR: Ext user interrupt pin 1 has an interrupt pending/is enabled. |
| 0 | INT0 | 0 | IFR/IMR: Ext user interrupt pin 0 has no interrupt pending/is disabled (masked). |
| | | 1 | IFR/IMR: Ext user interrupt pin 0 has an interrupt pending/is enabled. |

3.14 IDLE3 Power-Down Mode

The IDLE1 and IDLE2 power-down modes operate as described in the *TMS320C54x DSP Reference Set, Volume 1: CPU and Peripherals* (literature number SPRU131). The IDLE3 mode is special in that the clocking circuitry is shut off to conserve power. The 5421 cannot enter an IDLE3 mode unless both subsystems execute an IDLE3 instruction. The power-reduced benefits of IDLE3 cannot be realized until both subsystems enter the IDLE3 state and the internal clocks are automatically shut off. The order in which subsystems enter IDLE3 does not matter.

3.15 Emulating the 5421 Device

The 5421 is a single device, but actually consists of two independent subboundary systems that contain register/status information used by the emulator tools. The emulator tools must be informed of the multicore device by modifying the **board.cfg** file. The board.cfg file is an ASCII file that can be modified with most editors. This provides the emulator with a description of the JTAG chain. The board.cfg file must identify two processors when using the 5421. The file contents would look something like this:

```
"CPU_B" TI320C5xx
```

```
"CPU_A" TI320C5xx
```

Use Code Composer Studio to convert this file into a binary file (**board.dat**), readable by the emulation tools. Place the board.dat file in the directory that contains the emulator software.

The subsystems are serially connected together internally. Emulation information is serially transmitted into the device using the TDI pin. The device responds with serial scan information transmitted out the TDO pin.

4 Documentation Support

Extensive documentation supports all TMS320™ DSP family generations of devices from product announcement through applications development. The following types of documentation are available to support the design and use of the TMS320C5000™ family of DSPs:

- *TMS320C54x™ DSP Functional Overview* (literature number SPRU307)
- Device-specific data sheets
- Complete User Guides
- Development-support tools
- Hardware and software application reports

The five-volume *TMS320C54x DSP Reference Set* (literature number SPRU210) consists of:

- *Volume 1: CPU and Peripherals* (literature number SPRU131)
- *Volume 2: Mnemonic Instruction Set* (literature number SPRU172)
- *Volume 3: Algebraic Instruction Set* (literature number SPRU179)
- *Volume 4: Applications Guide* (literature number SPRU173)
- *Volume 5: Enhanced Peripherals* (literature number SPRU302)

The reference set describes in detail the TMS320C54x™ DSP family of products currently available and the hardware and software applications, including algorithms, for fixed-point TMS320™ DSP family of devices.

A series of DSP textbooks is published by Prentice-Hall and John Wiley & Sons to support digital signal processing research and education. The TMS320™ DSP family newsletter, *Details on Signal Processing*, is published quarterly and distributed to update TMS320 customers on product information.

Information regarding TI DSP products is also available on the Worldwide Web at <http://www.ti.com> uniform resource locator (URL).

5 Electrical Specifications

This section provides the absolute maximum ratings and the recommended operating conditions for the 320VC5421 DSP.

5.1 Absolute Maximum Ratings

The list of absolute maximum ratings are specified over operating case temperature. Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability. All voltage values are with respect to V_{SS} .

| | |
|--|------------------------------|
| Supply voltage I/O range, DV_{DD} | – 0.5 V to 4.0 V |
| Supply voltage core range, CV_{DD} | – 0.5 V to 2.4 V |
| Supply voltage analog PLL range, AV_{DD} | – 0.5 V to 2.4 V |
| Input voltage range, V_I | – 0.5 V to $DV_{DD} + 0.5$ V |
| Output voltage range, V_O | – 0.5 V to $DV_{DD} + 0.5$ V |
| Operating case temperature range, T_C | –40°C to 85°C |
| Storage temperature range T_{stg} | – 65°C to 150°C |

5.2 Recommended Operating Conditions

The device recommended operating conditions are supplied in Table 5–1 and the electrical characteristics over recommended operating case temperature range (unless otherwise noted) are listed in Table 5–2. Figure 5–1 provides the test load circuit values for a 3.3-V device.

Table 5–1. Recommended Operating Conditions

| | | MIN | NOM | MAX | UNIT | |
|-----------|-------------------------------|---|------|--------------|--------------|---------|
| DV_{DD} | Device supply voltage, I/O | 3 | 3.3 | 3.6 | V | |
| CV_{DD} | Device supply voltage, core | 1.75 | 1.80 | 1.98 | V | |
| AV_{DD} | Device supply voltage, PLL | 1.75 | 1.80 | 1.98 | V | |
| V_{SS} | Supply voltage, GND | 0 | | | V | |
| V_{IH} | High-level input voltage, I/O | Schmitt triggered inputs $DV_{DD} = 3.3 \pm 0.3$ V | | $0.7DV_{DD}$ | DV_{DD} | V |
| | | All other inputs | | 2 | DV_{DD} | |
| V_{IL} | Low-level input voltage, I/O | Schmitt triggered inputs $DV_{DD} = 3.3 \pm 0.3$ V | | 0 | $0.3DV_{DD}$ | V |
| | | All other inputs | | 0 | 0.8 | |
| I_{OH} | High-level output current | | | | –300 | μ A |
| I_{OL} | Low-level output current | | | | 1.5 | mA |
| T_C | Operating case temperature | –40 | | | 85 | °C |

5.3 Electrical Characteristics

Table 5–2 describes the electrical characteristics over recommended operating case temperature range (unless otherwise noted).

Table 5–2. Electrical Characteristics

| PARAMETER | | TEST CONDITIONS† | MIN | TYP‡ | MAX | UNIT |
|-----------|--|---|---|------|-----|---------------|
| V_{OH} | High-level output voltage§ | $DV_{DD} = 3.3 \pm 0.3 \text{ V}$, $I_{OH} = \text{MAX}$ | 2.4 | | | V |
| V_{OL} | Low-level output voltage§ | $I_{OL} = \text{MAX}$ | | | 0.4 | V |
| I_{IZ} | Input current in high impedance | $DV_{DD} = \text{MAX}$, $V_I = V_{SS}$ to DV_{DD} | -10 | | 10 | μA |
| I_I | Input current ($V_I = V_{SS}$ to DV_{DD}) | $\overline{\text{TRST}}$ | | | 35 | μA |
| | | See pin descriptions | With internal pullups | -35 | 10 | |
| | | PPD[15:0] | Bus holders enabled, $DV_{DD} = \text{MAX}^*$ | -200 | 200 | |
| | | All other input-only pins | | -10 | 10 | |
| I_{DCC} | Supply current, both core CPUs | $CV_{DD} = 1.8 \text{ V}$, $f_x = 100 \text{ MHz}^{\dagger\dagger}$, $T_C = 25^\circ\text{C}$ | | 90# | | mA |
| I_{DDP} | Supply current, pins | $DV_{DD} = 3.3 \text{ V}$, $f_{\text{clock}} = 100 \text{ MHz}^{\#}$, $T_C = 25^\circ\text{C}^{\parallel}$ | | 54 | | mA |
| I_{DDA} | Supply current, PLL | | | 5 | | mA |
| I_{DDC} | Supply current, standby | IDLE2 | PLL x n mode, 20 MHz input | 2 | | mA |
| | | IDLE3 | PLL x n mode, 20 MHz input | 600 | | μA |
| C_i | Input capacitance | | | 10 | | pF |
| C_o | Output capacitance | | | 10 | | pF |

† For test conditions shown as MIN, MAX, or NOM, use the appropriate value specified in the recommended operating conditions table.

‡ All values are typical unless otherwise specified.

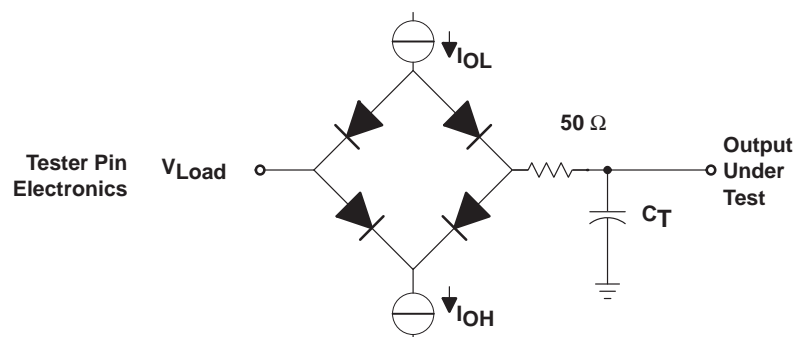
§ All input and output voltage levels except $\overline{\text{RS}}$, $\overline{\text{INT0}}$, $\overline{\text{INT1}}$, $\overline{\text{NMI}}$, CLKIN , BCLKX , BCLKR , $\overline{\text{HAS}}$, $\overline{\text{HCS}}$, $\overline{\text{HDS1}}$, $\overline{\text{HDS2}}$, and $\overline{\text{HPIRS}}$ are LVTTTL-compatible.

$\dagger\dagger$ Clock mode: PLL x 1 with external source

This value is based on 50% usage of MAC and 50% usage of NOP instructions. Actual operating current varies with the program being executed.

\parallel This value was obtained using the following conditions: external memory writes at a rate of 20 million writes per second, $\text{CLKOFF} = 0$, full-duplex operation of all six McBSPs at a rate of 10 million bits per second each, and 15-pF loads on all outputs. For more details on how this calculation is performed, refer to the *Calculation of TMS320LC54x Power Dissipation Application Report* (literature number SPRA164).

* $V_{IL(\text{MIN})} \leq V_I \leq V_{IL(\text{MAX})}$ or $V_{IH(\text{MIN})} \leq V_I \leq V_{IH(\text{MAX})}$



Where:

- I_{OL} = 1.5 mA (all outputs)
- I_{OH} = 300 μA (all outputs)
- V_{Load} = 1.5 V
- C_T = 40 pF typical load circuit capacitance

Figure 5–1. 3.3-V Test Load Circuit

5.4 Package Thermal Resistance Characteristics

Table 5–3 provides the thermal resistance characteristics for the recommended package types used on the 320VC5421 DSP.

Table 5–3. Thermal Resistance Characteristics

| PARAMETER | PGE PACKAGE | UNIT |
|-----------------|-------------|------|
| $R_{\theta JA}$ | 56 | °C/W |
| $R_{\theta JC}$ | 5 | °C/W |

5.5 Timing Parameter Symbology

Timing parameter symbols used in the timing requirements and switching characteristics tables are created in accordance with JEDEC Standard 100. To shorten the symbols, some of the pin names and other related terminology have been abbreviated as follows:

Lowercase subscripts and their meanings:

| | |
|-----|--|
| a | access time |
| c | cycle time (period) |
| d | delay time |
| dis | disable time |
| en | enable time |
| f | fall time |
| h | hold time |
| r | rise time |
| su | setup time |
| t | transition time |
| v | valid time |
| w | pulse duration (width) |
| X | Unknown, changing, or don't care level |

Letters and symbols and their meanings:

| | |
|---|----------------|
| H | High |
| L | Low |
| V | Valid |
| Z | High impedance |

5.6 Clock Options

The frequency of the reference clock provided at the CLKIN pin can be divided by a factor of two or four to generate the internal machine cycle. The selection of the clock mode is described in the software-programmable phase-locked loop (PLL) section.

5.6.1 Divide-By-Two, Divide-By-Four, and Bypass Clock Option (PLL Disabled)

The frequency of the reference clock provided at the CLKIN pin can be divided by a factor of two or four to generate the internal machine cycle. The selection of the clock mode is described in the software-programmable phase-locked loop (PLL) section.

The following timing requirements and switching characteristics tables assume testing over recommended operating conditions and $H = 0.5t_{c(CO)}$ (see Figure 5–2).

Table 5–4. Divide-By-2 and Divide-by-4 Clock Options Timing Requirements

| | MIN | MAX | UNIT |
|---------------------------------------|-----|-----|------|
| $t_{c(CI)}$ Cycle time, CLKIN | 20 | † | ns |
| $t_f(CI)$ Fall time, CLKIN | | 8 | ns |
| $t_r(CI)$ Rise time, CLKIN | | 8 | ns |
| $t_w(CIL)$ Pulse duration, CLKIN low | 5 | | ns |
| $t_w(CIH)$ Pulse duration, CLKIN high | 5 | | ns |

† This device utilizes a fully static design and therefore can operate with $t_{c(CI)}$ approaching ∞ . The device is characterized at frequencies approaching 0 Hz.

Table 5–5. Divide-By-2 and Divide-by-4 Clock Options Switching Characteristics

| PARAMETER | MIN | TYP | MAX | UNIT |
|---|-----|--------------|-----|------|
| $t_{c(CO)}$ Cycle time, CLKOUT | 40 | $2t_{c(CI)}$ | † | ns |
| $t_{c(CO)}$ Cycle time, CLKOUT – bypass mode | 40 | $2t_{c(CI)}$ | † | ns |
| $t_d(CIH-CO)$ Delay time, CLKIN high to CLKOUT high/low | 3 | 6 | 10 | ns |
| $t_f(CO)$ Fall time, CLKOUT | | 2 | | ns |
| $t_r(CO)$ Rise time, CLKOUT | | 2 | | ns |
| $t_w(COL)$ Pulse duration, CLKOUT low | H–2 | H–1 | H+2 | ns |
| $t_w(COH)$ Pulse duration, CLKOUT high | H–2 | H–1 | H+2 | ns |

† This device utilizes a fully static design and therefore can operate with $t_{c(CI)}$ approaching ∞ . The device is characterized at frequencies approaching 0 Hz.

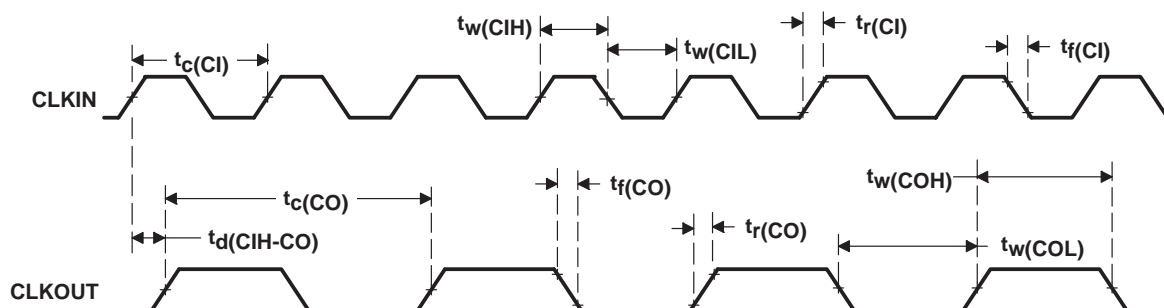


Figure 5–2. External Divide-by-Two Clock Timing

5.6.2 Multiply-By-N Clock Option (PLL Enabled)

The frequency of the reference clock provided at the CLKIN pin can be multiplied by a factor of N to generate the internal machine cycle. The selection of the clock mode and the value of N is described in the software-programmable phase-locked loop (PLL) section.

The following timing requirements and switching characteristics tables assume testing over recommended operating conditions and $H = 0.5t_{c(CO)}$ (see Figure 5–3).

Table 5–6. Multiply-By-N Clock Option Timing Requirements

| | | MIN | MAX | UNIT |
|---------------------------------------|--|-----------------|-----|------|
| $t_{c(CI)}$ Cycle time, CLKIN | Integer PLL multiplier N (N = 1–15) [†] | 20 [‡] | 200 | ns |
| | PLL multiplier N = x.5 [†] | 20 [‡] | 100 | |
| | PLL multiplier N = x.25, x.75 [†] | 20 [‡] | 50 | |
| $t_f(CI)$ Fall time, CLKIN | | | 8 | ns |
| $t_r(CI)$ Rise time, CLKIN | | | 8 | ns |
| $t_w(CIL)$ Pulse duration, CLKIN low | | 5 | | ns |
| $t_w(CIH)$ Pulse duration, CLKIN high | | 5 | | ns |

[†] N = Multiplication factor

[‡] The multiplication factor and minimum CLKIN cycle time should be chosen such that the resulting CLKOUT cycle time is within the specified range ($t_{c(CO)}$)

Table 5–7. Multiply-By-N Clock Option Switching Characteristics

| PARAMETER | | MIN | TYP | MAX | UNIT |
|--|--|-----|-------------------------|-----|---------|
| $t_{c(CO)}$ Cycle time, CLKOUT | | 10 | $t_{c(CI)}/N^{\dagger}$ | | ns |
| $t_d(CI-CO)$ Delay time, CLKIN high/low to CLKOUT high/low | | 4 | 10 | 16 | ns |
| $t_f(CO)$ Fall time, CLKOUT | | | 2 | | ns |
| $t_r(CO)$ Rise time, CLKOUT | | | 2 | | ns |
| $t_w(COL)$ Pulse duration, CLKOUT low | | H–2 | H–1 | H+2 | ns |
| $t_w(COH)$ Pulse duration, CLKOUT high | | H–2 | H–1 | H+2 | ns |
| t_p Transitory phase, PLL lock up time | | | | 30 | μ s |

[†] N = Multiplication factor

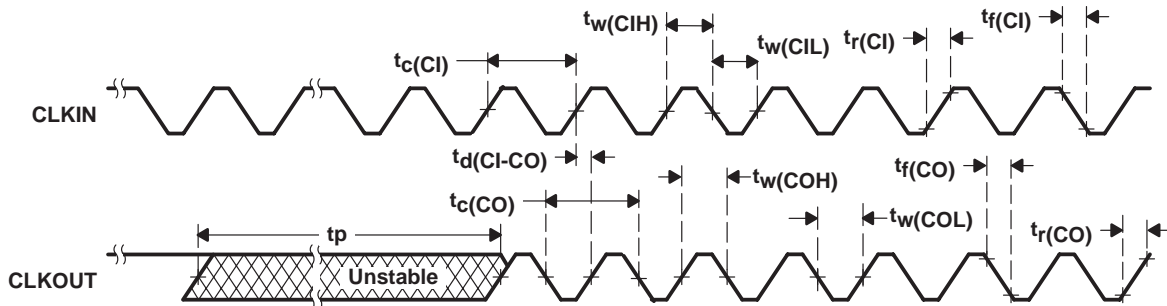


Figure 5–3. External Multiply-by-One Clock Timing

5.7 External Memory Interface Timing

5.7.1 Memory Read

External memory reads can be performed in consecutive or nonconsecutive mode under control of the CONSEC bit in the BSCR. The following timing requirements and switching characteristics tables assume testing over recommended operating conditions with $\overline{\text{MSTRB}} = 0$ and $H = 0.5t_{c(\text{CO})}$ (see Figure 5–4).

Table 5–8. Memory Read Timing Requirements

| | | MIN | MAX | UNIT |
|---------------------------------------|--|-----|-------|------|
| $t_{a(\text{A})\text{M}}$ | Access time, read data access from address valid [†] | | 2H–12 | ns |
| $t_{a(\text{MSTRBL})}$ | Access time, read data access from $\overline{\text{MSTRB}}$ low | | 2H–11 | ns |
| $t_{\text{su}(\text{D})\text{R}}$ | Setup time, read data before CLKOUT low | 9 | | ns |
| $t_{\text{h}(\text{D})\text{R}}$ | Hold time, read data after CLKOUT low | 0 | | ns |
| $t_{\text{h}(\text{A-D})\text{R}}$ | Hold time, read data after address invalid | 0 | | ns |
| $t_{\text{h}(\text{D})\text{MSTRBH}}$ | Hold time, read data after $\overline{\text{MSTRB}}$ high | 0 | | ns |

[†] Address, $\overline{\text{PS}}$, and $\overline{\text{DS}}$ timings are all included in timings referenced as address.

Table 5–9. Memory Read Switching Characteristics

| PARAMETER | | MIN | MAX | UNIT |
|---------------------------------------|---|-----|----------------|------|
| $t_{\text{d}(\text{CLKL-A})}$ | Delay time, CLKOUT low to address valid ^{†‡} | –1 | 5 | ns |
| $t_{\text{d}(\text{CLKH-A})}$ | Delay time, CLKOUT high (transition) to address valid ^{†§} | –1 | 6 | ns |
| $t_{\text{d}(\text{CLKL-MSL})}$ | Delay time, CLKOUT low to $\overline{\text{MSTRB}}$ low | –1 | 4 | ns |
| $t_{\text{d}(\text{CLKL-MSH})}$ | Delay time, CLKOUT low to $\overline{\text{MSTRB}}$ high | –1 | 4 | ns |
| $t_{\text{h}(\text{CLKL-A})\text{R}}$ | Hold time, address valid after CLKOUT low ^{†‡} | –1 | 5 [§] | ns |
| $t_{\text{h}(\text{CLKH-A})\text{R}}$ | Hold time, address valid after CLKOUT high ^{†§} | –1 | 6 [§] | ns |

[†] Address, $\overline{\text{PS}}$, and $\overline{\text{DS}}$ timings are all included in timings referenced as address.

[‡] In the case of a memory read preceded by a memory read

[§] In the case of a memory read preceded by a memory write

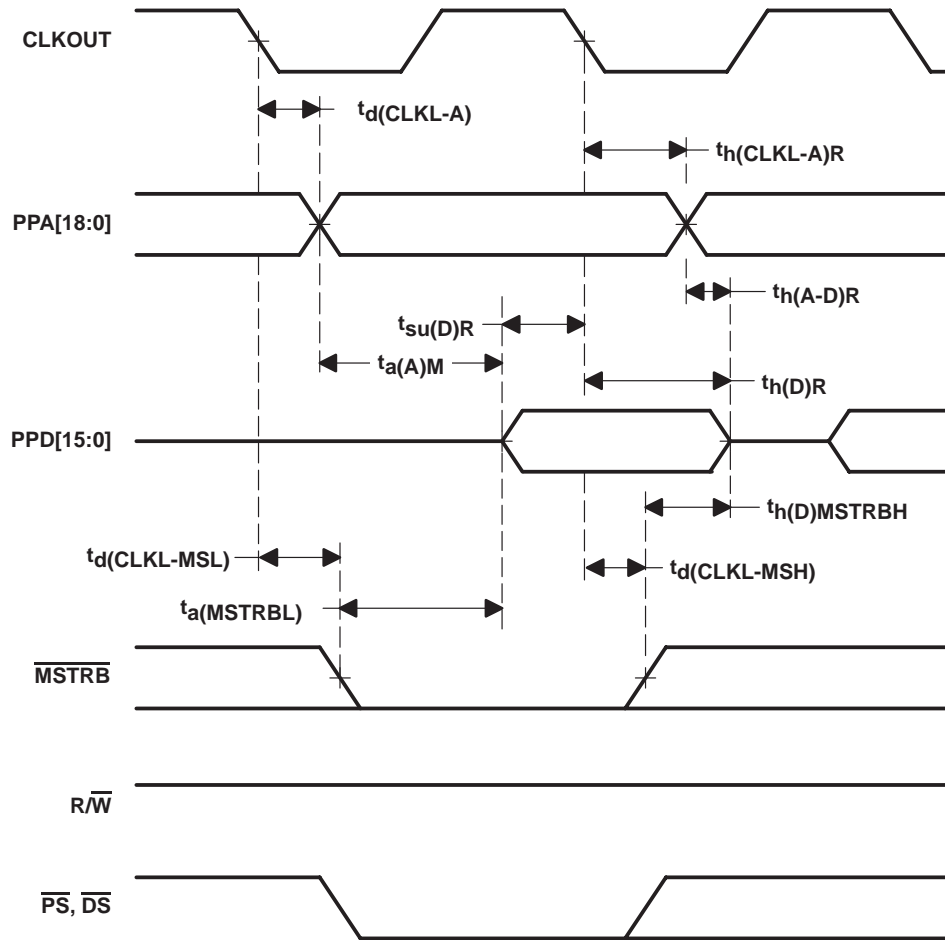


Figure 5-4. Memory Read ($\overline{MSTRB} = 0$)

5.7.2 Memory Write

The following switching characteristics table assumes testing over recommended operating conditions with $\overline{\text{MSTRB}} = 0$ and $H = 0.5t_{c(\text{CO})}$ (see Figure 5–5).

Table 5–10. Memory Write Switching Characteristics

| PARAMETER | MIN | MAX | UNIT |
|----------------------------|-------|------------|------|
| $t_{d(\text{CLKH-A})}$ | – 1 | 6 | ns |
| $t_{d(\text{CLKL-A})}$ | – 1 | 5 | ns |
| $t_{d(\text{CLKL-MSL})}$ | – 1 | 4 | ns |
| $t_{d(\text{CLKL-D}W)$ | 0 | 7 | ns |
| $t_{d(\text{CLKL-MSH})}$ | – 1 | 4 | ns |
| $t_{d(\text{CLKH-RWL})}$ | 0 | 4 | ns |
| $t_{d(\text{CLKH-RWH})}$ | 0 | 4 | ns |
| $t_{d(\text{RWL-MSTRBL})}$ | H – 2 | H + 2 | ns |
| $t_{h(\text{A})W}$ | – 1 | 6 | ns |
| $t_{h(\text{D})MSH}$ | H – 3 | H + 3 \S | ns |
| $t_w(\text{SL})MS$ | 2H–4 | | ns |
| $t_{su(\text{A})W}$ | 2H–4 | | ns |
| $t_{su(\text{D})MSH}$ | 2H–5 | 2H+5 \S | ns |

\dagger Address, $\overline{\text{PS}}$, and $\overline{\text{DS}}$ timings are all included in timings referenced as address.

\ddagger In the case of a memory write preceded by a memory write

\S In the case of a memory write preceded by an I/O cycle

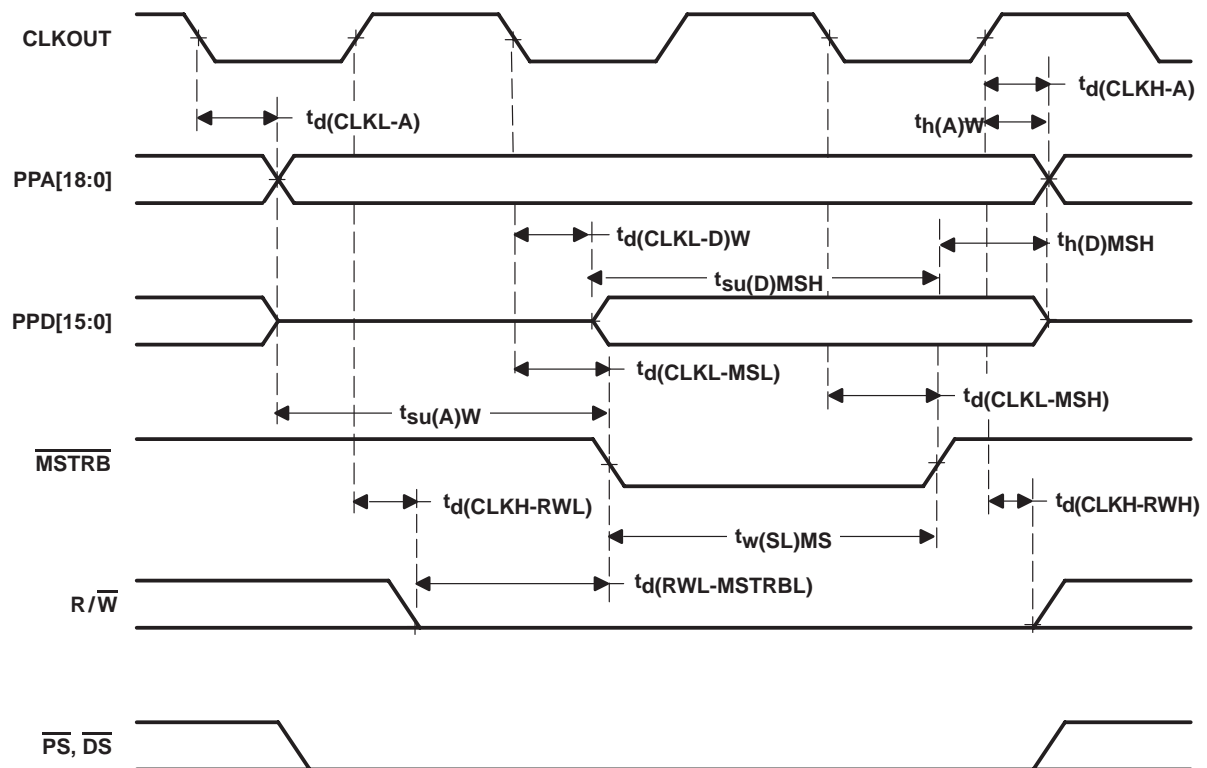


Figure 5–5. Memory Write ($\overline{\text{MSTRB}} = 0$)

5.8 Ready Timing For Externally Generated Wait States

The following timing requirements table assumes testing over recommended operating conditions and $H = 0.5t_{c(CO)}$ (see Figure 5–6 and Figure 5–7).

Table 5–11. Ready Timing Requirements for Externally Generated Wait States†

| | | MIN | MAX | UNIT |
|-------------------|---|-----|------|------|
| $t_{su}(RDY)$ | Setup time, READY before CLKOUT low | 8 | | ns |
| $t_{h}(RDY)$ | Hold time, READY after CLKOUT low | 0 | | ns |
| $t_{v}(RDY)MSTRB$ | Valid time, READY after \overline{MSTRB} low‡ | | 2H–8 | ns |
| $t_{h}(RDY)MSTRB$ | Hold time, READY after \overline{MSTRB} low‡ | 2H | | ns |

† The hardware wait states can be used only in conjunction with the software wait states to extend the bus cycles. To generate wait states by READY, at least two software wait states must be programmed. READY is not sampled until the completion of the internal software wait states.

‡ These timings are included for reference only. The critical timings for READY are those referenced to CLKOUT

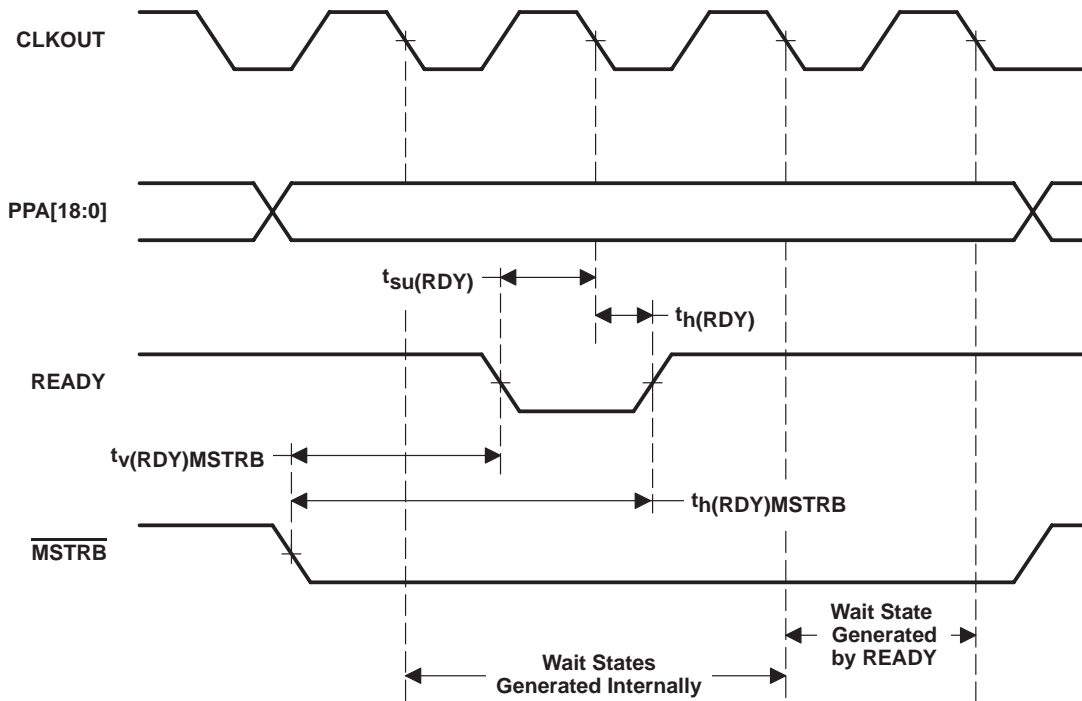


Figure 5–6. Memory Read With Externally Generated Wait States

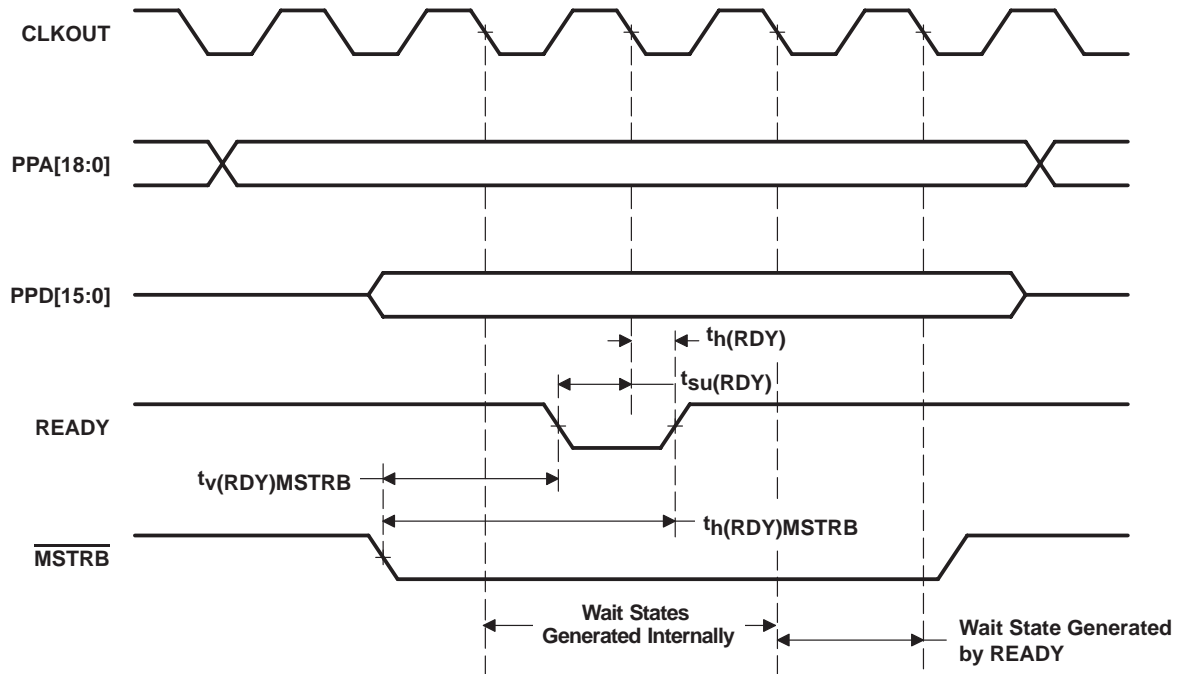


Figure 5–7. Memory Write With Externally Generated Wait States

5.9 Parallel I/O Interface Timing

5.9.1 Parallel I/O Port Read

The following timing requirements and switching characteristics tables assume testing over recommended operating conditions with $\overline{\text{IOSTRB}} = 0$ and $H = 0.5t_{c(\text{CO})}$ (see Figure 5–8).

Table 5–12. Parallel I/O Port Read Timing Requirements

| | | MIN | MAX | UNIT |
|---|---|-----|-------|------|
| $t_{a(\text{A})\text{IO}}$ | Access time, read data access from address valid [†] | | 3H–12 | ns |
| $t_{a(\text{ISTRBL})\text{IO}}$ | Access time, read data access from $\overline{\text{IOSTRB}}$ low | | 2H–11 | ns |
| $t_{\text{su}(\text{D})\text{IOR}}$ | Setup time, read data before CLKOUT high | 9 | | ns |
| $t_{\text{h}(\text{D})\text{IOR}}$ | Hold time, read data after CLKOUT high | 0 | | ns |
| $t_{\text{h}(\text{ISTRBH-D})\text{R}}$ | Hold time, read data after $\overline{\text{IOSTRB}}$ high | 0 | | ns |

[†] Address and $\overline{\text{IS}}$ timings are included in timings referenced as address.

Table 5–13. Parallel I/O Port Read Switching Characteristics

| PARAMETER | MIN | MAX | UNIT | |
|------------------------------------|--|-----|------|----|
| $t_{\text{d}(\text{CLKL-A})}$ | Delay time, CLKOUT low to address valid [†] | –1 | 5 | ns |
| $t_{\text{d}(\text{CLKH-ISTRBL})}$ | Delay time, CLKOUT high to $\overline{\text{IOSTRB}}$ low | 0 | 5 | ns |
| $t_{\text{d}(\text{CLKH-ISTRBH})}$ | Delay time, CLKOUT high to $\overline{\text{IOSTRB}}$ high | 0 | 5 | ns |
| $t_{\text{h}(\text{A})\text{IOR}}$ | Hold time, address after CLKOUT low [†] | –1 | 5 | ns |

[†] Address and $\overline{\text{IS}}$ timings are included in timings referenced as address.

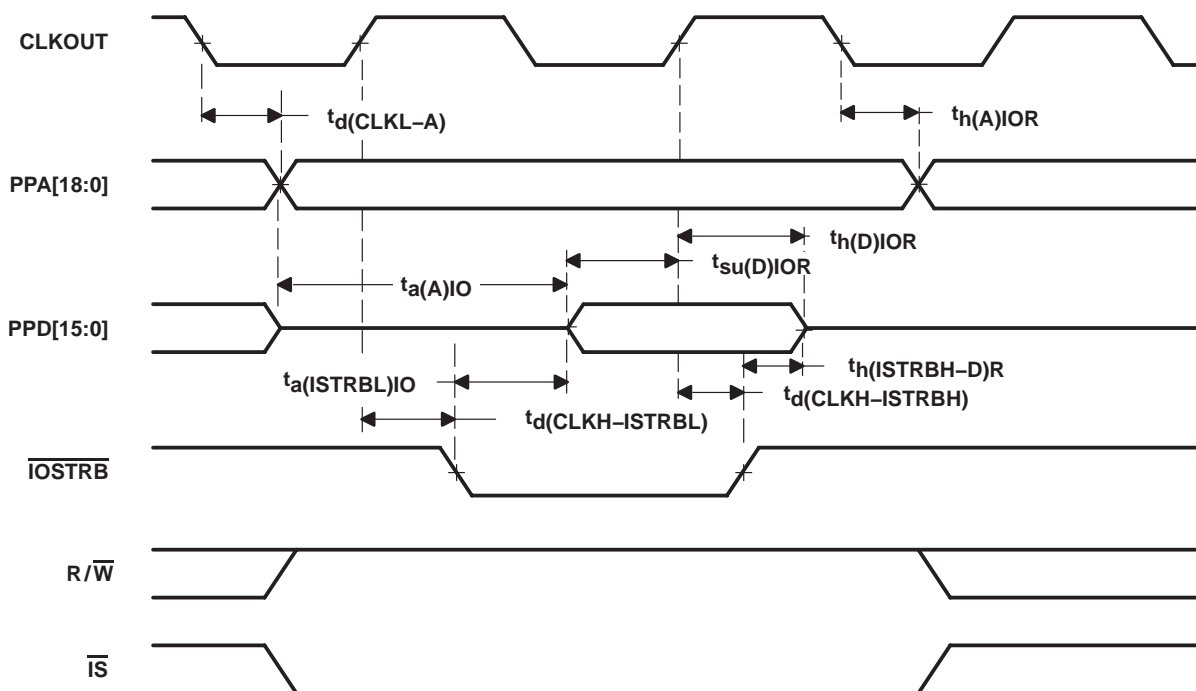


Figure 5–8. Parallel I/O Port Read ($\overline{\text{IOSTRB}}=0$)

5.9.2 Parallel I/O Port Write

The following switching characteristics table assumes testing over recommended operating conditions with $\overline{\text{IOSTRB}} = 0$ and $H = 0.5t_{c(\text{CO})}$ (see Figure 5–9).

Table 5–14. Parallel I/O Port Write Switching Characteristics

| PARAMETER | | MIN | MAX | UNIT |
|---|--|-----|-----|------|
| $t_{d(\text{CLKL-A})}$ | Delay time, CLKOUT low to address valid† | -1 | 5 | ns |
| $t_{d(\text{CLKH-ISTRBL})}$ | Delay time, CLKOUT high to $\overline{\text{IOSTRB}}$ low | 0 | 5 | ns |
| $t_{d(\text{CLKH-D})\text{IOW}}$ | Delay time, CLKOUT high to write data valid | H-5 | H+5 | ns |
| $t_{d(\text{CLKH-ISTRBH})}$ | Delay time, CLKOUT high to $\overline{\text{IOSTRB}}$ high | 0 | 5 | ns |
| $t_{d(\text{CLKL-RWL})}$ | Delay time, CLKOUT low to $\overline{\text{R/W}}$ low | 0 | 4 | ns |
| $t_{d(\text{CLKL-RWH})}$ | Delay time, CLKOUT low to $\overline{\text{R/W}}$ high | 0 | 4 | ns |
| $t_{h(\text{A})\text{IOW}}$ | Hold time, address valid after CLKOUT low† | -1 | 5 | ns |
| $t_{h(\text{D})\text{IOW}}$ | Hold time, write data after $\overline{\text{IOSTRB}}$ high | H-3 | H+7 | ns |
| $t_{\text{su}(\text{D})\text{IOSTRBH}}$ | Setup time, write data before $\overline{\text{IOSTRB}}$ high | H-5 | H+1 | ns |
| $t_{\text{su}(\text{A})\text{IOSTRBL}}$ | Setup time, address valid before $\overline{\text{IOSTRB}}$ low† | H-5 | H+3 | ns |

† Address and $\overline{\text{IS}}$ timings are included in timings referenced as address.

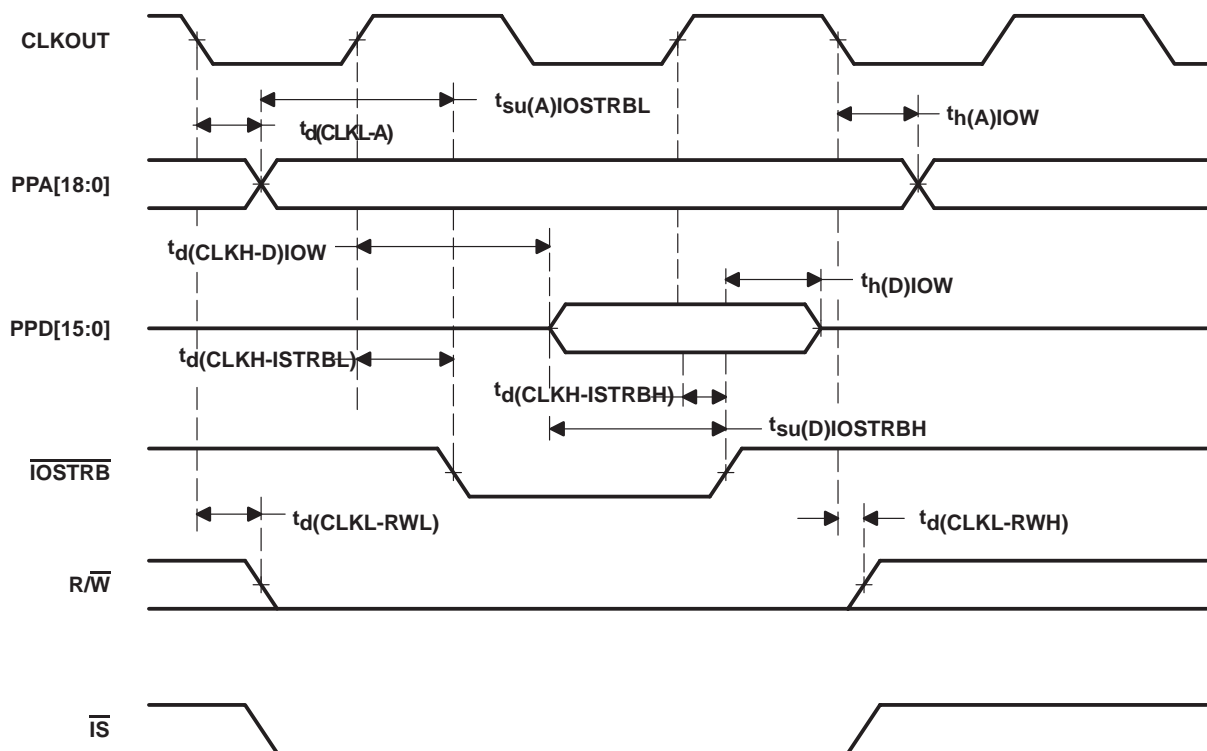


Figure 5–9. Parallel I/O Port Write ($\overline{\text{IOSTRB}}=0$)

5.10 Externally Generated Wait States

5.10.1 I/O Port Read and Write With Externally Generated Wait States

The following timing requirements table assumes testing over recommended operating conditions and $H = 0.5t_{c(CO)}$ (see Figure 5–10 and Figure 5–11).

Table 5–15. Externally Generated Wait States Timing Requirements†

| | | MIN | MAX | UNIT |
|--------------------|--|-----|------|------|
| $t_{su(RDY)}$ | Setup time, READY before CLKOUT low | 8 | | ns |
| $t_h(RDY)$ | Hold time, READY after CLKOUT low | 0 | | ns |
| $t_{v(RDY)IOSTRB}$ | Valid time, READY after \overline{IOSTRB} low‡ | | 3H–9 | ns |
| $t_h(RDY)IOSTRB$ | Hold time, READY after \overline{IOSTRB} low‡ | 3H | | ns |

† The hardware wait states can be used only in conjunction with the software wait states to extend the bus cycles. To generate wait states using READY, at least two software wait states must be programmed.

‡ These timings are included for reference only. The critical timings for READY are those referenced to CLKOUT.

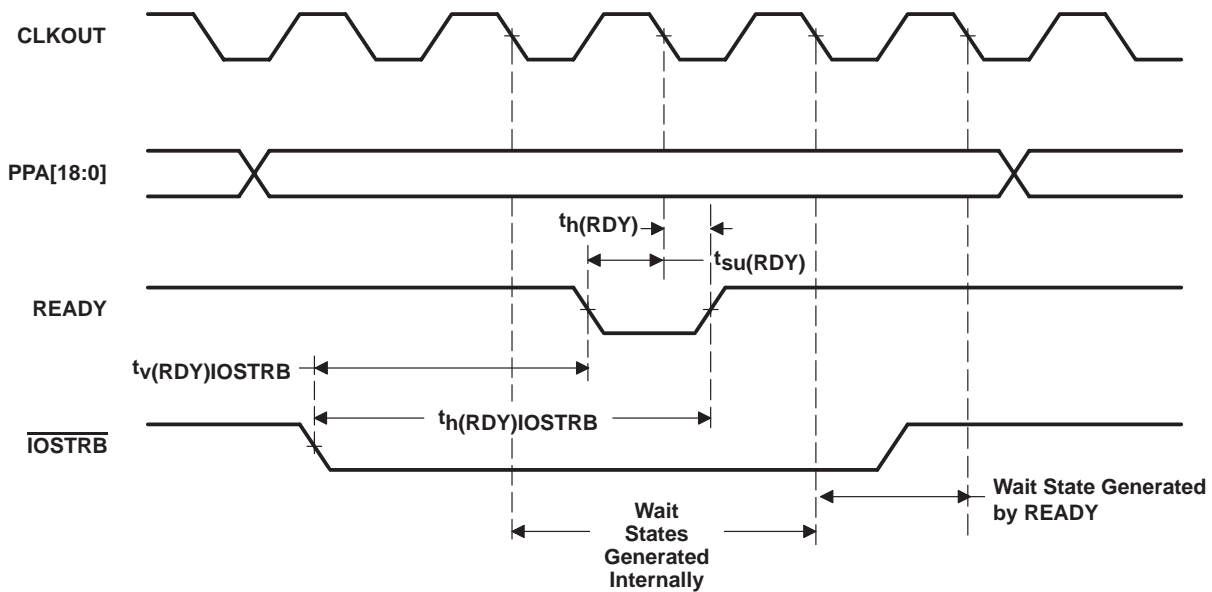


Figure 5–10. I/O Port Read With Externally Generated Wait States

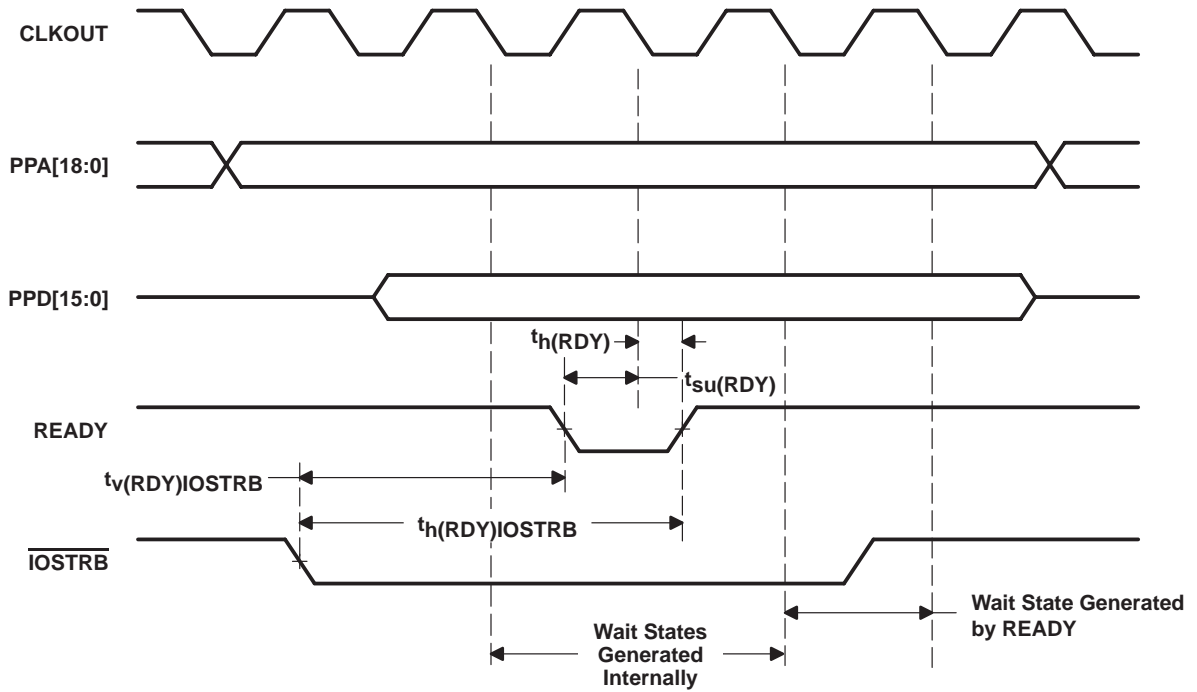


Figure 5–11. I/O Port Write With Externally Generated Wait States

5.11 Reset, $\overline{\text{BIO}}$, Interrupt, and $\overline{\text{MP/MC}}$ Timings

The following timing requirements table assumes testing over recommended operating conditions and $H = 0.5t_{c(\text{CO})}$ (see Figure 5–12, Figure 5–13, and Figure 5–14).

Table 5–16. Reset, $\overline{\text{BIO}}$, Interrupt, and $\overline{\text{MP/MC}}$ Timing Requirements

| | | MIN | MAX | UNIT |
|---------------------------------------|--|------|-------|------|
| $t_{\text{h}(\text{RS})}$ | Hold time, $\overline{\text{RS}}$ after CLKOUT low | 0 | | ns |
| $t_{\text{h}(\text{BIO})}$ | Hold time, $\overline{\text{BIO}}$ after CLKOUT low | 0 | | ns |
| $t_{\text{h}(\text{INT})}$ | Hold time, $\overline{\text{INTn}}$, $\overline{\text{NMI}}$, after CLKOUT low [†] | 0 | | ns |
| $t_{\text{w}(\text{RSL})}$ | Pulse duration, $\overline{\text{RS}}$ low ^{‡§} | 4H+5 | | ns |
| $t_{\text{w}(\text{BIO})\text{A}}$ | Pulse duration, $\overline{\text{BIO}}$ low, asynchronous [†] | 5H | | ns |
| $t_{\text{w}(\text{INTH})\text{A}}$ | Pulse duration, $\overline{\text{INTn}}$, $\overline{\text{NMI}}$ high (asynchronous) [†] | 4H | | ns |
| $t_{\text{w}(\text{INTL})\text{A}}$ | Pulse duration, $\overline{\text{INTn}}$, $\overline{\text{NMI}}$ low (asynchronous) [†] | 4H | | ns |
| $t_{\text{w}(\text{INTL})\text{WKP}}$ | Pulse duration, $\overline{\text{INTn}}$, $\overline{\text{NMI}}$ low for IDLE2/IDLE3 wakeup [†] | 8 | | ns |
| $t_{\text{w}(\text{XIO})}$ | Pulse duration, XIO switched | 4H | | ns |
| $t_{\text{en}(\text{XIO})}$ | Enable time, after XIO switched | | 4H+10 | ns |
| $t_{\text{su}(\text{RS})}$ | Setup time, $\overline{\text{RS}}$ before CLKIN low [§] | 5 | | ns |
| $t_{\text{su}(\text{BIO})}$ | Setup time, $\overline{\text{BIO}}$ before CLKOUT low | 9 | 12 | ns |
| $t_{\text{su}(\text{INT})}$ | Setup time, $\overline{\text{INTn}}$, $\overline{\text{NMI}}$, $\overline{\text{RS}}$ before CLKOUT low | 9 | 13 | ns |

[†] The external interrupts ($\overline{\text{INT0}}\text{--}\overline{\text{INT1}}$, $\overline{\text{NMI}}$) are synchronized to the core CPU by way of a two flip-flop synchronizer which samples these inputs with consecutive falling edges of CLKOUT. The input to the interrupt pins is required to represent a 1-0-0 sequence at the timing that is corresponding to a three-CLKOUT sampling sequence.

[‡] If the PLL mode is selected, then at power-on sequence, or at wakeup from IDLE3, $\overline{\text{RS}}$ must be held low for at least 50 μs to ensure synchronization and lock-in of the PLL.

[§] $\overline{\text{RS}}$ can cause a change in clock frequency, changing the value of H (see the software-programmable phase-locked loop (PLL) section).

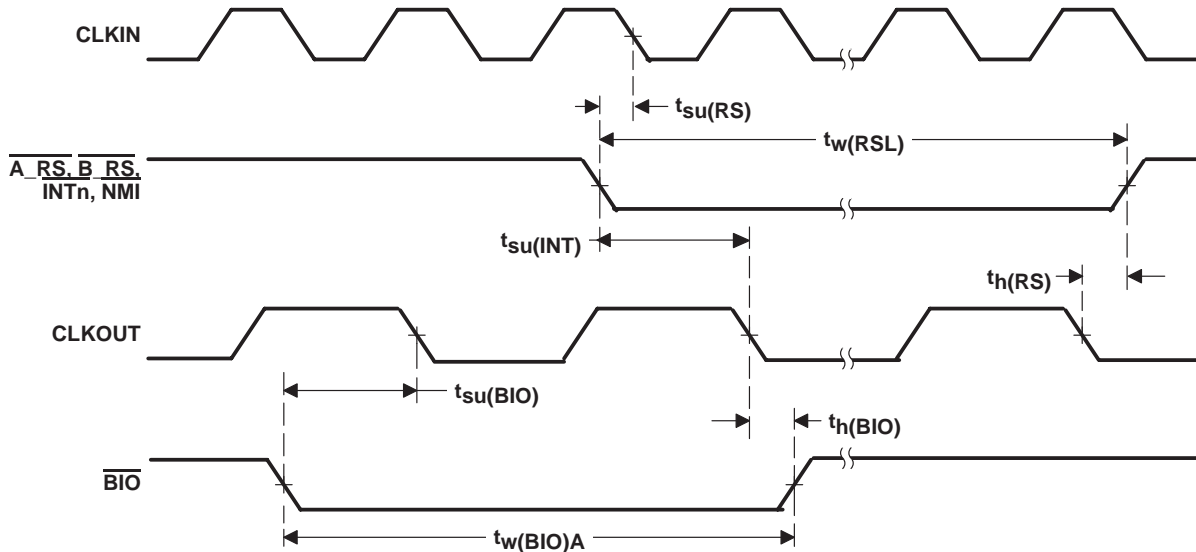


Figure 5–12. Reset and $\overline{\text{BIO}}$ Timings

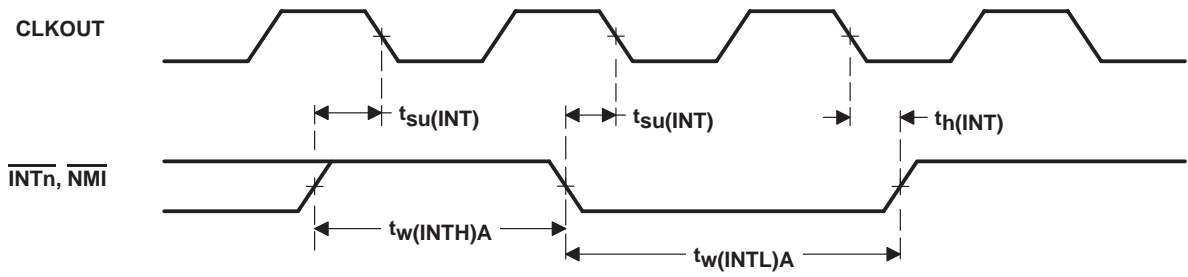


Figure 5-13. Interrupt Timing

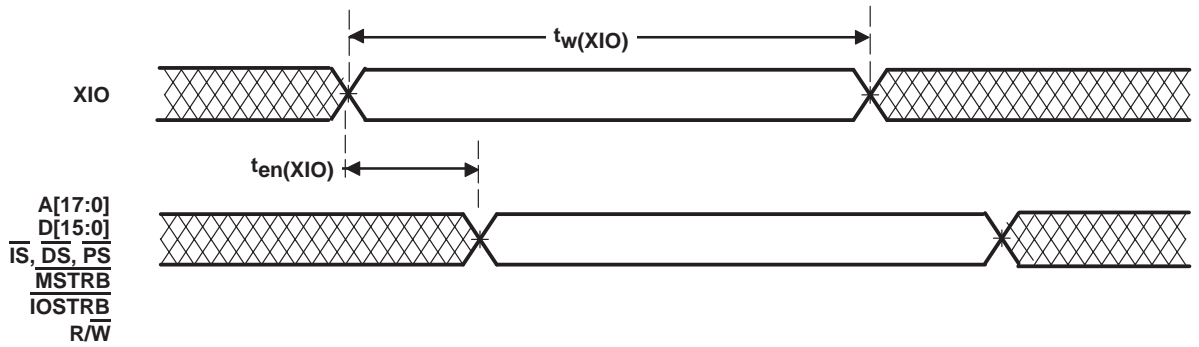


Figure 5-14. XIO Timing

5.12 $\overline{\text{HOLD}}$ and $\overline{\text{HOLDA}}$ Timings

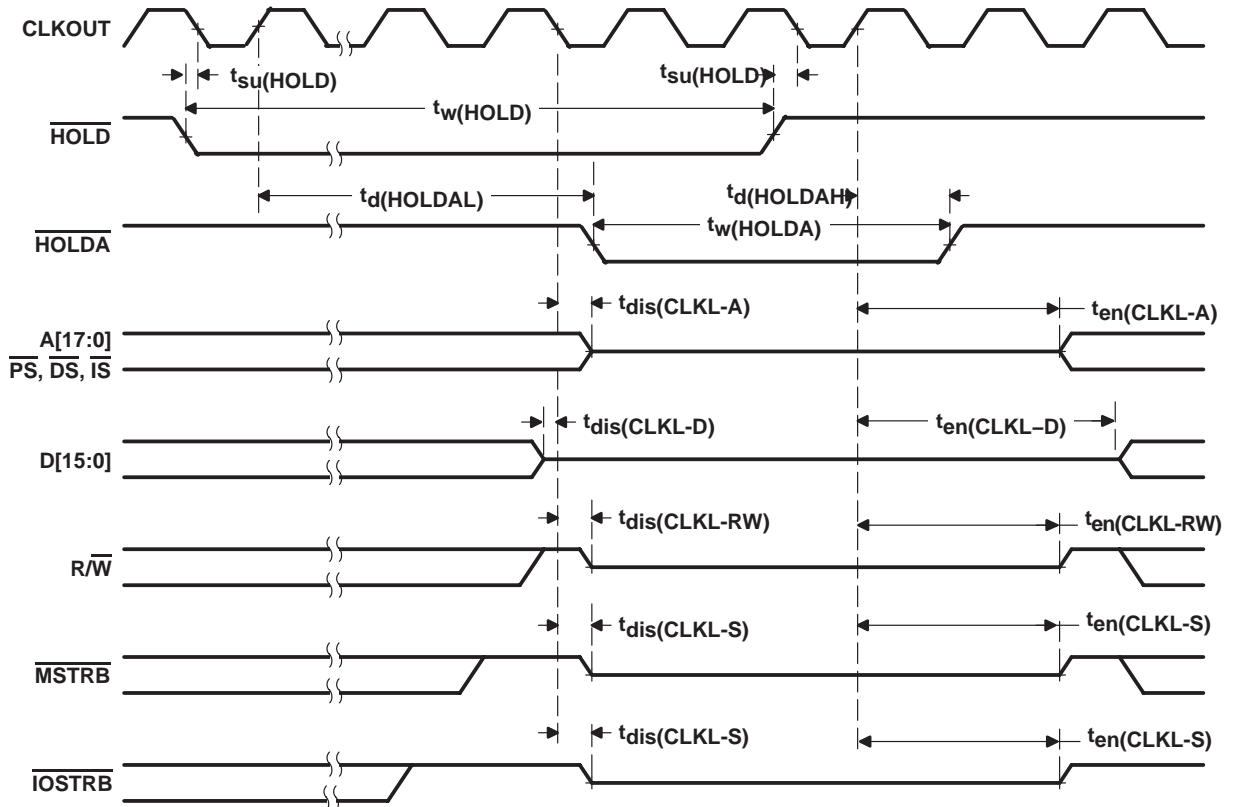
The following timing requirements and switching characteristics tables assume testing over recommended operating conditions and $H = 0.5t_{c(CO)}$ (see Figure 5–15).

Table 5–17. $\overline{\text{HOLD}}$ and $\overline{\text{HOLDA}}$ Timing Requirements

| | | MIN | MAX | UNIT |
|----------------------------------|---|-------|-----|------|
| $t_w(\overline{\text{HOLD}})$ | Pulse duration, $\overline{\text{HOLD}}$ low | 4H+10 | | ns |
| $t_{su}(\overline{\text{HOLD}})$ | Setup time, $\overline{\text{HOLD}}$ low/high before CLKOUT low | 8 | | ns |

Table 5–18. $\overline{\text{HOLD}}$ and $\overline{\text{HOLDA}}$ Switching Characteristics

| PARAMETER | | MIN | MAX | UNIT |
|--|---|------|-------|------|
| $t_{dis}(\text{CLKL-A})$ | Disable time, address, $\overline{\text{PS}}$, $\overline{\text{DS}}$, $\overline{\text{IS}}$ high impedance from CLKOUT high | | 5 | ns |
| $t_{dis}(\text{CLKL-RW})$ | Disable time, $\overline{\text{R/W}}$ high impedance from CLKOUT high | | 5 | ns |
| $t_{dis}(\text{CLKL-S})$ | Disable time, $\overline{\text{MSTRB}}$, $\overline{\text{IOSTRB}}$ high impedance from CLKOUT high | | 5 | ns |
| $t_{dis}(\text{CLKL-D})$ | Disable time, Data from CLKOUT high | | 5 | ns |
| $t_{en}(\text{CLKL-A})$ | Enable time, address, $\overline{\text{PS}}$, $\overline{\text{DS}}$, $\overline{\text{IS}}$ from CLKOUT high | | 2H+5 | ns |
| $t_{en}(\text{CLKL-D})$ | Enable time, Data from CLKOUT high | | 2H+5 | ns |
| $t_{en}(\text{CLKL-RW})$ | Enable time, $\overline{\text{R/W}}$ enabled from CLKOUT high | | 2H+5 | ns |
| $t_{en}(\text{CLKL-S})$ | Enable time, $\overline{\text{MSTRB}}$, $\overline{\text{IOSTRB}}$ enabled from CLKOUT high | 1 | 2H+5 | ns |
| $t_d(\overline{\text{HOLDA}})$ | Delay time, $\overline{\text{HOLDA}}$ low after CLKOUT high | 0 | 11H+5 | ns |
| $t_d(\overline{\text{HOLDA}}\text{H})$ | Delay time, $\overline{\text{HOLDA}}$ high after CLKOUT high | 0 | 5 | ns |
| $t_w(\overline{\text{HOLDA}})$ | Pulse duration, $\overline{\text{HOLDA}}$ low duration | 2H–3 | | ns |



NOTE A: A[17:16] apply to DMA accesses to extended DATA and PROGRAM memory. The CPU has access to **only** extended PROGRAM memory.

Figure 5–15. \overline{HOLD} and \overline{HOLDA} Timings (HM = 1)

5.13 External Flag (XF) and TOUT Timings

The following switching characteristics table assumes testing over recommended operating conditions and

$H = 0.5t_{c(CO)}$ (see Figure 5–16 and Figure 5–17).

Table 5–19. External Flag (XF) and TOUT Switching Characteristics

| PARAMETER | | MIN | MAX | UNIT |
|--------------|--------------------------------------|------|------|------|
| $t_d(XF)$ | Delay time, CLKOUT low to XF high | -1 | 4 | ns |
| | Delay time, CLKOUT low to XF low | 0 | 4 | |
| $t_d(TOUTH)$ | Delay time, CLKOUT high to TOUT high | -1 | 5 | ns |
| $t_d(TOURL)$ | Delay time, CLKOUT high to TOUT low | -1 | 5 | ns |
| $t_w(TOUT)$ | Pulse duration, TOUT | 2H-5 | 2H+2 | ns |

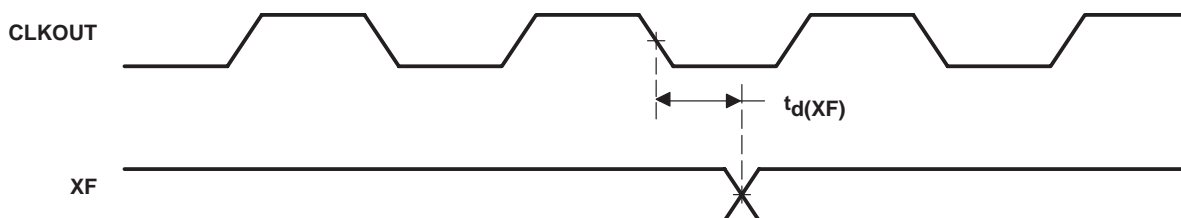


Figure 5–16. External Flag (XF) Timing

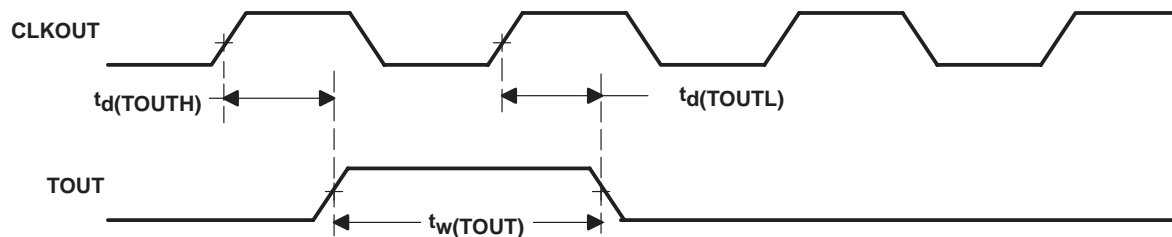


Figure 5–17. Timer (TOUT) Timing

5.14 General-Purpose I/O Timing

The following timing requirements and switching characteristics tables assume testing over recommended operating conditions (see Figure 5–18).

Table 5–20. General-Purpose I/O Timing Requirements

| | | MIN | MAX | UNIT |
|---------------------------|--|-----|-----|------|
| $t_{su}(\text{GPIO-COH})$ | Setup time, GPIOx input valid before CLKOUT high, GPIOx configured as general-purpose input. | 7 | | ns |
| $t_h(\text{GPIO-COH})$ | Hold time, GPIOx input valid after CLKOUT high, GPIOx configured as general-purpose input. | 0 | | ns |

Table 5–21. General-Purpose I/O Switching Characteristics

| PARAMETER | | MIN | MAX | UNIT |
|------------------------|---|-----|-----|------|
| $t_d(\text{COH-GPIO})$ | Delay time, CLKOUT high to GPIOx output change. GPIOx configured as general-purpose output. | –1 | 5 | ns |

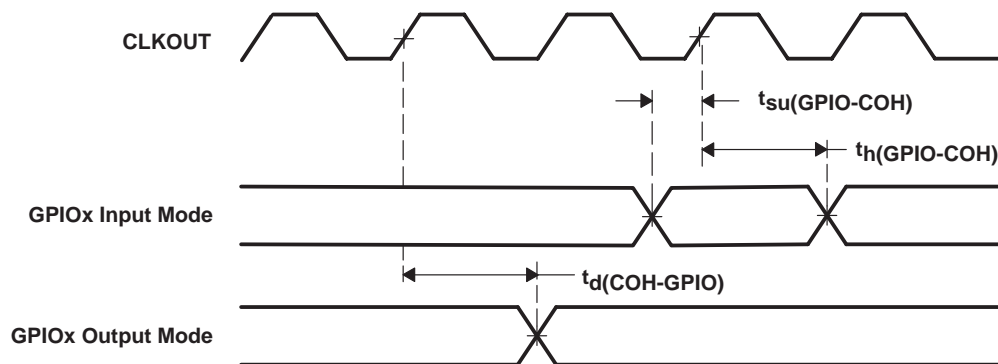


Figure 5–18. GPIO Timings

5.15 Multichannel Buffered Serial Port (McBSP) Timing

5.15.1 McBSP Transmit and Receive Timings

The following timing requirements and switching characteristics tables assume testing over recommended operating conditions and $H = 0.5t_{c(CO)}$ (see Figure 5–19 and Figure 5–20).

Table 5–22. McBSP Transmit and Receive Timing Requirements†

| | | | MIN | MAX | UNIT |
|-----------------------------|---|-------------|-----|-----|------|
| $t_c(\text{BCKRX})$ | Cycle time, BCLKR/X | BCLKR/X ext | 4H | | ns |
| $t_w(\text{BCKRX})$ | Pulse duration, BCLKR/X low or BCLKR/X high | BCLKR/X ext | 6 | | ns |
| $t_h(\text{BCKRL-BFRH})$ | Hold time, external BFSR high after BCLKR low | BCLKR int | 0 | | ns |
| | | BCLKR ext | 4 | | |
| $t_h(\text{BCKRL-BDRV})$ | Hold time, BDR valid after BCLKR low | BCLKR int | 0 | | ns |
| | | BCLKR ext | 5 | | |
| $t_h(\text{BCKXL-BFXH})$ | Hold time, external BFSX high after BCLKX low | BCLKX int | 0 | | ns |
| | | BCLKX ext | 4 | | |
| $t_{su}(\text{BFRH-BCKRL})$ | Setup time, external BFSR high before BCLKR low | BCLKR int | 10 | | ns |
| | | BCLKR ext | 4 | | |
| $t_{su}(\text{BDRV-BCKRL})$ | Setup time, BDR valid before BCLKR low | BCLKR int | 10 | | ns |
| | | BCLKR ext | 3 | | |
| $t_{su}(\text{BFXH-BCKXL})$ | Setup time, external BFSX high before BCLKX low | BCLKX int | 10 | | ns |
| | | BCLKX ext | 6 | | |
| $t_r(\text{BCKRX})$ | Rise time, BCLKR/X | BCLKR/X ext | | 8 | ns |
| $t_f(\text{BCKRX})$ | Fall time, BCLKR/X | BCLKR/X ext | | 8 | ns |

† Polarity bits CLKRP = CLKXP = FSRP = FSXP = 0. If the polarity of any of the signals is inverted, then the timing references of that signal are also inverted.

Table 5–23. McBSP Transmit and Receive Switching Characteristics†

| PARAMETER | | | MIN | MAX | UNIT | |
|--------------------------------------|---|-------------|---------------|---------------|------|-------|
| $t_c(\text{BCKRX})$ | Cycle time, BCLKR/X | BCLKR/X int | 4H | | ns | |
| $t_w(\text{BCKRXH})$ | Pulse duration, BCLKR/X high | BCLKR/X int | $D-4\ddagger$ | $D+1\ddagger$ | ns | |
| $t_w(\text{BCKRXL})$ | Pulse duration, BCLKR/X low | BCLKR/X int | $C-4\ddagger$ | $C+1\ddagger$ | ns | |
| $t_d(\text{BCKRH-BFRV})$ | Delay time, BCLKR high to internal BFSR valid | BCLKR int | -3 | 3 | ns | |
| $t_d(\text{BCKXH-BFXV})$ | Delay time, BCLKX high to internal BFSX valid | BCLKX int | -3 | 8 | ns | |
| | | BCLKX ext | 2 | 15 | | |
| $t_{\text{dis}}(\text{BCKXH-BDXHZ})$ | Disable time, BCLKX high to BDX high impedance following last data bit | BCLKX int | -8 | 3 | ns | |
| | | BCLKX ext | 1 | 12 | | |
| $t_d(\text{BCKXH-BDXV})$ | Delay time, BCLKX high to BDX valid. This applies to all bits except the first bit transmitted. | BCLKX int | -1 | 11 | ns | |
| | | BCLKX ext | 4 | 20 | | |
| | Delay time, BCLKX high to BDX valid.§ | DXENA = 0 | BCLKX int | | | 11 |
| | | | BCLKX ext | | | 20 |
| | Only applies to first bit transmitted when in Data Delay 1 or 2 (XDATDLY=01b or 10b) modes | DXENA = 1 | BCLKX int | | | 4H+6 |
| | | | BCLKX ext | | | 4H+15 |
| $t_{\text{en}}(\text{BCKXH-BDX})$ | Enable time, BCLKX high to BDX driven.§ Only applies to first bit transmitted when in Data Delay 1 or 2 (XDATDLY=01b or 10b) modes | DXENA = 0 | BCLKX int | 5 | ns | |
| | | | BCLKX ext | 16 | | |
| | | DXENA = 1 | BCLKX int | 4H | | |
| | | | BCLKX ext | 4H+12 | | |
| $t_d(\text{BFXH-BDXV})$ | Delay time, BFSX high to BDX valid.§ Only applies to first bit transmitted when in Data Delay 0 (XDATDLY=00b) mode. | DXENA = 0 | BFSX int | 9 | ns | |
| | | | BFSX ext | 15 | | |
| | | DXENA = 1 | BFSX int | 4H | | |
| | | | BFSX ext | 4H+15 | | |
| $t_{\text{en}}(\text{BFXH-BDX})$ | Enable time, BFSX high to BDX driven.§ Only applies to first bit transmitted when in Data Delay 0 (XDATDLY=00b) mode | DXENA = 0 | BFSX int | 2 | ns | |
| | | | BFSX ext | 14 | | |
| | | DXENA = 1 | BFSX int | 4H-1 | | |
| | | | BFSX ext | 2H+5 | | |

† Polarity bits CLKRP = CLKXP = FSRP = FSXP = 0. If the polarity of any of the signals is inverted, then the timing references of that signal are also inverted.

‡ $T = \text{BCLKRX period} = (1 + \text{CLKGDV}) * 2H$

$C = \text{BCLKRX low pulse width} = T/2$ when CLKGDV is odd or zero and $= (\text{CLKGDV}/2) * 2H$ when CLKGDV is even

$D = \text{BCLKRX high pulse width} = T/2$ when CLKGDV is odd or zero and $= (\text{CLKGDV}/2 + 1) * 2H$ when CLKGDV is even

§ See the *TMS320C54x DSP Reference Set, Volume 5: Enhanced Peripherals* (literature number SPRU302) for a description of the DX enable (DXENA) and data delay features of the McBSP.

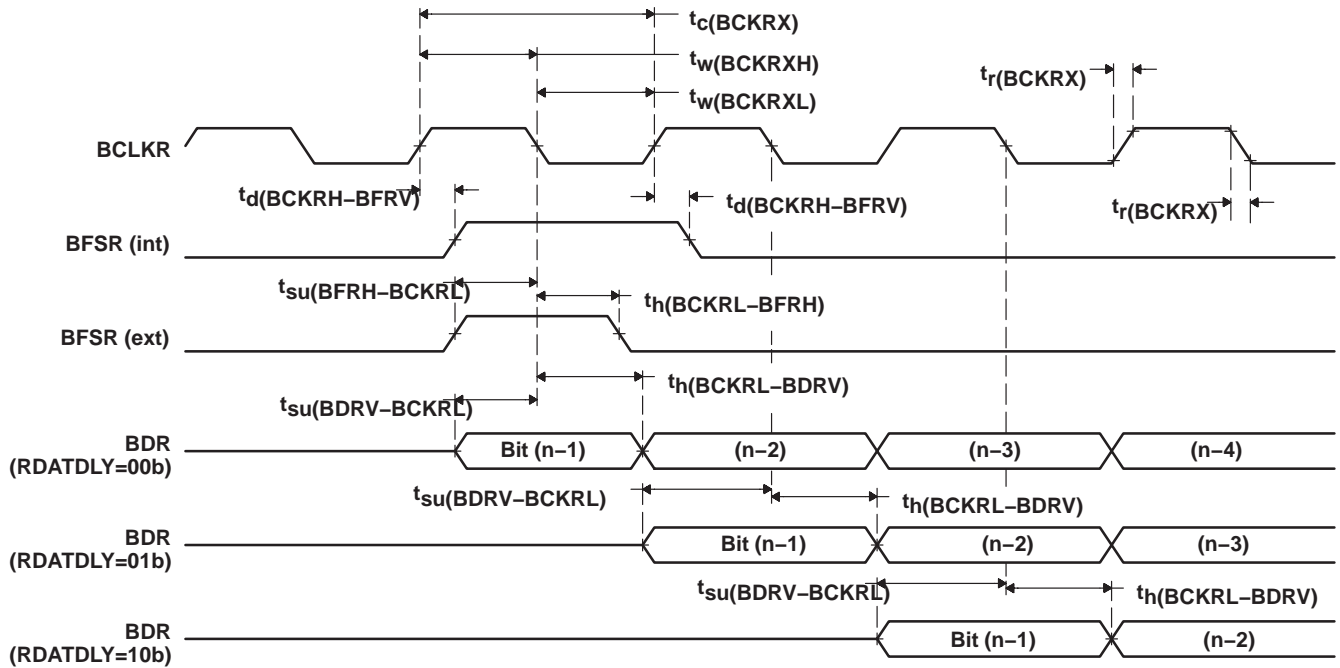


Figure 5–19. McBSP Receive Timings

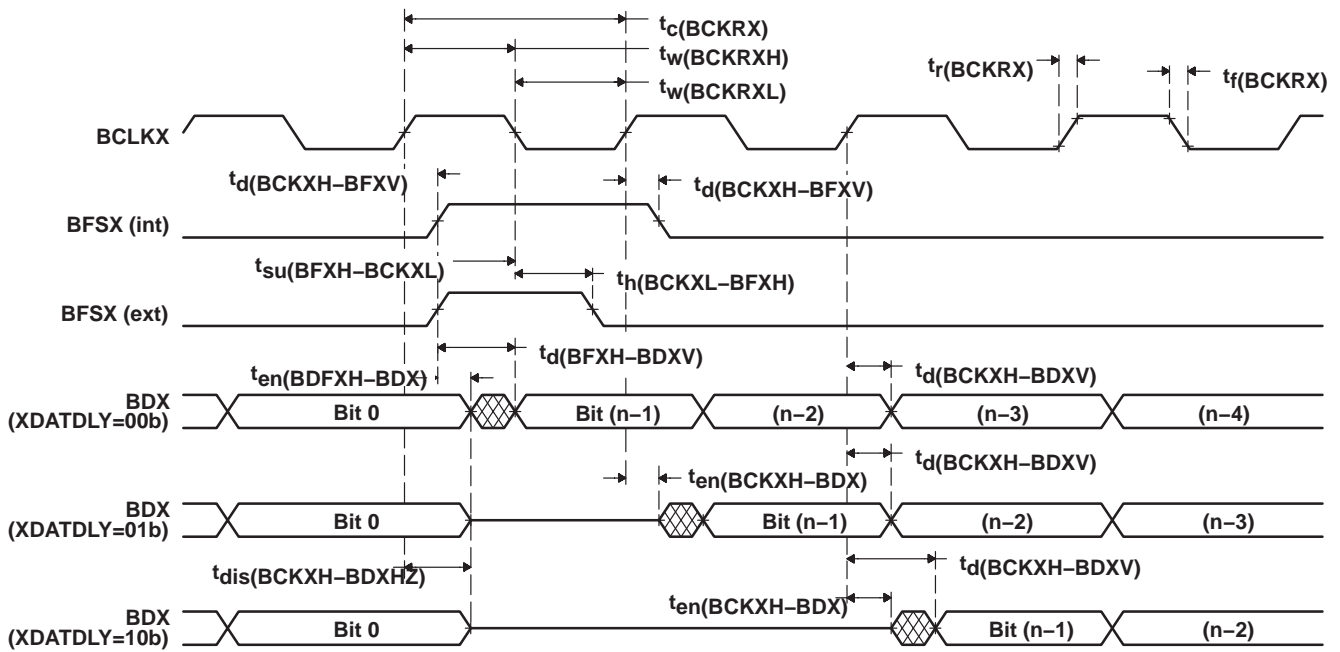


Figure 5–20. McBSP Transmit Timings

5.15.2 McBSP Transmit and Receive Timing Using CLKRX as a Clock Source Input to the Sample Rate Generator (SRGR)

The 5421 McBSP has been enhanced to allow the use of an external clock source as an input to the sample rate generator (SRGR). This capability is enabled by reconfiguring either the transmit shift clock (BCLKX), or the receive shift clock (BCLKR) to function as the input clock to the SRGR. When the McBSP is used in this mode, the output of the SRGR is then used as a common shift clock for both the receive and transmit sections of the serial port. This clock is output on the other of these two pins. Therefore, if BCLKX is reconfigured as the SRGR input, then BCLKR is used as the shift clock for both the transmit and receive sections of the McBSP. If BCLKR is reconfigured as the SRGR input, then BCLKX is used as the shift clock for both the transmit and receive sections of the McBSP. The relevant timings for this mode of operation are depicted in Figure 5–21. The other timings for serial port operations are the same as when using an internal clock source as described in the standard McBSP transmit and receive timings presented in section 5.15.1.

The following timing requirements and switching characteristics tables assume testing over recommended operating conditions and $H = 0.5t_{c(CO)}$ (see Figure 5–21).

Table 5–24. McBSP Sample Rate Generator Timing Requirements

| | | MIN | MAX | UNIT |
|---------------------|---------------------------------------|-----|-----|------|
| $t_c(\text{BCKS})$ | Cycle time, SRGR clock input | 2H | | ns |
| $t_w(\text{BCKSH})$ | Pulse duration, SRGR clock input high | H–4 | H+1 | ns |
| $t_w(\text{BCKSL})$ | Pulse duration, SRGR clock input low | H–4 | H+1 | ns |
| $t_r(\text{BCKS})$ | Rise time, SRGR clock input | | 8 | ns |
| $t_f(\text{BCKS})$ | Fall time, SRGR clock input | | 8 | ns |

Table 5–25. McBSP Sample Rate Generator Switching Characteristics

| PARAMETER | MIN | MAX | UNIT | |
|-----------------------------|--|-----|------|----|
| $t_d(\text{BCKSH-BCLKRXH})$ | Delay time, from SRGR clock input to SRGR output | 3 | 13 | ns |

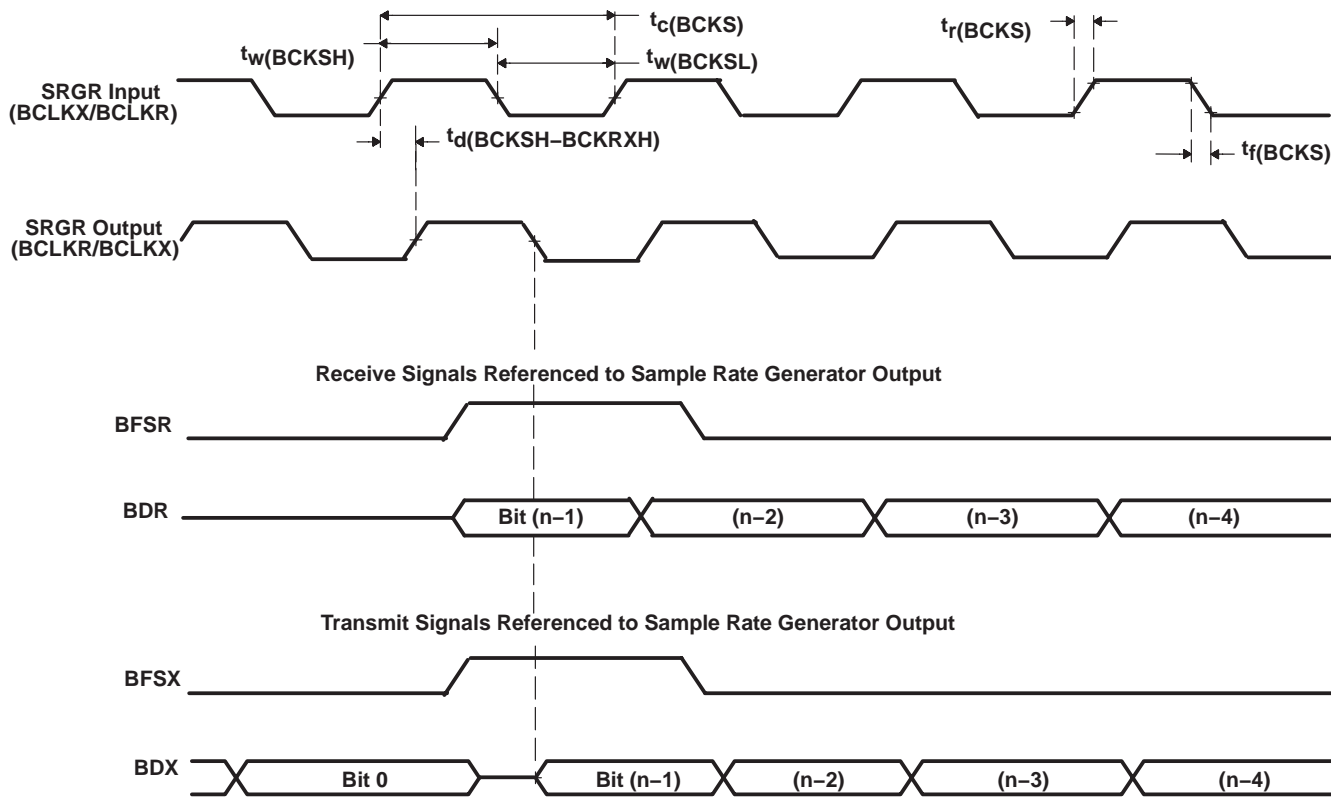


Figure 5-21. McBSP Sample Rate Generator Timings

5.15.3 McBSP General-Purpose I/O Timing

The following timing requirements and switching characteristics tables assume testing over recommended operating conditions (see Figure 5–22).

Table 5–26. McBSP General-Purpose I/O Timing Requirements

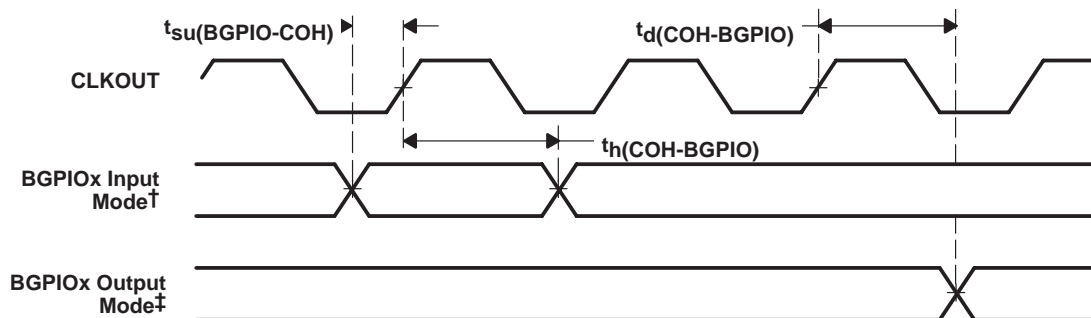
| | MIN | MAX | UNIT |
|---|-----|-----|------|
| $t_{su}(BGPIO-COH)$ Setup time, BGPIOx input mode before CLKOUT high [†] | 9 | | ns |
| $t_h(COH-BGPIO)$ Hold time, BGPIOx input mode after CLKOUT high [†] | 0 | | ns |

[†] BGPIOx refers to BCLKRx, BFSRx, BDRx, BCLKXx, or BFSXx when configured as a general-purpose input.

Table 5–27. McBSP General-Purpose I/O Switching Characteristics

| PARAMETER | MIN | MAX | UNIT |
|---|-----|-----|------|
| $t_d(COH-BGPIO)$ Delay time, CLKOUT high to BGPIOx output mode [‡] | -5 | 5 | ns |

[‡] BGPIOx refers to BCLKRx, BFSRx, BCLKXx, BFSXx, or BDXx when configured as a general-purpose output.



[†] BGPIOx refers to BCLKRx, BFSRx, BDRx, BCLKXx, or BFSXx when configured as a general-purpose input.

[‡] BGPIOx refers to BCLKRx, BFSRx, BCLKXx, BFSXx, or BDXx when configured as a general-purpose output.

Figure 5–22. McBSP General-Purpose I/O Timings

5.15.4 McBSP as SPI Master or Slave Timing

The following timing requirements and switching characteristics tables assume testing over recommended operating conditions and $H = 0.5t_{c(CO)}$ (see Figure 5–23, Figure 5–24, Figure 5–25, and Figure 5–26).

Table 5–28. McBSP as SPI Master or Slave Timing Requirements (CLKSTP = 10b, CLKXP = 0)†

| | | MASTER | | SLAVE | | UNIT |
|----------------------|--|--------|-----|---------|-----|------|
| | | MIN | MAX | MIN | MAX | |
| $t_{su}(BDRV-BCKXL)$ | Setup time, BDR valid before BCLKX low | 12 | | 2 – 12H | | ns |
| $t_h(BCKXL-BDRV)$ | Hold time, BDR valid after BCLKX low | 4 | | 6 + 12H | | ns |
| $t_{su}(BFXL-BCKXH)$ | Setup time, BFSX low before BCLKX high | | | 10 | | ns |
| $t_c(BCKX)$ | Cycle time, BCLKX | 12H | | 32H | | ns |

† For all SPI slave modes, CLKG is programmed as 1/2 of the CPU clock by setting CLKSM = CLKGDV = 1.

Table 5–29. McBSP as SPI Master or Slave Switching Characteristics (CLKSTP = 10b, CLKXP = 0)†

| PARAMETER | MASTER† | | SLAVE | | UNIT |
|------------------------|---------|-----|-------------------|-----|--------------------|
| | MIN | MAX | MIN | MAX | |
| $t_h(BCKXL-BFXL)$ | T – 5 | | T + 6 | | ns |
| $t_d(BFXL-BCKXH)$ | C – 5 | | C + 5 | | ns |
| $t_d(BCKXH-BDXV)$ | –3 | | 12 | | 6H + 4 10H + 19 |
| $t_{dis}(BCKXL-BDXHZ)$ | C – 6 | | C + 10 | | ns |
| $t_{dis}(BFXH-BDXHZ)$ | | | 4H + 4 8H + 17 | | ns |
| $t_d(BFXL-BDXV)$ | | | 4H + 4 8H + 17 | | ns |

† For all SPI slave modes, CLKG is programmed as 1/2 of the CPU clock by setting CLKSM = CLKGDV = 1.

‡ T = BCLKX period = (1 + CLKGDV) * 2H

C = BCLKX low pulse width = T/2 when CLKGDV is odd or zero and = (CLKGDV/2) * 2H when CLKGDV is even

§ FSRP = FSXP = 1. As a SPI master, BFSX is inverted to provide active-low slave-enable output. As a slave, the active-low signal input on BFSX and BFSR is inverted before being used internally.

CLKXM = FSXM = 1, CLKRM = FSRM = 0 for master McBSP

CLKXM = CLKRM = FSXM = FSRM = 0 for slave McBSP

¶ BFSX should be low before the rising edge of clock to enable slave devices and then begin a SPI transfer at the rising edge of the master clock (BCLKX).

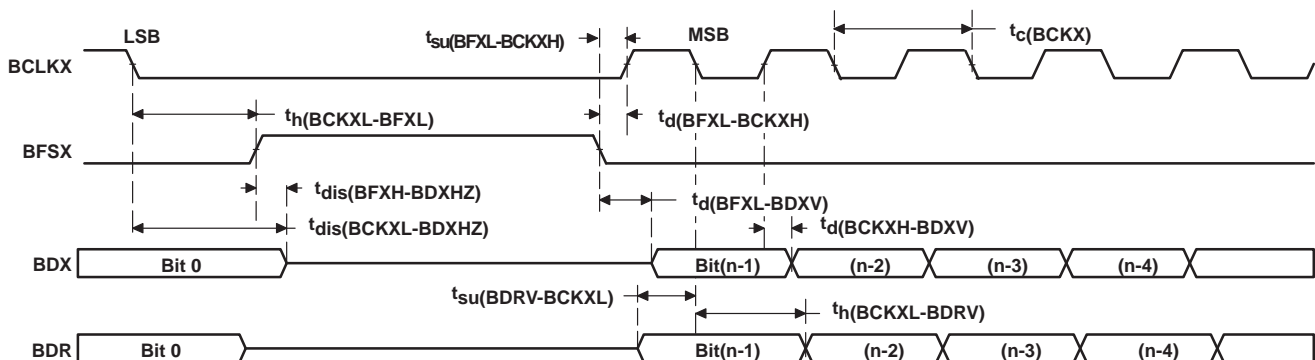


Figure 5–23. McBSP Timing as SPI Master or Slave: CLKSTP = 10b, CLKXP = 0

Table 5–30. McBSP as SPI Master or Slave Timing Requirements (CLKSTP = 11b, CLKXP = 0)†

| | | MASTER | | SLAVE | | UNIT |
|----------------------|---|--------|-----|---------|-----|------|
| | | MIN | MAX | MIN | MAX | |
| $t_{su}(BDRV-BCKXH)$ | Setup time, BDR valid before BCLKX high | 12 | | 2 – 12H | | ns |
| $t_h(BCKXH-BDRV)$ | Hold time, BDR valid after BCLKX high | 4 | | 6 + 12H | | ns |
| $t_{su}(BFXL-BCKXH)$ | Setup time, BFSX low before BCLKX high | | | 10 | | ns |
| $t_c(BCKX)$ | Cycle time, BCLKX | 12H | | 32H | | ns |

† For all SPI slave modes, CLKG is programmed as 1/2 of the CPU clock by setting CLKSM = CLKGDV = 1.

Table 5–31. McBSP as SPI Master or Slave Switching Characteristics (CLKSTP = 11b, CLKXP = 0)†

| PARAMETER | | MASTER† | | SLAVE | | UNIT |
|------------------------|---|---------|--------|--------|----------|------|
| | | MIN | MAX | MIN | MAX | |
| $t_h(BCKXL-BFXL)$ | Hold time, BFSX low after BCLKX low§ | C – 5 | C + 6 | | | ns |
| $t_d(BFXL-BCKXH)$ | Delay time, BFSX low to BCLKX high¶ | T – 5 | T + 5 | | | ns |
| $t_d(BCKXL-BDXV)$ | Delay time, BCLKX low to BDX valid | –3 | 12 | 6H + 4 | 10H + 19 | ns |
| $t_{dis}(BCKXL-BDXHZ)$ | Disable time, BDX high impedance following last data bit from BCLKX low | –6 | 10 | 6H + 4 | 10H + 17 | ns |
| $t_d(BFXL-BDXV)$ | Delay time, BFSX low to BDX valid | D – 2 | D + 10 | 4H + 4 | 8H + 17 | ns |

† For all SPI slave modes, CLKG is programmed as 1/2 of the CPU clock by setting CLKSM = CLKGDV = 1.

‡ T = BCLKX period = (1 + CLKGDV) * 2H

C = BCLKX low pulse width = T/2 when CLKGDV is odd or zero and = (CLKGDV/2) * 2H when CLKGDV is even

D = BCLKX high pulse width = T/2 when CLKGDV is odd or zero and = (CLKGDV/2 + 1) * 2H when CLKGDV is even

§ FSRP = FSXP = 1. As a SPI master, BFSX is inverted to provide active-low slave-enable output. As a slave, the active-low signal input on BFSX and BFSR is inverted before being used internally.

CLKXM = FSXM = 1, CLKRM = FSRM = 0 for master McBSP

CLKXM = CLKRM = FSXM = FSRM = 0 for slave McBSP

¶ BFSX should be low before the rising edge of clock to enable slave devices and then begin a SPI transfer at the rising edge of the master clock (BCLKX).

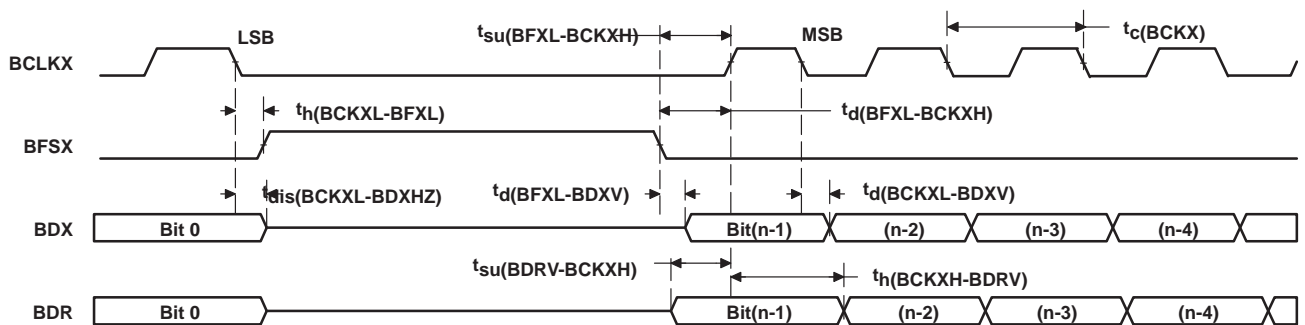


Figure 5–24. McBSP Timing as SPI Master or Slave: CLKSTP = 11b, CLKXP = 0

Table 5–32. McBSP as SPI Master or Slave Timing Requirements (CLKSTP = 10b, CLKXP = 1)†

| | MASTER | | SLAVE | | UNIT |
|--|--------|-----|---------|-----|------|
| | MIN | MAX | MIN | MAX | |
| $t_{su}(BDRV-BCKXH)$ Setup time, BDR valid before BCLKX high | 12 | | 2 – 12H | | ns |
| $t_h(BCKXH-BDRV)$ Hold time, BDR valid after BCLKX high | 4 | | 6 + 12H | | ns |
| $t_{su}(BFXL-BCKXL)$ Setup time, BFSX low before BCLKX low | | | 10 | | ns |
| $t_c(BCKX)$ Cycle time, BCLKX | 12H | | 32H | | ns |

† For all SPI slave modes, CLKG is programmed as 1/2 of the CPU clock by setting CLKSM = CLKGDV = 1.

Table 5–33. McBSP as SPI Master or Slave Switching Characteristics (CLKSTP = 10b, CLKXP = 1)†

| PARAMETER | MASTER† | | SLAVE | | UNIT |
|---|---------|--------|--------|----------|------|
| | MIN | MAX | MIN | MAX | |
| $t_h(BCKXH-BFXL)$ Hold time, BFSX low after BCLKX high§ | T – 5 | T + 6 | | | ns |
| $t_d(BFXL-BCKXL)$ Delay time, BFSX low to BCLKX low¶ | D – 5 | D + 5 | | | ns |
| $t_d(BCKXL-BDXV)$ Delay time, BCLKX low to BDX valid | –3 | 12 | 6H + 4 | 10H + 19 | ns |
| $t_{dis}(BCKXH-BDXHZ)$ Disable time, BDX high impedance following last data bit from BCLKX high | D – 6 | D + 10 | | | ns |
| $t_{dis}(BFXH-BDXHZ)$ Disable time, BDX high impedance following last data bit from BFSX high | | | 4H + 4 | 8H + 17 | ns |
| $t_d(BFXL-BDXV)$ Delay time, BFSX low to BDX valid | | | 4H + 4 | 8H + 17 | ns |

† For all SPI slave modes, CLKG is programmed as 1/2 of the CPU clock by setting CLKSM = CLKGDV = 1.

‡ T = BCLKX period = (1 + CLKGDV) * 2H

D = BCLKX high pulse width = T/2 when CLKGDV is odd or zero and = (CLKGDV/2 + 1) * 2H when CLKGDV is even

§ FSRP = FSXP = 1. As a SPI master, BFSX is inverted to provide active-low slave-enable output. As a slave, the active-low signal input on BFSX and BFSR is inverted before being used internally.

CLKXM = FSXM = 1, CLKRM = FSRM = 0 for master McBSP

CLKXM = CLKRM = FSXM = FSRM = 0 for slave McBSP

¶ BFSX should be low before the rising edge of clock to enable slave devices and then begin a SPI transfer at the rising edge of the master clock (BCLKX).

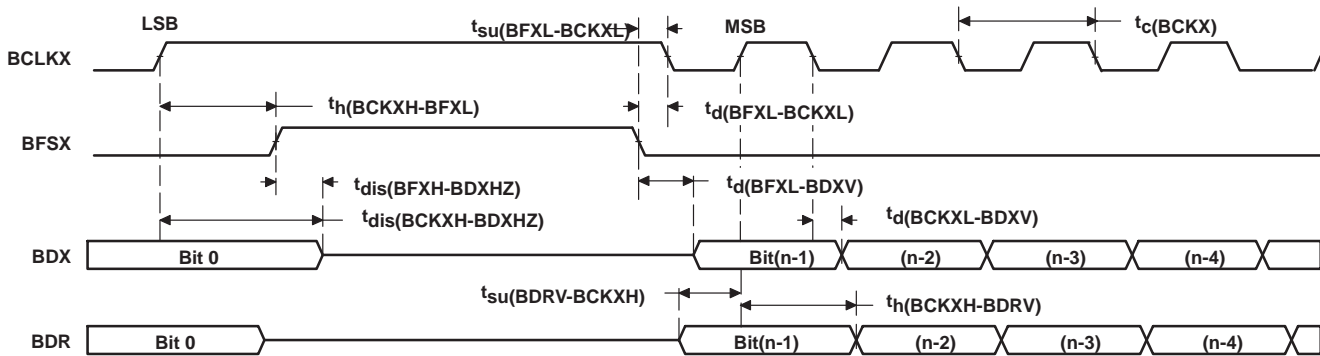


Figure 5–25. McBSP Timing as SPI Master or Slave: CLKSTP = 10b, CLKXP = 1

Table 5–34. McBSP as SPI Master or Slave Timing Requirements (CLKSTP = 11b, CLKXP = 1)†

| | | MASTER | | SLAVE | | UNIT |
|----------------------|--|--------|-----|---------|-----|------|
| | | MIN | MAX | MIN | MAX | |
| $t_{su}(BDRV-BCKXL)$ | Setup time, BDR valid before BCLKX low | 12 | | 2 – 12H | | ns |
| $t_h(BCKXL-BDRV)$ | Hold time, BDR valid after BCLKX low | 4 | | 6 + 12H | | ns |
| $t_{su}(BFXL-BCKXL)$ | Setup time, BFSX low before BCLKX low | | | 10 | | ns |
| $t_c(BCKX)$ | Cycle time, BCLKX | 12H | | 32H | | ns |

† For all SPI slave modes, CLKG is programmed as 1/2 of the CPU clock by setting CLKSM = CLKGDV = 1.

Table 5–35. McBSP as SPI Master or Slave Switching Characteristics (CLKSTP = 11b, CLKXP = 1)†

| PARAMETER | | MASTER‡ | | SLAVE | | UNIT |
|------------------------|--|---------|--------|--------|----------|------|
| | | MIN | MAX | MIN | MAX | |
| $t_h(BCKXH-BFXL)$ | Hold time, BFSX low after BCLKX high§ | D – 5 | D + 6 | | | ns |
| $t_d(BFXL-BCKXL)$ | Delay time, BFSX low to BCLKX low¶ | T – 5 | T + 5 | | | ns |
| $t_d(BCKXH-BDXV)$ | Delay time, BCLKX high to BDX valid | –3 | 12 | 6H + 4 | 10H + 19 | ns |
| $t_{dis}(BCKXH-BDXHZ)$ | Disable time, BDX high impedance following last data bit from BCLKX high | –6 | 10 | 6H + 4 | 10H + 17 | ns |
| $t_d(BFXL-BDXV)$ | Delay time, BFSX low to BDX valid | C – 2 | C + 10 | 4H + 4 | 8H + 17 | ns |

† For all SPI slave modes, CLKG is programmed as 1/2 of the CPU clock by setting CLKSM = CLKGDV = 1.

‡ T = BCLKX period = (1 + CLKGDV) * 2H

C = BCLKX low pulse width = T/2 when CLKGDV is odd or zero and = (CLKGDV/2) * 2H when CLKGDV is even

D = BCLKX high pulse width = T/2 when CLKGDV is odd or zero and = (CLKGDV/2 + 1) * 2H when CLKGDV is even

§ FSRP = FSXP = 1. As a SPI master, BFSX is inverted to provide active-low slave-enable output. As a slave, the active-low signal input on BFSX and BFSR is inverted before being used internally.

CLKXM = FSXM = 1, CLKRM = FSRM = 0 for master McBSP

CLKXM = CLKRM = FSXM = FSRM = 0 for slave McBSP

¶ BFSX should be low before the rising edge of clock to enable slave devices and then begin a SPI transfer at the rising edge of the master clock (BCLKX).

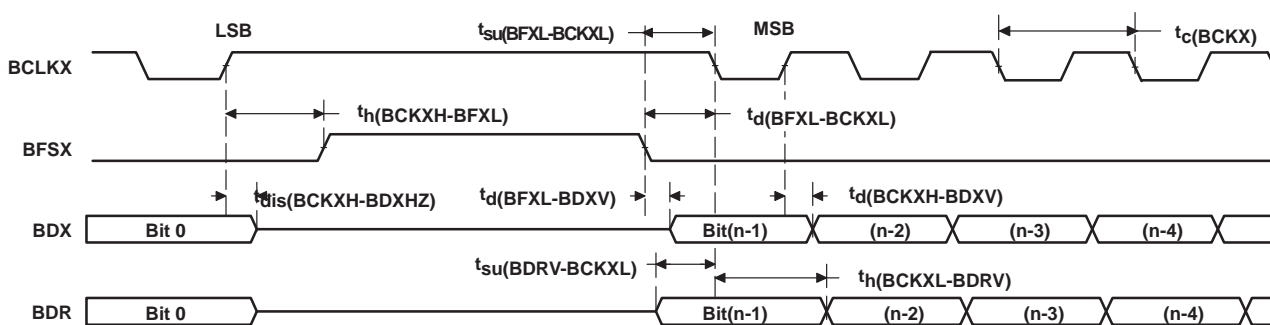


Figure 5–26. McBSP Timing as SPI Master or Slave: CLKSTP = 11b, CLKXP = 1

5.16 Host-Port Interface Timing

The following timing requirements and switching characteristics tables assume testing over recommended operating conditions and $H = 0.5t_{c(CO)}$ (see Figure 5–27 through Figure 5–34). In the following tables, \overline{DS} refers to the logical OR of \overline{HCS} , $\overline{HDS1}$, and $\overline{HDS2}$, and HD refers to any of the HPI data bus pins (HD0, HD1, HD2, etc.).

Table 5–36. HPI16 Mode Timing Requirements

| | | MIN | MAX | UNIT | | |
|-----------------------------|--|---|--|----------|----------|----|
| $t_{su}(HBV-DSL)$ | Setup time, HAD valid before \overline{DS} falling edge ^{†‡} | 5 | | ns | | |
| $t_h(DSL-HBV)$ | Hold time, HAD valid after \overline{DS} falling edge ^{†‡} | 5 | | ns | | |
| $t_{su}(HBV-HSL)$ | Setup time, HAD valid before \overline{HAS} falling edge [†] | 5 | | ns | | |
| $t_h(HSL-HBV)$ | Hold time, HAD valid after \overline{HAS} falling edge [†] | 5 | | ns | | |
| $t_{su}(HAV-DSH)$ | Setup time, address valid before \overline{DS} rising edge (nonmultiplexed write) [‡] | 5 | | ns | | |
| $t_{su}(HAV-DSL)$ | Setup time, address valid before \overline{DS} falling edge (nonmultiplexed read) [‡] | –(4H + 5) | | ns | | |
| $t_h(DSH-HAV)$ | Hold time, address valid after \overline{DS} rising edge (nonmultiplexed mode) [‡] | 1 | | ns | | |
| $t_{su}(HSL-DSL)$ | Setup time, \overline{HAS} low before \overline{DS} falling edge [‡] | 5 | | ns | | |
| $t_h(HSL-DSL)$ | Hold time, \overline{HAS} low after \overline{DS} falling edge [‡] | 2 | | ns | | |
| $t_w(DSL)$ | Pulse duration, \overline{DS} low [‡] | 30 | | ns | | |
| $t_w(DSH)$ | Pulse duration, \overline{DS} high [‡] | 10 | | ns | | |
| $t_c(DSH-DSH)$ [§] | Cycle time, \overline{DS} rising edge to next \overline{DS} rising edge [‡] | Nonmultiplexed or multiplexed mode (no increment) memory accesses (or writes to the FETCH bit) with no DMA activity. | Reads | 10H + 30 | ns | |
| | | | Writes | 10H + 10 | | |
| | | Nonmultiplexed or multiplexed mode (no increment) memory accesses (or writes to the FETCH bit) with 16-bit DMA activity. | Reads | 16H + 30 | ns | |
| | | | Writes | 16H + 10 | | |
| | | Nonmultiplexed or multiplexed mode (no increment) memory accesses (or writes to the FETCH bit) with 32-bit DMA activity. | Reads | 24H + 30 | ns | |
| | | | Writes | 24H + 10 | | |
| | Cycle time, \overline{DS} rising edge to next \overline{DS} rising edge [‡] | (In autoincrement mode, WRITE timings are the same as READ timings.) | Multiplexed (autoincrement) memory accesses (or writes to the FETCH bit) with no DMA activity. | | 10H + 10 | ns |
| | | | Multiplexed (autoincrement) memory accesses (or writes to the FETCH bit) with 16-bit DMA activity. | | 16H + 10 | ns |
| | | | Multiplexed (autoincrement) memory accesses (or writes to the FETCH bit) with 32-bit DMA activity. | | 24H + 10 | ns |
| | | Cycle time, \overline{DS} rising edge to next \overline{DS} rising edge for writes to DSPINT and \overline{HINT} [‡] | | | 8H | ns |
| | Cycle time, \overline{DS} rising edge to next \overline{DS} rising edge for HPIC reads, HPIC XADD bit writes, and address register reads and writes [‡] | | | 40 | ns | |
| $t_{su}(HDV-DSH)W$ | Setup time, HD valid before \overline{DS} rising edge [‡] | 10 | | ns | | |
| $t_h(DSH-HDV)W$ | Hold time, HD valid after \overline{DS} rising edge, write [‡] | 1 | | ns | | |
| $t_{su}(SELV-DSL)$ | Setup time, SELA/B valid before \overline{DS} falling edge [‡] | 5 | | ns | | |
| $t_h(DSH-SELV)$ | Hold time, SELA/B valid after \overline{DS} rising edge [‡] | 0 | | ns | | |

[†] HAD stands for HCNTL0, HCNTL1, and HR/W.

[‡] DS refers to either HCS or HDS, whichever is controlling the transfer. Refer to the *TMS320C54x DSP Reference Set, Volume 5: Enhanced Peripherals* (literature number SPRU302) for information regarding logical operation of the HPI16. These timings are shown assuming that HDS is the signal controlling the transfer.

[§] These timings are for HPI accesses which do not cross from one subsystem to the other. For accesses which do cross from one subsystem to the other, additional cycles are required. A detailed description of these considerations is provided in the application note *Memory Transfers with TMS320VC5420 and TMS320VC5421 DSPs* (literature number SPRA620).

Table 5–37. HPI16 Mode Switching Characteristics

| PARAMETER | | MIN | MAX | UNIT |
|---|--|-----|---------------------|------|
| $t_{d(DSL-HDD)}$ | Delay time, \overline{DS} low to HD driven [†] | 3 | 20 | ns |
| $t_{d(DSL-HDV1)}^{\#}$ | Delay time, \overline{DS} low to HD valid for first word of an HPI read [†] | | | ns |
| | Case 1a: Memory accesses initiated immediately following a write when DMAC is active in 16-bit mode and $t_w(DSH)$ was < 18H | | $32H+20 - t_w(DSH)$ | |
| | Case 1b: Memory accesses initiated by an autoincrement when DMAC is active in 16-bit mode and $t_w(DSH)$ was < 18H | | $16H+20 - t_w(DSH)$ | |
| | Case 1c: Memory accesses not initiated by an autoincrement (or not immediately following a write) when DMAC is active in 16-bit mode | | 16H+20 | |
| | Case 1d: Memory accesses initiated by an autoincrement when DMAC is active in 16-bit mode and $t_w(DSH)$ was $\geq 18H$ | | 20 | |
| | Case 1e: Memory accesses initiated immediately following a write when DMAC is active in 32-bit mode and $t_w(DSH)$ was < 26H | | $48H+20 - t_w(DSH)$ | |
| | Case 1f: Memory access initiated by an autoincrement when DMAC is active in 32-bit mode and $t_w(DSH)$ was < 26H | | $24H+20 - t_w(DSH)$ | |
| | Case 1g: Memory access not initiated by an autoincrement (or not immediately following a write) when DMAC is active in 32-bit mode | | 24H+20 | |
| Case 1h: Memory access initiated by an autoincrement when DMAC is active in 32-bit mode and $t_w(DSH)$ was $\geq 26H$ | | 20 | | |
| $t_{d(HSL-HDV1)}^{\#}$ | Delay time, \overline{HAS} low to HD valid for first word of an HPI read | | | ns |
| | Case 2a: Memory accesses initiated immediately following a write when DMAC is inactive and $t_w(DSH)$ was < 10H | | $20H+20 - t_w(DSH)$ | |
| | Case 2b: Memory accesses initiated by an autoincrement when DMAC is inactive and $t_w(DSH)$ was < 10H | | $10H+20 - t_w(DSH)$ | |
| | Case 2c: Memory accesses not initiated by an autoincrement (or not immediately following a write) when DMAC is inactive | | 10H+20 | |
| | Case 2d: Memory accesses initiated by an autoincrement when DMAC is inactive and $t_w(DSH)$ was $\geq 10H$ | | 20 | |
| Case 3: HPIC/HPIA reads | | 20 | | |
| $t_{d(DSL-HDV2)}$ | Multiplexed reads with autoincrement. Prefetch completed. | 3 | 20 | ns |
| $t_{d(DSH-HYH)}^{\#}$ | Delay time, \overline{DS} high to HRDY high [§] (writes and autoincrement reads) | | | ns |
| | Memory accesses (or writes to the FETCH bit) when no DMA is active | | 10H+5 | |
| | Memory accesses (or writes to the FETCH bit) with one or more 16-bit DMA channels active | | 16H+5 | |
| | Memory accesses (or writes to the FETCH bit) with one or more 32-bit DMA channels active | | 24H+5 | |
| | Writes to DSPINT and HINT [‡] | | 4H + 5 | |
| $t_v(HYH-HDV)$ | Valid time, HD valid after HRDY high | | 7 | ns |
| $t_h(DSH-HDV)_R$ | Hold time, HD valid after \overline{DS} rising edge, read [‡] | 0 | 10 | ns |
| $t_d(COH-HYH)$ | Delay time, CLKOUT rising edge to HRDY high | | 5 | ns |
| $t_d(DSL-HYL)$ | Delay time, \overline{DS} low to HRDY low [¶] | | 12 | ns |
| $t_d(DSH-HYL)$ | Delay time, \overline{DS} high to HRDY low [¶] | | 12 | ns |

[†] HAD stands for HCNTL0, HCNTL1, and HR/W.

[‡] HDS refers to either HDS1 or HDS2.

[§] \overline{DS} refers to either \overline{HCS} or \overline{HDS} , whichever is controlling the transfer. Refer to the *TMS320C54x DSP Reference Set, Volume 5: Enhanced Peripherals* (literature number SPRU302) for information regarding logical operation of the HPI16. These timings are shown assuming that HDS is the signal controlling the transfer.

[¶] HRDY does not go low for other register accesses.

[#] These timings are for HPI accesses which do not cross from one subsystem to the other. For accesses which do cross from one subsystem to the other, additional cycles are required. A detailed description of these considerations is provided in the application note *Memory Transfers with TMS320VC5420 and TMS320VC5421 DSPs* (literature number SPRA620).

Table 5–37. HPI16 Mode Switching Characteristics (Continued)

| PARAMETER | MIN | MAX | UNIT |
|---|-----|-----|------|
| $t_d(\text{HSL-HYL})$ Delay time, $\overline{\text{HAS}}$ low to $\overline{\text{HRDY}}$ low, read | | 12 | ns |
| $t_d(\text{COH-HTX})$ Delay time, CLKOUT rising edge to $\overline{\text{HINT}}$ change | | 5 | ns |

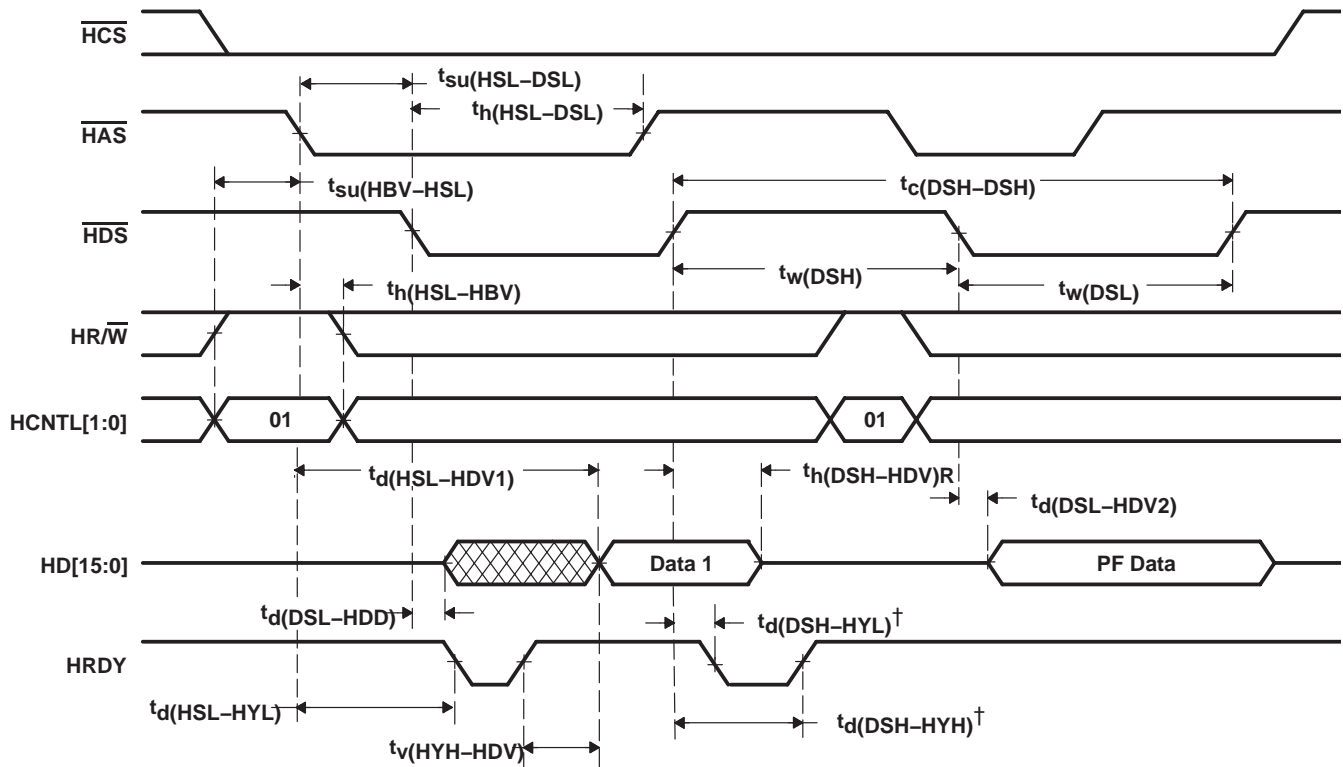
† HAD stands for $\overline{\text{HCNTL0}}$, $\overline{\text{HCNTL1}}$, and $\overline{\text{HR}/\overline{\text{W}}}$.

‡ $\overline{\text{HDS}}$ refers to either $\overline{\text{HDS1}}$ or $\overline{\text{HDS2}}$.

§ $\overline{\text{DS}}$ refers to either $\overline{\text{HCS}}$ or $\overline{\text{HDS}}$, whichever is controlling the transfer. Refer to the *TMS320C54x DSP Reference Set, Volume 5: Enhanced Peripherals* (literature number SPRU302) for information regarding logical operation of the HPI16. These timings are shown assuming that $\overline{\text{HDS}}$ is the signal controlling the transfer.

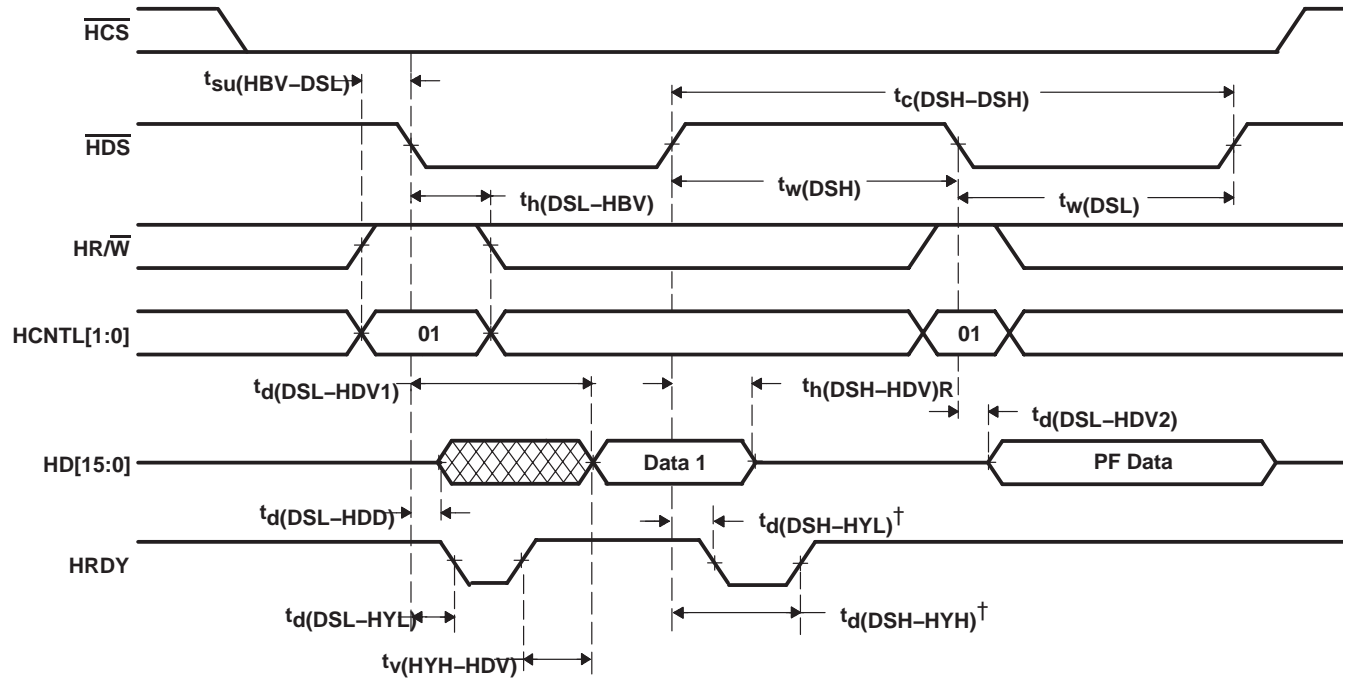
¶ $\overline{\text{HRDY}}$ does not go low for other register accesses.

These timings are for HPI accesses which do not cross from one subsystem to the other. For accesses which do cross from one subsystem to the other, additional cycles are required. A detailed description of these considerations is provided in the application note *Memory Transfers with TMS320VC5420 and TMS320VC5421 DSPs* (literature number SPRA620).



† $\overline{\text{HRDY}}$ goes low at these times only after autoincrement reads.

Figure 5–27. Multiplexed Read Timings Using $\overline{\text{HAS}}$



† $HRDY$ goes low at these times only after autoincrement reads.

Figure 5–28. Multiplexed Read Timings With \overline{HCS} Held High

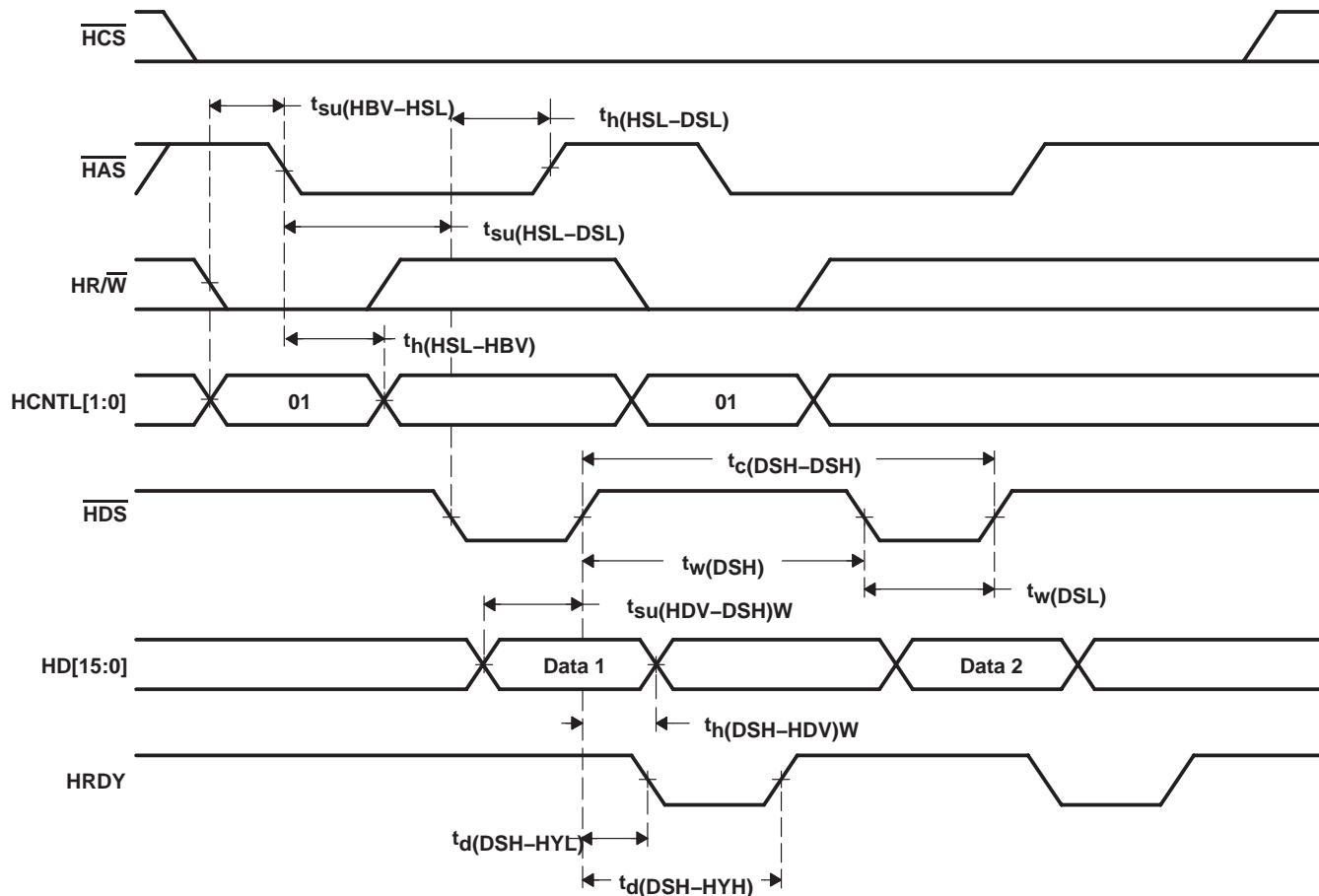


Figure 5–29. Multiplexed Write Timings Using $\overline{\text{HAS}}$

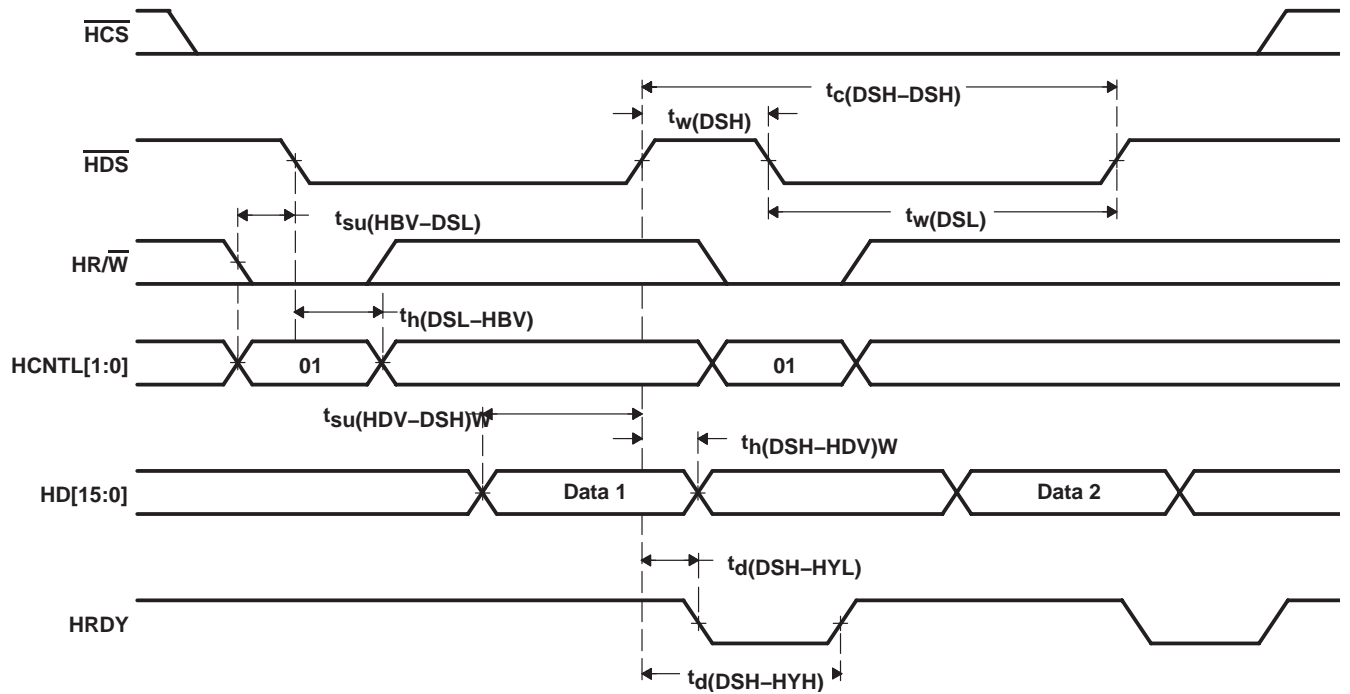


Figure 5–30. Multiplexed Write Timings With $\overline{\text{HAS}}$ Held High

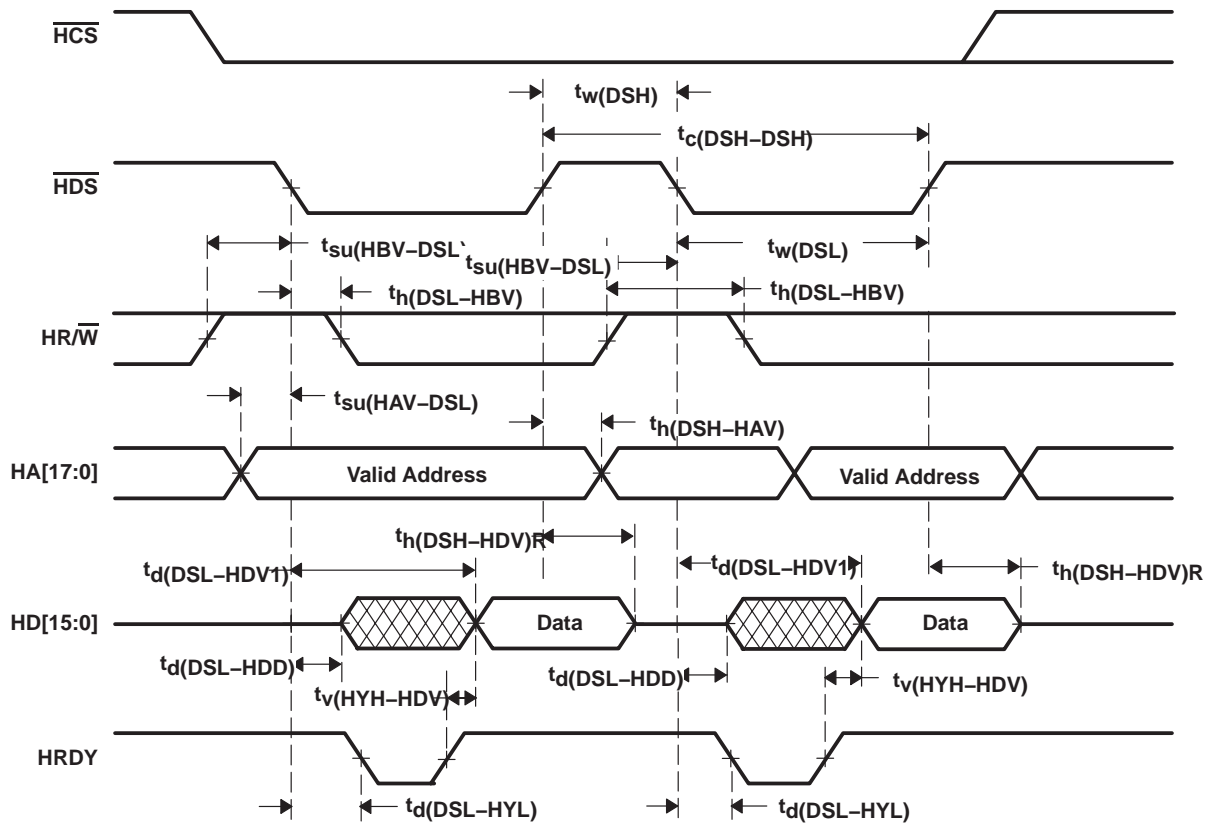


Figure 5–31. Nonmultiplexed Read Timings

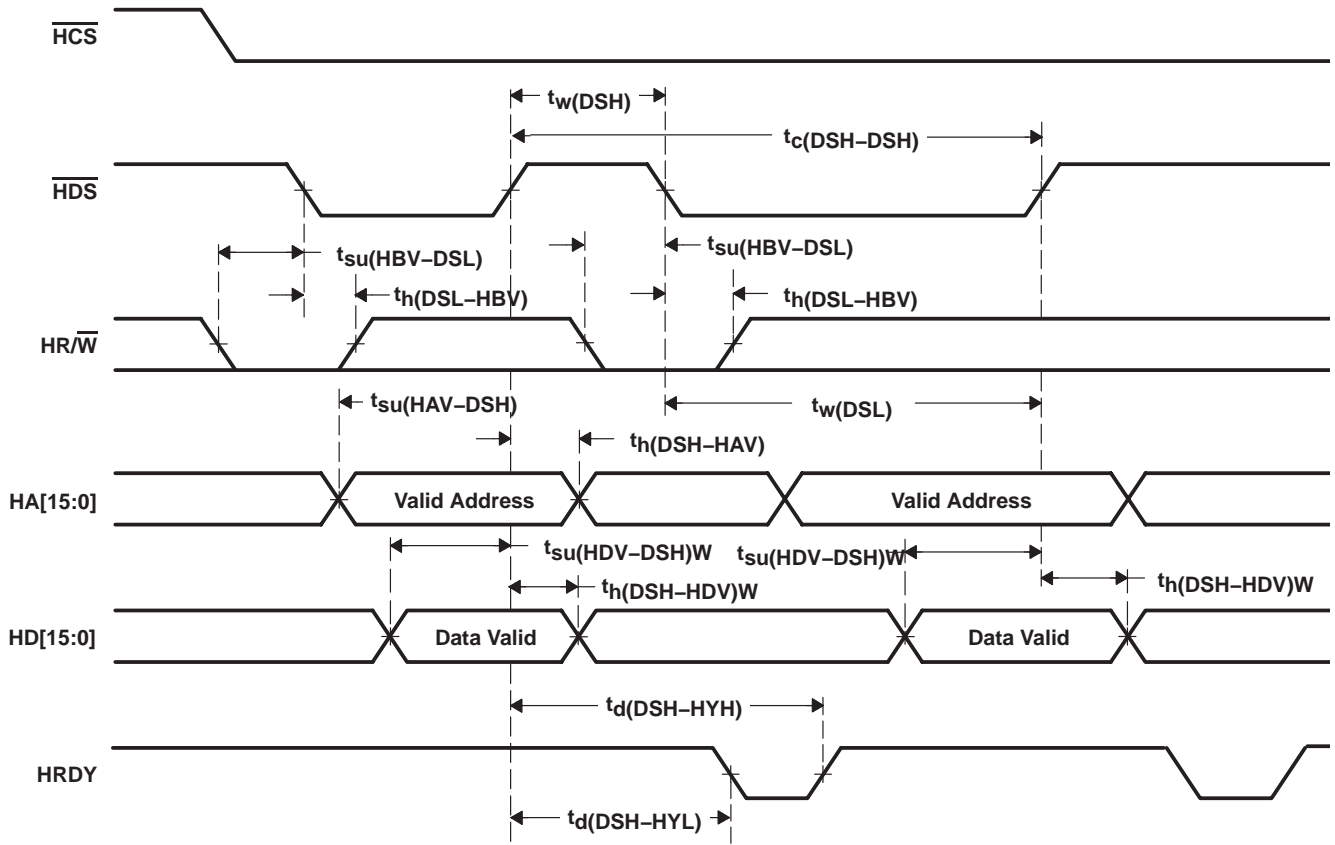


Figure 5-32. Nonmultiplexed Write Timings

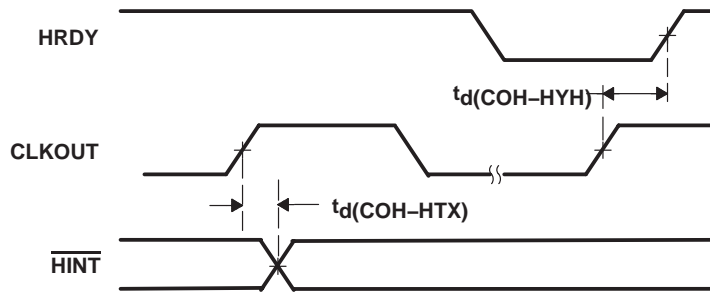


Figure 5-33. HRDY and $\overline{\text{HINT}}$ Relative to CLKOUT

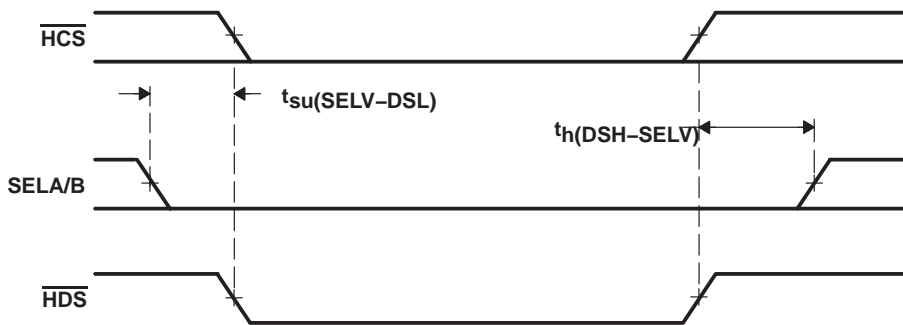


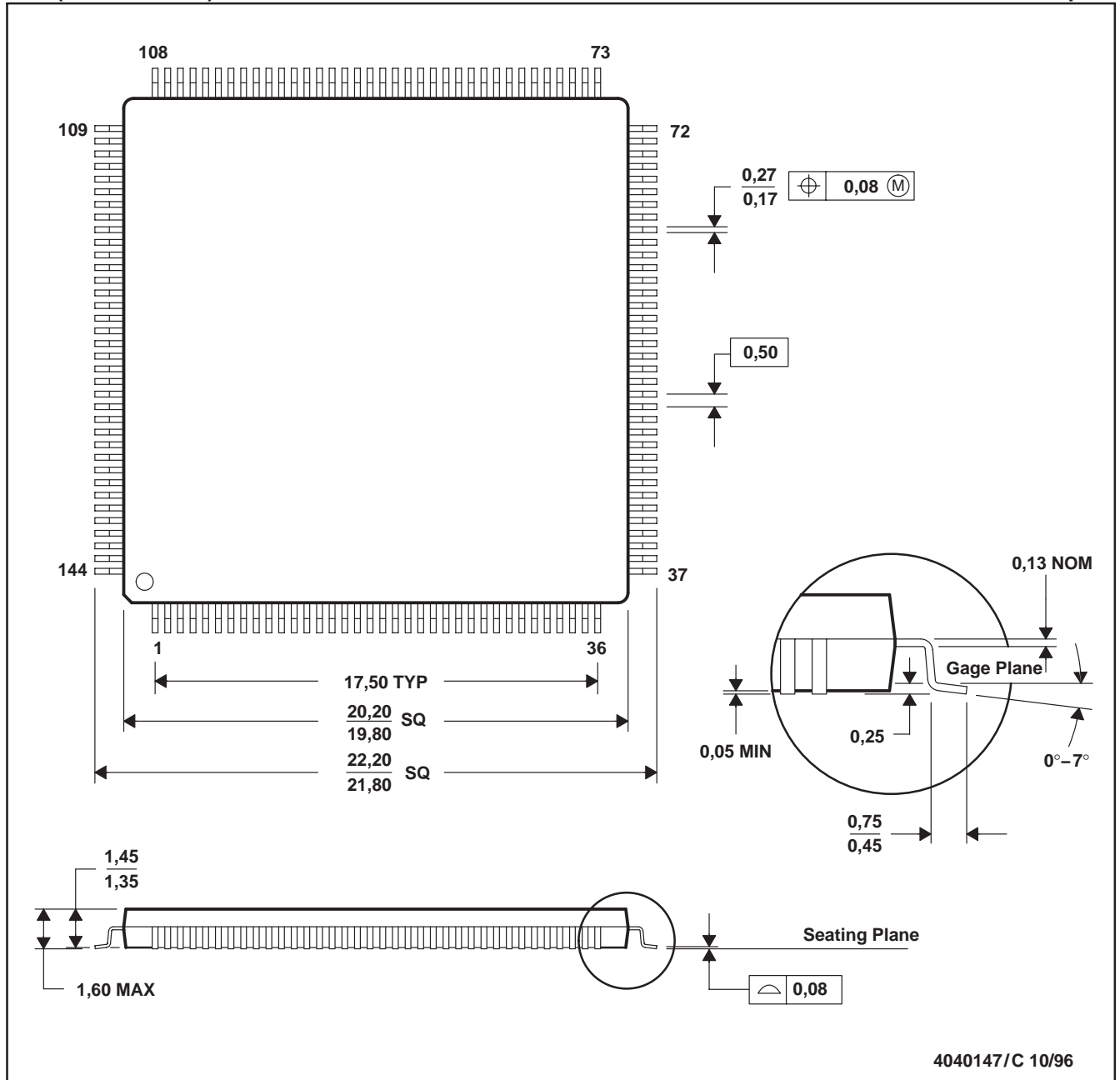
Figure 5-34. SELA/B Timing

6 Mechanical Data

6.1 Low Profile Quad Flatpack Mechanical Data

PGE (S-PQFP-G144)



Low-Profile Quad Flatpack



- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Falls within JEDEC MO-136

Figure 6-1. Low-Profile Quad Flatpack

PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead finish/ Ball material (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|--------------------|---------------|--------------|-----------------|------|-------------|-----------------|--------------------------------------|----------------------|--------------|-------------------------|---|
| SM320VC5421PGE20EP | ACTIVE | LQFP | PGE | 144 | 60 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | SM320VC5421 PGE20EP |  |
| V62/04607-01XE | ACTIVE | LQFP | PGE | 144 | 60 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | SM320VC5421 PGE20EP |  |

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBsolete: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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TRAY

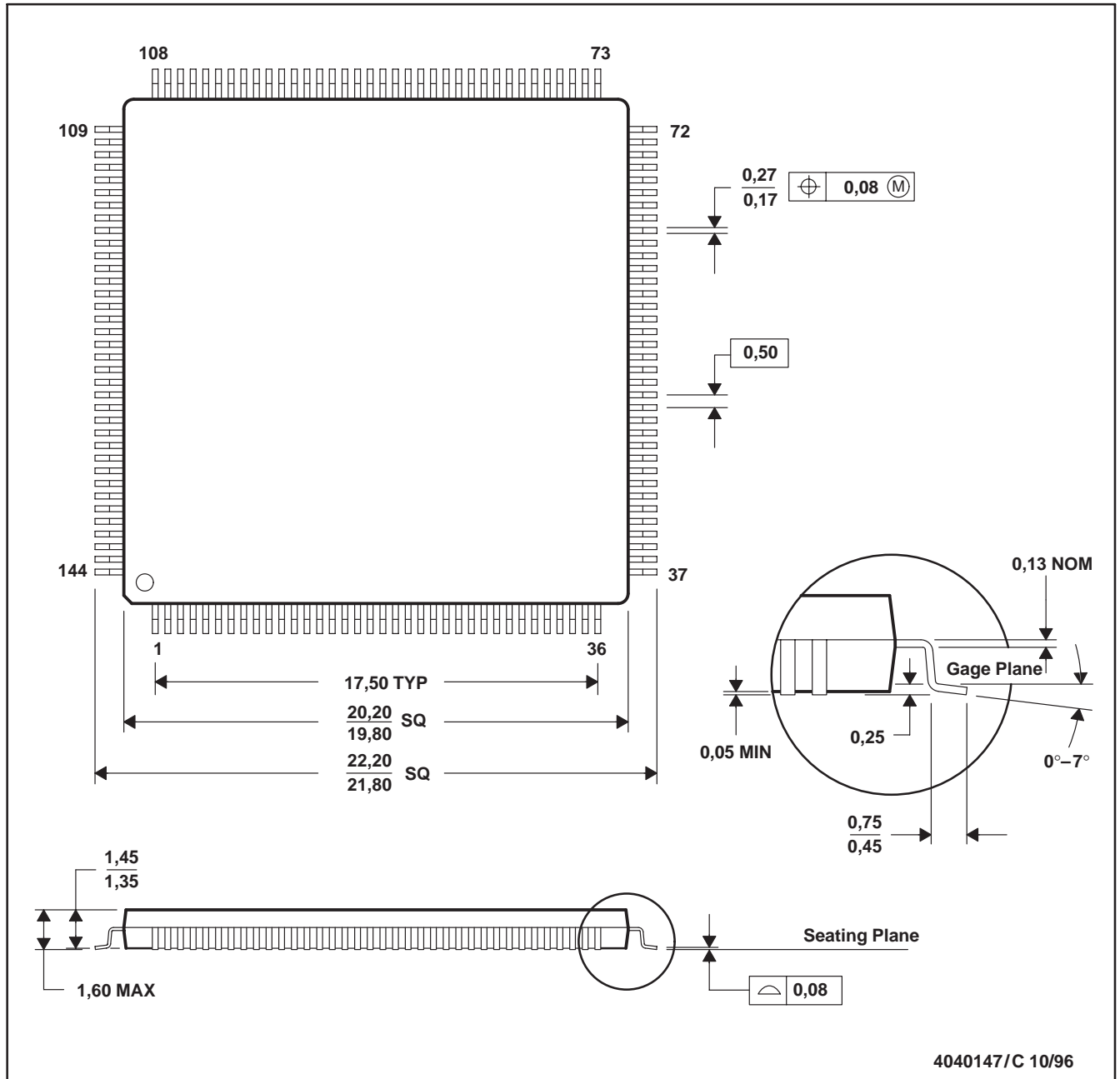

Chamfer on Tray corner indicates Pin 1 orientation of packed units.

*All dimensions are nominal

| Device | Package Name | Package Type | Pins | SPQ | Unit array matrix | Max temperature (°C) | L (mm) | W (mm) | K0 (µm) | P1 (mm) | CL (mm) | CW (mm) |
|--------------------|--------------|--------------|------|-----|-------------------|----------------------|--------|--------|---------|---------|---------|---------|
| SM320VC5421PGE20EP | PGE | LQFP | 144 | 60 | 5X12 | 150 | 315 | 135.9 | 7620 | 25.4 | 17.8 | 17.55 |
| V62/04607-01XE | PGE | LQFP | 144 | 60 | 5X12 | 150 | 315 | 135.9 | 7620 | 25.4 | 17.8 | 17.55 |

PGE (S-PQFP-G144)

PLASTIC QUAD FLATPACK



- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Falls within JEDEC MS-026

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