SNx4AHC573 具有三态输出的八路透明 D 类锁存器

1 特性

- 工作范围为 2V 至 5.5V V_{CC}
- 三态输出可直接驱动总线
- 闩锁性能超过 250mA，符合 JESD 17 规范
- 对于符合 MIL-PRF-38535 标准的产品，所有参数均经过测试，除非另有说明。对于所有其他产品，生产流程不一定包含对所有参数的测试。

2 应用

- 服务器
- PC 和笔记本电脑
- 网络交换机
- 可穿戴保健和健身设备
- 电信基础设施
- 电子销售终端

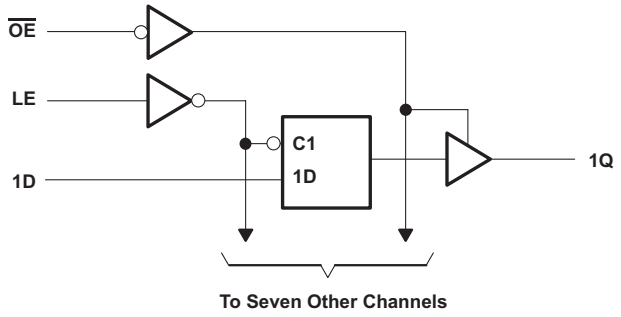
3 说明

SNx4AHC573 器件为八通道透明 D 类锁存器，可在 2V 至 5.5V V_{CC} 下运行。

器件信息

器件型号	封装(1)	封装尺寸(2)	本体尺寸(3)
SNx4AHC573	DB（SSOP，20）	7.50mm × 7.8mm	7.50mm x 5.30mm
	DGV（TVSOP，20）	5.00mm x 6.4mm	5.00mm x 4.40mm
	DW（SOIC，20）	12.80mm × 10.3mm	12.8mm x 7.5mm
	N（PDIP，20）	25.40mm x 9.4mm	25.40mm x 6.35mm
	NS（SOP，20）	12.6mm × 7.8mm	12.6mm × 5.3mm
	PW（TSSOP，20）	6.50mm × 6.4mm	6.50mm × 4.40mm

(1) 有关更多信息，请参阅节 11。
(2) 封装尺寸（长 × 宽）为标称值，并包括引脚（如适用）。
(3) 本体尺寸（长 × 宽）为标称值，不包括引脚。



简化原理图

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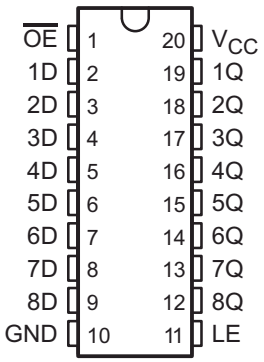
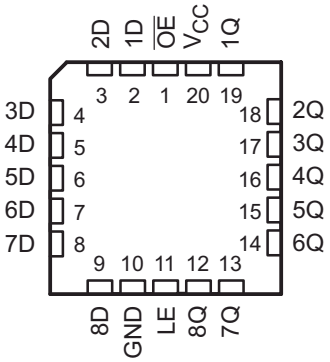
4 Pin Configuration and Functions

SN54AHC573 . . . J OR W PACKAGE
SN74AHC573 . . . DB, DGV, DW, N, NS, OR PW PACKAGE
(TOP VIEW)



SN54AHC573 . . . FK PACKAGE
(TOP VIEW)



PIN		I/O	DESCRIPTION
NO.	NAME		
1	$\overline{OE}$	I	Output Enable
2	1D	I	1D Input
3	2D	I	2D Input
4	3D	I	3D Input
5	4D	I	4D Input
6	5D	I	5D Input
7	6D	I	6D Input
8	7D	I	7D Input
9	8D	I	8D Input
10	GND	—	Ground
11	LE	I	Latch Enable
12	8Q	O	8Q Output
13	7Q	O	7Q Output
14	6Q	O	6Q Output
15	5Q	O	5Q Output
16	4Q	O	4Q Output
17	3Q	O	3Q Output
18	2Q	O	2Q Output
19	1Q	O	1Q Output
20	V_{CC}	—	Power Pin

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1)

			MIN	MAX	UNIT
V_{CC}	Supply voltage range		– 0.5	7	V
V_I	Input voltage range(2)		– 0.5	7	V
V_O	Output voltage range(2)		– 0.5	V_{CC} + 0.5	V
I_{IK}	Input clamp current	V_I < 0		– 20	mA
I_{OK}	Output clamp current	V_O < 0 or V_O > V_{CC}		±20	mA
I_O	Continuous output current	V_O = 0 to V_{CC}		±25	mA
	Continuous current through V_{CC} or GND			±75	mA
T_{stg}	Storage temperature range		– 65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

5.2 ESD Ratings

			Value	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	±2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2)	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)(1)

			SN54AHC573		SN74AHC573		UNIT
			MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage		2	5.5	2	5.5	V
V_{IH}	High-level input voltage	V_{CC} = 2 V	1.5		1.5		V
		V_{CC} = 3 V	2.1		2.1		
		V_{CC} = 5.5 V	3.85		3.85		
V_{IL}	Low-level input voltage	V_{CC} = 2 V		0.5		0.5	V
		V_{CC} = 3 V		0.9		0.9	
		V_{CC} = 5.5 V		1.65		1.65	
V_I	Input voltage		0	5.5	0	5.5	V
V_O	Output voltage		0	V_{CC}	0	V_{CC}	V
I_{OH}	High-level output current	V_{CC} = 2 V		– 50		– 50	μA
		V_{CC} = 3.3 V ± 0.3 V		– 4		– 4	mA
		V_{CC} = 5 V ± 0.5 V		– 8		– 8	
I_{OL}	Low-level output current	V_{CC} = 2 V		50		50	μA
		V_{CC} = 3.3 V ± 0.3 V		4		4	mA
		V_{CC} = 5 V ± 0.5 V		8		8	
$\Delta t/\Delta v$	Input transition rise or fall rate	V_{CC} = 3.3 V ± 0.3 V		100		100	ns/V
		V_{CC} = 5 V ± 0.5 V		20		20	
T_A	Operating free-air temperature		– 55	125	– 40	125	°C

(1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs* (SCBA004).

5.4 Thermal Information

THERMAL METRIC(1)		SN74AHC573						UNIT
		DW	DB	DGV	N	NS	PW	
		20 PINS						
$R_{\theta JA}$	Junction-to-ambient thermal resistance	81.1	97.9	117.2	53.3	77.6	116.8	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	48.9	59.6	32.7	40.0	42.7	58.5	
$R_{\theta JB}$	Junction-to-board thermal resistance	53.8	53.1	58.7	34.2	45.7	78.7	
ψ_{JT}	Junction-to-top characterization parameter	19.5	21.3	1.15	26.4	10.2	12.6	
ψ_{JB}	Junction-to-board characterization parameter	53.1	52.7	58.0	34.1	45.2	77.9	
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	N/A	N/A	N/A	N/A	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report (SPRA953).

5.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	T_A = 25°C			SN54AHC573		SN74AHC573		−40°C to 125°C SN74AHC573		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
V_{OH}	I_{OH} = −50 µA	2 V	1.9	2		1.9		1.9		1.9		V
		3 V	2.9	3		2.9		2.9		2.9		
		4.5 V	4.4	4.5		4.4		4.4		4.4		
	I_{OH} = −4 mA	3 V	2.58			2.48		2.48		2.48		
	I_{OH} = −8 mA	4.5 V	3.94			3.8		3.8		3.8		V
V_{OL}	I_{OL} = 50 µA	2 V			0.1		0.1		0.1		0.1	
		3 V			0.1		0.1		0.1		0.1	
		4.5 V			0.1		0.1		0.1		0.1	
	I_{OL} = 4 mA	3 V			0.36		0.5		0.44		0.44	
	I_{OL} = 8 mA	4.5 V			0.36		0.5		0.44		0.44	
I_I	V_I = 5.5 V or GND	0 V to 5.5 V			±0.1		±1[(1)]		±1		±1	µA
I_{OZ}	V_I = V_{IL} or V_{IH}, V_O = V_{CC} or GND	5.5 V			±0.25		±2.5		±2.5		±2.5	µA
I_{CC}	V_I = V_{CC} or GND, I_O = 0	5.5 V			4		40		40		40	µA
C_i	V_I = V_{CC} or GND	5 V		2.5	10				10		10	pF
C_o	V_O = V_{CC} or GND	5 V		3.5								pF

(1) On products compliant to MIL-PRF-38535, this parameter is not production tested at V_{CC} = 0 V.

5.6 Timing Requirements, V_{CC} = 3.3 V ± 0.3 V

over recommended operating free-air temperature range (unless otherwise noted) (see Load Circuit and Voltage Waveforms)

PARAMETER		T_A = 25°C		SN54AHC573		SN74AHC573		T_A = −40°C to 125°C SN74AHC573		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_w	Pulse duration, LE high	5		5		5		5		ns
t_{su}	Setup time, data before LE ↓	3.5		3.5		3.5		3.5		ns
t_h	Hold time, data after LE ↓	1.5		1.5		1.5		1.5		ns

5.7 Timing Requirements, V_{CC} = 5 V ± 0.5 V

over recommended operating free-air temperature range (unless otherwise noted) (see Load Circuit and Voltage Waveforms)

PARAMETER		T_A = 25°C		SN54AHC573		SN74AHC573		T_A = −40°C to 125°C SN74AHC573		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_w	Pulse duration, LE high	5		5		5		5		ns
t_{su}	Setup time, data before LE ↓	3.5		3.5		3.5		3.5		ns
t_h	Hold time, data after LE ↓	1.5		1.5		1.5		1.5		ns

5.8 Switching Characteristics, V_{CC} = 3.3 V ± 0.3 V

over recommended operating free-air temperature range (unless otherwise noted) (see Load Circuit and Voltage Waveforms)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T_A = 25°C			SN54AHC573		SN74AHC573		T_A = –40°C to 125°C SN74AHC573		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	D	Q	C_L = 15 pF		7[1]	11[1]	1[1]	13[1]	1	13	1	14	ns
t_{PHL}					7[1]	11[1]	1[1]	13[1]	1	13	1	14	
t_{PLH}	LE	Q	C_L = 15 pF		7.6[1]	11.9[1]	1[1]	14[1]	1	14	1	15	ns
t_{PHL}					7.6[1]	11.9[1]	1[1]	14[1]	1	14	1	15	
t_{PZH}	$\overline{OE}$	Q	C_L = 15 pF		7.3[1]	11.5[1]	1[1]	13.5[1]	1	13.5	1	14.5	ns
t_{PZL}					7.3[1]	11.5[1]	1[1]	13.5[1]	1	13.5	1	14.5	
t_{PHZ}	$\overline{OE}$	Q	C_L = 15 pF		8.3[1]	11[1]	1[1]	13[1]	1	13	1	14	ns
t_{PLZ}					8.3[1]	11[1]	1[1]	13[1]	1	13	1	14	
t_{PLH}	D	Q	C_L = 50 pF		9.5	14.5	1	16.5	1	16.5	1	18	ns
t_{PHL}					9.5	14.5	1	16.5	1	16.5	1	18	
t_{PLH}	LE	Q	C_L = 50 pF		10.1	15.4	1	17.5	1	17.5	1	19	ns
t_{PHL}					10.1	15.4	1	17.5	1	17.5	1	19	
t_{PZH}	$\overline{OE}$	Q	C_L = 50 pF		9.8	15	1	17	1	17	1	18	ns
t_{PZL}					9.8	15	1	17	1	17	1	18	
t_{PHZ}	$\overline{OE}$	Q	C_L = 50 pF		10.7	14.5	1	16.5	1	16.5	1	17.5	ns
t_{PLZ}					10.7	14.5	1	16.5	1	16.5	1	17.5	
$t_{sk(o)}$			C_L = 50 pF			1.5[2]				1.5			ns

(1) On products compliant to MIL-PRF-38535, this parameter is not production tested.
(2) On products compliant to MIL-PRF-38535, this parameter does not apply.

5.9 Switching Characteristics, V_{CC} = 5 V ± 0.5 V

over recommended operating free-air temperature range (unless otherwise noted) (see Load Circuit and Voltage Waveforms)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T_A = 25°C			SN54AHC573		SN74AHC573		T_A = –40°C to 125°C SN74AHC573		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	D	Q	C_L = 15 pF		4.5[1]	6.8[1]	1[1]	8[1]	1	8	1	8.5	ns
t_{PHL}					4.5[1]	6.8[1]	1[1]	8[1]	1	8	1	8.5	
t_{PLH}	LE	Q	C_L = 15 pF		5[1]	7.7[1]	1[1]	9[1]	1	9	1	10	ns
t_{PHL}					5[1]	7.7[1]	1[1]	9[1]	1	9	1	10	
t_{PZH}	$\overline{OE}$	Q	C_L = 15 pF		5.2[1]	7.7[1]	1[1]	9[1]	1	9	1	10	ns
t_{PZL}					5.2[1]	7.7[1]	1[1]	9[1]	1	9	1	10	
t_{PHZ}	$\overline{OE}$	Q	C_L = 15 pF		5.2[1]	7.7[1]	1[1]	9[1]	1	9	1	10	ns
t_{PLZ}					5.2[1]	7.7[1]	1[1]	9[1]	1	9	1	10	
t_{PLH}	D	Q	C_L = 50 pF		6	8.8	1	10	1	10	1	11	ns
t_{PHL}					6	8.8	1	10	1	10	1	11	
t_{PLH}	LE	Q	C_L = 50 pF		6.5	9.7	1	11	1	11	1	12	ns
t_{PHL}					6.5	9.7	1	11	1	11	1	12	
t_{PZH}	$\overline{OE}$	Q	C_L = 50 pF		6.7	9.7	1	11	1	11	1	12	ns
t_{PZL}					6.7	9.7	1	11	1	11	1	12	
t_{PHZ}	$\overline{OE}$	Q	C_L = 50 pF		6.7	9.7	1	11	1	11	1	12	ns
t_{PLZ}					6.7	9.7	1	11	1	11	1	12	
$t_{sk(o)}$			C_L = 50 pF			1[2]				1			ns

(1) On products compliant to MIL-PRF-38535, this parameter is not production tested.
(2) On products compliant to MIL-PRF-38535, this parameter does not apply.

5.10 Noise Characteristics

V_{CC} = 5 V, C_L = 50 pF, T_A = 25°C (1)

PARAMETER		SN74AHC573		UNIT
		MIN	MAX	
$V_{OL(P)}$	Quiet output, maximum dynamic V_{OL}		1	V
$V_{OL(V)}$	Quiet output, minimum dynamic V_{OL}		–0.8	V
$V_{OH(V)}$	Quiet output, minimum dynamic V_{OH}	4		V
$V_{IH(D)}$	High-level dynamic input voltage	3.5		V
$V_{IL(D)}$	Low-level dynamic input voltage		1.5	V

(1) Characteristics are for surface-mount packages only.

5.11 Operating Characteristics

V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS		TYP	UNIT
C_{pd}	Power dissipation capacitance	No load,	f = 1 MHz	16	pF

5.12 Typical Characteristics

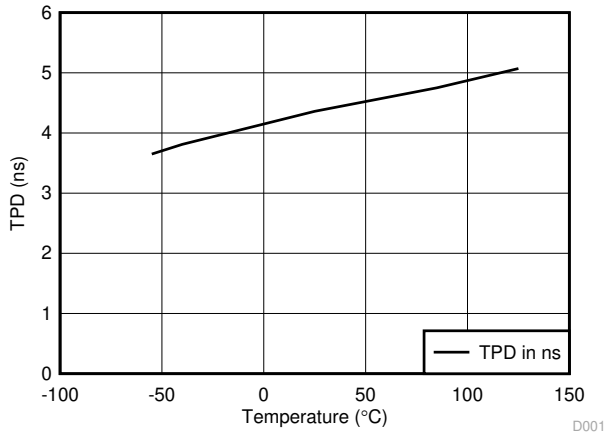


图 5-1. TPD vs Temperature at 5 V

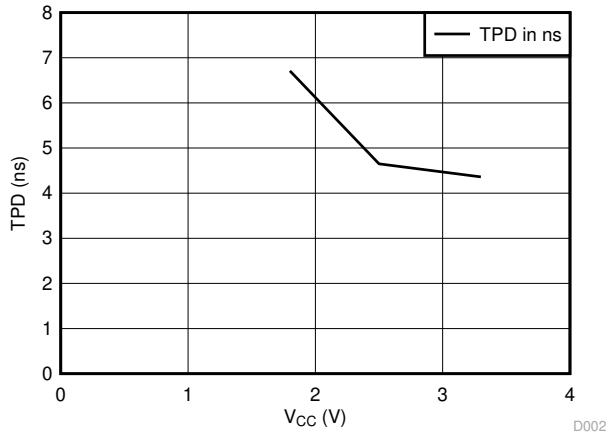
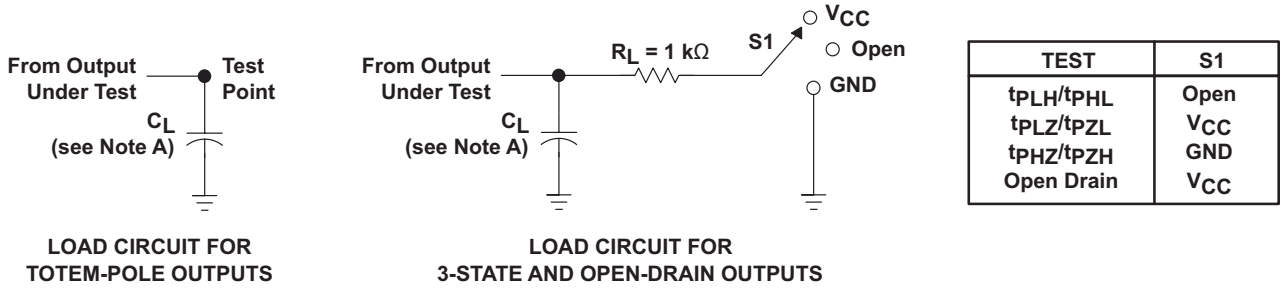


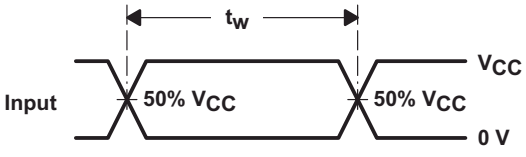
图 5-2. TPD vs V_{CC}

6 Parameter Measurement Information

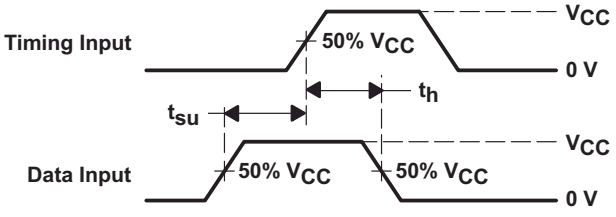


LOAD CIRCUIT FOR TOTEM-POLE OUTPUTS

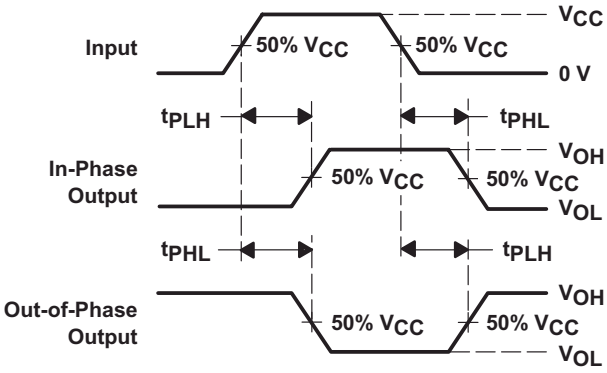
LOAD CIRCUIT FOR 3-STATE AND OPEN-DRAIN OUTPUTS



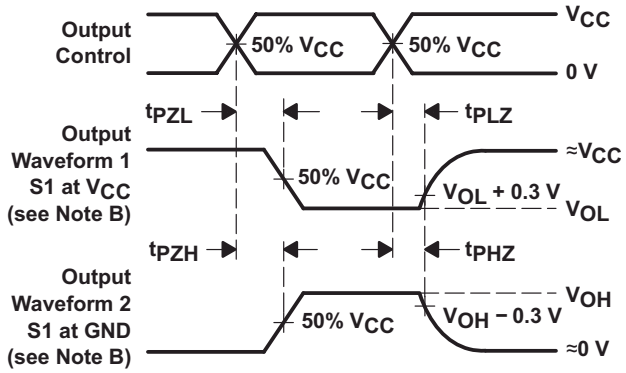
VOLTAGE WAVEFORMS PULSE DURATION



VOLTAGE WAVEFORMS SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS PROPAGATION DELAY TIMES INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS ENABLE AND DISABLE TIMES LOW- AND HIGH-LEVEL ENABLING

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r ≤ 3 ns, t_f ≤ 3 ns.
D. The outputs are measured one at a time with one input transition per measurement.
E. All parameters and waveforms are not applicable to all devices.

图 6-1. Load Circuit and Voltage Waveforms

7 Detailed Description

7.1 Overview

The SNx4AHC573 devices are octal transparent D-type latches designed for 2-V to 5.5-V V_{CC} operation.

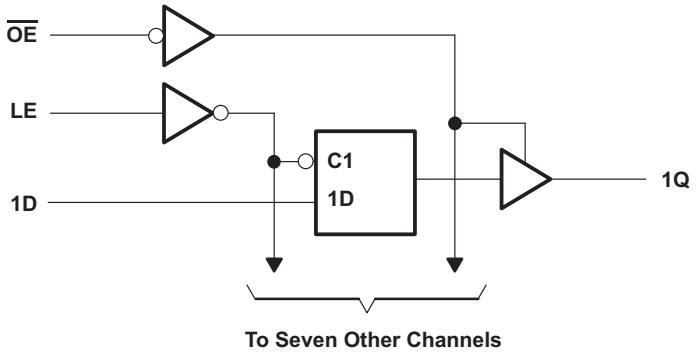
When the latch-enable (LE) input is high, the Q outputs follow the data (D) inputs. When LE is low, the Q outputs are latched at the logic levels of the D inputs.

A buffered output-enable ($\overline{OE}$) input can be used to place the eight outputs in either a normal logic state (high or low) or the high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive bus lines without interface or pull-up components.

$\overline{OE}$ does not affect the internal operations of the latches. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pull-up resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

7.2 Functional Block Diagram



7.3 Feature Description

- Wide operating voltage range
  - Operates from 2 V to 5.5 V
- Allows down voltage translation
  - Inputs accept voltages to 5.5 V
- Slow edges reduce output ringing

7.4 Device Functional Modes

表 7-1. Function Table (Each Latch)

INPUTS			OUTPUT Q
$\overline{OE}$	LE	D	
L	H	H	H
L	H	L	L
L	L	X	Q_0
H	X	X	Z

8 Application and Implementation

备注

以下应用部分中的信息不属于 TI 器件规格的范围，TI 不担保其准确性和完整性。TI 的客 户应负责确定器件是否适用于其应用。客户应验证并测试其设计，以确保系统功能。

8.1 Application Information

The SN74AHC573 is a low-drive CMOS device that can be used for a multitude of bus-interface type applications where output ringing is a concern. The low drive and slow edge rates will minimize overshoot and undershoot on the outputs. The inputs accept voltages up to 5.5 V allowing down translation to the V_{CC} level. 图 8-2 shows how the slower edges can reduce ringing on the output compared to higher drive parts like AC.

8.2 Typical Application

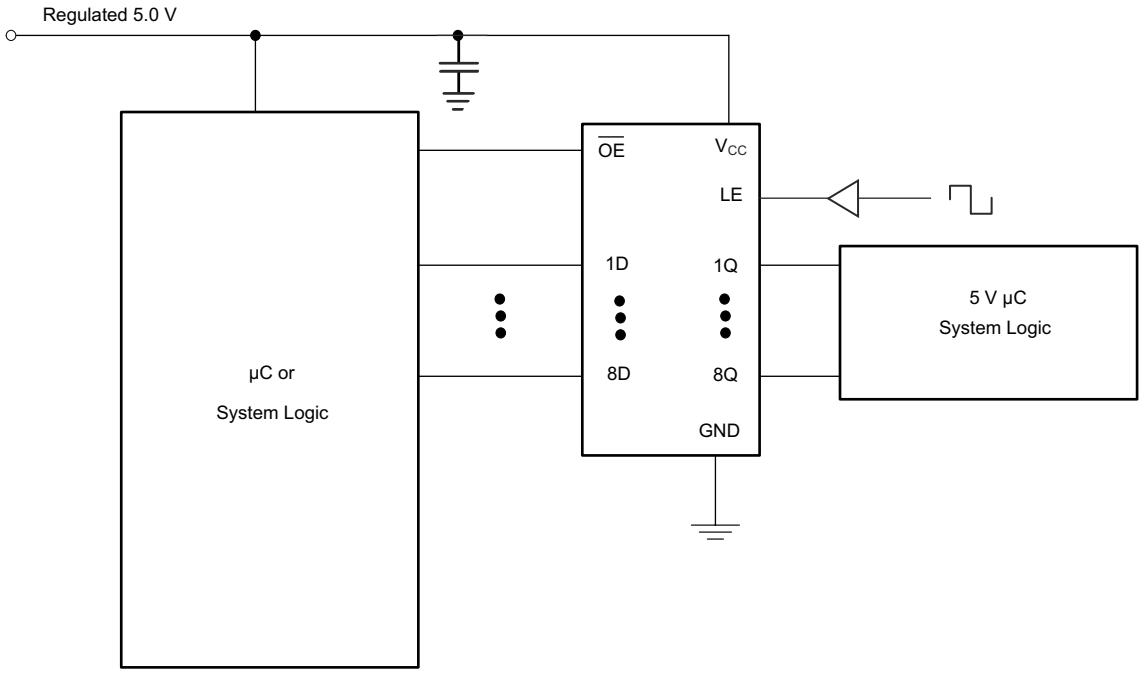


图 8-1. Typical Application Schematic

8.2.1 Design Requirements

This device uses CMOS technology and has balanced output drive. Care should be taken to avoid bus contention because it can drive currents that would exceed maximum limits. The high drive will also create fast edges into light loads; therefore, routing and load conditions should be considered to prevent ringing.

8.2.2 Detailed Design Procedure

1. Recommended input conditions
   - Rise time and fall time specs: See (Δt/ ΔV) in the *节 5.3* table.
   - Specified High and low levels: See (V_{IH} and V_{IL}) in the *节 5.3* table.
   - Inputs are overvoltage tolerant allowing them to go as high as 5.5 V at any valid V_{CC}.
2. Recommend output conditions
   - Load currents should not exceed 25 mA per output and 75 mA total for the part.
   - Outputs should not be pulled above V_{CC}.

8.2.3 Application Curves

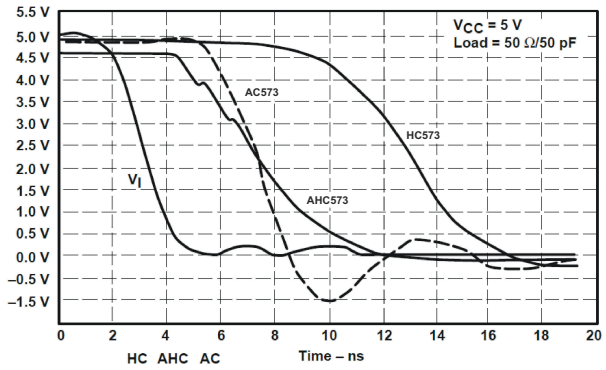


图 8-2. Switching Characteristics Comparison

8.3 Power Supply Recommendations

The power supply can be any voltage between the MIN and MAX supply voltage rating located in the 节 5.3 table.

Each V_{CC} pin should have a good bypass capacitor to prevent power disturbance. For devices with a single supply, 0.1 μF bypass capacitor is recommended. If there are multiple V_{CC} pins, 0.01 μF or 0.022 μF is recommended for each power pin. It is acceptable to parallel multiple bypass capacitors to reject different frequencies of noise. A 0.1 μF and 1 μF are commonly used in parallel. The bypass capacitor should be installed as close to the power pin as possible for best results.

8.4 Layout

8.4.1 Layout Guidelines

When using multiple bit logic devices inputs should not ever float.

In many cases, functions or parts of functions of digital logic devices are unused, for example, when only two inputs of a triple-input AND gate are used or only 3 of the 4 buffer gates are used. Such input pins should not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. Specified in 图 8-3 are the rules that must be observed under all circumstances. All unused inputs of digital logic devices must be connected to a high or low bias to prevent them from floating. The logic level that should be applied to any particular unused input depends on the function of the device. Generally they will be tied to GND or V_{CC}; whichever makes more sense or is more convenient. It is generally acceptable to float outputs unless the part is a transceiver. If the transceiver has an output enable pin, it will disable the outputs section of the part when asserted. This will not disable the input section of the IO’s so they cannot float when disabled.

8.4.2 Layout Example

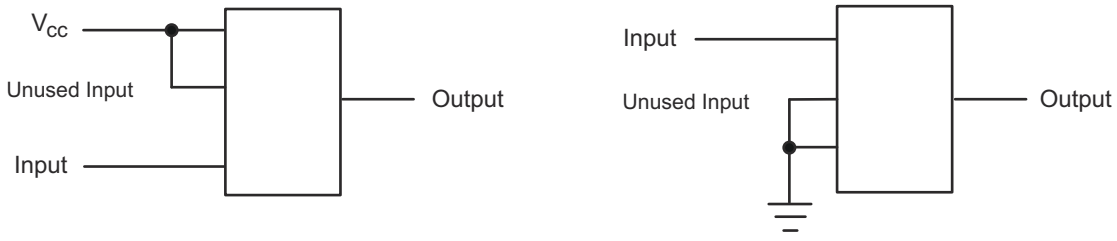


图 8-3. Layout Diagram

9 Device and Documentation Support

9.1 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

表 9-1. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
SN54AHC573	Click here	Click here	Click here	Click here	Click here
SN74AHC573	Click here	Click here	Click here	Click here	Click here

9.2 Trademarks

所有商标均为其各自所有者的财产。

9.3 静电放电警告

静电放电 (ESD) 会损坏这个集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

9.4 术语表

TI 术语表　　本术语表列出并解释了术语、首字母缩略词和定义。

10 Revision History

Changes from Revision L (September 2014) to Revision M (August 2024)	Page
• 向*器件信息*表中添加了封装尺寸	1
• Updated *Handling Ratings* to *ESD Ratings* table	4
• Updated R θ JA values: PW = 103.3 to 116.8, DW = 79.4 to 81.1, NS = 79.2 to 77.6; Updated PW, DW, and NS packages for R θ JC(top), R θ JB, Ψ JT, Ψ JB, and R θ JC(bot), all values in °C/W	5

Changes from Revision K (January 2004) to Revision L (September 2014)	Page
• 将文档更新为新的 TI 数据表格式	1
• 删除了“订购信息”表	1
• 向“特性”列表中添加了“军用免责声明”	1
• 添加了“应用”	1
• Added Handling Ratings table	4
• Changed MAX operating temperature to 125°C in Recommended Operating Conditions table.	5
• Added Thermal Information table	5
• Added –40°C to 125°C temperature range for SN74AHC573 in Electrical Characteristics table	6
• Added T_A = –40°C to 125°C temperature range for SN74AHC573 in Timing Requirements table.	6
• Added T_A = –40°C to 125°C temperature range for SN74AHC573 in Timing Requirements table.	6
• Added T_A = –40°C to 125°C temperature range for SN74AHC573 in Switching Characteristics table.	7
• Added T_A = –40°C to 125°C temperature range for SN74AHC573 in Switching Characteristics table.	7
• Added Typical Characteristics	8
• Added Application and Implementation section	11
• Added Power Supply Recommendations and Layout sections	12

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
5962-9685601Q2A	Active	Production	LCCC (FK) | 20	55 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9685601Q2A SNJ54AHC573FK
5962-9685601QRA	Active	Production	CDIP (J) | 20	20 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9685601QRA SNJ54AHC573J
5962-9685601QSA	Active	Production	CFP (W) | 20	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9685601QSA SNJ54AHC573W
SN74AHC573DBR	Active	Production	SSOP (DB) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HA573
SN74AHC573DBR.A	Active	Production	SSOP (DB) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HA573
SN74AHC573DGSR	Active	Production	VSSOP (DGS) | 20	5000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	AHC573
SN74AHC573DGVR	Active	Production	TVSOP (DGV) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HA573
SN74AHC573DGVR.A	Active	Production	TVSOP (DGV) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HA573
SN74AHC573DW	Obsolete	Production	SOIC (DW) | 20	-	-	Call TI	Call TI	-40 to 125	AHC573
SN74AHC573DWR	Active	Production	SOIC (DW) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	AHC573
SN74AHC573DWR.A	Active	Production	SOIC (DW) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	AHC573
SN74AHC573DWRE4	Active	Production	SOIC (DW) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	AHC573
SN74AHC573DWRG4	Active	Production	SOIC (DW) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	AHC573
SN74AHC573N	Active	Production	PDIP (N) | 20	20 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 125	SN74AHC573N
SN74AHC573N.A	Active	Production	PDIP (N) | 20	20 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 125	SN74AHC573N
SN74AHC573NSR	Active	Production	SOP (NS) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	AHC573
SN74AHC573NSR.A	Active	Production	SOP (NS) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	AHC573
SN74AHC573PW	Obsolete	Production	TSSOP (PW) | 20	-	-	Call TI	Call TI	-40 to 125	HA573
SN74AHC573PWR	Active	Production	TSSOP (PW) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HA573
SN74AHC573PWR.A	Active	Production	TSSOP (PW) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HA573
SN74AHC573PWRG4	Active	Production	TSSOP (PW) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HA573
SN74AHC573PWRG4.A	Active	Production	TSSOP (PW) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HA573
SN74AHC573RKSR	Active	Production	VQFN (RKS) | 20	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	AHC573

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SNJ54AHC573FK	Active	Production	LCCC (FK) | 20	55 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9685601Q2A SNJ54AHC 573FK
SNJ54AHC573FK.A	Active	Production	LCCC (FK) | 20	55 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9685601Q2A SNJ54AHC 573FK
SNJ54AHC573J	Active	Production	CDIP (J) | 20	20 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9685601QRA SNJ54AHC573J
SNJ54AHC573J.A	Active	Production	CDIP (J) | 20	20 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9685601QRA SNJ54AHC573J
SNJ54AHC573W	Active	Production	CFP (W) | 20	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9685601QSA SNJ54AHC573W
SNJ54AHC573W.A	Active	Production	CFP (W) | 20	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9685601QSA SNJ54AHC573W

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

OTHER QUALIFIED VERSIONS OF SN54AHC573, SN74AHC573 :

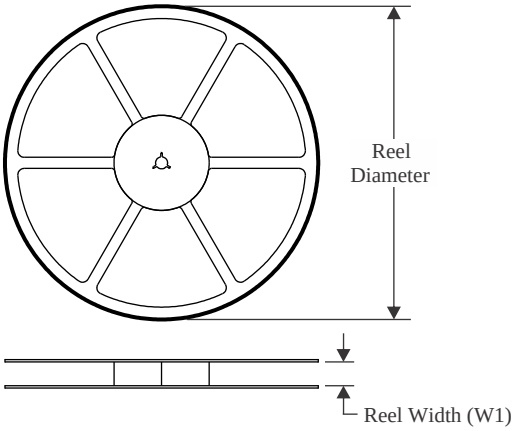
- Catalog : SN74AHC573
- Automotive : SN74AHC573-Q1, SN74AHC573-Q1
- Military : SN54AHC573

NOTE: Qualified Version Definitions:

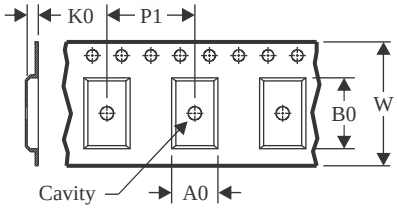
- Catalog - TI's standard catalog product
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects
- Military - QML certified for Military and Defense Applications

TAPE AND REEL INFORMATION

REEL DIMENSIONS

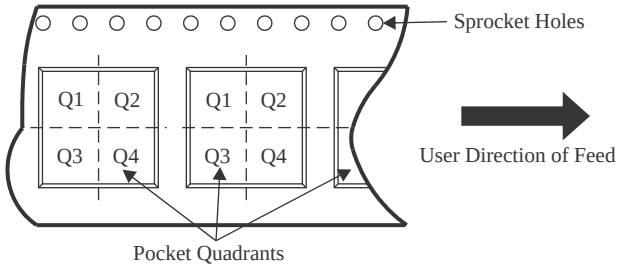


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

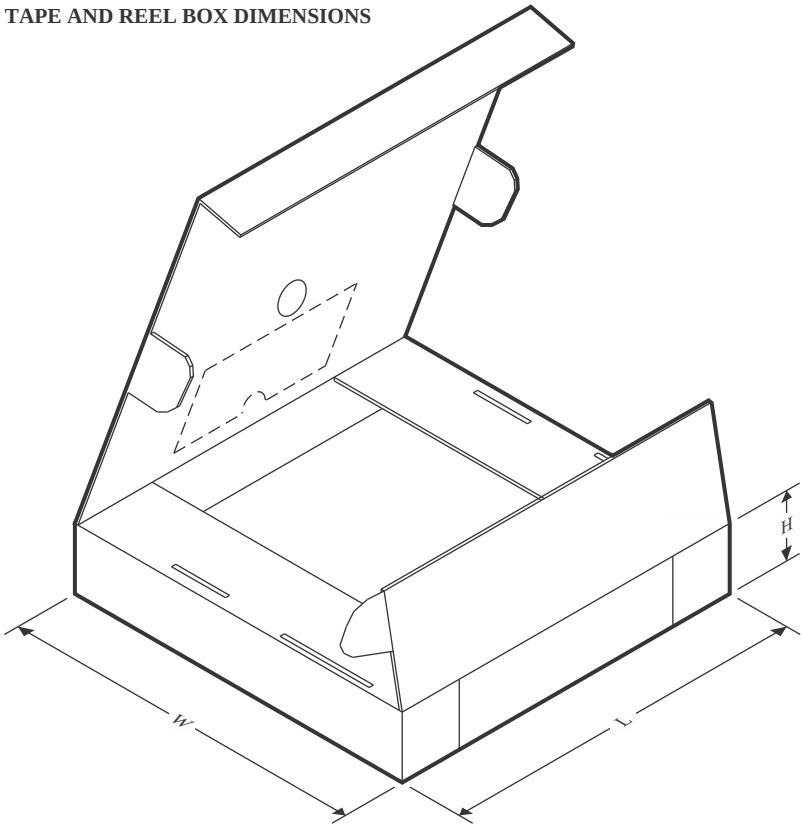
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74AHC573DBR	SSOP	DB	20	2000	330.0	16.4	8.2	7.5	2.5	12.0	16.0	Q1
SN74AHC573DGSR	VSSOP	DGS	20	5000	330.0	16.4	5.4	5.4	1.45	8.0	16.0	Q1
SN74AHC573DGVR	TVSOP	DGV	20	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74AHC573DWR	SOIC	DW	20	2000	330.0	24.4	10.9	13.3	2.7	12.0	24.0	Q1
SN74AHC573NSR	SOP	NS	20	2000	330.0	24.4	8.4	13.0	2.5	12.0	24.0	Q1
SN74AHC573PWR	TSSOP	PW	20	2000	330.0	16.4	6.95	7.0	1.4	8.0	16.0	Q1
SN74AHC573PWRG4	TSSOP	PW	20	2000	330.0	16.4	6.95	7.0	1.4	8.0	16.0	Q1
SN74AHC573RKSR	VQFN	RKS	20	3000	180.0	12.4	2.8	4.8	1.2	4.0	12.0	Q1

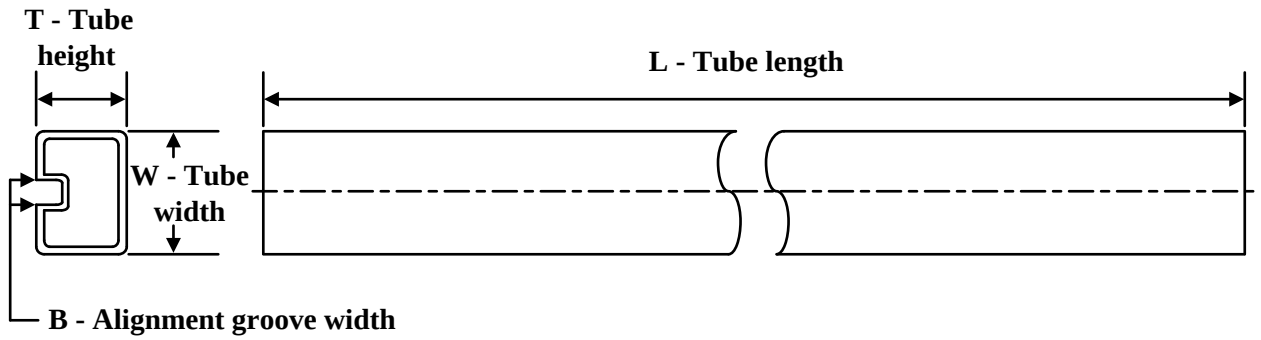
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74AHC573DBR	SSOP	DB	20	2000	353.0	353.0	32.0
SN74AHC573DGSR	VSSOP	DGS	20	5000	353.0	353.0	32.0
SN74AHC573DGVR	TVSOP	DGV	20	2000	353.0	353.0	32.0
SN74AHC573DWR	SOIC	DW	20	2000	356.0	356.0	45.0
SN74AHC573NSR	SOP	NS	20	2000	356.0	356.0	45.0
SN74AHC573PWR	TSSOP	PW	20	2000	353.0	353.0	32.0
SN74AHC573PWRG4	TSSOP	PW	20	2000	353.0	353.0	32.0
SN74AHC573RKSR	VQFN	RKS	20	3000	210.0	185.0	35.0

TUBE



*All dimensions are nominal

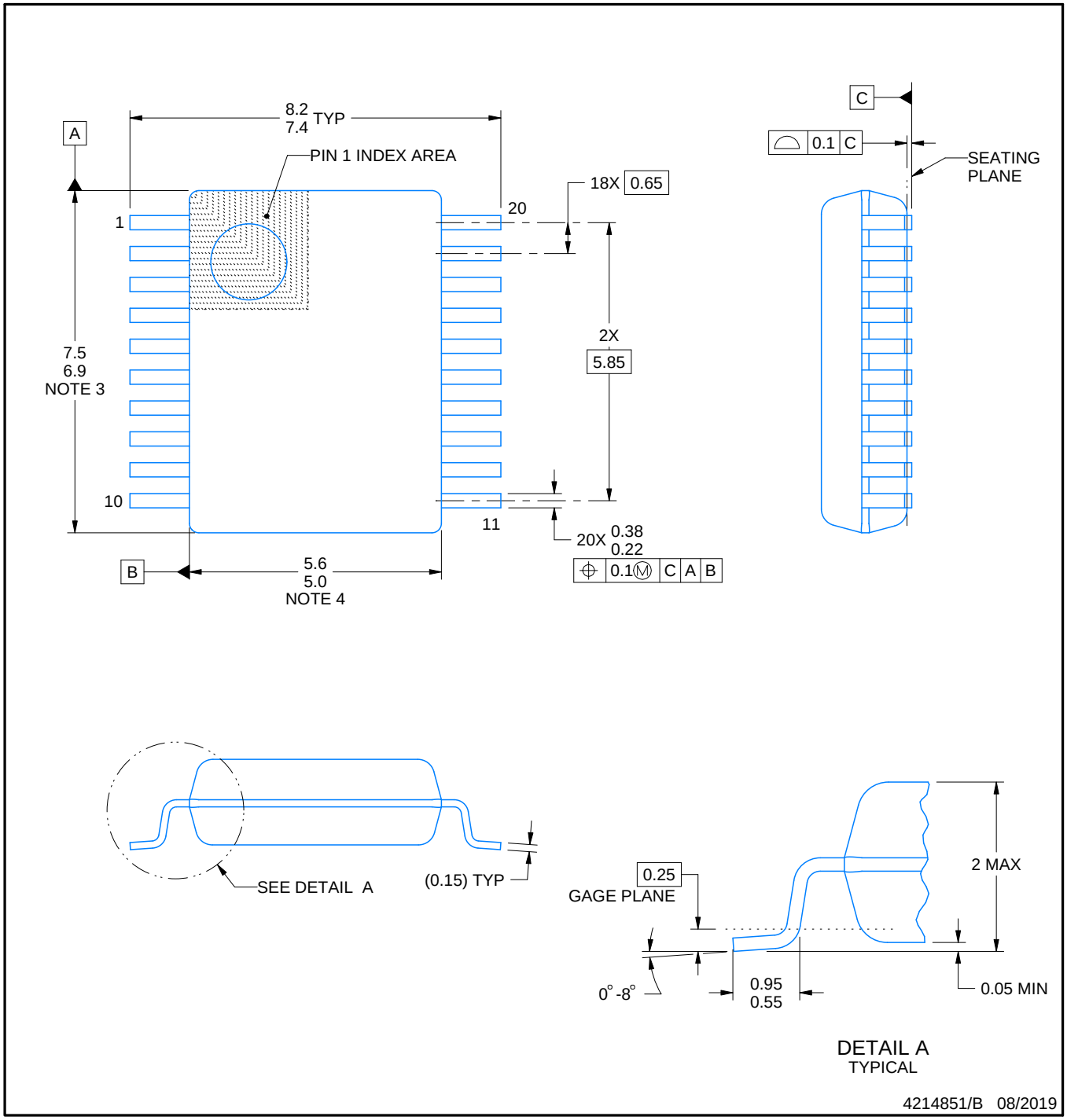
Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
5962-9685601Q2A	FK	LCCC	20	55	506.98	12.06	2030	NA
5962-9685601QSA	W	CFP	20	25	506.98	26.16	6220	NA
SN74AHC573N	N	PDIP	20	20	506	13.97	11230	4.32
SN74AHC573N.A	N	PDIP	20	20	506	13.97	11230	4.32
SNJ54AHC573FK	FK	LCCC	20	55	506.98	12.06	2030	NA
SNJ54AHC573FK.A	FK	LCCC	20	55	506.98	12.06	2030	NA
SNJ54AHC573W	W	CFP	20	25	506.98	26.16	6220	NA
SNJ54AHC573W.A	W	CFP	20	25	506.98	26.16	6220	NA

PACKAGE OUTLINE

DB0020A

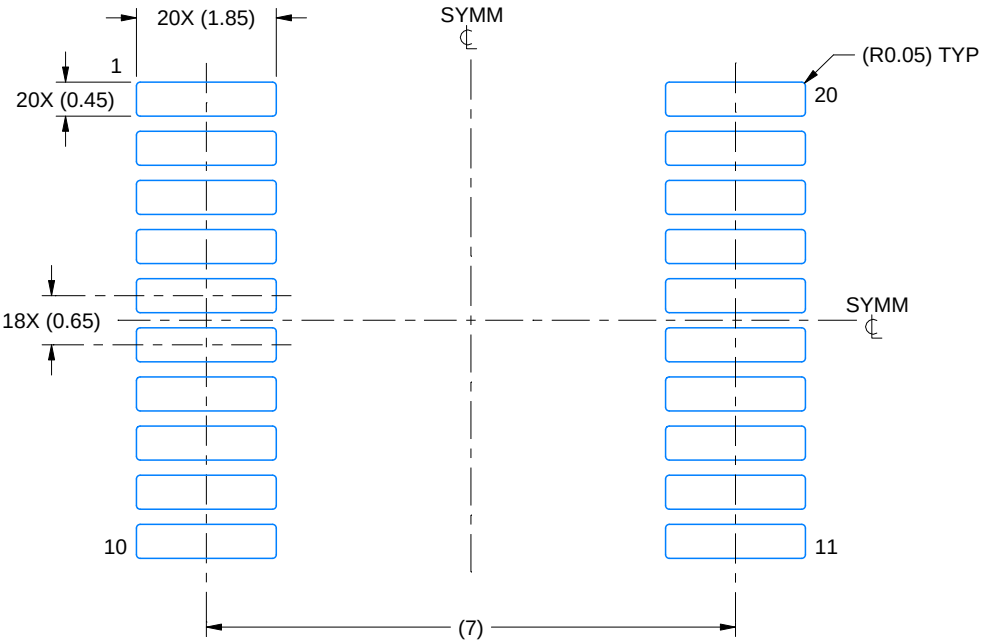
SSOP - 2 mm max height

SMALL OUTLINE PACKAGE

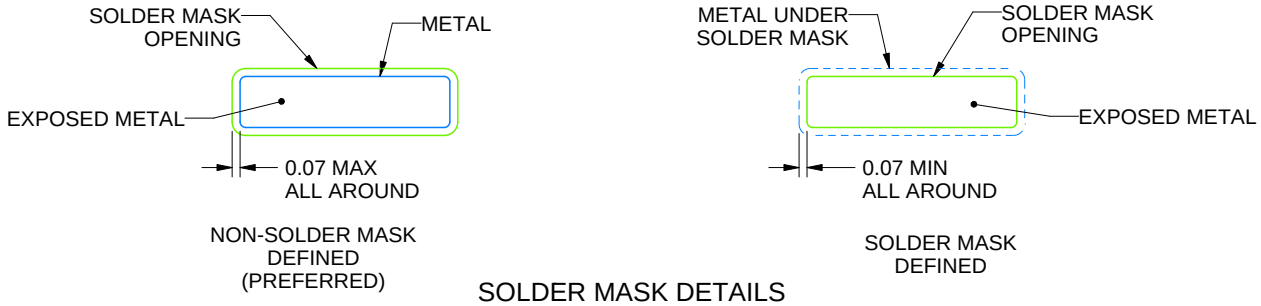


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-150.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



SOLDER MASK DETAILS

4214851/B 08/2019

NOTES: (continued)

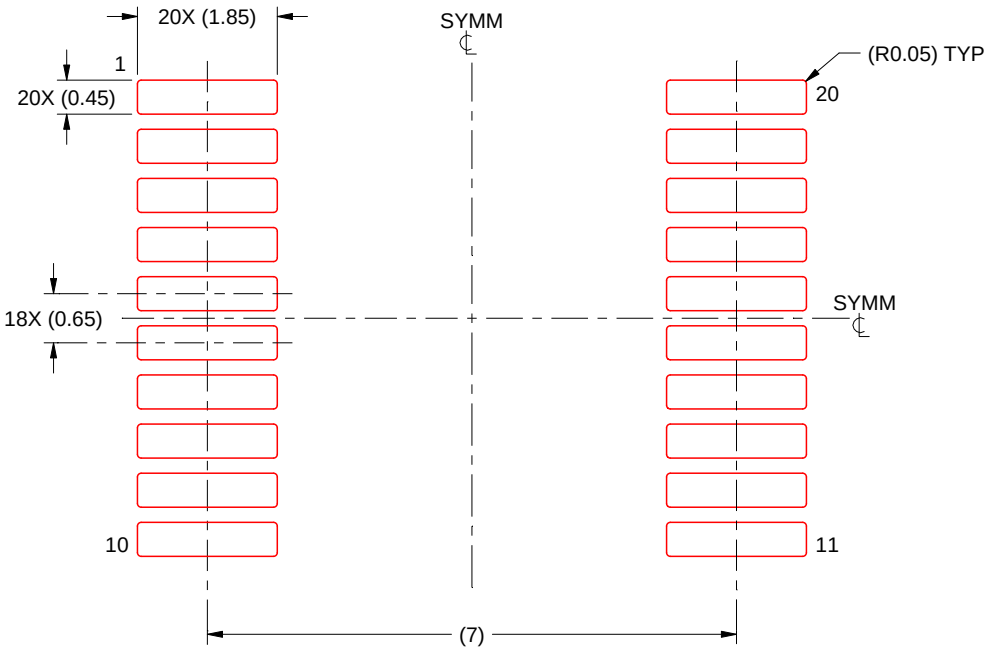
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DB0020A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4214851/B 08/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

GENERIC PACKAGE VIEW

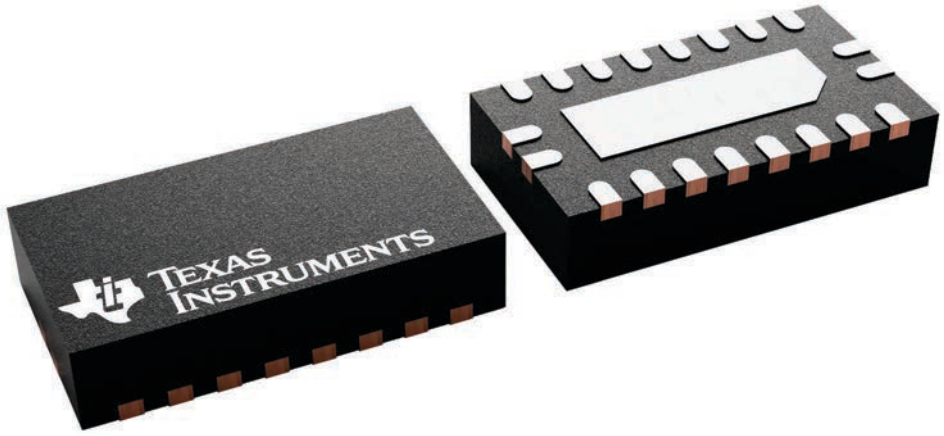
RKS 20

VQFN - 1 mm max height

2.5 x 4.5, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

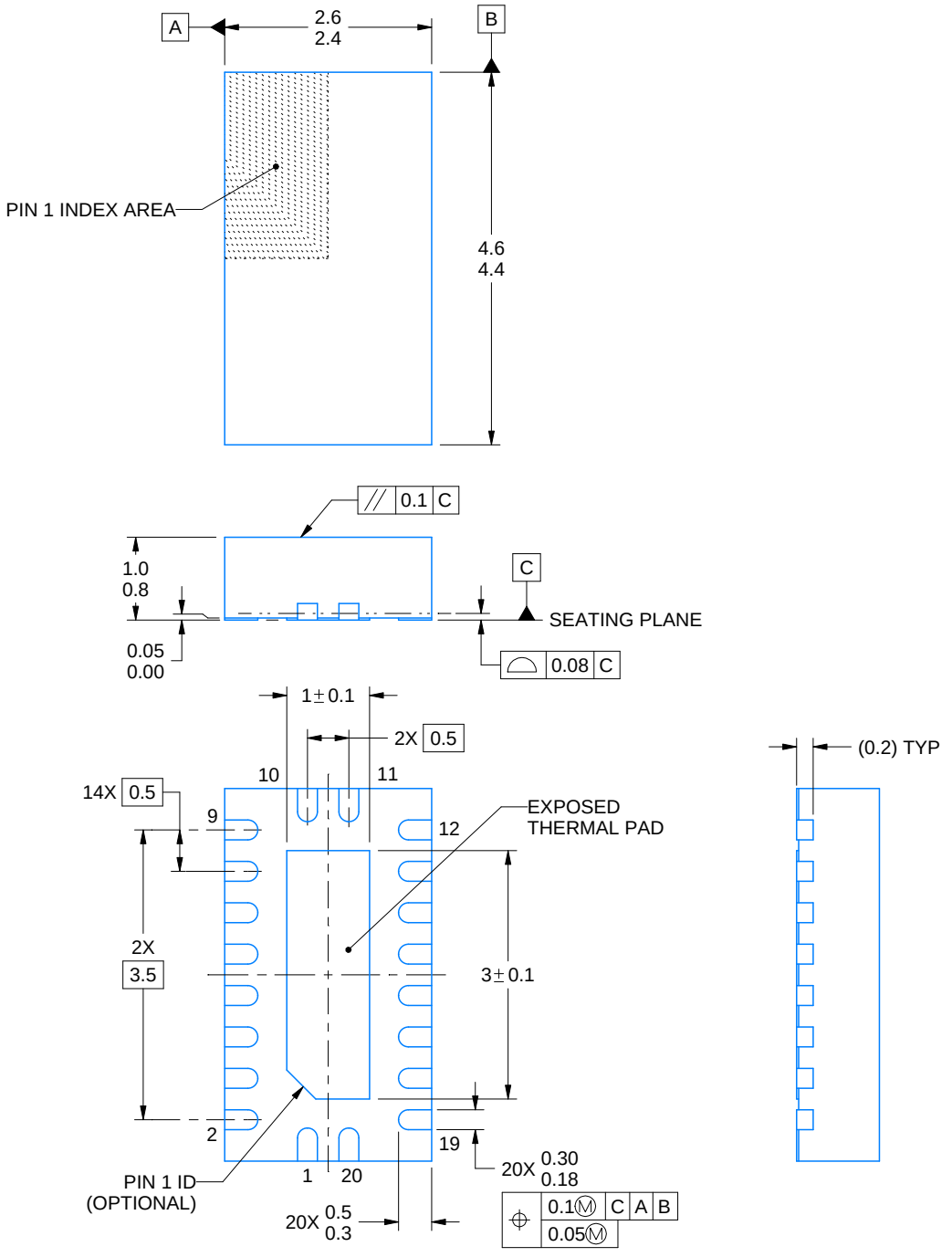


PACKAGE OUTLINE

RKS0020A

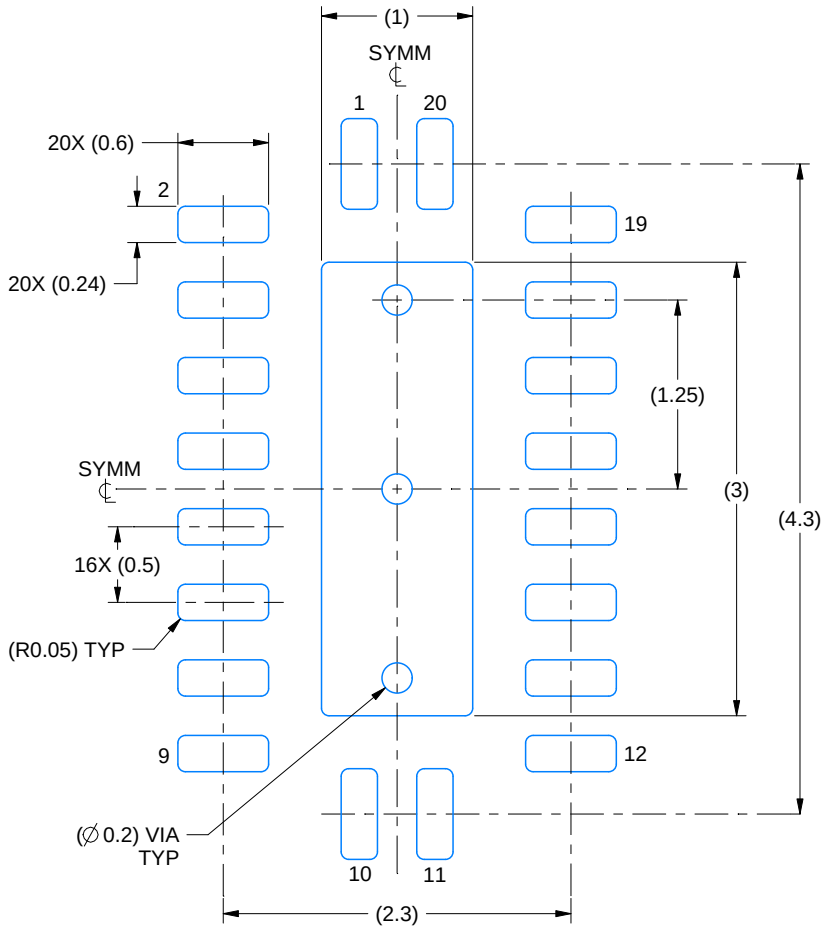
VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

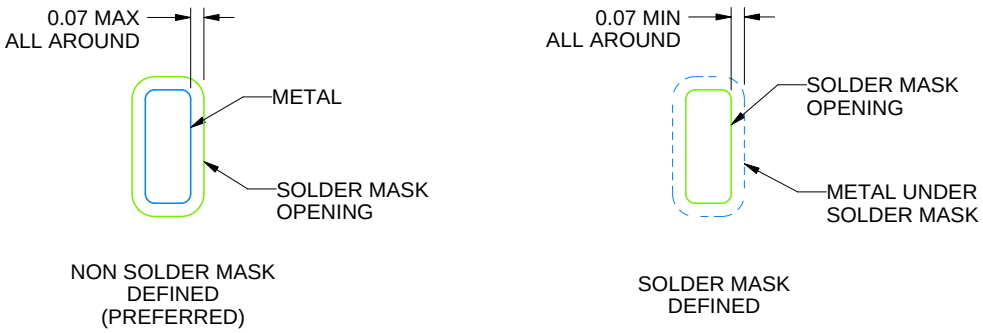


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
SCALE:20X

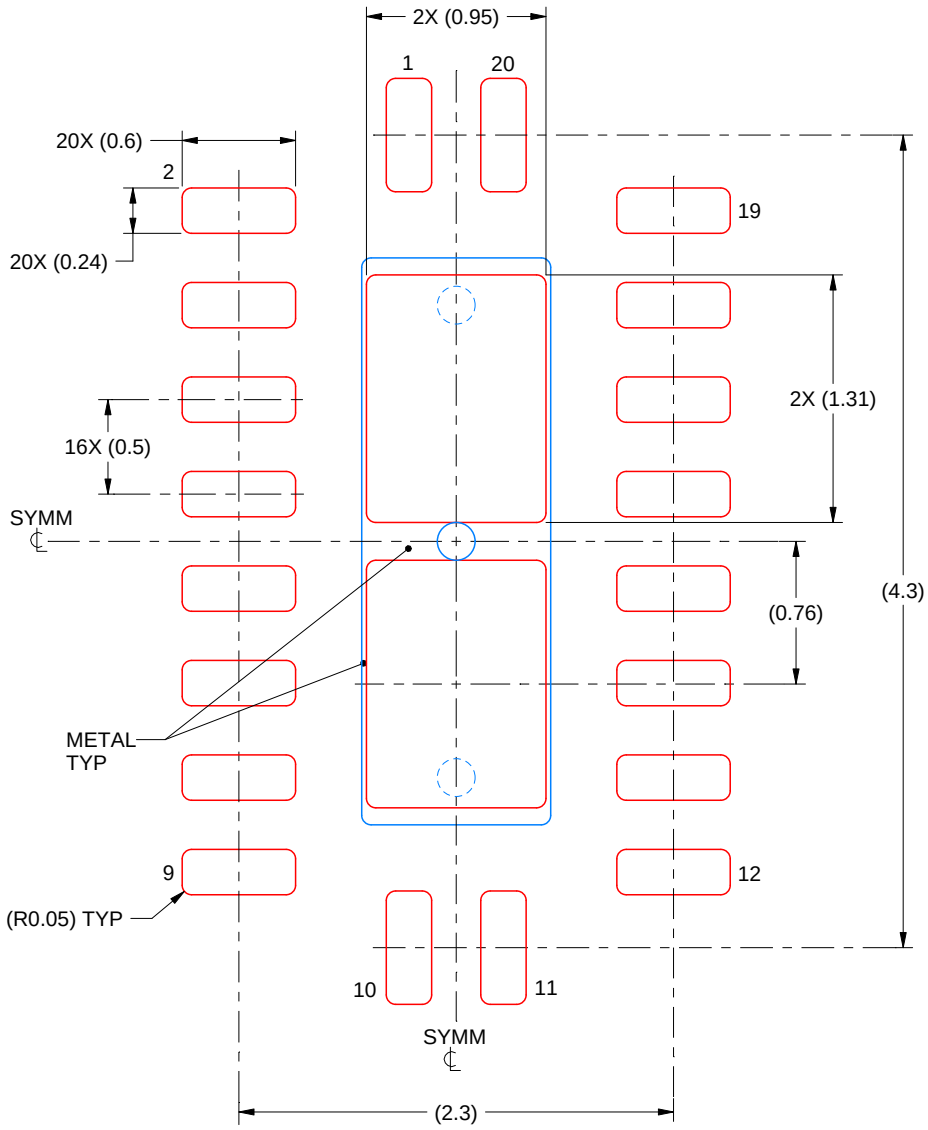


SOLDER MASK DETAILS

4222490/B 02/2021

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If some or all are implemented, recommended via locations are shown.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
83% PRINTED SOLDER COVERAGE BY AREA
SCALE:25X

4222490/B 02/2021

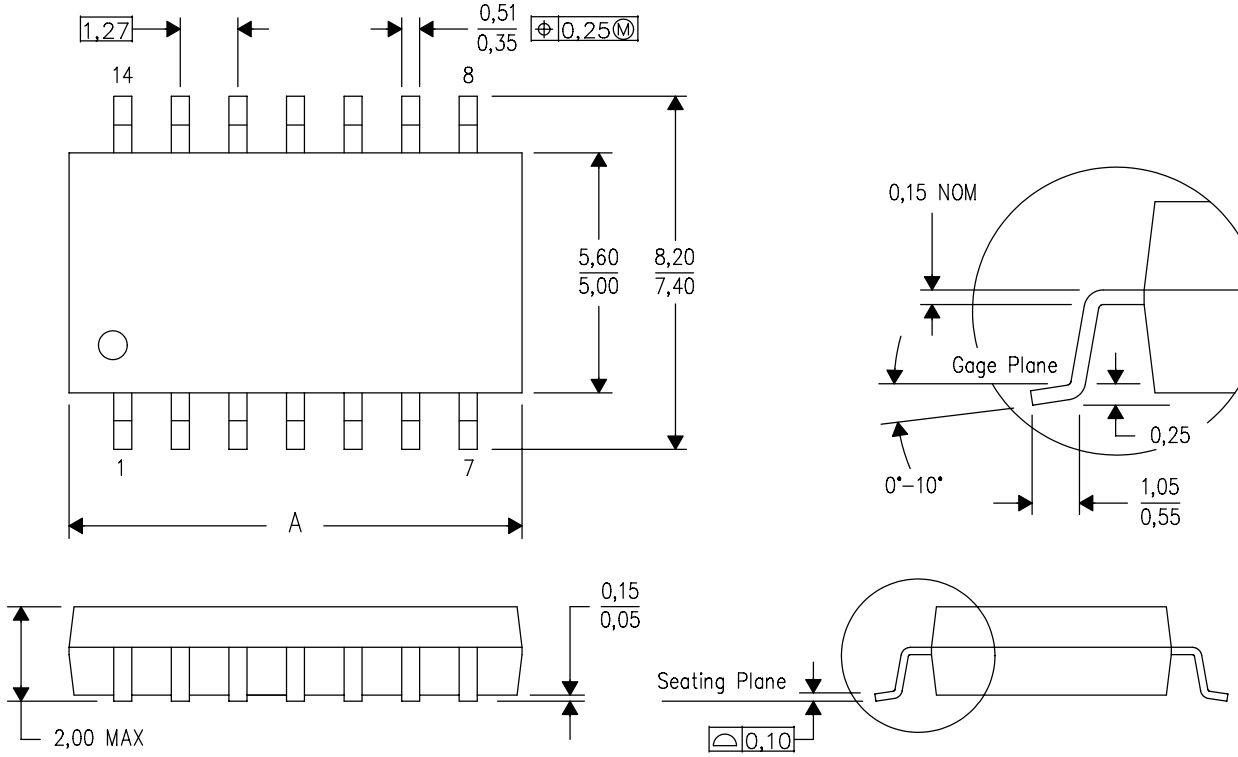
NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

MECHANICAL DATA

NS (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

14-PINS SHOWN



DIM \ PINS **	14	16	20	24
A MAX	10,50	10,50	12,90	15,30
A MIN	9,90	9,90	12,30	14,70

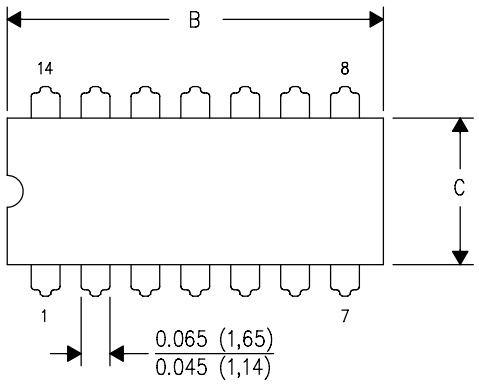
4040062/C 03/03

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

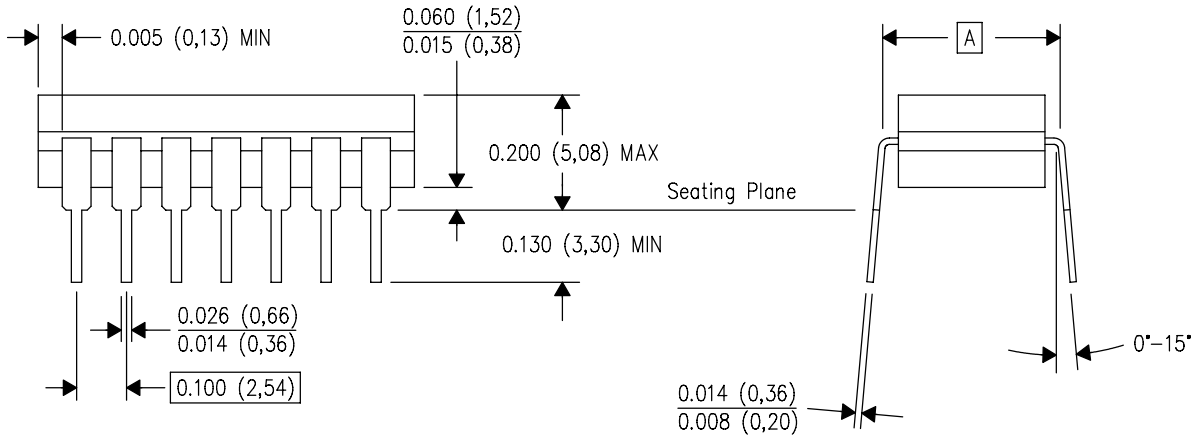
J (R–GDIP–T**)

14 LEADS SHOWN

CERAMIC DUAL IN–LINE PACKAGE



DIM \ PINS **	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)

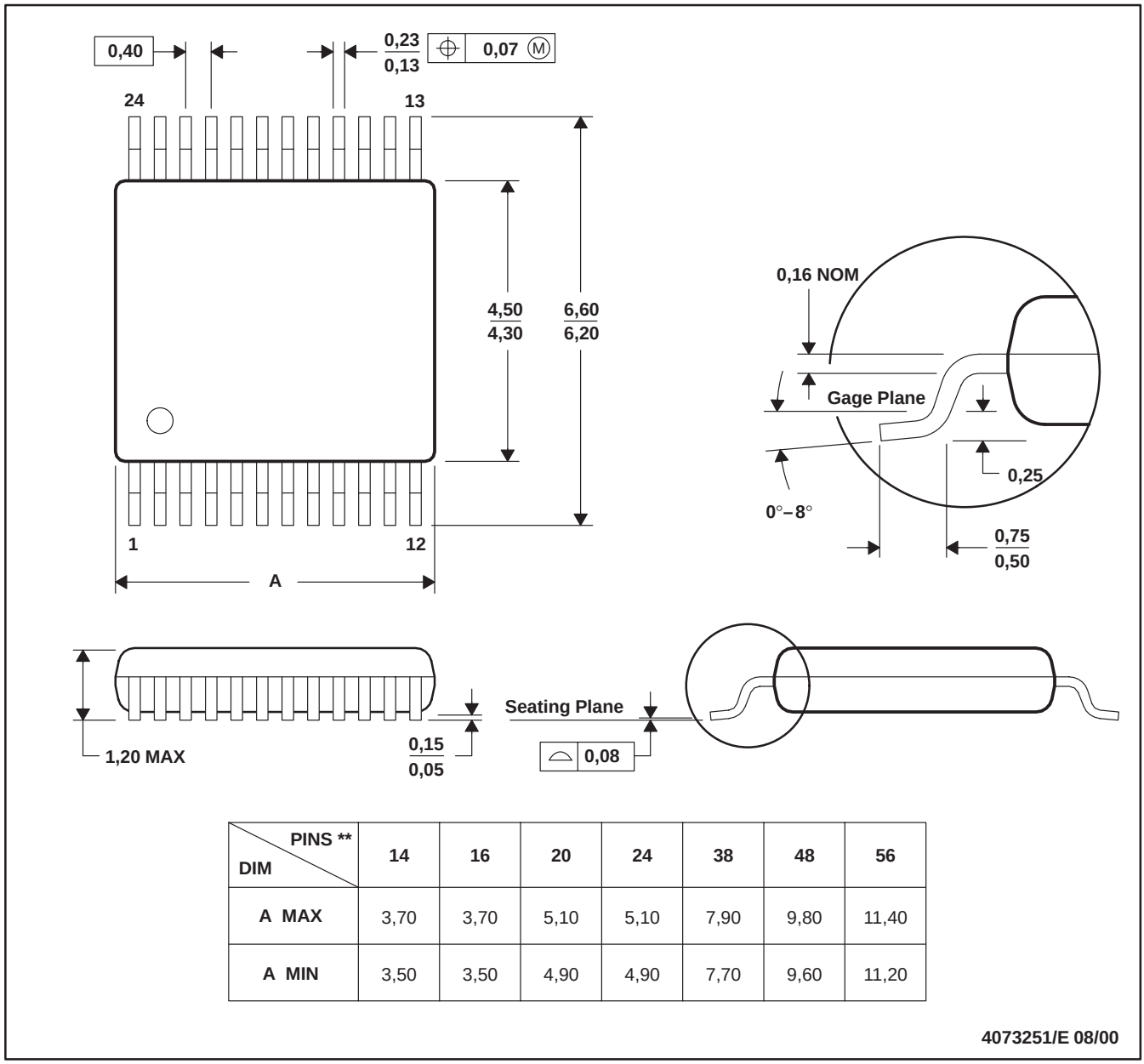


4040083/F 03/03

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package is hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
E. Falls within MIL STD 1835 GDIP1–T14, GDIP1–T16, GDIP1–T18 and GDIP1–T20.

DGV (R-PDSO-G)** **PLASTIC SMALL-OUTLINE**

24 PINS SHOWN



DIM \ PINS **	14	16	20	24	38	48	56
A MAX	3,70	3,70	5,10	5,10	7,90	9,80	11,40
A MIN	3,50	3,50	4,90	4,90	7,70	9,60	11,20

4073251/E 08/00

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.
D. Falls within JEDEC: 24/48 Pins – MO-153
14/16/20/56 Pins – MO-194

GENERIC PACKAGE VIEW

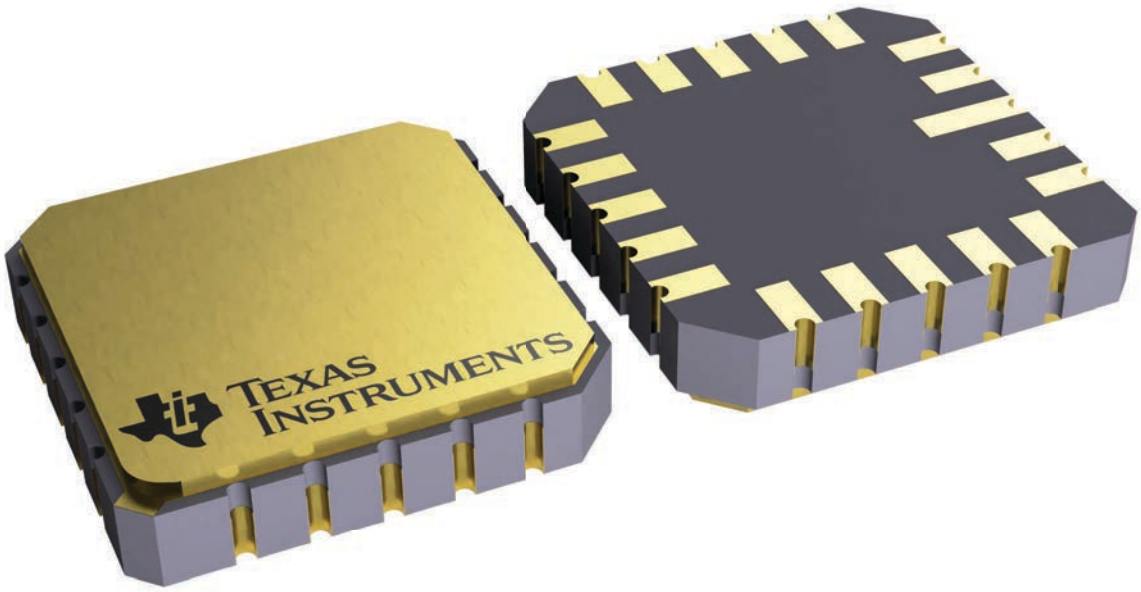
FK 20

LCCC - 2.03 mm max height

8.89 x 8.89, 1.27 mm pitch

LEADLESS CERAMIC CHIP CARRIER

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

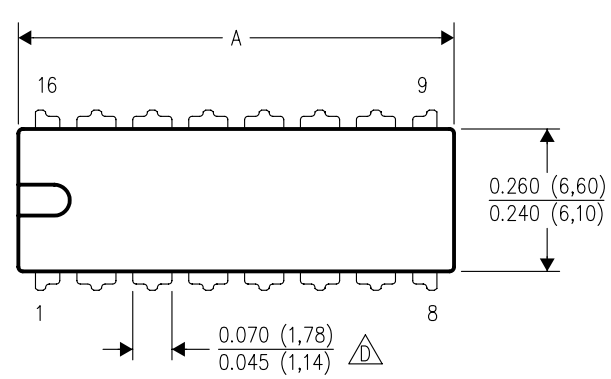


4229370VA\

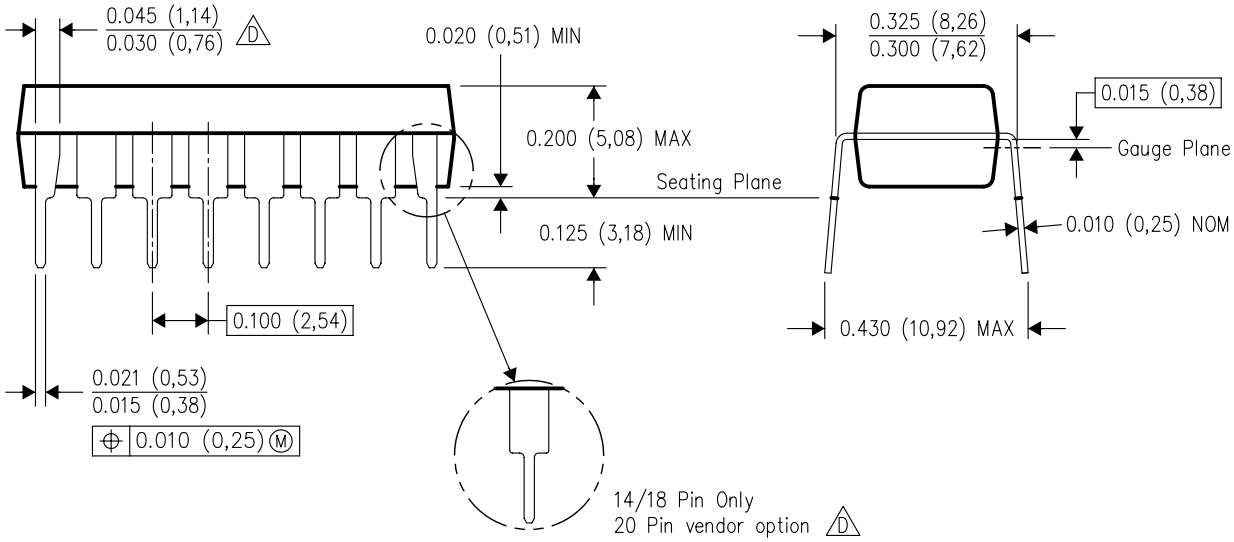
N (R–PDIP–T**)

PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN

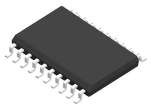


DIM \ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS–001 VARIATION (C)	AA	BB	AC	AD



4040049/E 12/2002

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

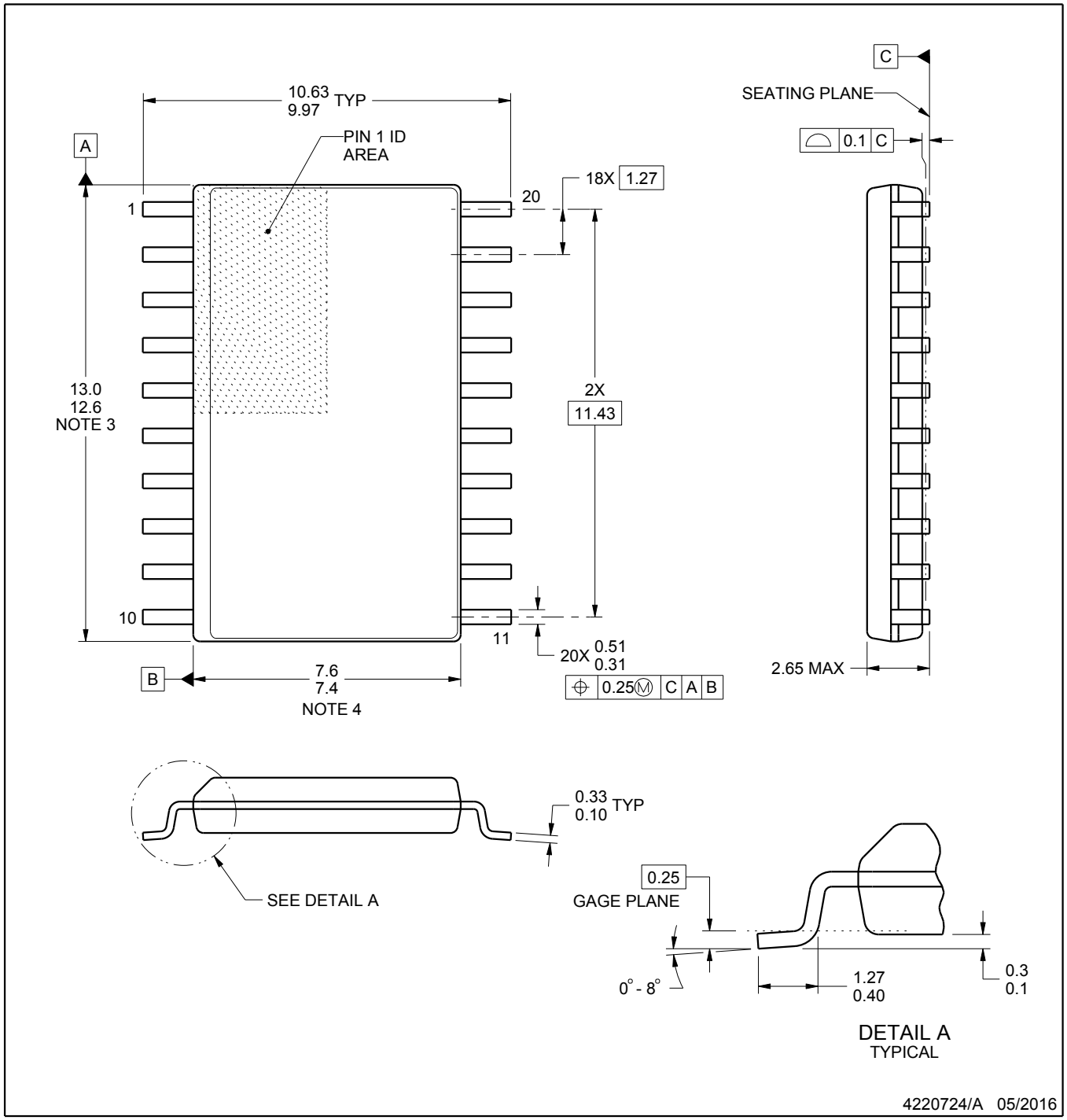


PACKAGE OUTLINE

DW0020A

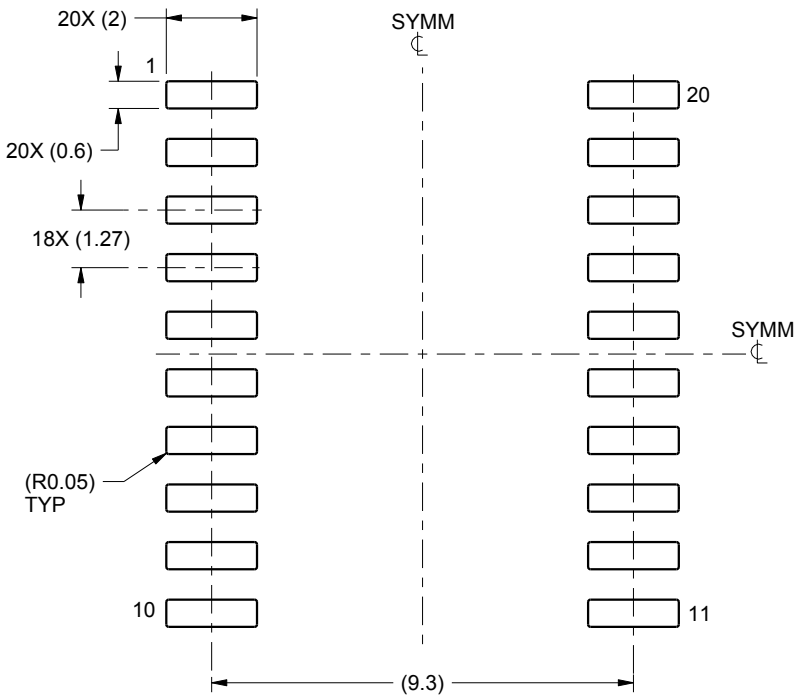
SOIC - 2.65 mm max height

SOIC

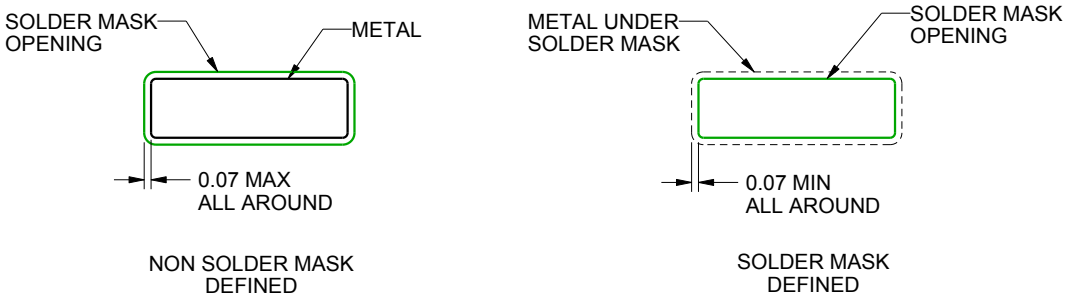


NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm per side.
5. Reference JEDEC registration MS-013.



LAND PATTERN EXAMPLE
SCALE:6X

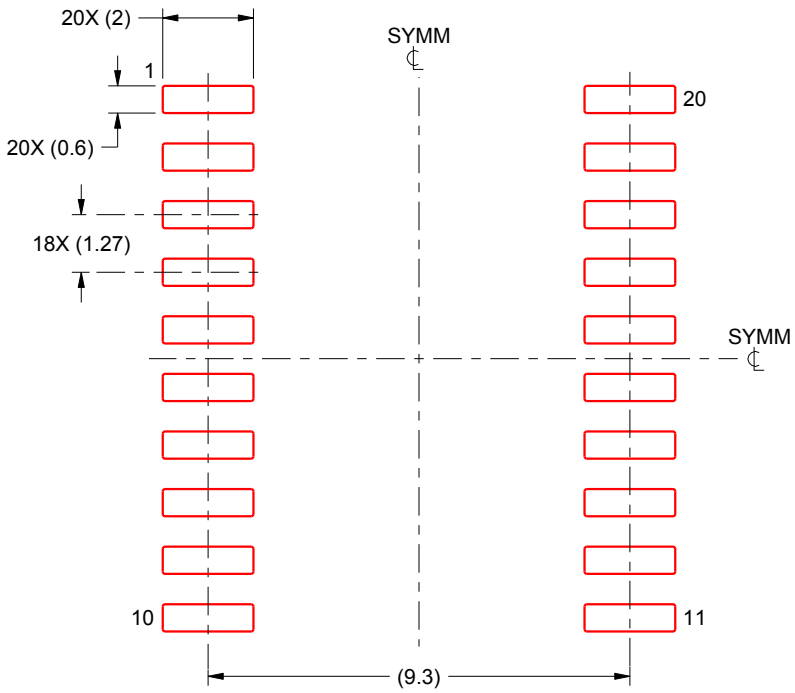


SOLDER MASK DETAILS

4220724/A 05/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



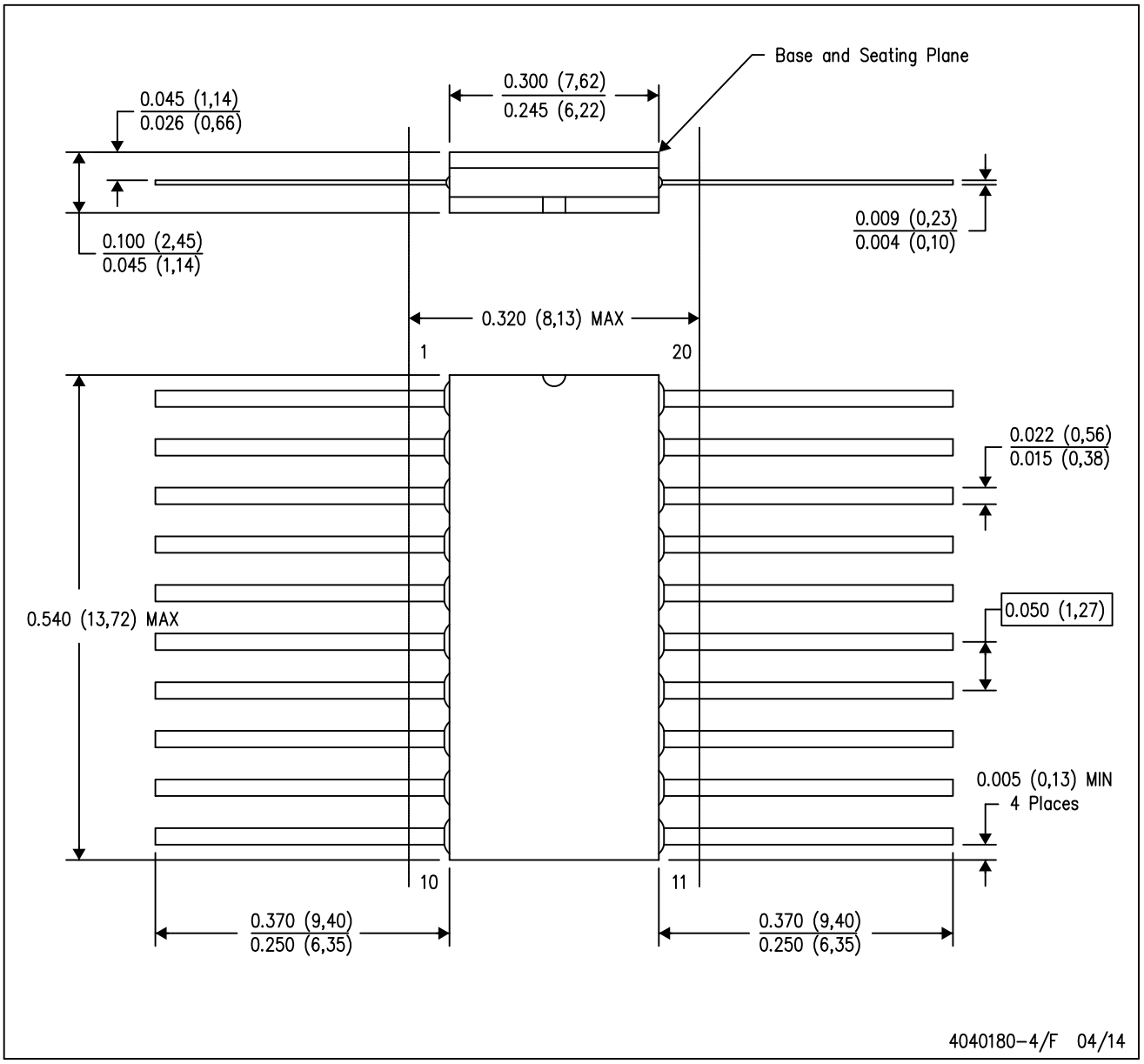
SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

4220724/A 05/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

W (R–GDFP–F20) CERAMIC DUAL FLATPACK



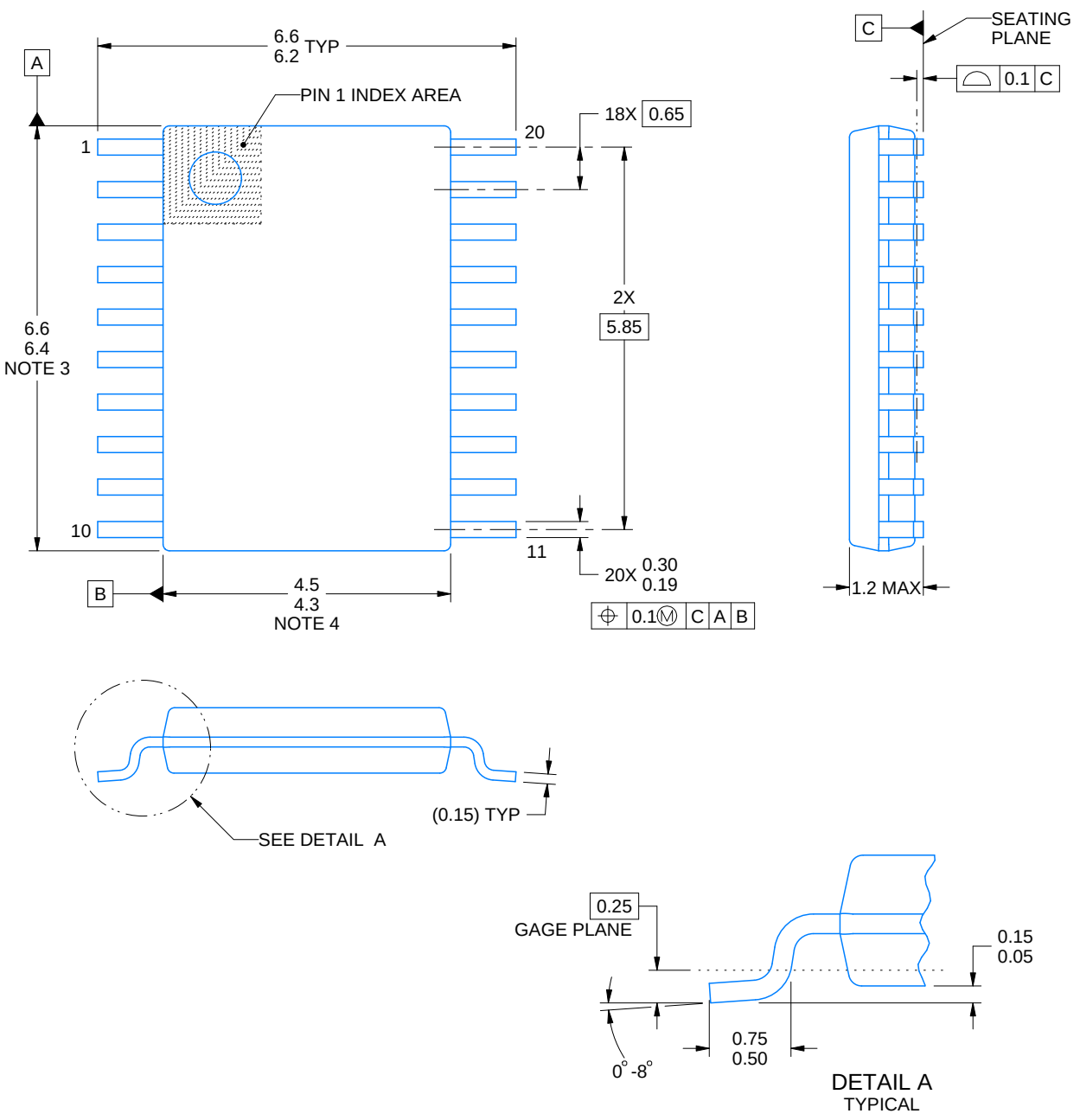
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only.
E. Falls within Mil–Std 1835 GDFP2–F20

PACKAGE OUTLINE

PW0020A

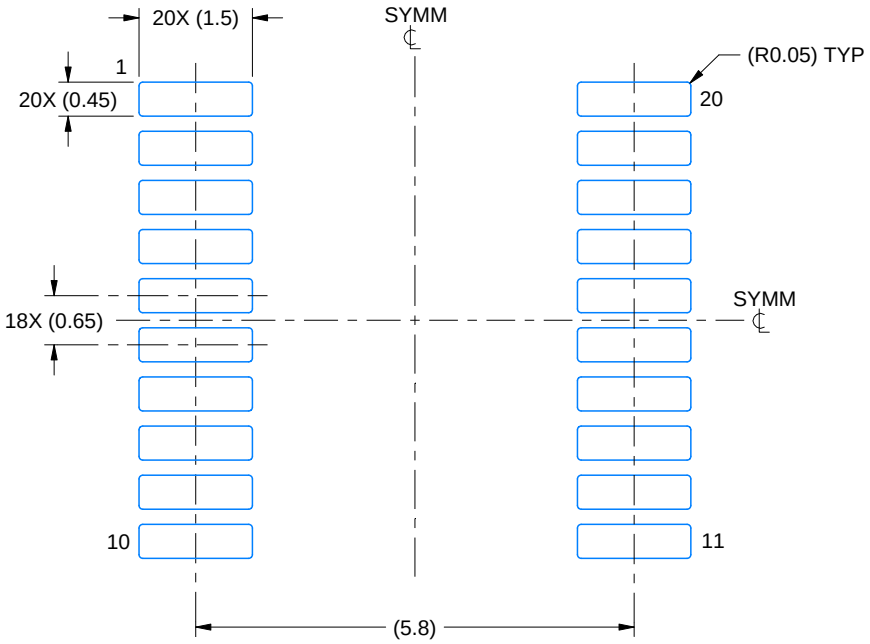
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



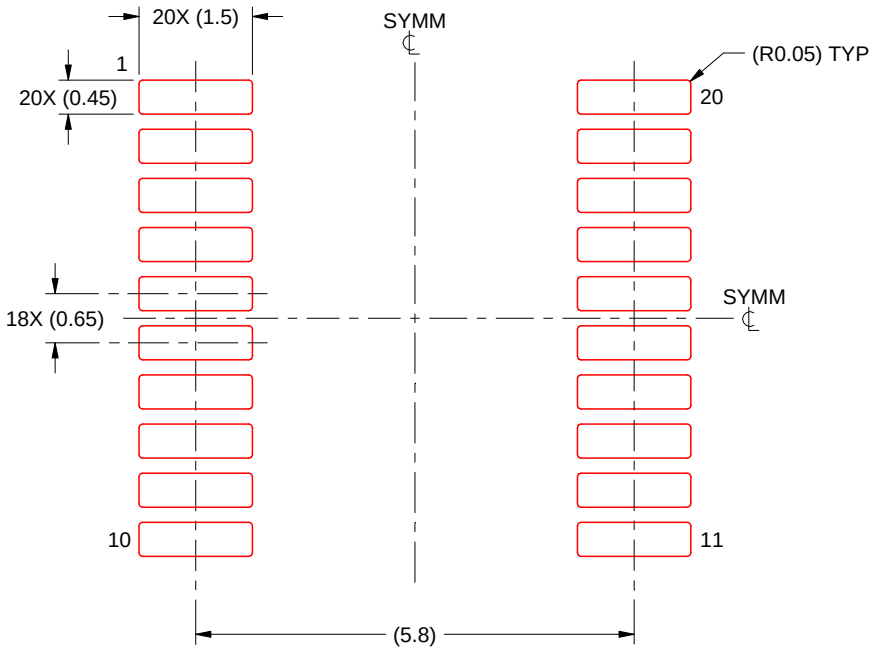
LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

SOLDER MASK DETAILS

4220206/A 02/2017

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220206/A 02/2017

NOTES: (continued)

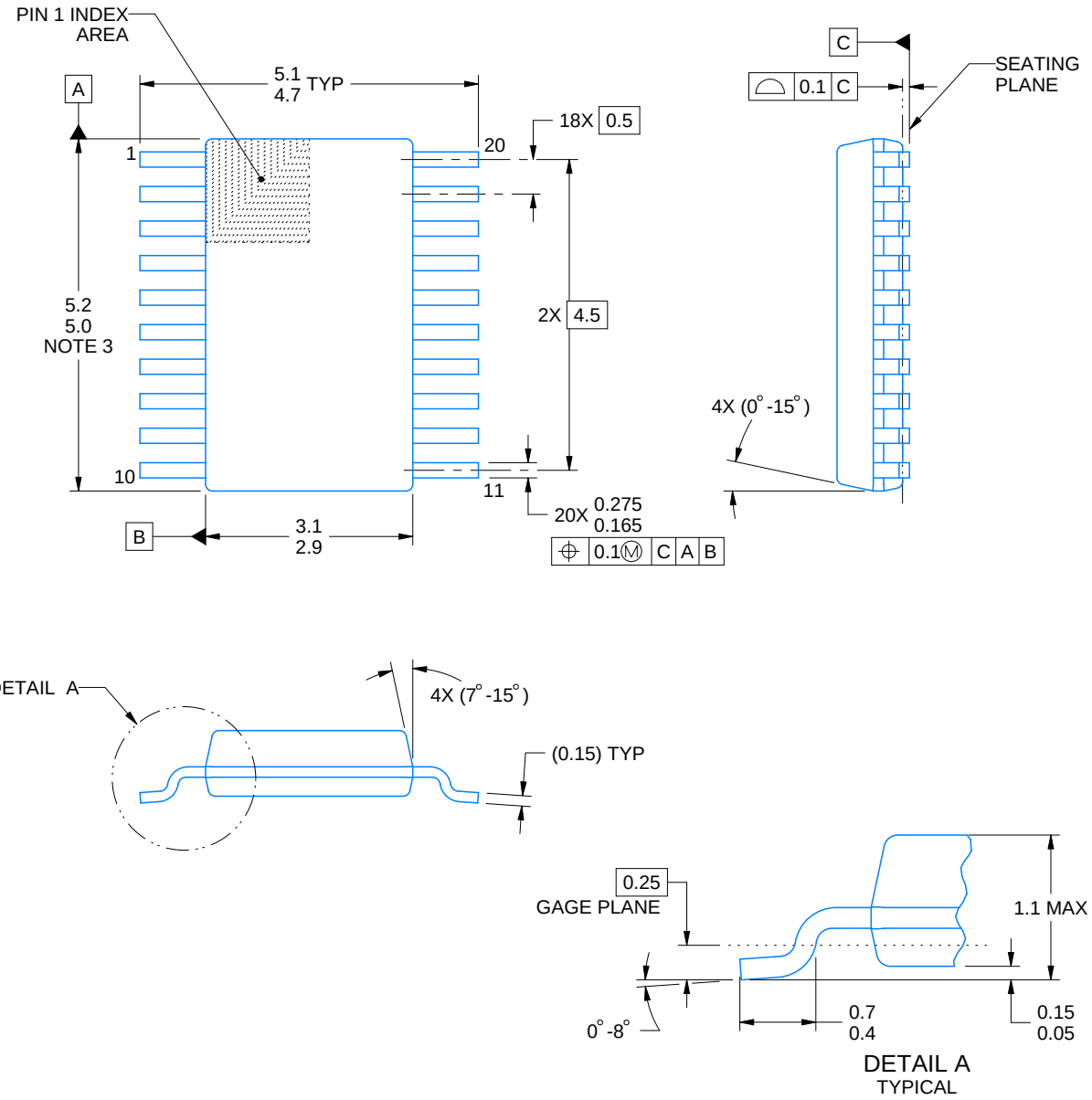
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

DGS0020A

VSSOP - 1.1 mm max height

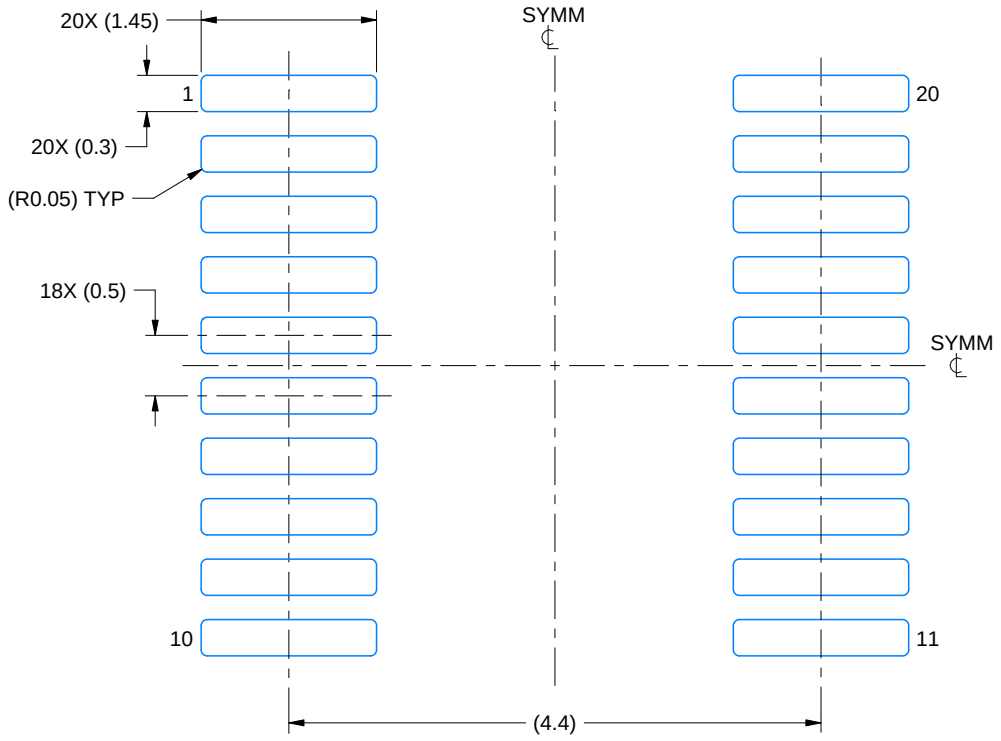
SMALL OUTLINE PACKAGE



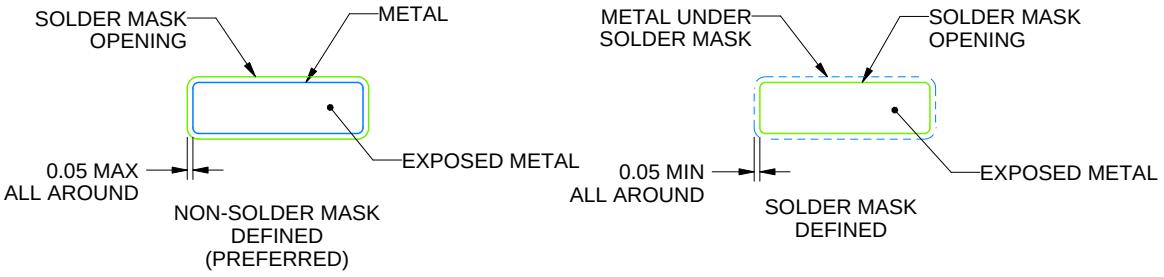
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. No JEDEC registration as of September 2020.
5. Features may differ or may not be present.



LAND PATTERN EXAMPLE
SCALE: 16X

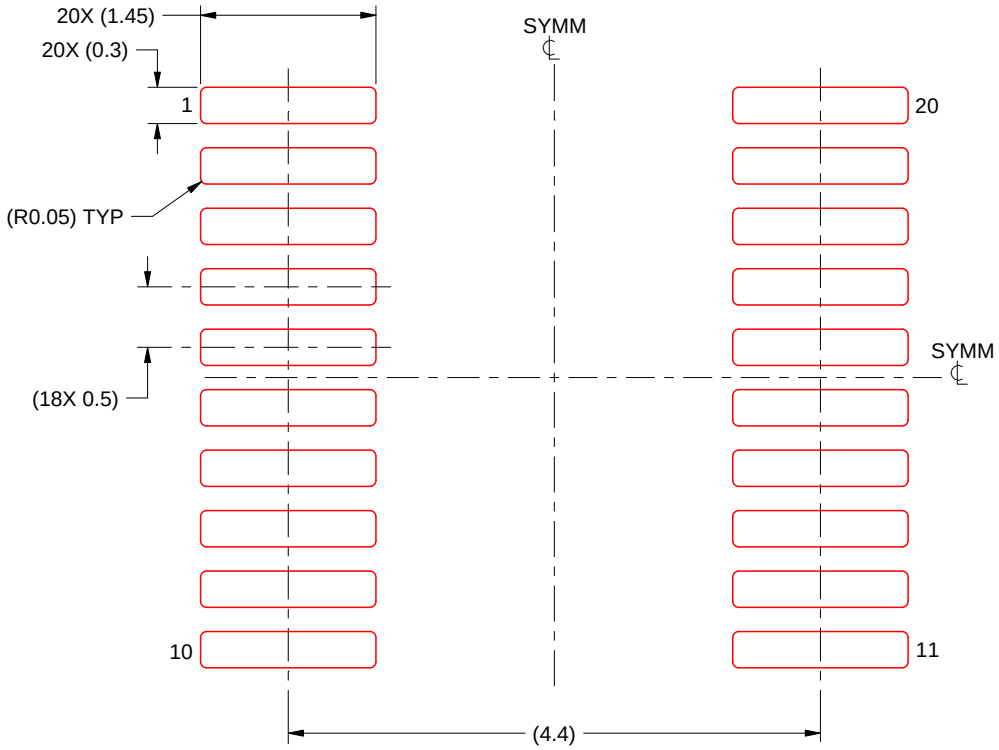


SOLDER MASK DETAILS

4226367/A 10/2020

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
9. Size of metal pad may vary due to creepage requirement.
10. Vias are optional depending on application, refer to device data sheet. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 16X

4226367/A 10/2020

NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

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最后更新日期：2025 年 10 月