- **Eight Latches in a Single Package**
- **3-State Bus-Driving True Outputs**
- **Full Parallel Access for Loading**
- **Buffered Control Inputs**
- **pnp Inputs Reduce dc Loading on Data Lines**

description

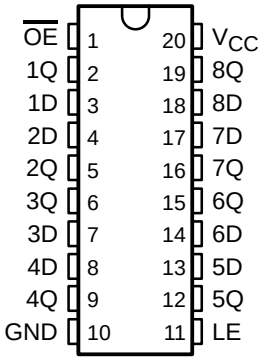
These octal transparent D-type latches feature 3-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. They are particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

While the latch-enable (LE) input is high, the Q outputs follow the data (D) inputs. When LE is taken low, the Q outputs are latched at the logic levels set up at the D inputs.

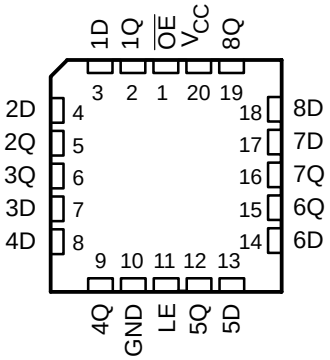
A buffered output-enable ($\overline{OE}$) input can be used to place the eight outputs in either a normal logic state (high or low) or a high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and the increased drive provide the capability to drive bus lines without interface or pullup components.

$\overline{OE}$ does not affect internal operations of the latches. Old data can be retained or new data can be entered while the outputs are off.

SN54ALS373A, . . . J OR W PACKAGE
SN54AS373 . . . J PACKAGE
SN74ALS373A, SN74AS373 . . . DW, N, OR NS PACKAGE
(TOP VIEW)



SN54ALS373A, SN54AS373 . . . FK PACKAGE
(TOP VIEW)



ORDERING INFORMATION

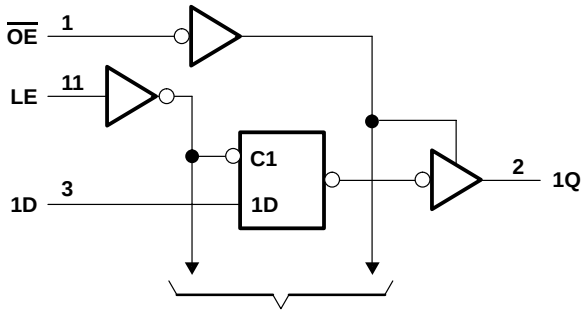
T_A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
0°C to 70°C	PDIP – N	Tube	SN74ALS373AN	SN74ALS373AN
			SN74AS373N	SN74AS373N
	SOIC – DW	Tube	SN74ALS373ADW	ALS373A
		Tape and reel	SN74ALS373ADWR	
		Tube	SN74AS373DW	AS373
		Tape and reel	SN74AS373DWR	
	SOP – NS	Tape and reel	SN74ALS373ANSR	ALS373A
			SN74AS373NSR	74AS373
–55°C to 125°C	CDIP – J	Tube	SNJ54ALS373AJ	SNJ54ALS373AJ
			SNJ54AS373J	SNJ54AS373J
	CFP – W	Tube	SNJ54ALS373AW	SNJ54ALS373AW
	LCCC – FK	Tube	SNJ54ALS373AFK	SNJ54ALS373AFK
			SNJ54AS373FK	SNJ54AS373FK

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

FUNCTION TABLE
(each latch)

INPUTS			OUTPUT
$\overline{OE}$	LE	D	Q
L	H	H	H
L	H	L	L
L	L	X	Q_0
H	X	X	Z

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (SN54ALS373A, SN74ALS373A) (unless otherwise noted)†

Supply voltage, V_{CC} . . . . . 7 V
Input voltage, V_I . . . . . 7 V
Voltage applied to any output in the high state or power-off state . . . . . 5.5 V
Package thermal impedance, θ_{JA} (see Note 1): DW package . . . . . 58°C/W
N package . . . . . 69°C/W
NS package . . . . . 60°C/W
Storage temperature range, T_{stg} . . . . . –65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions

		SN54ALS373A			SN74ALS373A			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.7			0.8	V
I_{OH}	High-level output current			–1			–2.6	mA
I_{OL}	Low-level output current			12			24	mA
T_A	Operating free-air temperature	–55		125	0		70	°C

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 1)

		SN54ALS373A		SN74ALS373A		UNIT
		MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency					MHz
t_w	Pulse duration, LE high	12		10		ns
t_{su}	Setup time, data before LE↓	10		10		ns
t_h	Hold time, data after LE↓	7		7		ns

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54ALS373A			SN74ALS373A			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = –18 mA			–1.5			–1.5	V
V_{OH}	V_{CC} = 4.5 V to 5.5 V,	I_{OH} = –0.4 mA	V_{CC}–2			V_{CC}–2			V
	V_{CC} = 4.5 V	I_{OH} = –1 mA	2.4	3.3					
		I_{OH} = –2.6 mA				2.4	3.2		
V_{OL}	V_{CC} = 4.5 V	I_{OL} = 12 mA		0.25	0.4		0.25	0.4	V
		I_{OL} = 24 mA					0.35	0.5	
I_{OZH}	V_{CC} = 5.5 V,	V_O = 2.7 V			20			20	µA
I_{OZL}	V_{CC} = 5.5 V,	V_O = 0.4 V			–20			–20	µA
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	µA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.4 V			–0.1			–0.1	mA
I_O‡	V_{CC} = 5.5 V,	V_O = 2.25 V	–20		–112	–30		–112	mA
I_{CC}	V_{CC} = 5.5 V	Outputs high		9	16		9	16	mA
		Outputs low		16	25		16	25	
		Outputs disabled		17	27		17	27	

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ The output conditions have been chosen to produce a current that closely approximates one-half of the true short-circuit output current, I_{OS}.

switching characteristics (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX§				UNIT
			SN54ALS373A		SN74ALS373A		
			MIN	MAX	MIN	MAX	
t_{PLH}	D	Q	2	17	2	12	ns
t_{PHL}			1	19	4	16	
t_{PLH}	LE	Any Q	6	29	6	22	ns
t_{PHL}			1	27	7	23	
t_{PZH}	$\overline{OE}$	Any Q	6	22	1	18	ns
t_{PZL}			5	24	5	20	
t_{PHZ}	$\overline{OE}$	Any Q	2	16	1	10	ns
t_{PLZ}			2	24	2	12	

§ For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

absolute maximum ratings over operating free-air temperature range (SN54AS373, SN74AS373) (unless otherwise noted)†

Supply voltage, V_{CC} . . . . . 7 V
Input voltage, V_I . . . . . 7 V
Voltage applied to any output in the high state or power-off state . . . . . 5.5 V
Package thermal impedance, θ_{JA} (see Note 1): DW package . . . . . 58°C/W
N package . . . . . 69°C/W
NS package . . . . . 60°C/W
Storage temperature range, T_{stg} . . . . . –65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 2: The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions

		SN54AS373			SN74AS373			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{OH}	High-level output current			–12			–15	mA
I_{OL}	Low-level output current			32			48	mA
T_A	Operating free-air temperature	–55		125	0		70	°C

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 1)

		SN54AS373		SN74AS373		UNIT
		MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency					MHz
t_w	Pulse duration, LE high	5.5*		4.5*		ns
t_{su}	Setup time, data before LE↓	2*		2*		ns
t_h	Hold time, data after LE↓	3*		3*		ns

* On products compliant to MIL-STD-883, Class B, this parameter is based on characterization data but is not production tested.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54AS373			SN74AS373			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	V_{CC} = 4.5 V,	I_I = –18 mA			–1.2			–1.2	V
V_{OH}	V_{CC} = 4.5 V to 5.5 V,	I_{OH} = –2 mA	V_{CC}–2			V_{CC}–2			V
	V_{CC} = 4.5 V	I_{OH} = –12 mA	2.4	3.2					
		I_{OH} = –15 mA				2.4	3.3		
V_{OL}	V_{CC} = 4.5 V	I_{OL} = 32 mA		0.27	0.5				V
		I_{OL} = 48 mA					0.32	0.5	
I_{OZH}	V_{CC} = 5.5 V,	V_O = 2.7 V			50			50	µA
I_{OZL}	V_{CC} = 5.5 V,	V_O = 0.4 V			–50			–50	µA
I_I	V_{CC} = 5.5 V,	V_I = 7 V			0.1			0.1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V			20			20	µA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.4 V		–0.02	–0.5		–0.02	–0.5	mA
I_O‡	V_{CC} = 5.5 V,	V_O = 2.25 V	–30		–112	–30		–112	mA
I_{CC}	V_{CC} = 5.5 V	Outputs high		55	90		55	90	mA
		Outputs low		55	85		55	85	
		Outputs disabled		65	100		65	100	

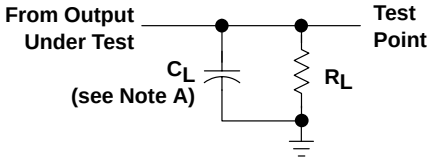
† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ The output conditions have been chosen to produce a current that closely approximates one-half of the true short-circuit output current, I_{OS}.

switching characteristics (see Figure 1)

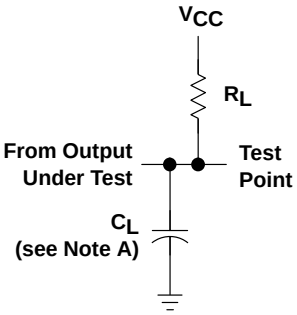
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = MIN to MAX§				UNIT
			SN54AS373		SN74AS373		
			MIN	MAX	MIN	MAX	
t_{PLH}	D	Q	3	9	3.5	6	ns
t_{PHL}			3	8	3.5	6	
t_{PLH}	LE	Any Q	6.5	14.5	6.5	11.5	ns
t_{PHL}			5	9	5	7.5	
t_{PZH}	$\overline{OE}$	Any Q	2	7.5	2	6.5	ns
t_{PZL}			4.5	10.5	4.5	9.5	
t_{PHZ}	$\overline{OE}$	Any Q	3	10	3	6.5	ns
t_{PLZ}			3	8	3	7	

§ For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

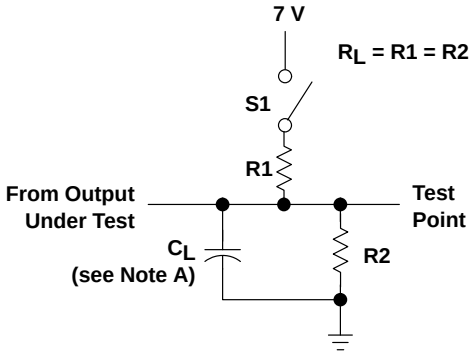
PARAMETER MEASUREMENT INFORMATION
SERIES 54ALS/74ALS AND 54AS/74AS DEVICES



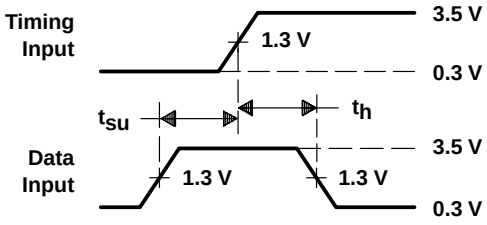
LOAD CIRCUIT FOR
BI-STATE
TOTEM-POLE OUTPUTS



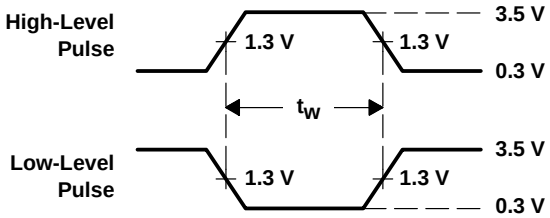
LOAD CIRCUIT
FOR OPEN-COLLECTOR OUTPUTS



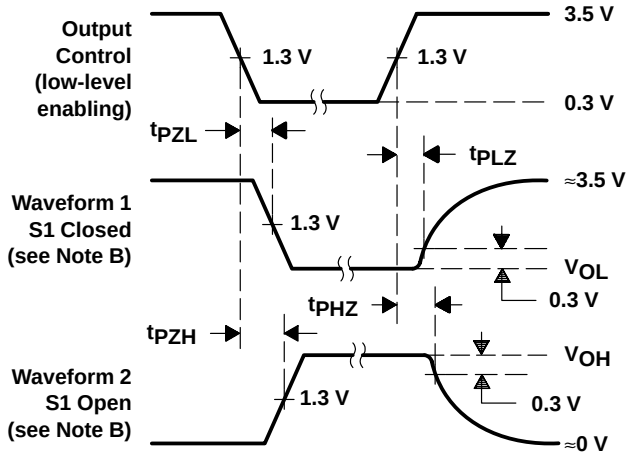
LOAD CIRCUIT
FOR 3-STATE OUTPUTS



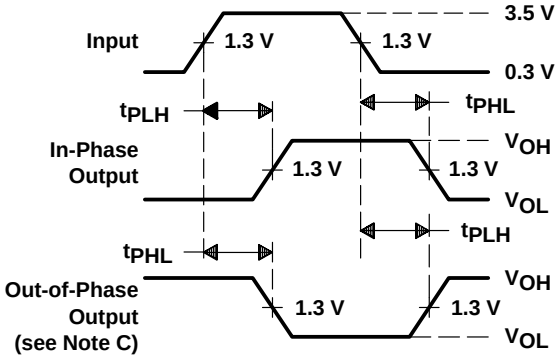
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PULSE DURATIONS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES, 3-STATE OUTPUTS



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. When measuring propagation delay items of 3-state outputs, switch S1 is open.
D. All input pulses have the following characteristics: PRR ≤ 1 MHz, $t_r = t_f = 2$ ns, duty cycle = 50%.
E. The outputs are measured one at a time with one transition per measurement.

Figure 1. Load Circuits and Voltage Waveforms

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
83020012A	Active	Production	LCCC (FK) | 20	55 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	83020012A SNJ54ALS 373AFK
8302001RA	Active	Production	CDIP (J) | 20	20 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	8302001RA SNJ54ALS373AJ
JM38510/37203B2A	Active	Production	LCCC (FK) | 20	55 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	JM38510/ 37203B2A
JM38510/37203B2A.A	Active	Production	LCCC (FK) | 20	55 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	JM38510/ 37203B2A
JM38510/37203BRA	Active	Production	CDIP (J) | 20	20 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	JM38510/ 37203BRA
JM38510/37203BRA.A	Active	Production	CDIP (J) | 20	20 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	JM38510/ 37203BRA
M38510/37203B2A	Active	Production	LCCC (FK) | 20	55 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	JM38510/ 37203B2A
M38510/37203BRA	Active	Production	CDIP (J) | 20	20 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	JM38510/ 37203BRA
SN54ALS373AJ	Active	Production	CDIP (J) | 20	20 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	SN54ALS373AJ
SN54ALS373AJ.A	Active	Production	CDIP (J) | 20	20 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	SN54ALS373AJ
SN74ALS373ADBR	Active	Production	SSOP (DB) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	G373A
SN74ALS373ADBR.A	Active	Production	SSOP (DB) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	G373A
SN74ALS373ADW	Obsolete	Production	SOIC (DW) | 20	-	-	Call TI	Call TI	0 to 70	ALS373A
SN74ALS373ADWR	Active	Production	SOIC (DW) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	ALS373A
SN74ALS373ADWR.A	Active	Production	SOIC (DW) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	ALS373A
SN74ALS373AN	Active	Production	PDIP (N) | 20	20 | TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	SN74ALS373AN
SN74ALS373AN.A	Active	Production	PDIP (N) | 20	20 | TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	SN74ALS373AN
SN74ALS373ANSR	Active	Production	SOP (NS) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	ALS373A
SN74ALS373ANSR.A	Active	Production	SOP (NS) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	ALS373A
SN74AS373N	Active	Production	PDIP (N) | 20	20 | TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	SN74AS373N
SN74AS373N.A	Active	Production	PDIP (N) | 20	20 | TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	SN74AS373N
SN74AS373NSR	Active	Production	SOP (NS) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	74AS373

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SN74AS373NSR.A	Active	Production	SOP (NS) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	74AS373
SNJ54ALS373AFK	Active	Production	LCCC (FK) | 20	55 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	83020012A SNJ54ALS 373AFK
SNJ54ALS373AFK.A	Active	Production	LCCC (FK) | 20	55 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	83020012A SNJ54ALS 373AFK
SNJ54ALS373AJ	Active	Production	CDIP (J) | 20	20 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	8302001RA SNJ54ALS373AJ
SNJ54ALS373AJ.A	Active	Production	CDIP (J) | 20	20 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	8302001RA SNJ54ALS373AJ

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF SN54ALS373A, SN74ALS373A :

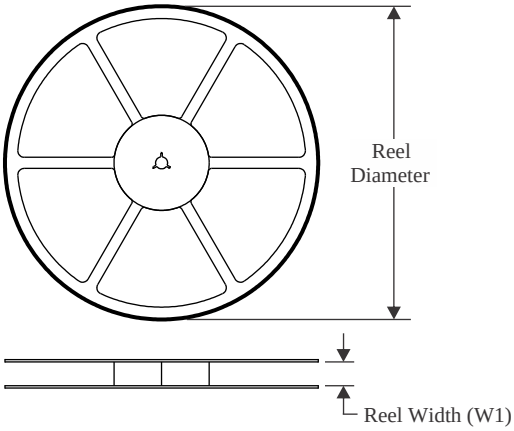
- Catalog : SN74ALS373A
- Military : SN54ALS373A

NOTE: Qualified Version Definitions:

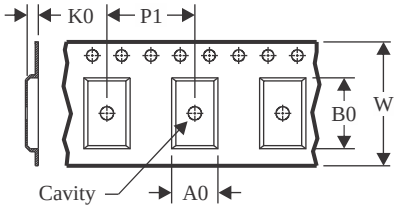
- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

TAPE AND REEL INFORMATION

REEL DIMENSIONS

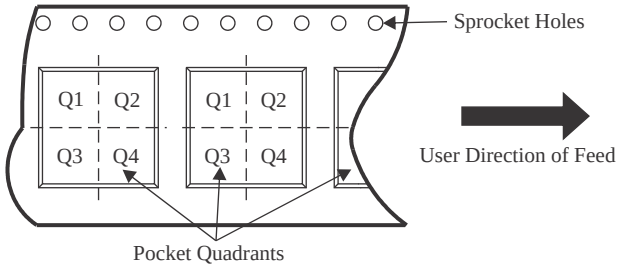


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

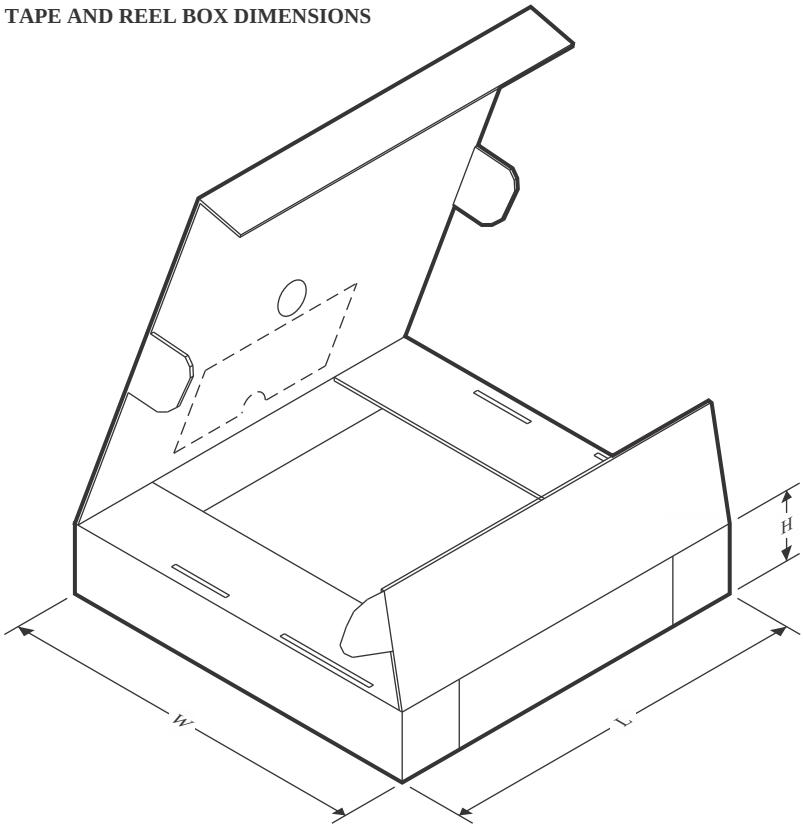
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74ALS373ADBR	SSOP	DB	20	2000	330.0	16.4	8.2	7.5	2.5	12.0	16.0	Q1
SN74ALS373ADWR	SOIC	DW	20	2000	330.0	24.4	10.8	13.3	2.7	12.0	24.0	Q1
SN74ALS373ANSR	SOP	NS	20	2000	330.0	24.4	8.4	13.0	2.5	12.0	24.0	Q1
SN74AS373NSR	SOP	NS	20	2000	330.0	24.4	8.4	13.0	2.5	12.0	24.0	Q1

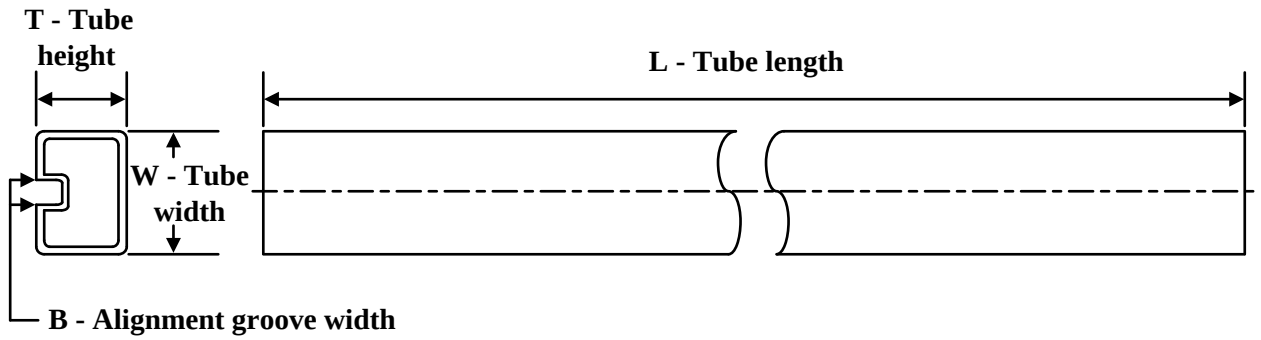
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74ALS373ADBR	SSOP	DB	20	2000	353.0	353.0	32.0
SN74ALS373ADWR	SOIC	DW	20	2000	356.0	356.0	45.0
SN74ALS373ANSR	SOP	NS	20	2000	356.0	356.0	45.0
SN74AS373NSR	SOP	NS	20	2000	356.0	356.0	45.0

TUBE



*All dimensions are nominal

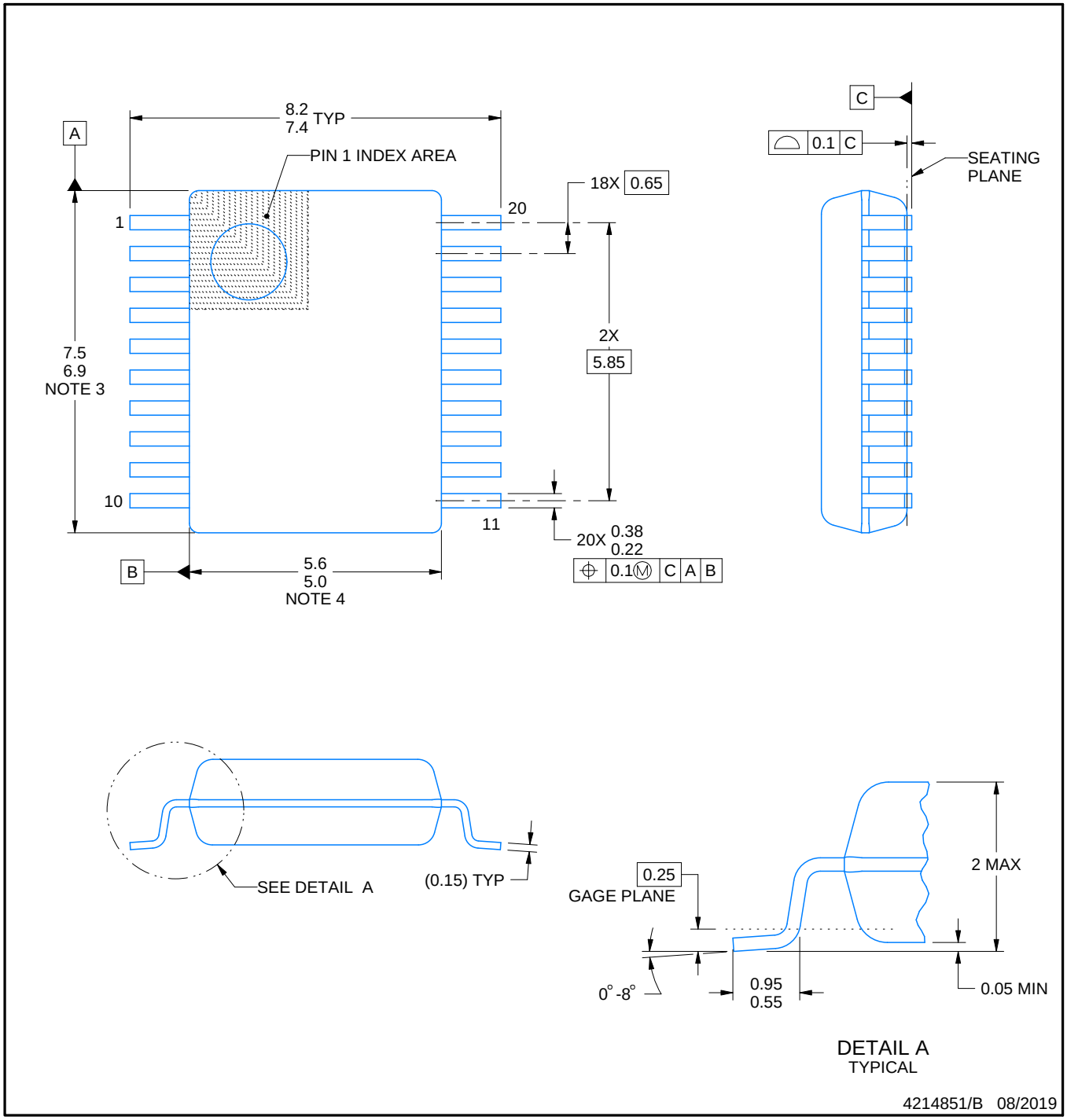
Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
83020012A	FK	LCCC	20	55	506.98	12.06	2030	NA
JM38510/37203B2A	FK	LCCC	20	55	506.98	12.06	2030	NA
JM38510/37203B2A.A	FK	LCCC	20	55	506.98	12.06	2030	NA
M38510/37203B2A	FK	LCCC	20	55	506.98	12.06	2030	NA
SN74ALS373AN	N	PDIP	20	20	506	13.97	11230	4.32
SN74ALS373AN.A	N	PDIP	20	20	506	13.97	11230	4.32
SN74AS373N	N	PDIP	20	20	506	13.97	11230	4.32
SN74AS373N.A	N	PDIP	20	20	506	13.97	11230	4.32
SNJ54ALS373AFK	FK	LCCC	20	55	506.98	12.06	2030	NA
SNJ54ALS373AFK.A	FK	LCCC	20	55	506.98	12.06	2030	NA

PACKAGE OUTLINE

DB0020A

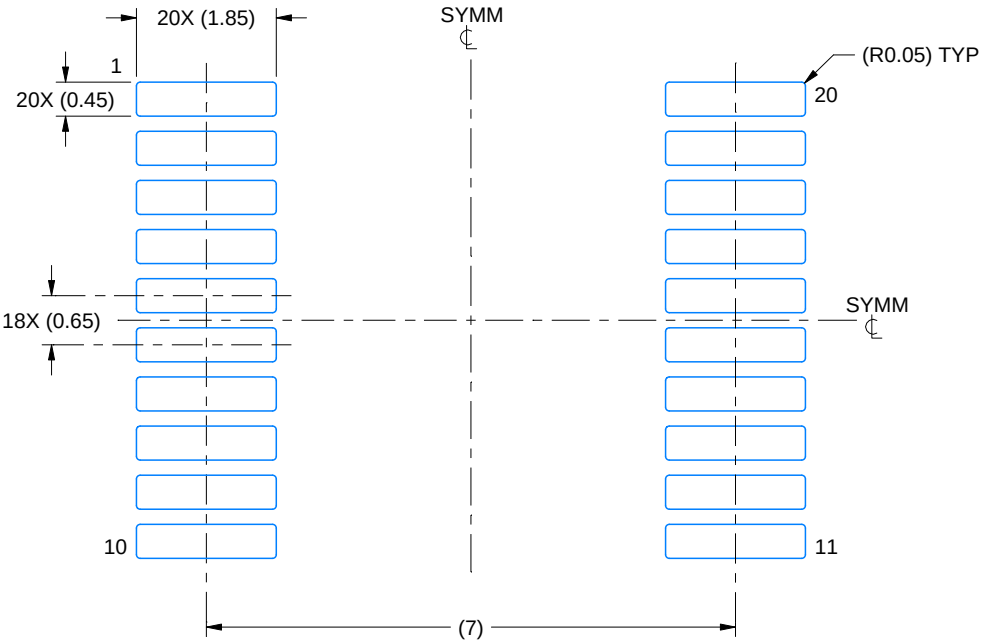
SSOP - 2 mm max height

SMALL OUTLINE PACKAGE

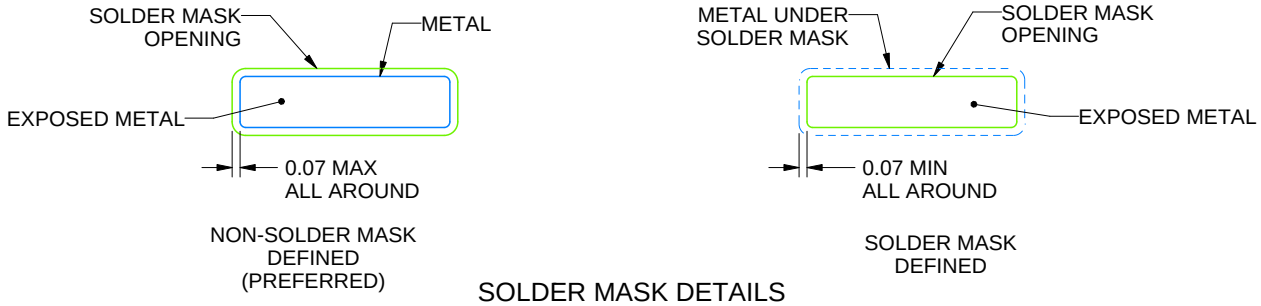


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-150.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



SOLDER MASK DETAILS

4214851/B 08/2019

NOTES: (continued)

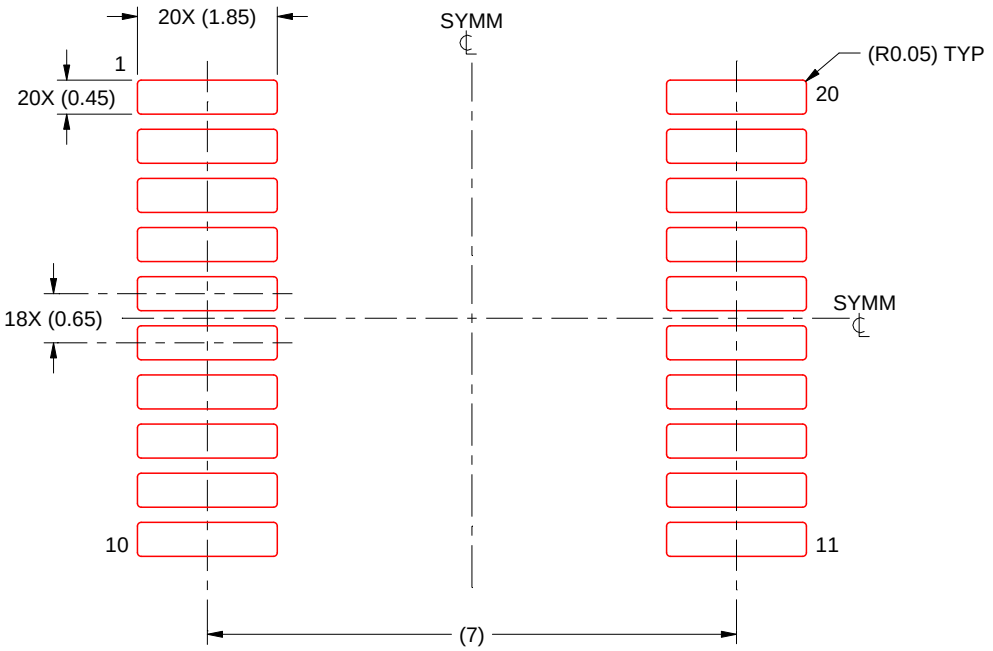
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DB0020A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4214851/B 08/2019

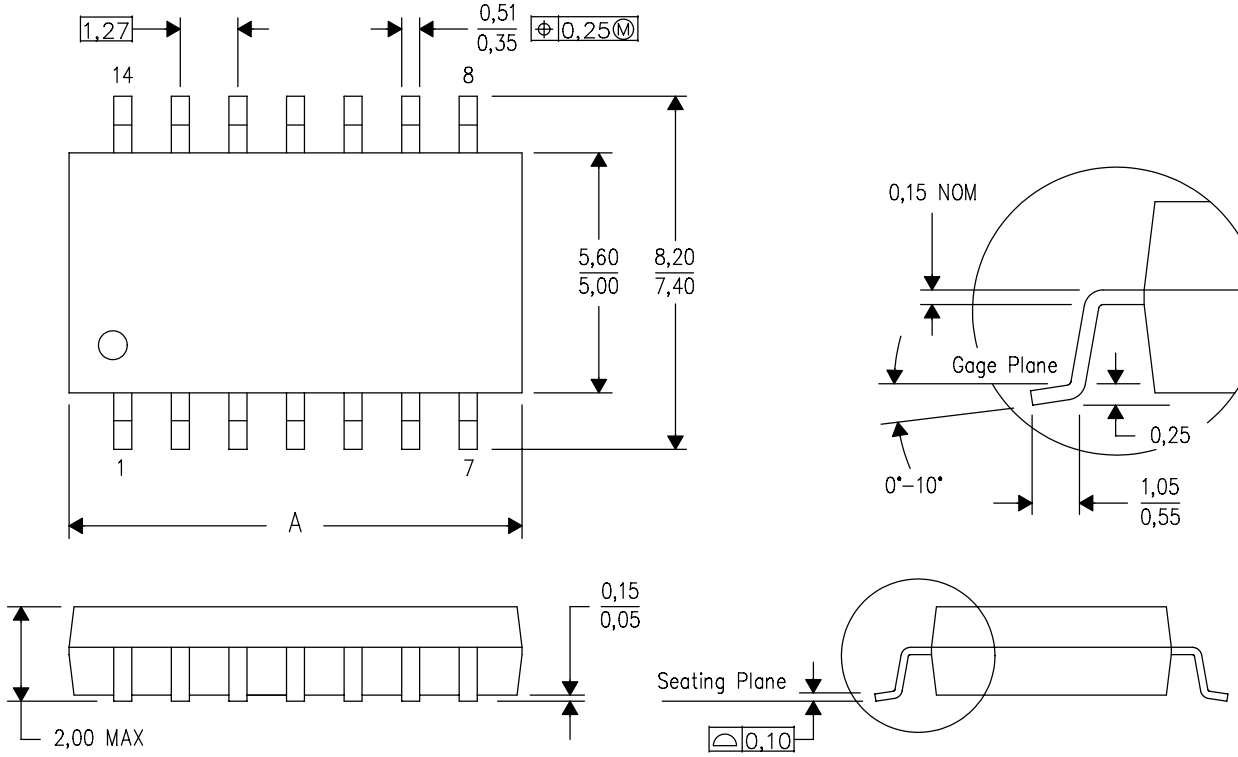
NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

MECHANICAL DATA

NS (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

14-PINS SHOWN



DIM \ PINS **	14	16	20	24
A MAX	10,50	10,50	12,90	15,30
A MIN	9,90	9,90	12,30	14,70

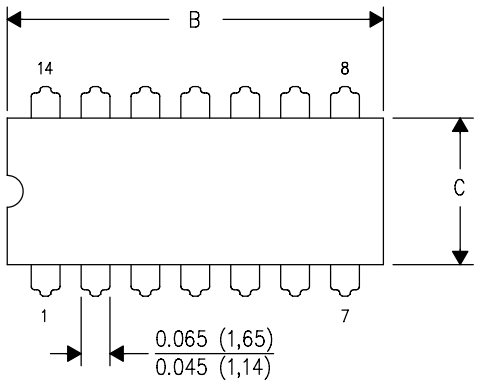
4040062/C 03/03

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

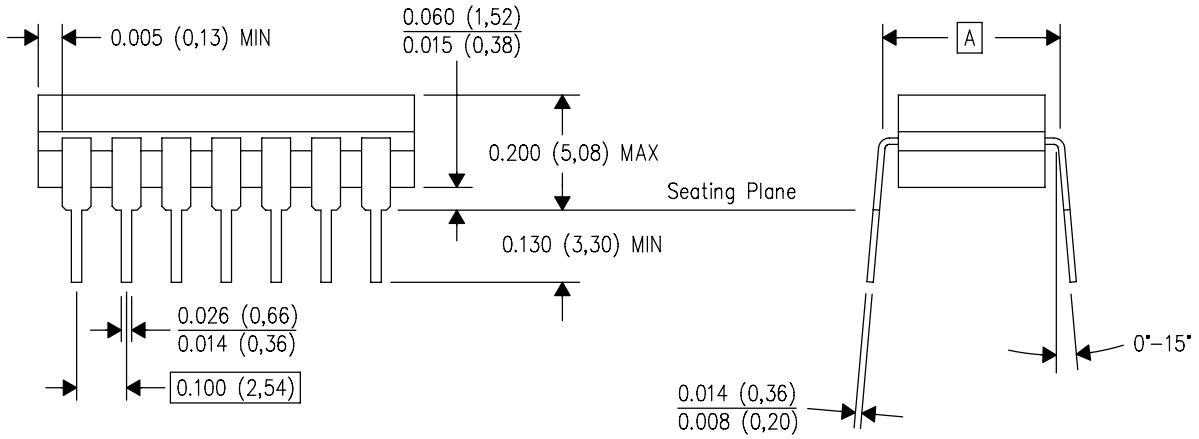
J (R–GDIP–T**)

14 LEADS SHOWN

CERAMIC DUAL IN–LINE PACKAGE



DIM \ PINS **	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)



4040083/F 03/03

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package is hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
E. Falls within MIL STD 1835 GDIP1–T14, GDIP1–T16, GDIP1–T18 and GDIP1–T20.

GENERIC PACKAGE VIEW

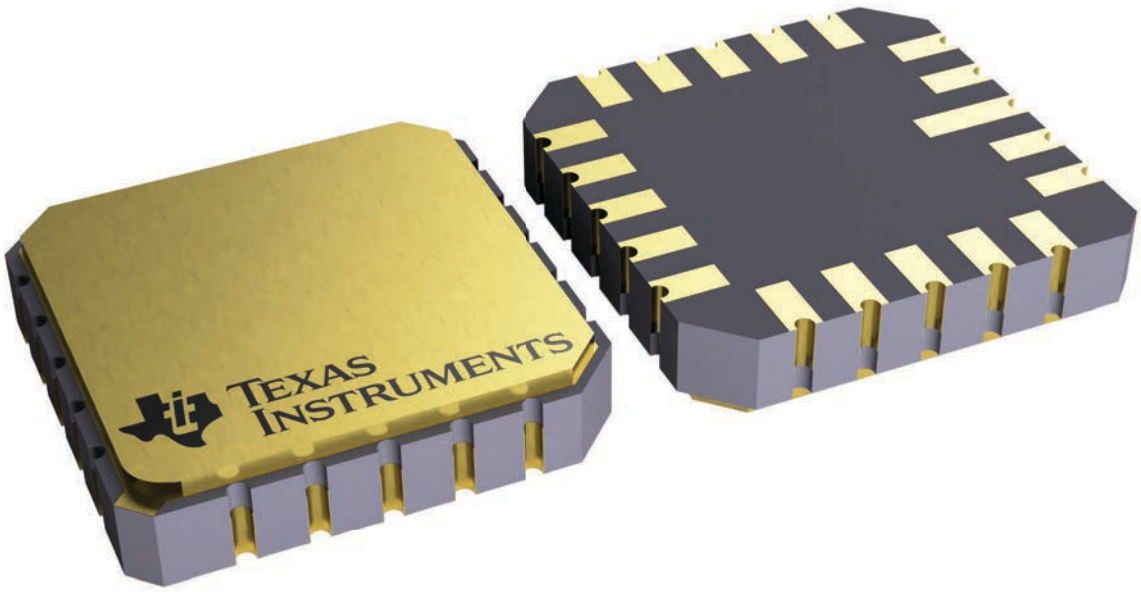
FK 20

LCCC - 2.03 mm max height

8.89 x 8.89, 1.27 mm pitch

LEADLESS CERAMIC CHIP CARRIER

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

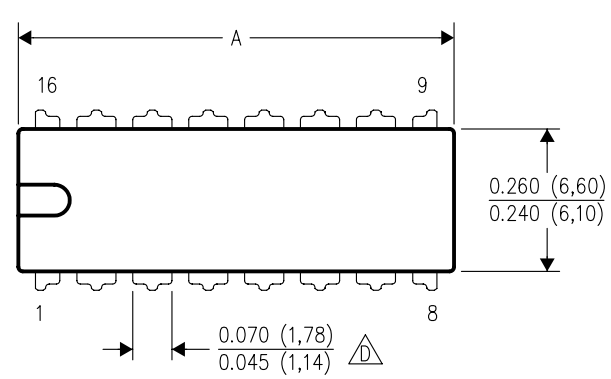


4229370VA\

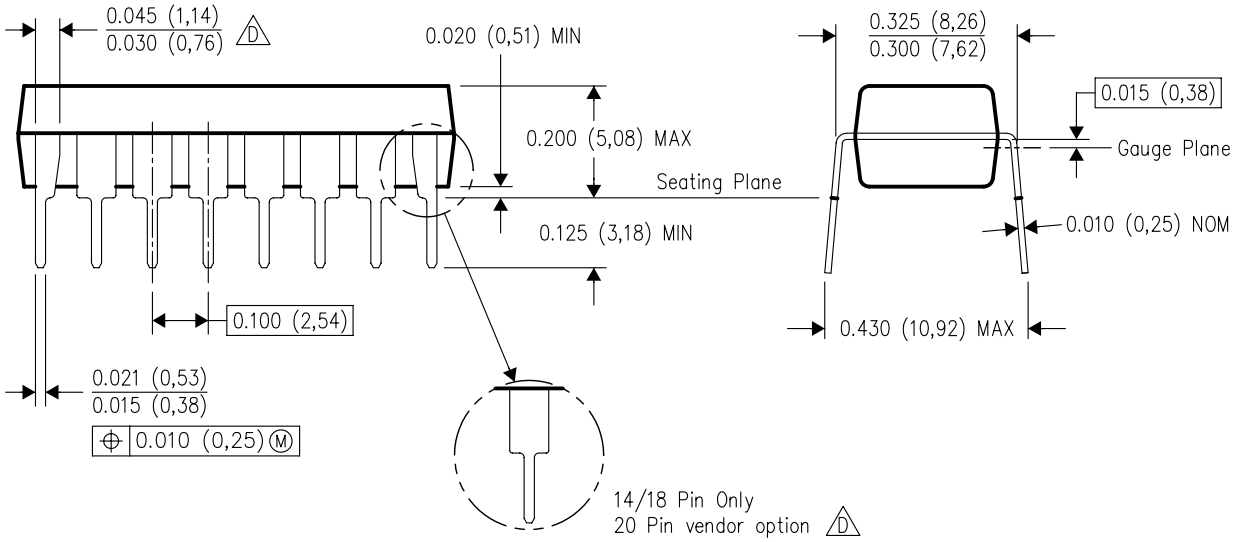
N (R–PDIP–T**)

PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN

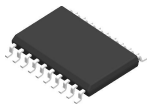


DIM \ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS–001 VARIATION (C)	AA	BB	AC	AD



4040049/E 12/2002

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

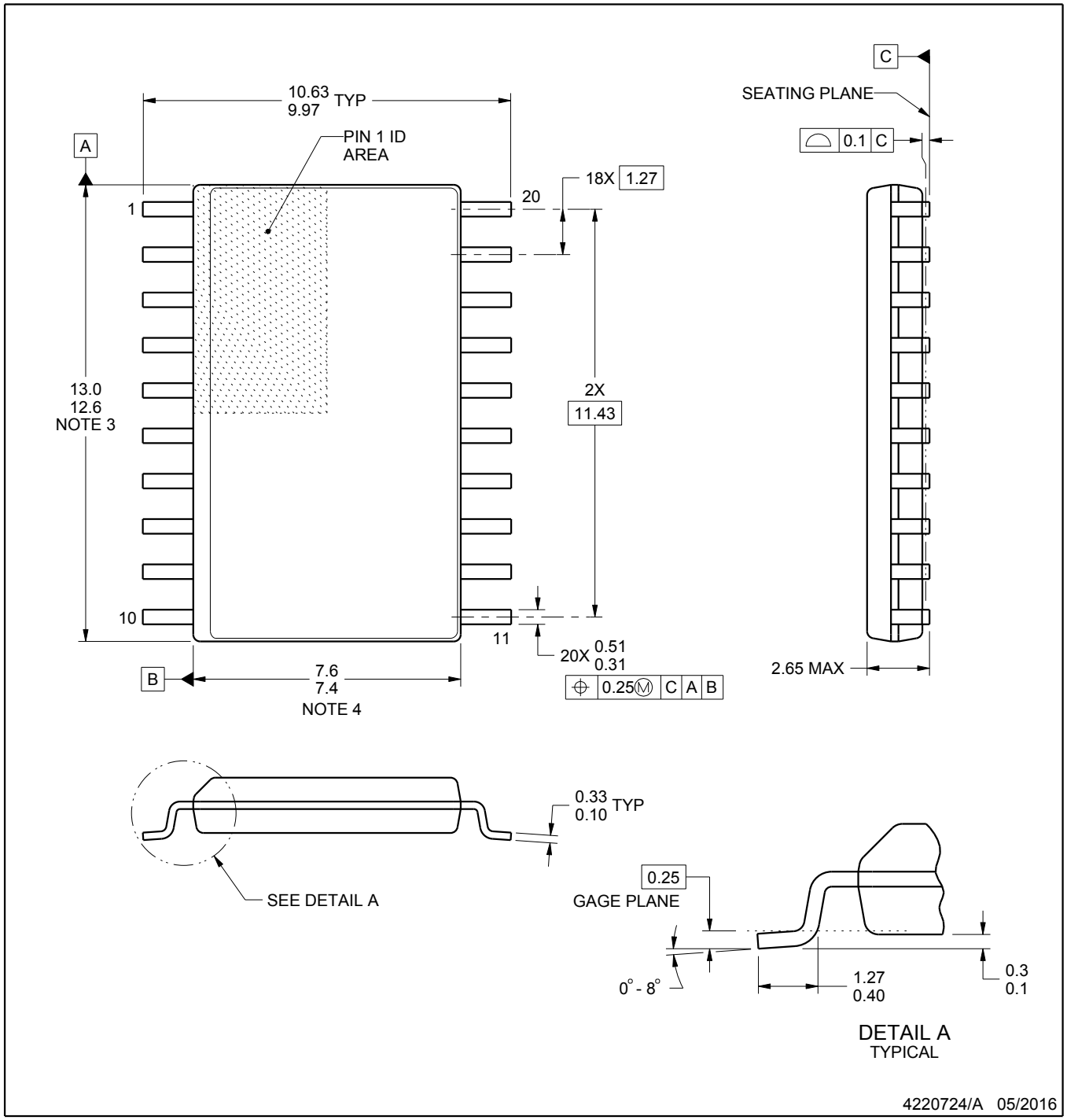


PACKAGE OUTLINE

DW0020A

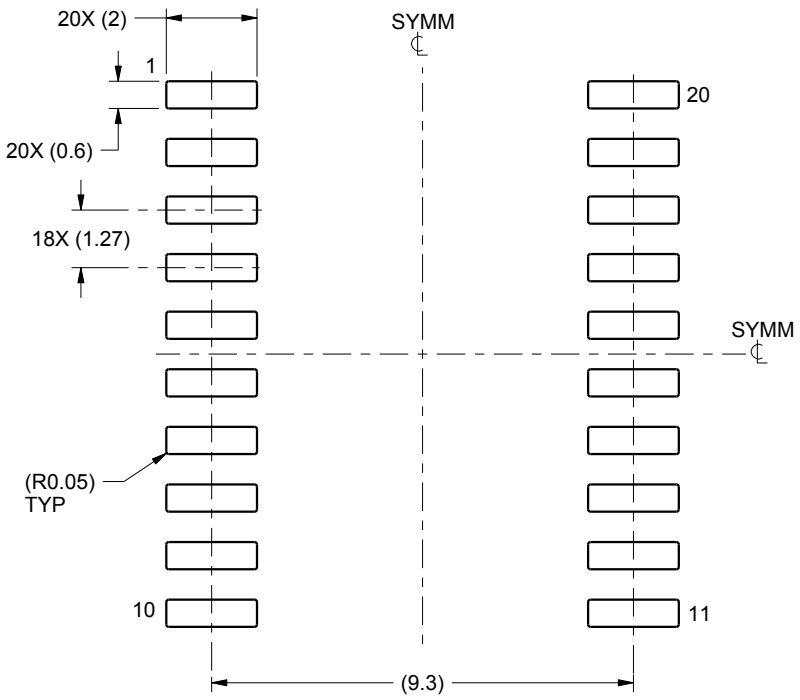
SOIC - 2.65 mm max height

SOIC

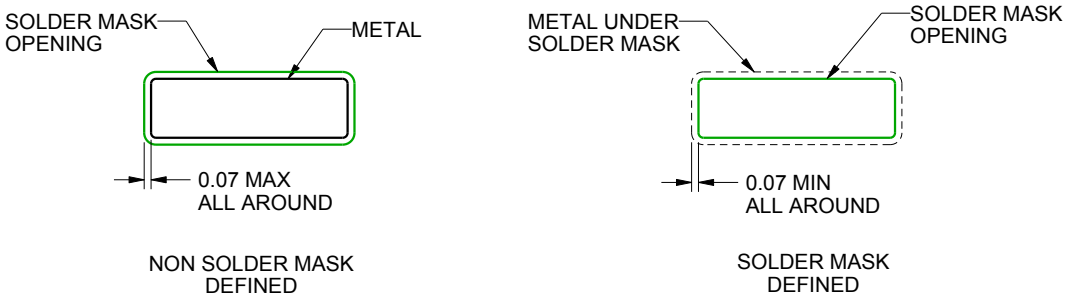


NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm per side.
5. Reference JEDEC registration MS-013.



LAND PATTERN EXAMPLE
SCALE:6X

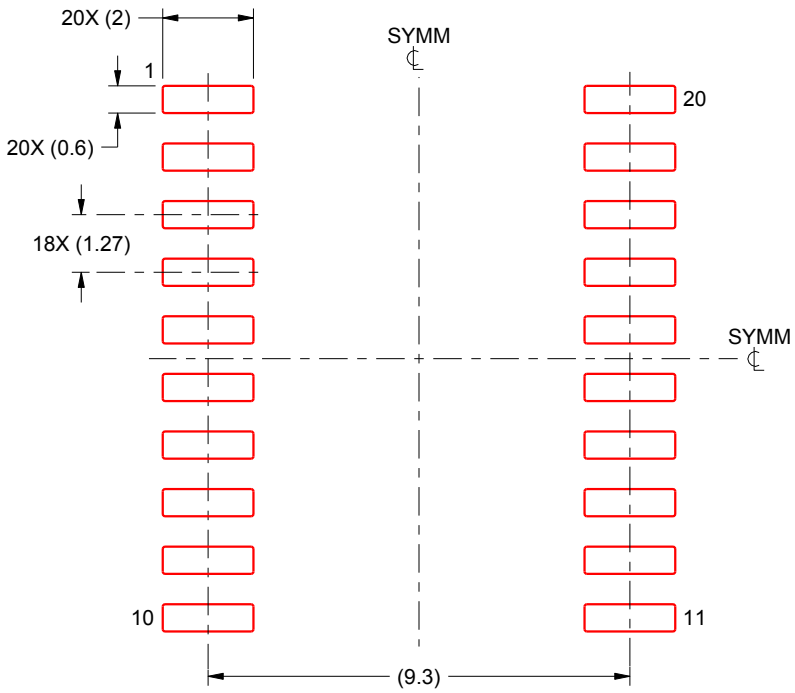


SOLDER MASK DETAILS

4220724/A 05/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

4220724/A 05/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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