

SN54ALS374A, SN54AS374, SN74ALS374A, SN74AS374 OCTAL D-TYPE EDGE-TRIGGERED FLIP-FLOPS WITH 3-STATE OUTPUTS

SDAS167C – APRIL 1982 – REVISED NOVEMBER 1999

- D-Type Flip-Flops in a Single Package With 3-State Bus Driving True Outputs
- Full Parallel Access for Loading
- Buffered Control Inputs
- Package Options Include Plastic Small-Outline (DW) Packages, Ceramic Chip Carriers (FK), and Standard Plastic (N) and Ceramic (J) DIPs

description

These octal D-type edge-triggered flip-flops feature 3-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. They are particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

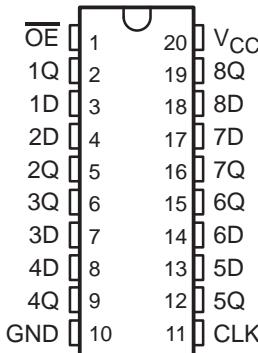
On the positive transition of the clock (CLK) input, the Q outputs are set to the logic levels set up at the data (D) inputs.

A buffered output-enable (\overline{OE}) input places the eight outputs in either a normal logic state (high or low logic levels) or the high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and the increased drive provide the capability to drive bus lines without interface or pullup components.

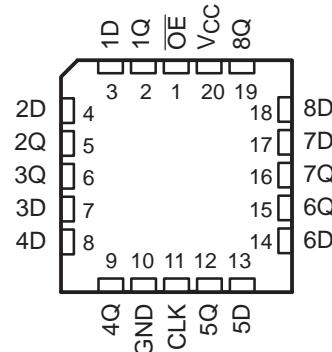
\overline{OE} does not affect internal operations of the flip-flops. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

The SN54ALS374A and SN54AS374 are characterized for operation over the full military temperature range of -55°C to 125°C . The SN74ALS374A and SN74AS374 are characterized for operation from 0°C to 70°C .

SN54ALS374A, SN54AS374 . . . J PACKAGE
SN74ALS374A, SN74AS374 . . . DW OR N PACKAGE
(TOP VIEW)



SN54ALS374A, SN54AS374 . . . FK PACKAGE
(TOP VIEW)



FUNCTION TABLE
(each flip-flop)

INPUTS			OUTPUT
\overline{OE}	CLK	D	Q
L	↑	H	H
L	↑	L	L
L	H or L	X	Q ₀
H	X	X	Z



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

**TEXAS
INSTRUMENTS**

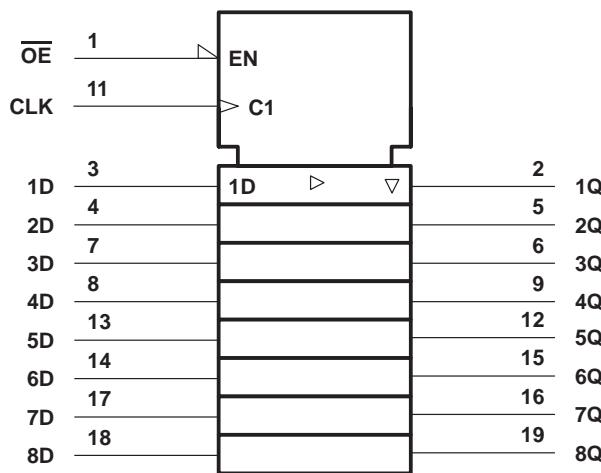
POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

Copyright © 1999, Texas Instruments Incorporated
On products compliant to MIL-PRF-38535, all parameters are tested unless otherwise noted. On all other products, production processing does not necessarily include testing of all parameters.

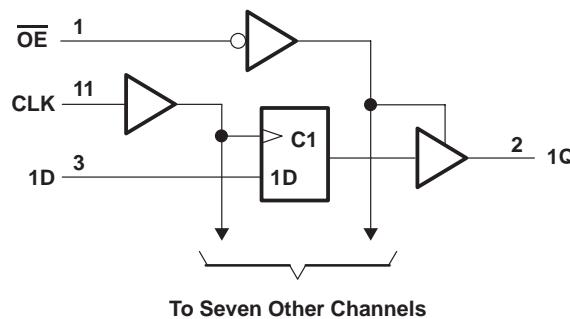
**SN54ALS374A, SN54AS374, SN74ALS374A, SN74AS374
OCTAL D-TYPE EDGE-TRIGGERED FLIP-FLOPS
WITH 3-STATE OUTPUTS**

SDAS167C – APRIL 1982 – REVISED NOVEMBER 1999

logic symbol[†]



logic diagram (positive logic)



[†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[‡]

Supply voltage range, V_{CC}	-0.5 V to 7 V
Input voltage range, V_I	-0.5 V to 7 V
Voltage applied to a disabled 3-state output	-0.5 V to 5.5 V
Package thermal impedance, θ_{JA} (see Note 1): DW package	58°C/W
N package	69°C/W
Storage temperature range, T_{stg}	-65°C to 150°C

[‡] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The package thermal impedance is calculated in accordance with JESD 51.

recommended operating conditions

		SN54ALS374A			SN74ALS374A			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.7			0.8	V
I_{OH}	High-level output current			-1			-2.6	mA
I_{OL}	Low-level output current			12			24	mA
T_A	Operating free-air temperature	-55		125	0		70	°C

**SN54ALS374A, SN54AS374, SN74ALS374A, SN74AS374
OCTAL D-TYPE EDGE-TRIGGERED FLIP-FLOPS
WITH 3-STATE OUTPUTS**

SDAS167C – APRIL 1982 – REVISED NOVEMBER 1999

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	SN54ALS374A			SN74ALS374A			UNIT
		MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}	$V_{CC} = 4.5 \text{ V}$, $I_I = -18 \text{ mA}$			-1.5			-1.5	V
V_{OH}	$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$, $I_{OH} = -0.4 \text{ mA}$	$V_{CC}-2$			$V_{CC}-2$			V
	$V_{CC} = 4.5 \text{ V}$	$I_{OH} = -1 \text{ mA}$	2.4	3.3			2.4	3.2
V_{OL}	$V_{CC} = 4.5 \text{ V}$	$I_{OL} = 12 \text{ mA}$	0.25	0.4	0.25	0.4		V
		$I_{OL} = 24 \text{ mA}$			0.35	0.5		
I_{OZH}	$V_{CC} = 5.5 \text{ V}$, $V_O = 2.7 \text{ V}$			20			20	μA
I_{OZL}	$V_{CC} = 5.5 \text{ V}$, $V_O = 0.4 \text{ V}$			-20			-20	μA
I_I	$V_{CC} = 5.5 \text{ V}$, $V_I = 7 \text{ V}$			0.1			0.1	mA
I_{IH}	$V_{CC} = 5.5 \text{ V}$, $V_I = 2.7 \text{ V}$			20			20	μA
I_{IL}	$V_{CC} = 5.5 \text{ V}$, $V_I = 0.4 \text{ V}$			-0.2			-0.2	mA
I_O^{\ddagger}	$V_{CC} = 5.5 \text{ V}$, $V_O = 2.25 \text{ V}$	-20	-112	-30	-112			mA
I_{CC}	$V_{CC} = 5.5 \text{ V}$	Outputs high	11	20	11	19		mA
		Outputs low	19	28	19	28		
		Outputs disabled	20	31	20	31		

† All typical values are at $V_{CC} = 5 \text{ V}$, $T_A = 25^\circ\text{C}$.

‡ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS} .

timing requirements over recommended operating free-air temperature range (unless otherwise noted)

		SN54ALS374A		SN74ALS374A		UNIT
		MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency		30		35	MHz
t_w	Pulse duration	CLK high or low	16.5	14		ns
t_{su}	Setup time	Data before $CLK\uparrow$	10	10		ns
t_h	Hold time	Data after $CLK\uparrow$	4	0		ns

**switching characteristics over recommended operating conditions (unless otherwise noted
(see Figure 3))**

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN54ALS374A		SN74ALS374A		UNIT
			MIN	MAX	MIN	MAX	
t_{max}			30		35		MHz
t_{PLH}	CLK	Q	3	14	3	12	ns
t_{PHL}			5	17	5	16	
t_{PZH}	\overline{OE}	Q	3	18	3	17	ns
t_{PZL}			5	21	5	18	
t_{PHZ}	\overline{OE}	Q	1	11	1	10	ns
t_{PLZ}			2	19	2	18	

**SN54ALS374A, SN54AS374, SN74ALS374A, SN74AS374
OCTAL D-TYPE EDGE-TRIGGERED FLIP-FLOPS
WITH 3-STATE OUTPUTS**

SDAS167C – APRIL 1982 – REVISED NOVEMBER 1999

recommended operating conditions

		SN54AS374			SN74AS374			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V _{CC}	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V _{IH}	High-level input voltage	2			2			V
V _{IL}	Low-level input voltage			0.7			0.8	V
I _{OH}	High-level output current			-12			-15	mA
I _{OL}	Low-level output current			32			48	mA
T _A	Operating free-air temperature	-55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	SN54AS374			SN74AS374			UNIT
		MIN	TYP†	MAX	MIN	TYP†	MAX	
V _{IK}	V _{CC} = 4.5 V, I _I = -18 mA		-1.2			-1.2		V
V _{OH}	V _{CC} = 4.5 V to 5.5 V, I _{OH} = -2 mA	V _{CC} -2			V _{CC} -2			V
	V _{CC} = 4.5 V	I _{OH} = -12 mA	2.4	3.2			2.4	
V _{OL}	V _{CC} = 4.5 V	I _{OL} = 32 mA	0.29	0.5				V
		I _{OL} = 48 mA					0.34	
I _{OZH}	V _{CC} = 5.5 V, V _O = 2.7 V		50			50		µA
I _{OZL}	V _{CC} = 5.5 V, V _O = 0.4 V		-50			-50		µA
I _I	V _{CC} = 5.5 V, V _I = 7 V		0.1			0.1		mA
I _{IH}	V _{CC} = 5.5 V, V _I = 2.7 V		20			20		µA
I _{IL}	OE, CLK Data	V _{CC} = 5.5 V, V _I = 0.4 V	-0.5			-0.5		mA
			-3			-2		
I _O ‡	V _{CC} = 5.5 V, V _O = 2.25 V	-30	-112		-30	-112		mA
I _{CC}	V _{CC} = 5.5 V	Outputs high	77	120		77	120	mA
		Outputs low	84	128		84	128	
		Outputs disabled	84	128		84	128	

† All typical values are at V_{CC} = 5 V, T_A = 25°C.

‡ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

timing requirements over recommended operating free-air temperature range (unless otherwise noted)

		SN54AS374		SN74AS374		UNIT
		MIN	MAX	MIN	MAX	
f _{clock}	Clock frequency		100*		125	MHz
t _w	Pulse duration	CLK high	5.5*		4	ns
		CLK low	3*		3	
t _{su}	Setup time	Data before CLK↑	3*		2	ns
t _h	Hold time	Data after CLK↑	3*		2	ns

* On products compliant to MIL-PRF-38535, this parameter is not production tested.

SN54ALS374A, SN54AS374, SN74ALS374A, SN74AS374
OCTAL D-TYPE EDGE-TRIGGERED FLIP-FLOPS
WITH 3-STATE OUTPUTS

SDAS167C – APRIL 1982 – REVISED NOVEMBER 1999

**switching characteristics over recommended operating conditions (unless otherwise noted)
(see Figure 3)**

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN54AS374		SN74AS374		UNIT
			MIN	MAX	MIN	MAX	
f_{max}			100*		125		MHz
t_{PLH}	CLK	Q	3	11	3	8	ns
t_{PHL}			4	11.5	4	9	
t_{PZH}	\overline{OE}	Q	2	7	2	6	ns
t_{PZL}			3	11	3	10	
t_{PHZ}	\overline{OE}	Q	2	10	2	6	ns
t_{PLZ}			2	7	2	6	

* On products compliant to MIL-PRF-38535, this parameter is not production tested.

**SN54ALS374A, SN54AS374, SN74ALS374A, SN74AS374
OCTAL D-TYPE EDGE-TRIGGERED FLIP-FLOPS
WITH 3-STATE OUTPUTS**

SDAS167C – APRIL 1982 – REVISED NOVEMBER 1999

APPLICATION INFORMATION

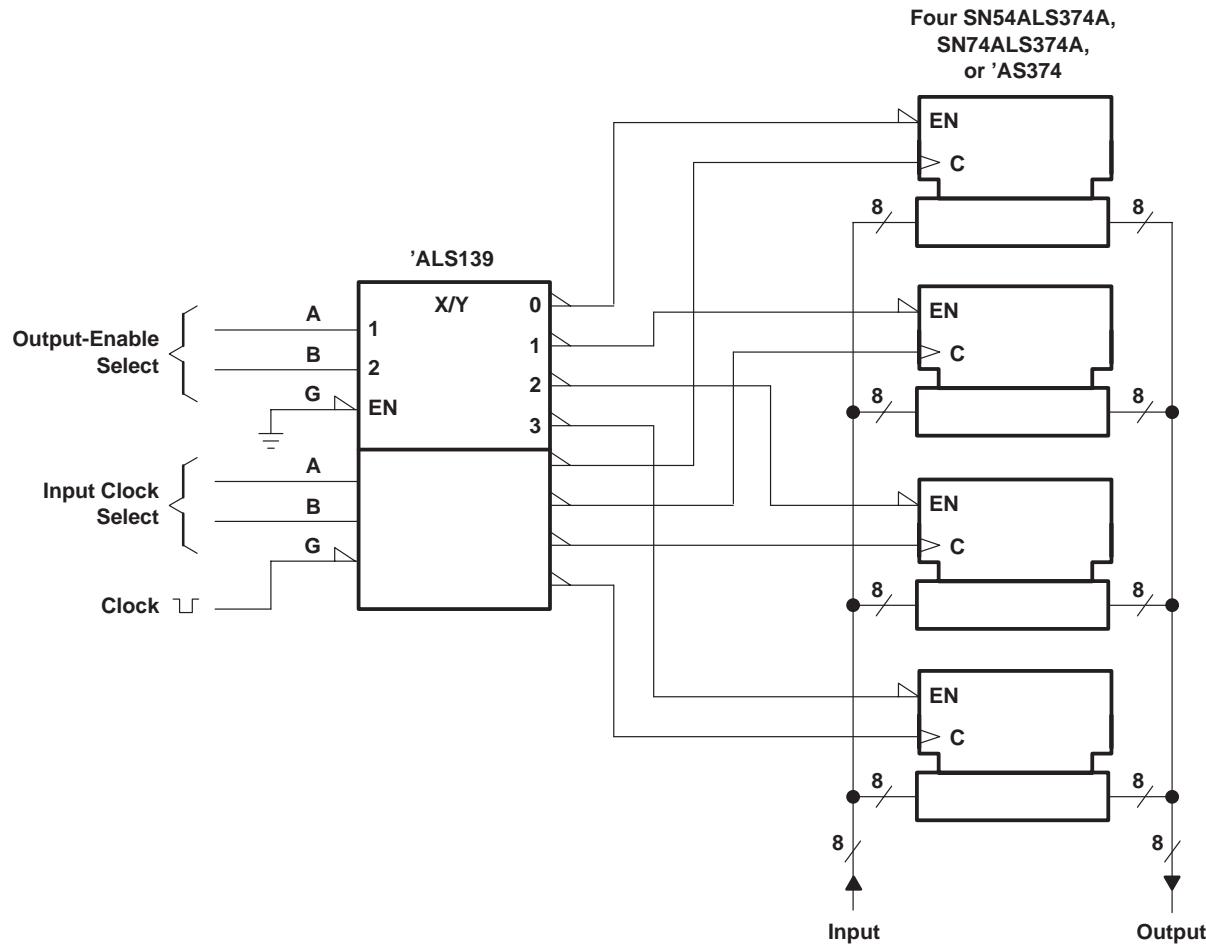


Figure 1. Expandable 4-Word by 8-Bit General File Register

APPLICATION INFORMATION

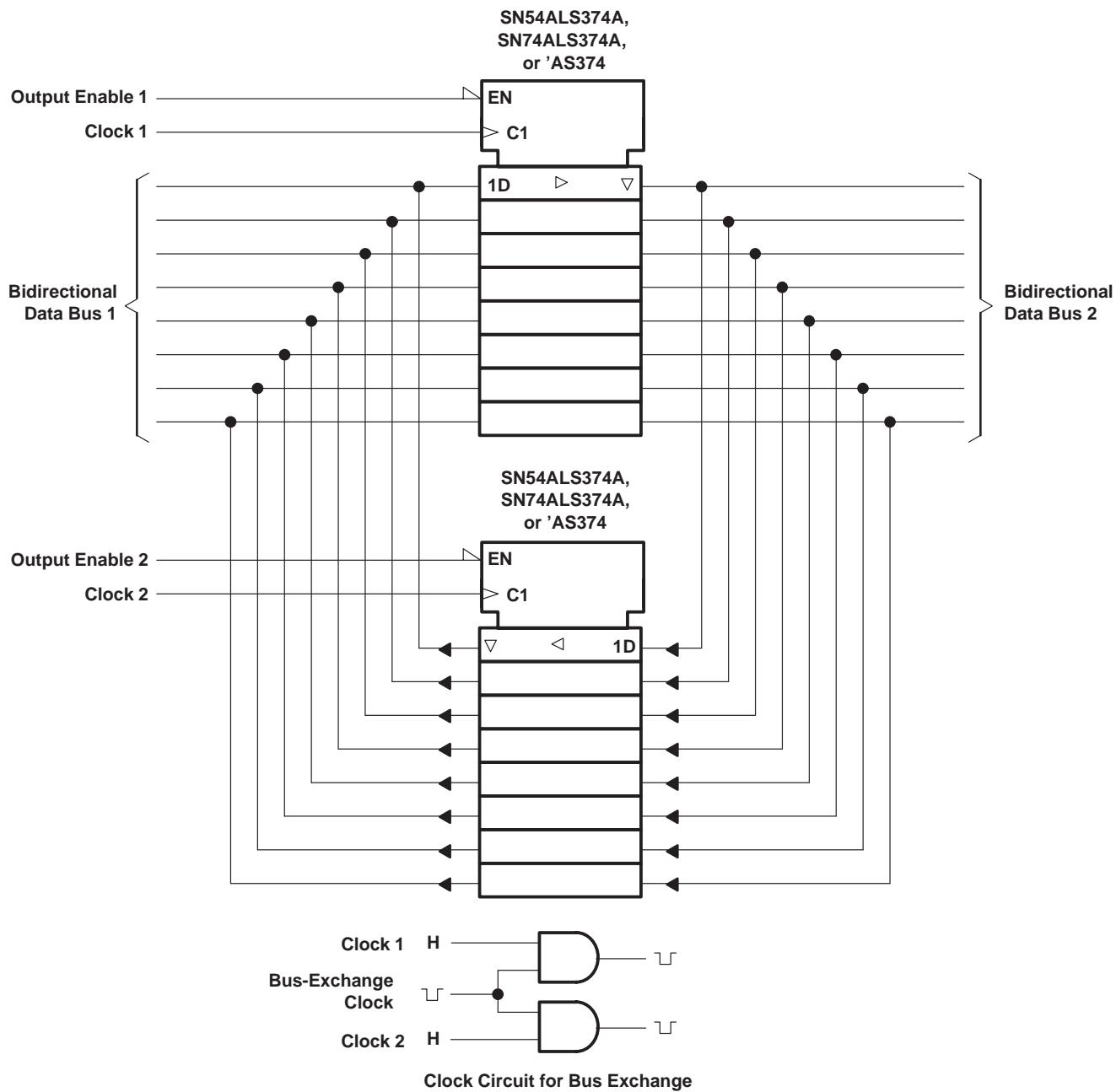
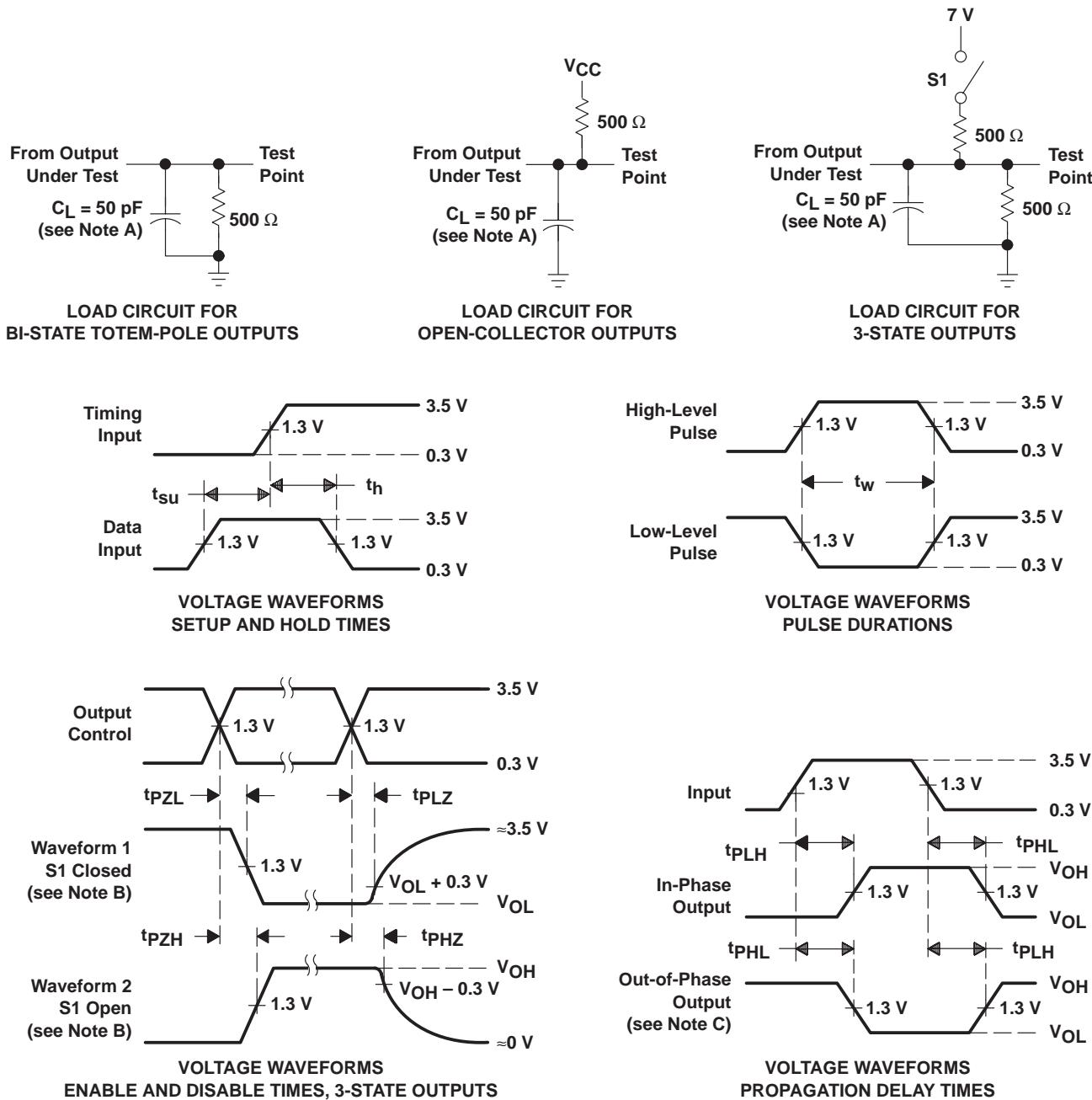


Figure 2. Bidirectional Bus Driver

**SN54ALS374A, SN54AS374, SN74ALS374A, SN74AS374
OCTAL D-TYPE EDGE-TRIGGERED FLIP-FLOPS
WITH 3-STATE OUTPUTS**

SDAS167C – APRIL 1982 – REVISED NOVEMBER 1999

**PARAMETER MEASUREMENT INFORMATION
SERIES 54ALS/74ALS AND 54AS/74AS DEVICES**



NOTES: A. C_L includes probe and jig capacitance.
 B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 C. When measuring propagation delay items of 3-state outputs, switch S1 is open.
 D. All input pulses have the following characteristics: PRR ≤ 1 MHz, $t_f = t_r = 2$ ns, duty cycle = 50%.
 E. The outputs are measured one at a time with one transition per measurement.

Figure 3. Load Circuits and Voltage Waveforms

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
5962-9756201QRA	Active	Production	CDIP (J) 20	20 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9756201QR A SNJ54ALS374J
83020022A	Active	Production	LCCC (FK) 20	55 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	83020022A SNJ54ALS 374AFK
8302002RA	Active	Production	CDIP (J) 20	20 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	8302002RA SNJ54ALS374AJ
8302002SA	Active	Production	CFP (W) 20	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	8302002SA SNJ54ALS374AW
JM38510/37204B2A	Active	Production	LCCC (FK) 20	55 TUBE	No	SNPB	N/A for Pkg Type	-	JM38510/ 37204B2A
JM38510/37204B2A.A	Active	Production	LCCC (FK) 20	55 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	JM38510/ 37204B2A
JM38510/37204BRA	Active	Production	CDIP (J) 20	20 TUBE	No	SNPB	N/A for Pkg Type	-	JM38510/ 37204BRA
JM38510/37204BRA.A	Active	Production	CDIP (J) 20	20 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	JM38510/ 37204BRA
M38510/37204B2A	Active	Production	LCCC (FK) 20	55 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	JM38510/ 37204B2A
M38510/37204BRA	Active	Production	CDIP (J) 20	20 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	JM38510/ 37204BRA
SN54ALS374AJ	Active	Production	CDIP (J) 20	20 TUBE	No	SNPB	N/A for Pkg Type	-	SN54ALS374AJ
SN54ALS374AJ.A	Active	Production	CDIP (J) 20	20 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	SN54ALS374AJ
SN54AS374J	Active	Production	CDIP (J) 20	20 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	SN54AS374J
SN54AS374J.A	Active	Production	CDIP (J) 20	20 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	SN54AS374J
SN74ALS374ADW	Obsolete	Production	SOIC (DW) 20	-	-	Call TI	Call TI	0 to 70	ALS374A
SN74ALS374ADWR	Active	Production	SOIC (DW) 20	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	ALS374A
SN74ALS374ADWR.A	Active	Production	SOIC (DW) 20	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	ALS374A
SN74ALS374AN	Active	Production	PDIP (N) 20	20 TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	SN74ALS374AN
SN74ALS374AN.A	Active	Production	PDIP (N) 20	20 TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	SN74ALS374AN
SN74ALS374ANSR	Active	Production	SOP (NS) 20	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	ALS374A

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SN74ALS374ANSR.A	Active	Production	SOP (NS) 20	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	ALS374A
SN74AS374N	Active	Production	PDIP (N) 20	20 TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	SN74AS374N
SN74AS374N.A	Active	Production	PDIP (N) 20	20 TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	SN74AS374N
SNJ54ALS374AFK	Active	Production	LCCC (FK) 20	55 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	83020022A SNJ54ALS 374AFK
SNJ54ALS374AFK.A	Active	Production	LCCC (FK) 20	55 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	83020022A SNJ54ALS 374AFK
SNJ54ALS374AJ	Active	Production	CDIP (J) 20	20 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	8302002RA SNJ54ALS374AJ
SNJ54ALS374AJ.A	Active	Production	CDIP (J) 20	20 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	8302002RA SNJ54ALS374AJ
SNJ54ALS374AW	Active	Production	CFP (W) 20	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	8302002SA SNJ54ALS374AW
SNJ54ALS374AW.A	Active	Production	CFP (W) 20	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	8302002SA SNJ54ALS374AW
SNJ54AS374J	Active	Production	CDIP (J) 20	20 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9756201QR A SNJ54AS374J
SNJ54AS374J.A	Active	Production	CDIP (J) 20	20 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9756201QR A SNJ54AS374J

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

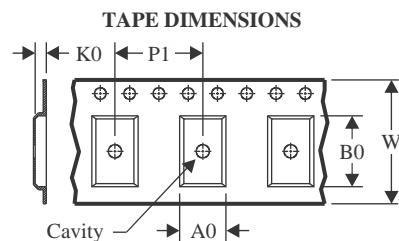
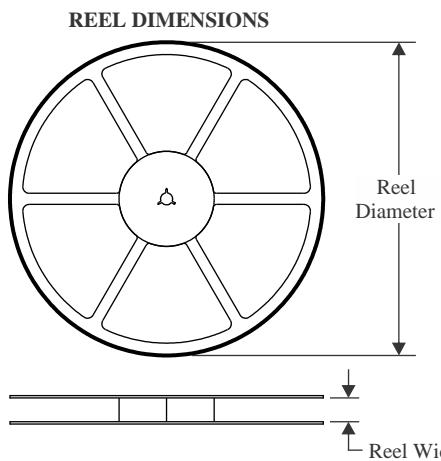
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF SN54ALS374A, SN54AS374, SN74ALS374A, SN74AS374 :

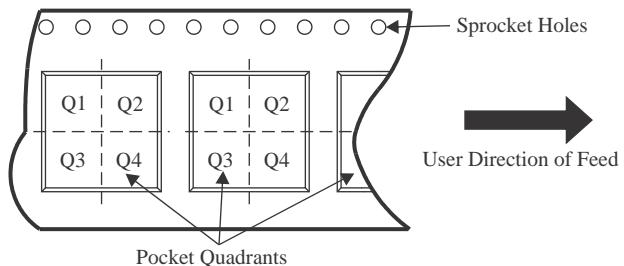
- Catalog : [SN74ALS374A](#), [SN74AS374](#)
- Military : [SN54ALS374A](#), [SN54AS374](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

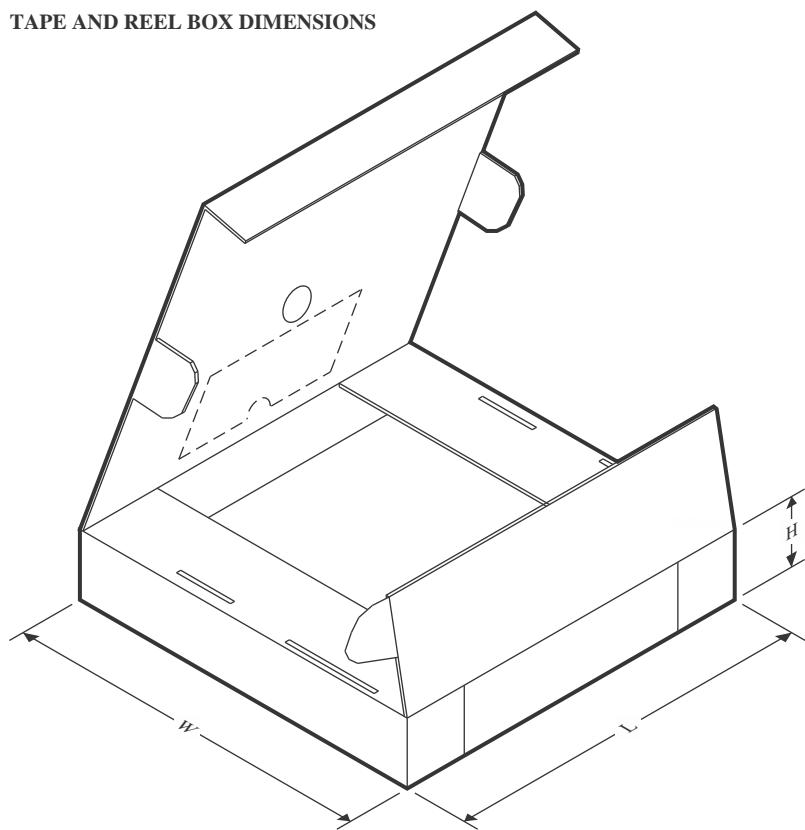
TAPE AND REEL INFORMATION


A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


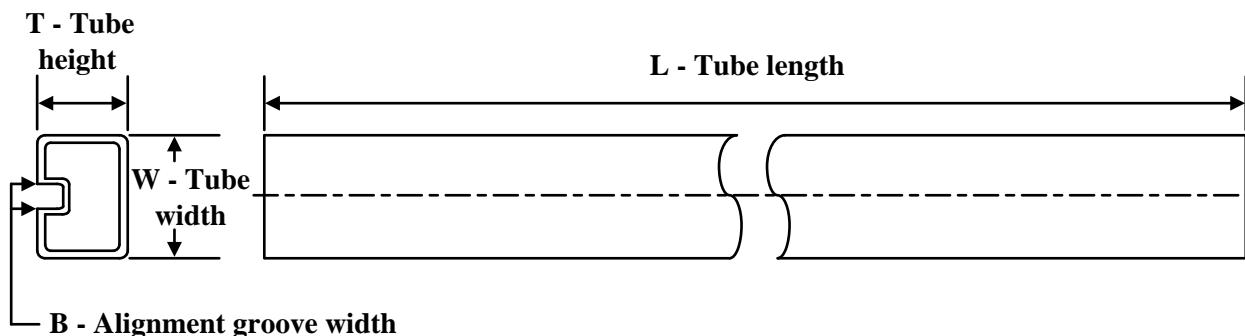
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74ALS374ADWR	SOIC	DW	20	2000	330.0	24.4	10.8	13.3	2.7	12.0	24.0	Q1
SN74ALS374ANSR	SOP	NS	20	2000	330.0	24.4	8.4	13.0	2.5	12.0	24.0	Q1

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74ALS374ADWR	SOIC	DW	20	2000	356.0	356.0	45.0
SN74ALS374ANSR	SOP	NS	20	2000	356.0	356.0	45.0

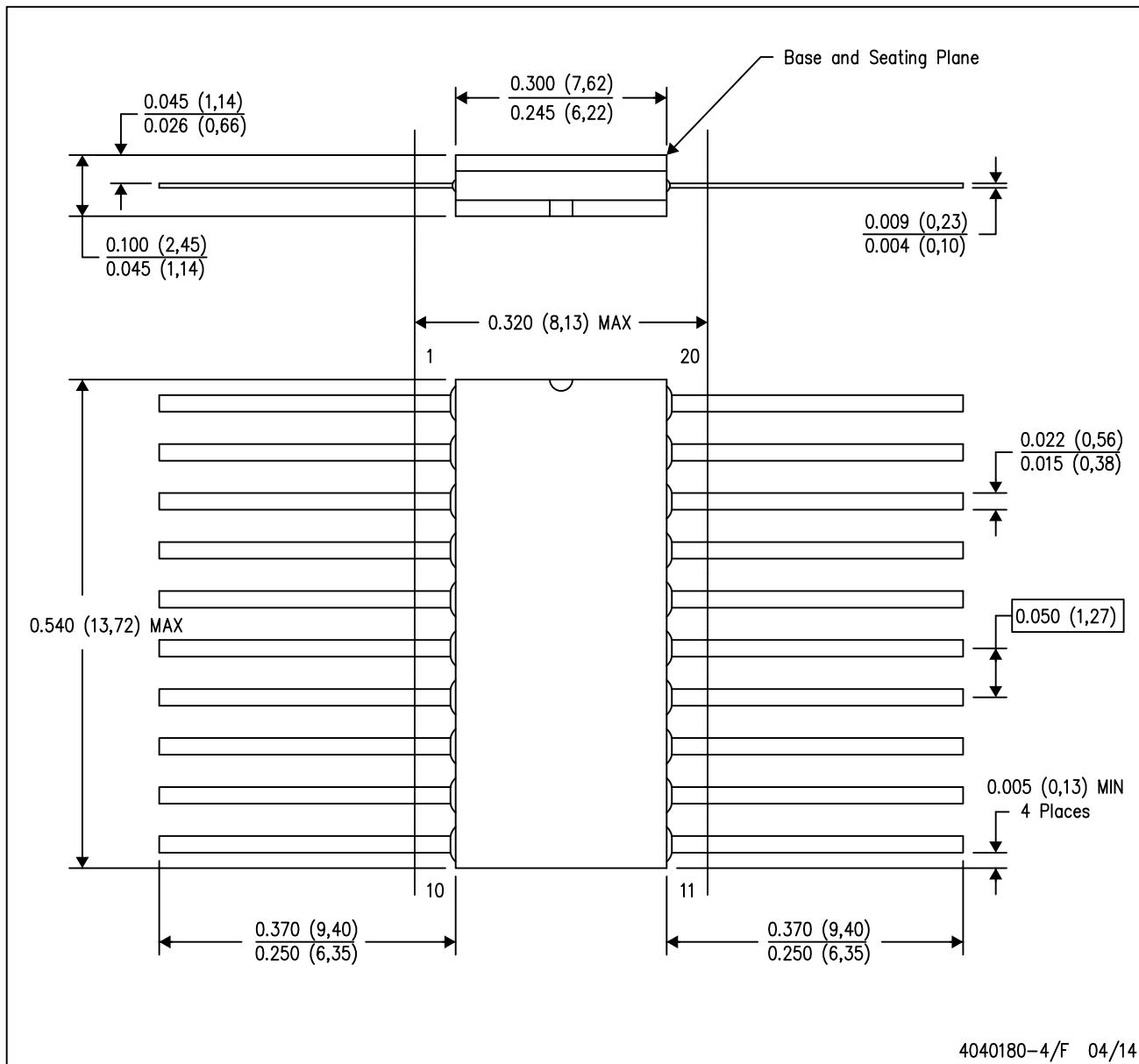
TUBE


*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
83020022A	FK	LCCC	20	55	506.98	12.06	2030	NA
8302002SA	W	CFP	20	25	506.98	26.16	6220	NA
JM38510/37204B2A	FK	LCCC	20	55	506.98	12.06	2030	NA
JM38510/37204B2A.A	FK	LCCC	20	55	506.98	12.06	2030	NA
M38510/37204B2A	FK	LCCC	20	55	506.98	12.06	2030	NA
SN74ALS374AN	N	PDIP	20	20	506	13.97	11230	4.32
SN74ALS374AN.A	N	PDIP	20	20	506	13.97	11230	4.32
SN74AS374N	N	PDIP	20	20	506	13.97	11230	4.32
SN74AS374N.A	N	PDIP	20	20	506	13.97	11230	4.32
SNJ54ALS374AFK	FK	LCCC	20	55	506.98	12.06	2030	NA
SNJ54ALS374AFK.A	FK	LCCC	20	55	506.98	12.06	2030	NA
SNJ54ALS374AW	W	CFP	20	25	506.98	26.16	6220	NA
SNJ54ALS374AW.A	W	CFP	20	25	506.98	26.16	6220	NA

W (R-GDFP-F20)

CERAMIC DUAL FLATPACK



NOTES:

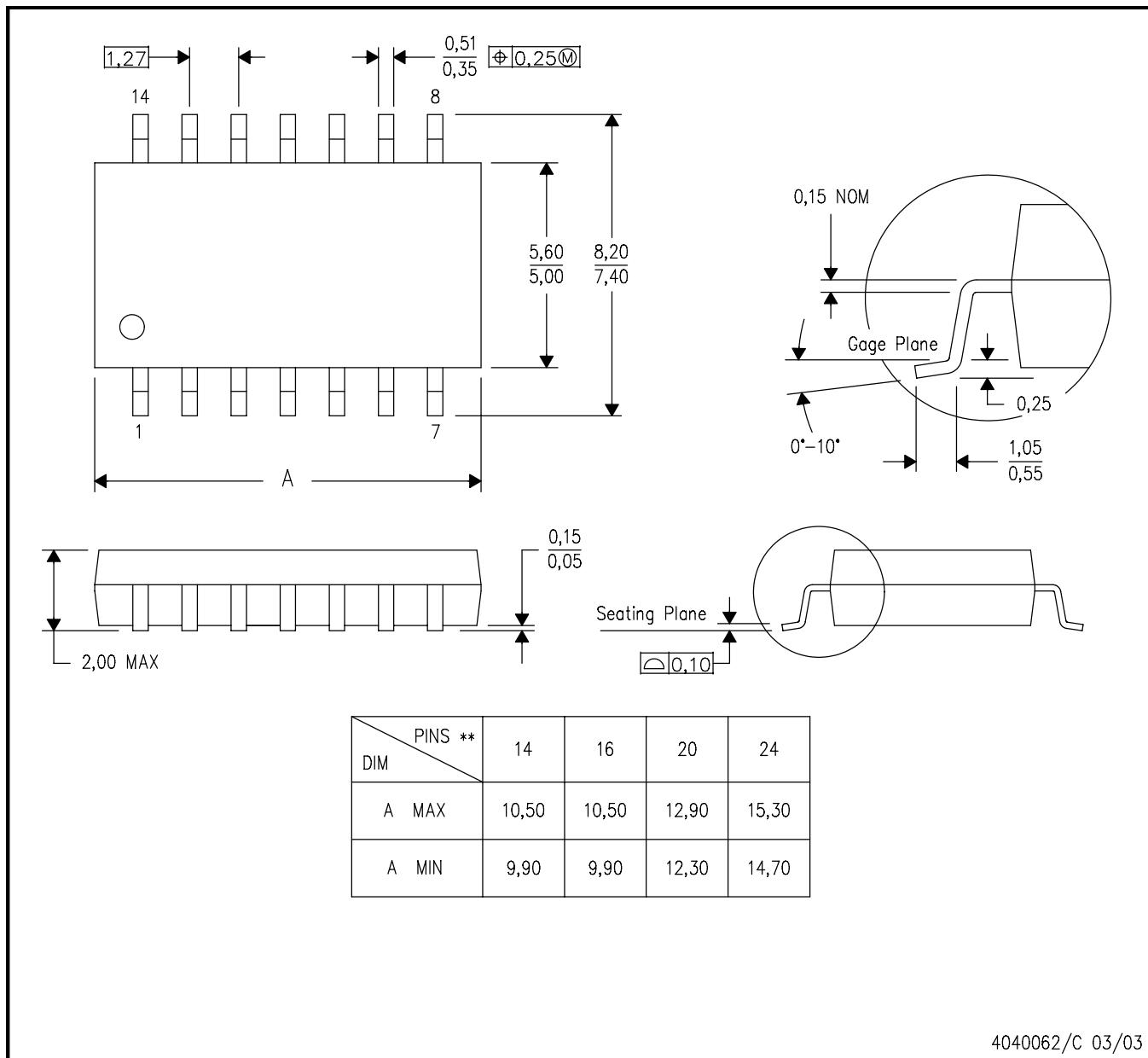
- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. This package can be hermetically sealed with a ceramic lid using glass frit.
- D. Index point is provided on cap for terminal identification only.
- E. Falls within Mil-Std 1835 GDFP2-F20

MECHANICAL DATA

NS (R-PDSO-G)**

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



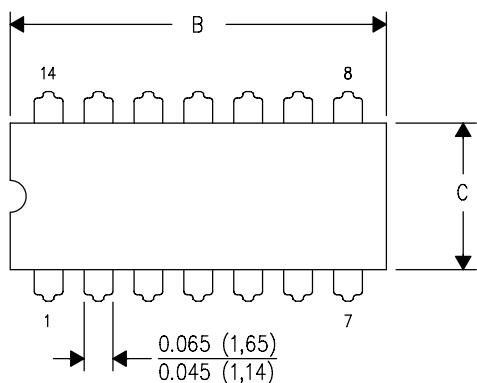
NOTES:

- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

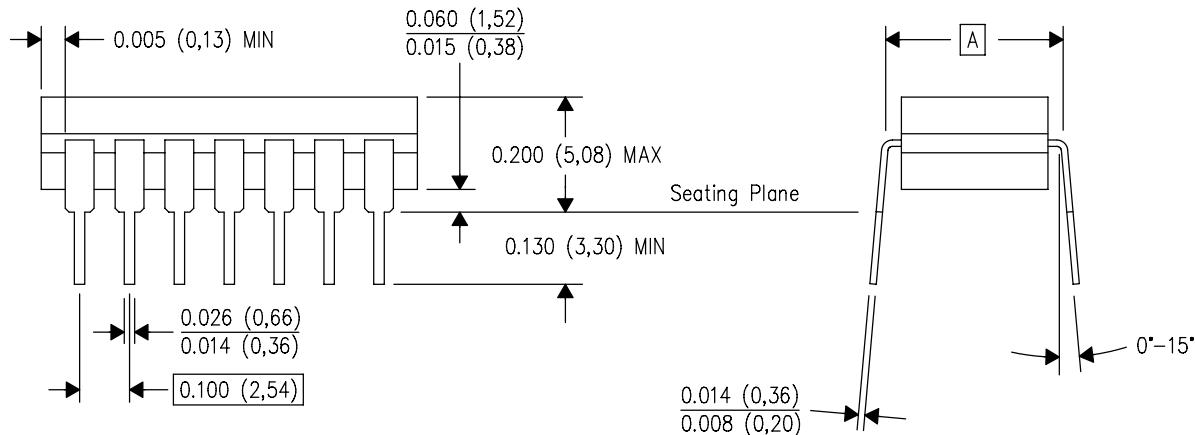
J (R-GDIP-T**)

14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



PINS ** DIM	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)



4040083/F 03/03

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package is hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

GENERIC PACKAGE VIEW

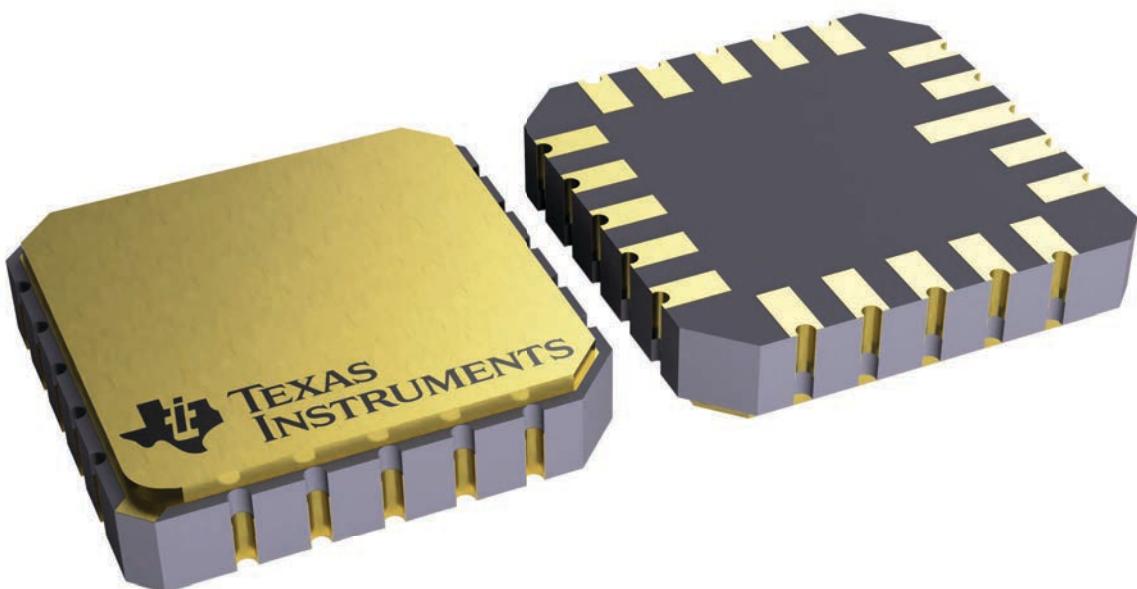
FK 20

LCCC - 2.03 mm max height

8.89 x 8.89, 1.27 mm pitch

LEADLESS CERAMIC CHIP CARRIER

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

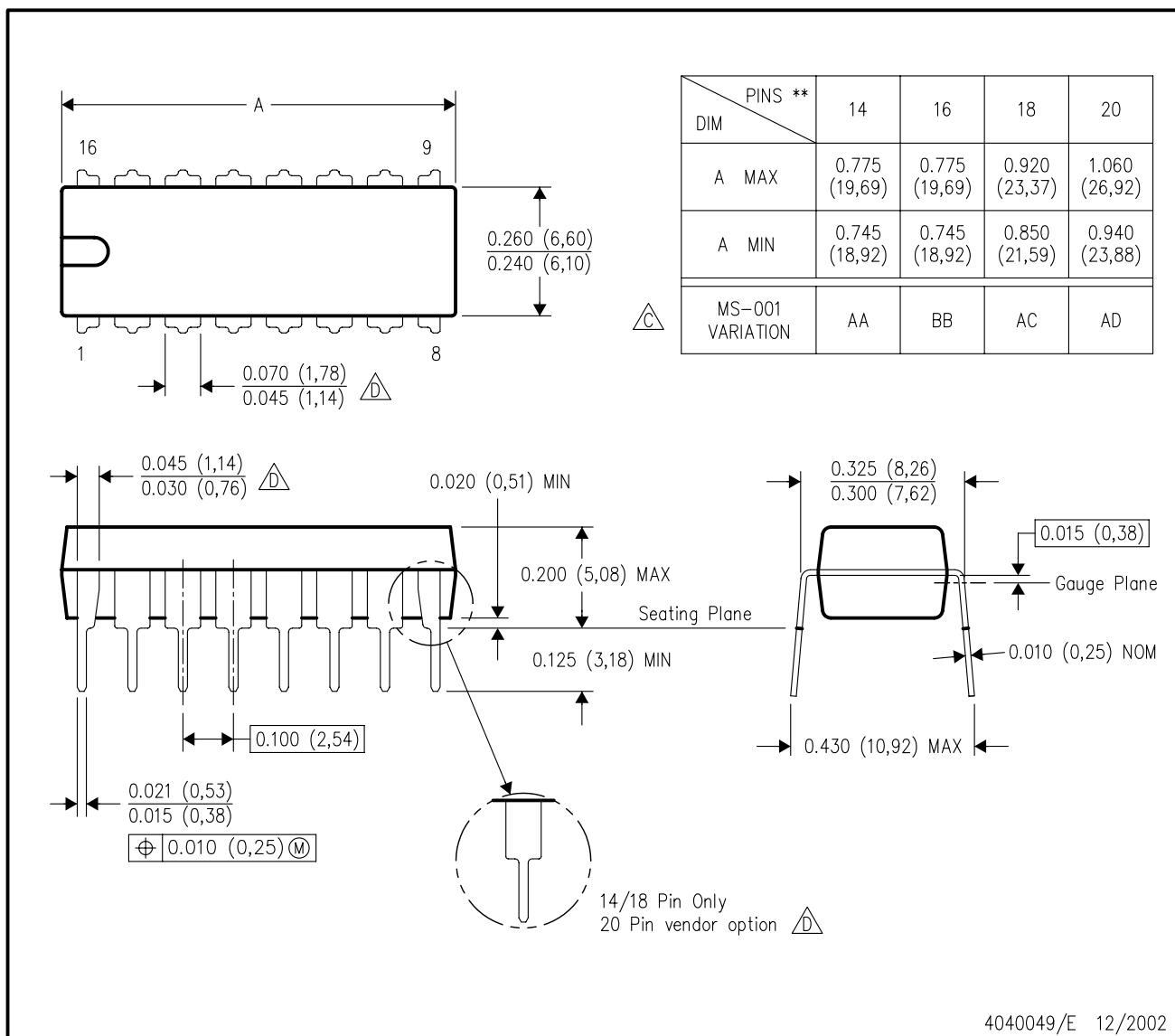


4229370VA\

N (R-PDIP-T**)

16 PINS SHOWN

PLASTIC DUAL-IN-LINE PACKAGE



NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.

△ Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).

△ The 20 pin end lead shoulder width is a vendor option, either half or full width.

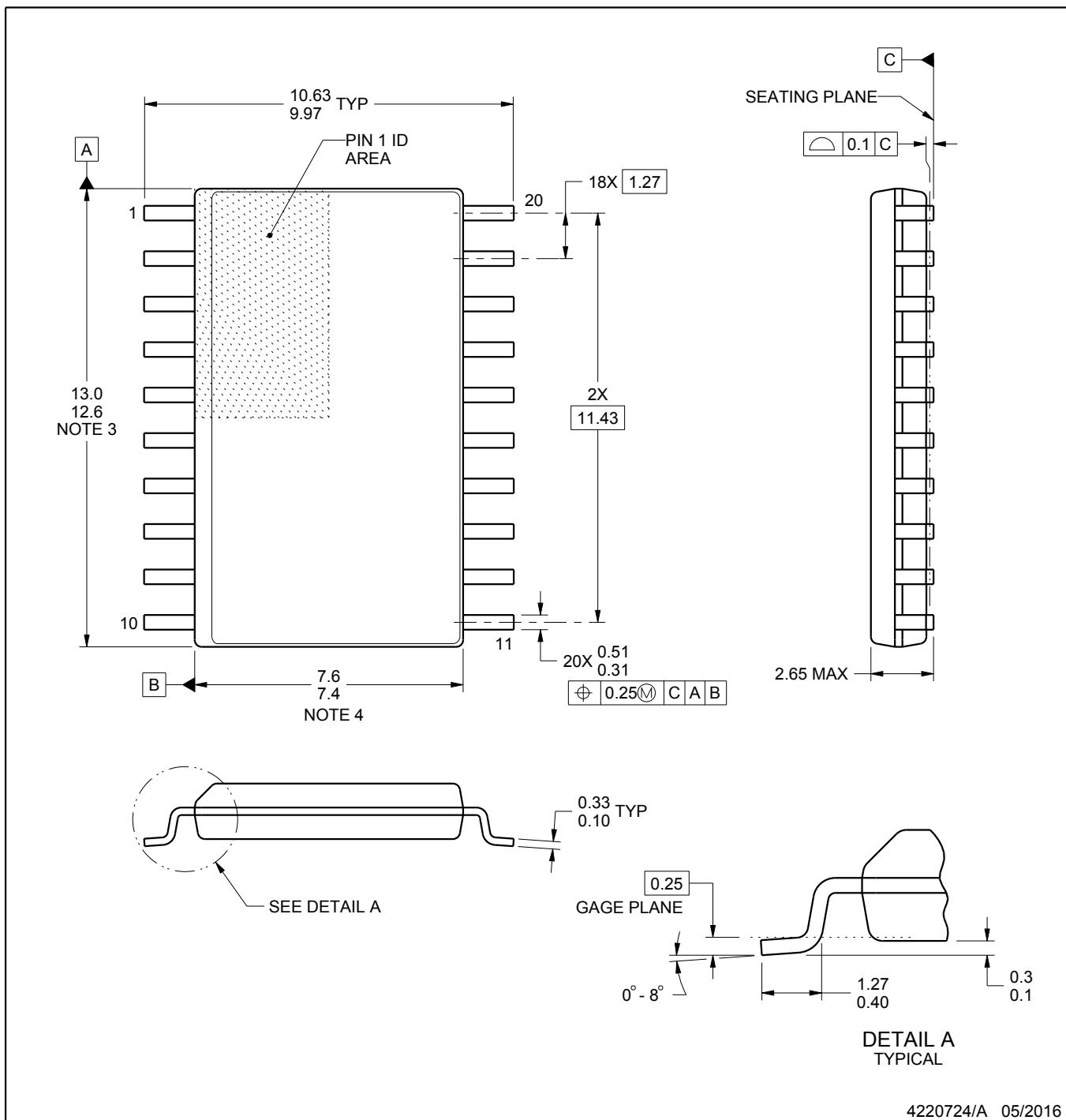
PACKAGE OUTLINE

DW0020A



SOIC - 2.65 mm max height

SOIC



NOTES:

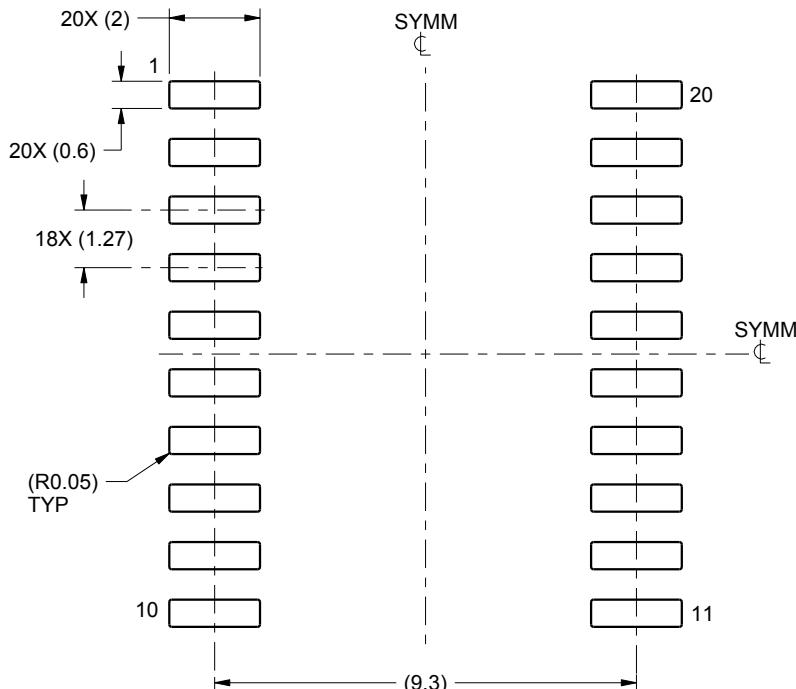
1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm per side.
5. Reference JEDEC registration MS-013.

EXAMPLE BOARD LAYOUT

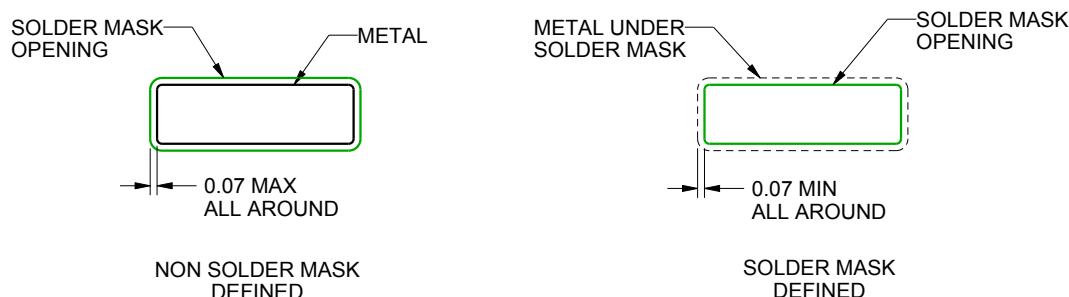
DW0020A

SOIC - 2.65 mm max height

SOIC



LAND PATTERN EXAMPLE
SCALE:6X



SOLDER MASK DETAILS

4220724/A 05/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

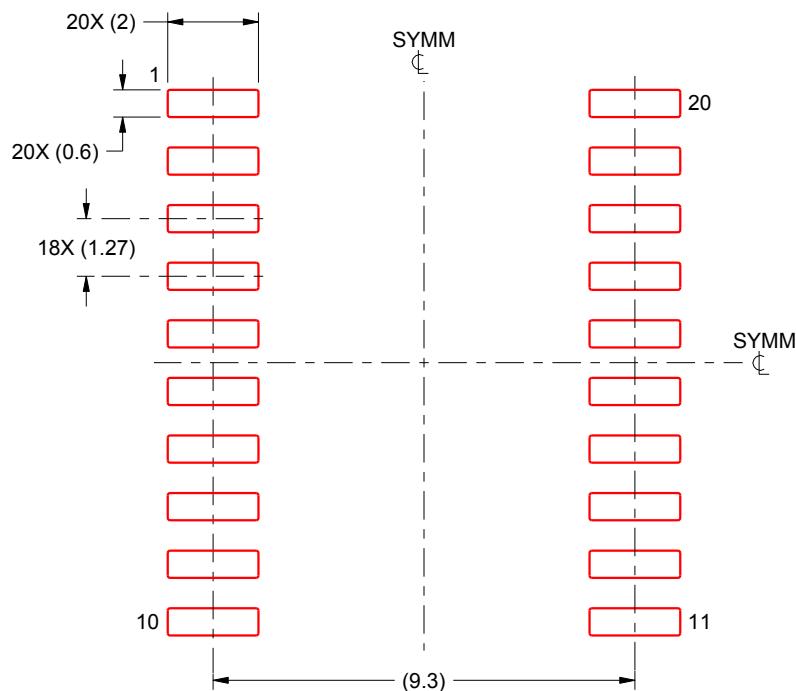
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DW0020A

SOIC - 2.65 mm max height

SOIC



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

4220724/A 05/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you fully indemnify TI and its representatives against any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to [TI's Terms of Sale](#), [TI's General Quality Guidelines](#), or other applicable terms available either on [ti.com](#) or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products. Unless TI explicitly designates a product as custom or customer-specified, TI products are standard, catalog, general purpose devices.

TI objects to and rejects any additional or different terms you may propose.

Copyright © 2026, Texas Instruments Incorporated

Last updated 10/2025