SNx4HC393 双路 4 位二进制计数器

1 特性

- 2V 至 6V 的宽工作电压范围
- 输出可驱动多达 10 个 LSTTL 负载
- 低功耗：80 µA 最大 I_{CC}
- t_{pd} 典型值 = 13ns
- 5V 时，输出驱动为 ±4mA
- 低输入电流，最大值 1 µA
- 具有独立时钟的双路 4 位二进制计数器
- 针对每个 4 位计数器的直接清零
- 可将计数器封装数量减少 50%，从而显著提高系统密度

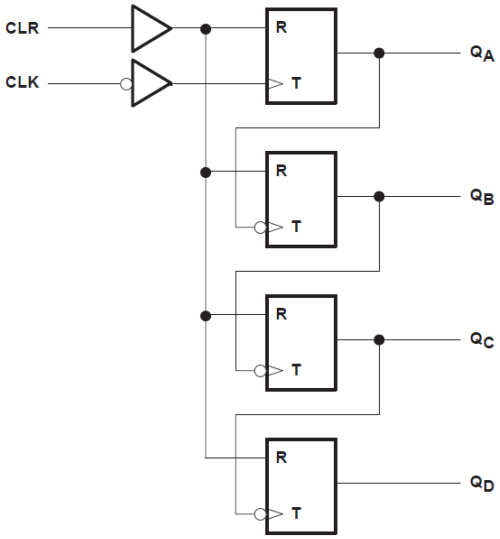
2 说明

'HC393 器件包含八个触发器和额外的门控，可在单个封装中实现两个独立的 4 位计数器。

器件信息

器件型号	封装(1)	封装尺寸(2)	本体尺寸(3)
SNx4HC393	D（SOIC，14）	8.65mm x 6mm	8.65mm x 3.9mm
	N（PDIP，14））	19.3mm x 9.4mm	19.3mm x 6.35mm
	NS（SOP，14）	10.3mm x 7.8mm	10.3mm x 5.3mm
	DB（SSOP，14）	6.2mm x 7.8mm	6.2mm x 5.3mm
	PW（TSSOP，14）	5mm x 6.4mm	5mm x 4.4mm
	DYY（SOT-23，14）	4.2mm x 3.26mm	4.2mm x 2mm
	J（CDIP，14）	19.55mm x 7.9mm	19.55mm x 6.7mm
	W（CFP，14）	9.21mm x 9mm	9.21mm x 6.28mm
	FK（LCCC，14）	8.9mm x 8.9mm	8.9mm x 8.9mm

(1) 如需了解更多信息，请参阅机械、封装和可订购信息。
(2) 封装尺寸（长 × 宽）为标称值，并包括引脚（如适用）。
(3) 本体尺寸（长 × 宽）为标称值，不包括引脚。



逻辑图，每个计数器（正逻辑）

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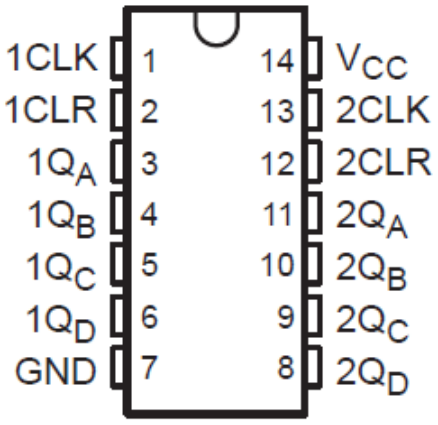
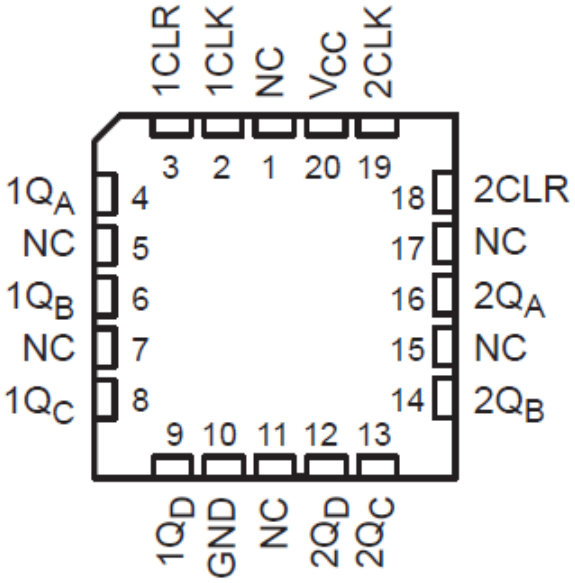
3 引脚配置和功能



SN54HC393 J 或 W 封装，14 引脚 CDIP 或 CFP；SN74HC393 D、DB、DYY、N、NS 或 PW 封装；14 引脚 SOIC、SSOP、SOT-23、TVSOP、SOP 或 TSSOP
（顶视图）



A. NC - 无内部连接

SN54HC393 FK 封装，20 引脚 LCCC
（顶视图）

表 3-1. 引脚功能

引脚		类型 [1]	说明
名称	编号		
1CLK	1	I	计数器 1 时钟输入
1CLR	2	I	计数器 1 清零输入
$1Q_A$	3	O	计数器 1 A 输出
$1Q_B$	4	O	计数器 1 B 输出
$1Q_C$	5	O	计数器 1 B 输出
$1Q_D$	6	O	计数器 1 B 输出
GND	7	G	接地
$2Q_D$	8	O	计数器 2 D 输出
$2Q_C$	9	O	计数器 2 C 输出
$2Q_B$	10	O	计数器 2 B 输出
$2Q_A$	11	O	计数器 2 A 输出
2CLR	12	I	计数器 2 清零输入
2CLK	13	I	计数器 2 时钟输入
V_{CC}	14	P	V_{CC}

1. I = 输入，O = 输出，I/O = 输入或输出，G = 接地，P = 电源。

4 规格

4.1 绝对最大额定值

在自然通风条件下的工作温度范围内测得（除非另有说明）(1)

			最小值	最大值	单位
V_{CC}	电源电压范围		-0.5	7	V
I_{IK}	输入钳位电流(2)	$V_I < 0V$ 或 $V_I > V_{CC}$		±20	mA
I_{OK}	输出钳位电流(2)	$V_O < 0V$ 或 $V_O > V_{CC}$		±20	mA
I_O	持续输出电流	$V_O = 0$ 至 V_{CC}		±25	mA
	通过 V_{CC} 或 GND 的持续电流			±50	mA
T_{stg}	贮存温度范围		-65	150	℃

(1) 超出*绝对最大额定值*下列出的应力可能会对器件造成永久损坏。这些仅为在应力额定值下的工作情况，对于额定值下的器件的功能性操作以及在超出*推荐的运行条件*下标明的任何其它条件下的操作，在此并未说明。长时间处于绝对最大额定条件下可能会影响器件的可靠性。

(2) 如果遵守输入和输出电流额定值，输入和输出电压可超过额定值。

4.2 建议运行条件

在自然通风条件下的工作温度范围内测得（除非另有说明）(1)

			SN54HC393			SN74HC393			单位
			最小值	标称值	最大值	最小值	标称值	最大值	
V_{CC}	电源电压		2	5	6	2	5	6	V
V_{IH}	高电平输入电压	V_{CC} = 2V	1.5			1.5			V
		V_{CC} = 4.5V	3.15			3.15			
		V_{CC} = 6V	4.2			4.2			
V_{IL}	低电平输入电压	V_{CC} = 2V			0.5			0.5	V
		V_{CC} = 4.5V			1.35			1.35	
		V_{CC} = 6V			1.8			1.8	
V_I	输入电压		0		V_{CC}	0		V_{CC}	V
V_O	输出电压		0		V_{CC}	0		V_{CC}	V
$\Delta t/\Delta v$(2)	输入转换上升/下降时间	V_{CC} = 2V			1000			1000	ns
		V_{CC} = 4.5V			500			500	
		V_{CC} = 6V			400			400	
T_A	自然通风条件下的工作温度范围		-55		125	-40		85	℃

(1) 器件所有的未使用输入必须保持在 V_{CC} 或 GND 以确保器件正常运行。请参阅 TI 应用报告 *CMOS 输入缓慢变化或悬空的影响*，文献编号 SCBA004。

(2) 如果此器件在阈值区间（从 V_{ILmax} = 0.5V 至 V_{IHmin} = 1.5V）内使用，感应接地有可能进入错误状态，从而产生双时钟。在 t_t = 1000ns 且 V_{CC} = 2V 的输入范围内工作不会损坏器件；但在功能上，在移位、计数或切换操作模式下不能确保 CLK 输入。

4.3 热性能信息

热指标(1)		SN74HC393						单位
		D (SOIC)	DB (SSOP)	DYY (SOT-23)	N (PDIP)	NS (SO)	PW (TSSOP)	
		14 引脚	14 引脚	14 引脚	14 引脚	14 引脚	14 引脚	
$R_{\theta JA}$	结至环境热阻	86	96	124.1	80	76	113	°C/W

(1) 有关新旧热指标的更多信息，请参阅半导体和 IC 封装热指标应用报告。

4.4 电气特性

在自然通风条件下的建议运行温度范围内测得（除非另有说明）

参数	测试条件		V_{CC}	T_A = 25°C			SN54HC393		SN74HC393		单位
				最小值	典型值	最大值	最小值	最大值	最小值	最大值	
V_{OH}	V_I = V_{IH} 或 V_{IL}	I_{OH}=-20 μA	2V	1.9	1.998		1.9		1.9		V
			4.5V	4.4	4.499		4.4		4.4		
			6V	5.9	5.999		5.9		5.9		
		I_{OH} = -4mA	4.5V	3.98	4.3		3.7		3.84		
		I_{OH} = -5.2mA	6V	5.48	5.8		5.2		5.34		
V_{OL}	V_I = V_{IH} 或 V_{IL}	I_{OL} = 20 μA	2V		0.002	0.1		0.1		0.1	V
			4.5V		0.001	0.1		0.1		0.1	
			6		0.001	0.1		0.1		0.1	
		I_{OL} = 4mA	4.5V		0.17	0.26		0.4		0.33	
		I_{OL} = 5.2mA	6V		0.15	0.26		0.4		0.33	
I_I	V_I = V_{CC} 或 0		6V		±0.1	±100		±1000		±1000	nA
I_{CC}	V_I = V_{CC} 或 0	I_O = 0	6V			8		160		80	μA
C_i			2V 至 6V		3	10		10		10	pF

4.5 时序要求

在自然通风条件下的建议运行温度范围内测得（除非另有说明）

参数			V_{CC}	T_A = 25°C		SN54HC393		SN74HC393		单位
				最小值	最大值	最小值	最大值	最小值	最大值	
f_{clock}	时钟频率		2V		6		4.2		5	MHz
			4.5V		31		21		25	
			6V		36		25		28	
t_w	脉冲持续时间	CLK 高电平或低电平	2V	80		120		100		ns
			4.5V	16		24		20		
			6V	14		20		18		
		CLR 高电平	2V	80		120		100		
			4.5V	16		24		20		
			6V	14		20		18		
t_{su}	安装时间，清零功能失效		2V	25		25		25		ns
			4.5V	5		5		5		
			6V	5		5		5		

4.6 开关特性

在建议的自然通风条件下的工作温度范围内，C_L = 50 pF（除非另有说明）(图 5-1)

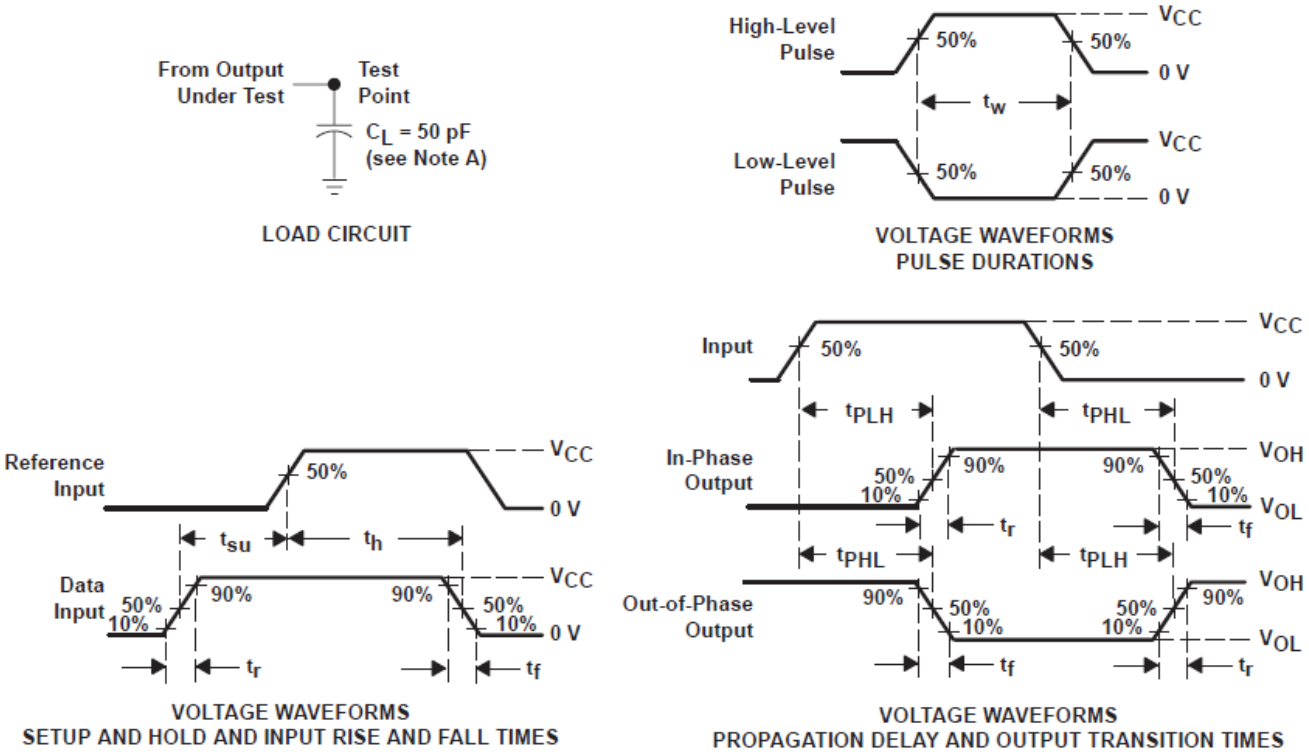
参数	从（输入）	至（输出）	V_{CC}	T_A = 25°C			SN54HC393		SN74HC393		单位
				最小值	典型值	最大值	最小值	最大值	最小值	最大值	
f_{max}	CLK	Q_A	2V	6	10		4.2		5		MHz
			4.5V	31	50		21		25		
			6V	36	60		25		28		
t_{pd}	CLK	Q_A	2V		50	120		180		150	ns
			4.5V		15	24		36		30	
			6V		13	20		31		26	
		Q_B	2V		72	190		285		240	
			4.5V		22	38		57		47	
			6V		18	32		48		40	
		Q_C	2V		91	240		360		300	
			4.5V		28	48		72		60	
			6V		22	41		61		51	
		Q_D	2V		100	290		430		360	
			4.5V		32	58		87		72	
			6V		24	50		74		62	
t_{PHL}	CLR	不限	2V		45	165		250		205	
			4.5V		17	33		49		41	
			6V		14	28		42		35	
t_t		不限	2V		28	75		110		95	ns
			4.5V		8	15		22		19	
			6V		6	13		19		16	

4.7 工作特性

T_A = 25°C

参数		测试条件	典型值	单位
C_{PD}	功率耗散电容	无负载	40	pF

5 参数测量信息



A. C_L 包括探头和测试夹具电容。

B. 任意选择波形之间的相位关系。所有输入脉冲均由具有以下特性的发生器提供：PRR ≤ 1MHz，Z_O = 50 Ω，t_r = 6ns，t_f = 6ns。

C. 对于时钟输入，f_{max} 是在输入占空比为 50% 时测量的。

D. 一次测量一个输出，每次测量一个输入转换。

E. t_{PLH} 和 t_{PHL} 与 t_{pd} 一样。

图 5-1. 负载电路和电压波形

6 详细说明

6.1 概述

'HC393 器件包含八个触发器和额外的门控，可在单个封装中实现两个独立的 4 位计数器。这些器件包含两个独立的 4 位二进制计数器，每个计数器都具有清零(CLR)输入和时钟(CLK)输入。每个封装都可以实现 N 位二进制计数器，可实现 256 位异步二进制计数器。'HC393 器件的每个计数器级都有并行输出，因此输入计数频率的任何因数都可用于系统计时信号。

6.2 功能方框图

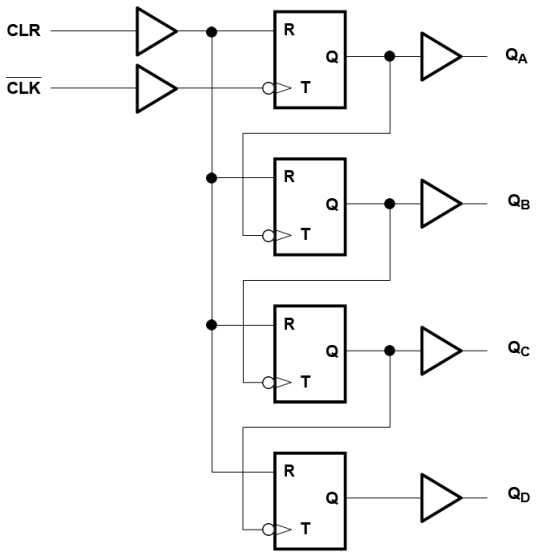


图 6-1. 逻辑图，每个计数器（正逻辑）

6.3 器件功能模式

表 6-1. 功能表计数序列
(每个缓冲器)

数量	输出			
	Q_D	Q_C	Q_B	Q_A
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	L	H	H	L
7	L	H	H	H
8	H	L	L	L
9	H	L	L	H
10	H	L	H	L
11	H	L	H	H
12	H	H	L	L
13	H	H	L	H
14	H	H	H	L
15	H	H	H	H

7 应用和实施

备注

以下应用部分中的信息不属于 TI 器件规格的范围，TI 不担保其准确性和完整性。TI 的客 户应负责确定器件是否适用于其应用。客户应验证并测试其设计，以确保系统功能。

7.1 电源相关建议

电源可以是*建议运行条件* 中最小和最大电源电压额定值之间的任何电压。每个 V_{CC} 端子均应具有一个良好的旁路电容器，以防止功率干扰。建议为该器件使用 0.1 µF 电容器。可以并联多个旁路电容器以抑制不同的噪声频率。0.1 µF 和 1 µF 电容器通常并联使用。为了获得最佳效果，旁路电容器必须尽可能靠近电源端子安装。

7.2 布局

7.2.1 布局指南

- 旁路电容器的放置
  - 靠近器件的正电源端子放置
  - 提供电气短接地返回路径
  - 使用宽布线以最大限度减小阻抗
  - 尽可能将器件、电容器和布线保持在电路板的同一面
- 信号布线几何形状
  - 8mil 至 12mil 布线宽度
  - 布线长度小于 12cm 可最大限度减轻传输线路影响
  - 避免信号布线出现 90° 角
  - 在信号布线下方使用不间断的接地平面
  - 通过接地对信号布线周围的区域进行泛洪填充
  - 对于长度超过 12cm 的布线
    - 使用阻抗受控的布线
    - 在输出端附近使用串联阻尼电阻进行源端接
    - 避免分支；对必须单独分支的信号进行缓冲

7.2.2 布局示例

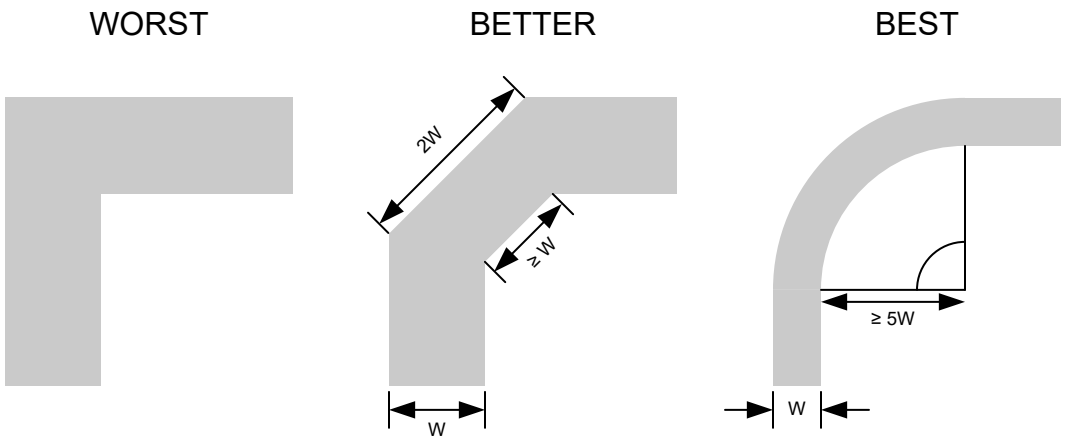


图 7-1. 可改善信号完整性的布线转角示例

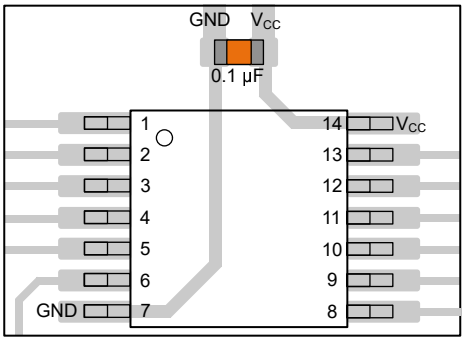


图 7-2. TSSOP 和类似封装的旁路电容器放置示例

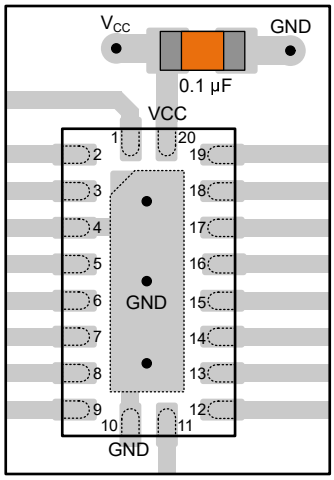


图 7-3. WQFN 和类似封装的旁路电容器放置示例

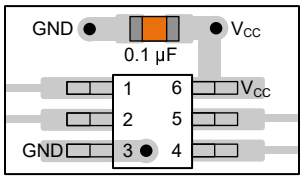


图 7-4. SOT、SC70 和类似封装的旁路电容器放置示例

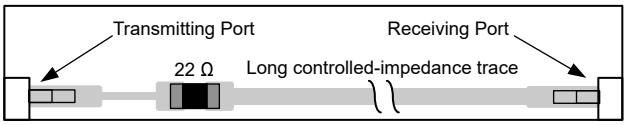


图 7-5. 可改善信号完整性的阻尼电阻放置示例

8 器件和文档支持

TI 提供广泛的开发工具。下面列出了用于评估器件性能、生成代码和开发解决方案的工具和软件。

8.1 文档支持

8.1.1 相关文档

8.2 接收文档更新通知

要接收文档更新通知，请导航至 ti.com 上的器件产品文件夹。点击*通知* 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

8.3 支持资源

TI E2E™ 中文支持论坛是工程师的重要参考资料，可直接从专家处获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题，获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的使用条款。

8.4 商标

TI E2E™ is a trademark of Texas Instruments.
所有商标均为其各自所有者的财产。

8.5 静电放电警告

静电放电 (ESD) 会损坏这个集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

8.6 术语表

TI 术语表　　本术语表列出并解释了术语、首字母缩略词和定义。

9 修订历史记录

注：以前版本的页码可能与当前版本的页码不同

Changes from Revision D (July 2003) to Revision E (December 2024)	Page
• 添加了*器件信息* 表、*引脚功能* 表、*热性能信息* 表、*器件功能模式*、”应用和实施“部分、*器件和文档支持* 部分以及*机械、封装和订购信息* 部分	1
• 向 *器件信息*表，*引脚功能和配置*部分以及*热性能信息*表中添加 DDY 封装	1

10 机械、封装和可订购信息

以下页面包含机械、封装和可订购信息。这些信息是指定器件可用的最新数据。数据如有变更，恕不另行通知，且不会对此文档进行修订。有关此数据表的浏览器版本，请查阅左侧的导航栏。

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
84100012A	ACTIVE	LCCC	FK	20	55	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	84100012A SNJ54HC 393FK	Samples
8410001CA	ACTIVE	CDIP	J	14	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	8410001CA SNJ54HC393J	Samples
8410001DA	ACTIVE	CFP	W	14	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	8410001DA SNJ54HC393W	Samples
JM38510/66309BCA	ACTIVE	CDIP	J	14	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	JM38510/ 66309BCA	Samples
M38510/66309BCA	ACTIVE	CDIP	J	14	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	JM38510/ 66309BCA	Samples
SN54HC393J	ACTIVE	CDIP	J	14	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	SN54HC393J	Samples
SN74HC393D	OBSOLETE	SOIC	D	14		TBD	Call TI	Call TI	-40 to 85	HC393	
SN74HC393DBR	ACTIVE	SSOP	DB	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC393	Samples
SN74HC393DR	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 85	HC393	Samples
SN74HC393DT	OBSOLETE	SOIC	D	14		TBD	Call TI	Call TI	-40 to 85	HC393	
SN74HC393N	ACTIVE	PDIP	N	14	25	RoHS & Green	NIPDAU	N / A for Pkg Type	-40 to 85	SN74HC393N	Samples
SN74HC393NSR	ACTIVE	SOP	NS	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC393	Samples
SN74HC393PW	OBSOLETE	TSSOP	PW	14		TBD	Call TI	Call TI	-40 to 85	HC393	
SN74HC393PWR	ACTIVE	TSSOP	PW	14	2000	RoHS & Green	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 85	HC393	Samples
SN74HC393PWT	OBSOLETE	TSSOP	PW	14		TBD	Call TI	Call TI	-40 to 85	HC393	
SN74HCS393DYYR	ACTIVE	SOT-23-THIN	DYY	14	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HCS393	Samples
SNJ54HC393FK	ACTIVE	LCCC	FK	20	55	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	84100012A SNJ54HC 393FK	Samples
SNJ54HC393J	ACTIVE	CDIP	J	14	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	8410001CA SNJ54HC393J	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SNJ54HC393W	ACTIVE	CFP	W	14	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	8410001DA SNJ54HC393W	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

OTHER QUALIFIED VERSIONS OF SN54HC393, SN74HC393 :

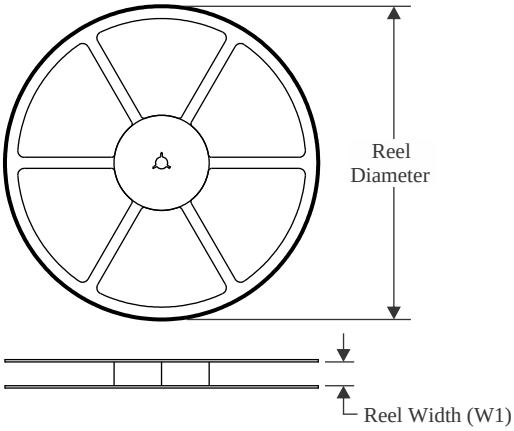
- Catalog : SN74HC393
- Military : SN54HC393

NOTE: Qualified Version Definitions:

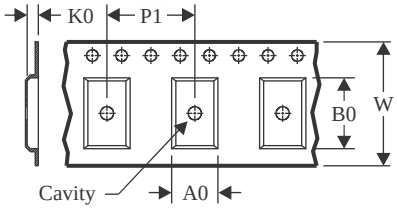
- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

TAPE AND REEL INFORMATION

REEL DIMENSIONS

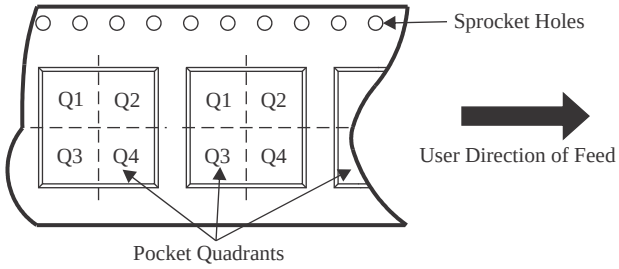


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

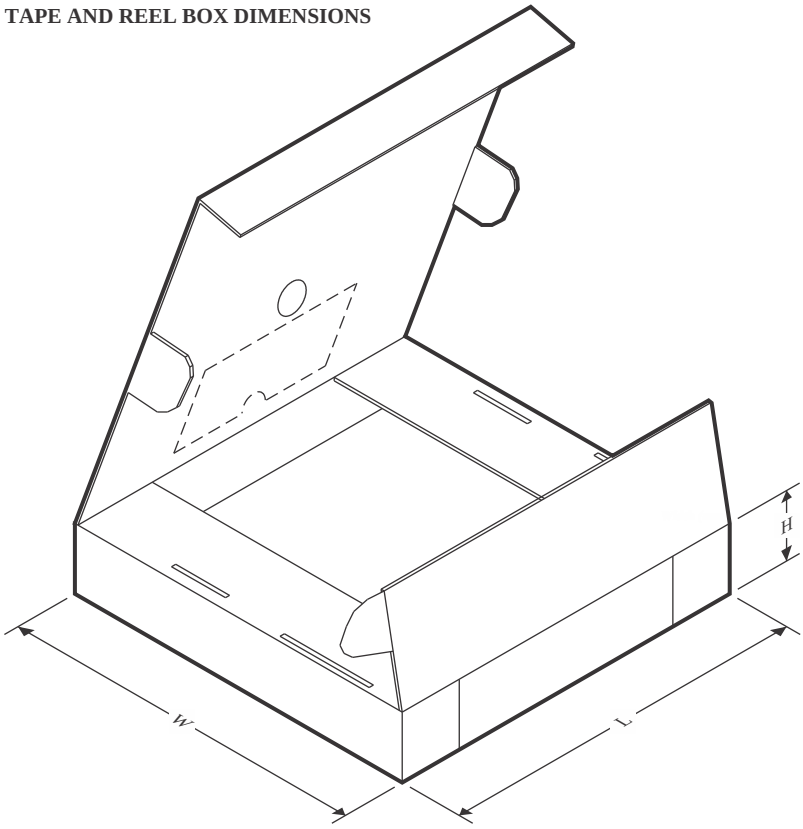
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74HC393DBR	SSOP	DB	14	2000	330.0	16.4	8.35	6.6	2.4	12.0	16.0	Q1
SN74HC393DR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
SN74HC393DR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
SN74HC393NSR	SOP	NS	14	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1
SN74HC393NSR	SOP	NS	14	2000	330.0	16.4	8.45	10.55	2.5	12.0	16.2	Q1
SN74HC393PWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74HC393PWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74HCS393DYYR	SOT-23-THIN	DYY	14	3000	330.0	12.4	4.8	3.6	1.6	8.0	12.0	Q3

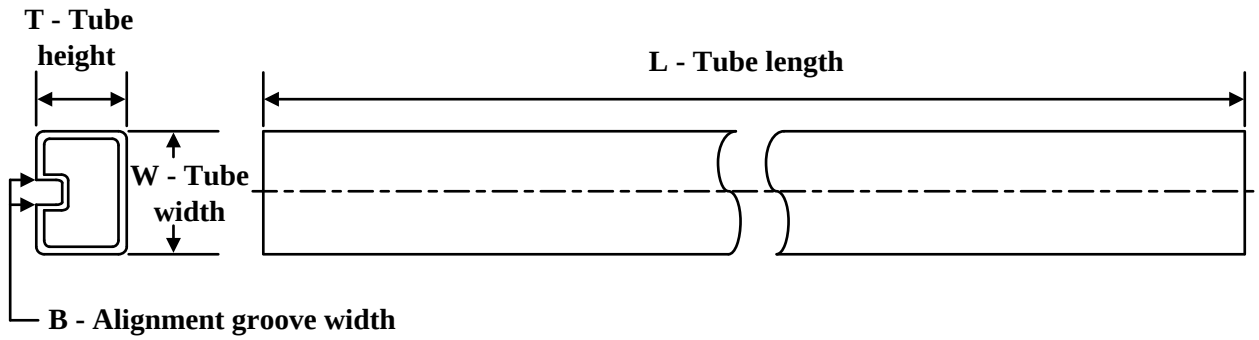
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74HC393DBR	SSOP	DB	14	2000	356.0	356.0	35.0
SN74HC393DR	SOIC	D	14	2500	356.0	356.0	35.0
SN74HC393DR	SOIC	D	14	2500	356.0	356.0	35.0
SN74HC393NSR	SOP	NS	14	2000	367.0	367.0	38.0
SN74HC393NSR	SOP	NS	14	2000	356.0	356.0	35.0
SN74HC393PWR	TSSOP	PW	14	2000	356.0	356.0	35.0
SN74HC393PWR	TSSOP	PW	14	2000	356.0	356.0	35.0
SN74HCS393DYYR	SOT-23-THIN	DYY	14	3000	336.6	336.6	31.8

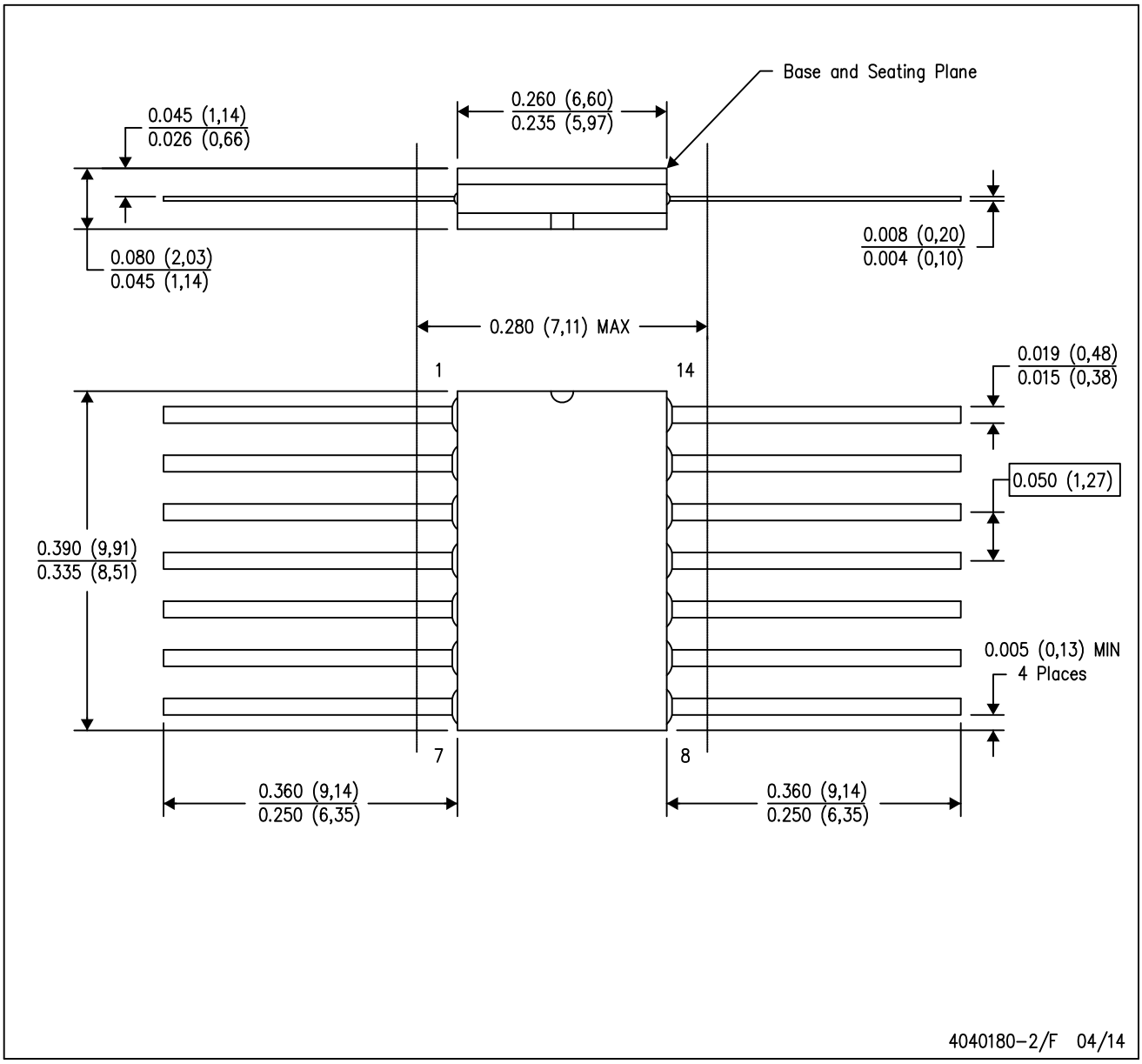
TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
84100012A	FK	LCCC	20	55	506.98	12.06	2030	NA
8410001DA	W	CFP	14	25	506.98	26.16	6220	NA
SN74HC393N	N	PDIP	14	25	506	13.97	11230	4.32
SN74HC393N	N	PDIP	14	25	506	13.97	11230	4.32
SNJ54HC393FK	FK	LCCC	20	55	506.98	12.06	2030	NA
SNJ54HC393W	W	CFP	14	25	506.98	26.16	6220	NA

W (R–GDFP–F14) CERAMIC DUAL FLATPACK



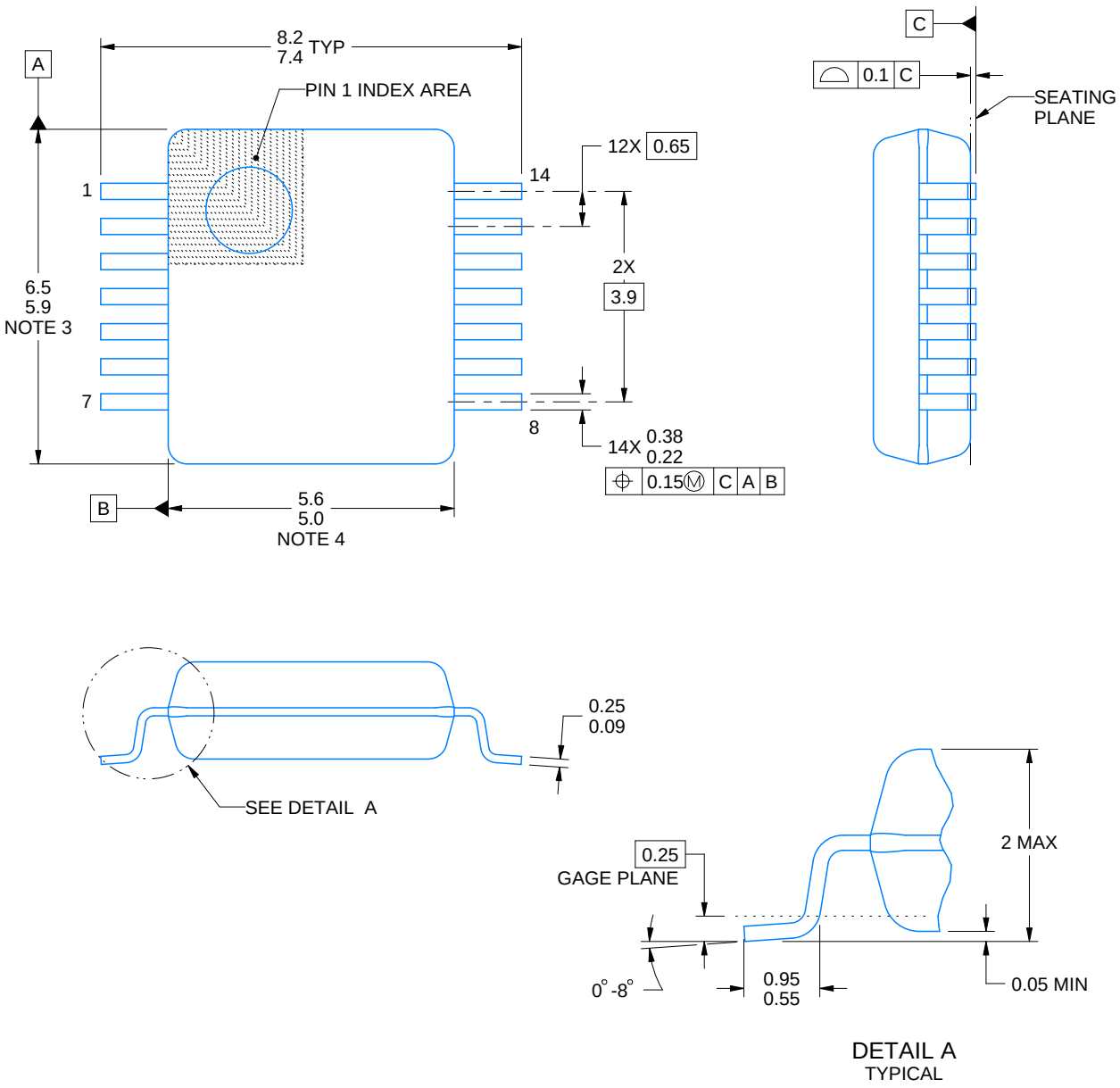
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only.
E. Falls within MIL STD 1835 GDFP1–F14

PACKAGE OUTLINE

DB0014A

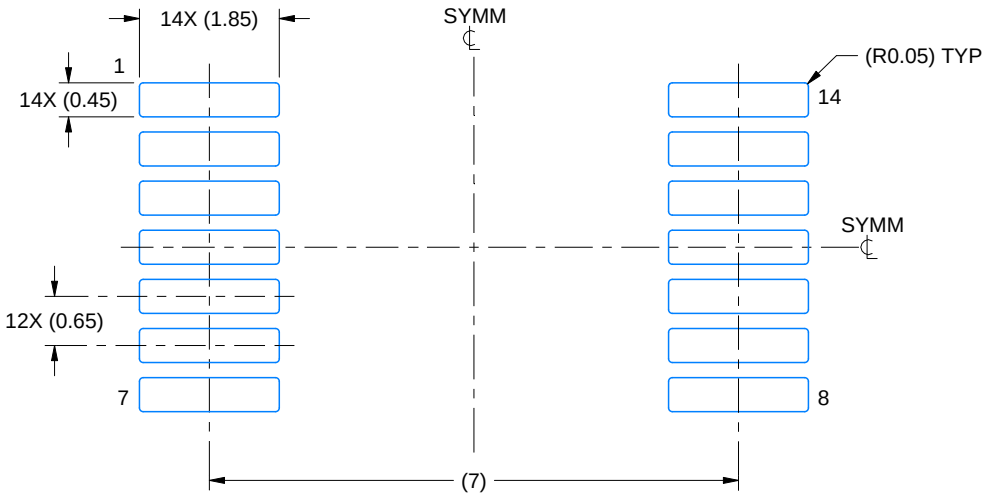
SSOP - 2 mm max height

SMALL OUTLINE PACKAGE

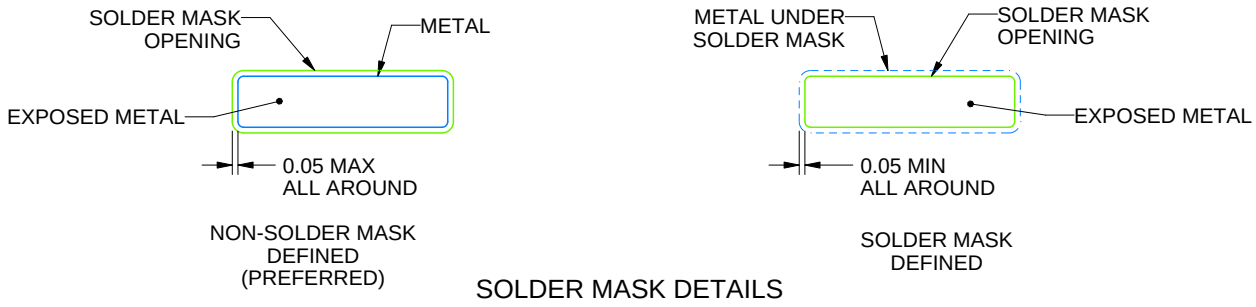


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-150.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

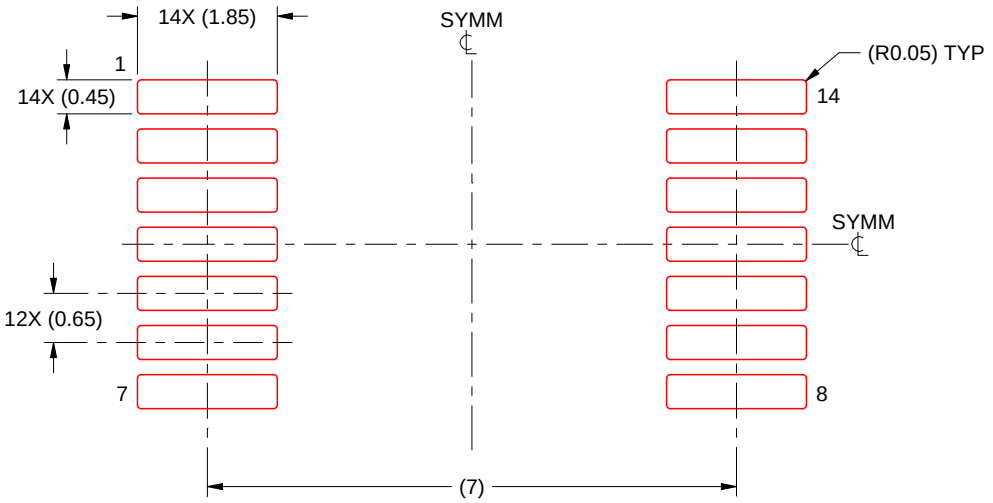


SOLDER MASK DETAILS

4220762/A 05/2024

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220762/A 05/2024

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

GENERIC PACKAGE VIEW

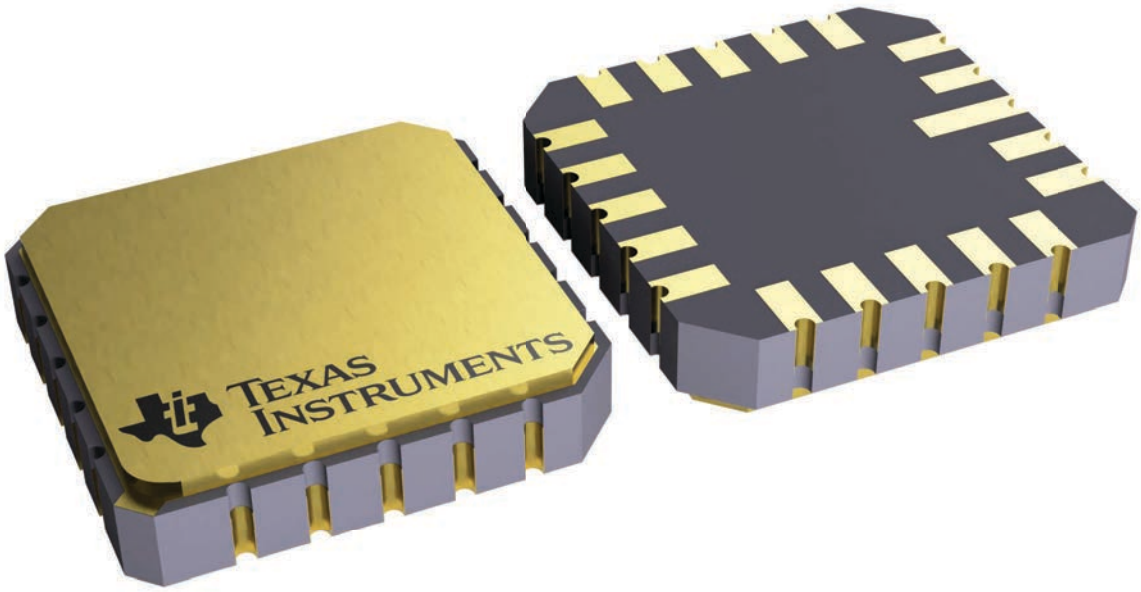
FK 20

LCCC - 2.03 mm max height

8.89 x 8.89, 1.27 mm pitch

LEADLESS CERAMIC CHIP CARRIER

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

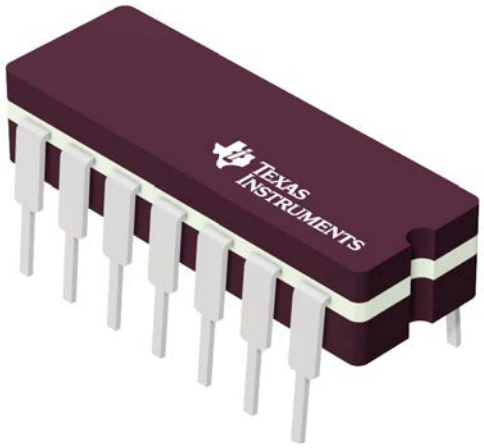


4229370VA\

GENERIC PACKAGE VIEW

J 14 CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

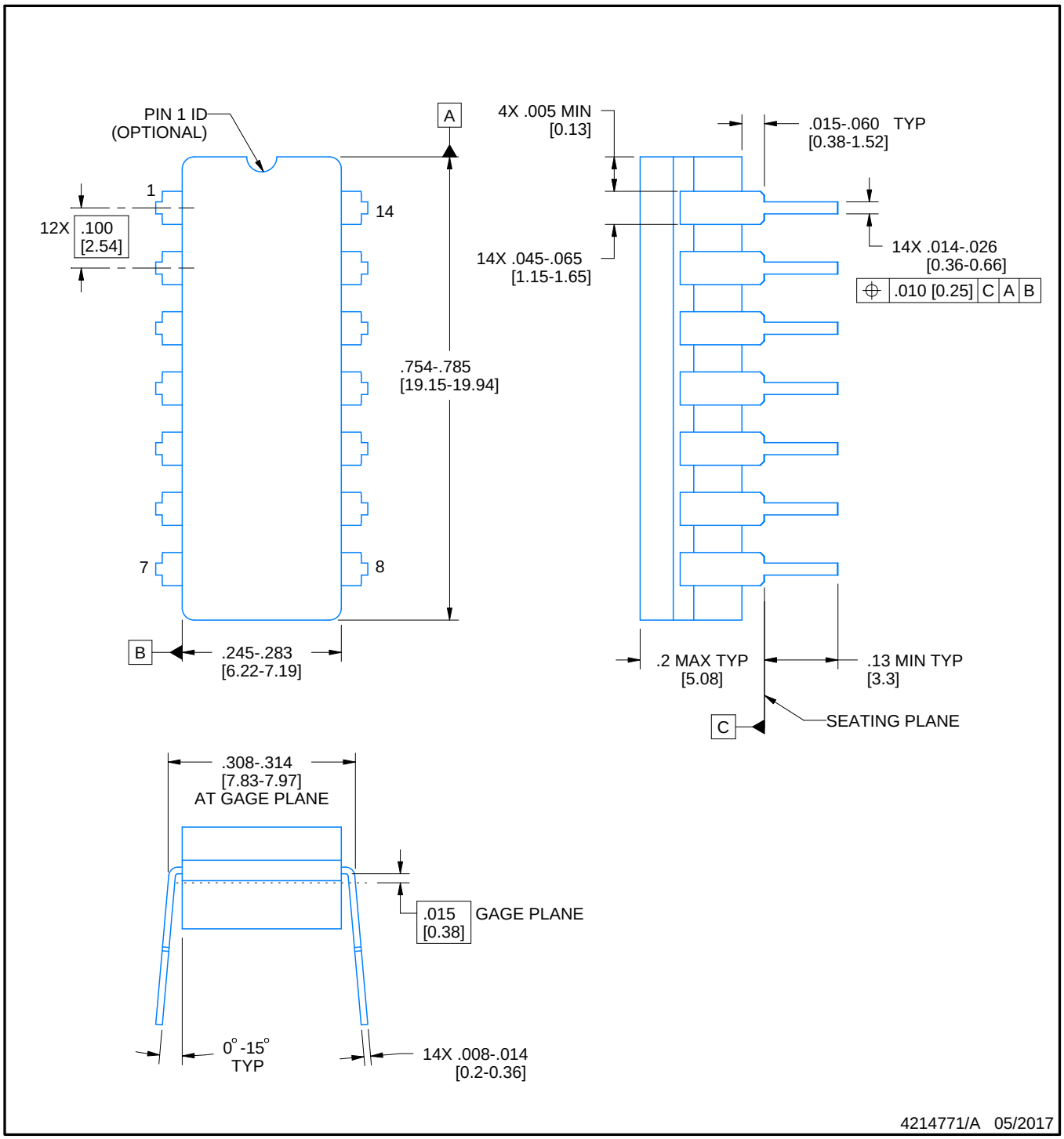
4040083-5/G

PACKAGE OUTLINE

J0014A

CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE



NOTES:

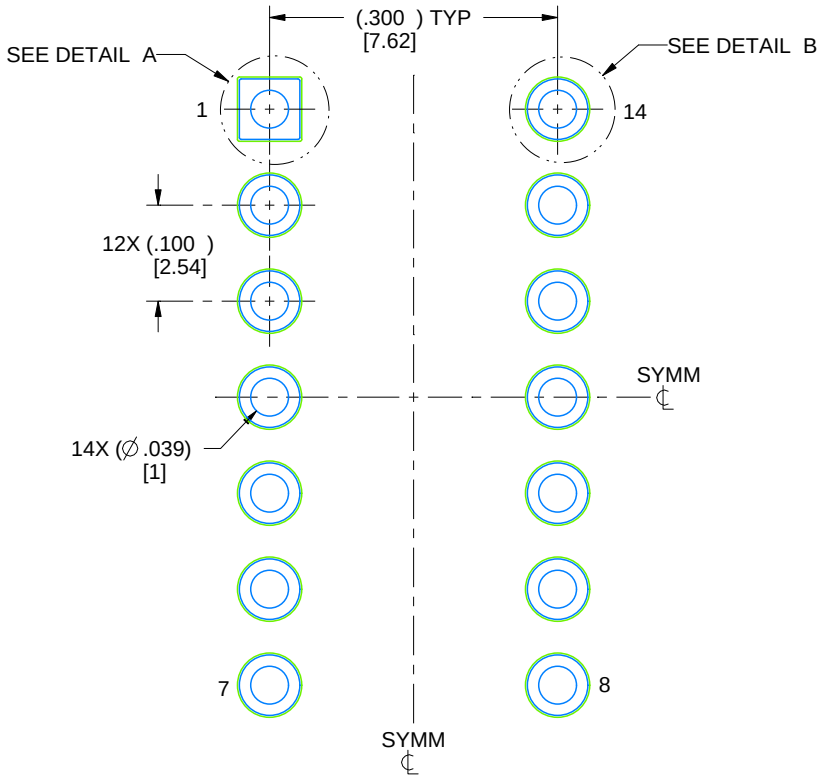
1. All controlling linear dimensions are in inches. Dimensions in brackets are in millimeters. Any dimension in brackets or parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This package is hermitically sealed with a ceramic lid using glass frit.
4. Index point is provided on cap for terminal identification only and on press ceramic glass frit seal only.
5. Falls within MIL-STD-1835 and GDIP1-T14.

EXAMPLE BOARD LAYOUT

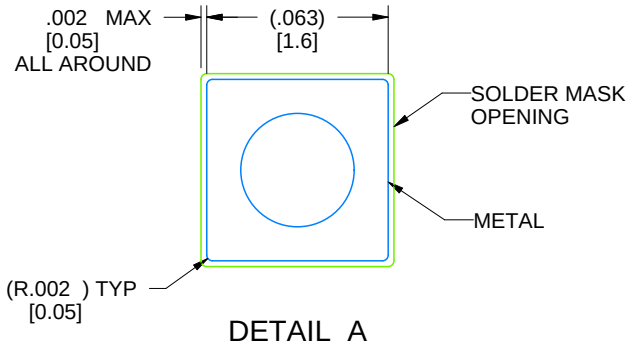
J0014A

CDIP - 5.08 mm max height

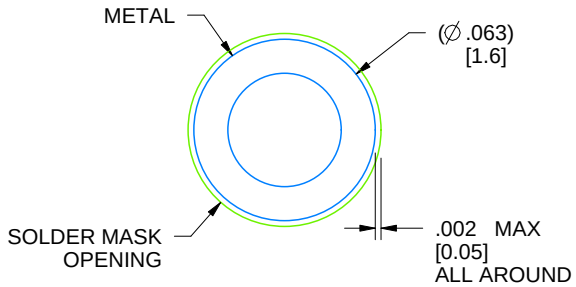
CERAMIC DUAL IN LINE PACKAGE



LAND PATTERN EXAMPLE
NON-SOLDER MASK DEFINED
SCALE: 5X



DETAIL A
SCALE: 15X



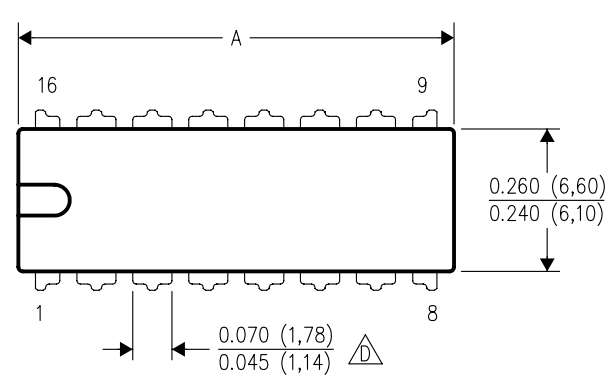
DETAIL B
13X, SCALE: 15X

4214771/A 05/2017

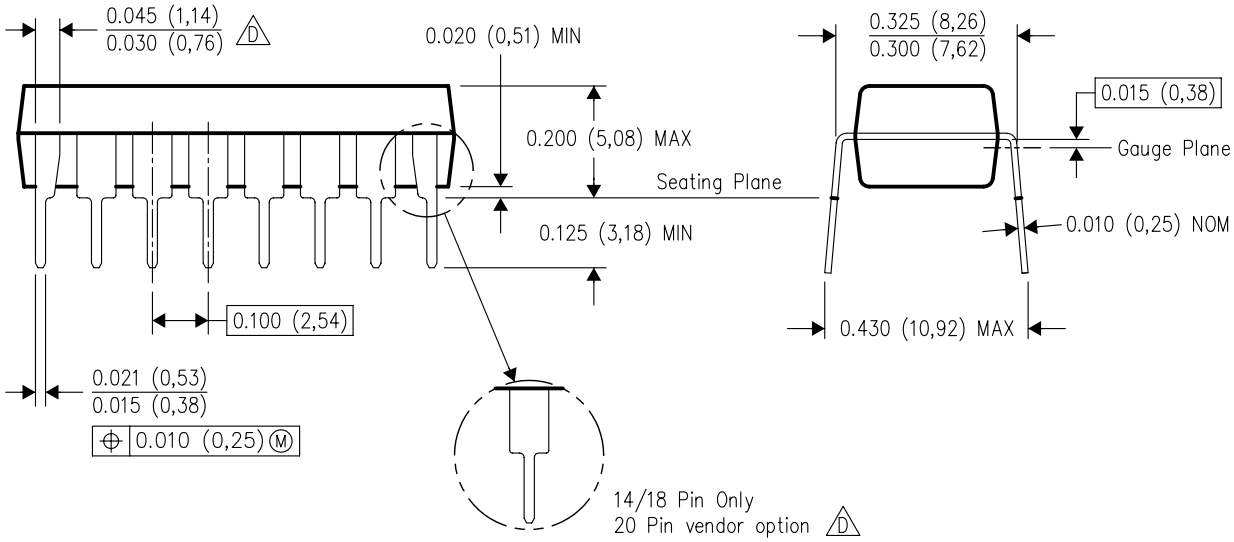
N (R–PDIP–T**)

PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN



DIM \ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS–001 VARIATION (C)	AA	BB	AC	AD



4040049/E 12/2002

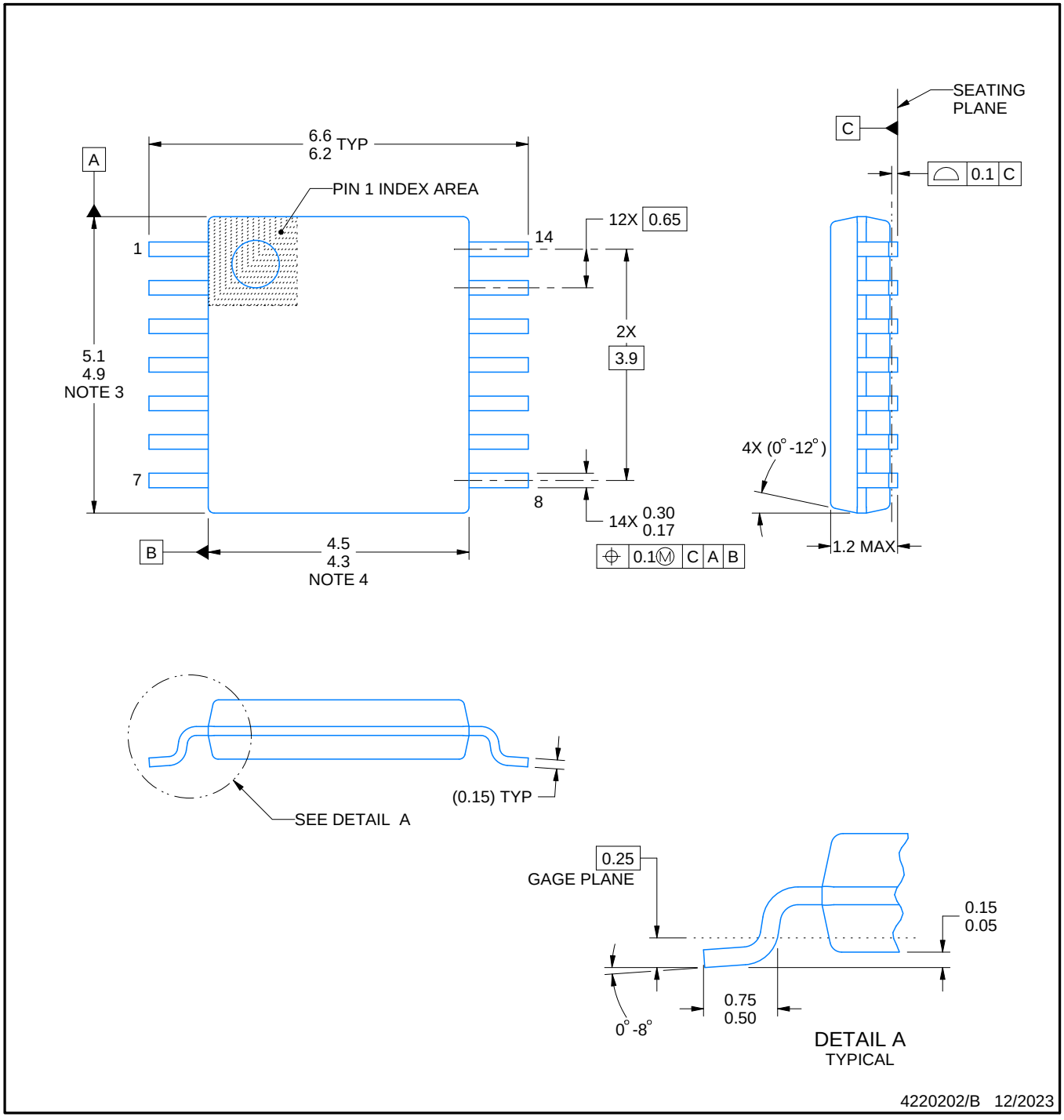
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

PACKAGE OUTLINE

PW0014A

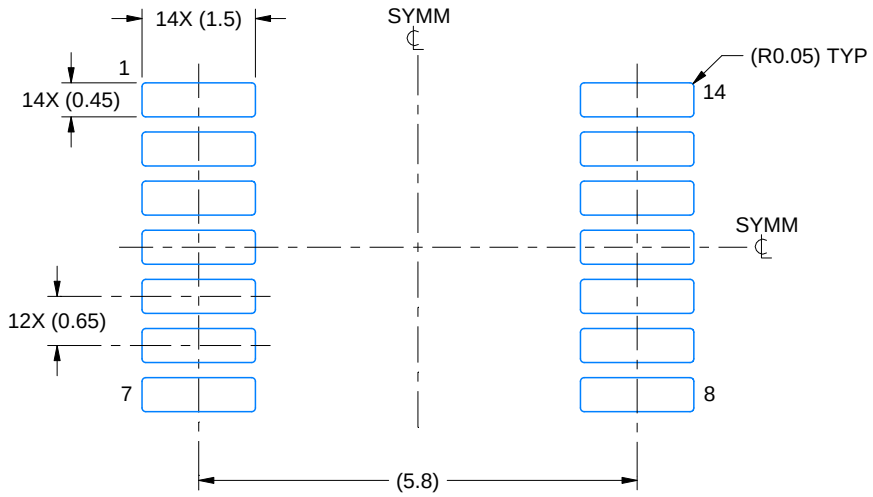
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

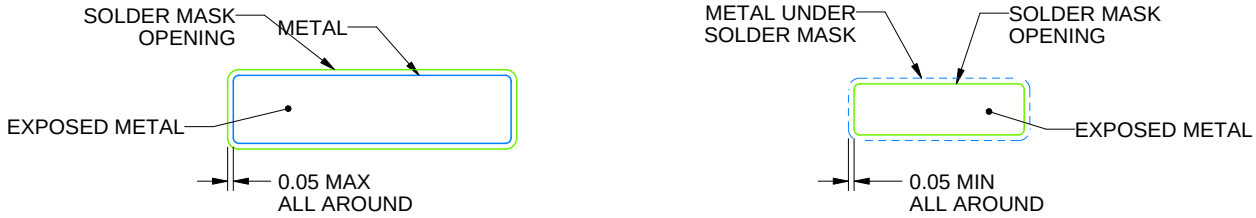


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

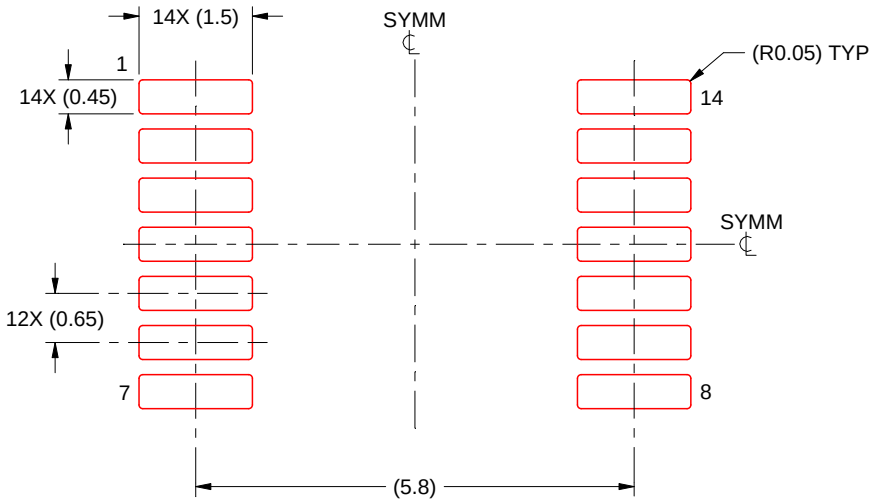


SOLDER MASK DETAILS

4220202/B 12/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220202/B 12/2023

NOTES: (continued)

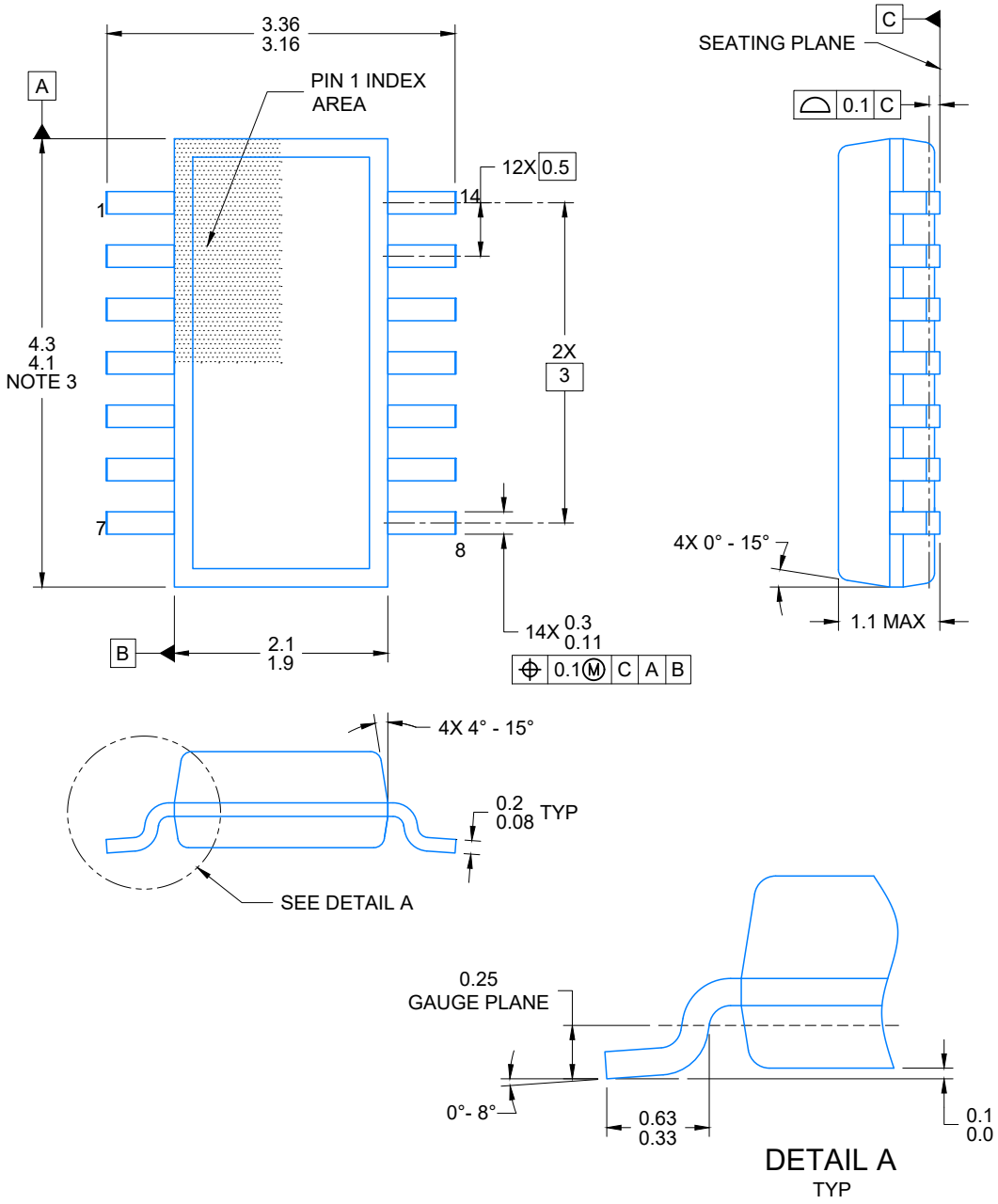
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

DYY0014A

SOT-23-THIN - 1.1 mm max height

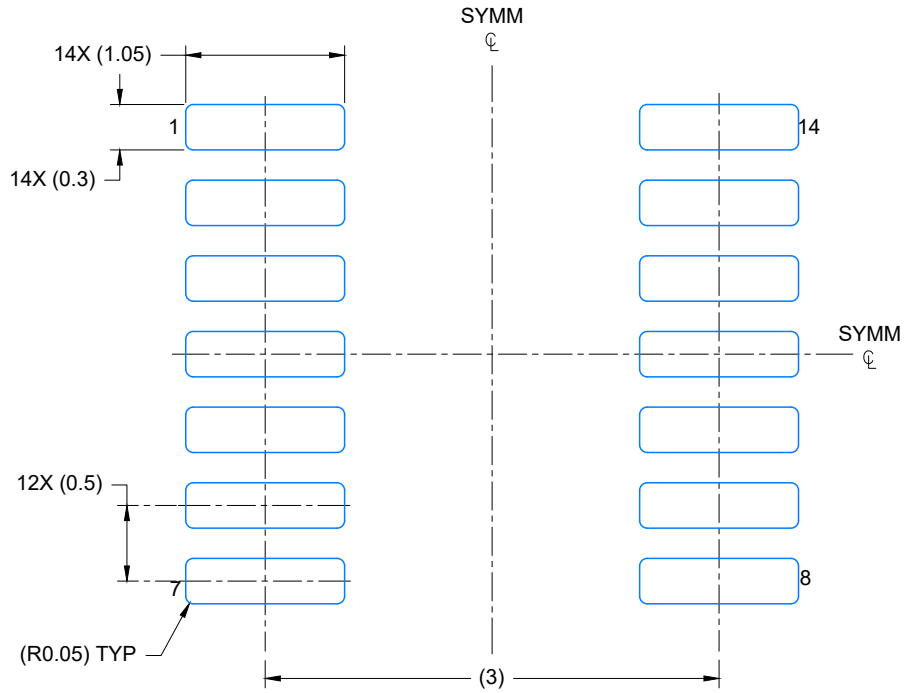
PLASTIC SMALL OUTLINE



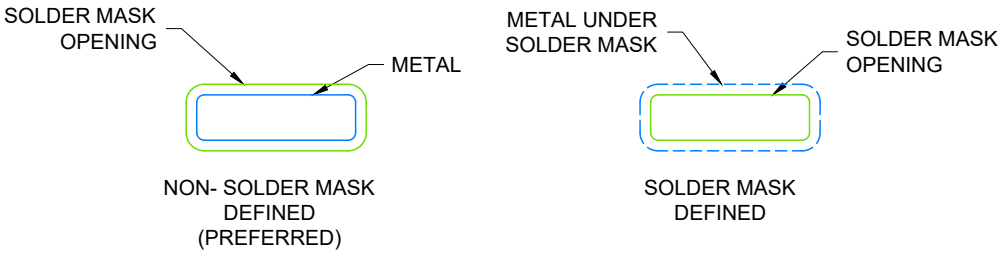
4224643/D 07/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
5. Reference JEDEC Registration MO-345, Variation AB



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 20X



SOLDER MASK DETAILS

4224643/D 07/2024

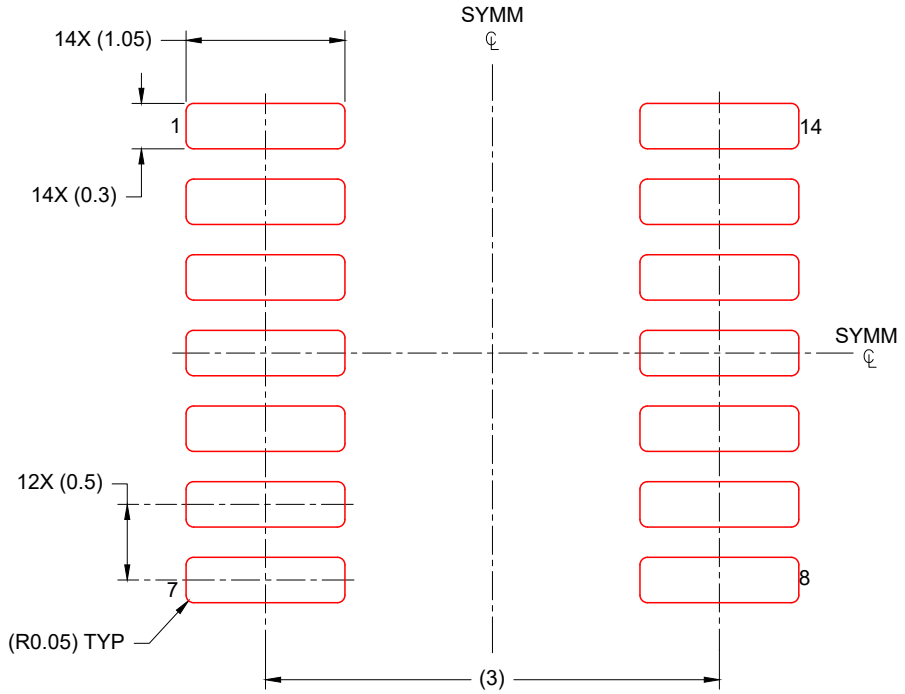
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

SOT-23-THIN - 1.1 mm max height

PLASTIC SMALL OUTLINE

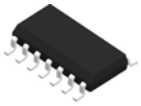


SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 20X

4224643/D 07/2024

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

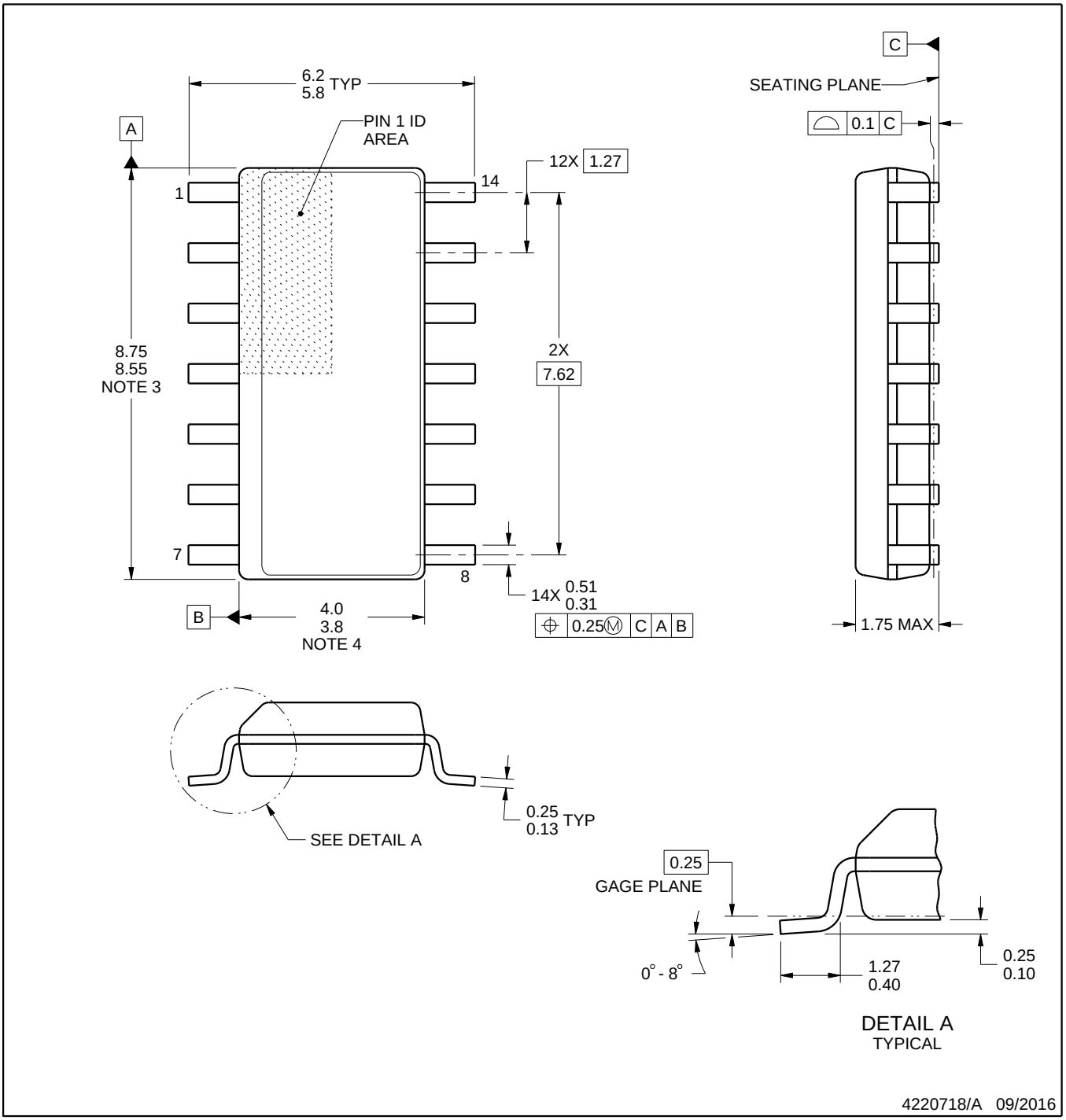


PACKAGE OUTLINE

D0014A

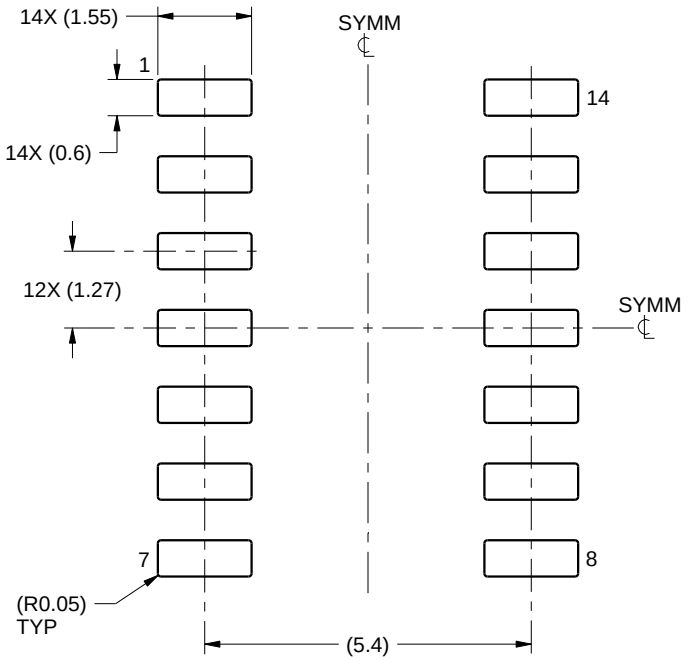
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

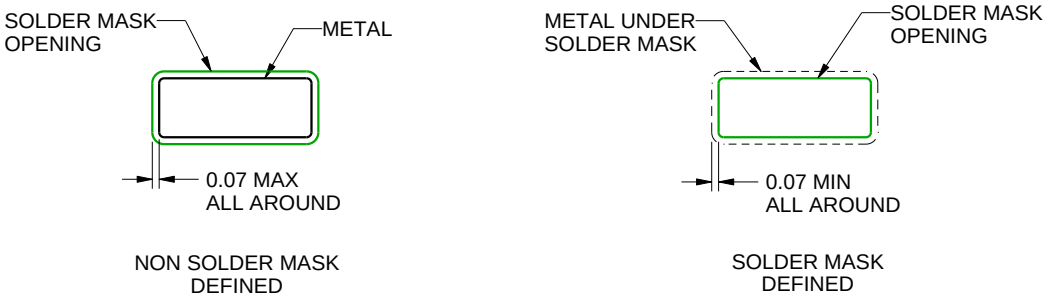


NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm, per side.
5. Reference JEDEC registration MS-012, variation AB.



LAND PATTERN EXAMPLE
SCALE:8X



SOLDER MASK DETAILS

4220718/A 09/2016

NOTES: (continued)

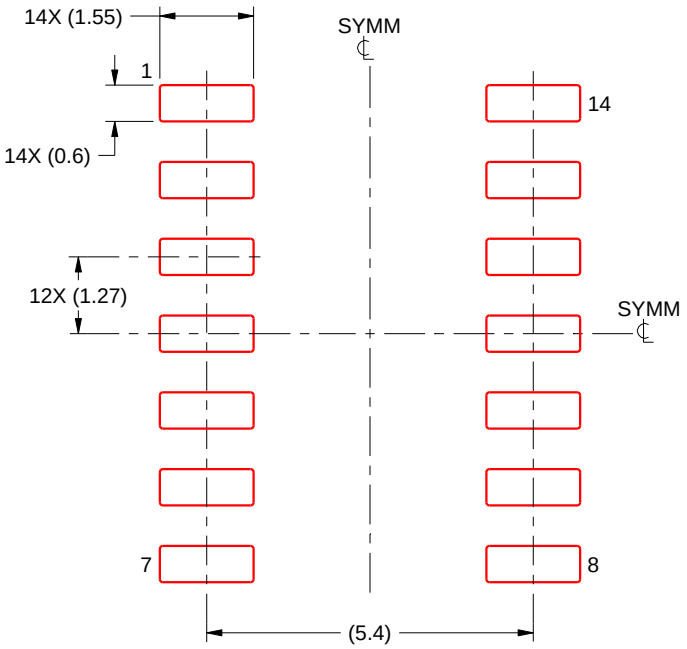
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:8X

4220718/A 09/2016

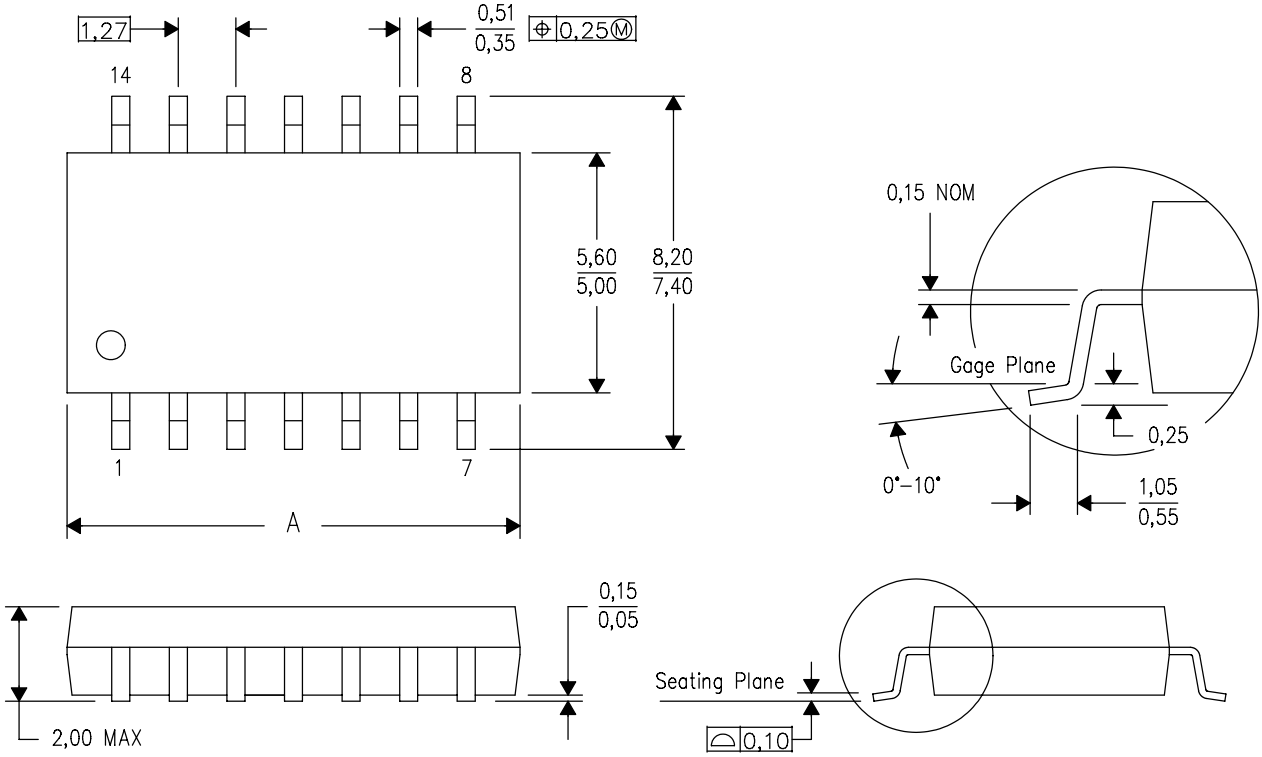
NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

MECHANICAL DATA

NS (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

14-PINS SHOWN



DIM \ PINS **	14	16	20	24
A MAX	10,50	10,50	12,90	15,30
A MIN	9,90	9,90	12,30	14,70

4040062/C 03/03

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

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