SNx4LVC86A 四路双输入异或门

1 特性

- 工作电压范围为 1.65V 至 3.6V
- 额定温度范围为 –40°C 至 85°C、–40°C 至 125°C 以及 –55°C 至 125°C
- 输入电压高达 5.5V
- 电压为 3.3V 时，t_{pd} 最大值为 4.6ns
- V_{OLP}（输出接地反弹）典型值 <0.8V（V_{CC} = 3.3V、T_A = 25°C）
- V_{OHV}（输出 V_{OH} 下冲）典型值 >2V（V_{CC} = 3.3V、T_A = 25°C）
- 闩锁性能超过 250mA，符合 JESD 17 规范
- ESD 保护性能超过 JESD 22 规范要求
  - 2000V 人体放电模型 (A114-A)
  - 1000V 充电器件模型 (C101)

2 应用

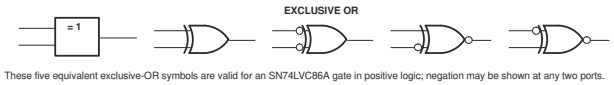
- AV 接收器
- 音频接口盒：便携式
- 蓝光播放器与家庭影院
- MP3 播放器或录音机
- 个人数字助理 (PDA)
- 电源：电信/服务器交流/直流电源：单路控制器：模拟式和数字式
- 固态硬盘 (SSD)：客户端和企业级
- 电视：LCD 电视、数字电视和高清电视 (HDTV)
- 平板电脑：企业级
- 视频分析：服务器
- 无线耳机、键盘和鼠标

3 说明

SN54LVC86A 四路双输入异或门可在 2.7V 至 3.6V V_{CC} 下运行，SN74LVC86A 四路双输入异或门可在 1.65V 至 3.6V V_{CC} 下运行。

器件型号	封装(1)	封装尺寸(2)	本体尺寸(3)
SNx4LVC86A	BQA（WQFN，14）	3mm × 2.5mm	3mm × 2.5mm
	RGY（VQFN，14）	3.50mm × 3.50mm	3.50mm × 3.50mm
	D（SOIC，14）	8.65mm x 6mm	8.65mm × 3.91mm
	NS（SOP，14）	10.2mm x 7.8mm	10.20mm × 5.30mm
	DB（SSOP，14）	6.2mm x 7.8mm	6.20mm × 5.30mm
	PW（TSSOP，14）	5mm x 6.4mm	5.00mm × 4.40mm
	W（CFP，14）	9.21mm × 9mm	9.21mm × 6.29mm
	FK（LCCC，20）	8.89mm × 8.89mm	8.89mm × 8.89mm

(1) 如需了解更多信息，请参阅机械、封装和可订购信息。
(2) 封装尺寸（长 × 宽）为标称值，并包括引脚（如适用）。
(3) 本体尺寸（长 x 宽）为标称值，不包括引脚。



These five equivalent exclusive-OR symbols are valid for an SN74LVC86A gate in positive logic; negation may be shown at any two ports.

异或逻辑

内容

4 引脚配置和功能

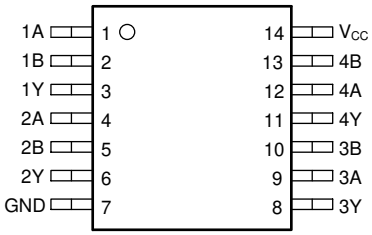


图 4-1. SN54LVC86A J 或 W 封装，14 引脚 CDIP 或 CFP；SN74LVC86A D、DB、NS 或 PW 封装，14 引脚 SOIC、SSOP、SOP 或 TSSOP（顶视图）

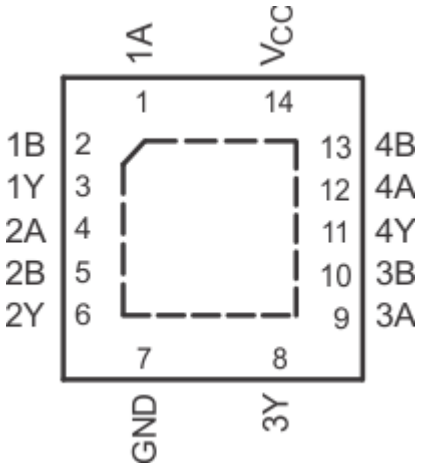


图 4-2. SN74LVC86A BQA 或 RGY 封装，14 引脚 WQFN 或 VQFN（顶视图）

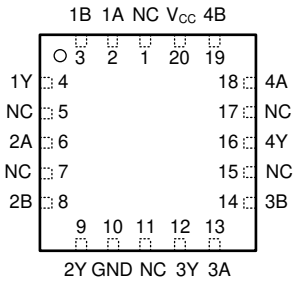


图 4-3. SN54LVC86A FK 封装，14 引脚 LCCC（顶视图）

表 4-1. 引脚功能

引脚			I/O	说明
编号	J、W、D、DB、NS、PW、RGY	FK		
	14 引脚	20 引脚		
1A	1	2	I	栅极 1 输入
1B	2	3	I	栅极 1 输入
1Y	3	4	O	栅极 1 输出
2A	4	6	I	栅极 2 输入
2B	5	8	I	栅极 2 输入
2Y	6	9	O	栅极 2 输出
3Y	8	12	O	栅极 3 输出
3A	9	13	I	栅极 3 输入
3B	10	14	I	栅极 3 输入
4Y	11	16	O	栅极 4 输出
4A	12	18	I	栅极 4 输入
4B	13	19	I	栅极 4 输入
GND	7	10	—	接地引脚
NC	—	1、5、7、11、15、17	—	不连接

表 4-1. 引脚功能（续）

引脚			I/O	说明
编号	J、W、D、DB、NS、PW、RGY	FK		
	14 引脚	20 引脚		
V_{CC}	14	20	—	电源引脚

5 规格

5.1 绝对最大额定值

在自然通风条件下的工作温度范围内测得（除非另有说明）

			最小值	最大值	单位
V_{CC}	电源电压范围		-0.5	6.5	V
V_I	输入电压范围(1)		-0.5	6.5	V
V_O	输出电压范围(1) (2)		-0.5	V_{CC} + 0.5	V
I_{IK}	输入钳位电流	V_I < 0		-50	mA
I_{OK}	输出钳位电流	V_O < 0		-50	mA
I_O	持续输出电流			±50	mA
	通过 V_{CC} 或 GND 的持续电流			±100	mA
P_{tot}	功率耗散	T_A = -40°C 至 125°C(3) (4)		500	mW
T_{stg}	贮存温度范围		-65	150	°C

(1) 如果遵守输入和输出电流额定值，有可能超过输入负电压和输出电压额定值。
(2) V_{CC} 的值在建议运行条件表中提供。
(3) 对于 D 封装：在 70°C 以上时，P_{tot} 值以 8mW/K 的幅度线性降额。
(4) 对于 DB、DGV、NS 和 PW 封装：在 60°C 以上时，P_{tot} 值以 5.5mW/K 的幅度线性降额。

5.2 ESD 等级

			值	单位
$V_{(ESD)}$	静电放电	人体放电模型 (HBM)，符合 ANSI/ESDA/JEDEC JS-001 标准，所有引脚(1)	±2000	V
		充电器件模型 (CDM)，符合 JEDEC 规范 JESD22-C101，所有引脚(2)	±1000	

(1) JEDEC 文档 JEP155 指出：500V HBM 能够在标准 ESD 控制流程下安全生产。
(2) JEDEC 文档 JEP157 指出：250V CDM 能够在标准 ESD 控制流程下安全生产。

5.3 建议运行条件，SN54LVC86A

在自然通风条件下的工作温度范围内测得（除非另有说明）

			SN54LVC86A		单位
			-55°C 至 125°C		
			最小值	最大值	
V_{CC}	电源电压	运行	2	3.6	V
		仅数据保留	1.5		
V_{IH}	高电平输入电压	V_{CC} = 2.7V 至 3.6V	2		V
V_{IL}	低电平输入电压	V_{CC} = 2.7V 至 3.6V		0.8	V
V_I	输入电压		0	5.5	V
V_O	输出电压		0	V_{CC}	V
I_{OH}	高电平输出电流	V_{CC} = 2.7V		-12	mA
		V_{CC} = 3V		-24	
I_{OL}	低电平输出电流	V_{CC} = 2.7V		12	mA
		V_{CC} = 3V		24	
Δt/Δv	输入转换上升或下降速率			9	ns/V

5.4 建议运行条件，SN74LVC86A

在自然通风条件下的工作温度范围内测得（除非另有说明）

			SN74LVC86A						单位
			T_A = 25°C		–40 至 85°C		–40 至 125°C		
			最小值	最大值	最小值	最大值	最小值	最大值	
V_{CC}	电源电压	运行	1.65	3.6	1.65	3.6	1.65	3.6	V
		仅数据保留	1.5		1.5		1.5		
V_{IH}	高电平输入电压	V_{CC} = 1.65V 至 1.95V	0.65 × V_{CC}		0.65 × V_{CC}		0.65 × V_{CC}		V
		V_{CC} = 2.3V 至 2.7V	1.7		1.7		1.7		
		V_{CC} = 2.7V 至 3.6V	2		2		2		
V_{IL}	低电平输入电压	V_{CC} = 1.65V 至 1.95V		0.35 × V_{CC}		0.35 × V_{CC}		0.35 × V_{CC}	V
		V_{CC} = 2.3V 至 2.7V		0.7		0.7		0.7	
		V_{CC} = 2.7V 至 3.6V		0.8		0.8		0.8	
V_I	输入电压		0	5.5	0	5.5	0	5.5	V
V_O	输出电压		0	V_{CC}	0	V_{CC}	0	V_{CC}	V
I_{OH}	高电平输出电流	V_{CC} = 1.65V		-4		-4		-4	mA
		V_{CC} = 2.3V		-8		-8		-8	
		V_{CC} = 2.7V		-12		-12		-12	
		V_{CC} = 3V		-24		-24		-24	
I_{OL}	低电平输出电流	V_{CC} = 1.65V		4		4		4	mA
		V_{CC} = 2.3V		8		8		8	
		V_{CC} = 2.7V		12		12		12	
		V_{CC} = 3V		24		24		24	
$\Delta t/\Delta v$	输入转换上升或下降速率			9		9		9	ns/V

5.5 热性能信息

热指标(1)		SN74LVC86A						单位
		BQA	D	DB	NS	PW	RGY	
		14 引脚	14 引脚	14 引脚	14 引脚	14 引脚	14 引脚	
$R_{\theta JA}$	结至环境热阻	102.3	127.8	96	123.8	150.8	92.1	°C/W

(1) 有关新旧热指标的更多信息，请参阅 *IC 封装热指标* 应用报告 SPRA953。

5.6 电气特性，SN54LVC86A

在自然通风条件下的工作温度范围内测得（除非另有说明）

参数	测试条件	V_{CC}	SN54LVC86A			单位
			-55°C 至 125°C			
			最小值	典型值	最大值	
V_{OH}	I_{OH} = -100 μA	2.7V 至 3.6V	V_{CC} – 0.2			V
	I_{OH} = -12mA	2.7V	2.2			
		3V	2.4			
	I_{OH} = -24mA	3V	2.2			
V_{OL}	I_{OL}=100 μA	2.7V 至 3.6V			0.2	V
	I_{OL} = 12mA	2.7V			0.4	
	I_{OL} = 24mA	3V			0.55	

在自然通风条件下的工作温度范围内测得（除非另有说明）

参数	测试条件		V_{CC}	SN54LVC86A -55°C 至 125°C 最小值 典型值 最大值	单位
I_I	V_I= 5.5V 或 GND		3.6V	±5	μA
I_{CC}	$V_I = V_{CC}$ 或 GND	I_O = 0	3.6V	10	μA
ΔI_{CC}	一个输入电压为 V_{CC} – 0.6V，其他输入电压为 V_{CC} 或 GND		2.7V 至 3.6V	500	μA
C_i	$V_I = V_{CC}$ 或 GND		3.3V	5(1)	pF

(1) T_A = 25°C

5.7 电气特性，SN74LVC86A

在自然通风条件下的工作温度范围内测得（除非另有说明）

参数	测试条件		V_{CC}	SN74LVC86A T_A = 25°C 最小值	典型值	最大值	-40°C 至 85°C 最小值	最大值	-40°C 至 125°C 最小值	最大值	单位
V_{OH}	I_{OH} = – 100 μA		1.65V 至 3.6V	V_{CC} – 0.2			V_{CC} – 0.2		V_{CC} – 0.3		V
	I_{OH} = -4mA		1.65V	1.29			1.2		1.05		
	I_{OH} = -8mA		2.3V	1.9			1.7		1.55		
	I_{OH} = -12mA		2.7V	2.2			2.2		2.05		
			3V	2.4			2.4		2.25		
	I_{OH} = -24mA		3V	2.3			2.2		2		
V_{OL}	I_{OL} = 100 μA		1.65V 至 3.6V			0.1		0.2		0.3	V
	I_{OL} = 4mA		1.65V			0.24		0.45		0.6	
	I_{OL} = 8mA		2.3V			0.3		0.7		0.75	
	I_{OL} = 12mA		2.7V			0.4		0.4		0.6	
	I_{OL} = 24mA		3V			0.55		0.55		0.8	
I_I	V_I=5.5V 或 GND		3.6V			±1		±5		±20	μA
I_{CC}	$V_I = V_{CC}$ 或 GND	I_O = 0	3.6V			1		10		40	μA
ΔI_{CC}	一个输入电压为 V_{CC} – 0.6V，其他输入电压为 V_{CC} 或 GND		2.7V 至 3.6V			500		500		5000	μA
C_i	$V_I = V_{CC}$ 或 GND		3.3V		5						pF

5.8 开关特性，SN54LVC86A

在自然通风条件下的建议工作温度范围内测得（除非另有说明）（请参阅负载电路和电压波形）

参数	从（输入）	至（输出）	V_{CC}	SN54LVC86A -55°C 至 125°C 最小值	最大值	单位
t_{pd}	A	Y	2.7V		5.6	ns
			3.3V ± 0.3V	1	4.6	

5.9 开关特性，SN74LVC86A

在自然通风条件下的建议工作温度范围内测得（除非另有说明）（请参阅负载电路和电压波形）

参数	从（输入）	至（输出）	V_{CC}	SN74LVC86A							单位
				T_A = 25°C			-40°C 至 85°C		-40°C 至 125°C		
				最小值	典型值	最大值	最小值	最大值	最小值	最大值	
t_{pd}	A	Y	1.8V ± 0.15V	1	4.1	9.4	1	9.9	1	11.4	ns
			2.5V ± 0.2V	1	2.9	7.1	1	7.6	1	9.7	
			2.7V	1	2.8	5.4	1	5.6	1	7.1	
			3.3V ± 0.3V	1	2.5	4.4	1	4.6	1	5.8	
$t_{sk(o)}$			3.3V ± 0.3V					1		1.5	ns

5.10 工作特性

T_A = 25°C

参数		测试条件	V_{CC}	典型值	单位
C_{pd}	每个栅极的功率耗散电容	f = 10MHz	1.8V	6.5	pF
			2.5V	7.5	
			3.3V	8.5	

5.11 典型特性

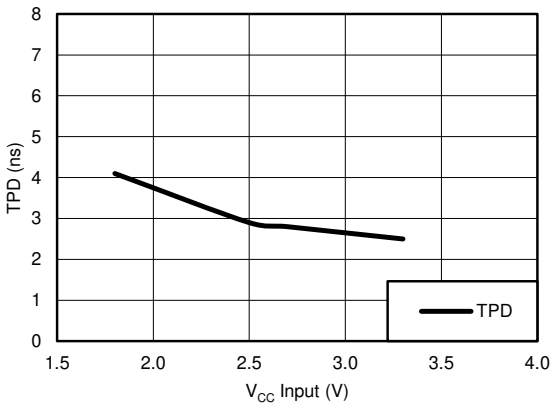


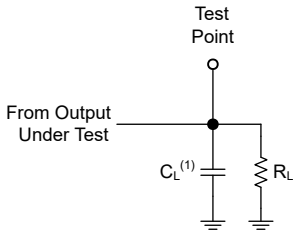
图 5-1. TPD 与 V_{CC} 间的关系 (T_A = 25°C)

6 参数测量信息

对于下表中列出的示例，波形之间的相位关系是任意选择的。所有输入脉冲均由具有以下特性的发生器提供：PRR ≤ 1MHz，Z_O = 50Ω，t_t ≤ 2.5ns。

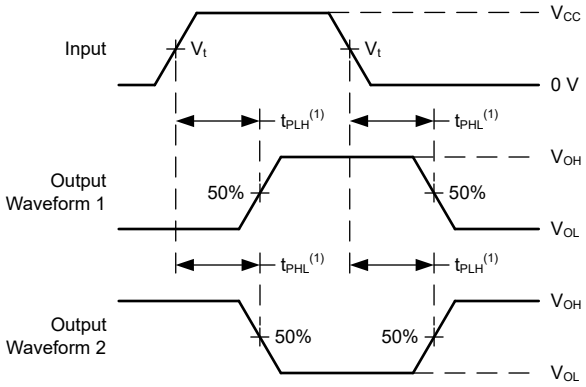
输出单独测量，每次测量一个输入转换。

V_{CC}	V_t	R_L	C_L	Δ V
1.8V ± 0.15V	V_{CC}/2	1kΩ	30pF	0.15V
2.5V ± 0.2V	V_{CC}/2	500Ω	30pF	0.15V
2.7V	1.5V	500Ω	50pF	0.3V
3.3V ± 0.3V	1.5V	500Ω	50pF	0.3V



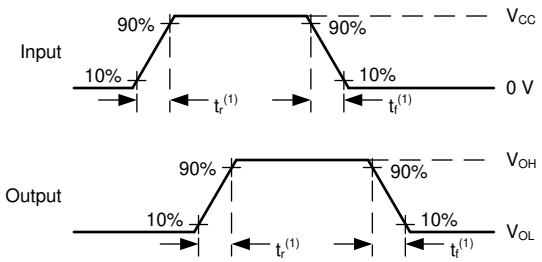
(1) C_L 包括探头和测试夹具电容。

图 6-1. 推挽输出的负载电路



(1) t_{PLH} 和 t_{PHL} 之间的较大者与 t_{pd} 相同。

图 6-2. 电压波形传播延迟



(1) t_r 和 t_f 之间的较大值与 t_t 相同。

图 6-3. 电压波形，输入和输出转换时间

7 详细说明

7.1 概述

'LVC86A 器件以正逻辑执行布尔函数 $Y = A \oplus B$ 或 $Y = \overline{A}B + A\overline{B}$。

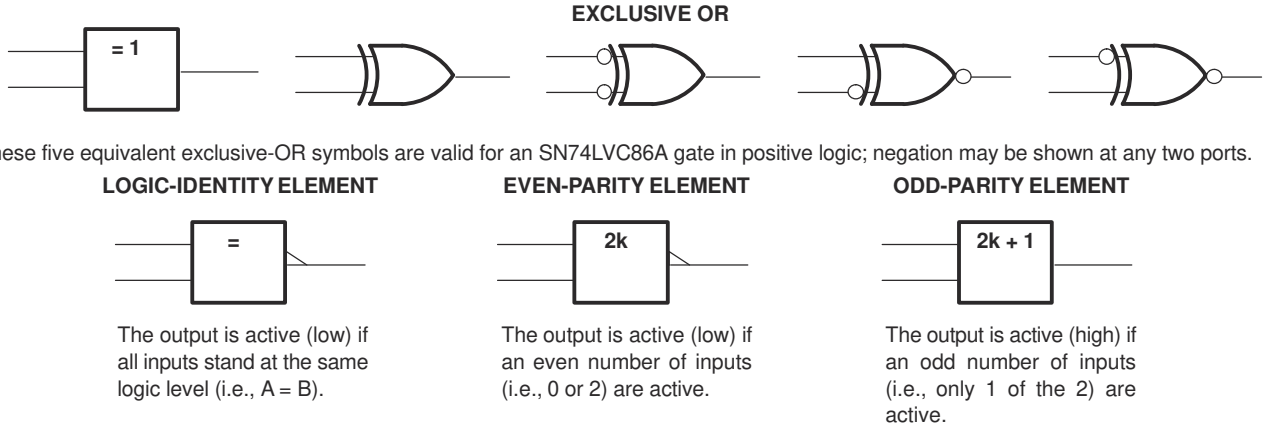
常用作真/补元件。如果一个输入为低电平，则可在输出时重新生成真实形态的其他输入。如果一个输入为高电平，另一个输入的信号则可在输出时重新生成反向信号。

输入可以由 3.3V 或 5V 器件驱动。此功能允许在 3.3V/5V 的混合系统环境中将此类器件用作降压转换器。

7.2 功能方框图

异或逻辑

异或门具有许多应用，可用其他逻辑符号更好地表示其中部分应用。



7.3 特性说明

- 宽工作电压范围
  - 工作电压范围为 1.65V 至 3.6V
- 支持升压或降压转换
  - 输入和输出支持高达 5.5V 电压

7.4 器件功能模式

表 7-1. 功能表
(每个逻辑门)

输入		输出
A	B	Y
L	L	L
L	H	H
H	L	H
H	H	L

8 应用和实施

8.1 应用信息

SN74LVC86A 器件是一款高驱动、开漏 CMOS 器件，可用于多种缓冲器类型的功能。该器件可以在 3V 下产生 24mA 驱动电流，因此非常适合驱动多个输入，也适合用于高达 100MHz 的高速应用。输入和输出可承受 5.5V 电压，因此该器件可转换高达 5.5V 或低至 V_{CC} 的电压。

8.2 典型应用

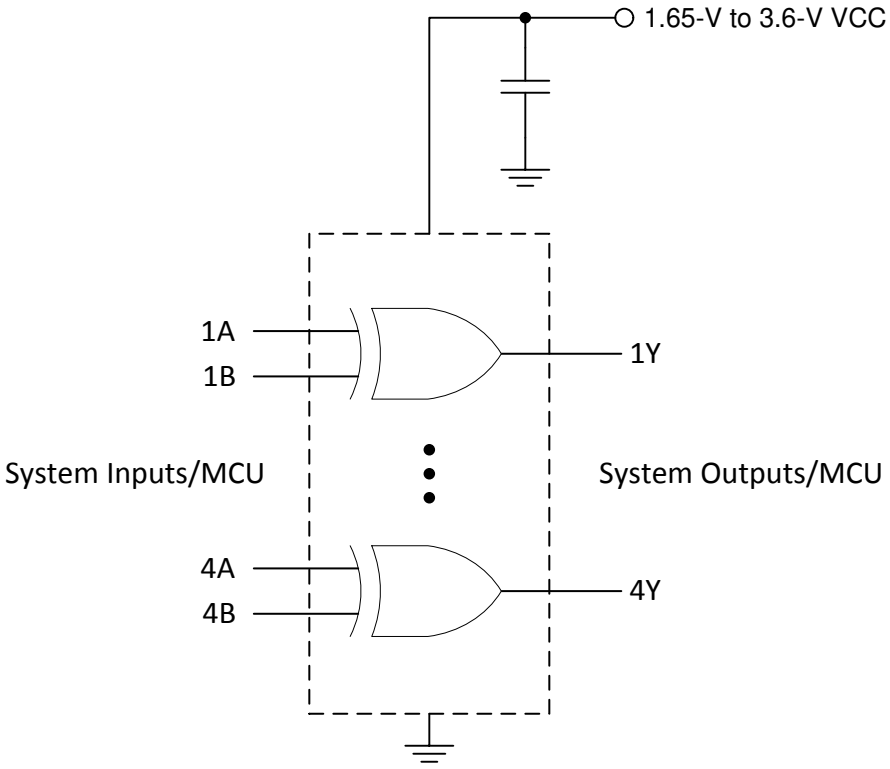


图 8-1. 典型或门应用和电源电压

8.2.1 设计要求

此器件采用 CMOS 技术并具有平衡输出驱动。注意避免总线争用，因为它可以驱动超过最大限制的电流。高驱动也会在轻负载时产生快速边缘，因此应考虑布线和负载条件以防止振铃。

8.2.2 详细设计过程

1. 建议的输入条件
   - 上升时间和下降时间规格：请参阅 *节 5.3* 中的 ($\Delta t/\Delta V$)。
   - 指定的高电平和低电平：请参阅 *节 5.3* 表中的 (V_{IH} 和 V_{IL}) 。
   - 输入具有过压容限，允许它们在任何有效 V_{CC} 下高达 5.5V。
2. 建议的输出条件
   - 每个输出的负载电流不应超过 25mA，该器件的总电流不应超过 50mA。
   - 输出不应被拉至高于 5.5V。

8.2.3 应用曲线

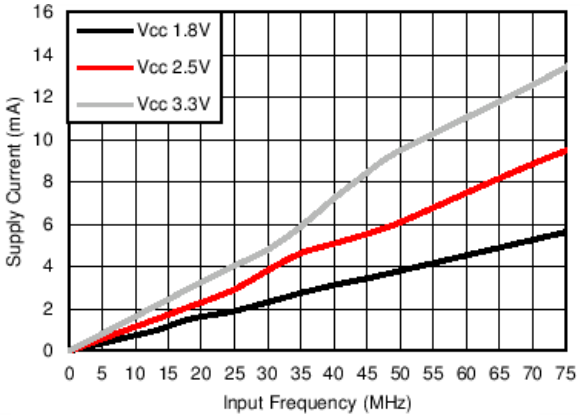


图 8-2. 电源电流与输入频率间的关系

电源相关建议

电源可以是 *节 5.3* 表中最小和最大电源电压额定值之间的任意电压。

每个 V_{CC} 引脚应具有一个良好的旁路电容器，以防止功率干扰。对于单电源器件，建议使用 0.1 µf；如果有多个 V_{CC} 引脚，则建议每个电源引脚使用 0.01 µf 或 0.022 µf。可以并联多个旁路电容器以抑制不同的噪声频率。0.1 µf 和 1 µf 通常并联使用。为了获得更佳效果，旁路电容器应尽可能靠近电源引脚安装。

8.3 布局

8.3.1 布局指南

当使用多位逻辑器件时，输入不应悬空。

在许多情况下，数字逻辑器件的功能或部分功能未被使用（例如，当仅使用三输入与门的两个输入或仅使用 4 个缓冲门中的 3 个时）。此类输入引脚不应悬空，因为外部连接处的未定义电压会导致未定义的操作状态。节 8.3.2 指定了在所有情况下都必须遵守的规则。数字逻辑器件的所有未使用输入必须连接至一个高或低偏置以防止悬空。应为任何特定未使用输入应用的逻辑电平取决于器件的功能。通常，它们将连接到 GND 或 V_{CC}，具体取决于哪种更合理或更方便。使输出悬空是可以接受的，除非该器件是收发器。

8.3.2 布局示例

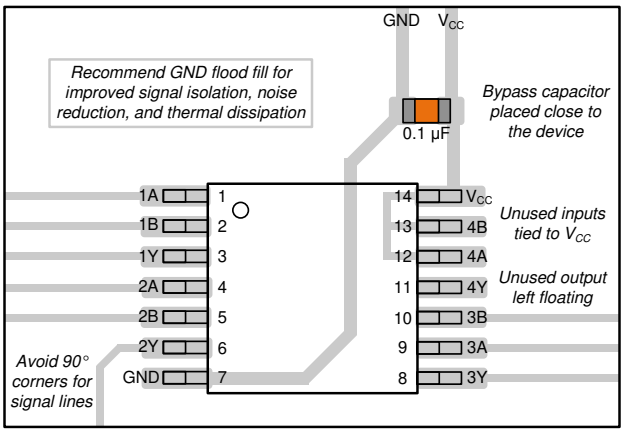


图 8-3. SN74LVC86A 的示例布局

9 器件和文档支持

9.1 文档支持（模拟）

9.1.1 相关链接

下表列出了快速访问链接。类别包括技术文档、支持和社区资源、工具和软件，以及申请样片或购买产品的快速链接。

表 9-1. 相关链接

器件	产品文件夹	样片 & 购买	技术文档	工具 & 软件	支持 & 社区
SN54LVC86A	点击此处	点击此处	点击此处	点击此处	点击此处
SN74LVC86A	点击此处	点击此处	点击此处	点击此处	点击此处

9.2 接收文档更新通知

要接收文档更新通知，请导航至 ti.com 上的器件产品文件夹。点击*通知* 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

9.3 支持资源

TI E2E™ 中文支持论坛是工程师的重要参考资料，可直接从专家处获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题，获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的使用条款。

9.4 商标

TI E2E™ is a trademark of Texas Instruments.
所有商标均为其各自所有者的财产。

9.5 静电放电警告

静电放电 (ESD) 会损坏这个集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

9.6 术语表

TI 术语表　　本术语表列出并解释了术语、首字母缩略词和定义。

10 修订历史记录

注：以前版本的页码可能与当前版本的页码不同

Changes from Revision Q (May 2024) to Revision R (August 2024)	Page
• 更新了 $R_{\theta JA}$ 值：D 封装从 86 更新为 127.8，NS 封装从 76 更新为 123.8，PW 封装从 113 更新为 150.8，RGY 封装从 47 更新为 92.1，所有值均以 °C/W 为单位	6

Changes from Revision P (April 2005) to Revision Q (April 2024)	Page
• 添加了*器件信息* 表、*引脚功能* 表、*ESD 等级* 表、*热性能信息* 表、*器件功能模式*、“应用和实施”部分、*器件和文档支持* 部分以及*机械、封装和可订购信息* 部分	1
• 删除了对机器放电模型的引用	1
• 向*器件信息* 表、*引脚配置和功能* 部分以及*热性能信息* 表中添加了 BQA 封装	1

11 机械、封装和可订购信息

以下页面包含机械、封装和可订购信息。这些信息是指定器件的最新可用数据。数据如有变更，恕不另行通知，且不会对此文档进行修订。有关此数据表的浏览器版本，请查阅左侧的导航栏。

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
5962-9761901Q2A	ACTIVE	LCCC	FK	20	55	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-9761901Q2A SNJ54LVC 86AFK	Samples
5962-9761901QDA	ACTIVE	CFP	W	14	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-9761901QD A SNJ54LVC86AW	Samples
SN74LVC86ABQAR	ACTIVE	WQFN	BQA	14	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LVC86A	Samples
SN74LVC86AD	ACTIVE	SOIC	D	14	50	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LVC86A	Samples
SN74LVC86ADBR	ACTIVE	SSOP	DB	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LC86A	Samples
SN74LVC86ADG4	ACTIVE	SOIC	D	14	50	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LVC86A	Samples
SN74LVC86ADR	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LVC86A	Samples
SN74LVC86ADRG4	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LVC86A	Samples
SN74LVC86ADT	ACTIVE	SOIC	D	14	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LVC86A	Samples
SN74LVC86ANSR	ACTIVE	SOP	NS	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LVC86A	Samples
SN74LVC86APW	ACTIVE	TSSOP	PW	14	90	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LC86A	Samples
SN74LVC86APWE4	ACTIVE	TSSOP	PW	14	90	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LC86A	Samples
SN74LVC86APWG4	ACTIVE	TSSOP	PW	14	90	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LC86A	Samples
SN74LVC86APWR	ACTIVE	TSSOP	PW	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LC86A	Samples
SN74LVC86APWRG4	ACTIVE	TSSOP	PW	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LC86A	Samples
SN74LVC86ARGYR	ACTIVE	VQFN	RGY	14	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	LC86A	Samples
SN74LVC86ARGYRG4	ACTIVE	VQFN	RGY	14	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	LC86A	Samples
SNJ54LVC86AFK	ACTIVE	LCCC	FK	20	55	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-9761901Q2A	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
										SNJ54LVC 86AFK	
SNJ54LVC86AW	ACTIVE	CFP	W	14	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-9761901QD A SNJ54LVC86AW	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

OTHER QUALIFIED VERSIONS OF SN54LVC86A, SN74LVC86A :

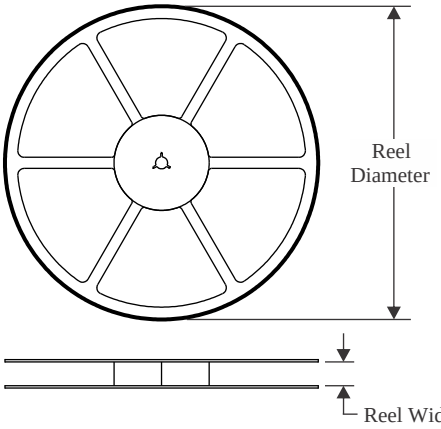
- Catalog : SN74LVC86A
- Automotive : SN74LVC86A-Q1, SN74LVC86A-Q1
- Enhanced Product : SN74LVC86A-EP, SN74LVC86A-EP
- Military : SN54LVC86A

NOTE: Qualified Version Definitions:

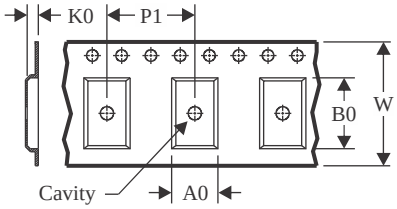
- Catalog - TI's standard catalog product
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects
- Enhanced Product - Supports Defense, Aerospace and Medical Applications
- Military - QML certified for Military and Defense Applications

TAPE AND REEL INFORMATION

REEL DIMENSIONS

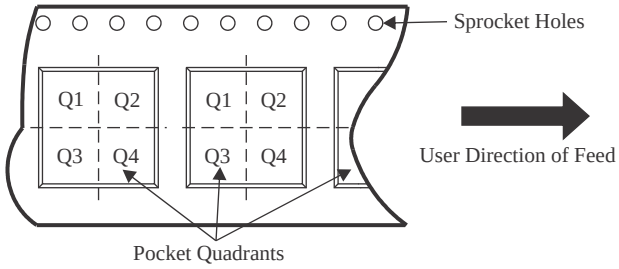


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

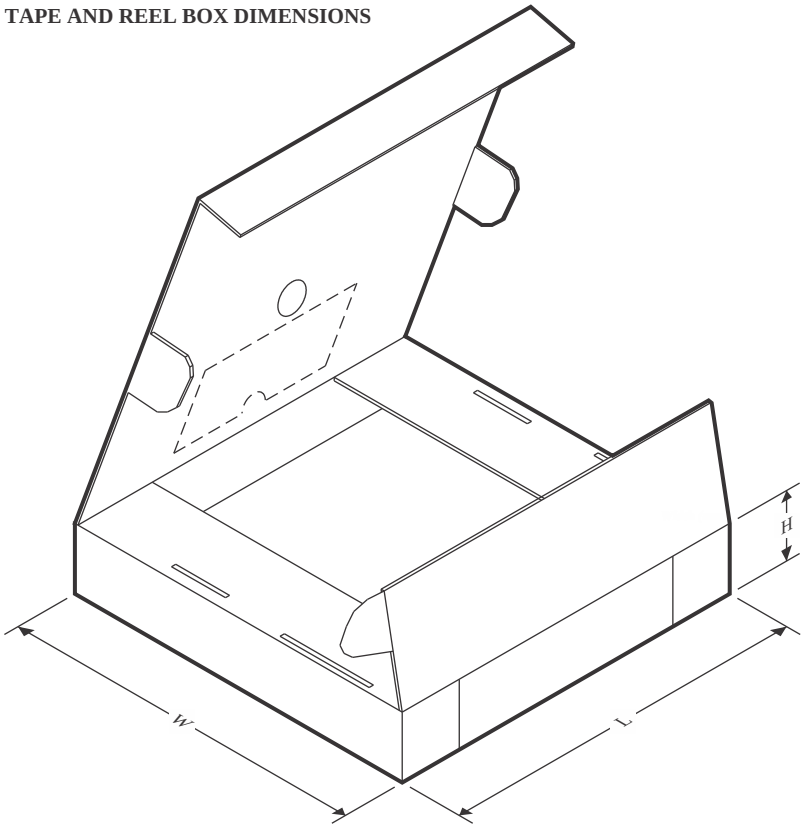
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LVC86ABQAR	WQFN	BQA	14	3000	180.0	12.4	2.8	3.3	1.1	4.0	12.0	Q1
SN74LVC86ADBR	SSOP	DB	14	2000	330.0	16.4	8.35	6.6	2.4	12.0	16.0	Q1
SN74LVC86ADR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
SN74LVC86ADT	SOIC	D	14	250	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
SN74LVC86ANSR	SOP	NS	14	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1
SN74LVC86APWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74LVC86ARGYR	VQFN	RGY	14	3000	330.0	12.4	3.75	3.75	1.15	8.0	12.0	Q1

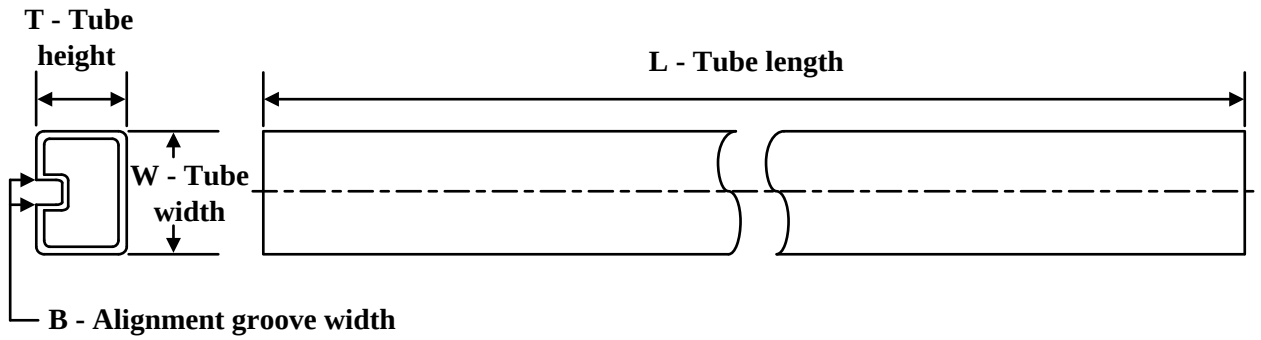
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LVC86ABQAR	WQFN	BQA	14	3000	210.0	185.0	35.0
SN74LVC86ADBR	SSOP	DB	14	2000	356.0	356.0	35.0
SN74LVC86ADR	SOIC	D	14	2500	356.0	356.0	35.0
SN74LVC86ADT	SOIC	D	14	250	210.0	185.0	35.0
SN74LVC86ANSR	SOP	NS	14	2000	356.0	356.0	35.0
SN74LVC86APWR	TSSOP	PW	14	2000	356.0	356.0	35.0
SN74LVC86ARGYR	VQFN	RGY	14	3000	356.0	356.0	35.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
5962-9761901Q2A	FK	LCCC	20	55	506.98	12.06	2030	NA
SN74LVC86AD	D	SOIC	14	50	506.6	8	3940	4.32
SN74LVC86ADG4	D	SOIC	14	50	506.6	8	3940	4.32
SN74LVC86APW	PW	TSSOP	14	90	530	10.2	3600	3.5
SN74LVC86APWE4	PW	TSSOP	14	90	530	10.2	3600	3.5
SN74LVC86APWG4	PW	TSSOP	14	90	530	10.2	3600	3.5
SNJ54LVC86AFK	FK	LCCC	20	55	506.98	12.06	2030	NA

GENERIC PACKAGE VIEW

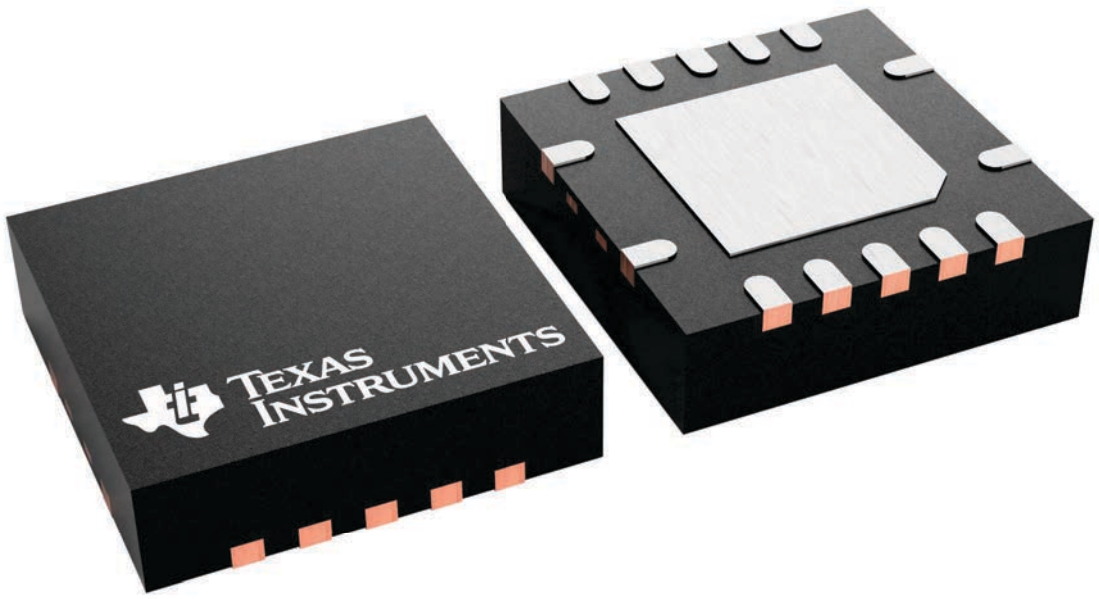
RGY 14

VQFN - 1 mm max height

3.5 x 3.5, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



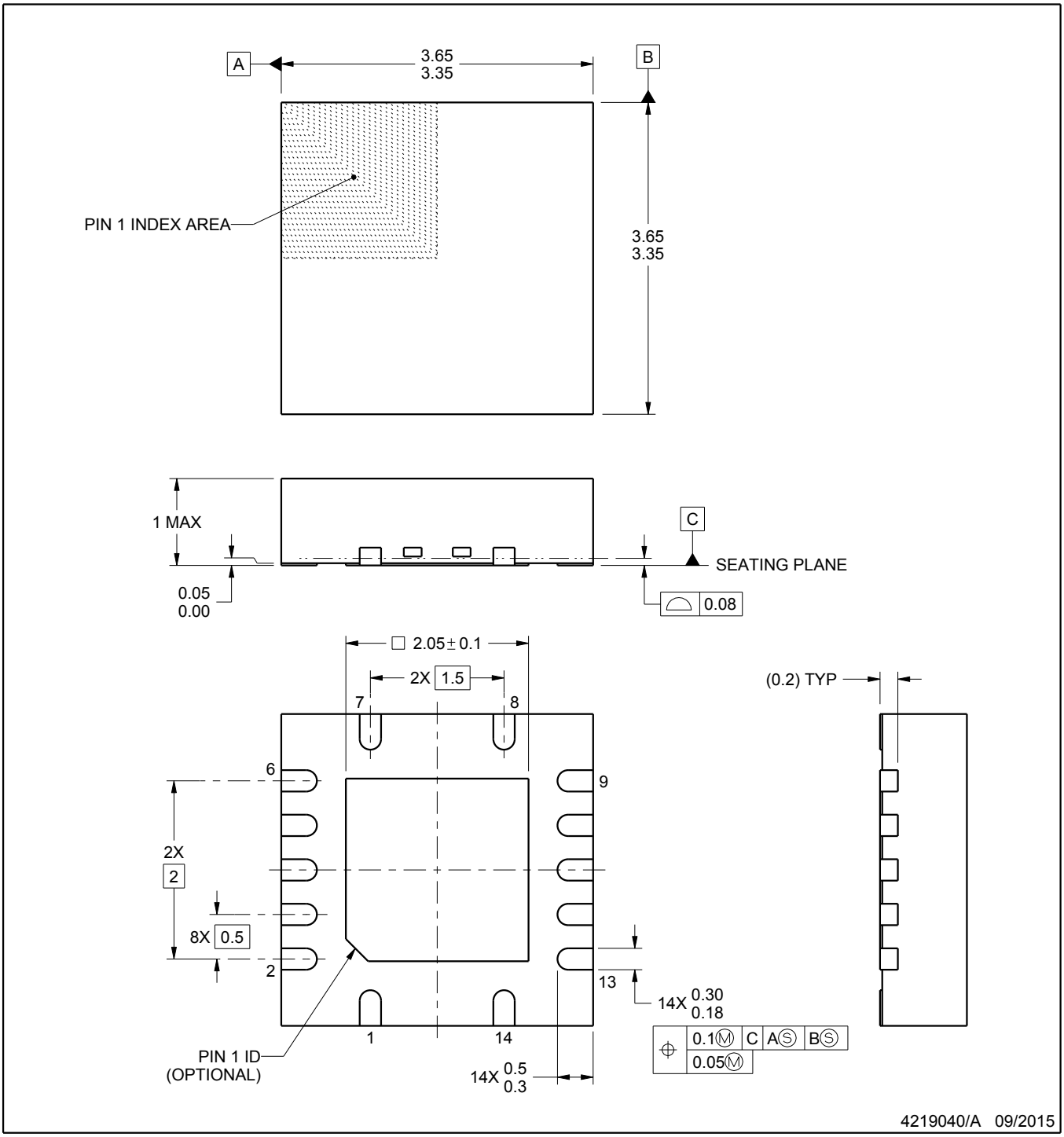
4231541/A

PACKAGE OUTLINE

RGY0014A

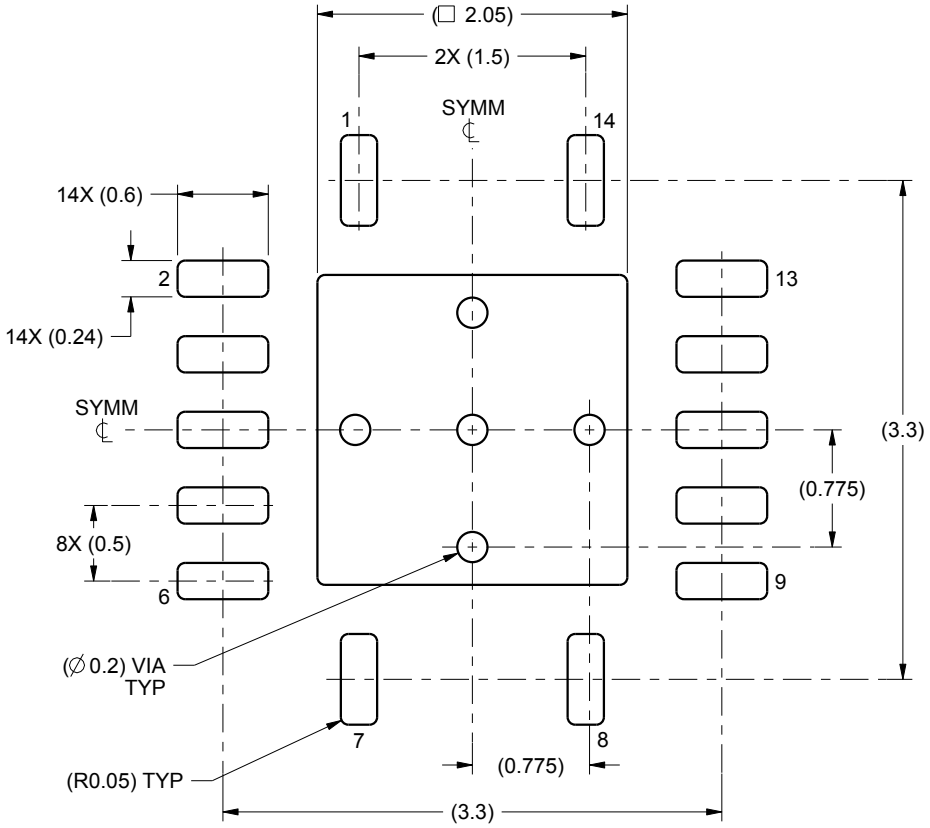
VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

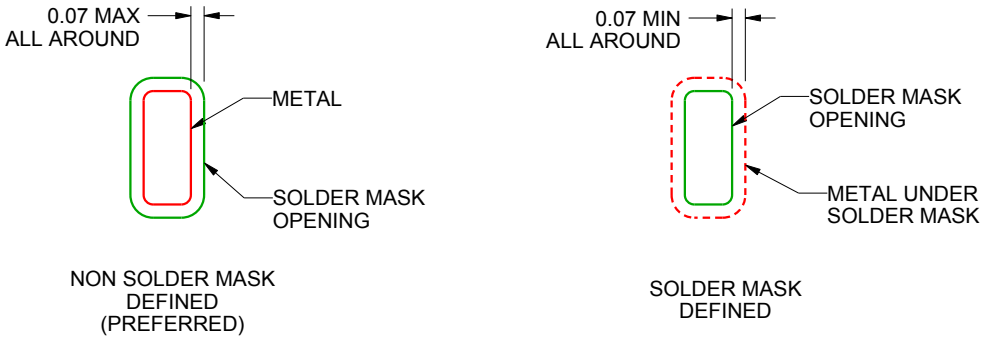


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
SCALE:20X

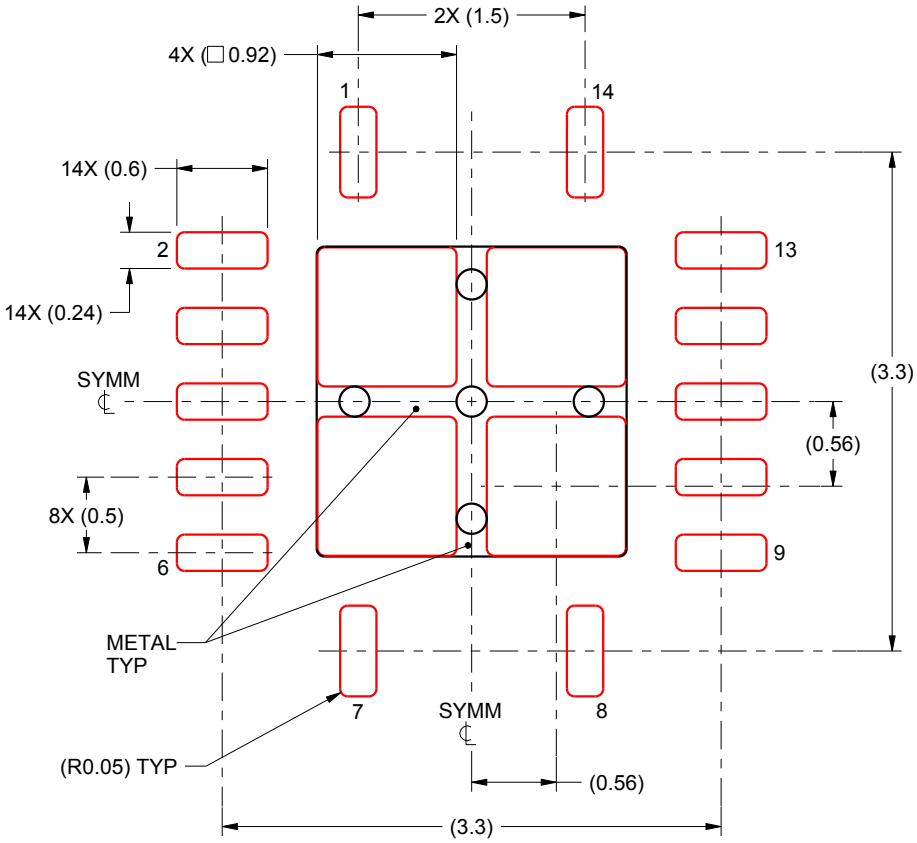


SOLDER MASK DETAILS

4219040/A 09/2015

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).



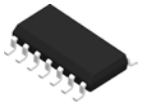
SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
80% PRINTED SOLDER COVERAGE BY AREA
SCALE:20X

4219040/A 09/2015

NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

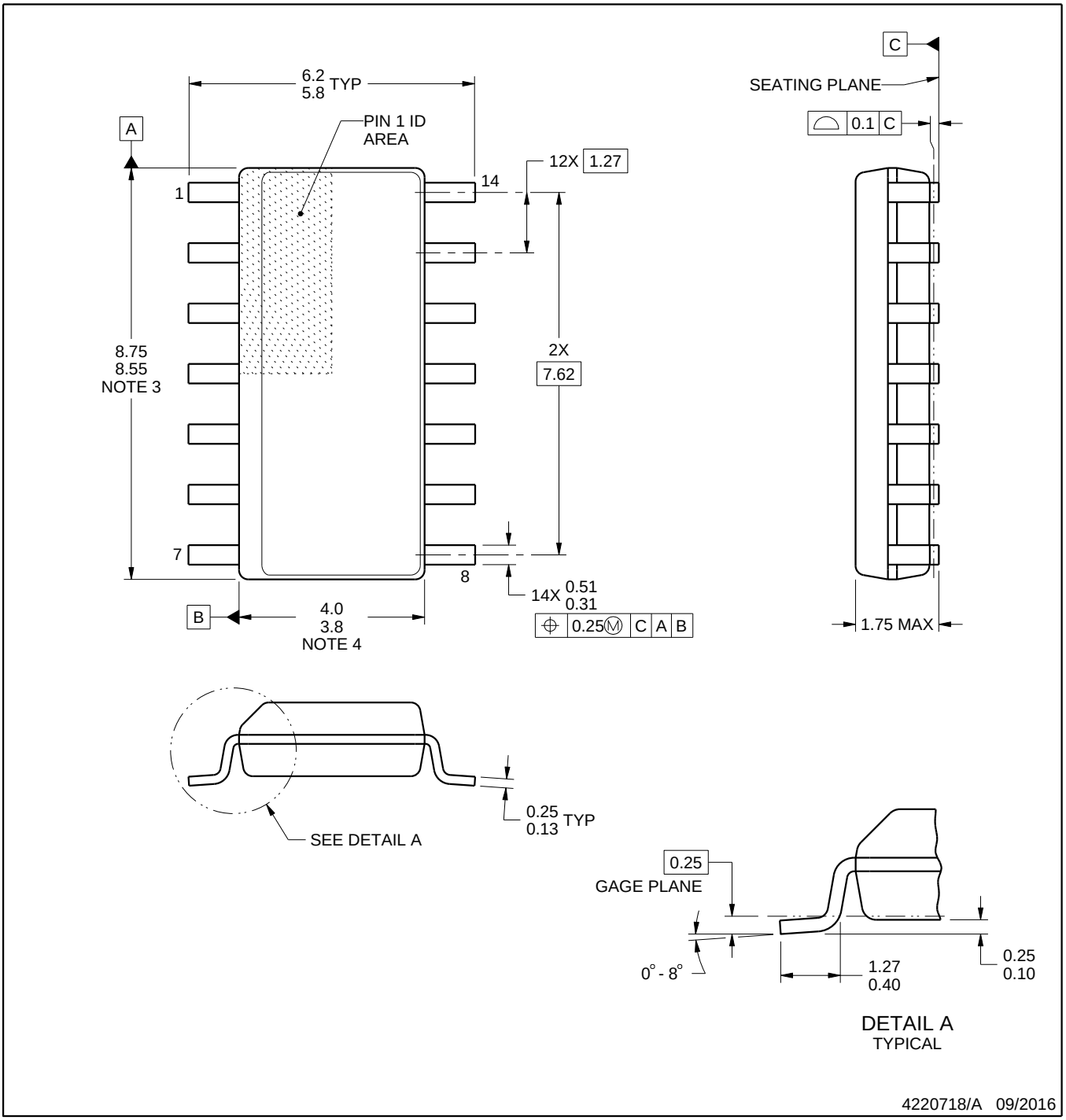


PACKAGE OUTLINE

D0014A

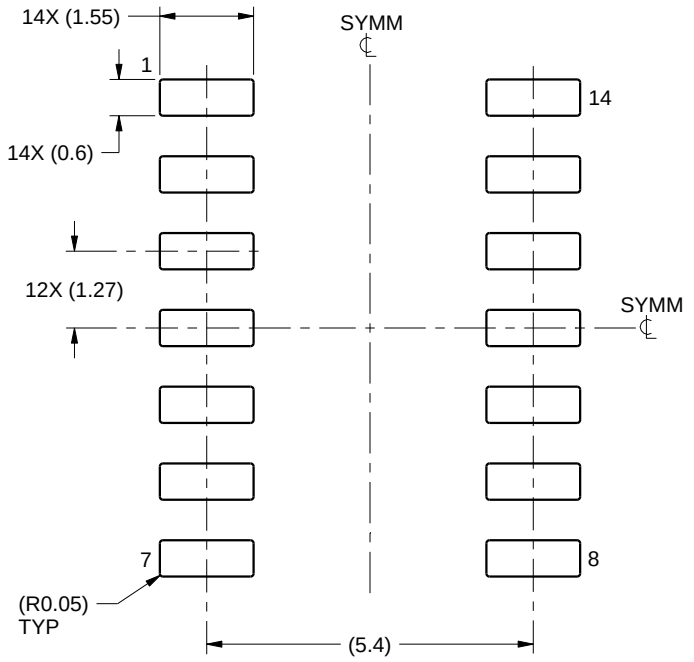
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

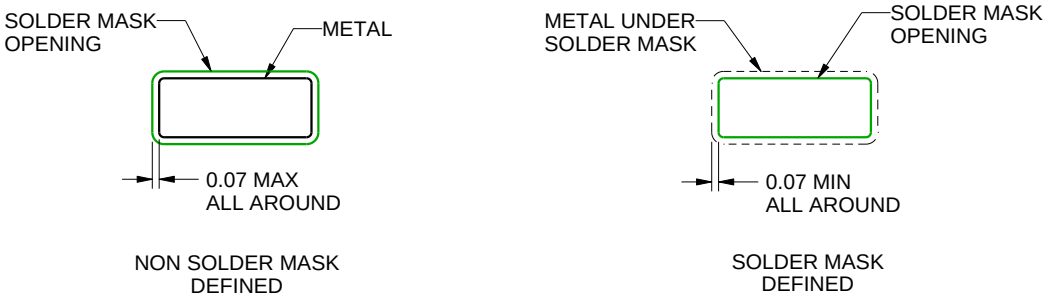


NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm, per side.
5. Reference JEDEC registration MS-012, variation AB.



LAND PATTERN EXAMPLE
SCALE:8X



SOLDER MASK DETAILS

4220718/A 09/2016

NOTES: (continued)

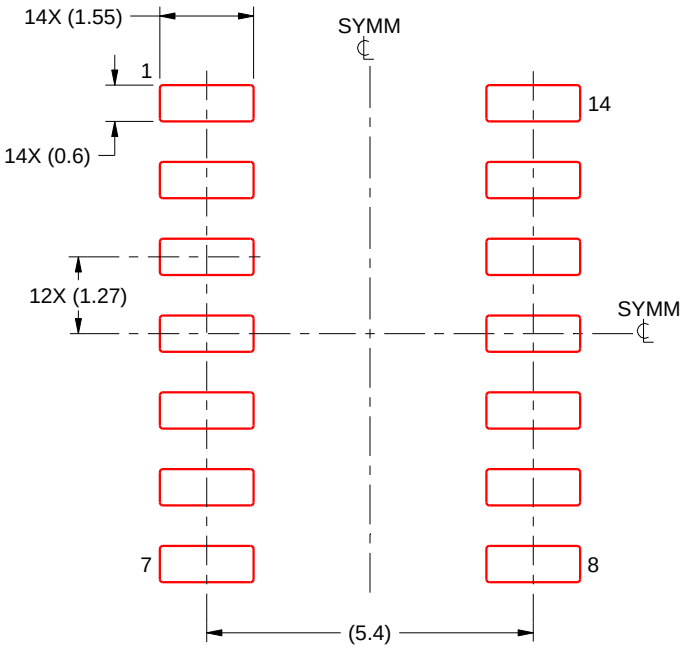
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:8X

4220718/A 09/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

GENERIC PACKAGE VIEW

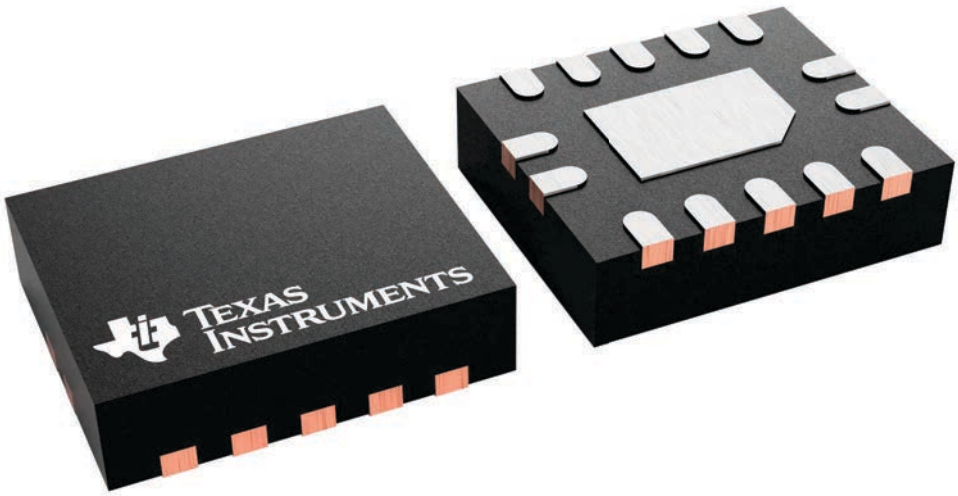
BQA 14

WQFN - 0.8 mm max height

2.5 x 3, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

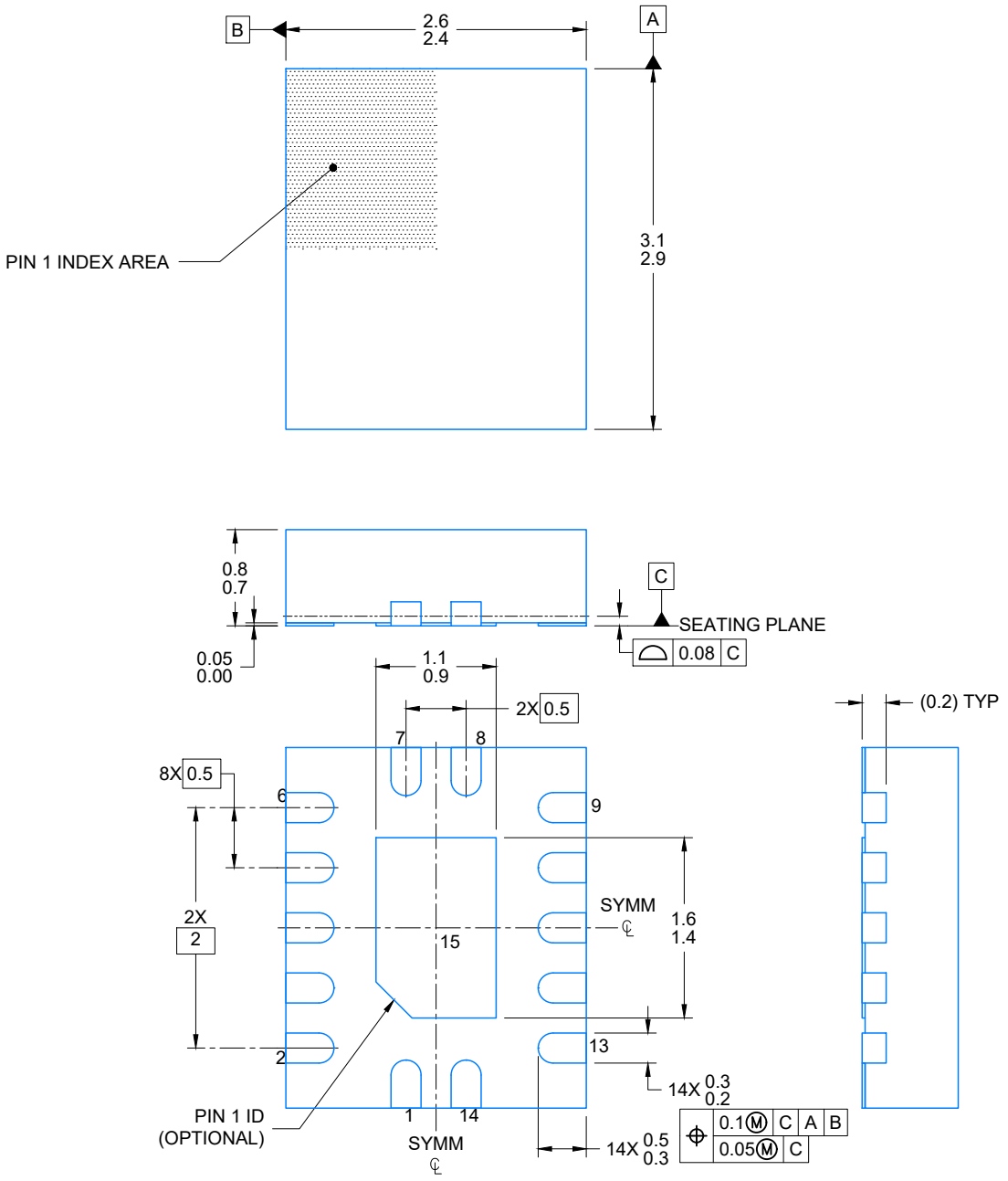


PACKAGE OUTLINE

BQA0014A

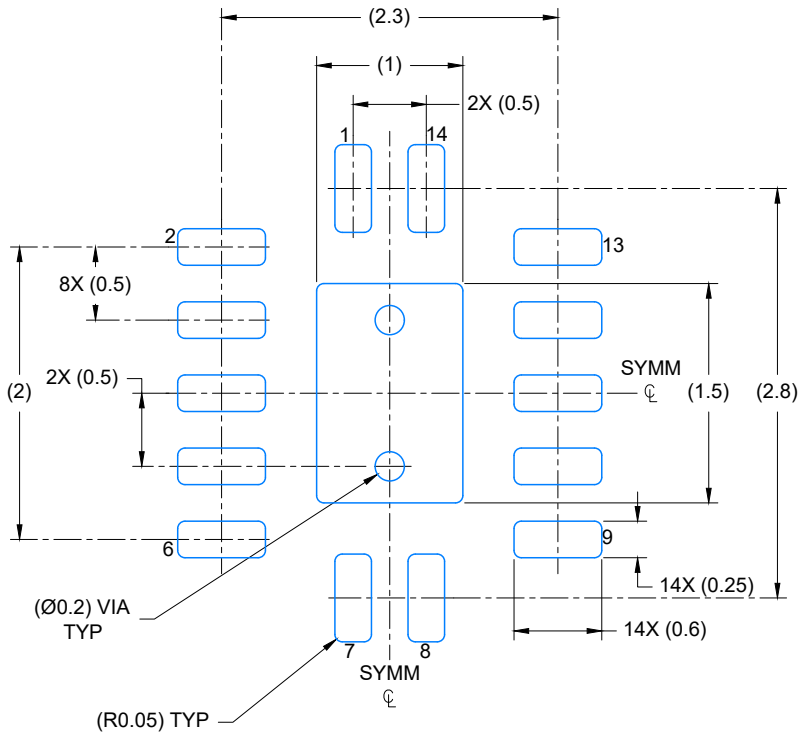
WQFN - 0.8 mm max height

PLASTIC QUAD FLAT PACK-NO LEAD

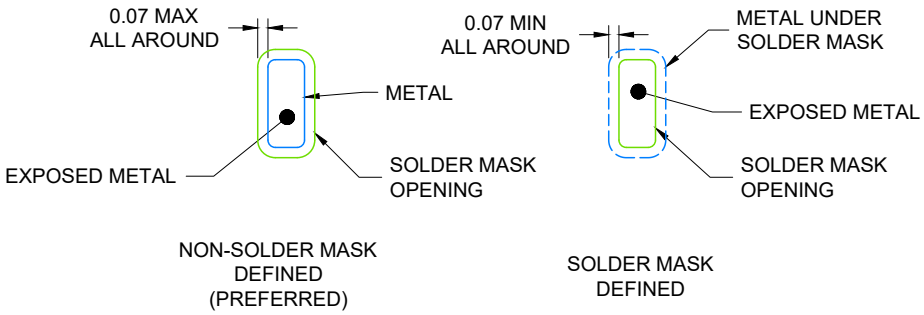


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.



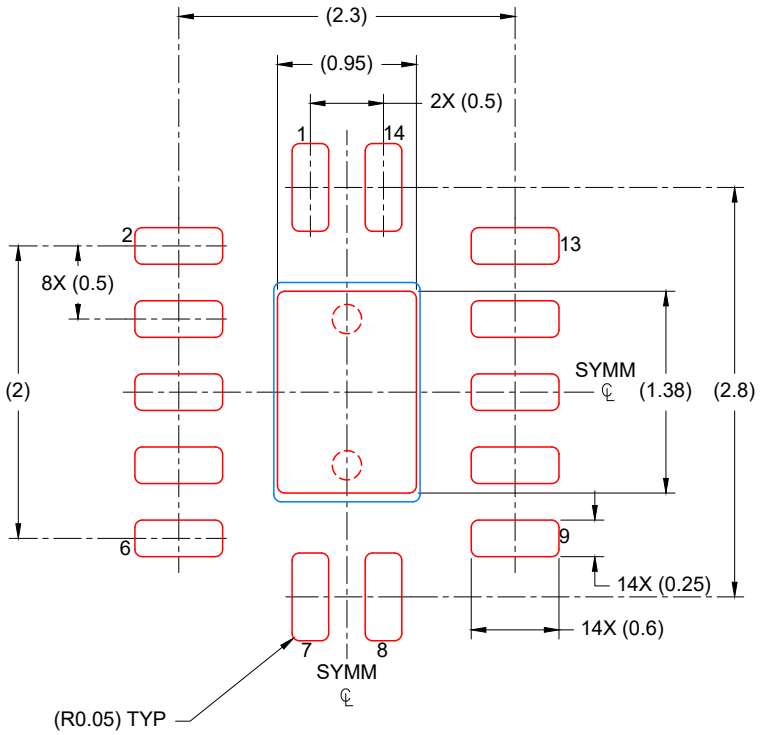
LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 20X



4224636/A 11/2018

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
88% PRINTED COVERAGE BY AREA
SCALE: 20X

4224636/A 11/2018

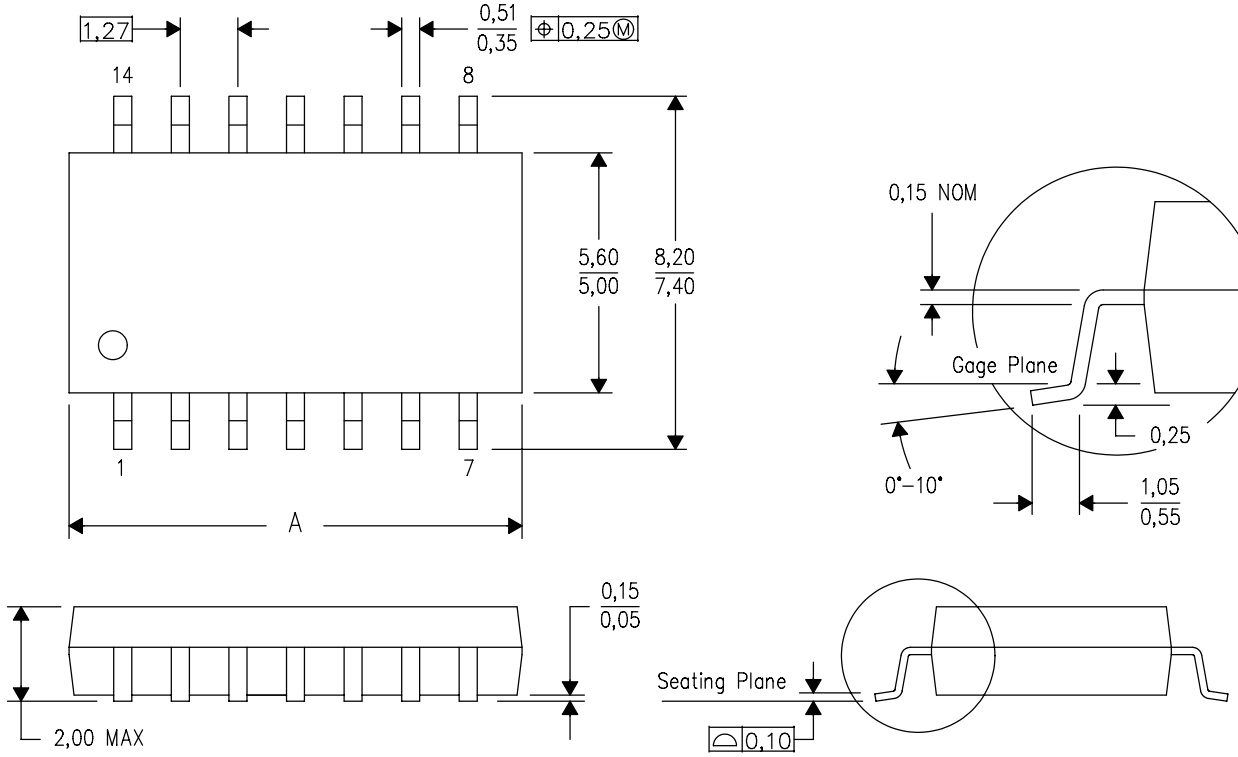
NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

MECHANICAL DATA

NS (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

14-PINS SHOWN

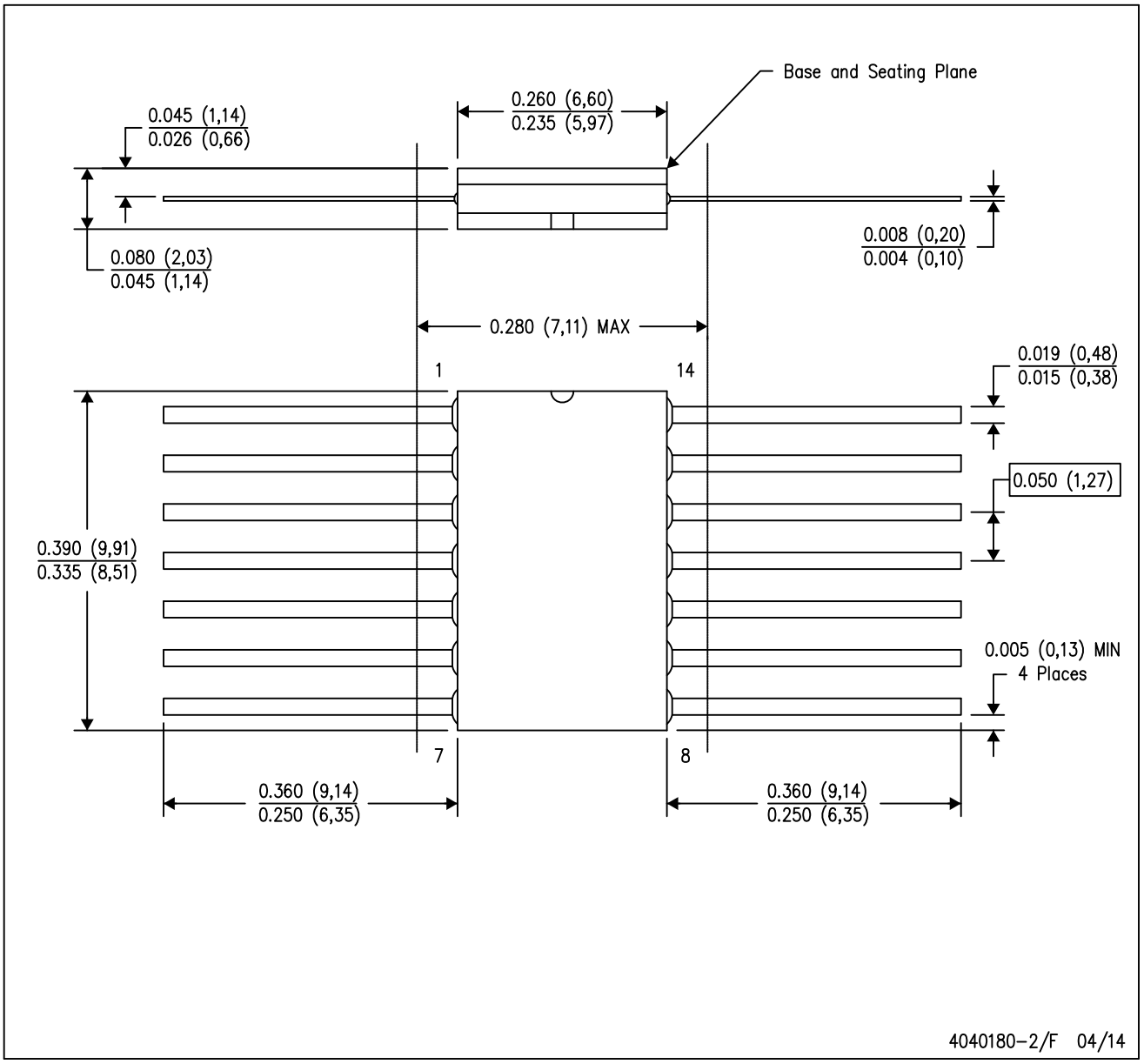


DIM \ PINS **	14	16	20	24
A MAX	10,50	10,50	12,90	15,30
A MIN	9,90	9,90	12,30	14,70

4040062/C 03/03

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

W (R–GDFP–F14) CERAMIC DUAL FLATPACK



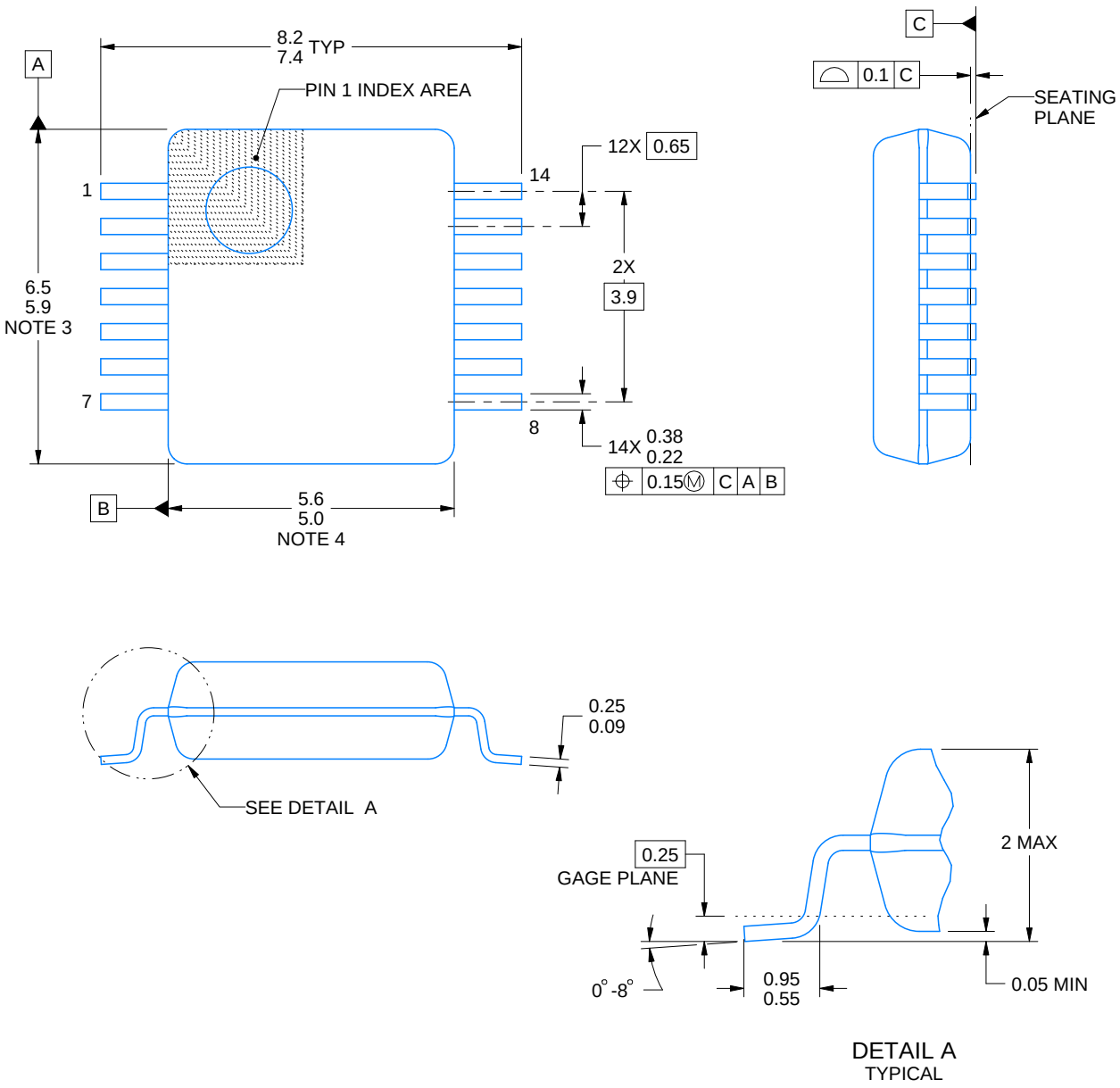
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only.
E. Falls within MIL STD 1835 GDFP1–F14

PACKAGE OUTLINE

DB0014A

SSOP - 2 mm max height

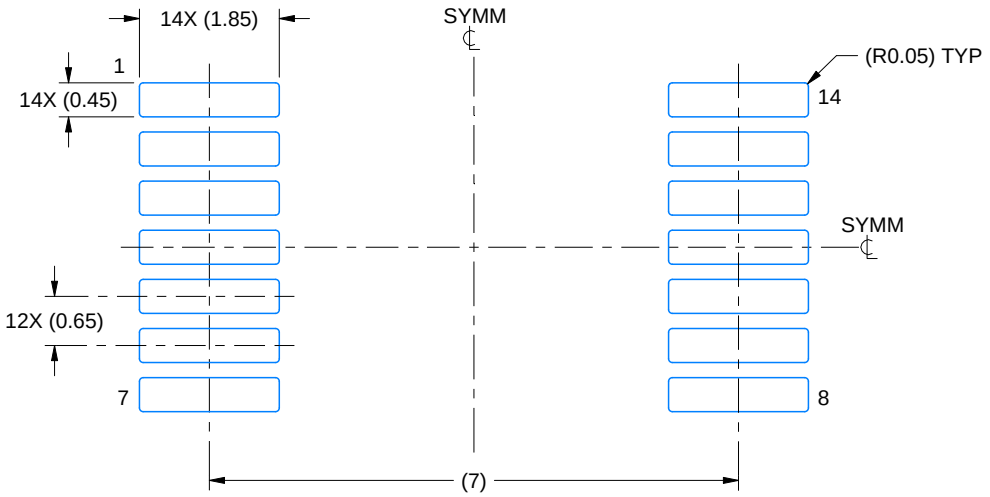
SMALL OUTLINE PACKAGE



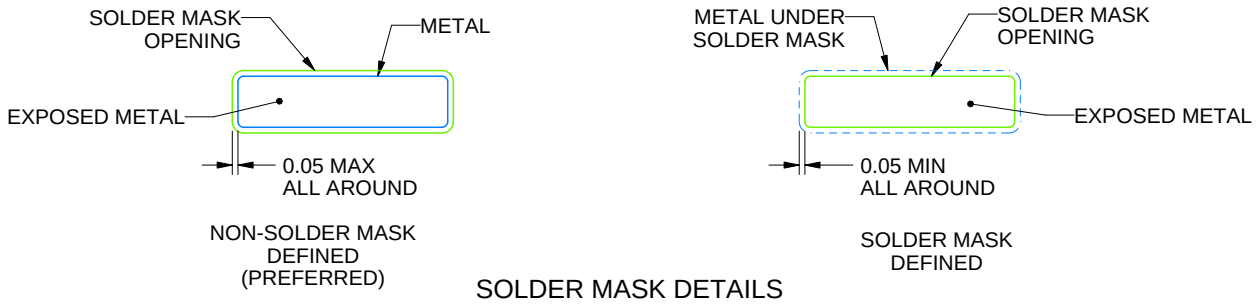
4220762/A 05/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-150.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

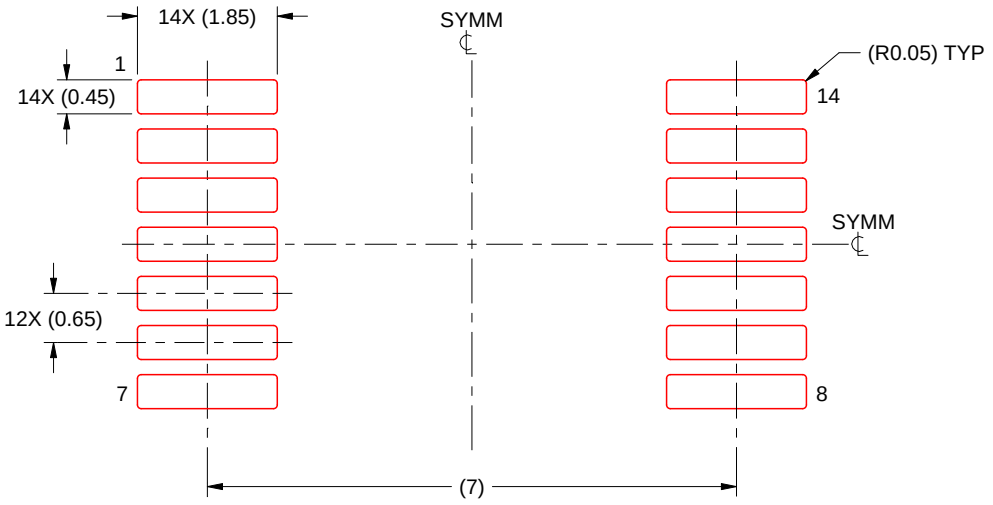


SOLDER MASK DETAILS

4220762/A 05/2024

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220762/A 05/2024

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

GENERIC PACKAGE VIEW

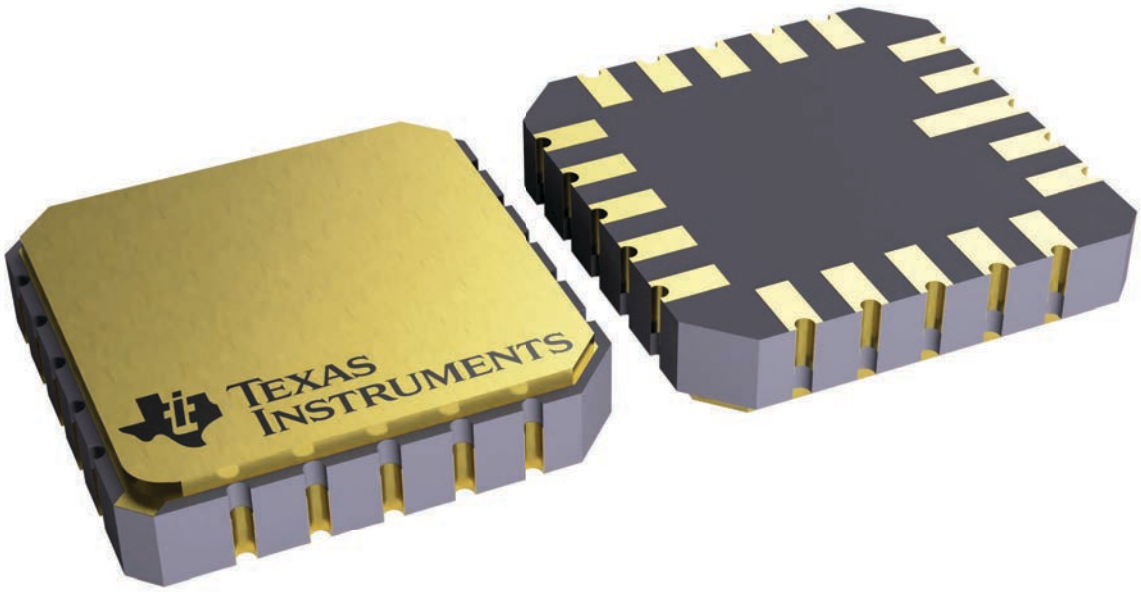
FK 20

LCCC - 2.03 mm max height

8.89 x 8.89, 1.27 mm pitch

LEADLESS CERAMIC CHIP CARRIER

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



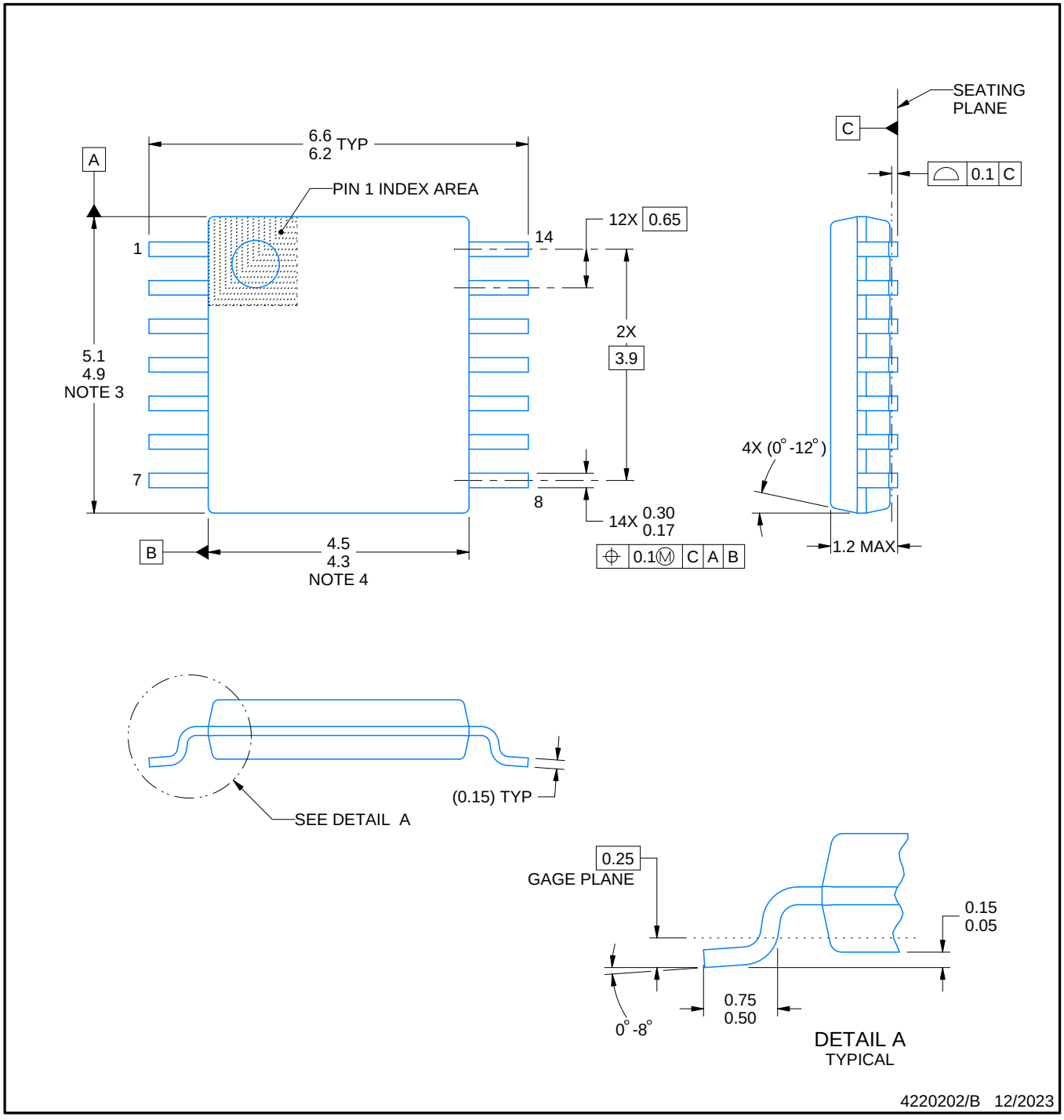
4229370VA\

PACKAGE OUTLINE

PW0014A

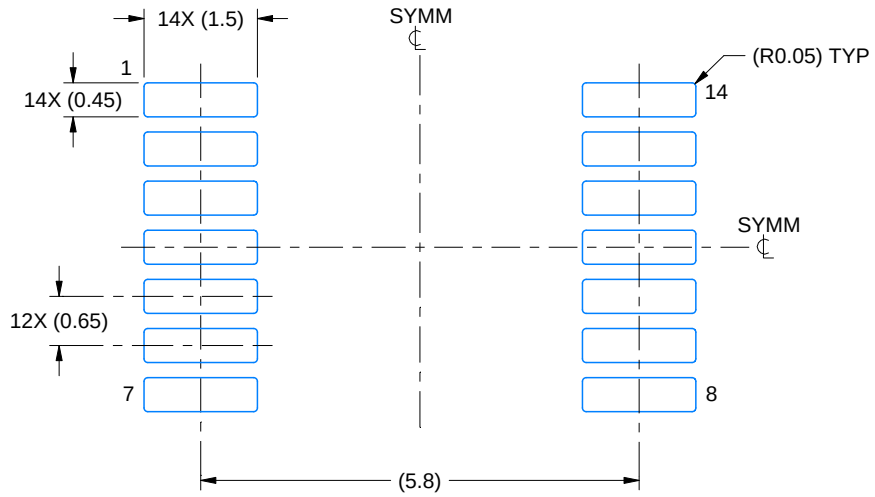
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

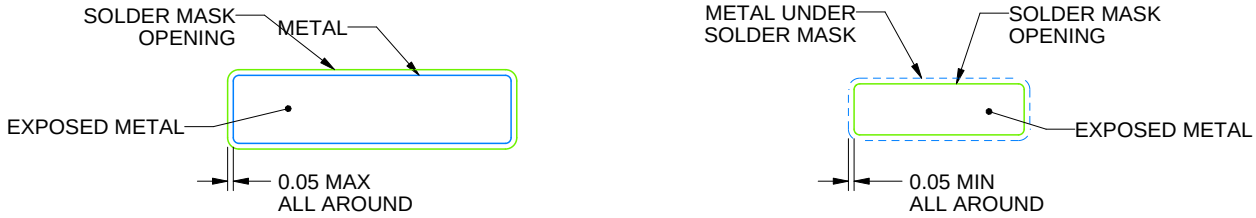


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

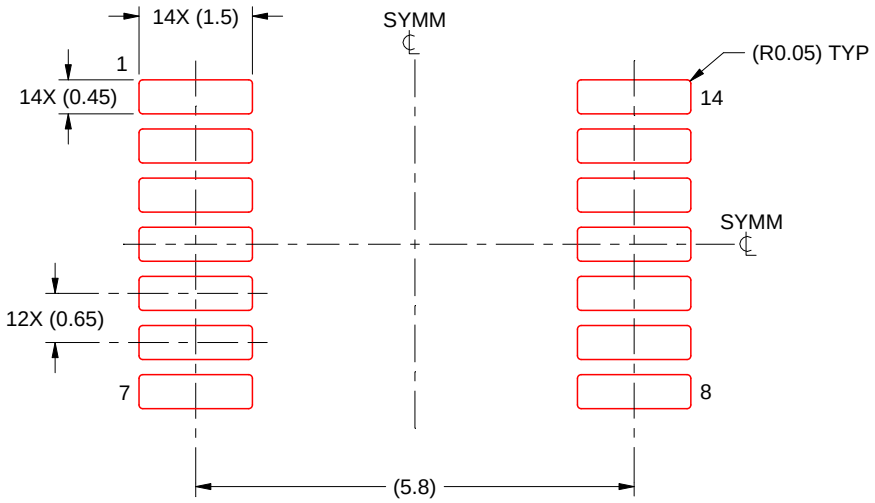


SOLDER MASK DETAILS

4220202/B 12/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220202/B 12/2023

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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