

RAD-TOLERANT CLASS V, DUAL DIFFERENTIAL LINE RECEIVER

FEATURES

- Single 5-V Supply
- Differential Line Operation
- Dual Channels
- TTL Compatibility
- ± 15 -V Common-Mode Input Voltage Range
- ± 15 -V Differential Input Voltage Range
- Individual Channel Strobes
- Built-In Optional Line-Termination Resistor
- Individual Frequency Response Controls
- Designed for Use With Dual Differential Drivers
SN55183 and **SN75183**
- Designed to Be Interchangeable With National Semiconductor **DS7820A** and **DS8820A**
- Rad-Tolerant: >40 kRad (Si) ELDRS
- QML-V Qualified, SMD 5962-79008

DESCRIPTION/ORDERING INFORMATION

The SN55182 dual differential line receiver is designed to sense small differential signals in the presence of large common-mode noise. This device gives TTL-compatible output signals as a function of the polarity of the differential input voltage. The frequency response of each channel can be easily controlled by a single external capacitor to provide immunity to differential noise spikes. The output goes to a high level when the inputs are open circuited. A strobe input (STRB) is provided that, when in the low level, disables the receiver and forces the output to a high level.

The receiver is of monolithic single-chip construction, and both halves of the dual circuits use common power-supply and ground terminals.

The SN55182 is characterized for operation over the full military temperature range of -55°C to 125°C .

PACKAGING/ORDERING INFORMATION⁽¹⁾

| TEMPERATURE | PACKAGED DEVICES | |
|--|---|-----------------|
| | CERAMIC FLATPACK W (14) ⁽²⁾ | SYMBOL |
| -55°C to 125°C | 5962-7900801VDA | 5962-7900801VDA |

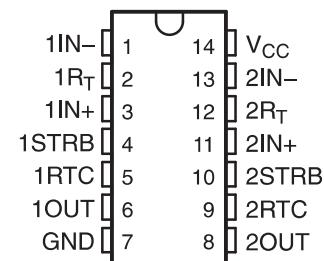
(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.

(2) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.

SN55182...J OR W PACKAGE

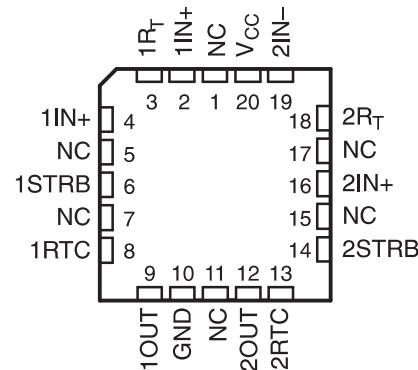
SN75182...N PACKAGE

(TOP VIEW)



SN55182...FK PACKAGE

(TOP VIEW)



NC – No internal connection



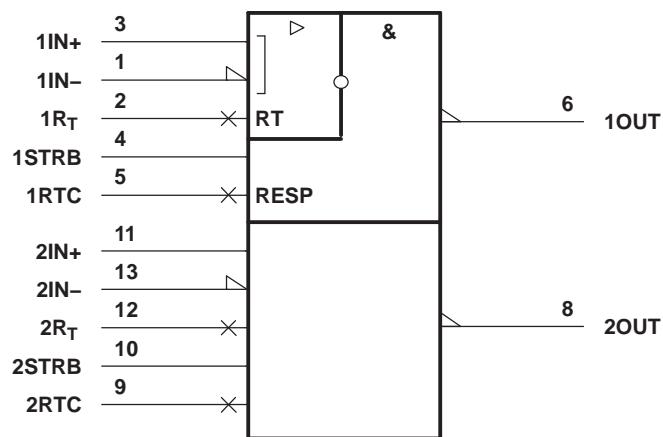
Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

FUNCTION TABLE⁽¹⁾

| INPUTS | | OUTPUT OUT |
|--------|-----------------|---------------|
| STRB | V _{ID} | |
| L | X | H |
| H | H | H |
| H | L | L |

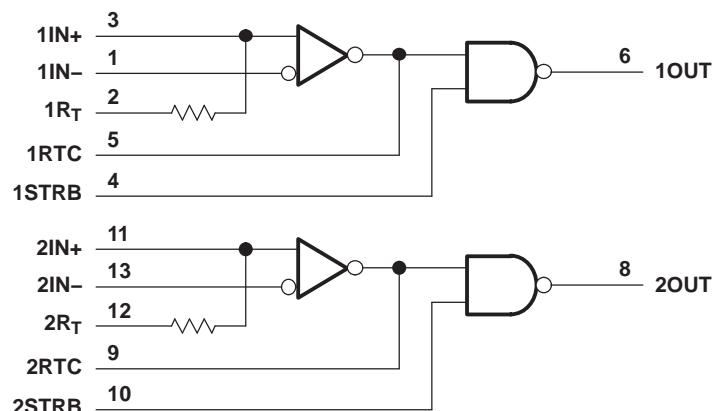
(1) H = $V_I \geq V_{IH}$ min or V_{ID} more positive than V_{TH} max
 L = $V_I \leq V_{IL}$ max or V_{ID} more negative than V_{TL} max
 X = irrelevant

LOGIC SYMBOL

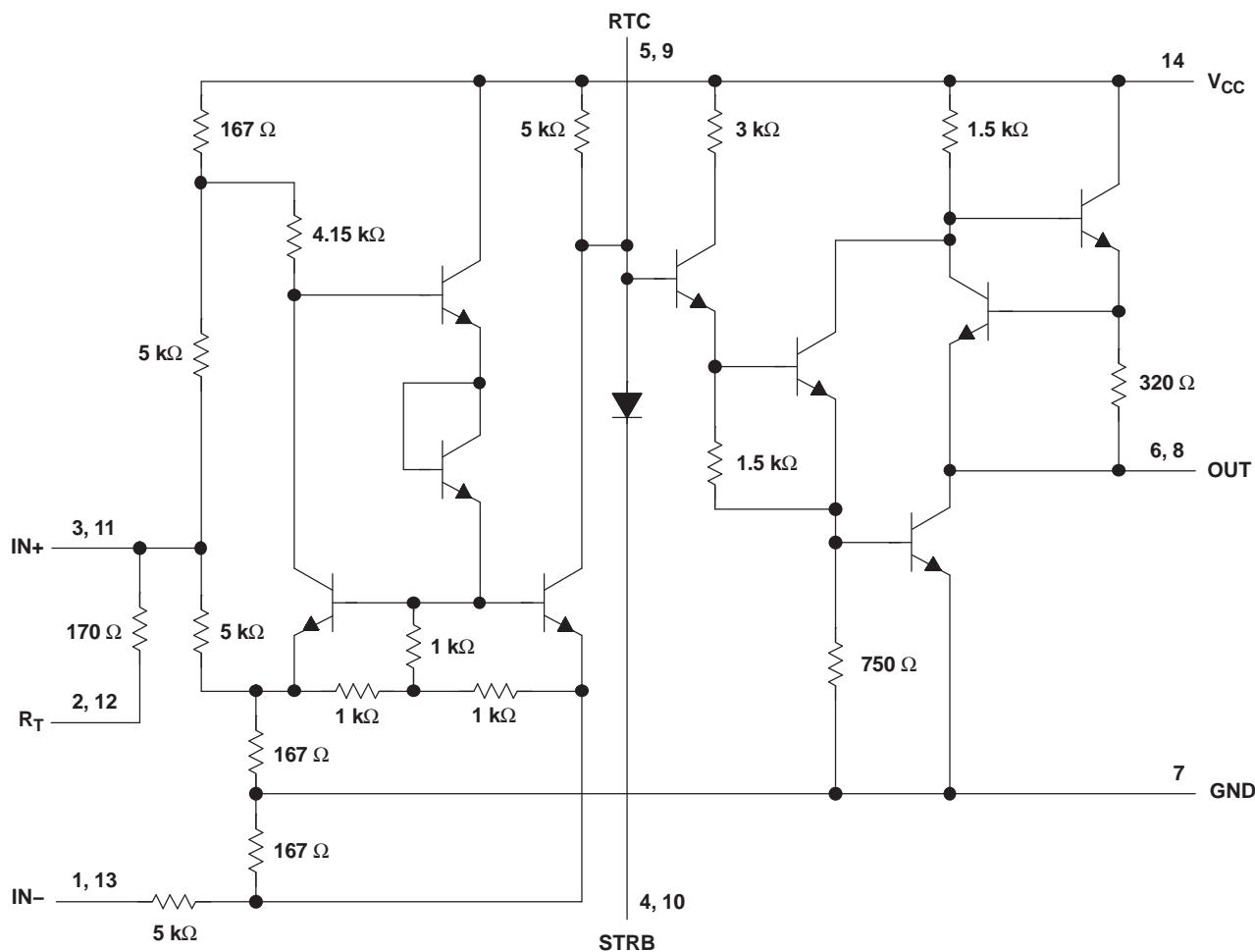


This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
 Pin numbers shown are for the J, N, and W packages.

LOGIC DIAGRAM (POSITIVE LOGIC)



Pin numbers shown are for the J, N, and W packages.

SCHEMATIC (EACH RECEIVER)


Resistor values shown are nominal.

Pin numbers shown are for the J, N, and W packages.

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

over operating free-air temperature range (unless otherwise noted)

| | | UNIT |
|---------------|--|------------------------------|
| V_{CC} | Supply voltage ⁽²⁾ | 8 V |
| V_{IC} | Common-mode input voltage | ± 20 V |
| V_{ID} | Differential input voltage ⁽³⁾ | ± 20 V |
| $V_{I(STRB)}$ | Strobe input voltage | 8 V |
| I_O | Output sink current | 50 mA |
| | Continuous total power dissipation | See Dissipation Rating Table |
| T_{stg} | Storage temperature range | -65°C to 150°C |
| | Lead temperature 1.6 mm (1/16 inch) from case for 60 seconds: J or W package | 300°C |

(1) The absolute maximum ratings under any condition are limited by the constraints of the silicon process. Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not implied.

(2) All voltage values, except differential voltages, are with respect to network ground terminal.

(3) Differential voltage values are at the noninverting terminal with respect to the inverting terminal.

DISSIPATION RATING TABLE

| PACKAGE | T _A ≤ 25°C POWER RATING | DERATING FACTOR ABOVE T _A = 25°C | T _A = 70°C POWER RATING | T _A = 125°C POWER RATING |
|------------------|---------------------------------------|--|---------------------------------------|--|
| W ⁽¹⁾ | 1000 mW | 8.0 mW/°C | 640 mW | 200 mW |

(1) In the FK, J, and W packages, SN55182 chips are alloy mounted.

RECOMMENDED OPERATING CONDITIONS

| | | MIN | NOM | MAX | UNIT |
|-----------------------|---------------------------------|-----|-----|------|------|
| V _{CC} | Supply voltage | 4.5 | 5 | 5.5 | V |
| V _{IC} | Common-mode input voltage | | | ±15 | V |
| V _{IH(STRB)} | High-level strobe input voltage | 2.1 | | 5.5 | V |
| V _{IL(STRB)} | Low-level strobe input voltage | 0 | | 0.9 | V |
| I _{OH} | High-level output current | | | -400 | µA |
| I _{OL} | Low-level output current | | | 16 | mA |
| T _A | Operating free-air temperature | -55 | | 125 | °C |

ELECTRICAL CHARACTERISTICS

over recommended ranges of V_{CC} , V_{IC} , and operating free-air temperature (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS ⁽¹⁾ | | MIN | TYP ⁽²⁾ | MAX | UNIT |
|-----------------------------|--|---|---|------|--------------------|---------------|------------------|
| V_{IT+} | Positive-going input threshold voltage | $V_O = 2.5 \text{ V}$, $I_{OH} = -400 \mu\text{A}$ | $V_{IC} = -3 \text{ V to } 3 \text{ V}$ | | 0.5 | 1 | V |
| | | | $V_{IC} = -15 \text{ V to } 15 \text{ V}$ | | 1 | | |
| V_{IT-} | Negative-going input threshold voltage | $V_O = 0.4 \text{ V}$, $I_{OL} = 16 \text{ mA}$ | $V_{IC} = -3 \text{ V to } 3 \text{ V}$ | | -0.5 | -1 | V |
| | | | $V_{IC} = -15 \text{ V to } 15 \text{ V}$ | | -1 | | |
| V_{OH} | High-level output voltage | $V_{ID} = 1 \text{ V}$, $V_{(STRB)} = 2.1 \text{ V}$, $I_{OH} = -400 \mu\text{A}$ | $V_{ID} = 1 \text{ V}$, $V_{(STRB)} = 0.4 \text{ V}$, $I_{OH} = -400 \mu\text{A}$ | 2.5 | 4.2 | 5.5 | V |
| | | | $V_{ID} = 1 \text{ V}$, $V_{(STRB)} = 2.1 \text{ V}$, $I_{OL} = 16 \text{ mA}$ | 2.5 | 4.2 | 5.5 | |
| V_{OL} | Low-level output voltage | | | | 0.25 | 0.4 | V |
| I_I | Input current | Inverting input | $V_{IC} = 15 \text{ V}$ | | 3 | 4.2 | mA |
| | | | $V_{IC} = 0$ | | 0 | -0.5 | |
| | | | $V_{IC} = -15 \text{ V}$ | | -3 | -4.2 | |
| | | Noninverting input | $V_{IC} = 15 \text{ V}$ | | 5 | 7 | |
| | | | $V_{IC} = 0$ | | -1 | -1.4 | |
| | | | $V_{IC} = -15 \text{ V}$ | | -7 | -9.8 | |
| $I_{IH(STRB)}$ | High-level strobe input current | $V_{(STRB)} = 5.5 \text{ V}$ | | | 5 | μA | |
| $I_{IL(STRB)}$ | Low-level strobe input current | $V_{(STRB)} = 0$ | | | -1 | -1.4 | mA |
| r_I | Input resistance | Inverting input | | | 3.6 | 5 | $\text{k}\Omega$ |
| | | | | | 1.8 | 2.5 | |
| Line-terminating resistance | | $T_A = 25^\circ\text{C}$ | | 120 | 170 | 250 | Ω |
| I_{OS} | Short-circuit output current | $V_{CC} = 5.5 \text{ V}$ | $V_O = 0$ | -2.8 | -4.5 | -6.7 | mA |
| I_{CC} | Supply current (average per receiver) | $V_{IC} = 15 \text{ V}$ | $V_{ID} = -1 \text{ V}$ | | 4.2 | 6 | mA |
| | | $V_{IC} = 0$ | $V_{ID} = -0.5 \text{ V}$ | | 6.8 | 10.2 | |
| | | $V_{IC} = -15 \text{ V}$ | $V_{ID} = -1 \text{ V}$ | | 9.4 | 14 | |

(1) Unless otherwise noted, $V_{(STRB)} \geq 2.1 \text{ V}$ or open.

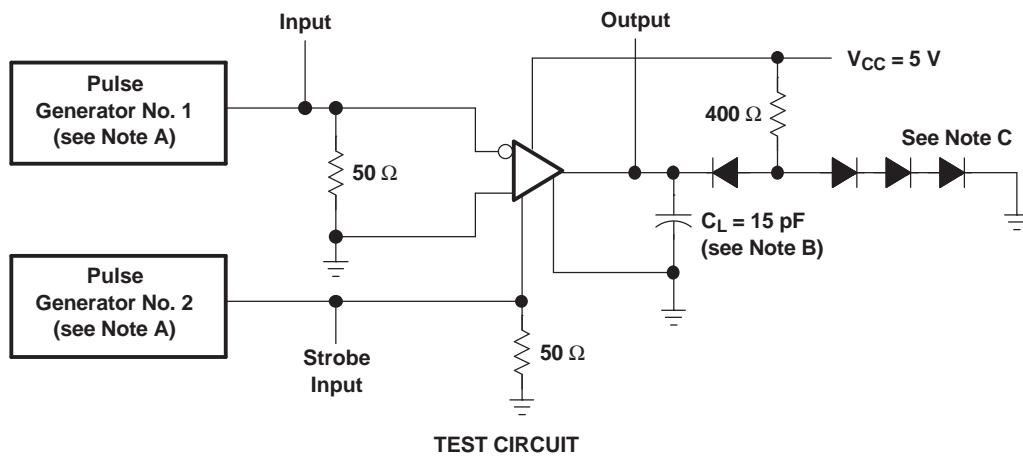
(2) All typical values are at $V_{CC} = 5 \text{ V}$, $V_{IC} = 0$, and $T_A = 25^\circ\text{C}$.

SWITCHING CHARACTERISTICS

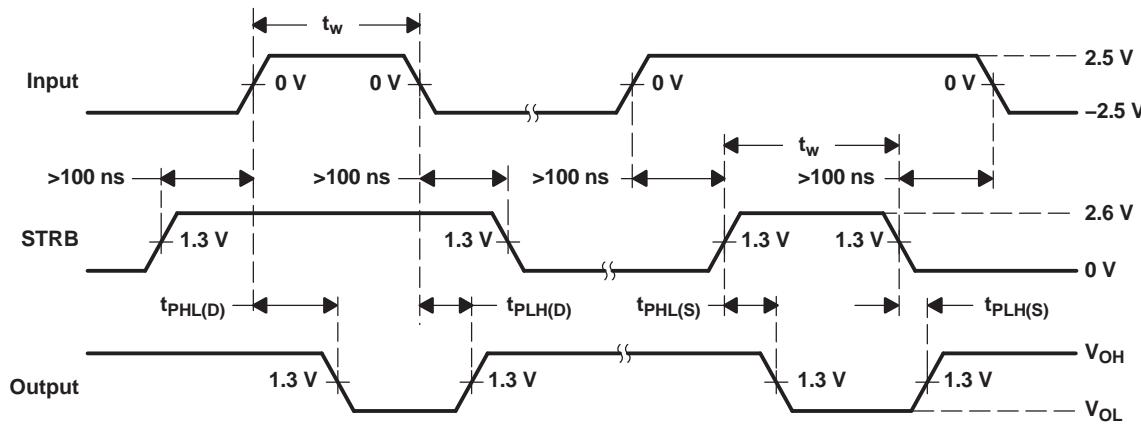
$V_{CC} = 5 \text{ V}$, $T_A = 25^\circ\text{C}$

| PARAMETER | | TEST CONDITIONS | | MIN | TYP | MAX | UNIT |
|--------------|---|---|--|-----|-----|-----|------|
| $t_{PLH(D)}$ | Propagation delay time, low- to high-level output from differential input | $R_L = 400 \Omega$, $C_L = 15 \text{ pF}$, See Figure 1 | | 18 | 40 | | ns |
| $t_{PHL(D)}$ | Propagation delay time, high- to low-level output from differential input | $R_L = 400 \Omega$, $C_L = 15 \text{ pF}$, See Figure 1 | | 31 | 45 | | ns |
| $t_{PLH(S)}$ | Propagation delay time, low- to high-level output from STRB input | $R_L = 400 \Omega$, $C_L = 15 \text{ pF}$, See Figure 1 | | 9 | 30 | | ns |
| $t_{PHL(S)}$ | Propagation delay time, high- to low-level output from STRB input | $R_L = 400 \Omega$, $C_L = 15 \text{ pF}$, See Figure 1 | | 15 | 25 | | ns |

PARAMETER MEASUREMENT INFORMATION



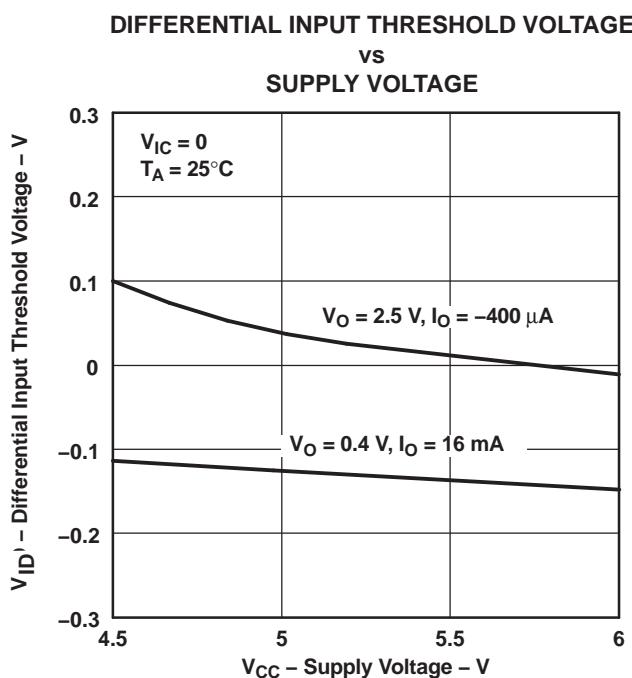
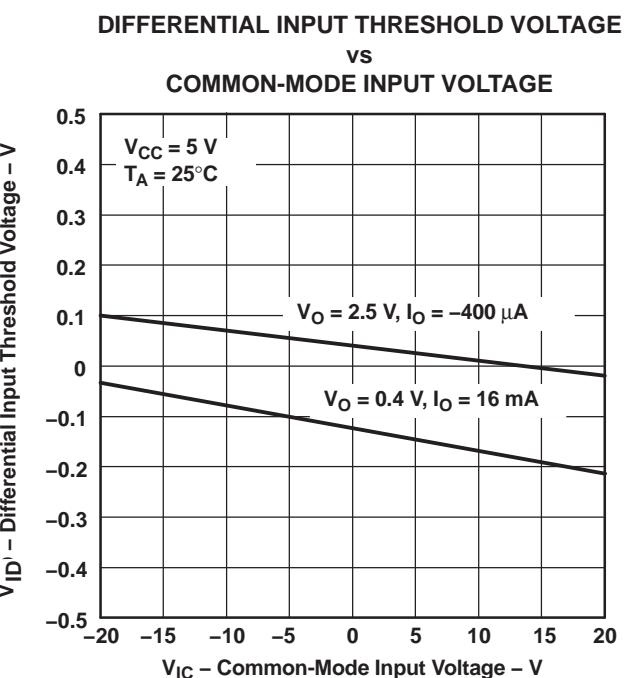
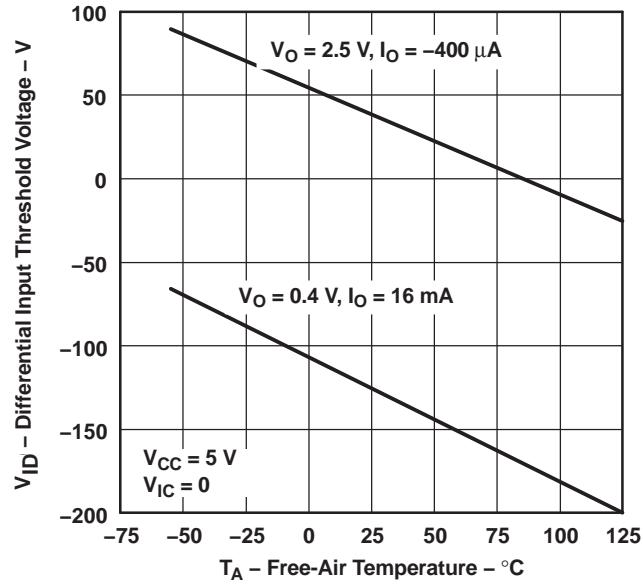
TEST CIRCUIT



VOLTAGE WAVEFORMS

- A. The pulse generators have the following characteristics: $Z_0 = 50 \Omega$, $t_r \leq 10 \text{ ns}$, $t_f \leq 10 \text{ ns}$, $t_w = 0.5 \pm 0.1 \mu\text{s}$, PRR $\leq 1 \text{ MHz}$.
- B. C_L includes probe and jig capacitance.
- C. All diodes are 1N3064 or equivalent.

Figure 1. Test Circuit and Voltage Waveforms

TYPICAL CHARACTERISTICS⁽¹⁾

Figure 2.

Figure 3.
DIFFERENTIAL INPUT THRESHOLD VOLTAGE
vs
FREE-AIR TEMPERATURE

Figure 4.

(1) Operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied.

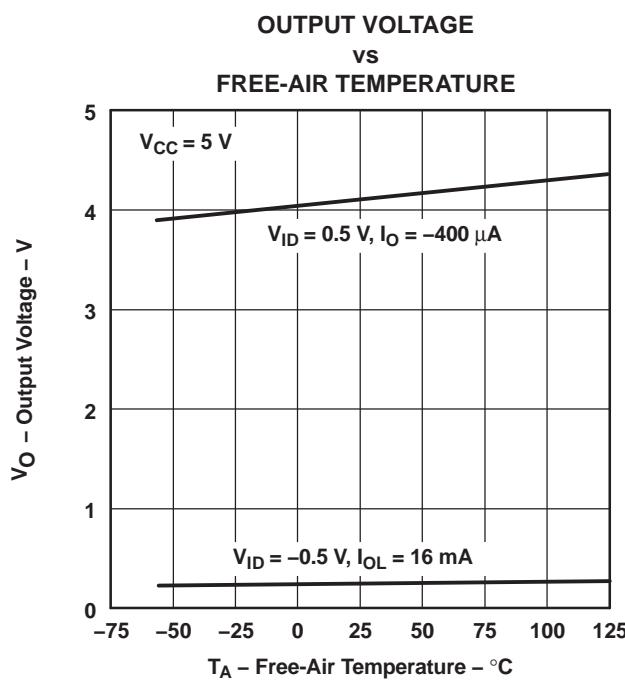
TYPICAL CHARACTERISTICS⁽¹⁾

Figure 5.
INPUT CURRENT
vs
INPUT VOLTAGE

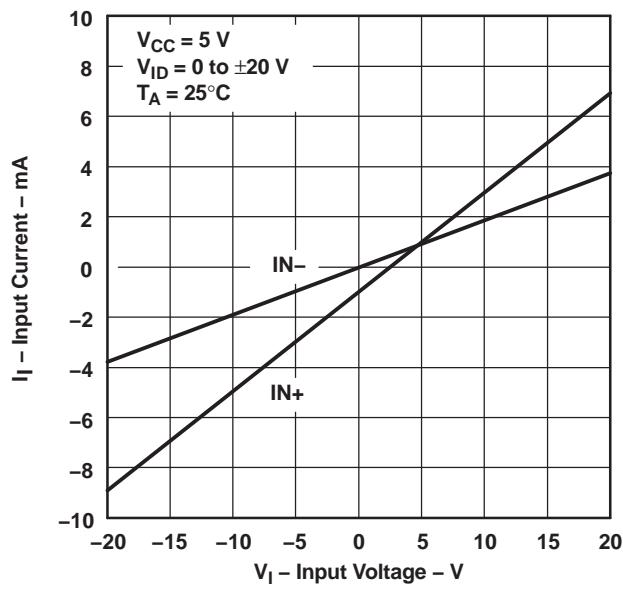


Figure 7.

VOLTAGE TRANSFER CHARACTERISTICS

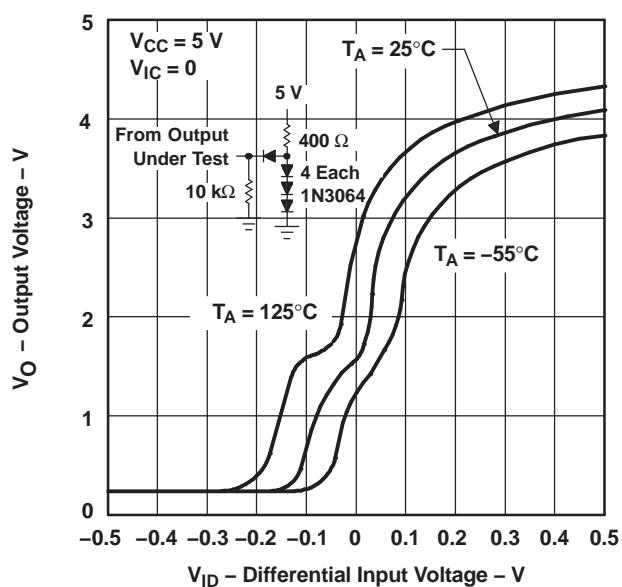


Figure 6.
TERMINATING RESISTANCE
vs
FREE-AIR TEMPERATURE

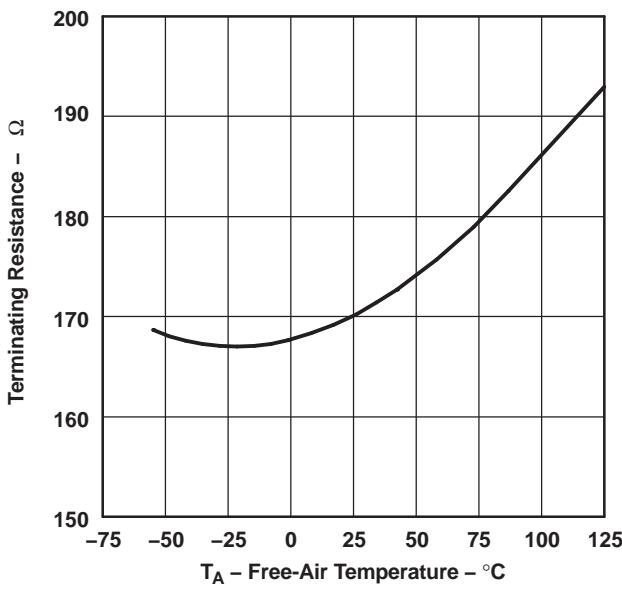
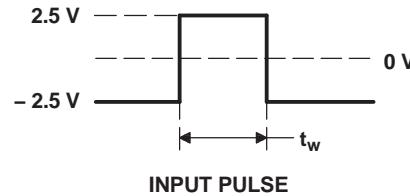
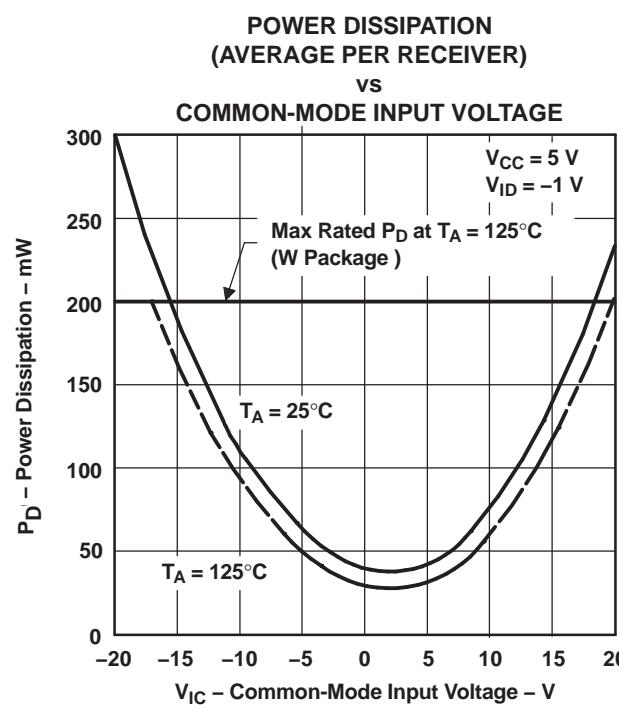
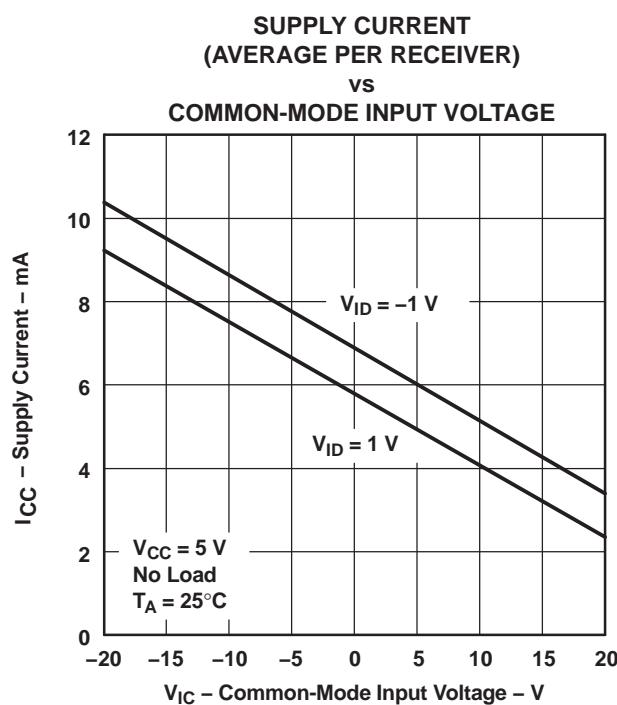


Figure 8.

(1) Operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied.

TYPICAL CHARACTERISTICS⁽¹⁾


A. Figure 11 shows the maximum duration of the illustrated pulse that can be applied differently without the output changing from the low to high level.

Figure 11.

(1) Operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied.

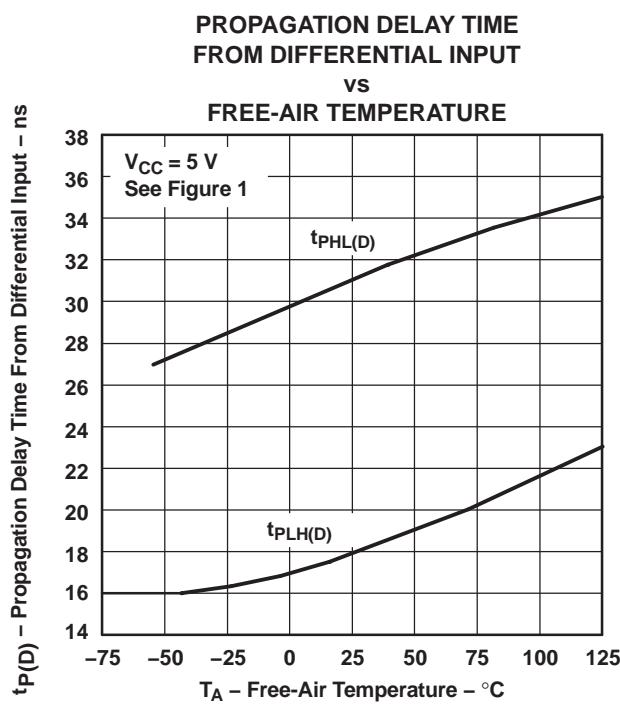
TYPICAL CHARACTERISTICS⁽¹⁾

Figure 12.

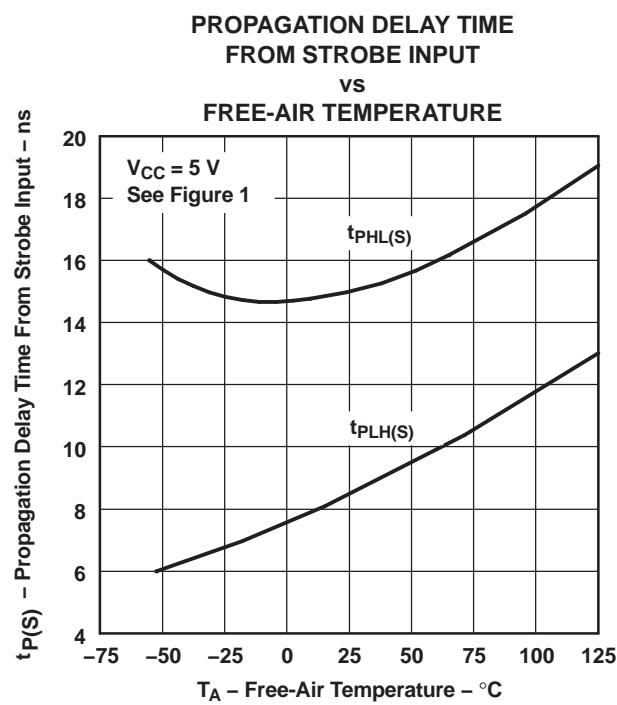
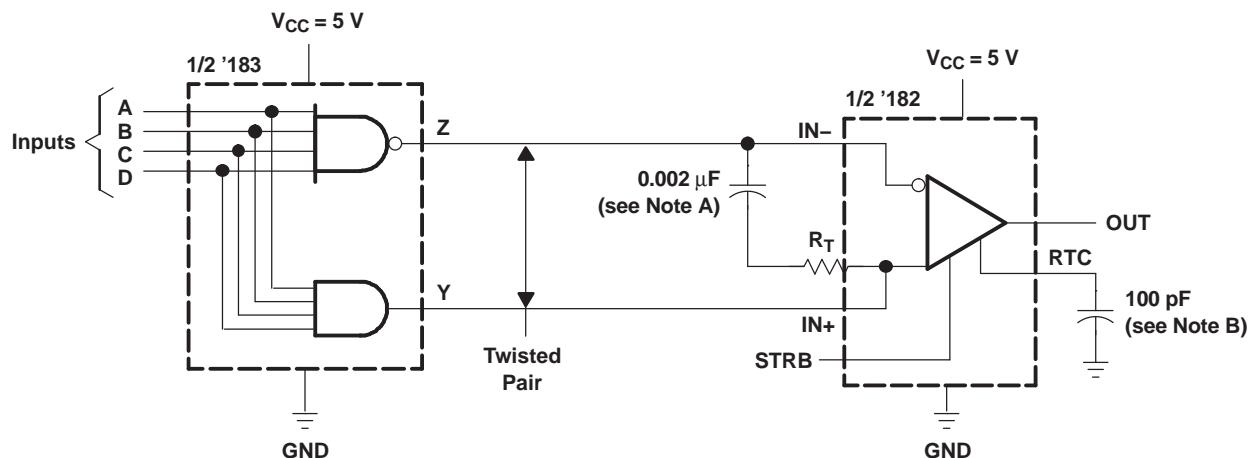


Figure 13.

(1) Operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied.

APPLICATION INFORMATION



NOTES: A. When the inputs are open circuited, the output is high. A capacitor may be used for dc isolation of the line-terminating resistor. At the frequency of operation, the impedance of the capacitor should be relatively small.

Example: let $f = 5 \text{ MHz}$
 $C = 0.002 \mu\text{F}$

$$Z_{(C)} = \frac{1}{2\pi f C} = \frac{1}{2\pi(5 \times 10^6)(0.002 \times 10^{-6})}$$

$$Z_{(C)} \approx 16\Omega$$

B. Use of a capacitor to control response time is optional.

Figure 14. Transmission of Digital Data Over Twisted-Pair Line

PACKAGING INFORMATION

| Orderable part number | Status (1) | Material type (2) | Package Pins | Package qty Carrier | RoHS (3) | Lead finish/ Ball material (4) | MSL rating/ Peak reflow (5) | Op temp (°C) | Part marking (6) |
|-----------------------|---------------|----------------------|----------------|-----------------------|-------------|--------------------------------------|-----------------------------------|--------------|----------------------------------|
| 5962-7900801VCA | Active | Production | CDIP (J) 14 | 25 TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | 5962-7900801VC A SNV55182J |
| 5962-7900801VCA.A | Active | Production | CDIP (J) 14 | 25 TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | 5962-7900801VC A SNV55182J |
| 5962-7900801VDA | Active | Production | CFP (W) 14 | 25 TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | 5962-7900801VD A SNV55182W |
| 5962-7900801VDA.A | Active | Production | CFP (W) 14 | 25 TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | 5962-7900801VD A SNV55182W |

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

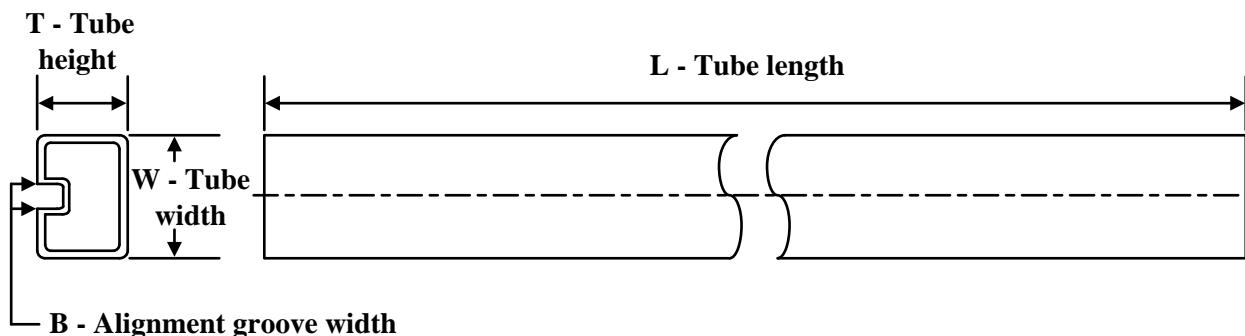
⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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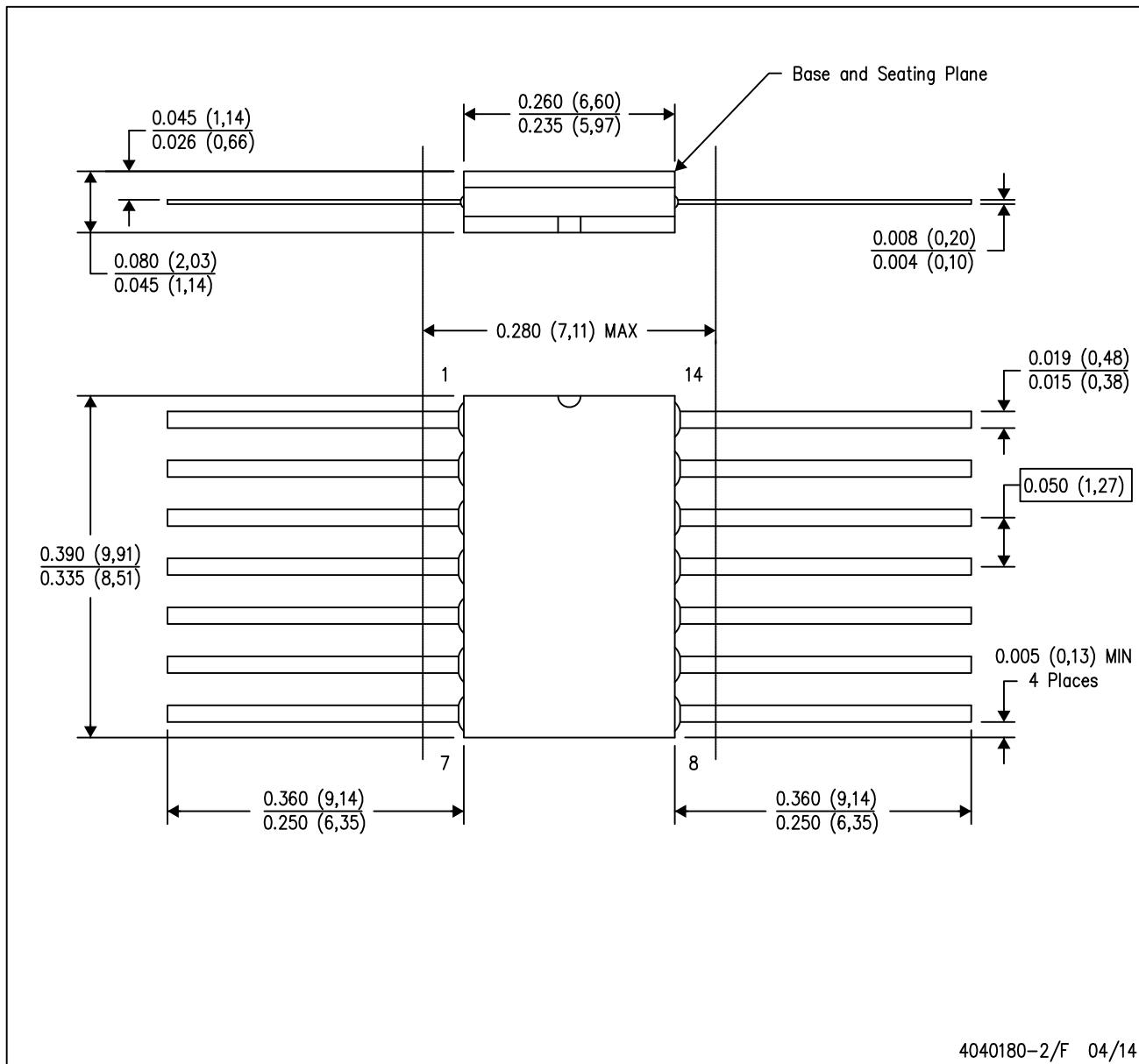
TUBE


*All dimensions are nominal

| Device | Package Name | Package Type | Pins | SPQ | L (mm) | W (mm) | T (μm) | B (mm) |
|-------------------|--------------|--------------|------|-----|--------|--------|--------|--------|
| 5962-7900801VDA | W | CFP | 14 | 25 | 506.98 | 26.16 | 6220 | NA |
| 5962-7900801VDA.A | W | CFP | 14 | 25 | 506.98 | 26.16 | 6220 | NA |

W (R-GDFP-F14)

CERAMIC DUAL FLATPACK



NOTES:

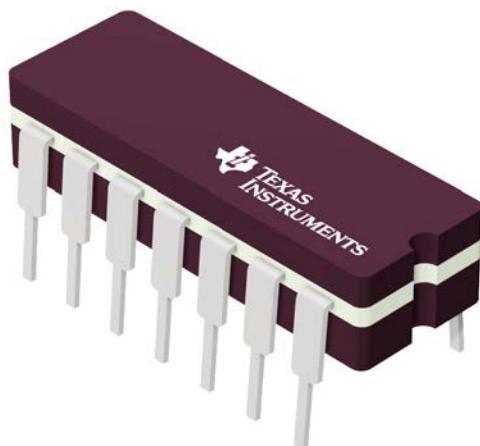
- All linear dimensions are in inches (millimeters).
- This drawing is subject to change without notice.
- This package can be hermetically sealed with a ceramic lid using glass frit.
- Index point is provided on cap for terminal identification only.
- Falls within MIL-STD 1835 GDFP1-F14

GENERIC PACKAGE VIEW

J 14

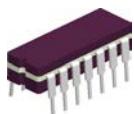
CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

4040083-5/G

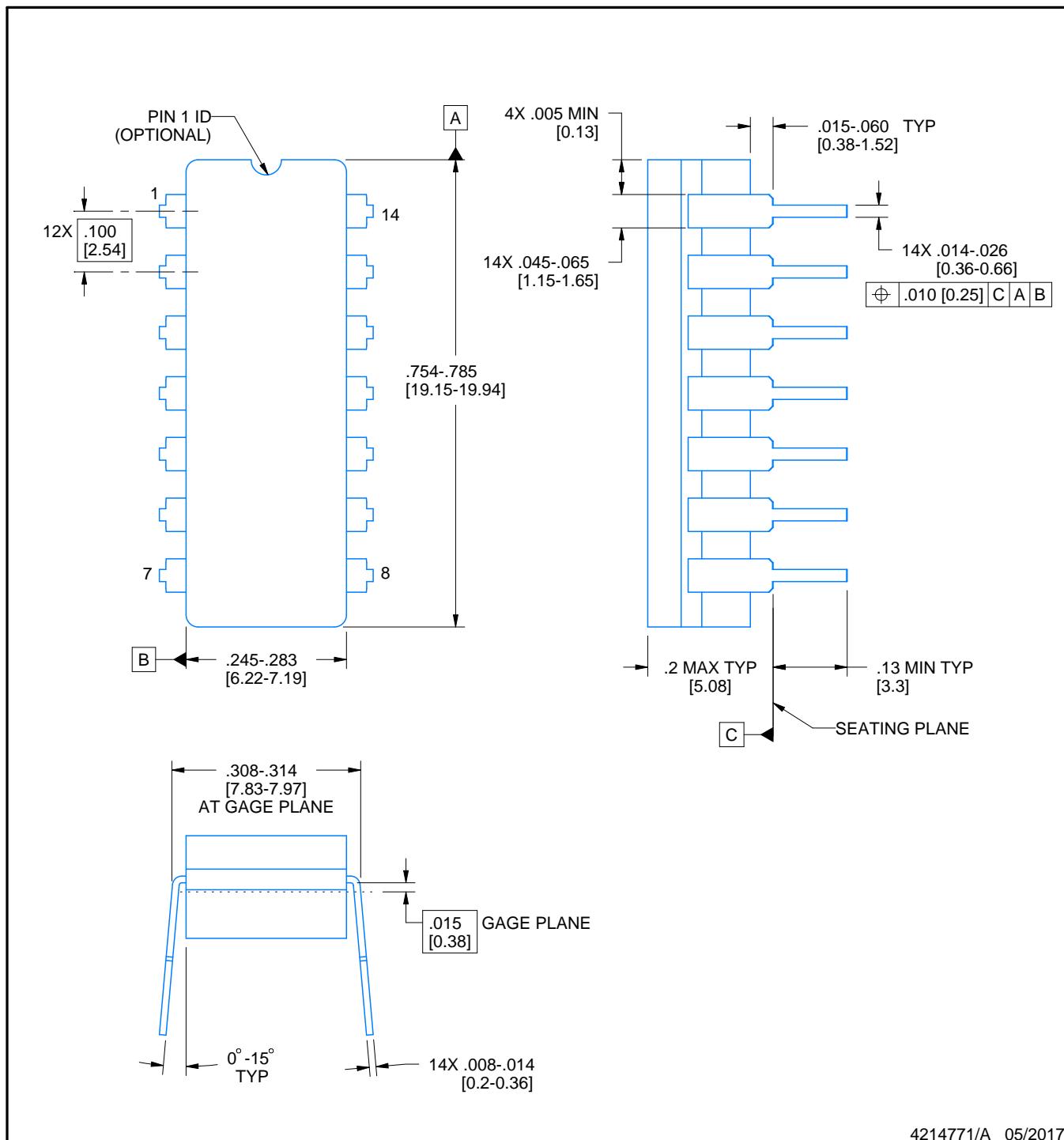


PACKAGE OUTLINE

J0014A

CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE



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NOTES:

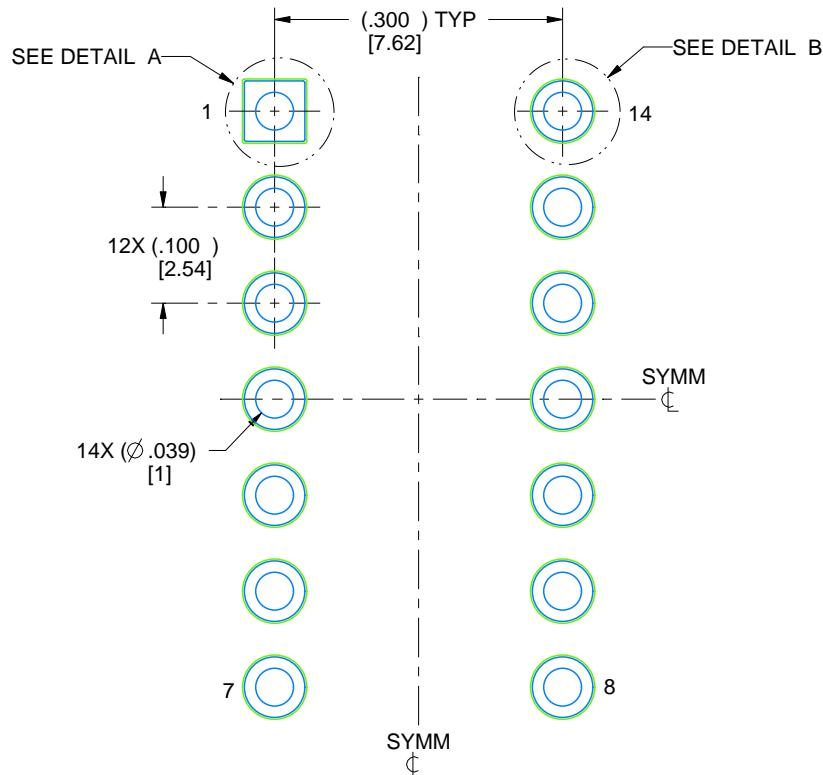
1. All controlling linear dimensions are in inches. Dimensions in brackets are in millimeters. Any dimension in brackets or parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This package is hermetically sealed with a ceramic lid using glass frit.
4. Index point is provided on cap for terminal identification only and on press ceramic glass frit seal only.
5. Falls within MIL-STD-1835 and GDIP1-T14.

EXAMPLE BOARD LAYOUT

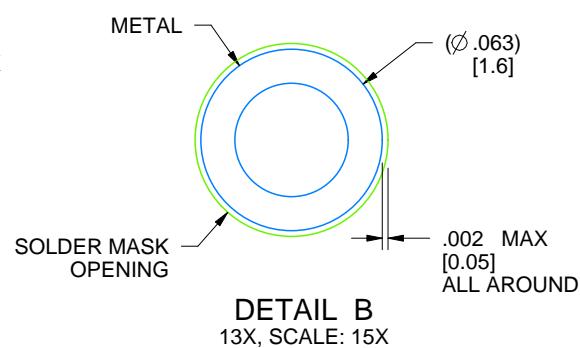
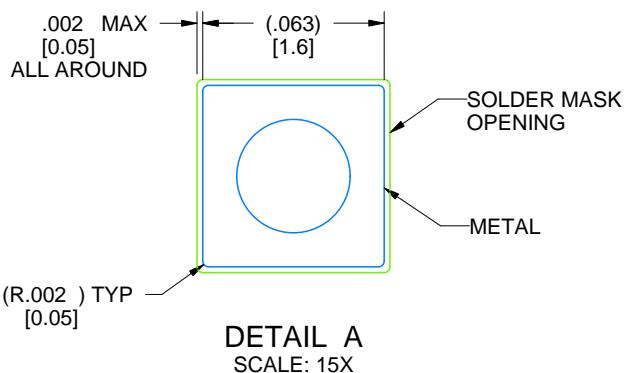
J0014A

CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE



LAND PATTERN EXAMPLE
NON-SOLDER MASK DEFINED
SCALE: 5X



4214771/A 05/2017

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