SN6507-Q1 适用于隔离式电源且具有占空比控制功能的低发射 36V 推挽式变压器驱动器

1 特性

- 提供功能安全
  - 可提供用于功能安全系统设计的文档：SN6507-Q1
- 符合面向汽车应用的 AEC-Q100（1 级）标准
- 使用 SN6507-Q1 并借助 WEBENCH® Power Designer 创建定制设计方案
- 用于隔离变压器的推挽式驱动器
- 宽输入电压范围：3V 至 36V
  - 输入电压容差高达 60V
  - 用于线路调节的占空比控制
- 具有可编程电流限制的 0.5A 开关
- 宽开关频率范围：100kHz 至 2MHz
  - 与小尺寸变压器兼容
  - 可编程开关频率
  - 外部时钟同步选项
- 低噪声和发射
  - 对称推挽式拓扑
  - 展频时钟
  - 引脚可配置压摆率控制
- 保护特性
  - 可调节欠压锁定 (UVLO)
  - 可编程过流保护 (OCP)
  - 过压锁定 (OVLO)
  - 热关断 (TSD)
- 宽温度范围：-55°C 至 125°C
- 可编程软启动，可减小浪涌电流
- 带有散热焊盘的 10 引脚 HVSSOP (DGQ) 封装

2 应用

适用于以下应用的隔离式电源：

- 电池管理系统 (BMS)
- 车载充电器
- 直流/直流转换器
- 逆变器和电机控制

3 说明

SN6507-Q1 是一款高压、高频推挽式变压器驱动器，以小尺寸解决方案提供隔离电源。该器件具有推挽式拓扑结构的简单性、低 EMI 和磁通消除等优点，可防止变压器饱和。采用占空比控制技术来减少宽输入范围的元件数量，同时选择高开关频率来缩小变压器尺寸，从而进一步节省空间。

该器件集成了控制器和两个异相切换的 0.5A NMOS 电源开关。其输入工作范围通过精密欠压锁定进行编程。该器件通过过流保护 (OCP)、可调节欠压锁定 (UVLO)、过压锁定 (OVLO)、热关断 (TSD) 和先断后通型电路来防止出现故障条件。

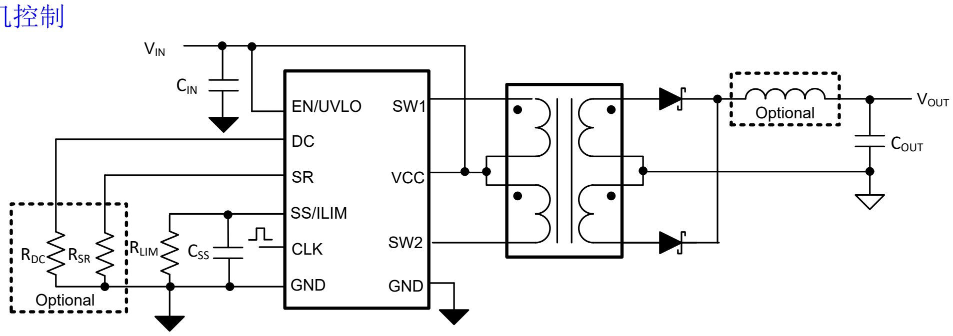
可编程软启动 (SS) 可尽可能减少浪涌电流，并为满足关键的上电要求提供电源时序。展频时钟 (SSC) 和引脚可配置的压摆率控制 (SRC) 进一步降低了辐射和传导发射，以满足超低 EMI 要求。

SN6507-Q1 可采用 10 引脚 HVSSOP DGQ 封装。该器件的运行温度范围为 –55°C 至 125°C。

封装信息

器件型号	封装(1)	封装尺寸（标称值）
SN6507-Q1	HVSSOP（10 引脚）	3.00mm × 3.00mm

(1) 有关所有的可用封装，请参阅数据表末尾的可订购产品附录。



简化原理图

本文档旨在为方便起见，提供有关 TI 产品中文版本的信息，以确认产品的概要。有关适用的官方英文版本的最新信息，请访问 www.ti.com，其内容始终优先。TI 不保证翻译的准确性和有效性。在实际设计之前，请务必参考最新版本的英文版本。

English Data Sheet: SLLSFM1

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4 Revision History

注：以前版本的页码可能与当前版本的页码不同

DATE	REVISION	NOTES
September 2022	*	Initial Release

5 Pin Configuration and Functions

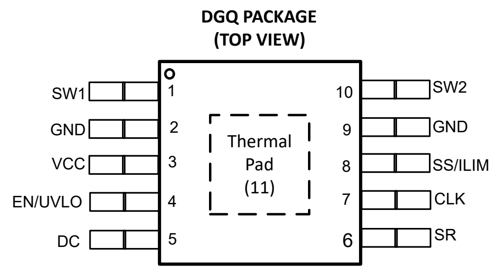


图 5-1. DGQ Package, 10-Pin HVSSOP (Top View)

表 5-1. Pin Functions

PIN			DESCRIPTION
NAME	NO.	TYPE[(1)]	
SW1	1	O	Open drain output of the first power MOSFET, switch 1. Typically connected to either of the outer terminals of the center tap transformer. Because large currents flow through these pins, their external traces should be kept short.
GND	2	GND	Ground connection of internal control circuits and power MOSFET. Pin 2 and Pin 9 must be shorted on PCB for optimzed emissions and efficiency.
VCC	3	P	The VCC pin is the main supply pin for the power and analog circuits. Short duration, high-current pulses are produced during the turn on and turn off of the power switches.
EN/UVLO	4	I	Enable input and undervoltage lockout (UVLO) programming pin. • If the pin voltage is above EN_UVLO threshold , the device is enabled and will start switching when VCC is above VCC_UVLO threshold. • If the pin is shorted to VCC, the device is self-started when VCC is above VCC_UVLO threshold. • If the pin is floating, or the pin voltage is below EN_UVLO threshold, the device stops switching.
DC	5	I	Duty cycle control pin to compensate input variation. A resistor on this pin to GND sets the duty cycle. If unused, leave the pin floating, the duty cycle is set to the default value (48%). Duty cyle control is disabled in SYNC mode.
SR	6	I	Slew rate control pin to further optimize emission performance. This pin adjusts slew rate of SW1 and SW2 by connecting a resistor to GND. If the pin is left floating, the device switches at the default slew rate.
CLK	7	I	This pin is used to sync the device with an external clock (SYNC mode) or program the switching frequency by connecting the pin to ground through a resistor. If shorted to GND, the device will switch at its default frequency (1MHz typical). If left floating, the device will stop switching.
SS/ILIM	8	I	Multifunction Soft-Start (SS) and Current-Limit (ILIM) input pin. • A capacitor to GND is needed to set the output soft-start time and input inrush current. • A resistor to GND is needed to protect the device through the programmable current limit.
GND	9	GND	Ground connection of internal control circuits and power MOSFET. Pin 2 and Pin 9 must be shorted on PCB for optimized emissions and efficiency.
SW2	10	O	Open drain output of the second power MOSFET, switch 2. Typically connected to either of the outer terminals of the center tap transformer. Because large currents flow through these pins, their external traces should be kept short.
PowerPAD	11	GND	GND pins (Pin 2 and Pin 9) must be electrically connected to the power pad (Pin 11) on the printed circuit board for proper operation.

(1) I = input, O = output, P = power, GND = ground

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)[1].

		MIN	MAX	UNIT
Supply voltage [2]	V_{CC}	–0.5	60	V
Voltage	EN/UVLO	–0.5	V_{CC} + 0.5	V
Voltage	SS/ILIM, CLK, DC	–0.5	6	V
Output switch voltage	SW1, SW2		85	V
Peak output switch current	$I_{(D1)Pk}$, $I_{(D2)Pk}$		1.6	A
Junction temperature, T_J		-55	150	°C
Storage temperature range, T_{stg}		–65	150	°C

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) All voltage values are with respect to the local ground terminal (GND) and are peak voltage values.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002[1] HBM ESD Classification Level 3A	±4000	V
		Charged-device model (CDM), per AEC Q100-011 CDM ESD Classification Level C6	±1500	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.3 Recommended Operating Conditions

			MIN	NOM	MAX	UNIT
V_{CC}	Input Voltage		3		36	V
I_{SW1}, I_{SW2}	Output switch current - Primary side	3 V < V_{CC} < 6 V			0.4	A
		6 V < V_{CC} < 36 V			0.5	
T_A	Ambient temperature		–55		125	°C
T_J	Junction temperature		–55		150	°C
C_{SS}	Soft-start capacitor on SS/ILIM pin		0.05		10	µF
R_{ILIM}	Current limiting resistor on SS/ILIM pin		18		261	kΩ
R_{SR}	Resistor on SR pin for Slew rate control		4.8		21	kΩ
R_{CLK}	Resistor on CLK pin for programmable frequency		4		111	kΩ

6.4 Thermal Information

THERMAL METRIC[1]		SN6507 DGQ (HVSSOP) 10 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	48.2	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	61.6	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	18.4	°C/W
ψ_{JT}	Junction-to-top characterization parameter	1.7	°C/W
ψ_{JB}	Junction-to-board characterization parameter	18.3	°C/W
$R_{\theta JC(bottom)}$	Junction-to-case(bottom) thermal resistance	5.8	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.5 Electrical Characteristics

Minimum and maximum limits apply over the recommended junction temperature range, unless otherwise indicated. All typical values are at T_A = 25°C, V_{CC} = 24 V, CLK F_{SW} = 1 MHz and $V_{EN/UVLO}$=2.5 V unless otherwise stated.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY CURRENT						
I_{cc}	VIN Supply Current (3 V < V_{CC} < 36V) , not including switch drive currents	$V_{EN/UVLO}$=2.5 V, R_L = 50 Ω		3	4	mA
$I_{SHUTDOWN}$	VIN shutdown current	$V_{EN/UVLO}$=0 V, R_L = 50 Ω		0.8	2.5	µA
$I_{LKG(SS/ILIM)}$	Leakage Current on SS/ILIM pin	$V_{EN/UVLO}$ = 0 V, Voltage of SS/ILIM = 5 V			0.7	µA
ENABLE AND UVLO						
$VCC_{UVLO-RISING}$	VCC Positive-going UVLO threshold	V_{CC} rising , EN/UVLO is shorted to V_{CC}		2.8	2.9	V
$VCC_{UVLO-FALLING}$	VCC Negative-going UVLO threshold	V_{CC} falling, EN/UVLO is shorted to V_{CC}	2.5	2.67		V
$VCC_{UVLO-HYS}$	VCC UVLO threshold hysteresis	EN/UVLO is shorted to V_{CC}	0.1	0.12		V
$EN_{UVLO-RISING}$	EN/UVLO Positive-going UVLO threshold	EN/UVLO rising	1.4	1.5	1.6	V
$EN_{UVLO-FALLING}$	EN/UVLO Negative-going UVLO threshold	EN/UVLO falling	1.25	1.35	1.45	V
$EN_{UVLO-HYS}$	EN/UVLO UVLO threshold hysteresis		0.14	0.15		V
POWER STAGE						
DMM	Average ON time mismatch between SW1 and SW2	R_L = 50 Ω to V_{CC}, Pull-Up Resistor Test Circuit Configuration		0		%
$R_{(ON)}$	Output switch ON resistance	V_{CC} = 24 V, I_{SW1}, I_{SW2} = 0.5 A		0.45	1	Ω
$V_{(SLEW)}$	Voltage slew rates on SW1 and SW2	R_L = 50 Ω to V_{CC}, V_{CC} = 12 V; R_{SR} = 9.6 kΩ (Default), Pull-Up Resistor Test Circuit Configuration		298		V/µs
$V_{(SLEW)}$	Voltage slew rates on SW1 and SW2	R_L = 50 Ω to V_{CC}, V_{CC} = 12 V; R_{SR} = 9.6 kΩ (Default), Pull-Up Resistor Test Circuit Configuration		369		V/µs
CLK						
F_{SW}	D1, D2 average switching Frequency (Default)	R_L = 50 Ω , R_{CLK} = 0 kΩ, Pull-Up Resistor Test Circuit Configuration	780	1000	1296	kHz
$F_{(SYNC)}$	External clock frequency on CLK pin	External clock applied on CLK pin for SYNC mode. SW1/SW2 switches at 1/2 the external CLK frequency	200		4000	kHz
$V_{CLK(High)}$	CLK pin logic high threshold			1.6	1.8	V
$V_{CLK(Low)}$	CLK pin logic low threshold		1.0	1.2		V
SOFT-START						
I_{SS}	SS ext capacitor charging current			275		µA
C_{SS} Range	SS ext capacitor range		0.05		5	µF
CURRENT LIMIT						
I_{LIM}	SW1 and SW2 Current Limit	R_{LIM} = 18.2 kΩ, 5 V < V_{CC} < 36 V	1.00	1.30	1.59	A
I_{LIM}	SW1 and SW2 Current Limit	R_{LIM} = 30.1 kΩ, 5 V < V_{CC} < 36 V	0.56	0.79	1.02	A
I_{LIM}	SW1 and SW2 Current Limit	R_{LIM} = 261 kΩ, 5 V < V_{CC} < 36 V	0.06	0.10	0.14	A

Minimum and maximum limits apply over the recommended junction temperature range, unless otherwise indicated. All typical values are at T_A = 25°C, V_{CC} = 24 V, CLK F_{SW} = 1 MHz and $V_{EN/UVLO}$=2.5 V unless otherwise stated.

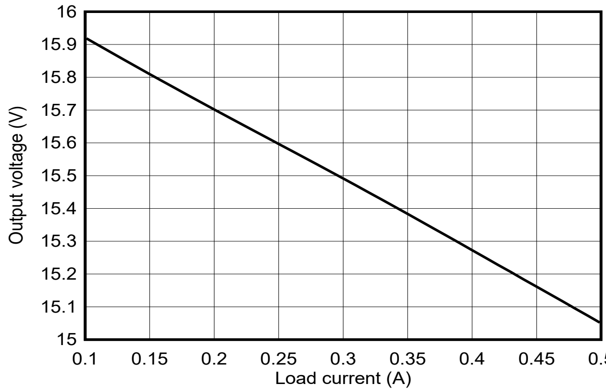
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
DC CONTROL						
D_{sw1}, D_{sw2}	Switching Duty Cycle on SW1 and SW2	DC pin floating (Default), F_{SW} = 300KHz, Timing Diagram		48		%
D_{sw1}, D_{sw2}	Switching Duty Cycle on SW1 and SW2	External CLK (SYNC mode), F_{SW} = 300KHz, Timing Diagram		48		%
INPUT OVLO						
$VCC_{OVLO\text{-}RISING}$	Input Over-voltage Lockout Rising Threshold	V_{CC} rising	36.9	38.7	40.5	V
$VCC_{OVLO\text{-}FALLING}$	Input Over-voltage Lockout Falling Threshold	V_{CC} falling	36.5	38.2	40.0	V
$VCC_{OVLO\text{-}HYS}$	Input Over-voltage Lockout Hysteresis	V_{CC} hysteresis voltage	0.47	0.57		V
THERMAL SHUT DOWN						
T_{SD+}	T_{SD} turn on temperature	T_J rising	170	184	198	°C
T_{SD-}	T_{SD} turn off temperature	T_J falling	135	147	159	°C
$T_{SD\text{-}HYST}$	T_{SD} hysteresis		32	37	42	°C

6.6 Switching Characteristics

Minimum and maximum limits apply over the recommended junction temperature range, unless otherwise indicated. All typical values are at T_A = 25°C, V_{CC} = 24 V, CLK F_{SW} = 1 MHz and $V_{EN/UVLO}$=2.5 V unless otherwise stated.

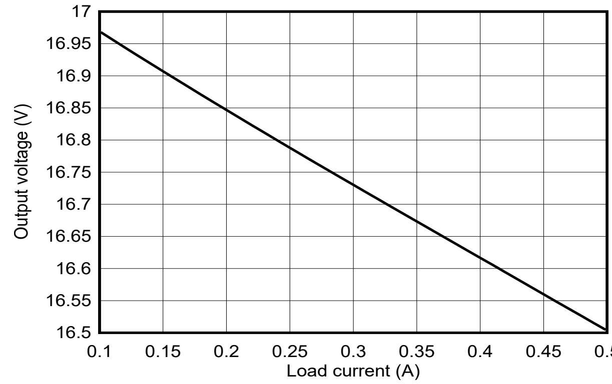
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
ENABLE AND UVLO						
T_{EN_glitch}	EN glitch filter		5			µs
POWER STAGE						
t_{BBM}	Break-before-make time	Measured at 0.5V_{CC} with R_L = 50 Ω, F_{SW} = 1 MHz, R_{SR} = 9.6 kΩ (or Default), Timing Diagram		70		ns
SOFT-START						
t_{PWRUP}	Power-up time	C_{SS} = 0 µF, from EN = High to full drive-current available at S_{W1} and S_{W2}		300	400	µs
t_{PWRDN}	Power-down time	C_{SS} = 0 µF, from EN = Low to output MOSFETs off (no current on S_{W1} and S_{W2})			30	µs

6.7 Typical Characteristics, SN6507-Q1



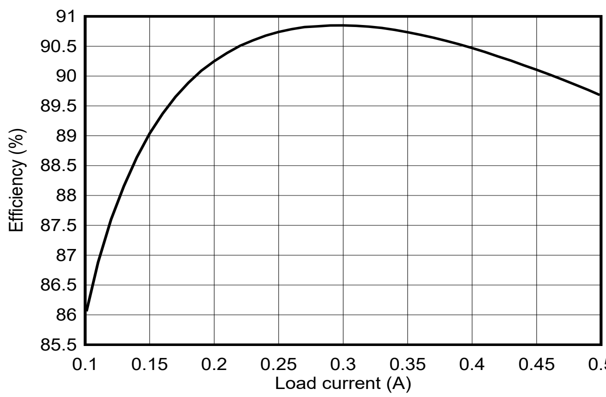
SN6507-Q1 + Wurth 750319692 V_{IN} = 12 V

图 6-1. Output Voltage vs Load Current



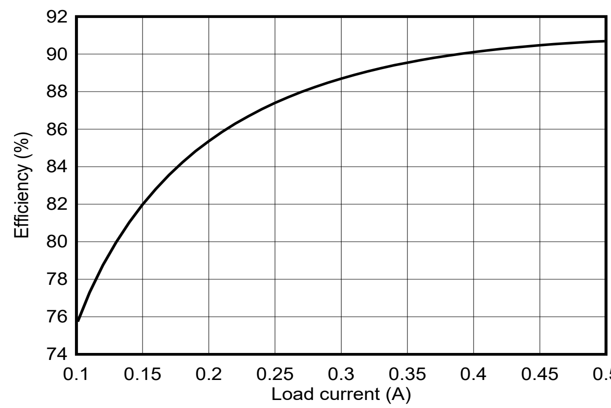
SN6507-Q1 + Wurth 750319696 V_{IN} = 24 V

图 6-2. Output Voltage vs Load Current



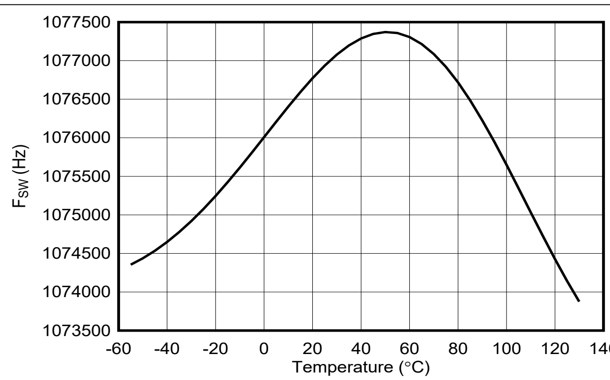
SN6507-Q1 + Wurth 750319692 V_{IN} = 12 V

图 6-3. Efficiency vs Load Current



SN6507-Q1 + Wurth 750319696 V_{IN} = 24 V

图 6-4. Efficiency vs Load Current



R_{CLK} = 0 kΩ

图 6-5. Switching Frequency vs Free-Air Temperature

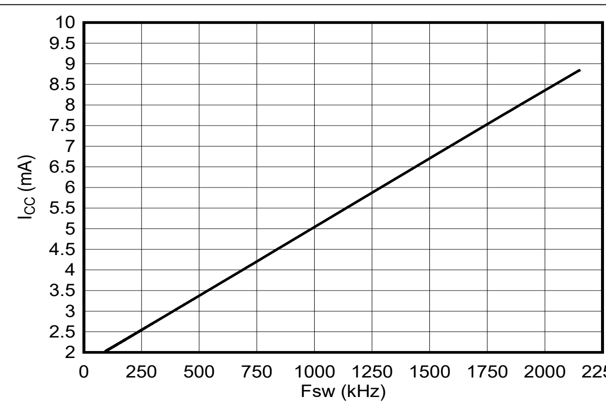


图 6-6. I_{CC} vs Switching Frequency

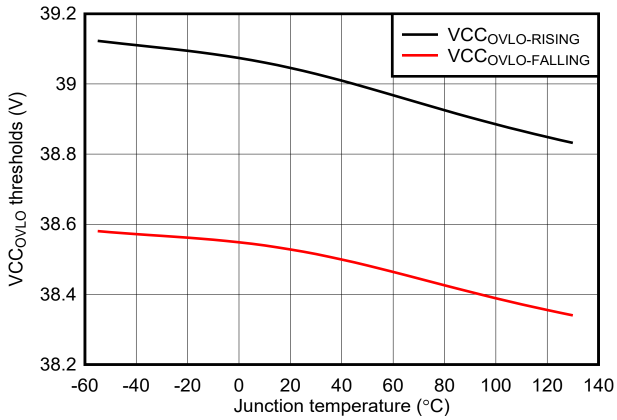


图 7-3 R_L = 50 Ω

图 6-7. V_{CC} OVLO Thresholds vs Junction Temperature

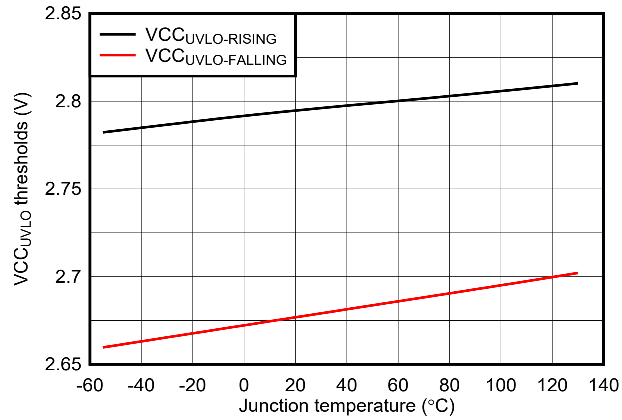


图 7-3 R_L = 50 Ω

图 6-8. V_{CC} UVLO Thresholds vs Junction Temperature

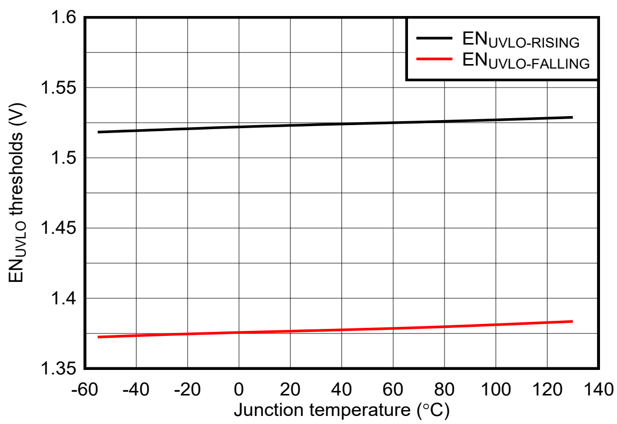


图 7-3 R_L = 50 Ω

图 6-9. EN/UVLO Thresholds vs Junction Temperature

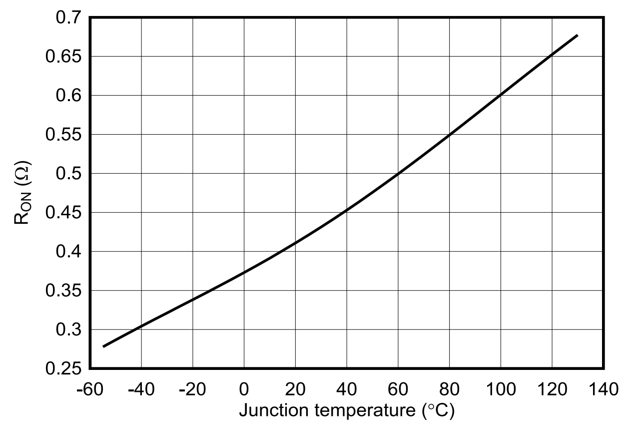


图 7-3 R_L = 50 Ω

图 6-10. R_{ON} vs Junction Temperature

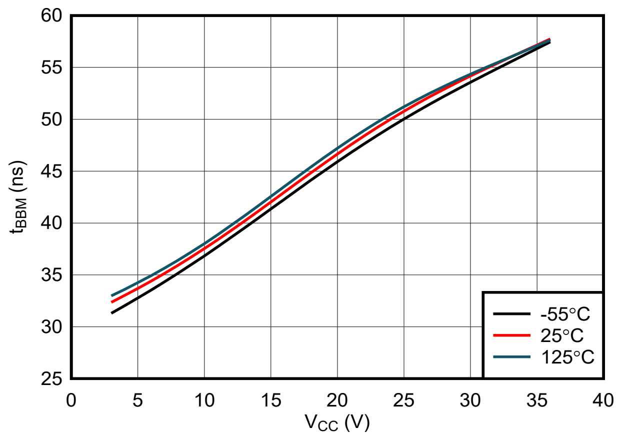


图 7-3 R_L = 50 Ω

图 6-11. Break-Before-Make Time vs V_{CC}

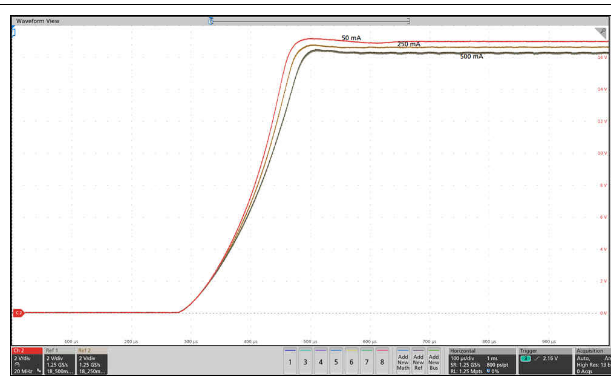


图 7-1 SN6507-Q1 + Wurth 750319696
V_{IN} = 24 V RILIM = 18.2 kΩ C_{SS} = 50 nF

图 6-12. Output Voltage During Soft Start with 50-mA, 250-mA, and 500-mA Loads

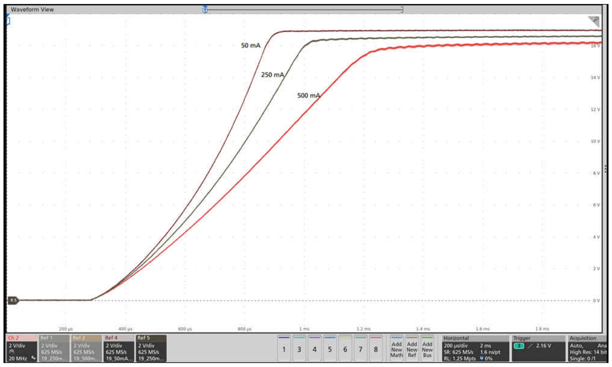


图 7-1 SN6507-Q1 + Wurth 750319696

V_{IN} = 24 V RILIM = 18.2 kΩ C_{SS} = 500 nF

图 6-13. Output Voltage During Soft Start with 50-mA, 250-mA, and 500-mA Loads

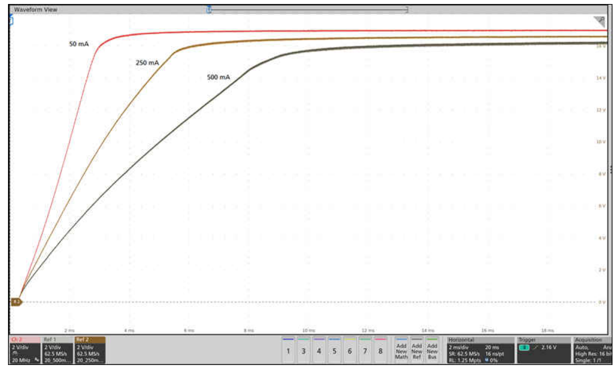


图 7-1 SN6507-Q1 + Wurth 750319696

V_{IN} = 24 V RILIM = 18.2 kΩ C_{SS} = 5 µF

图 6-14. Output Voltage During Soft Start with 50-mA, 250-mA, and 500-mA Loads

7 Parameter Measurement Information

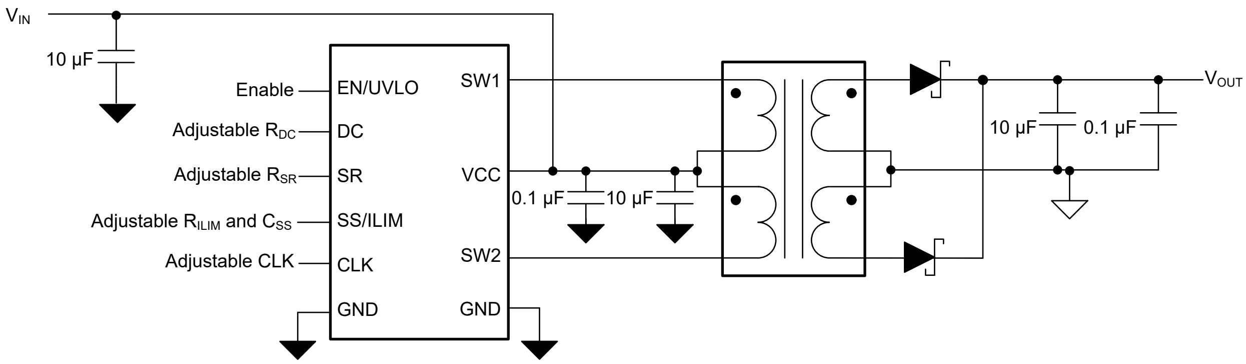


图 7-1. Measurement Circuit for Output

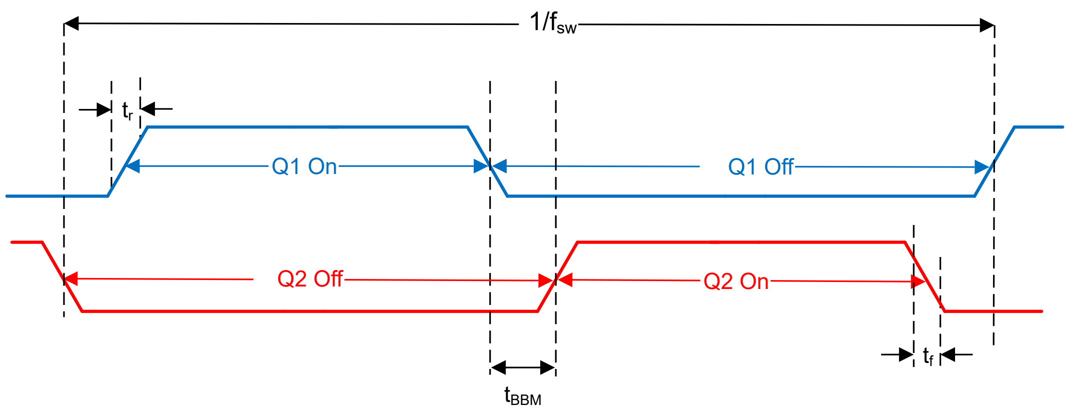


图 7-2. Timing Diagram

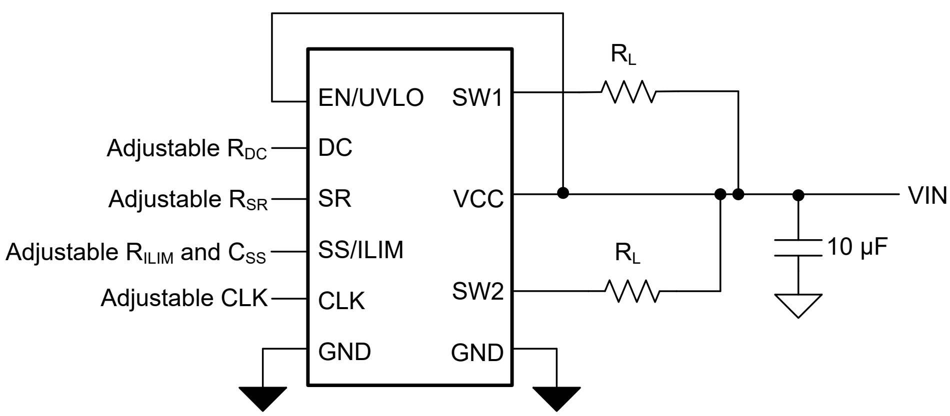


图 7-3. Pull-Up Resistor Test Circuit Configuration

8 Detailed Description

8.1 Overview

The SN6507-Q1 is a 36-V, 0.5-A push-pull transformer driver with two integrated n-channel power MOSFETs. It is designed for low cost, small size, low EMI isolated DC/DC power supplies.

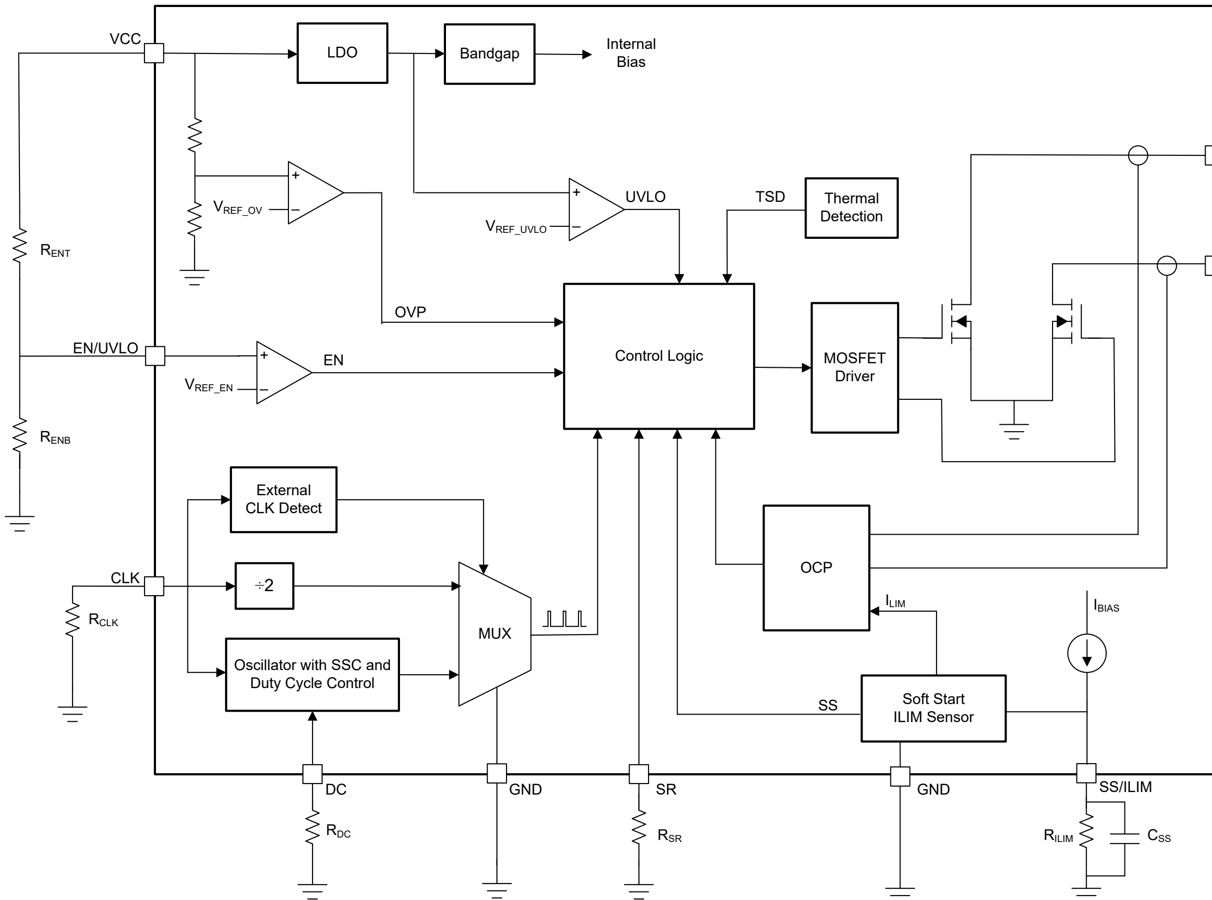
The device includes an oscillator that feeds a gate-drive circuit. The gate-drive, comprising a frequency divider and a break-before-make (BBM) logic, provides two complementary output signals which alternately turn the two output NMOS transistors on and off. A subsequent break-before-make logic inserts a dead-time between the high-pulses of the two signals to avoid shorting out both ends of the transformer's primary windings. The resulting output signals drive an isolation transformer and rectifier, converting the input voltage to an isolated output voltage.

To improve performance at wide-input applications, the device implements a Duty Cycle Control (DCC) feature that the duty cyle is dynamically adjusted to compensate for the input variation. It removes the need of pre-regulation if the input variation is within a certain degree. Or even if at wide input conditions where the input variation is out of regulation range, it saves secondary-side LDO size and power loss. The wide switching frequency range allows for better efficiency and smaller output ripple, as well as size optimization when selecting the transformers.

The transformer driver comes with multiple protection features to ensure robust operation, such as programmable overcurrent protection (OCP), input OVP, input UVLO and TSD. The device minimizes excessive output overvoltage transients by taking advantage of the overvoltage comparator. When the overvoltage comparator is activated, the MOSFETs are turned off and prevented from turning on until the overvoltage condition is removed. The device implements overload protection for both MOSFETs which help control the transformer current and avoid transformer saturation. It also shuts down if the junction temperature is higher than the thermal shutdown trip point. A programmable soft-start period reduces the inrush current during start-up and fault recovery.

For ultra-low EMI applications, the slew rate control feature provides design flexibility and simplicity to further improve emissions with a resistor-programmable option.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Push-Pull Converter

Push-pull converters require transformers with center-taps to transfer power from the primary to the secondary as shown in 图 8-1. When Q_1 conducts, V_{IN} drives a current through the lower half of the primary to ground, thus creating a negative voltage potential at the lower primary end with regards to the V_{IN} potential at the center-tap. .

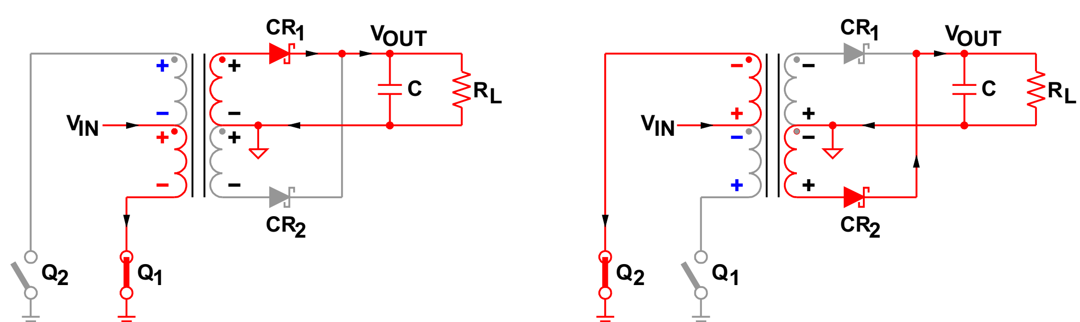


图 8-1. Switching Cycles of a Push-Pull Converter

At the same time the voltage across the upper half of the primary is such that the upper primary end is positive with regards to the center-tap in order to maintain the previously established current flow through Q_2, which now has turned high-impedance. The two voltage sources, each of which equaling V_{IN}, appear in series and cause a voltage potential at the open end of the primary of $2 \times V_{IN}$ with regards to ground.

Per dot convention the same voltage polarities that occur at the primary also occur at the secondary. The positive potential of the upper secondary end therefore forward biases diode CR_1. The secondary current starting from the upper secondary end flows through CR_1, charges capacitor C, and returns through the load impedance R_L back to the center-tap.

When Q_2 conducts, Q_1 goes high-impedance and the voltage polarities at the primary and secondary reverse. Now the lower end of the primary presents the open end with a $2 \times V_{IN}$ potential against ground. In this case CR_2 is forward biased while CR_1 is reverse biased and current flows from the lower secondary end through CR_2, charging the capacitor and returning through the load to the center-tap.

8.3.2 Core Magnetization

图 8-2 shows the ideal magnetizing curve for a push-pull converter with B as the magnetic flux density and H as the magnetic field strength. When Q_1 conducts the magnetic flux is pushed from A to A’, and when Q_2 conducts the flux is pulled back from A’ to A. The difference in flux and thus in flux density is proportional to the product of the primary voltage, V_P, and the time, t_{ON}, it is applied to the primary: $B \approx V_P \times t_{ON}$.

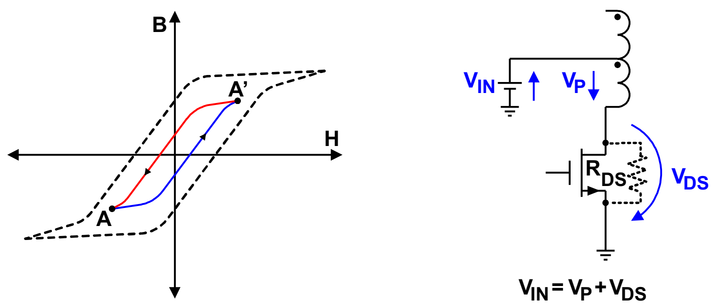


图 8-2. Core Magnetization and Self-Regulation Through Positive Temperature Coefficient of $R_{DS(on)}$

This volt-seconds (V-t) product is important as it determines the core magnetization during each switching cycle. If the V-t products of both phases are not identical, an imbalance in flux density swing results with an offset from the origin of the B-H curve. If balance is not restored, the offset increases with each following cycle and the transformer slowly creeps toward the saturation region.

Fortunately, due to the positive temperature coefficient of a MOSFET’s on-resistance, the output FETs of the SN6507-Q1 have a self-correcting effect on V-t imbalance. In the case of a slightly longer on-time, the prolonged current flow through a FET gradually heats the transistor which leads to an increase in $R_{DS\text{-}on}$. The higher resistance then causes the drain-source voltage, VDS, to rise. Because the voltage at the primary is the difference between the constant input voltage, V_{IN}, and the voltage drop across the MOSFET, $V_P = V_{IN} - V_{DS}$, $V_P$is gradually reduced and V-t balance restored.

8.3.3 Duty Cycle Control

The SN6507-Q1 implements a duty cycle control feature to provide line regulation to a certain degree through a resistor on DC pin. By making the DC pin voltage a function of the input, the duty cycle will adjust with V_{IN}, so that V_{OUT} can be kept constant. Compared to fixed duty cycle transformer drivers, this dynamic duty cycle control feature reduces LDO power loss for wide V_{IN} variations by pseudo-regulating the output. For applications where input variation is within a certain range, this feature can eliminate the post-regulation LDO. Another benefit of duty cycle control is to reduce the transformer cost and size because of the limited input range to primary side of the transformer.

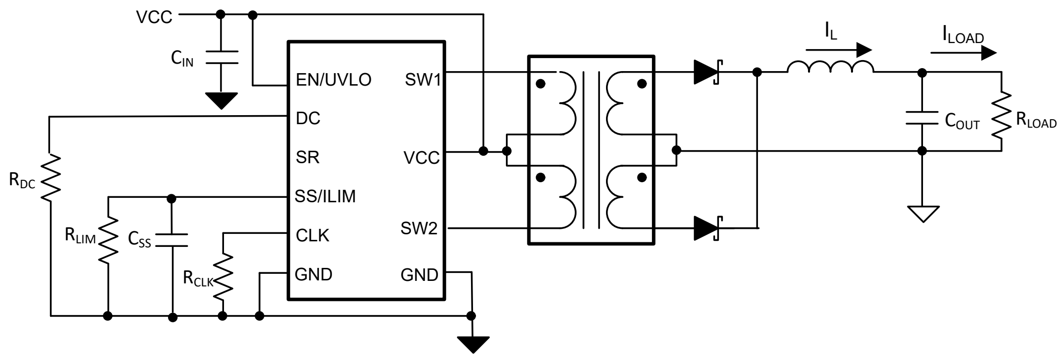


图 8-3. Schematic with duty cycle control

The calculation of DC pin resistor is shown in 方程式 1, where both R_{DC} and R_{CLK} are in kΩ.

$$R_{DC} = 0.816 \times D \times VCC \times (R_{CLK} + 1) - 1 \quad (1)$$

For fixed oscillator cases where R_{CLK} is shorted to GND, a value of R_{CLK} = 9.6kΩ should be used in the equation above to calculate R_{DC}.

The duty cycle control can compensate for input variation up to ±35%, where line regulation within ±5% can be achieved. To achieve this range, it is recommended that duty cycle at nominal V_{IN} is centered at 25% (D = 0.25). The transformer turns ratio needs take this duty cycle into calculation to ensure the expected output voltage level at all V_{IN} voltages, as discussed in 节 9.2.2.5.

The duty cycle control features supports up to a certain duty cycle and V_{IN} range. The minimum duty cycle is determined by the charge and discharge time of the gate capacitance of Power FETs, while the maximum duty cycle is limtied by the dead time (70 ns typical). For example, at 1 MHz, the adjustable duty cycle is between 10% and 43%. Exceeding above duty cycle range, the line regulation may saturate and input compensation does not work anymore. Meanwhile, if the duty cycle is lower than the minimum spec, the part may hit current limit at heavy loads. The V_{IN} range that duty cycle feature is applicable is from 6 V to 36 V.

To enable the duty cycle control feature, an inductor is required on the output side. The selection of the output inductor should make sure the inductor current will not go into discountinous conduction mode (DCM), meaning the inductor current ramp should not drop to zero at any time. The minimum inductance L_{MIN} is therefore calculated by the conditions that the part stays in continuous conduction mode (CCM) where the load DC current is smaller than half the current ramp amplitude seen on the inductor. Therefore L_{MIN} is a function of the load current and switching frequency as shown by below equation where I_{load} is in A, f_{SW} is in Hz, D is the duty cycle as a decimal (for 25% duty cycle, 0.25 would be used), and L_{min} is in H.

$$L_{MIN} = V_{OUT} \times \frac{1 - 2 \times D \times (V_{IN\,TYP}/V_{IN\,MAX})}{4 \times I_{LOAD\,MIN} \times f_{SW}} \quad (2)$$

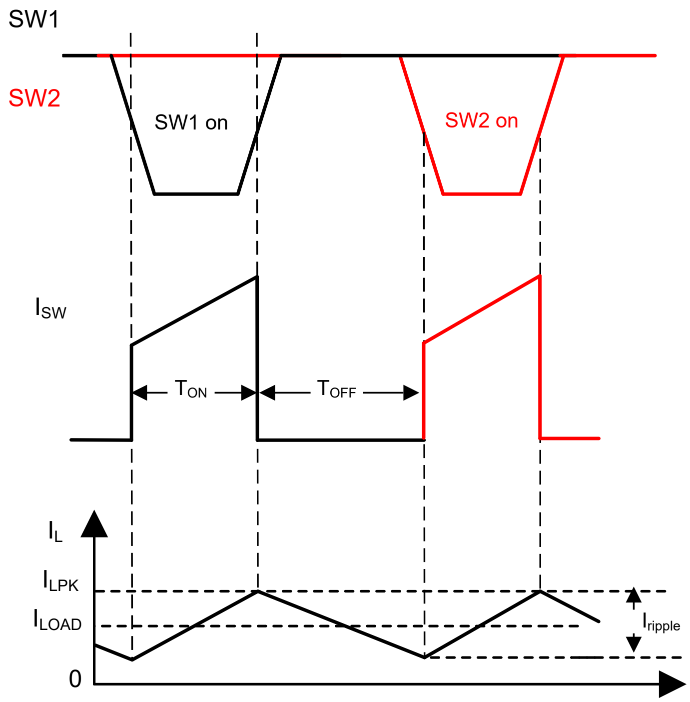


图 8-4. Waveforms in Continuous Conduction Mode (CCM)

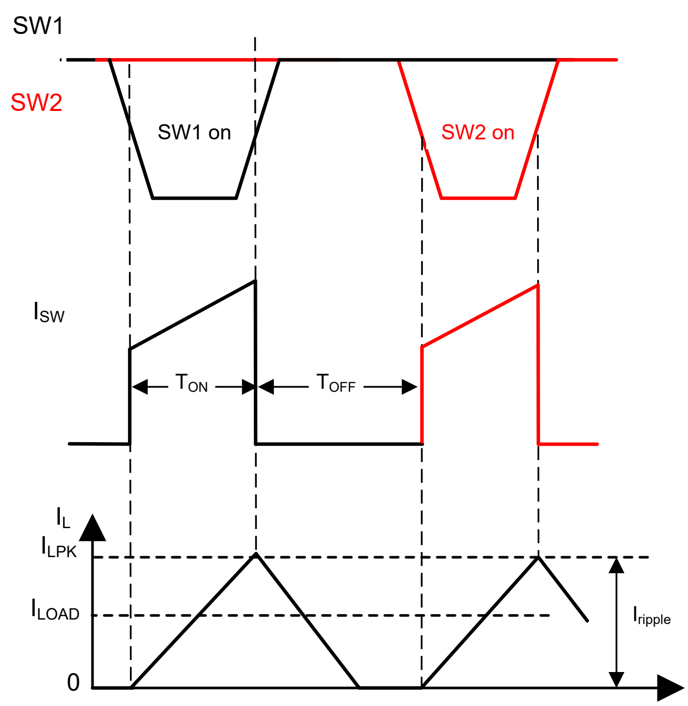


图 8-5. Waveforms in Discontinuous conduction Mode (DCM)

Programmable Switching Frequency

SN6507-Q1 has an internal oscillator to set the switching frequency of the power stage. As the two power switches are out of phase, the oscillator frequency is twice of the actual switching frequency of each power switch. The duty cycle is fixed with 70 ns deadtime to avoid shoot-through. The duty cycle is changeable if duty cycle feature is enabled. Please refer to 节 8.3.3.

SN6507-Q1 has a wide switching frequency range from 100 kHz up to 2 MHz, which is pin-programmable through a resistor (R_{CLK}) to GND. Below table lists the value of R_{CLK} to achieve certain operating frequencies (f_{SW}). The choice of switching frequency is a trade-off between power efficiency and size of capacitive and inductive components. For example, when operating at higher switching frequency, the size of the transformer and inductor is reduced, resulting in a smaller design footprint and lower cost. However, higher frequency increases switching losses and consequently degrades the overall power supply efficiency.

表 8-1. Recommended 1% R_{CLK} values and f_{SW} Look-up Table

R_{CLK}	f_{SW} (Typical)
111 kΩ	105 kHz
21 kΩ	523 kHz
9.6 kΩ	1.07 MHz
4.1 kΩ	2.13 MHz
0 kΩ (Short to GND)	Default (1 MHz)

图 8-6 can also be used to estimate the programmable switching frequency, f_{SW}, using an external resistor value, R_{CLK}, where R_{CLK} is in kΩ and f_{SW} is in kHz:

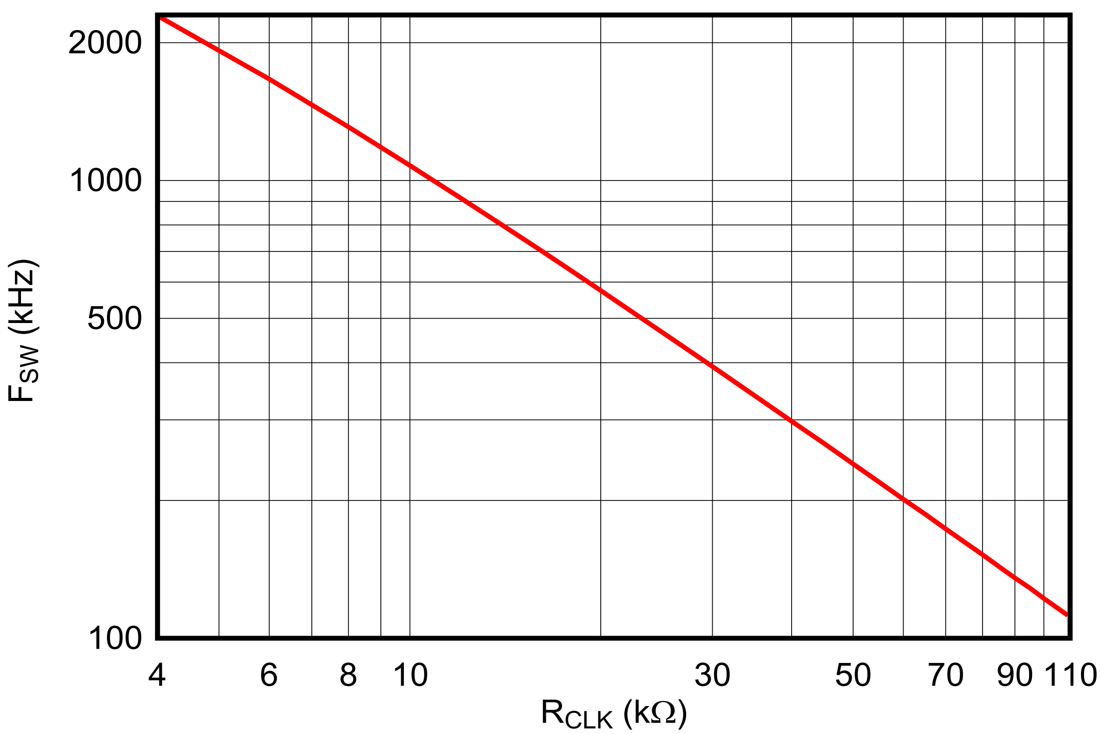


图 8-6. Approximate SN6507-Q1 Switching Frequency, F_{SW}, for R_{CLK} Range

If CLK pin is shorted to GND, the part switches at its default frequency, F_{SW}. CLK pin floating is not a valid state of operation and will cause the part to stop switching until an external clock signal is present.

8.3.4 Spread Spectrum Clocking

Radiated emissions is an important concern in high current switching power supplies. Due to the periodicity of the digital clock signals, the energy concentrates in one particular frequency and also in its odds harmonics, causing EMI issues. SN6507-Q1 implements Spread spectrum clocking (SSC) to reduce the radiated emissions of digital clock signals. The device modulates its internal clock in such a way that the emitting energy is spread over multiple frequency bins. This feature greatly improves the emissions performance of the entire power supply block and hence relieves the system designer from one major concern in isolated power supply design.

8.3.5 Slew Rate Control

To allow optimization of EMI with respect to efficiency, the SN6507-Q1 is designed to allow a resistor (R_{SR}) to select the strength of the driver of PowerFETs turning on. As shown in 图 8-7 below, the slew rate of the switching edges is controllable with the resistor. Rolling off harmonics through slew rate control can eliminate the need for shielding and common mode chokes in many applications.

The EMI benefit of slew rate control may result in slightly reduced efficiency and higher peak current (I_{SW_SR}). When the feature slows down the charging and discharging of the gate capacitance, the extended transition times of the FETs increases the transition losses during each switching cycle. This increases power dissipation, which decreases efficiency and exacerbates thermal concerns. This will limit how much the slew rate can be reduced. Another cost is the peak current of each cyle will be increased. It is because the slow edges reduce the on-time (I_{ON_SR}) and eventually the peak current (I_{SW_SR}) will increase to deliver the same average current to the load on each cycle.

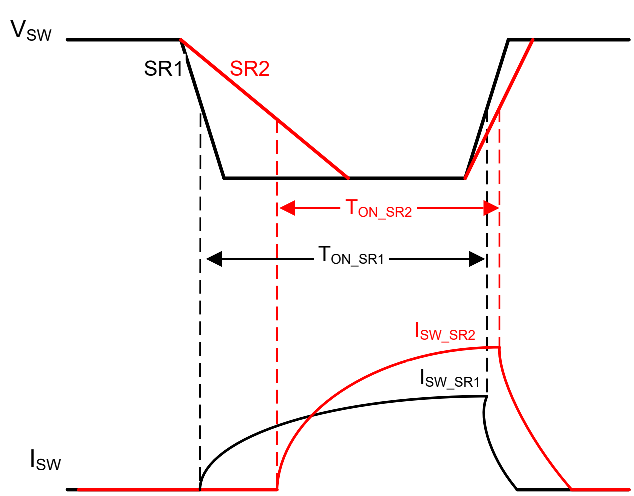


图 8-7. Slew Rate Control Scheme

The slew rate at different V_{IN} is programmed by R_{SR}. Higher R_{SR} values configure SN6507-Q1 for slower slew rates across V_{CC} levels while lower R_{SR} values configure SN6507-Q1 for faster slew rates. The relationship between V_{CC} and the slew rate for 12 V and 24 V cases are listed in 表 8-2 below. As the slew rate is independent of the switching frequency, care must be taken that at high frequencies, the slew rate should be fast enough to maximize the output power delivery to the load. If the SR pin is left floating, the slew rate will be set to the default value. An SR pin short to GND is read as a fault condition, and the device will stop switching.

表 8-2. Slew Rate Control Look-up Table

VCC (V)	R_{SR} (kΩ)	Typical SLEW RATE (V/µs)
5	4.8	337
5	Floating (Default)	263
5	15	224
5	21	198
12	4.8	424
12	Floating (Default)	298
12	15	237
12	21	199

表 8-2. Slew Rate Control Look-up Table (continued)

VCC (V)	R_{SR} (kΩ)	Typical SLEW RATE (V/μs)
24	4.8	583
24	Floating (Default)	369
24	15	273
24	21	218

8.3.6 Protection Features

SN6507-Q1 is protected by multiple protection features to improve the system level robustness and reliability. The protection features include programmable input undervoltage protection (UVLO), input over-voltage protection (OVP), programmable over current protection (OCP), and over-temperature protection (TSD).

8.3.6.1 Over Voltage Protection (OVP)

As SN6507-Q1 is a open-loop transformer driver, the over voltage protection feature is implemented to prevent the output voltage from rising too high. The overvoltage protection threshold is a fixed value and cannot be programmed. If the VCC pin voltage exceeds the overvoltage rising threshold, device stops switching after a 550 ns (typical) response time. To recover from an over voltage event, the input voltage must drop below the OVP falling threshold.

8.3.6.2 Over Current and Short Circuit Protection (OCP)

The SN6507-Q1 is protected from overcurrent conditions with cycle-by-cycle current limiting on both NMOS switches. OCP is disabled during soft-start. After soft-start finishes, the OCP is enabled, and the threshold is set at the programmed value. The switch current is sensed and compared to the current threshold that is programmed by the external resistor on SS/ILIM pin, R_{ILIM}. Common current limit thresholds (I_{LIM}) and their corresponding resistor values for R_{ILIM} are listed in 表 8-3 below. Leaving the ILIM/SS pin floating is not recommended for this device.

表 8-3. Recommended 1% R_{ILIM} values

R_{ILIM}	I_{LIM} (Typical)
18 kΩ	1.3 A
20 kΩ	1.2 A
22 kΩ	1.1 A
24 kΩ	1.0 A
27 kΩ	900 mA
30 kΩ	800 mA
35 kΩ	700 mA
40 kΩ	600 mA
50 kΩ	500 mA
62 kΩ	400 mA
85 kΩ	300 mA
127 kΩ	200 mA
261 kΩ	100 mA

In case of an extreme over-load condition on the isolated output due to a short circuit, the device behaves as follows:

- In the event of a transient overload or short circuit, if the resulting voltage dip is lower than 2.5 V (typical) on the SS/I_{LIM} pin, the device considers it as a “soft-short” condition. In soft-shorts, the converter goes into hiccup mode: on hitting the programmed OCP threshold, the driver will be shut-off for 100 ns (typical), and then retry driving. If the OCP trips again, the cycle continues. This retry keeps occurring for entire T_{ON} time of SW1 and SW2 until OCP does not trip or a "hard-short" is triggered. During the OCP retry events, both FETs are turned OFF, and the transient peak current may go higher than OCP limit.

- If the voltage dip is more than 2.5 V (typical), the devices considers it as a "hard-short" condition. The hard-short OCP threshold is fixed at 5 A (typical). If a hard-short condition lasts more than 200 μs, it indicates that the system is in a serious short-circuit fault condition, the device will fully discharge the soft-start cap and enters soft start once the short circuit is cleared. Note there is a 65 ns (typ.) response time to trigger hard-short OCP.

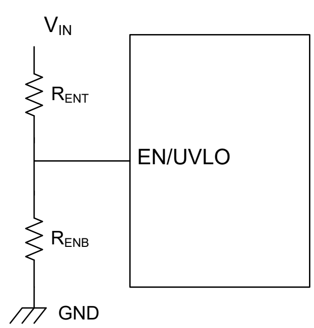
8.3.6.3 Under Voltage Lock-Out (UVLO)

Start-up and shutdown are controlled by the both EN/UVLO pin and VCC pin. For the device to remain in shutdown mode, apply a voltage below EN_{UVLO} to the EN/UVLO pin. In shutdown mode, the quiescent current is less than 0.8 µA (typical). If EN/UVLO pin sees a voltage higher than EN_{UVLO}, but V_{IN} is still below VCC_{UVLO}, the SW node is inactive. Once the V_{IN} is above VCC_{UVLO}, the chip begins to switch normally, provided the EN/UVLO voltage is above 1.5 V.

There are three ways to enable the device operation. The simplest way is to connect the EN/UVLO pin to VCC pin, allowing self-start-up of the device when VCC pin voltage is above VCC_{UVLO} level. However, many applications benefit from an input UVLO level different than that provided internal UVLO. So another way is to employ an enable resistor divider network as shown in Figure below, which establishes a programmable UVLO threshold. The thrid way is to connect an external logic output to drive this pin, allowing user-defined system power sequencing.

EN/UVLO pin has a 5 µs (typical) glitch filter to help avoid false turn-on and turn-off due to noise coupling. It also comes with an internal pull down design to ensure the device is in shutdown mode when the pin is left floating.

Programmable UVLO using EN/UVLO pin



Resistor values can be calculated using Equation below, where the input turn on threshold V_{IN_UVLO} is the desired typical start-up input voltage, EN_{UVLO} is 1.5 V typical, and R_{ENT} and R_{ENB} are in Ω.

$$V_{IN\_UVLO} = \left(1 + \frac{R_{ENT}}{R_{ENB}}\right) \times EN_{UVLO} \tag{3}$$

8.3.6.4 Thermal Shut Down (TSD)

Thermal shutdown prevents the device from reaching extreme junction temperatures by turning off the internal switches when the IC junction temperature exceeds 180°C (typical). In TSD, the switching stops immediately to prevent the internal MOSFETs from failing in either high ambient temperature operation conditions or due to self-heating from high switching current. To recover from thermal shut down condition, the junction temperature must be below the overtemperature protection falling threshold. When the junction temperature falls below 147°C (typical), the power FET switching is enabled.

8.4 Device Functional Modes

The functional modes of the device are divided into start-up, operating, and off-mode.

8.4.1 Start-Up Mode

When VCC pin voltage ramps up to VCC_{UVLO} , and EN/UVLO pin voltage is over EN_{UVLO} the internal oscillator starts operating. The output stage begins switching but the amplitude of the drain signals at SW1 and SW2 have not reached its full maximum yet.

8.4.1.1 Soft-Start

SN6507-Q1 device supports soft-start feature. Upon power up or when EN/UVLO pin transitions from Low to High, the gate drive of the output powerFET is gradually increased over a period of time from 0 V to full driving strength. Soft-start prevents high inrush current from VCC while charging large secondary side decoupling capacitors, and also prevents overshoot in secondary voltage during power-up.

The sort-start time to ramp to the peak switch current is calculated by the capacitor and resistor on SS/ILIM pin with the following formula.

$$T_{SS} = \frac{C_{SS}}{275\mu A - \frac{0.6}{R_{ILIM}}} \tag{4}$$

During soft-start, the over-current protection is disabled. To ensure a smooth transition between soft-start and the steady state, it's recommended to have a C_{SS} value between 50 nF and 5 µF with an output capacitor, C_{OUT}, of less than 10 times the value of C_{SS}.

8.4.2 Operation Mode

The SN6507-Q1 driver is in operation mode when EN pin is above EN_{UVLO}, VIN pin is above VCC_{UVLO}, and soft-start completes. In normal operation mode, the switching frequency is fixed, determined either by the CLK pin resistor or external Clock signal.

8.4.3 Shutdown Mode

The device has a dedicated EN/UVLO pin to put the device in very low power mode to save power when not in use. EN/UVLO pin has an internal pull down resistor which keeps device disabled when not driven. When disabled or when V_{CC} is < 2.8 V , both drain outputs, SW1 and SW2, are tri-stated.

8.4.4 SYNC Mode

The SN6507-Q1 has a CLK pin which can be used to synchronize the device with system clock and in turn with other SN6507-Q1 devices so that the system can control the exact switching frequency of the device. In SYNC mode, the CLK frequency is divided by two to drive the gates of powerFETs. 图 9-2 shows the timing diagram for the same.

The device cannot automatically change from SYNC mode to switching frequency control using the internal oscillator or resistor-programmable switching frequency mode. If a valid external CLK signal is not present, the output will stop switching, and a power cycle will be required to change the switching mode back to using the internal oscillator or the adjustable switching frequency using R_{CLK}.

When the device is in SYNC mode, duty cycle control and SSM are not supported, therefore it's recommended to leave DC pin floating in SYNC mode to reduce the solution size.

Note that it is recommended that the SN6507-Q1 V_{CC} pin powers up before CLK pin. Before device power-up, the initial state of external clock should be high-impedance.

9 Application and Implementation

备注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI’s customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The SN6507-Q1 is a transformer driver designed for low-cost, small form-factor, isolated DC/DC converters using the push-pull topology. The device includes an oscillator that feeds a gate-drive circuit. The gate-drive, comprising a frequency divider and a break-before-make (BBM) logic, provides two complementary output signals which alternately turn the two output transistors on and off.

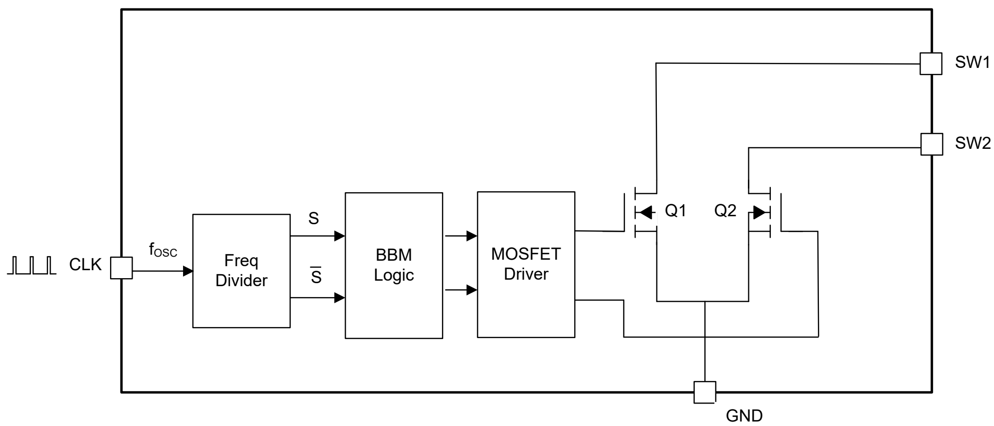


图 9-1. Block Diagram With Break-Before-Make Action

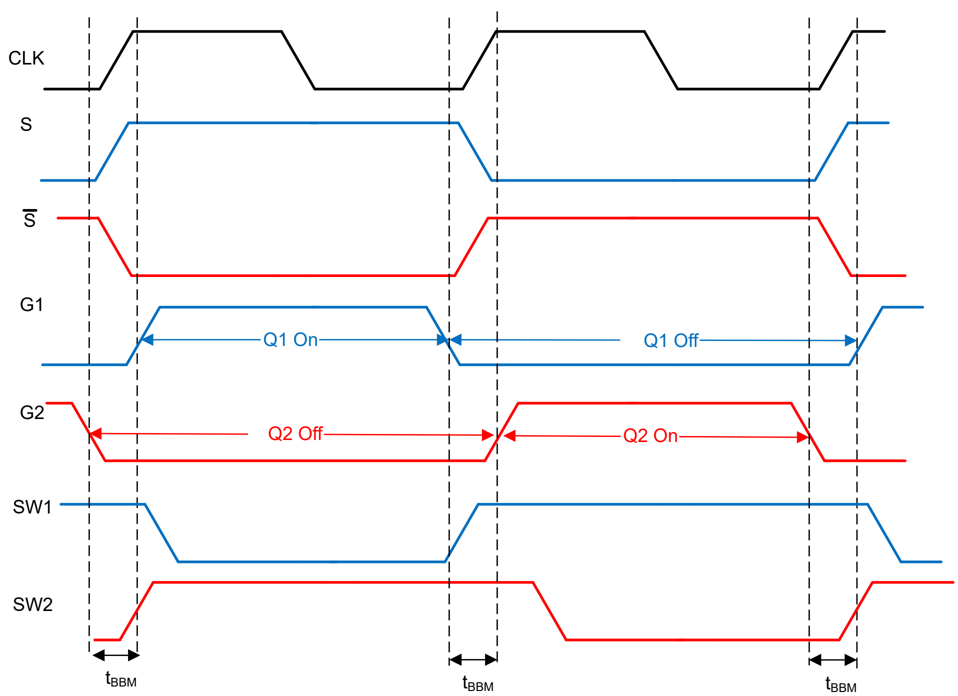


图 9-2. Output timing with Break-Before-Make Action

The output frequency of the oscillator is divided down by an asynchronous divider that provides two complementary output signals, S and $\overline{S}$, with a 50% duty cycle. A subsequent break-before-make logic inserts a dead-time between the high-pulses of the two signals. The resulting output signals, G_1 and G_2, present the gate-drive signals for the output transistors Q_1 and Q_2. As shown in 图 9-2, before either one of the gates can assume logic high, there must be a short time period during which both signals are low and both transistors are high-impedance. This short period, known as break-before-make time, is required to avoid shorting out both ends of the primary.

9.2 Typical Application

Two application cases are discussed. One is for Fixed input with slew rate control. The other is for wide-ranging input with duty cycle control.

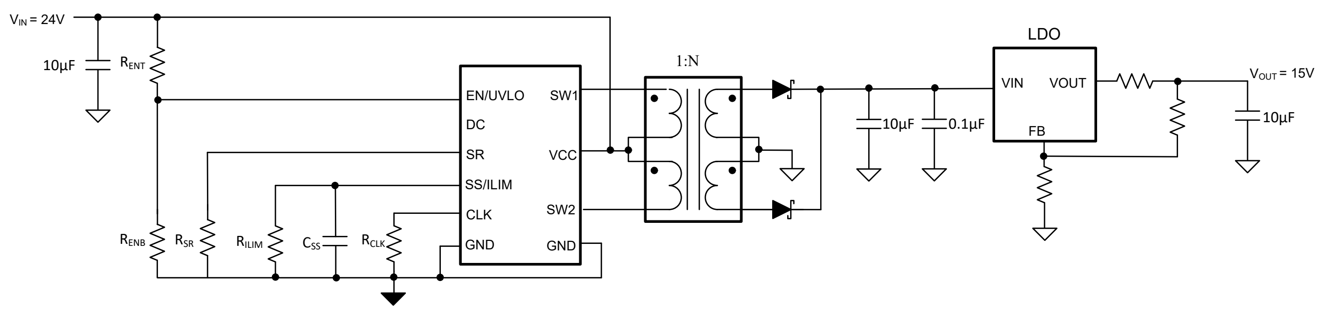


图 9-3. Typical Application Schematic for Fixed Input with Slew Rate Control

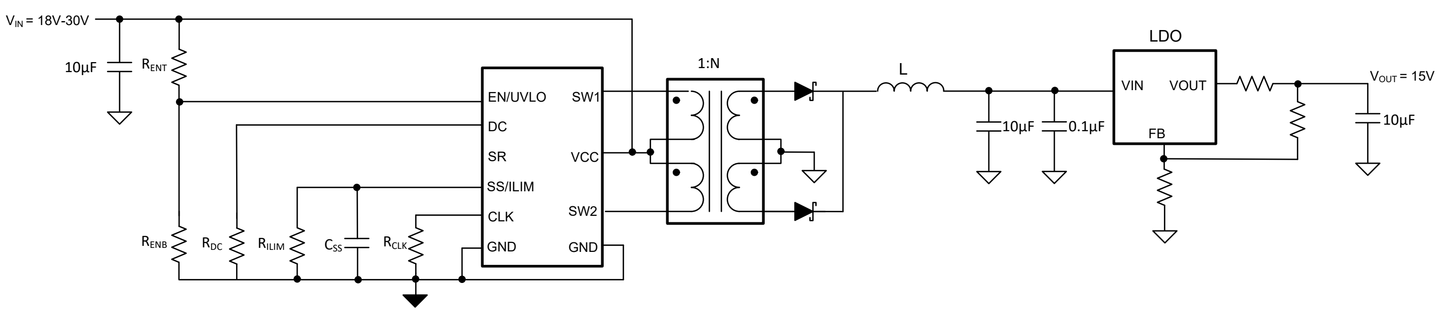


图 9-4. Typical Application Schematic for Wide-Ranging Input with Duty Cycle Control

9.2.1 Design Requirements

For this design example, use the parameters listed in 表 9-1 as design parameters.

表 9-1. Design Parameters

PARAMETER	COMMENT	EXAMPLE VALUE
Fixed V_{IN}	Input voltage for fixed input case	24 V ± 2%
Wide-ranging V_{IN}	Input voltage range for wide-input case	18 V (min) 24 V (typ.) 30 V (max)
f_{SW}	Switching frequency	1 MHz ± 10%
V_{OUT}	Output voltage	15 V
I_{LOAD}	Load current	200 mA
I_{LIM}	Peak Current Limit	500 mA
UVLO	Under Voltage Lockout	9 V
SS	Soft-Start Time	2 ms

9.2.2 Detailed Design Procedure

This section presents a detailed design procedures using the SN6507-Q1 transformer driver. The following recommendations on components selection focus on the design of an efficient push-pull converter with high current drive capability. Two cases are discussed: wide input range with duty cycle control, and a compact design with a fixed input voltage.

The pin configuration of SN6507-Q1 are discussed by 5 simple steps, followed by the selection of external components, including diodes, capacitors, inductor, LDO and transformers.

9.2.2.1 Pin Configuration

Here is an example of how to configure the SN6507-Q1 pins in 5 simple steps.

Step 1: Set the Switching Frequency

First, set the driver switching frequency with R_{CLK} using 表 8-1.

For example: R_{CLK} = 9.6 kΩ or shorted to GND, sets typical f_{SW} at about 1 MHz.

Step 2: Set the Input UVLO

The EN/UVLO (undervoltage lockout) pins are used to set minimum input voltage that the driver starts switching. The resister divider value can be calculated by 方程式 3.

For example, if the input threshold (V_{ON}) is expected to be at 9 V, the resistors are calculated as R_{ENT}/R_{ENB} = 5

Therefore,the resistors values are chosen as:

R_{ENT} = 5 kΩ, R_{ENB} = 1 kΩ

To make the device self-start at default UVLO thresold (2.8 V typical), users can skip Step 2 and directly short the EN/UVLO pin to VCC.

Step 3: Set the Current Limit and Soft-Start Time

The current limit can be set by a resistor on SS/ILIM pin according to 表 8-3. Peak currents may be very high during operation of the overcurrent protection system until the fault is cleared.

For example, to set the current limit is set at 500 mA (typical), the recommended R_{ILIM} is 50 kΩ.

Once R_{ILIM} is determined, substitue R_{ILIM} into 方程式 4, the soft-time calculation is:

$$T_{SS} = \frac{C_{SS}}{275\mu A - \frac{0.6}{50\mathrm{k}}}$$

Taking 2 ms (typical) soft-start time as an example, the capacitor on SS/ILIM pin :C_{SS} = 0.5 uF.

Note that both R_{ILIM} and C_{SS} are required on SS/ILIM pin to ensure the robust operation of this device. Missing the RC connection or leaving the pin floating should be avoided.

Step 4: Set the Duty Cycle

For fixed input cases, the duty cycle feature is not needed. This step can be skipped by leaving DC pin floating, so that the device will operate at default maximum duty (48% typical). The maximum duty cycle is determined by the switching period and the deadtime (70 ns typical) to avoid overlap of two power switches.

For wide-input cases, the duty cycle feature can be enabled by connecting a resistor R_{DC} on DC pin, and an inductor at the output side. The inductor selection is presented in 节 9.2.2.4.

To achieve maximum input compensation, the DC is set close to 0.25 (25% duty cycle) at typical V_{CC} (24 V). The R_{DC} is calculated as 50.9 kΩ by substituting DC = 0.25, V_{CC} = 24 V, and R_{CLK} = 9.6 into 方程式 1, where both R_{CLK} and R_{DC} are in kΩ.

9.2.2.2 LDO Selection

SN6507-Q1 is an open-loop transformer driver without load regulation capability. The output voltage may vary over a wide range load current. Therefore, if a high-accuracy, load independent supply is required, the implementation of a low dropout regulator (LDO) on the output side is strongly advised.

The minimum requirements for a suitable low dropout regulator are:

- Its current drive capability should slightly exceed the specified load current of the application to prevent the LDO from dropping out of regulation. Therefore, for a load current of 200 mA, choose a 200 mA to 300 mA LDO. While regulators with higher drive capabilities are acceptable, they also usually possess higher dropout voltages that will reduce overall converter efficiency.
- The internal dropout voltage, V_{DO}, at the specified load current should be as low as possible to maintain efficiency. For a low-cost 300 mA LDO, a V_{DO} of 600 mV at 300 mA is common. Be aware; however, that this lower value is usually specified at room temperature and can increase by a factor of 2 over temperature, which in turn will raise the required minimum input voltage.
- The required minimum input voltage preventing the regulator from dropping out of line regulation is given with:

  $$V_{I\text{-}min} = V_{DO\text{-}max} + V_{O\text{-}max} \quad (5)$$

  This means in order to determine V_I for worst-case condition, the user must take the maximum values for V_{DO} and V_O specified in the LDO data sheet for rated output current (that is, 200 mA) and add them together. Also specify that the output voltage of the push-pull rectifier at the specified load current is equal or higher than $V_{I\text{-}min}$. If it is not, the LDO will lose line-regulation and any variations at the input passes straight through to the output. Hence, below $V_{I\text{-}min}$ the output voltage follows the input and the regulator behaves like a simple conductor.
- The maximum regulator input voltage must be higher than the rectifier output under no-load. Under this condition there is no secondary current reflected back to the primary, thus making the voltage drop across $R_{DS\text{-}on}$ negligible and allowing the entire converter input voltage to drop across the primary. At this point, the secondary reaches its maximum voltage of

  $$V_{S\text{-}max} = V_{IN\text{-}max} \times N \quad (6)$$

with $V_{IN\text{-}max}$ as the maximum converter input voltage and n as the transformer turns ratio. Thus to prevent the LDO from damage the maximum regulator input voltage must be higher than $V_{S\text{-}max}$. 表 9-2 lists the maximum secondary voltages for various turns ratios commonly applied in push-pull converters.

表 9-2. Required Maximum LDO Input Voltages for Various Push-Pull Configurations

PUSH-PULL CONVERTER				LDO
CONFIGURATION	**$V_{IN\text{-}max}$ [V]**	**TURNS-RATIO (N)**	**$V_{S\text{-}max}$ [V]**	**$V_{I\text{-}max}$ [V]**
24 V_{IN} to 15 V_{OUT}	25	1.38:1	18	25
12 V_{IN} to 15 V_{OUT}	12.5	1:1.5	19	25

9.2.2.3 Diode Selection

A rectifier diode should always possess low-forward voltage to provide as much voltage to the converter output as possible. However, when SN6507-Q1 is used in high-frequency switching applications, the diode must also possess a low total capacitance, a short recovery time and a current rating greater than the load current. Schottky diodes meet these requirements and are therefore strongly recommended in SN6507-Q1 push-pull converter designs.

The necessary diode reverse voltage rating, V_R, is determined by the transformer secondary side voltage plus any voltage ringing. The voltage ringing, however, is difficult to predict, because it depends on multiple factors, such as loop resistance, the leakage inductance of the transformer, and the diode junction capacitance. As a rule of thumb, the diode voltage rating should be greater than 1.5 times the transformer turns ratio multiplied by the maximum input voltage. Because the two secondary windings are connected across the rectifier bridge, a factor of two is needed, producing the diode maximum DC blocking voltage rating:

$$Diode\ \ V_R > 1.5 \times 2 \times N \times V_{IN(MAX)} \tag{7}$$

For high-efficiency designs, diodes with low forward voltage, V_F, and diode capacitance, C_T, can be used, like BAT165E6327HTSA1 or equivalent can be used for high-efficiency 15-V outputs. Diode parameters like these parasitics and reverse recovery will impact system efficiency and can affect emissions. For low-emissions designs, low-emissions diodes can be used, like PMEG200G20ELRX or equivalent can be used for low-emissions outputs up to 100 V.

9.2.2.4 Capacitor and Inductor Selection

Capacitor Selection

The capacitors in the push-pull converter circuits are normally multi-layer ceramic chip (MLCC) capacitors. As with many high speed CMOS ICs, the device requires a bypass capacitor of 100 nF. Ensure this capacitor is placed within 2 mm of the SN6507-Q1 VCC pin.

The input bulk capacitor at the center-tap of the transformer primary side supports large currents into the primary winding during the fast switching transients. For minimum ripple make this capacitor 1 µF to 10 µF, where 10 µF is preferred. Place this capacitor close to the transformer primary winding center-tap to minimize trace inductance. If placed on the opposite side of the PCB from the transformer, an additional 100 nF capacitor can be placed on the same layer and close to the transformer center tap. Use two vias in parallel for each connection between these capacitors to the transformer center tap to ensure low-inductance paths.

The bulk capacitor at the rectifier output smooths the output voltage. Make this capacitor 500 nF to 10 µF. To avoid hitting OCP at the transistion from soft-start to steady state, the output capacitor C_{OUT} is recommended to be less than 10 times of C_{SS} connected to the SS/ILIM pin. Otherwise, if there is a short soft-start time due to a small C_{SS} value, the output capacitor is only partially charged and sees high current spikes on the first switching cycles after the device exits soft start mode.

Optional capacitors of values between 1 nF to 4.7 nF can be connected to the control pins of SN6507-Q1 for filtering if operating in noisy environments.

If an LDO is used, an additional small capacitor at the LDO input is not necessarily required. However, good analog design practice suggests using a small value of 47 nF to 100 nF improves the regulator's transient response and noise rejection.

If an LDO is used, an additional capacitor at the LDO output buffers the regulated output supply for the subsequent isolator and transceiver circuitry. The choice of output capacitor depends on the LDO stability requirements specified in the data sheet. However, in most cases, a low-ESR ceramic capacitor in the range of 4.7 µF to 10 µF will satisfy these requirements.

Inductor Selection

The inductor is required only for duty cycle feature. The minimum inductor value (L_{MIN}) is is calculated by 方程式 2. Higher inductance produces better regulation and lower voltage ripple, but requires a correspondingly larger size inductor. The optimum inductor value is determined by taking into account the tradeoff between the regualtion performance and the size.

For example, when V_{OUT} = 15 V, $V_{IN\ TYP}$ = 15 V, $V_{IN\ MAX}$ = 18 V, $I_{LOAD\ MIN}$ = 250 mA, f_{SW} = 1 MHz, D = 0.25, the minimum inductance is calculated to be 50 µH.

$$L_{MIN} = 15V \times \frac{1 - 2 \times 0.25 \times (15V/18V)}{4 \times 0.25A \times 1MHz} = 8.75\mu H \tag{8}$$

9.2.2.5 Transformer Selection

9.2.2.5.1 V-t Product Calculation

To prevent a transformer from saturation its V-t product must be greater than the maximum V-t product applied by the device: the maximum time this voltage is applied to the primary for half the period of the lowest frequency at the specified input voltage. For designs using duty cycle control, the maximum V-t applied by the device can be calculated by the typical voltage applied for one quarter of the period of the lowest switching frequency. For systems using a clock frequency set by R_{CLK}, f_{min} can be estimated as 15% below the typical or approximate switching frequency value, f_{SW}, for the corresponding R_{CLK} from 节 Programmable Switching Frequency. For systems where the CLK pin is connected to GND, the minimum specified F_{SW} from 节 6 should be used. Therefore, the transformer’s minimum V-t product is determined through 方程式 9 for fixed inputs and 方程式 10 for wide-ranging inputs using duty cycle control:

$$Vt_{min} \geq V_{IN(max)} \times \frac{T_{max}}{2} = \frac{V_{IN(max)}}{2 \times f_{min}} \tag{9}$$

$$Vt_{min} \geq V_{IN(typ)} \times \frac{T_{max}}{4} = \frac{V_{IN(typ)}}{4 \times f_{min}} \tag{10}$$

Example of Fixed Input:

For a fixed input system with $f_{SW(min)}$ of 780 kHz and a V_{IN} = 24 V supply with ±10 % tolerance, 方程式 9 yields the minimum V-t product of:

$$Vt_{min} \geq \frac{26.4V}{2 \times 780kHz} = 16.9\,V\mu s \tag{11}$$

Example of Wide-Ranging Input:

Taking the assumption of $f_{SW(min)}$ as 780 kHz with a $V_{IN(typ)}$ 24 V supply, 方程式 10 yields the minimum V-t product of:

$$Vt_{min} \geq \frac{24V}{4 \times 780kHz} = 7.7\,V\mu s \tag{12}$$

While Vt-wise all of these transformers can be driven by the device, other important factors such as isolation voltage, transformer wattage, and turns ratio must be considered before making the final decision.

9.2.2.5.2 Turns Ratio Estimate

From previous section, it has been determined that the transformer chosen must have a V-t product of 15 Vμs. However, before searching the manufacturer web sites for a suitable transformer, the user still needs to know its minimum turns ratio that allows the push-pull converter to operate flawlessly over the specified current and temperature range. This minimum transformation ratio is expressed through the ratio of minimum secondary to minimum primary voltage multiplied by a correction factor that takes the transformer’s typical efficiency of 97% into account:

$$V_{P\text{-}min} = V_{IN\text{-}min} - V_{DS\text{-}max} \tag{13}$$

$V_{S\text{-}min}$ must be large enough to allow for a maximum voltage drop, $V_{F\text{-}max}$, across the rectifier diode and still provide sufficient input voltage for the regulator to remain in regulation. From the 节 *9.2.2.2* section, this minimum input voltage is known and by adding $V_{F\text{-}max}$ gives the minimum secondary voltage with:

$$V_{S\text{-}min} = V_{F\text{-}max} + V_{DO\text{-}max} + V_{O\text{-}max} \tag{14}$$

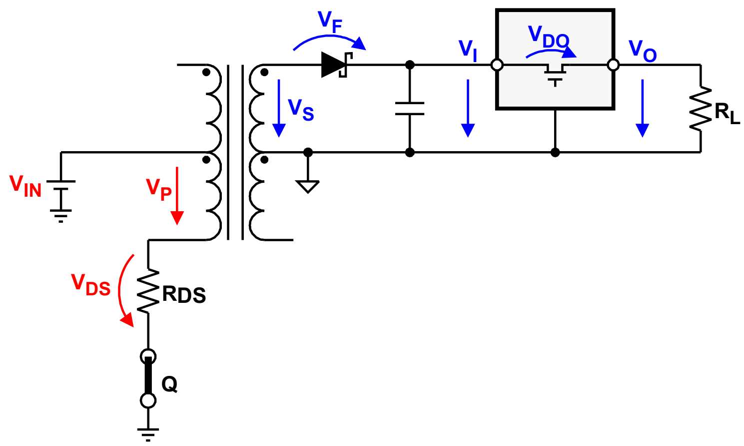


图 9-5. Establishing the Required Minimum Turns Ratio Through N_{min} = 1.03 × $V_{S\text{-}min}$ / $V_{P\text{-}min}$

Then calculating the available minimum primary voltage, $V_{P\text{-}min}$, involves subtracting the maximum possible drain-source voltage of the device, $V_{DS\text{-}max}$, from the minimum converter input voltage $V_{IN\text{-}min}$:

$$V_{P\text{-}min} = V_{IN\text{-}min} - V_{DS\text{-}max} \tag{15}$$

$V_{DS\text{-}max}$ however, is the product of the maximum $R_{DS(on)}$ and I_D values for a given supply specified in the data sheet:

$$V_{DS\text{-}max} = R_{DS\text{-}max} \times I_{Dmax} \tag{16}$$

Then inserting 方程式 16 into 方程式 15 yields:

$$V_{P\text{-}min} = V_{IN\text{-}min} - R_{DS\text{-}max} \times I_{Dmax} \tag{17}$$

and inserting 方程式 17 and 方程式 14 into 方程式 13 provides the minimum turns ration with:

$$N_{min} = 1.03 \times \frac{V_{F-max} + V_{DO-max} + V_{O-max}}{V_{IN-min} - R_{DS-max} \times I_{D-max}} \tag{18}$$

Examples are given on the calculation method. One is for the fixed input case without duty cycle control. The other is for the wide-ranging input, with or without duty cycle control.

Example of Fixed Input:

For a fixed 24 V V_{IN} to 15 V_{OUT} converter using the rectifier diode PMEG200G20ELRX and the LM317A LDO, the data sheet values taken for a load current of 500mA and a maximum temperature of 85°C are $V_{F\text{-}max}$ = 0.5 V, $V_{DO\text{-}max}$ = 0.7 V, and $V_{O\text{-}max}$ = 15.15 V.

Then assuming that the converter input voltage is taken from a 24V regulated supply with a maximum ±2% accuracy makes $V_{IN\text{-}min}$ = 23.52 V. Finally the maximum values for drain-source resistance and drain current at 24 V are taken from the data sheet with $R_{DS\text{-}max}$ = 1 Ω and $I_{D\text{-}max}$ = 0.5 A.

Inserting the values above into the Equation above yields a minimum turns ratio of:

$$N_{min} = 1.03 \times \frac{0.5\,V + 0.7\,V + 15.1\,V}{23.52\,V - 1\,\Omega \times 0.5\,A} = 0.72 \tag{19}$$

Example of Wide-Ranging Input:

- **Wide-Ranging Input without Duty-Cycle Control**

For converter designs with wide-input range but no duty cycle control, the turns ratio needs to take the minimum input voltage into consideration.

Assuming the same diode and LDO are used, the calculation, so $V_{F\text{-max}}$ = 0.5 V, $V_{DO\text{-max}}$ = 0.7 V, and $V_{O\text{-max}}$ = 15.15 V.

The input range from 18 V up to 30 V makes $V_{IN\text{-min}}$ = 18 V. The input range from 18 V up to 30 V with 24 V typical makes $V_{IN\text{-min}}$ = 18 V. Substituting the same $R_{DS\text{-max}}$ = 1 Ω and $I_{D\text{-max}}$ = 0.5 A into the Equation above yields to a minimum turns ratio of:

$$N_{min} = 1.03 \times \frac{0.5\,V + 0.7\,V + 15.1\,V}{18\,V - 1\,\Omega \times 0.5\,A} = 0.96 \quad (20)$$

- **Wide-Ranging Input with Duty-Cycle Control**

For converter designs with wide-input range, the duty cycle feature is useful to compensate input variaton. But care must be taken to make sure that high turns ratios don’t lead to primary currents that exceed the specified current limits of the device.

$$N_{min} = 1.03 \times \frac{V_{F-max} + V_{DO-max} + V_{O-max}}{V_{IN-typ} - R_{DS-max} \times I_{D-max}} \times \frac{1}{2D_{typ}} \quad (21)$$

Assuming the same diode and LDO are used, so $V_{F\text{-max}}$ = 0.5 V, $V_{DO\text{-max}}$ = 0.7 V, and $V_{O\text{-max}}$ = 15.15 V.

It's recommends the use to set the DC=25% at typical $V_{IN\text{-typ}}$ = 24 V. Substituting the same $R_{DS\text{-max}}$ = 1 Ω and $I_{D\text{-max}}$ = 0.5 A into the Equation above yields to a minimum turns ratio of:

$$N_{min} = 1.03 \times \frac{0.5\,V + 0.7\,V + 15.1\,V}{24\,V - 1\,\Omega \times 0.5\,A} \times \frac{1}{2 \times 0.25} = 1.38 \quad (22)$$

9.2.2.6 Low-Emissions Designs

For isolated power supply designs requiring low levels of radiated and conducted emissions, the following recommendations can help minimize emissions from SN6507-Q1 and its surrounding components:

- Ensure a push-pull isolation transformer with low parasitics, like leakage inductance and parasitic capacitances, is used to minimize common-mode currents across the isolation barrier and antenna effects in the system.
- Use low-emissions rectifier diodes with low recovery times, like PMEG200G20ELRX or equivalent.
- Configure SN6507-Q1 for its slowest slew-rate setting to minimize high-frequency content in the switching paths.
- Include a snubber circuit on the secondary-side of the isolation transformer to filter high-frequency content in the switching paths.

Using these configurations may each affect system-level efficiency. The SN6507DGQEVM can be used to evaluate these design options.

9.2.3 Application Curves

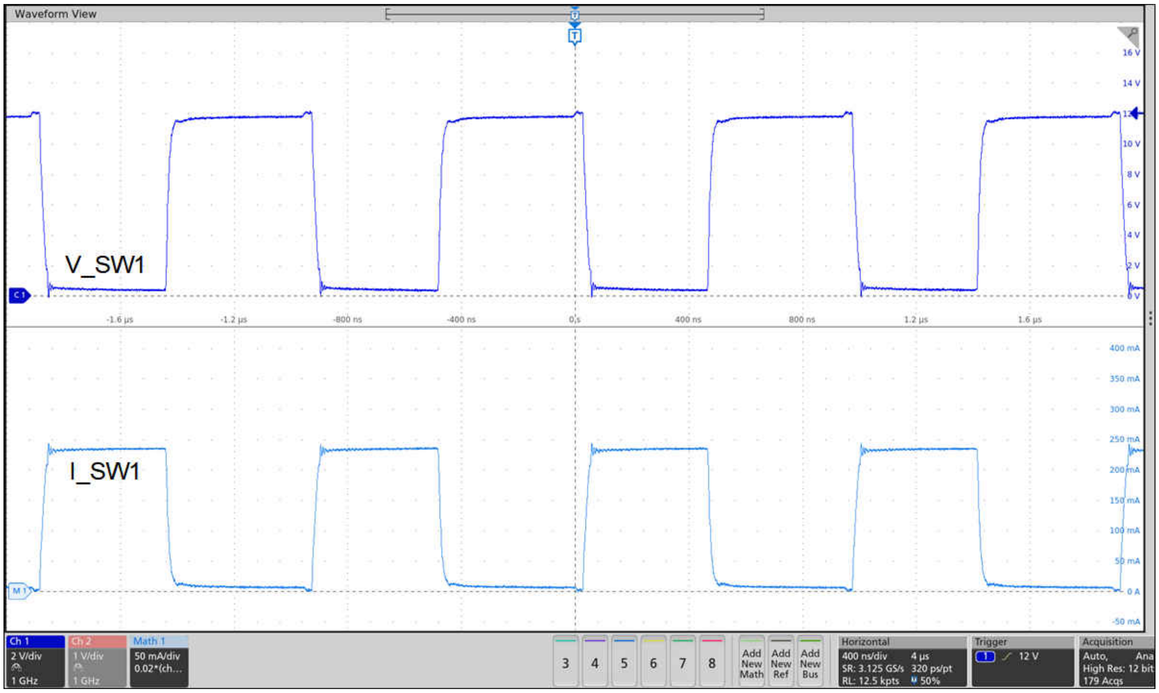


图 7-3 R_L = 50 Ω V_{IN} = 12 V

图 9-6. SN6507-Q1 SWx Voltage and Current Waveforms

9.2.4 System Examples

9.2.4.1 Higher Output Voltage Designs

The device can drive push-pull converters that provide doubling output voltages, or bipolar outputs with different rectifier topologies . 图 9-7 to 图 9-9 show some of these topologies together with their respective open-circuit output voltages.

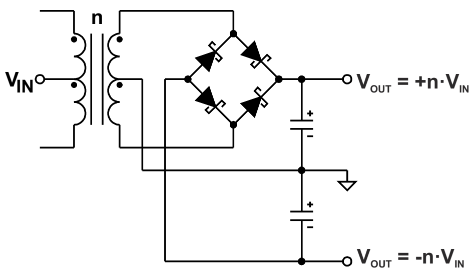


图 9-7. Bridge Rectifier With Center-Tapped Secondary Enables Bipolar Outputs

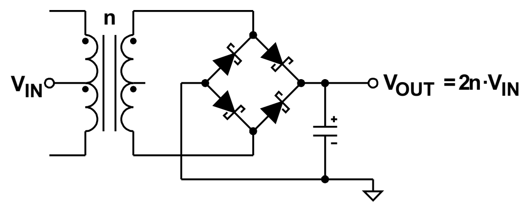


图 9-8. Bridge Rectifier Without Center-Tapped Secondary Performs Voltage Doubling

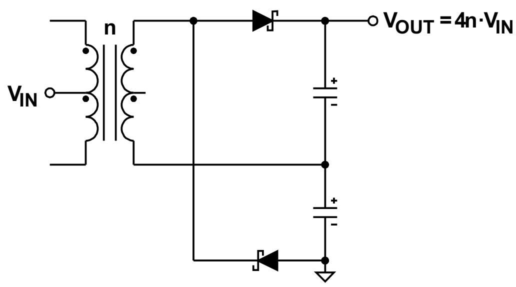


图 9-9. Half-Wave Rectifier Without Centered Ground and Center-Tapped Secondary Performs Voltage Doubling Twice, Hence Quadrupling V_{IN}

9.2.4.2 Commercially-Available Transformers

表 9-3 shows recommended transformer designs for SN6507-Q1 that are commercially available. Although SN6507-Q1 is compatible with many commercially-available and custom transformers, these part numbers or equivalents are optimized for use with SN6507-Q1. Transformer equivalents for automotive applications of the parts listed below may be available from their respective magnetics vendors under different part numbers.

表 9-3. Recommended Center Tapped Transformers for SN6507-Q1

APPLICATION	TURNS RATIO (1:N)	V-t product Min (V µ s)	ISOLATION (V_{RMS})	DIMENSION (mm) (L,W,H)	PART NUMBER 1
24 V→ 15 V	0.73	15	2.5 k	(8.5, 12.87, 5.16)	Wurth 750319696
	0.71	30	2.5 k	(10.3, 12.07, 5.97)	Coilcraft TX1-ZB1459-BE
	0.73	25	2.5 k	(11.8, 13.2, 11.1)	Bourns SM91207L-E
	0.75	25	3.75 k	(10.3, 13.2, 12.5)	Pulse PAG6356.086NLT
	0.75	41.2	2.5 k	(11, 13.5, 10.54)	Semitel EP7-817
12 V→ 15 V	1.4	22	2.5 k	(10.3, 12.07, 5.97)	Coilcraft TX1-ZB1445-CE
	1.4	22	2.5 k	(8.5, 12.87, 5.16)	Wurth 750319692
	1.2	15	2.5 k	(11.8, 13.2, 11.1)	Bourns SM91208L-E
	1.4	25.8	2.5 k	(11, 13.5, 10.54)	Semitel EP7-815

表 9-3. Recommended Center Tapped Transformers for SN6507-Q1 (continued)

APPLICATION	TURNS RATIO (1:N)	V-t product Min (V μ s)	ISOLATION (V_{RMS})	DIMENSION (mm) (L,W,H)	PART NUMBER [1]
24 V→ 30 V	1.4	30	2.5 k	(10.3, 12.07, 5.97)	Coilcraft TX1-ZC1891-AE
	1.4	30	2.5 k	(8.5, 12.87, 5.16)	Wurth 750319948
	1.43	36.1	2.5 k	(11, 13.5, 10.54)	Semitel EP7-818
12 V→ 30 V	2.6	22	2.5 k	(8.5, 12.87, 5.16)	Wurth 750319949
	2.8	22	2.5 k	(10.3, 12.07, 5.97)	Coilcraft TX1-ZC1892-AE
	2.8	25.8	2.5 k	(11, 13.5, 10.54)	Semitel EP7-816
24 V→ 24 V	1.09	15	2.5 k	(8.5, 12.87, 5.16)	Wurth 750319697
24 V→ 12 V	0.55	15	2.5 k	(8.5, 12.87, 5.16)	Wurth 750319695
	0.625	50	3.75 k	(10.3, 13.2, 12.5)	Pulse PAG6356.085NLT
24 V→ 5 V	0.27	15	2.5 k	(8.5, 12.87, 5.16)	Wurth 750319694
	0.25	50	3.75 k	(10.3, 13.2, 12.5)	Pulse PAG6356.082NLT
12 V→ 24 V	2.13	7.5	2.5 k	(8.5, 12.87, 5.16)	Wurth 750319693
12 V→ 12 V	1.13	7.5	2.5 k	(8.5, 12.87, 5.16)	Wurth 750319691
12 V→ 5 V	0.5	7.5	2.5 k	(8.5, 12.87, 5.16)	Wurth 750319690
24 V→ 3.3 V	0.125	50	3.75 k	(10.3, 13.2, 12.5)	Pulse PAG6356.081NLT

1. Not all recommended part numbers are validated by Texas Instruments. Refer to the latest transformer specifications to determine compatibility with SN6507-Q1.

9.3 Power Supply Recommendations

The device is designed to operate from an input voltage supply range between 3 V and 36 V nominal. If the input supply is located more than a few inches from the device, a 0.1 μF by-pass capacitor should be connected as close as possible to the device V_{CC} pin and a 10 μF capacitor should be connected close to the transformer center-tap pin.

9.4 Layout

9.4.1 Layout Guidelines

- The power supply input, V_{IN}, must be buffered to ground with a low-ESR ceramic bypass-capacitor. The recommended capacitor value can range from 1 μF to 10 μF, and is typically 10 μF. The capacitor must have a voltage rating greater than the V_{IN} voltage level and an X5R or X7R dielectric.
- The optimum placement of the V_{IN} capacitor is closest to the V_{IN} and GND pins at the board entrance to minimize the loop area formed by the bypass-capacitor connection, the V_{IN} terminal, and the GND pin. See 图 9-10 for a PCB layout example.
- To help ensure reliable operation, a 0.1-μF low-ESR ceramic bypass-capacitor is recommended at the device V_{CC} pin. The capacitor should be placed as close to the supply pins as possible in the PCB layout and on the same layer. The capacitor must have a voltage rating greater than the V_{IN} voltage level.
- The connections between the device SW1 and SW2 pins and the transformer primary endings and the connection of the device V_{CC} pin and the transformer center-tap must be as short as possible for minimum trace inductance.
- The connection of the device V_{CC} pin and the transformer center-tap must be buffered to ground with a low-ESR ceramic bypass-capacitor. The recommended capacitor value can range from 1 μF to 10 μF, and is typically 10 μF. The capacitor must have a voltage rating greater than the V_{IN} voltage level and an X5R or X7R dielectric.

- The device GND pins must be tied to the PCB ground plane using two vias to help minimize inductance.
- The ground connections of the capacitors and other connections to the ground plane should use two vias for minimum inductance.
- The rectifier diodes should be Schottky diodes with low forward voltage and low capacitance to maximize efficiency.
- The V_{OUT} pin must be buffered to ISO-Ground with a low-ESR ceramic bypass-capacitor. The typical capacitor value can range from 500 nF to 10 µF and should be less than 10 times the value of C_{SS} to ensure a smooth transition between soft-start and the steady state.

9.4.2 Layout Example

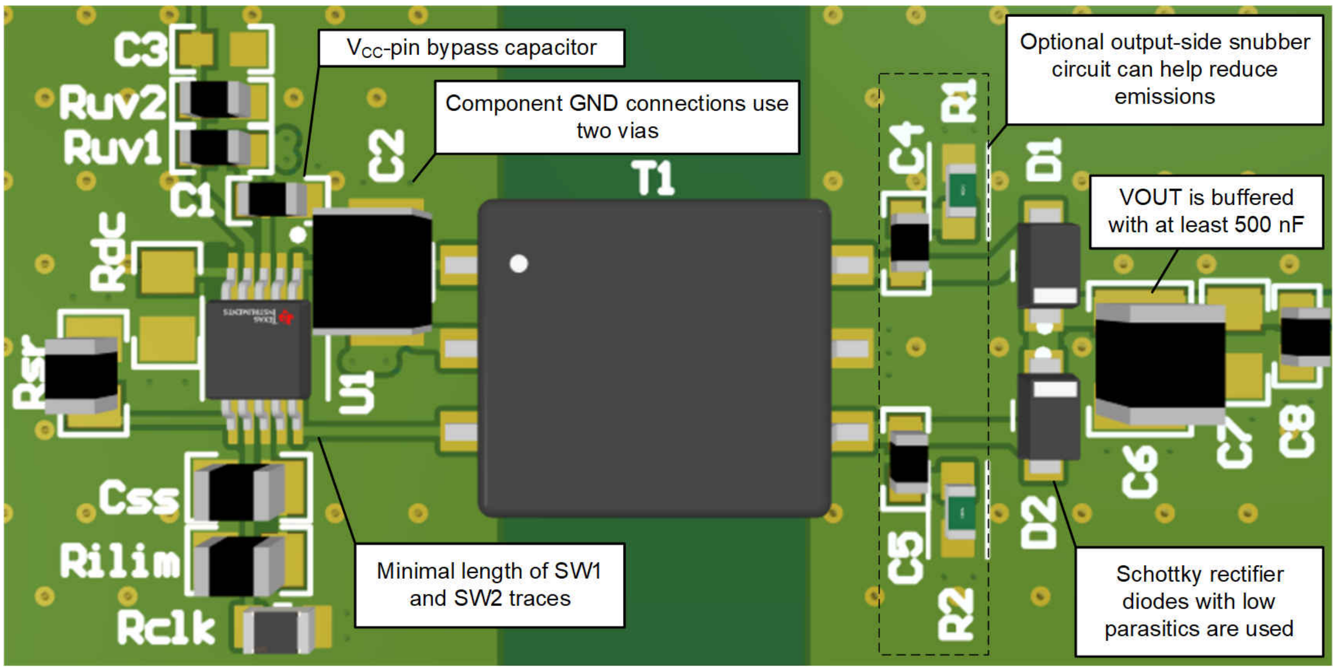


图 9-10. Layout Example of a 2-Layer Board

10 Device and Documentation Support

10.1 Documentation Support

10.1.1 Related Documentation

For related documentation see the following:

- Texas Instruments, *Digital Isolator Design Guide*
- Texas Instruments, *Isolation Glossary*
- Texas Instruments, *How to Isolate Signal and Power in Isolated CAN Systems* TI TechNote
- Texas Instruments, *How to Isolate Signal and Power for an RS-485 System* TI TechNote
- Texas Instruments, *How to Isolate Signal and Power for I^2C* TI TechNote
- Texas Instruments, *How to Reduce Emissions in Push-Pull Isolated Power Supplies* TI Application Note
- Texas Instruments, *Small Form-Factor Reinforced Isolated IGBT Gate Drive Reference Design for 3-Phase Inverter* TI Design
- Texas Instruments, *SN6507DGQEVM Low-Emissions 500 mA Push-Pull Transformer Driver for Isolated Power Supplies Evaluation Module* TI EVM User's Guide

10.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

10.3 Community Resources

10.4 Trademarks

WEBENCH® is a registered trademark of Texas Instruments.
所有商标均为其各自所有者的财产。

11 Mechanical, Packaging, and Orderable Information

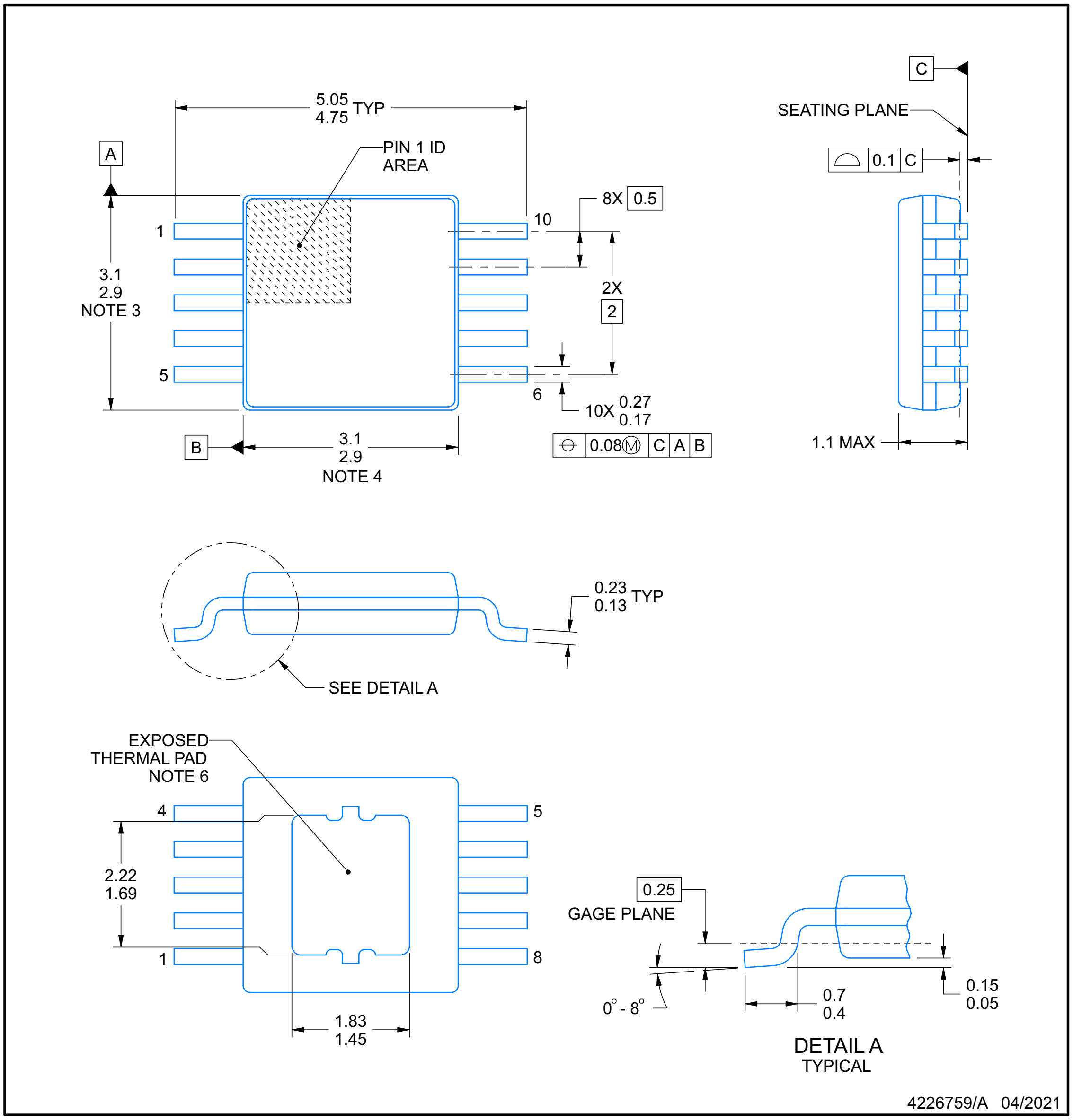
The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGE OUTLINE

DGQ0010D-C01

PowerPAD™ - 1.1 mm max height

PLASTIC SMALL OUTLINE



PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187, variation BA-T.
6. The thermal pad design could vary depending on manufacturing site.

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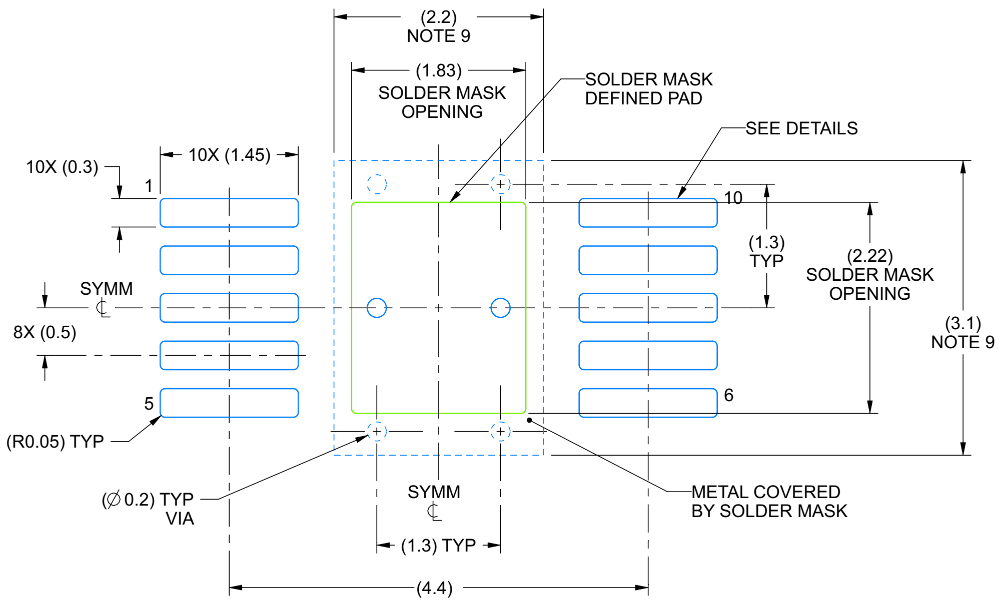
EXAMPLE BOARD LAYOUT

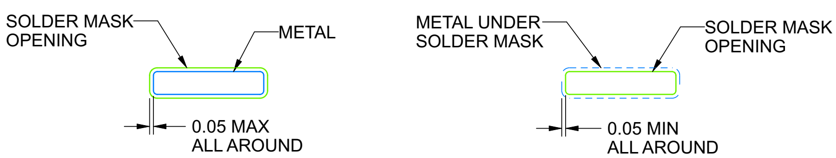
DGQ0010D-C01

PowerPAD ™ - 1.1 mm max height

PLASTIC SMALL OUTLINE



LAND PATTERN EXAMPLE
SCALE:15X



NON SOLDER MASK
DEFINED

SOLDER MASK
DEFINED

SOLDER MASK DETAILS

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NOTES: (continued)

7. Publication IPC-7351 may have alternate designs.
8. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
9. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
10. Size of metal pad may vary due to creepage requirement.

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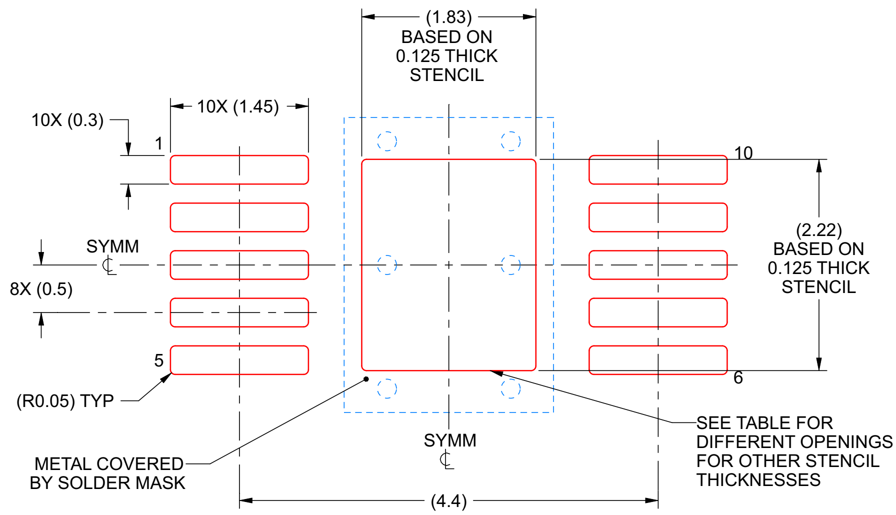
EXAMPLE STENCIL DESIGN

DGQ0010D-C01

PowerPAD ™ - 1.1 mm max height

PLASTIC SMALL OUTLINE



SOLDER PASTE EXAMPLE
EXPOSED PAD
100% PRINTED SOLDER COVERAGE BY AREA
SCALE:15X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	2.05 X 2.48
0.125	1.83 X 2.22 (SHOWN)
0.150	1.67 X 2.03
0.175	1.55 X 1.88

4226759/A 04/2021

NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN6507DGQRQ1	ACTIVE	HVSSOP	DGQ	10	2500	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-55 to 125	6507	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF SN6507-Q1 :

- Catalog : SN6507

NOTE: Qualified Version Definitions:

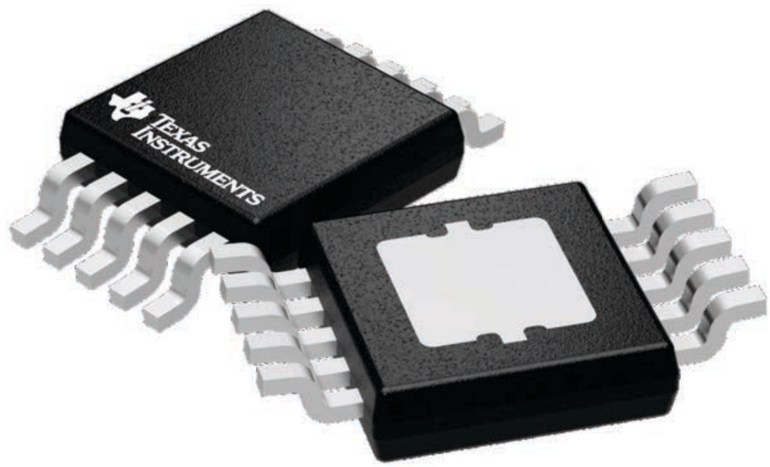
- Catalog - TI's standard catalog product

DGQ 10

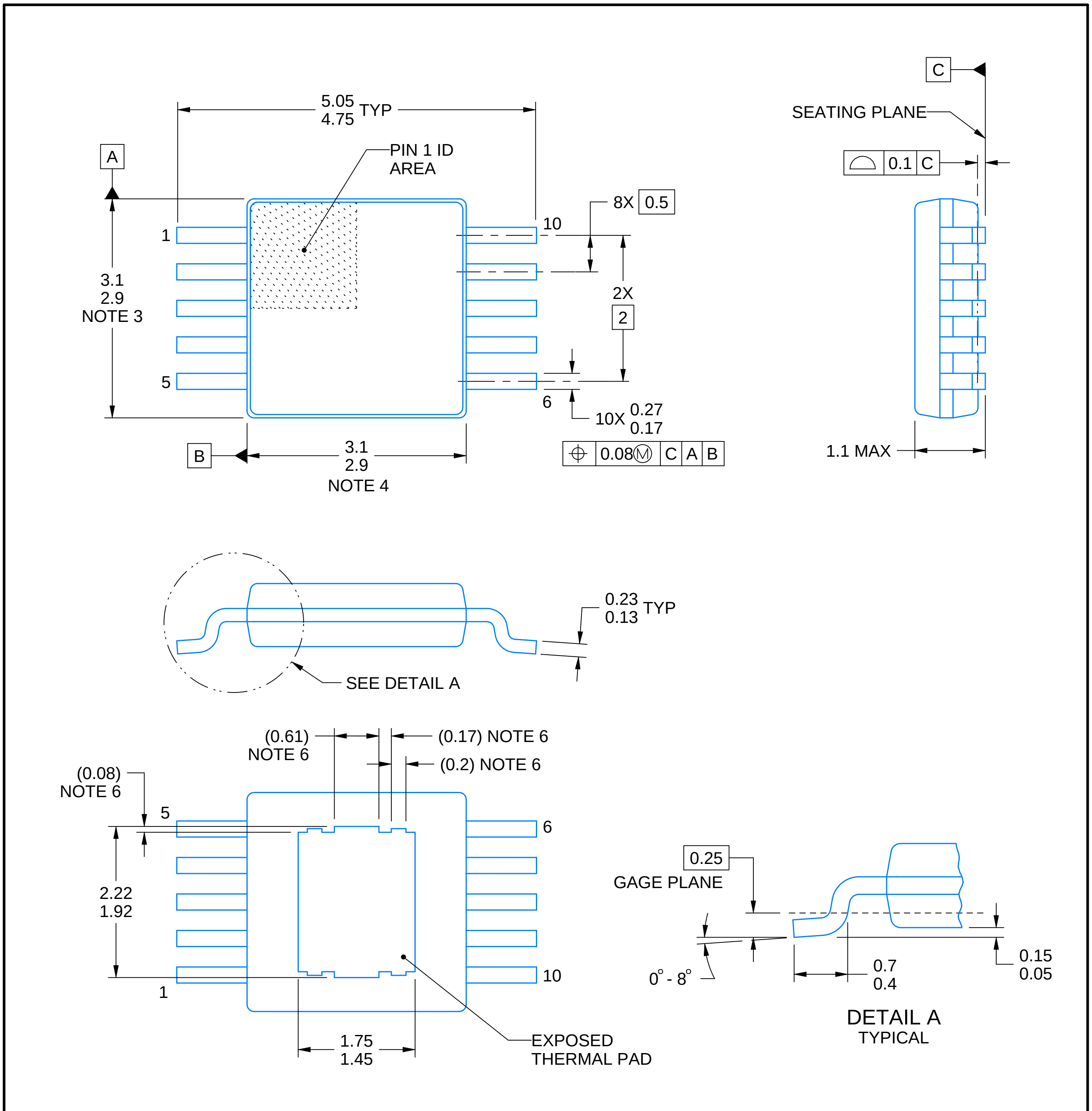
PowerPAD™ HVSSOP - 1.1 mm max height

3 x 3, 0.5 mm pitch

PLASTIC SMALL OUTLINE



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



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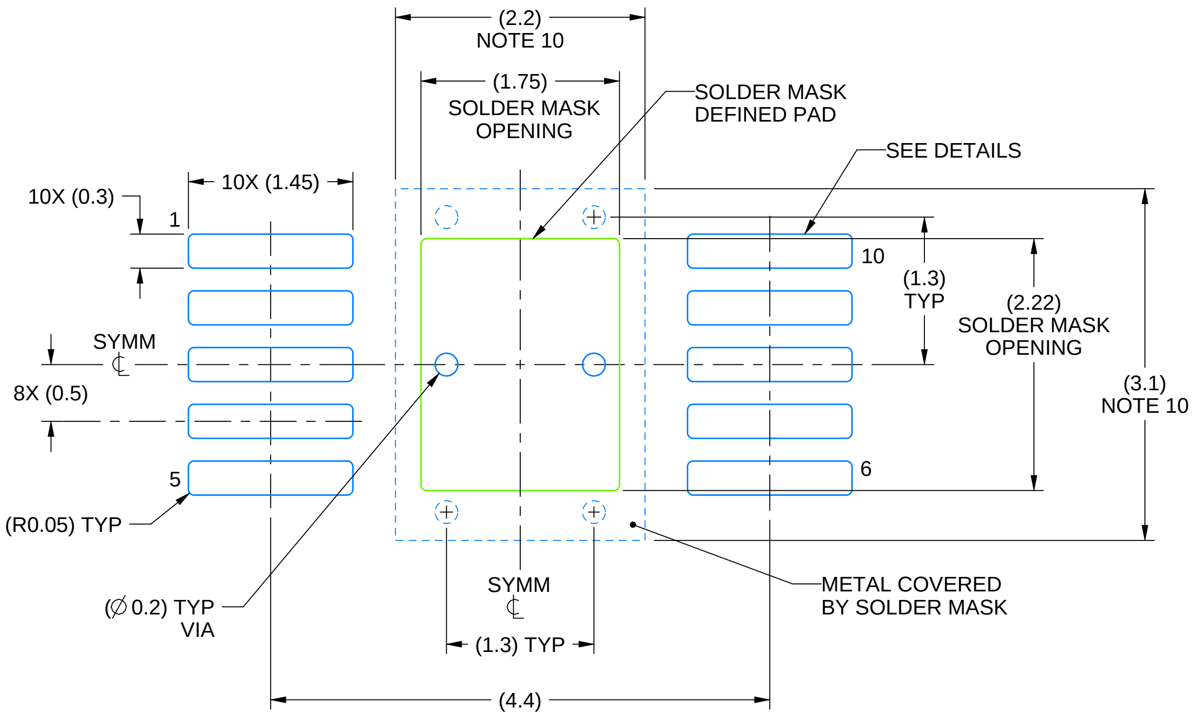
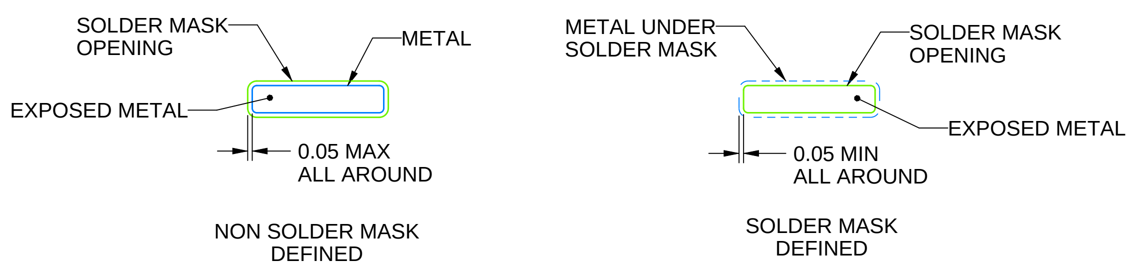
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187, variation BA-T.
6. Features may differ or may not be present.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



SOLDER MASK DETAILS

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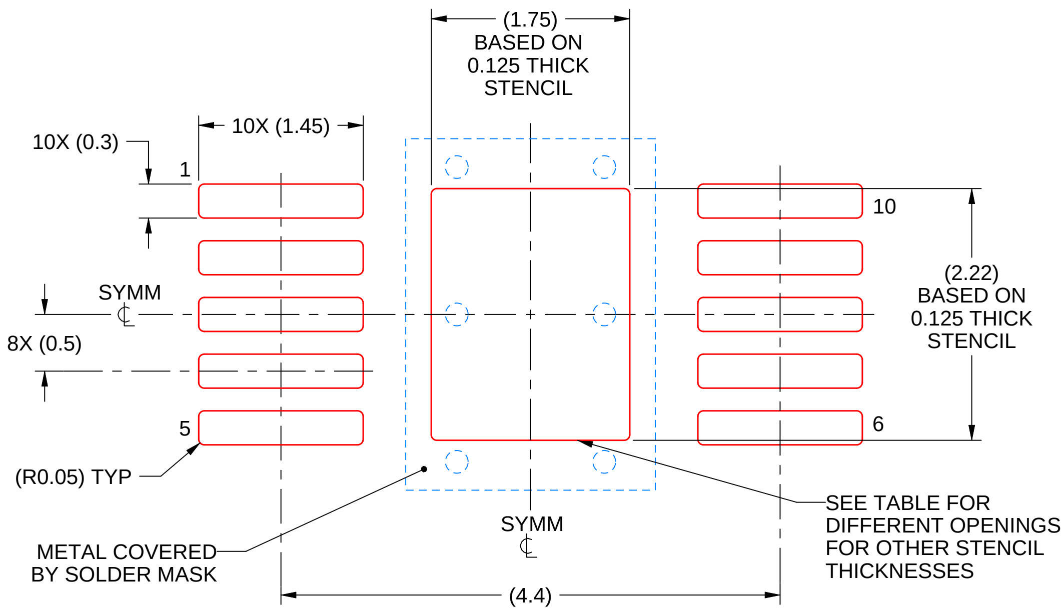
NOTES: (continued)

7. Publication IPC-7351 may have alternate designs.
8. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
9. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
10. Size of metal pad may vary due to creepage requirement.



SOLDER PASTE EXAMPLE
EXPOSED PAD
100% PRINTED SOLDER COVERAGE BY AREA
SCALE:15X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.100	1.96 X 2.48
0.125	1.75 X 2.22 (SHOWN)
0.150	1.6 X 2.03
0.175	1.48 X 1.88

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NOTES: (continued)

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