SN65HVD485E 半双工 RS-485 收发器

1 特性

- 高达 15kV 的总线引脚 ESD 保护
- 1/2 单位负载：一条总线上多达 64 个节点
- 总线开路失效防护接收器
- 无干扰上电和下电总线输入和输出
- 采用小型 VSSOP-8 封装
- 符合或超出 TIA/EIA-485A 标准要求
- 业界通用通用 SN75176 封装

2 应用

- 电机控制
- 电源逆变器
- 工业自动化
- 楼宇自动化网络
- 工业过程控制
- 电池供电型应用
- 电信设备

3 说明

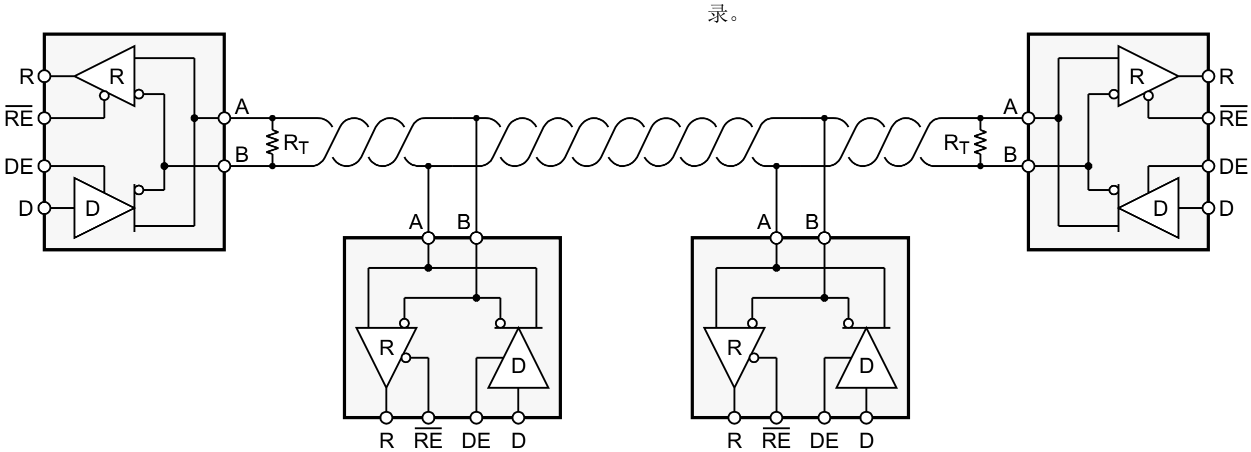
SN65HVD485E 器件是专为 RS-485 数据总线网络设计的半双工收发器。该器件由 5V 电源供电，完全符合 TIA/EIA-485A 标准。该器件适用于通过长双绞线电缆以高达 10Mbps 的速率传输数据，并且设计用于在非常低的电源电流（通常小于 2mA，不包括负载）下运行。当器件处于非活动关断模式时，电源电流降至 1mA 以下。

该器件的宽共模范围和高 ESD 保护级别使其适用于要求苛刻的应用，例如电气逆变器、电信机架上的状态/命令信号、有线机箱互连以及噪声容限至关重要的工业自动化网络。SN65HVD485E 器件符合 SN75176 器件的业界通用尺寸。上电复位电路使输出保持高阻抗状态，直到电源电压稳定。热关断功能可保护器件免受系统故障问题造成的损坏。SN65HVD485E 器件可在 –40°C 至 85°C 气温下运行。

封装信息

器件型号	封装(1)	封装尺寸（标称值）
SN65HVD485E	SOIC (8)	4.91mm × 3.90mm
	VSSOP (8)	3.00mm × 3.00mm
	PDIP (8)	9.81mm × 6.35mm

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。



典型应用原理图

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4 Revision History

注：以前版本的页码可能与当前版本的页码不同

Changes from Revision E (November 2015) to Revision F (February 2023) **Page**

- Changed the values in the *Thermal Information* table 5

Changes from Revision D (July 2015) to Revision E (November 2015) **Page**

- Changed 3.3 V To: 5 V at pin V_{CC} in 图 9-4 17

Changes from Revision C (March 2007) to Revision D (July 2015) **Page**

- 添加了 *引脚配置和功能* 部分、*特性说明* 部分、*器件功能模式*、*应用和实施* 部分、*电源相关建议* 部分、*布局* 部分、*器件和文档支持* 部分以及 *机械、封装和可订购信息* 部分 1
- 删除了 *订购信息* 表 1
- Changed *Thermal Information* table 5
- Added *Power Dissipation Characteristics* table 6

5 Device Comparison Table

Improved Replacement for Devices

PART NUMBER	REPLACE WITH	BENEFITS
ADM485	SN65HVD485E	Better ESD protection (±15 kV versus unspecified) Faster signaling rate (10 Mbps versus 5 Mbps) More nodes on a bus (64 versus 32) Wider power supply tolerance (10% vs 5%)
SP485E	SN65HVD485E	More nodes on a bus (64 versus 32) Wider power supply tolerance (10% versus 5%)
LMS485E	SN65HVD485E	Higher signaling rate (10 Mbps versus 2.5 Mbps) More nodes on a bus (64 versus 32) Wider power supply tolerance (10% versus 5%)
DS485	SN65HVD485E	Higher signaling rate (10 Mbps versus 2.5 Mbps) Better ESD (±15 kV versus ±2 kV) More nodes on a bus (64 versus 32) Wider power supply tolerance (10% versus 5%)
LTC485	SN65HVD485E	Better ESD (±15 kV versus ±2 kV) Wider power supply tolerance (10% versus 5%)
MAX485E	SN65HVD485E	Higher signaling rate (10 Mbps versus 2.5 Mbps) More nodes on a bus (64 versus 32) Wider power supply tolerance (10% versus 5%)
ST485E	SN65HVD485E	Higher signaling rate (10 Mbps versus 5 Mbps) Wider power supply tolerance (10% versus 5%)
ISL8485E	SN65HVD485E	More nodes on a bus (64 versus 32) Faster signaling rate (10 Mbps versus 5 Mbps)

6 Pin Configuration and Functions

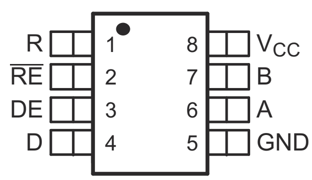


图 6-1. D, DGK, P Packages, 8-Pin SOIC, VSSOP, PDIP (Top View)

表 6-1. Pin Functions

PIN		TYPE	DESCRIPTION
NAME	NO.		
A	6	Bus input/output	Driver output or receiver input (complementary to B)
B	7	Bus input/output	Driver output or receiver input (complementary to A)
D	4	Digital input	Driver data input
DE	3	Digital input	Driver enable, active high
GND	5	Reference potential	Local device ground
R	1	Digital input	Receive data output
$\overline{RE}$	2	Digital input	Receiver enable, active low
V_{CC}	8	Supply	4.5-V to 5.5-V supply

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) [(1)] [(2)]

		MIN	MAX	UNIT
V_{CC}	Supply voltage	–0.5	7	V
	Voltage range at A or B	–9	14	V
	Voltage range at any logic pin	–0.3	V_{CC} + 0.3	V
	Receiver output current	–24	24	mA
	Voltage input range, transient pulse, A and B, through 100 Ω (see 图 8-13)	–50	50	V
T_J	Junction temperature	170	170	°C
	Continuous total power dissipation	Refer to 节 7.11		
T_{stg}	Storage temperature	–65	130	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under 节 7.3 is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values, except differential I/O bus voltages, are with respect to network ground terminal.

7.2 ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001[(1)]	Bus pins and GND	±15000	V
			All pins	±4000	
		Charged-device model (CDM), per JEDEC specification JESD22-C101[(2)]		±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)[(1)]

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		4.5		5.5	V
V_I	Input voltage at any bus terminal (separately or common mode)		–7		12	V
V_{IH}	High-level input voltage (D, DE, or RE inputs)		2		V_{CC}	V
V_{IL}	Low-level input voltage (D, DE, or RE inputs)		0		0.8	V
V_{ID}	Differential input voltage		–12		12	V
I_O	Output current	Driver	–60		60	mA
		Receiver	–8		8	
R_L	Differential load resistance		54	60		Ω
$1/t_{UI}$	Signaling rate		0		10	Mbps
T_A	Operating free-air temperature		–40		85	°C
T_J	Junction temperature[(2)]		–40		130	°C

(1) The algebraic convention, in which the least positive (most negative) limit is designated as minimum, is used in this data sheet.
(2) See 节 7.4 for information on maintenance of this specification for the DGK package.

7.4 Thermal Information

THERMAL METRIC[1]		SN65HVD485E			UNIT
		D (SOIC)	DGK (VSSOP)	P (PDIP)	
		8 PINS	8 PINS	8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance[2]	116.7	137.8	84.3	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	56.3	31.2	65.4	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	63.4	71.7	62.1	°C/W
ψ_{JT}	Junction-to-top characterization parameter	8.8	0.6	31.3	°C/W
ψ_{JB}	Junction-to-board characterization parameter	62.6	70.5	60.4	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report (SPRA953).
(2) See the *Package Thermal Characterization Methodologies* application note (SZZA003) for an explanation of this parameter.

7.5 Electrical Characteristics: Driver

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP[1]	MAX	UNIT
$\lvert V_{OD} \rvert$	Differential output voltage	I_O = 0, No load	3	4.3		V
		R_L = 54 W (see 图 8-1)	1.5	2.3		
		V_{TEST} = –7 V to 12 V (see 图 8-2)	1.5			
$\Delta\lvert V_{OD} \rvert$	Change in magnitude of differential output voltage	See 图 8-1 and 图 8-2	–0.2	0	0.2	V
$V_{OC(SS)}$	Steady-state common-mode output voltage	See 图 8-3	1	2.6	3	V
$\Delta V_{OC(SS)}$	Change in steady-state common-mode output voltage		–0.1	0	0.1	V
$V_{OC(PP)}$	Common-mode output voltage	See 图 8-3		500		mV
I_{OZ}	High-impedance output current	See receiver input currents				µA
I_I	Input current	D, DE	–100		100	µA
I_{OS}	Short-circuit output current	–7 V ≤ V_O ≤ 12 V (see 图 8-7)	–250		250	mA

(1) All typical values are at 25°C and with a 5-V supply.

7.6 Electrical Characteristics: Receiver

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP[(1)]	MAX	UNIT
V_{IT+}	Positive-going input threshold voltage	I_O = –8 mA		–85	–10	mV
V_{IT-}	Negative-going input threshold voltage	I_O = 8 mA	–200	–115		mV
V_{hys}	Hysteresis voltage (V_{IT+} – V_{IT-})			30		mV
V_{OH}	High-level output voltage	V_{ID} = 200 mV, I_{OH} = –8 mA (see 图 8-8)	4	4.6		V
V_{OL}	Low-level output voltage	V_{ID} = –200 mV, I_{OH} = 8 mA (see 图 8-8)		0.15	0.4	V
I_{OZ}	High-impedance-state output current	V_O = 0 to V_{CC}, $\overline{RE}$ = V_{CC}	–1		1	μA
I_I	Bus input current	V_{IH} = 12 V, V_{CC} = 5 V			0.5	mA
		V_{IH} = 12 V, V_{CC} = 0			0.5	
		V_{IH} = –7 V, V_{CC} = 5 V	–0.4			
		V_{IH} = –7 V, V_{CC} = 0	–0.4			
I_{IH}	High-level input current ($\overline{RE}$)	V_{IH} = 2 V	–60	–30		μA
I_{IL}	Low-level input current ($\overline{RE}$)	V_{IL} = 0.8 V	–60	–30		μA
C_{diff}	Differential input capacitance	V_I = 0.4 sin (4E6 π t) + 0.5 V, DE at 0 V		7		pF

(1) All typical values are at 25°C and with a 5-V supply.

7.7 Power Dissipation Characteristics

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$P_{(AVG)}$	Average power dissipation	R_L = 54 Ω, Input to D is a 10 Mbps 50% duty cycle square wave V_{CC} at 5.5 V, T_J = 130°C			219	mW
T_{SD}	Thermal shut-down junction temperature			165		°C

7.8 Supply Current

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP(1)	MAX	UNIT
I_{CC}	Driver and receiver enabled	D at V_{CC} or open or 0 V,	DE at V_{CC}, RE at 0 V, No load			2	mA
	Driver and receiver disabled	D at V_{CC} or open,	DE at 0 V, RE at V_{CC}			1	mA

(1) All typical values are at 25°C and with a 5-V supply.

7.9 Switching Characteristics: Driver

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	R_L = 54 Ω, C_L = 50 pF (see 图 8-4)			30	ns
t_{PHL}	Propagation delay time, high-to-low-level output				30	ns
t_r	Differential output signal rise time				25	ns
t_f	Differential output signal fall time				25	ns
$t_{sk(p)}$	Pulse skew ($\|t_{PHL} - t_{PLH}\|$)				5	ns
t_{PZH}	Propagation delay time, high-impedance-to-high-level output	R_L = 110 Ω, $\overline{RE}$ at 0 V (see 图 8-5)			150	ns
t_{PHZ}	Propagation delay time, high-level-to-high-impedance output				100	ns
t_{PZL}	Propagation delay time, high-impedance-to-low-level output	R_L = 110 Ω, $\overline{RE}$ at 0 V (see 图 8-6)			150	ns
t_{PLZ}	Propagation delay time, low-level-to-high-impedance output				100	ns
$t_{PZH(SHN)}$	Propagation delay time, shutdown-to-high-level output	R_L = 110 Ω, $\overline{RE}$ at VCC (see 图 8-5)			2600	ns
$t_{PZL(SHDN)}$	Propagation delay time, shutdown-to-low-level output	R_L = 110 Ω, $\overline{RE}$ at VCC (see 图 8-6)			2600	ns

7.10 Switching Characteristics: Receiver

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	V_{ID} = -1.5 V to 1.5 V, C_L = 15 pF (see 图 8-9)			200	ns
t_{PHL}	Propagation delay time, high-to-low-level output				200	ns
$t_{sk(p)}$	Pulse skew ($\|t_{PHL} - t_{PLH}\|$)			6		ns
t_r	Output signal rise time				3	ns
t_f	Output signal fall time				3	ns
t_{PZH}	Output enable time to high level	C_L = 15 pF, DE at 3 V, (see 图 8-10 and 图 8-11)			50	ns
t_{PZL}	Output enable time to low level				50	ns
t_{PHZ}	Output enable time from high level				50	ns
t_{PLZ}	Output enable time from low level				50	ns
$t_{PZH(SHDN)}$	Propagation delay time, shutdown-to-high-level output	C_L = 15 pF, DE at 0 V, (see 图 8-12)			3500	ns
$t_{PZL(SHDN)}$	Propagation delay time, shutdown-to-low-level output				3500	ns

7.11 Dissipation Ratings

PACKAGE[1]	JEDEC BOARD MODEL	T_A < 25°C POWER RATING	DERATING FACTOR[2] ABOVE T_A = 25°C	T_A = 70°C POWER RATING	T_A = 85°C POWER RATING
D (SIOC)	Low k[3]	507 mW	4.82 mW/°C	289 mW	217 mW
	High k[3]	824 mW	7.85 mW/°C	471 mW	353 mW
P (PDIP)	Low k[3]	686 mW	6.53 mW/°C	392 mW	294 mW
DGK (VSSOP)	Low k[3]	394 mW	3.76 mW/°C	255 mW	169 mW
	High k[4]	583 mW	5.55 mW/°C	333 mW	250 mW

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.
(2) This is the inverse of the junction-to-ambient thermal resistance when board-mounted and with no air flow.
(3) In accordance with the low-k thermal metric definitions of EIA/JESD51-3.
(4) In accordance with the high-k thermal metric definitions of EIA/JESDS1-7.

7.12 Typical Characteristics

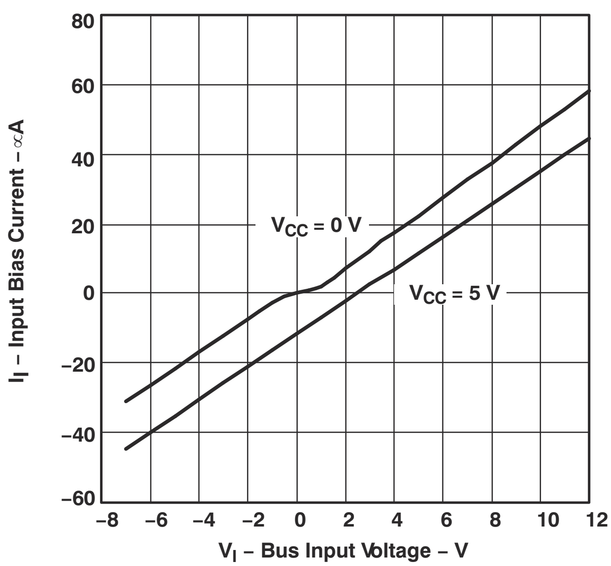


图 7-1. Bus Input Current vs Bus Input Voltage

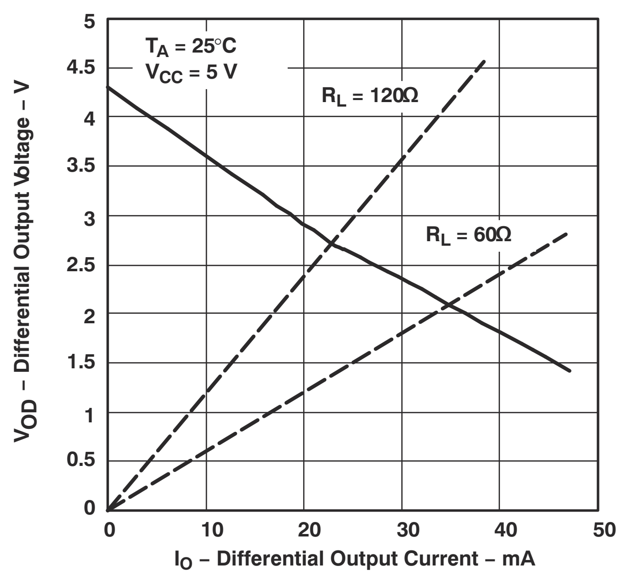


图 7-2. Driver Differential Output Voltage vs Differential Output Current

Parameter Measurement Information

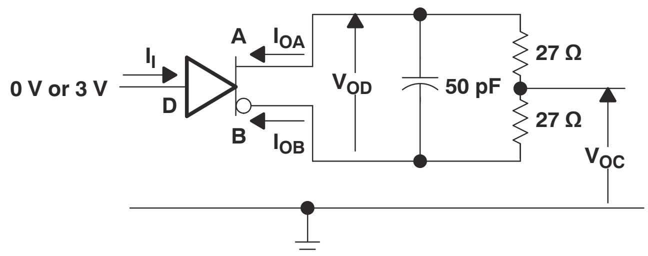


图 8-1. Driver Test Circuit, V_{OD} and V_{OC} Without Common-Mode Loading

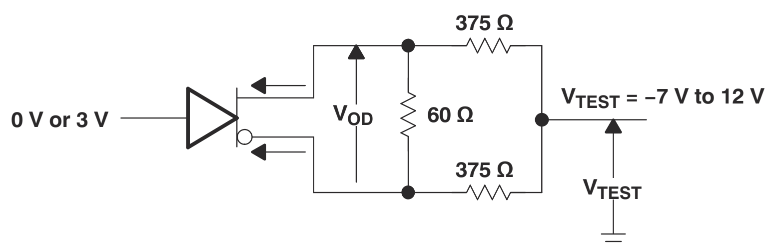


图 8-2. Driver Test Circuit, V_{OD} With Common-Mode Loading

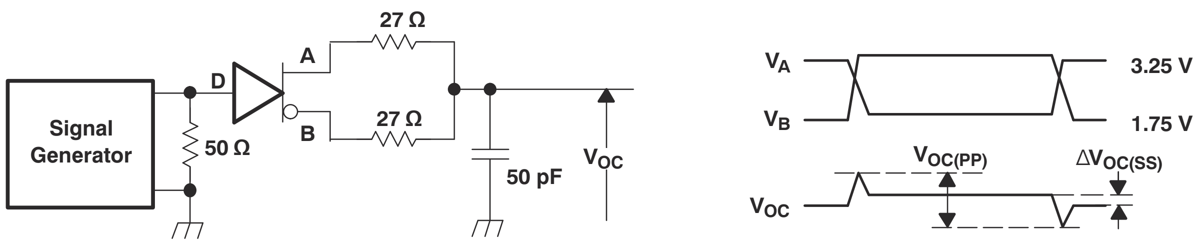


图 8-3. Driver V_{OC} Test Circuit and Waveforms

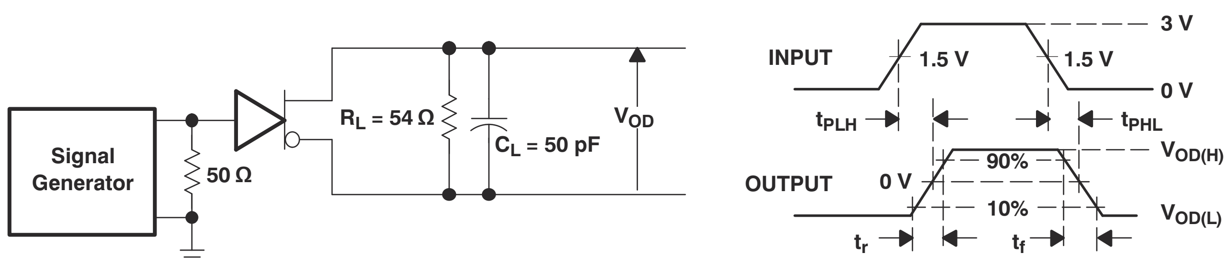


图 8-4. Driver Switching Test Circuit and Waveforms

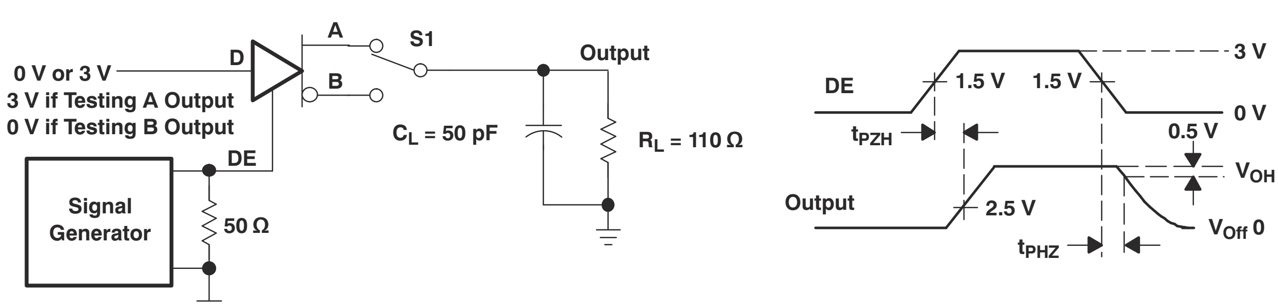


图 8-5. Driver Enable/Disable Test Circuit and Waveforms, High Output

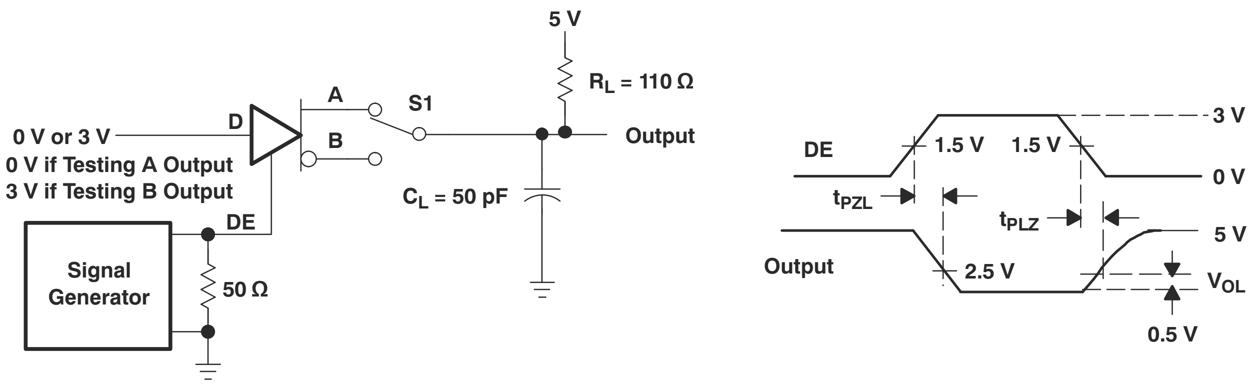


图 8-6. Driver Enable/Disable Test Circuit and Waveforms, Low Output

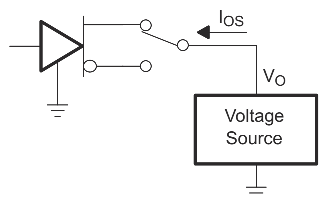


图 8-7. Driver Short-Circuit Test

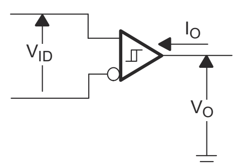


图 8-8. Receiver Parameter Definitions

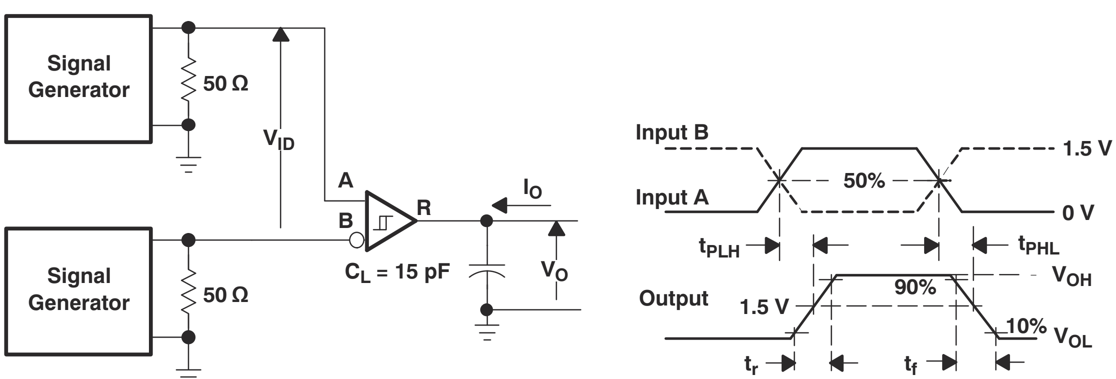


图 8-9. Receiver Switching Test Circuit and Waveforms

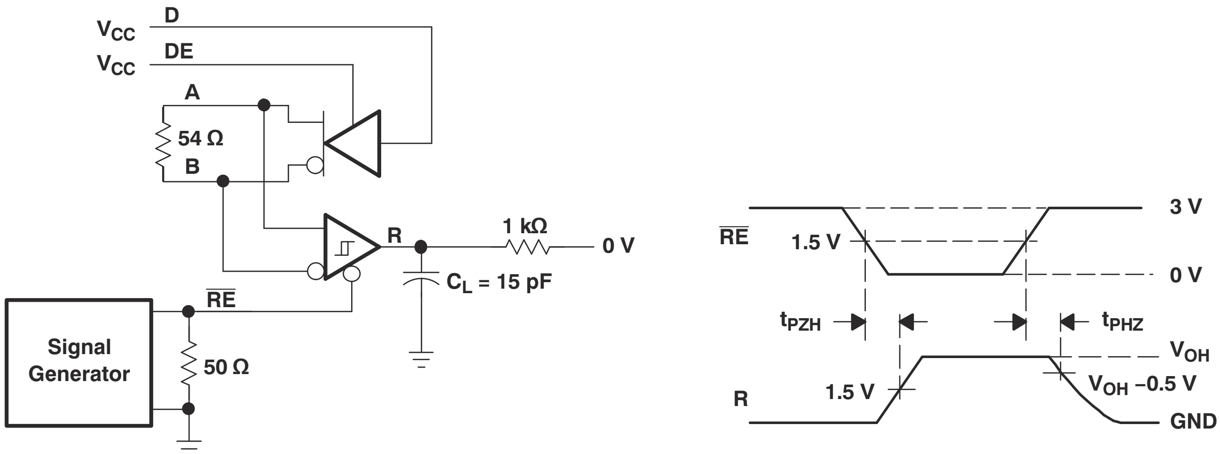


图 8-10. Receiver Enable/Disable Test Circuit and Waveforms, Data Output High

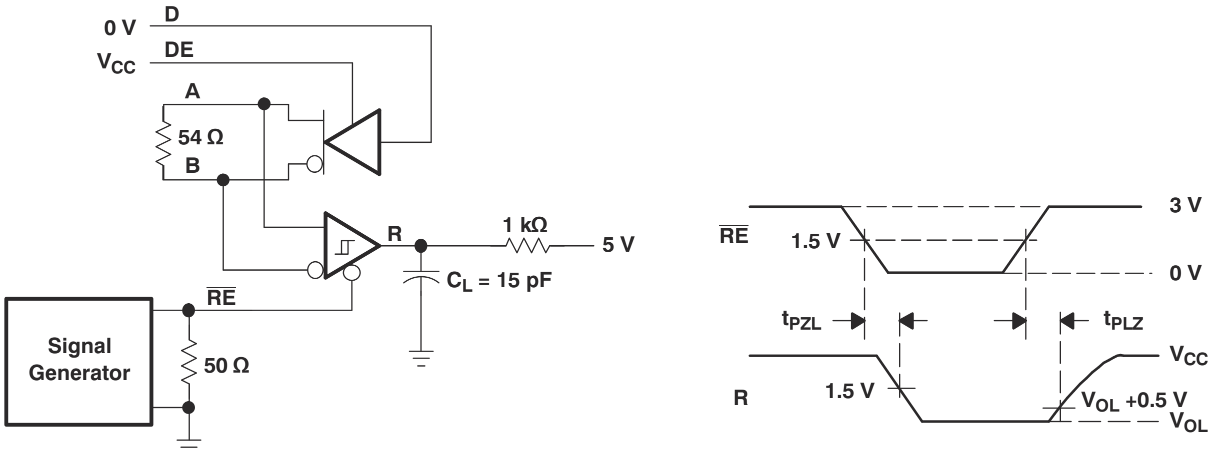


图 8-11. Receiver Enable/Disable Test Circuit and Waveforms, Data Output Low

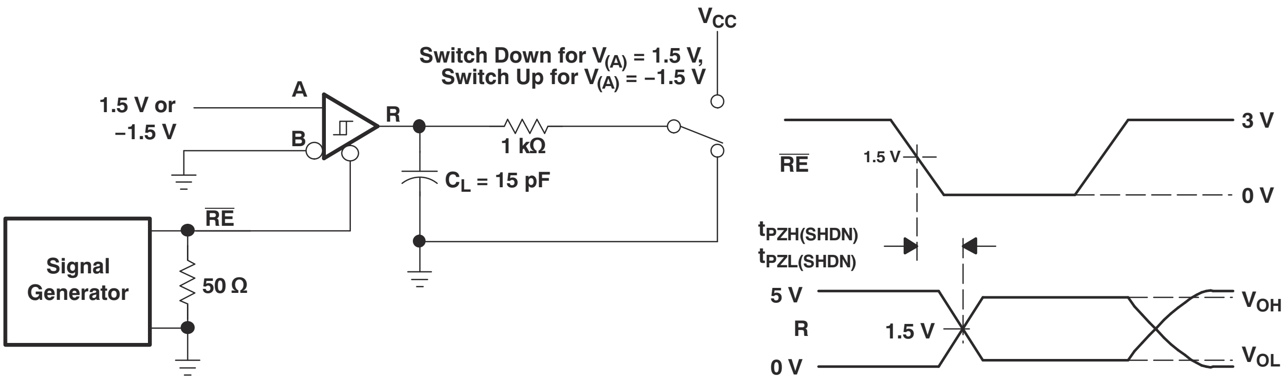


图 8-12. Receiver Enable From Shutdown Test Circuit and Waveforms

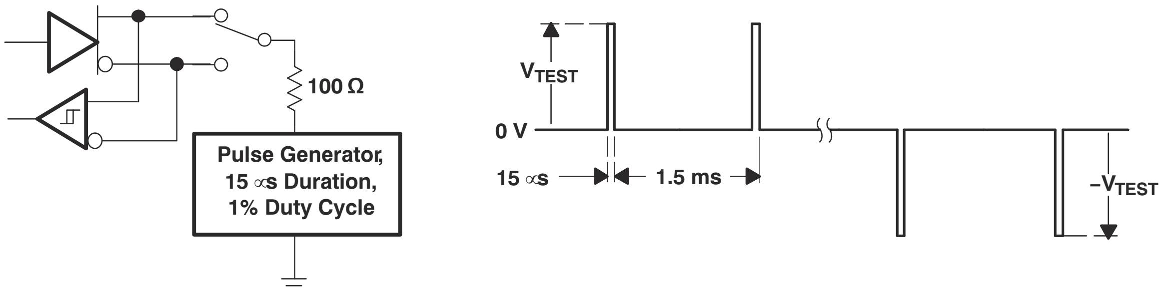


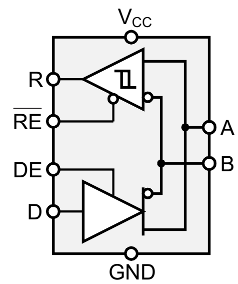
图 8-13. Test Circuit and Waveforms, Transient Over-Voltage Test

8 Detailed Description

8.1 Overview

The SN65HVD485E device is a half-duplex RS-485 transceiver suitable for data transmission at rates up to 10 Mbps over controlled-impedance transmission media (such as twisted-pair cabling). Up to 64 units of the SN65HVD485E device can share a common RS-485 bus due to the low bus-input currents of the device. The device also features a high degree of ESD protection and low standby current consumption of 1 mA (maximum).

8.2 Functional Block Diagram



8.3 Feature Description

The SN65HVD485E device provides internal biasing of the receiver input thresholds for open-circuit, bus-idle, or short-circuit failsafe conditions. It features a typical hysteresis of 30 mV to improve noise immunity. Internal ESD protection circuits protect the transceiver bus terminals against ±15-kV Human Body Model (HBM) electrostatic discharges.

8.4 Device Functional Modes

When the driver enable pin (DE) is logic high, the differential outputs A and B follow the logic states at data input D. A logic high at D causes A to turn high and B to turn low. In this case, the differential output voltage defined as $V_{OD} = V_A - V_B$ is positive. When D is low, the output states reverse, B turns high, A is low, and V_{OD} is negative.

When DE is low, both outputs turn high impedance. In this condition, the logic state at D is irrelevant. The DE pin has an internal pulldown resistor to ground; thus when left open, the driver is disabled (high impedance) by default. The D pin has an internal pullup resistor to VCC; thus when left open while the driver is enabled, output A turns high and B turns low.

表 8-1. Driver Function Table

INPUT D	ENABLE DE	OUTPUTS		FUNCTION
		A	B	
H	H	H	L	Actively drive bus High
L	H	L	H	Actively drive bus Low
X	L	Z	Z	Driver disabled
X	OPEN	Z	Z	Driver disabled by default
OPEN	H	H	L	Actively drive bus high by default

When the receiver enable pin ($\overline{RE}$) is logic low, the receiver is enabled. When the differential input voltage defined as $V_{ID} = V_A - V_B$ is positive and higher than the positive input threshold (V_{IT+}) the receiver output (R) turns high. When V_{ID} is negative and lower than the negative input threshold (V_{IT-}), the receiver output (R) turns low. If V_{ID} is between V_{IT+} and V_{IT-}, the output is indeterminate.

When $\overline{RE}$ is logic high or left open, the receiver output is high impedance and the magnitude and polarity of V_{ID} are irrelevant. Internal biasing of the receiver inputs causes the output to go failsafe high when the transceiver is disconnected from the bus (open-circuit), the bus lines are shorted (short-circuit), or the bus is not actively driven (idle bus).

表 8-2. Receiver Function Table

DIFFERENTIAL INPUT $V_{ID} = V_A - V_B$	ENABLE $\overline{RE}$	OUTPUT R	FUNCTION
$V_{IT+} < V_{ID}$	L	H	Receive valid bus High
$V_{IT-} < V_{ID} < V_{IT+}$	L	?	Indeterminate bus state
$V_{ID} < V_{IT-}$	L	L	Receive valid bus Low
X	H	Z	Receiver disabled
X	OPEN	Z	Receiver disabled by default
Open-circuit bus	L	H	Fail-safe high output
Short-circuit bus	L	H	Fail-safe high output
Idle (terminated) bus	L	H	Fail-safe high output

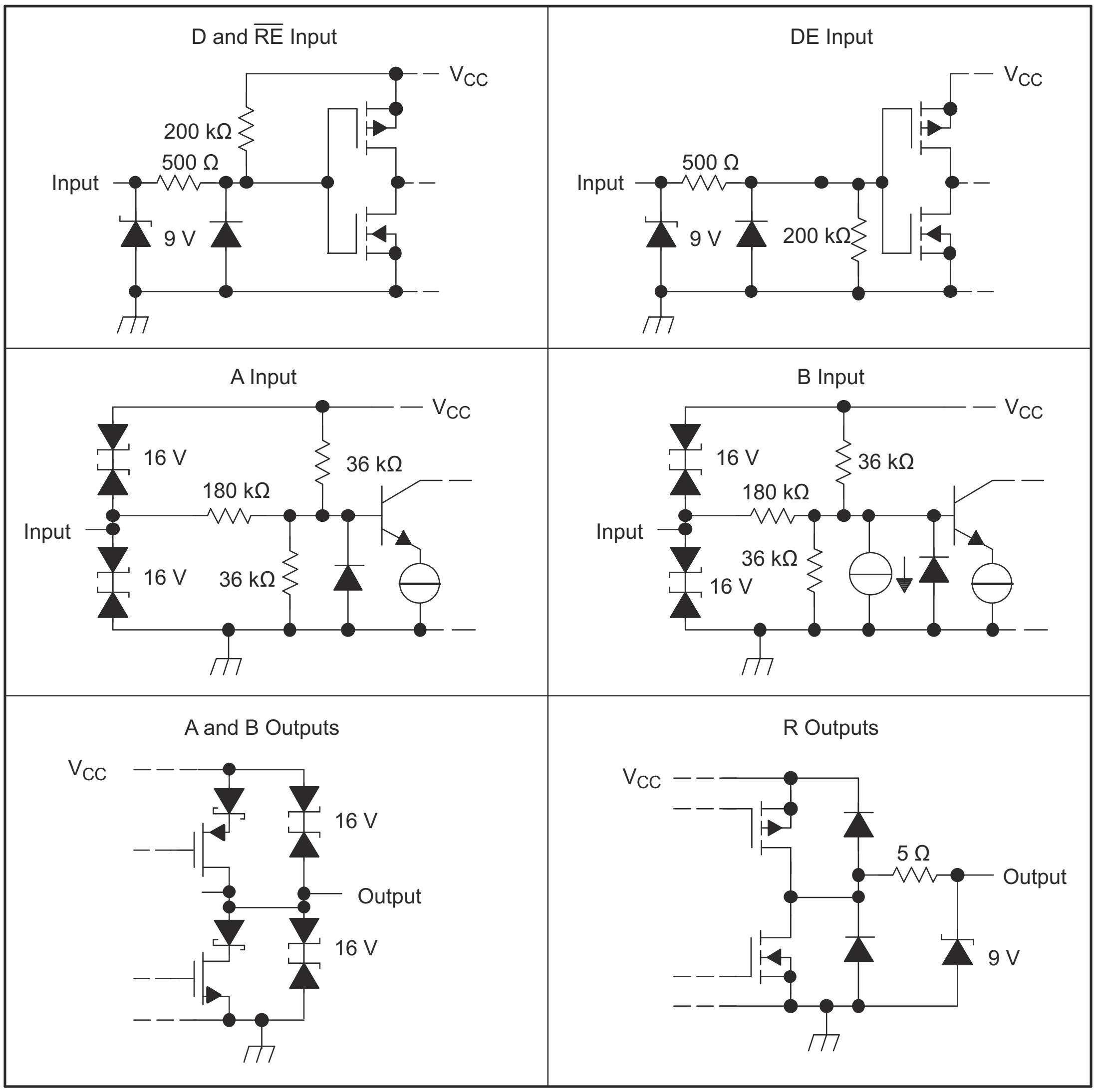


图 8-1. Equivalent Input and Output Schematic Diagrams

9 Application and Implementation

备注

以下应用部分中的信息不属于 TI 器件规格的范围，TI 不担保其准确性和完整性。TI 的客 户应负责确定器件是否适用于其应用。客户应验证并测试其设计，以确保系统功能。

9.1 Application Information

The SN65HVD485E device is a half-duplex RS-485 transceiver commonly used for asynchronous data transmissions. The driver and receiver enable pins allow for configuration of different operating modes.

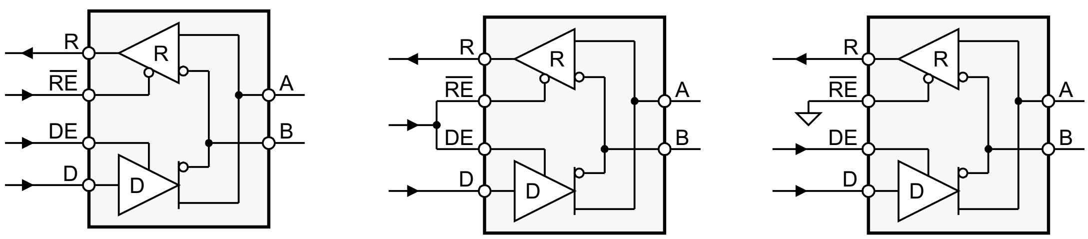


图 9-1. Half-Duplex Transceiver Configurations

Using independent enable lines provides the most flexible control as it allows for the driver and the receiver to be turned on and off individually. While this configuration requires two control lines, it allows for selective listening into the bus traffic whether the driver is transmitting data or not.

Combining the enable signals simplifies the interface to the controller by forming a single direction-control signal. In this configuration, the transceiver operates as a driver when the direction-control line is high and as a receiver when the direction-control line is low.

Additionally, only one line is required when connecting the receiver-enable input to ground and controlling only the driver-enable input. In this configuration, a node receives the data from the bus, receives the data it sends, and can verify that the correct data has been transmitted.

9.2 Typical Application

An RS-485 bus consists of multiple transceivers connecting in parallel to a bus cable. To eliminate line reflections, each cable end is terminated with a termination resistor (R_T) whose value matches the characteristic impedance (Z_0) of the cable. This method, known as parallel termination, allows for higher data rates over longer cable length.

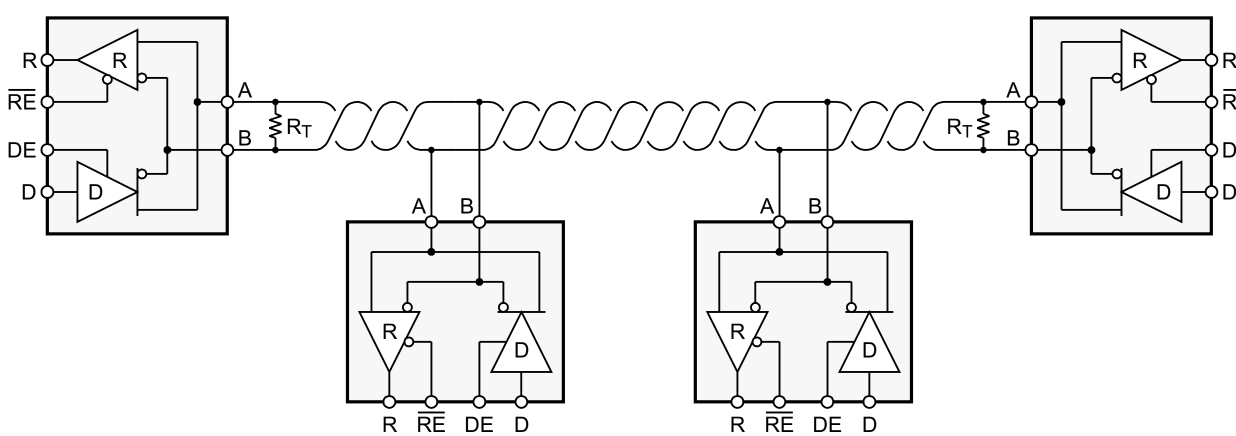


图 9-2. Typical RS-485 Network With Half-Duplex Transceivers

9.2.1 Design Requirements

RS-485 is a robust electrical standard suitable for long-distance networking that can be used in a wide range of applications with varying requirements such as distance, data rate, and number of nodes.

9.2.1.1 Data Rate and Bus Length

There is an inverse relationship between data rate and bus length: the higher the data rate, the shorter the cable length, and conversely the lower the data rate, the longer the cable can be without introducing data errors. While most RS-485 systems use data rates between 10 kbps and 100 kbps, some applications require data rates up to 250 kbps at distances of 4000 feet and longer. Longer distances are possible by allowing for small signal jitter of up to 5 or 10%.

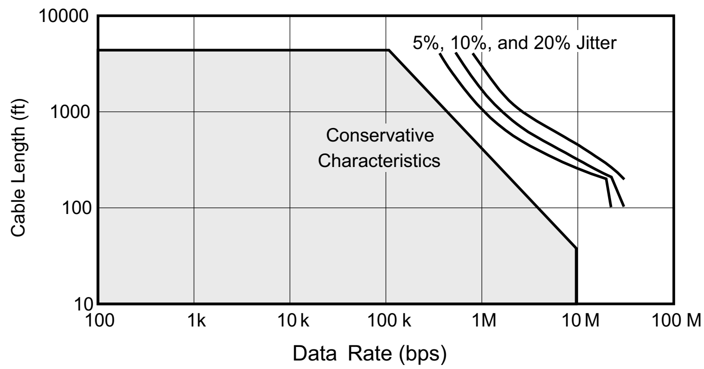


图 9-3. Cable Length vs Data Rate Characteristic

9.2.1.2 Stub Length

When connecting a node to the bus, the distance between the transceiver inputs and the cable trunk, known as the stub, must be as short as possible. Stubs present a nonterminated piece of bus line that can introduce reflections as the length of the stub increases. As a general guideline, the electrical length, or round-trip delay, of a stub must be less than one-tenth of the rise time of the driver; thus giving a maximum physical stub length as shown in 方程式 1.

$$L_{stub} \leqslant 0.1 \times t_r \times v \times c \tag{1}$$

where

- t_r is the 10/90 rise time of the driver
- *c* is the speed of light (3×10^8 m/s)
- *v* is the signal velocity of the cable or trace as a factor of *c*

9.2.1.3 Bus Loading

The RS-485 standard specifies that a compliant driver must be able to drive 32-unit loads (UL), where 1-unit load represents a load impedance of approximately 12 kΩ. Because the SN65HVD485E device is a ½ UL transceiver, it is possible to connect up to 64 receivers to the bus.

9.2.1.4 Receiver Failsafe

The differential receiver of the SN65HVD485E device is failsafe to invalid bus states caused by the following:

- Open bus conditions such as a disconnected connector
- Shorted bus conditions such as cable damage shorting the twisted pair together
- Idle bus conditions that occur when no driver on the bus is actively driving

In any of these cases, the differential receiver outputs a failsafe logic-high state so that the output of the receiver is not indeterminate.

Receiver failsafe is accomplished by offsetting the receiver thresholds such that the *input indeterminate* range does not include zero volts differential. To comply with the RS-422 and RS-485 standards, the receiver output must output a high when the differential input V_{ID} is more positive than 200 mV, and it must output a Low when V_{ID} is more negative than –200 mV. The receiver parameters that determine the failsafe performance are V_{IT+}, V_{IT-}, and V_{hys} (the separation between V_{IT+} and V_{IT-}). As shown in the 节 7.6 table, differential signals more negative than –200 mV cause a low receiver output, and differential signals more positive than 200 mV cause a high receiver output.

When the differential input signal is close to zero, it is still above the V_{IT+} threshold, and the receiver output is High. Only when the differential input is more than V_{hys} below V_{IT+} does the receiver output transition to a Low state. Therefore, the noise immunity of the receiver inputs during bus fault conditions includes the receiver hysteresis value (V_{hys}) as well as the value of V_{IT+}.

9.2.2 Detailed Design Procedure

To protect bus nodes against high-energy transients, the implementation of external transient protection devices is necessary.

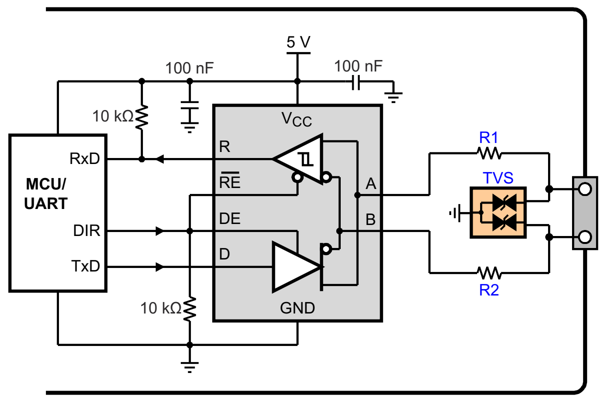


图 9-4. Transient Protection Against ESD, EFT, and Surge Transients

图 9-4 suggests a protection circuit against 10-kV ESD (IEC 61000-4-2), 4-kV EFT (IEC 61000-4-4), and 1-kV surge (IEC 61000-4-5) transients. 表 9-1 shows the associated bill of materials.

表 9-1. Bill of Materials

DEVICE	FUNCTION	ORDER NUMBER	MANUFACTURER
XCVR	5-V, 10-Mbps RS-485 transceiver	SN65HVD485E	TI
R1, R2	10-Ω, pulse-proof thick-film resistor	CRCW0603010RJNEAHP	Vishay
TVS	Bidirectional 400-W transient suppressor	CDSOT23-SM712	Bourns

9.2.2.1 Power Usage in an RS-485 Transceiver

Power consumption is a concern in many applications. Power supply current is delivered to the bus load and to the transceiver circuitry. For a typical RS-485 bus configuration, the load that an active driver must drive consists of all of the receiving nodes plus the termination resistors at each end of the bus.

The load presented by the receiving nodes depends on the input impedance of the receiver. The TIA/EIA-485-A standard defines a unit load as allowing up to 1 mA. With up to 32 unit loads allowed on the bus, the total current supplied to all receivers can be as high as 32 mA. The SN65HVD485E device is rated as a ½ unit load device, so up to 64 can be connected on one bus.

The current in the termination resistors depends on the differential bus voltage. The standard requires active drivers to produce at least 1.5 V of differential signal. For a bus terminated with one standard 120-Ω resistor at each end, this sums to 25-mA differential output current whenever the bus is active. Typically, the SN65HVD485E device can drive more than 25 mA to a 60-Ω load, which results in a differential output voltage higher than the minimum required by the standard (see 图 7-2).

Supply current increases with signaling rate primarily because of the totem pole outputs of the driver. When these outputs change state, there is a moment when both the high-side and low-side output transistors are conducting, which creates a short spike in the supply current. As the frequency of state changes increases, more power is used.

9.2.3 Application Curve

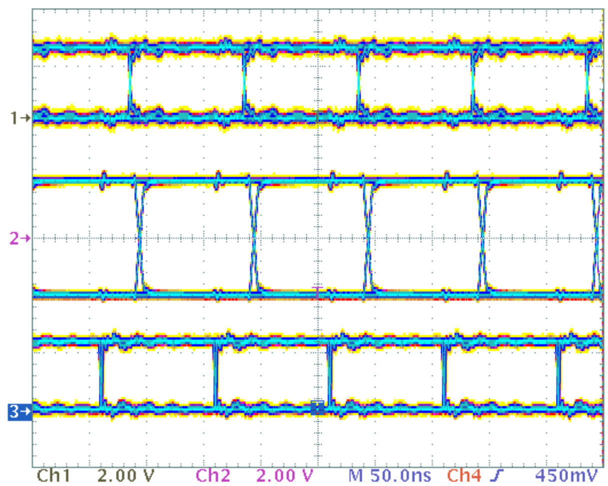


图 9-5. SN65HVD485E Single-Ended Input (Top), Differential Output (Middle), and Single-Ended Output (Bottom) at 10 MHz

9.3 Power Supply Recommendations

To ensure reliable operation at all data rates and supply voltages, each supply must be decoupled with a 100-nF ceramic capacitor located as close as possible to the supply pins. This helps to reduce supply voltage ripple present on the outputs of switched-mode power supplies and also helps to compensate for the resistance and inductance of the PCB power planes.

9.4 Layout

9.4.1 Layout Guidelines

Robust and reliable bus-node design often requires the use of external transient-protection devices to protect against EFT and surge transients that may occur in industrial environments. Because these transients have a wide frequency bandwidth (from approximately 3 MHz to 3 GHz), high-frequency layout techniques must be applied during PCB design.

1. Place the protection circuitry close to the bus connector to prevent noise transients from entering the board.
2. Use V_{CC} and ground planes to provide low-inductance power distribution. High-frequency currents tend to follow the path of least inductance and not the path of least resistance.
3. Design the protection components into the direction of the signal path. Do not force the transient currents to divert from the signal path to reach the protection device.
4. Apply 100-nF to 220-nF bypass capacitors as close as possible to the V_{CC} pins of transceiver, UART, or controller ICs on the board.
5. Use at least two vias for V_{CC} and ground connections of bypass capacitors and protection devices to minimize effective via inductance.
6. Use 1-kΩ to 10-kΩ pullup or pulldown resistors for enable lines to limit noise currents in these lines during transient events.
7. Insert series pulse-proof resistors into the A and B bus lines if the TVS clamping voltage is higher than the specified maximum voltage of the transceiver bus terminals. These resistors limit the residual clamping current into the transceiver and prevent it from latching up.
8. While pure TVS protection is sufficient for surge transients up to 1 kV, higher transients require metal-oxide varistors (MOVs), which reduces the transients to a few hundred volts of clamping voltage and transient blocking units (TBUs) that limit transient current to less than 1 mA.

9.4.2 Layout Example

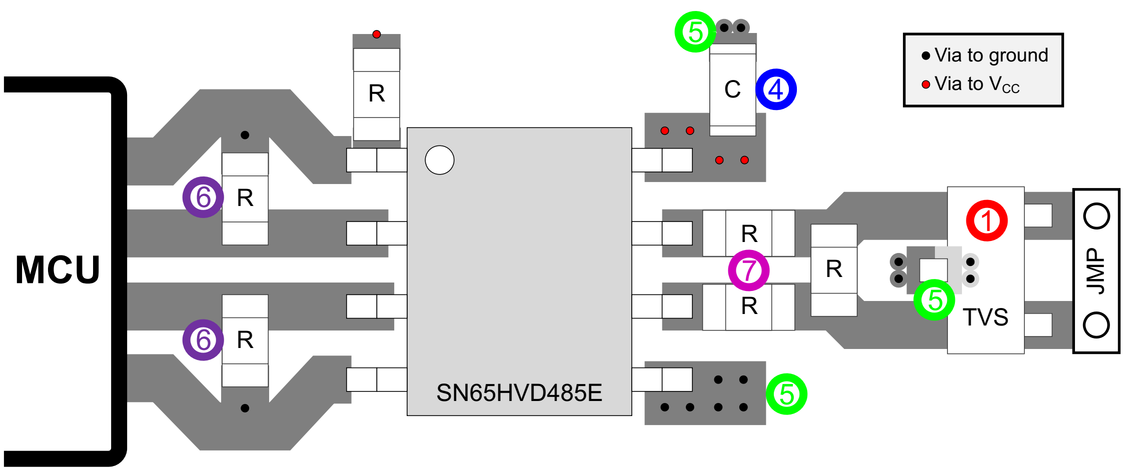


图 9-6. Layout Example

10 Device and Documentation Support

10.1 Device Support

10.1.1 Device Nomenclature

10.1.1.1 Thermal Characteristics of IC Packages

θ_{JA} (Junction-to-Ambient Thermal Resistance) is defined as the difference in junction temperature to ambient temperature divided by the operating power

θ_{JA} is NOT a constant and is a strong function of

- the PCB design (50% variation)
- altitude (20% variation)
- device power (5% variation)

θ_{JA} can be used to compare the thermal performance of packages if the specific test conditions are defined and used. Standardized testing includes specification of PCB construction, test chamber volume, sensor locations, and the thermal characteristics of holding fixtures. θ_{JA} is often misused when it is used to calculate junction temperatures for other installations.

TI uses two test PCBs as defined by JEDEC specifications. The low-k board gives average in-use condition thermal performance and consists of a single trace layer 25 mm long and 2-oz thick copper. The high-k board gives best case in-use condition and consists of two 1-oz buried power planes with a single trace layer 25 mm long with 2-oz thick copper. A 4% to 50% difference in θ_{JA} can be measured between these two test cards

θ_{JC} (Junction-to-Case Thermal Resistance) is defined as difference in junction temperature to case divided by the operating power. It is measured by putting the mounted package up against a copper block cold plate to force heat to flow from die, through the mold compound into the copper block.

θ_{JC} is a useful thermal characteristic when a heatsink is applied to package. It is NOT a useful characteristic to predict junction temperature as it provides pessimistic numbers if the case temperature is measured in a non-standard system and junction temperatures are backed out. It can be used with θ_{JB} in 1-dimensional thermal simulation of a package system.

θ_{JB} (Junction-to-Board Thermal Resistance) is defined to be the difference in the junction temperature and the PCB temperature at the center of the package (closest to the die) when the PCB is clamped in a cold-plate structure. θ_{JB} is only defined for the high-k test card.

θ_{JB} provides an overall thermal resistance between the die and the PCB. It includes a bit of the PCB thermal resistance (especially for BGA's with thermal balls) and can be used for simple 1-dimensional network analysis of package system (see 图 10-1).

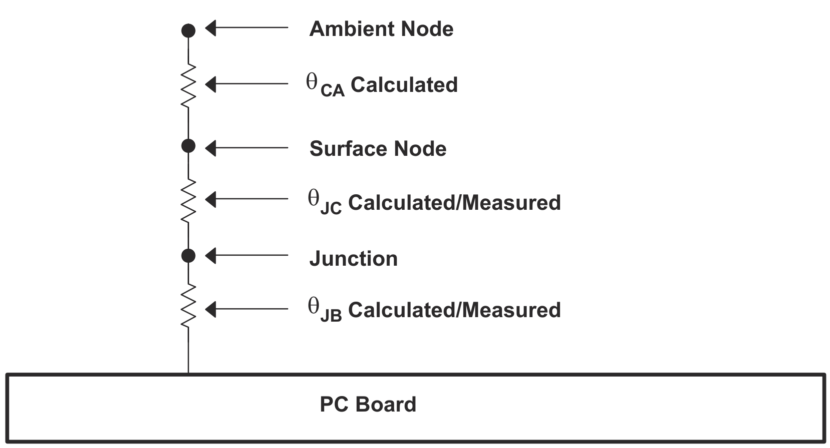


图 10-1. Thermal Resistance

10.2 Documentation Support

10.2.1 Related Documentation

For related documentation see the following:

SZZA003, *Package Thermal Characterization Methodologies*

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10.3 支持资源

TI E2E™ 支持论坛是工程师的重要参考资料，可直接从专家获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题可获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的《使用条款》。

10.4 Trademarks

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10.5 静电放电警告

静电放电 (ESD) 会损坏这个集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

10.6 术语表

TI 术语表　　本术语表列出并解释了术语、首字母缩略词和定义。

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN65HVD485ED	OBSOLETE	SOIC	D	8		TBD	Call TI	Call TI	-40 to 85	VP485	
SN65HVD485EDGKR	ACTIVE	VSSOP	DGK	8	2500	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 85	(NWH, NWJ)	Samples
SN65HVD485EDR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	VP485	Samples
SN65HVD485EDRG4	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	VP485	Samples
SN65HVD485EP	ACTIVE	PDIP	P	8	50	RoHS & Green	NIPDAU	N / A for Pkg Type	-40 to 85	65HVD485	Samples
SN65HVD485EPE4	ACTIVE	PDIP	P	8	50	RoHS & Green	NIPDAU	N / A for Pkg Type	-40 to 85	65HVD485	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

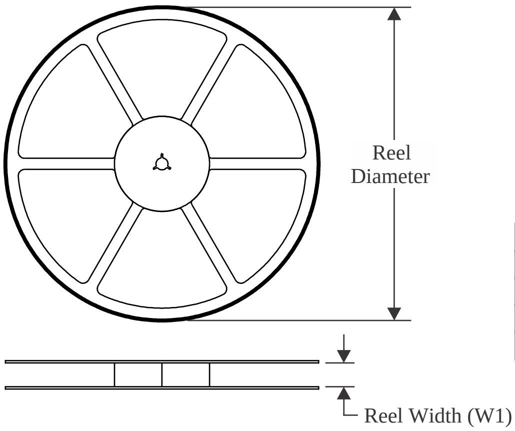
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

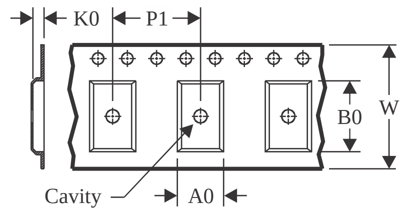
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

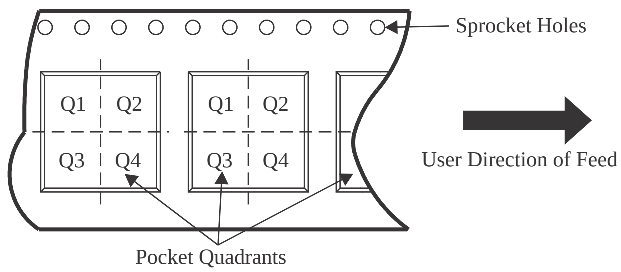


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

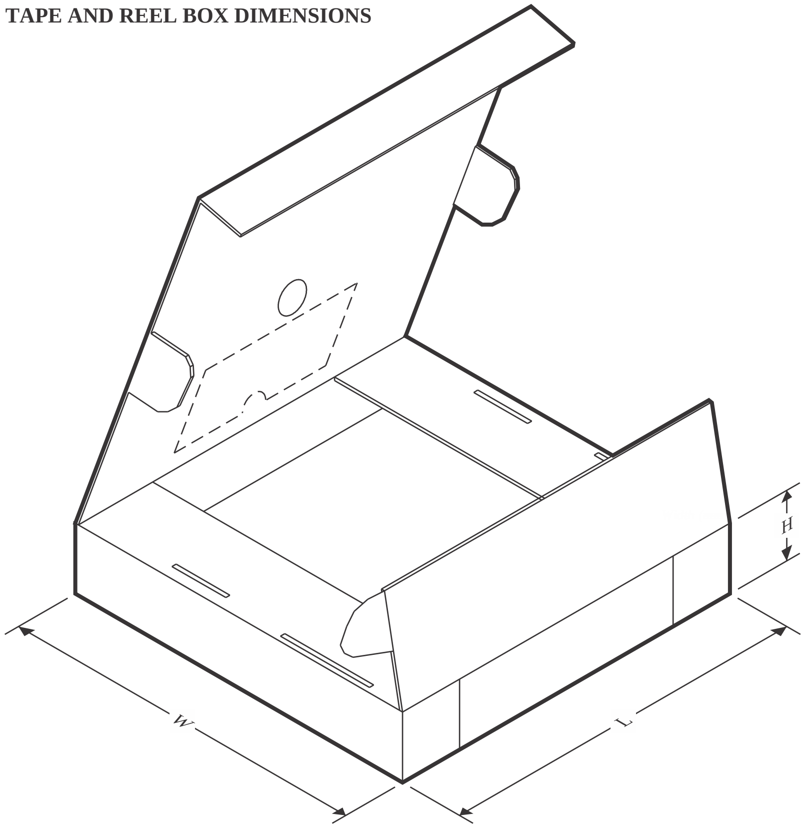
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN65HVD485EDGKR	VSSOP	DGK	8	2500	330.0	12.4	5.25	3.35	1.25	8.0	12.0	Q1
SN65HVD485EDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

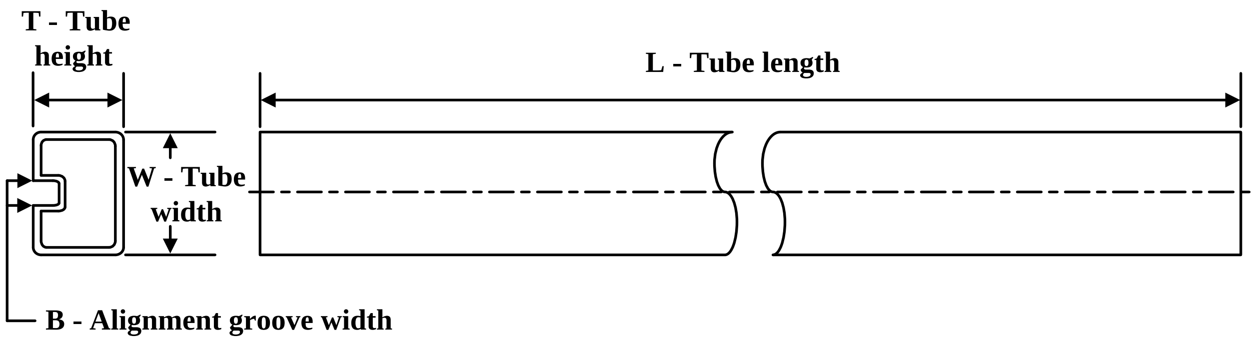
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN65HVD485EDGKR	VSSOP	DGK	8	2500	366.0	364.0	50.0
SN65HVD485EDR	SOIC	D	8	2500	356.0	356.0	35.0

TUBE



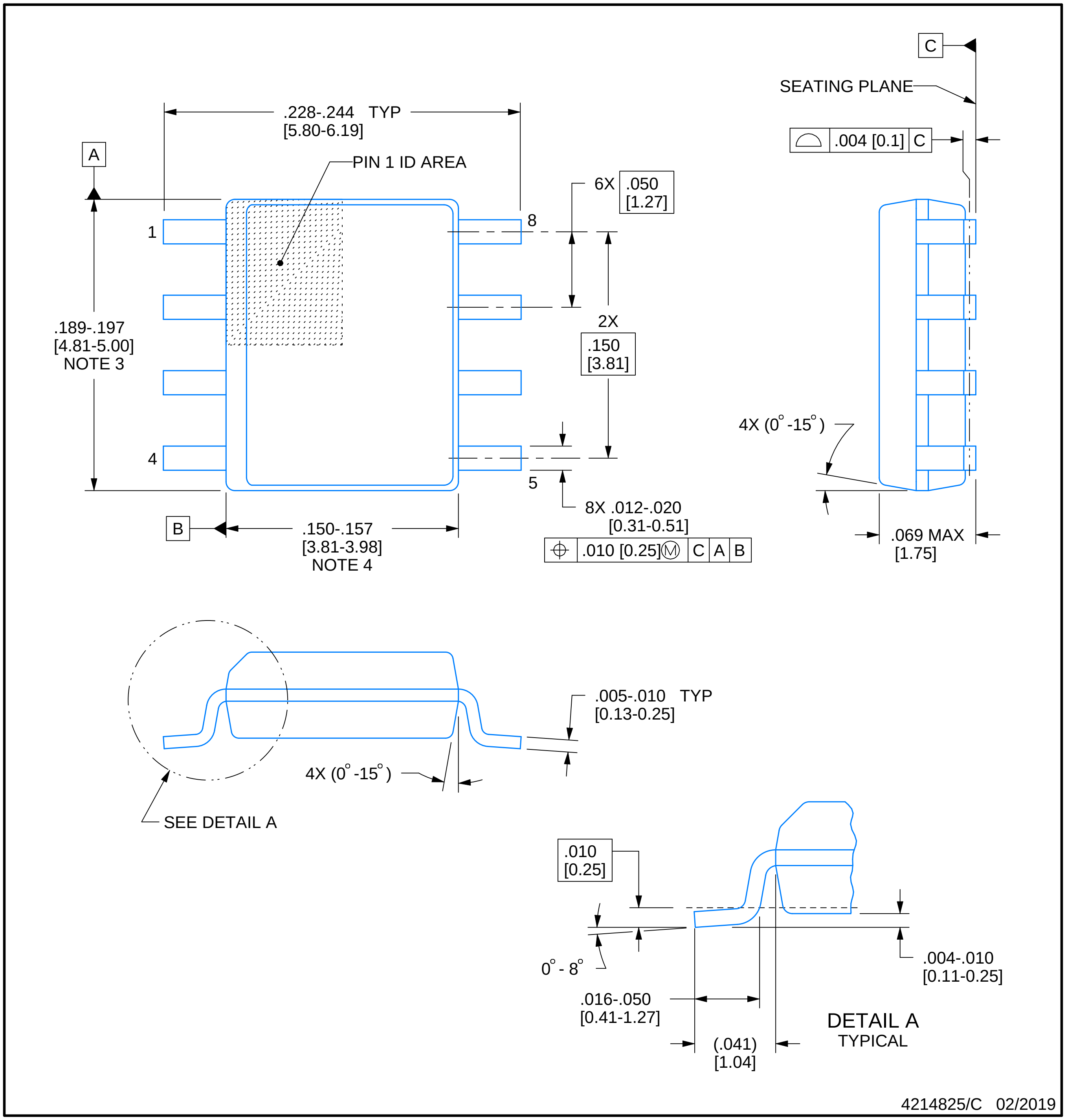
*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
SN65HVD485EP	P	PDIP	8	50	506	13.97	11230	4.32
SN65HVD485EPE4	P	PDIP	8	50	506	13.97	11230	4.32

D0008A

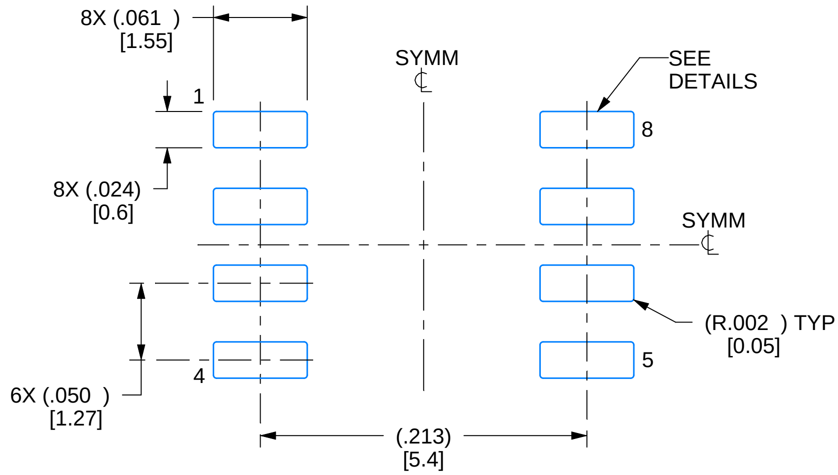
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

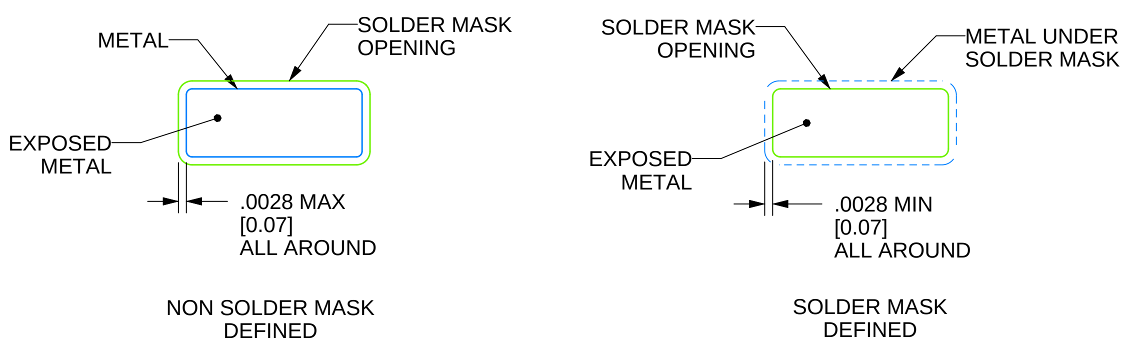


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X

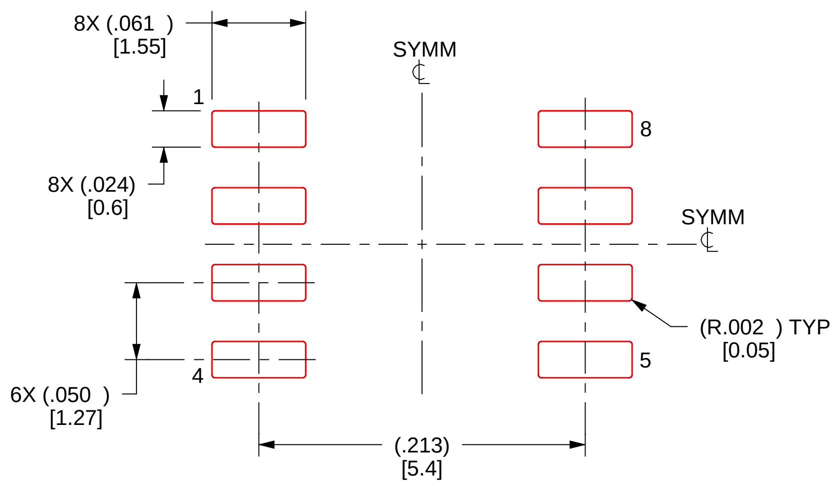


SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



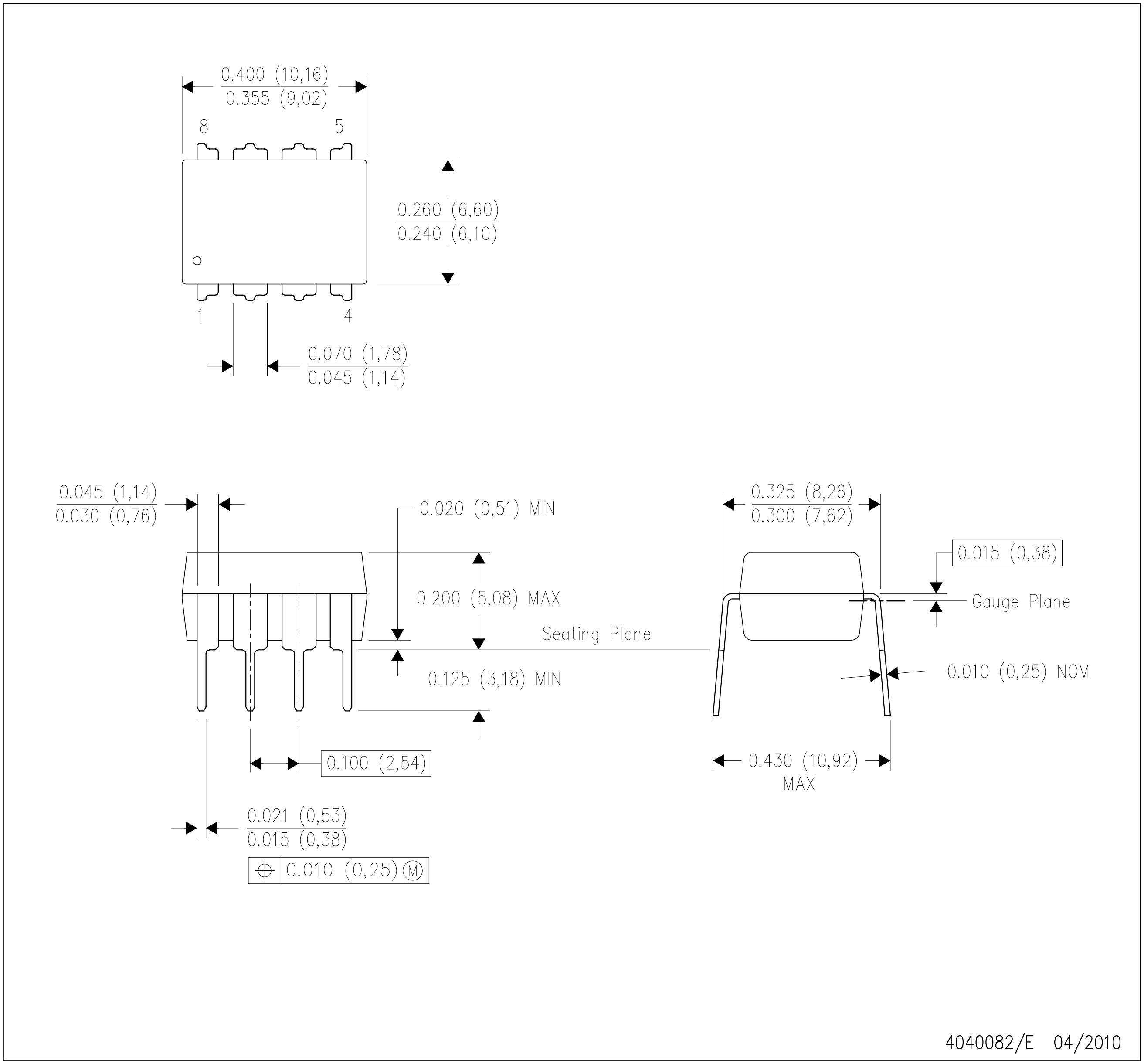
SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

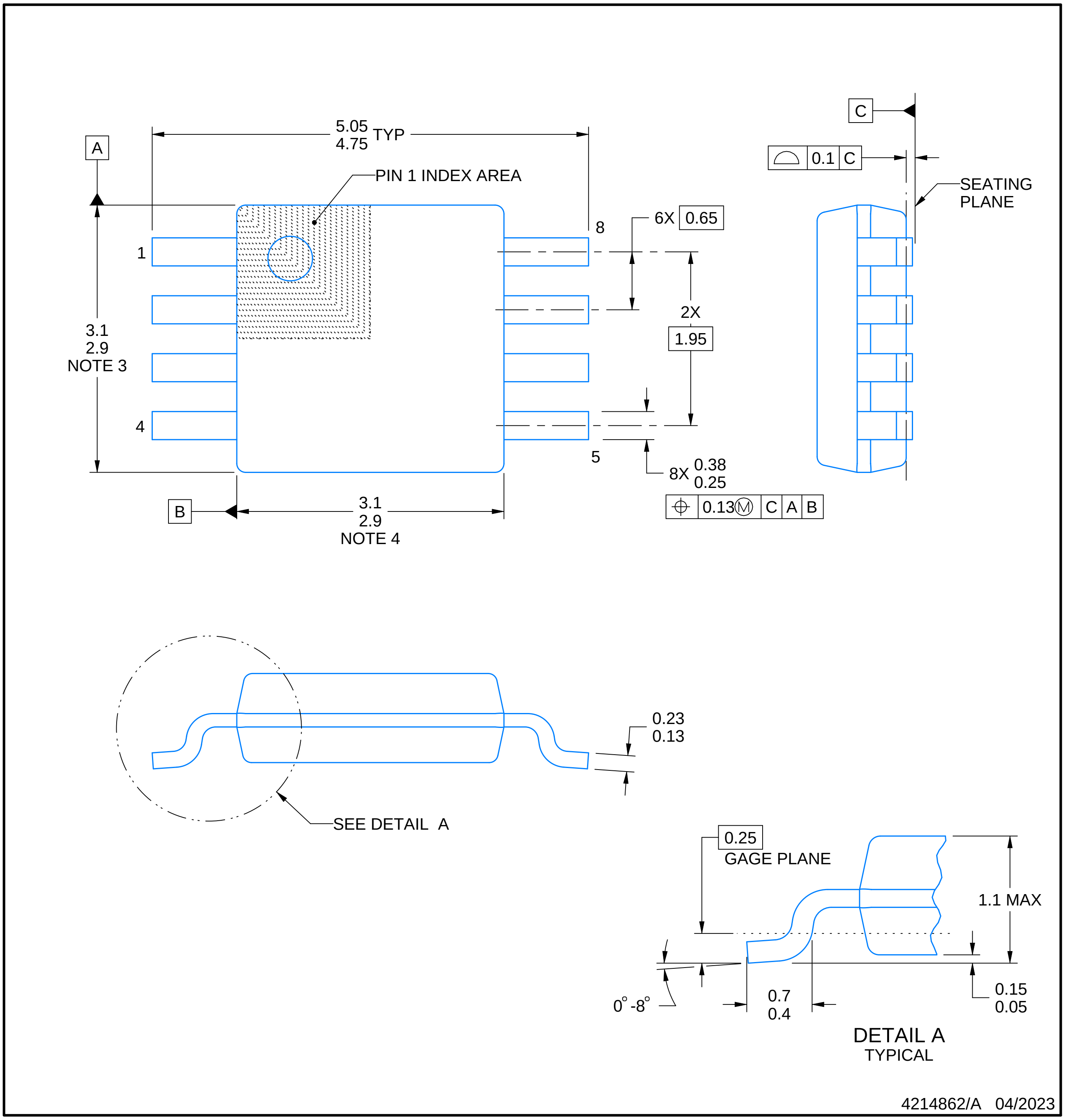
NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

P (R–PDIP–T8) PLASTIC DUAL–IN–LINE PACKAGE



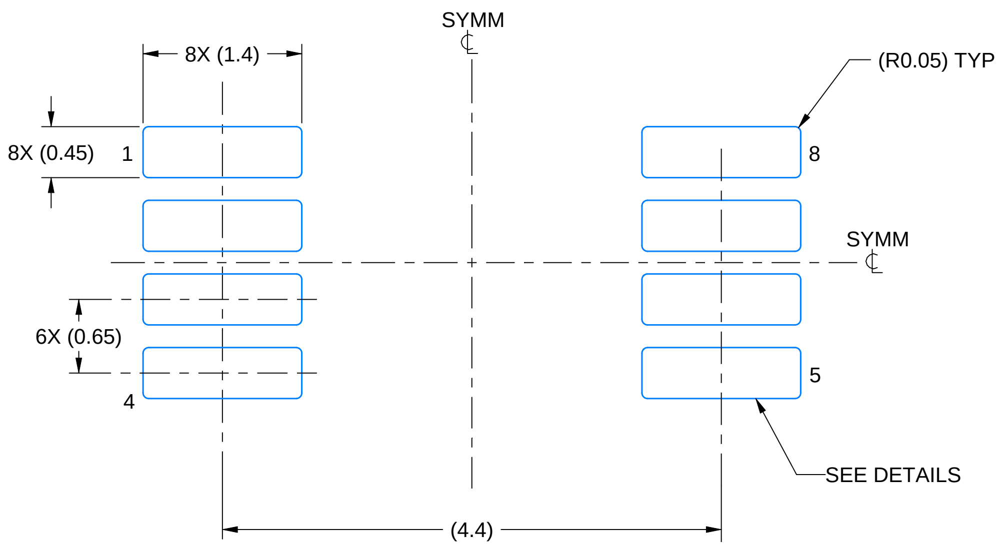
NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001 variation BA.



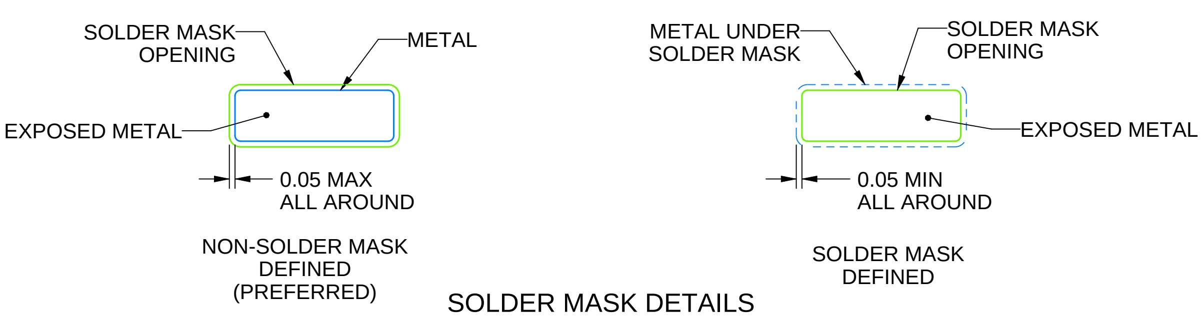
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X



SOLDER MASK DETAILS

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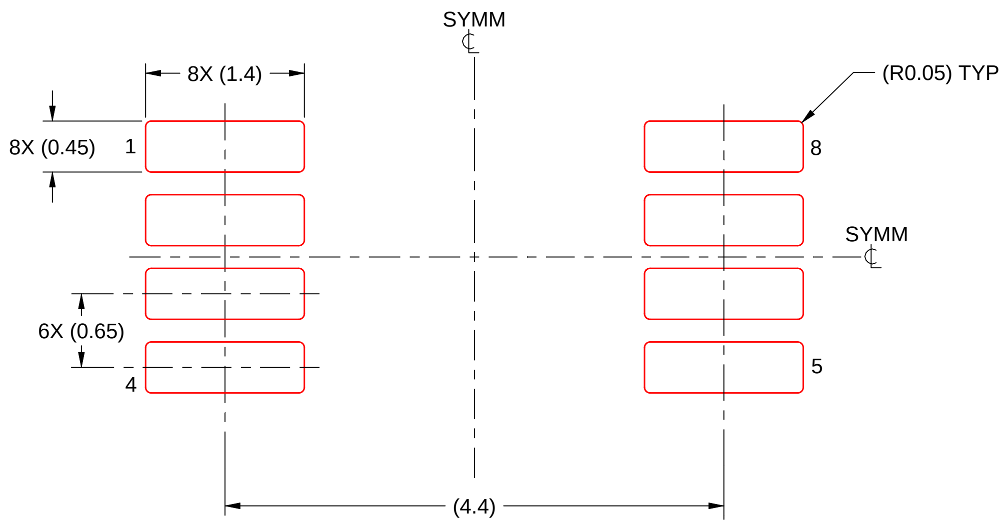
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.



SOLDER PASTE EXAMPLE
SCALE: 15X

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NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

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