参考文献

SNx5LBC174A 四路 RS-485 差分线路驱动器

1 特性

- 专为 TIA/EIA-485、TIA/EIA-422 和 ISO 8482 应用而设计
- 信号传输速率 [1] 高达 30Mbps
- 传播延迟时间 < 11ns
- 低待机功耗 - 最大 1.5mA
- 输出 ESD 保护：12kV
- 驱动器正负电流限制
- 上电和下电无干扰运行，适用于线路插入应用
- 热关断保护
- 业界通用引脚排列，与 SN75174、MC3487、DS96174、LTC487 和 MAX3042 兼容

2 应用

- 电机驱动器
- 工厂自动化和控制

3 说明

SN65LBC174A 和 SN75LBC174A 是具有三态输出的四通道差分线路驱动器，专为 TIA/EIA-485 (RS-485)、TIA/EIA-422 (RS-422) 和 ISO 8482 应用而设计。

这些器件经优化，能够以高达 30Mbit/s 的信号传输速率实现平衡多点总线传输。此传输介质可以是印刷电路板走线、底板、或者电缆。最终数据传输速率和距离取决于介质衰减特性和环境噪声耦合。

每个驱动器都具有电流限制和热关断电路，因此适用于嘈杂环境中的高速多点数据传输应用。这些器件采用 LinBiCMOS® 进行设计，有助于实现低功耗和稳健性。

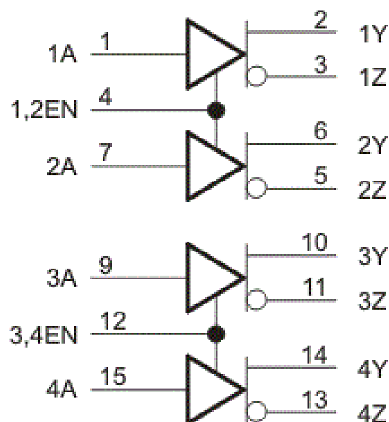
两个使能 (EN) 输入为驱动器提供两个使能端，或可通过外部集成，在单一信号下对所有四个驱动器进行使能控制。禁用或断电后，驱动器输出为总线提供高阻抗，从而降低系统负载。

SN75LBC174A 可在 0°C 至 70°C 的工作温度范围内运行。SN65LBC174A 可在 -40°C 至 85°C 的温度范围内运行。

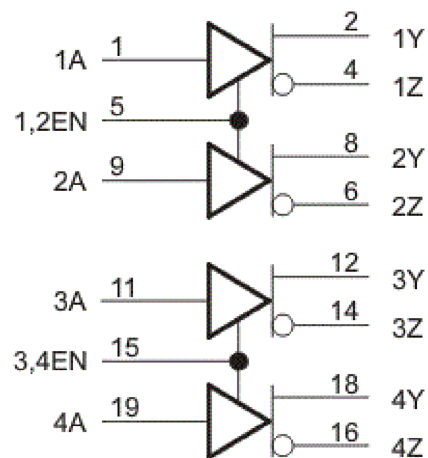
封装信息

器件型号	封装(1)	封装尺寸(2)
SN65LBC174A SN75LBC174A	SOIC（DW，16）	10.3mm x 10.3mm
	SOIC（DW，20）	12.8mm x 10.3mm
	PDIP（N，16）	19.3mm × 9.4mm

(1) 有关更多信息，请参阅节 11。
(2) 封装尺寸（长 × 宽）为标称值，并包括引脚（如适用）。



逻辑图（正逻辑）



逻辑图（正逻辑）

[1] 线路的信号传输速率是每秒进行电压转换的次数，以单位 bps（每秒位数）来表示。

本资源的原文使用英文撰写。 为方便起见，TI 提供了译文；由于翻译过程中可能使用了自动化工具，TI 不保证译文的准确性。 为确认准确性，请务必访问 ti.com 参考最新的英文版本（控制文档）。

Table of Contents

1 特性........ 1
2 应用........ 1
3 说明........ 1
4 Pin Configuration and Functions........ 3
5 Specifications........ 4
5.1 Absolute Maximum Ratings........ 4
5.2 Dissipation Rating Table........ 4
5.3 Recommended Operating Conditions........ 4
5.4 Thermal Information........ 5
5.5 Electrical Characteristics........ 6
5.6 Switching Characteristics........ 6
5.7 Typical Characteristics........ 7
6 Parameter Measure Information........ 8
7 Device Functional Modes........ 13
8 Application and Implementation........ 14
8.1 Application Information........ 14
9 Device and Documentation Support........ 15
9.1 接收文档更新通知........ 15
9.2 支持资源........ 15
9.3 Trademarks........ 15
9.4 静电放电警告........ 15
9.5 术语表........ 15
10 Revision History........ 15
11 Mechanical, Packaging, and Orderable Information........ 16

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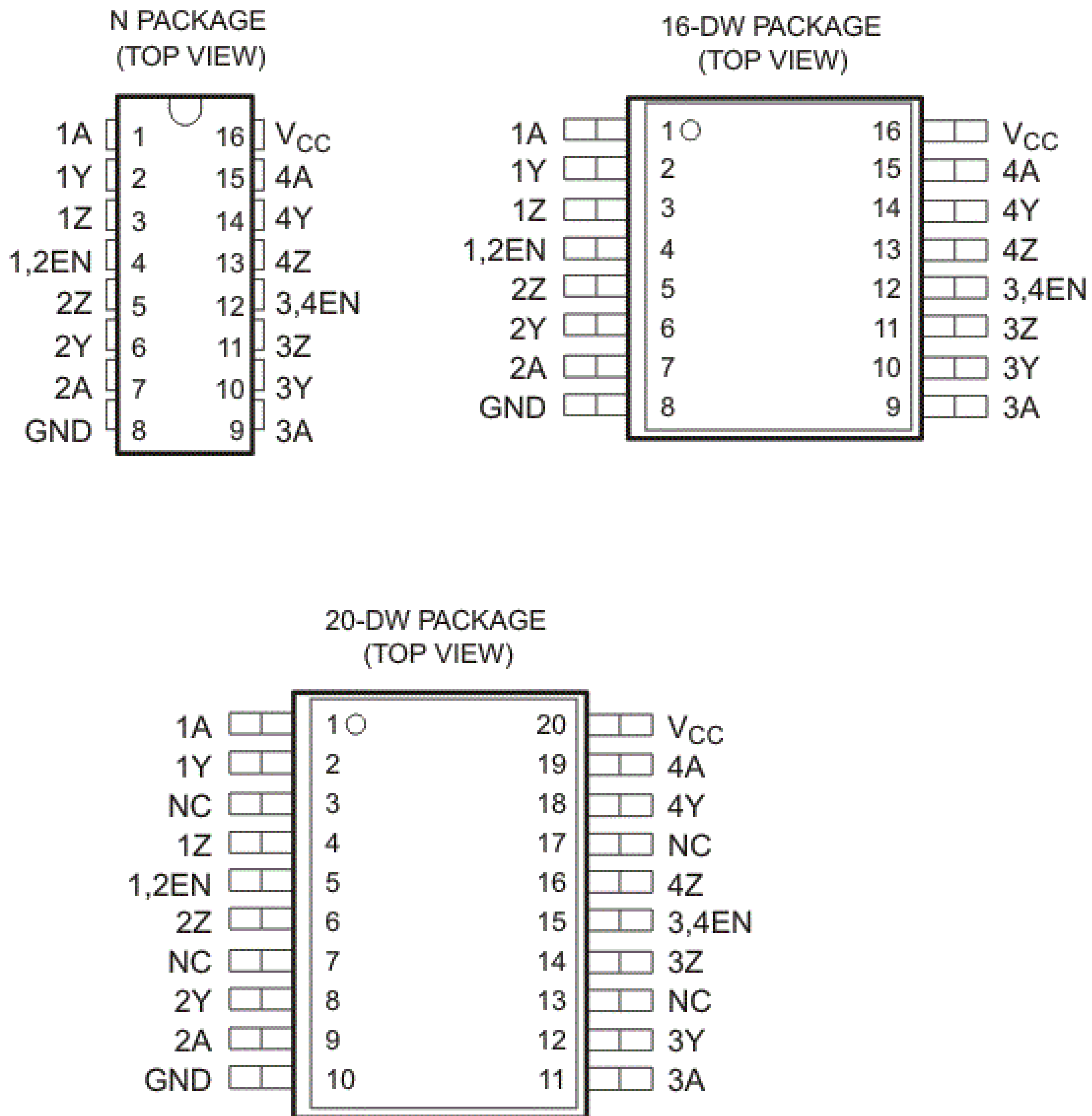
4 Pin Configuration and Functions



5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			VALUE / UNIT
Supply voltage range, V_{CC} (2)			–0.3 V to 6 V
Voltage range at any bus (DC)			–10 V to 15 V
Voltage range at any bus (transient pulse through 100 Ω, see 图 6-8)			–30 V to 30 V
Input voltage range at any A or EN terminal, V_I			–0.5 V to V_{CC} + 0.5 V
Electrostatic discharge	Human body model (3)	Y, Z, and GND	±12 kV
		All pins	±5 kV
	Charged-device model (4)	All pins	±1 kV
Storage temperature range, T_{stg}			–65°C to 150°C
Continuous power dissipation			See Dissipation Rating Table

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values, except differential I/O bus voltages, are with respect to GND.
(3) Tested in accordance with JEDEC standard 22, Test Method A114-A.
(4) Tested in accordance with JEDEC standard 22, Test Method C101.

5.2 Dissipation Rating Table

表 5-1. Dissipation Rating Table

PACKAGE(1)	JEDEC BOARD MODEL	T_A ≤ 25°C POWER RATING	DERATING FACTOR (2) ABOVE T_A = 25°C	T_A = 70°C POWER RATING	T_A = 85°C POWER RATING
16 DW	LOW K	1200 mW	9.6 mW/°C	769 mW	625 mW
	HIGH K	2240 mW	17.9 mW/°C	1434 mW	1165 mW
20 DW	LOW K	1483 mW	11.86 mW/°C	949 mW	771 mW
	HIGH K	2753 mW	22 mW/°C	1762 mW	1432 mW
16 N	LOW K	1150 mW	9.2 mW/°C	736 mW	598 mW

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.
(2) This is the inverse of the junction-to-ambient thermal resistance when board-mounted and with no air flow.

5.3 Recommended Operating Conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}		4.75	5	5.25	V
Voltage at any bus terminal	Y, Z	–7		12	V
High-level input voltage, V_{IH}	A, EN	2		V_{CC}	V
Low-level input voltage, V_{IL}		0		0.8	
Output current		–60		60	mA
Operating free-air temperature, T_A	SN75LBC174A	0		70	°C
	SN65LBC174A	–40		85	

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5.4 Thermal Information

THERMAL METRIC[1]		SN75ALS174A			UNIT
		N (PDIP)	DW (SOIC)	DW	
		16 PINS	16 PINS	20 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	60.6	71.1	66.8	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	48.1	37.4	34.4	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	40.6	36.8	39.7	°C/W
ψ_{JT}	Junction-to-top characterization parameter	27.5	13.3	8.9	°C/W
ψ_{JB}	Junction-to-board characterization parameter	40.3	36.4	39	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	n/a	n/a	n/a	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

5.5 Electrical Characteristics

over recommended operating conditions

PARAMETER		TEST CONDITIONS		MIN	TYP[1]	MAX	UNIT
V_{IK}	Input clamp voltage	I_I = -18 mA		–1.5	–0.77		V
V_O	Open-circuit output voltage	Y or Z, No load		0		V_{CC}	V
$\lvert V_{OD(SS)} \rvert$	Steady-state differential output voltage magnitude[2]	No load (open circuit)		3		V_{CC}	V
		R_L = 54Ω, See 图 6-1		1	1.6	2.5	
		With common-mode loading, See 图 6-2		1	1.6	2.5	
$\Delta V_{OD(SS)}$	Change in steady-state differential output voltage between logic states	See 图 6-1		–0.1		0.1	V
$V_{OC(SS)}$	Steady-state common-mode output voltage	See 图 6-3		2	2.4	2.8	V
$\Delta V_{OC(SS)}$	Change in steady-state common-mode output voltage between logic states	See 图 6-3		–0.02		0.02	V
I_I	Input current	A, EN		–50		50	μA
I_{OS}	Short-circuit output current	V_{TEST} = -7V to 12V, See 图 6-7	V_I = 0V	–200		200	mA
			$V_I = V_{CC}$				
I_{OZ}	High-impedance-state output current		EN at 0V	–50		50	μA
$I_{O(OFF)}$	Output current with power off		V_{CC} = 0V	–10		10	
I_{CC}	Supply current	V_I = 0V or V_{CC}, No load	All drivers enabled			23	mA
			All drivers disabled			1.5	
C_{IN}	Input Capacitance	A inputs			13		pF
		EN inputs			21		pF

(1) All typical values are at V_{CC} = 5V and 25°C.
(2) The minimum V_{OD} may not fully comply with TIA/EIA-485-A at operating temperatures below 0°C. System designers should take the possibly lower output signal into account in determining the maximum signal transmission distance.

5.6 Switching Characteristics

over recommended operating conditions

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high level output	R_L = 54Ω, C_L = 50pF, See 图 6-4	5.5	8	11	ns
t_{PHL}	Propagation delay time, high-to-low level output		5.5	8	11	ns
t_r	Differential output voltage rise time		2	7.5	11	ns
t_f	Differential output voltage fall time		2	7.5	11	ns
$t_{sk(p)}$	Pulse skew $\lvert t_{PLH} - t_{PHL} \rvert$			0.6	2	ns
				0.6	2	
$t_{sk(o)}$	Output skew[1]				2	ns
$t_{sk(pp)}$	Part-to-part skew[2]				3	ns
t_{PZH}	Propagation delay time, high-impedance-to-high-level output	See 图 6-5			25	ns
t_{PHZ}	Propagation delay time, high-level-output-to-high impedance				25	ns
t_{PZL}	Propagation delay time, high-impedance-to-low-level output	See 图 6-6			30	ns
t_{PLZ}	Propagation delay time, low-output-to-high impedance				20	ns

(1) Output skew ($t_{sk(o)}$) is the magnitude of the time delay difference between the outputs of a single device with all of the inputs connected together.
(2) Part-to-part skew ($t_{sk(pp)}$) is the magnitude of the difference in propagation delay times between any specified terminals of two devices when both devices operate with the same input signals, the same supply voltages, at the same temperature, and have identical packages and test circuits.

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5.7 Typical Characteristics

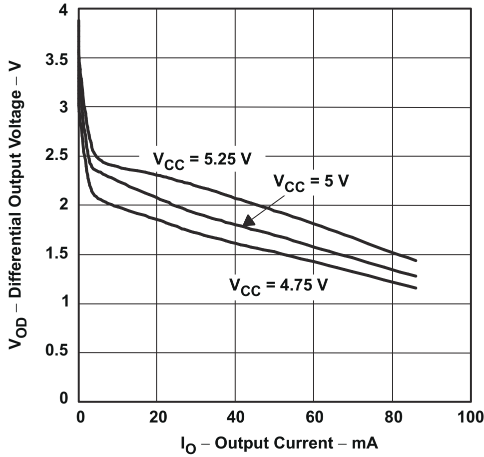


图 5-1. Differential Output Voltage vs Output Current

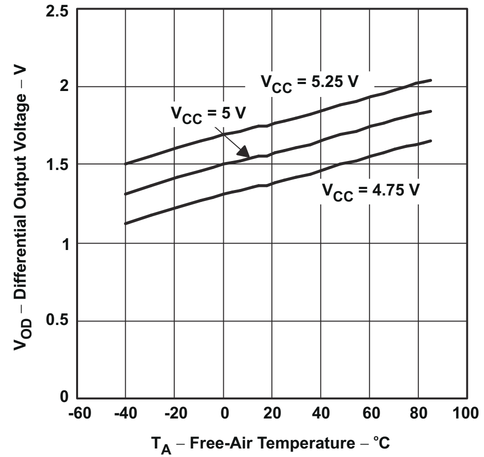


图 5-2. Differential Output Voltage vs Free-air Temperature

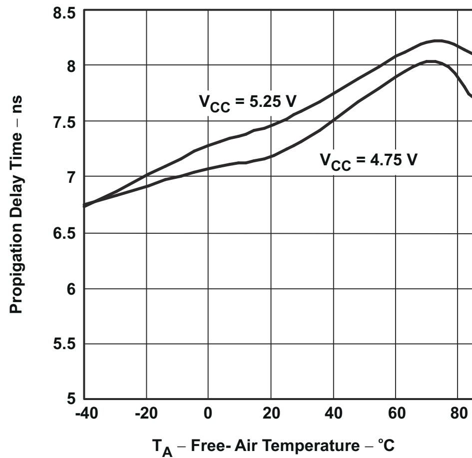


图 5-3. Propagation Delay Time vs Free-air Temperature

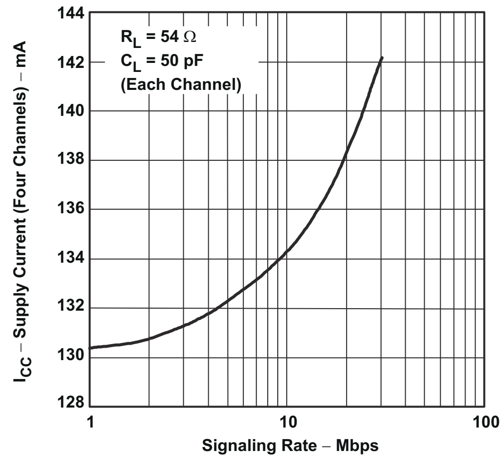


图 5-4. Supply Current (Four Channels) vs Signaling Rate

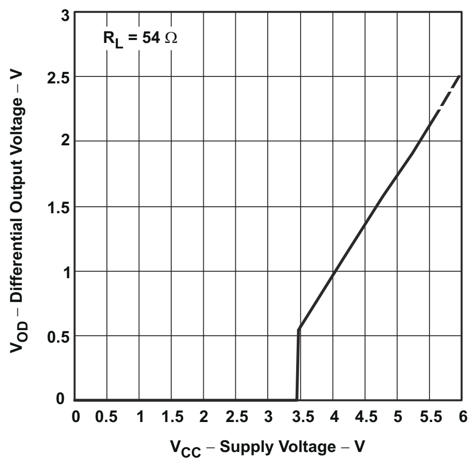


图 5-5. Differential Output Voltage vs Supply Voltage

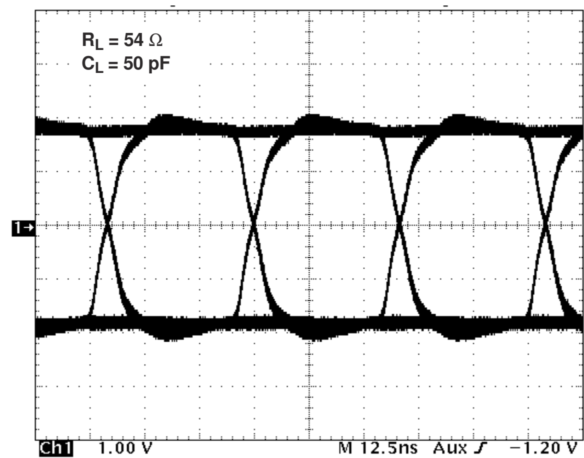


图 5-6. Eye Pattern, Pseudorandom Data at + 30Mbps

6 Parameter Measure Information

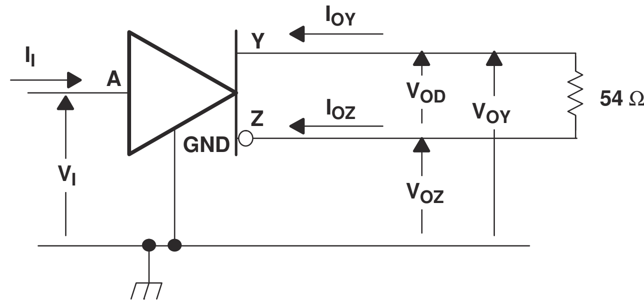


图 6-1. Test Circuit, V_{OD} Without Common-Mode Loading

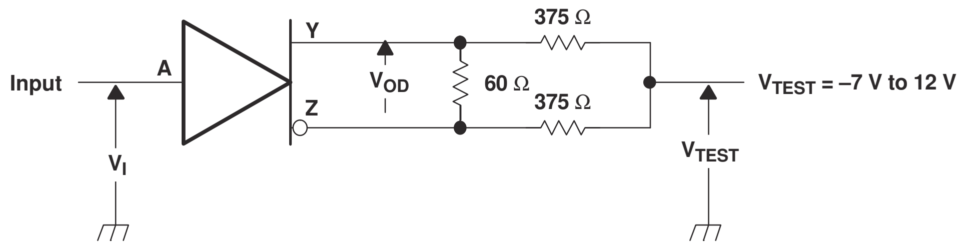
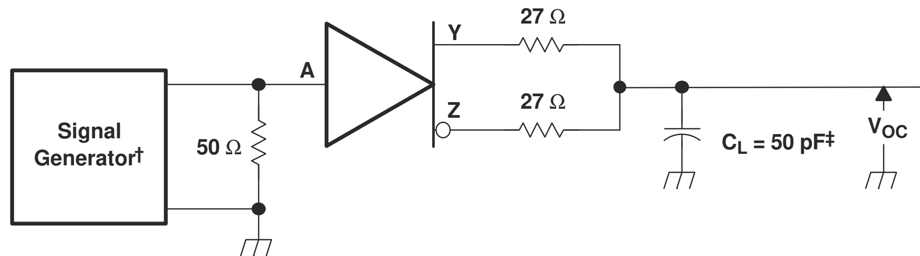


图 6-2. Test Circuit, V_{OD} With Common-Mode Loading



† PRR = 1 MHz, 50% Duty Cycle, t_r < 6 ns, t_f < 6 ns, Z_O = 50 Ω
‡ Includes probe and jig capacitance

图 6-3. V_{OC} Test Circuit

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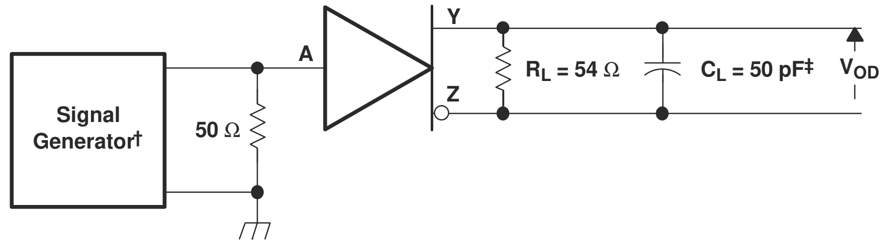


† PRR = 1 MHz, 50% Duty Cycle, t_r < 6 ns, t_f < 6 ns, Z_O = 50 Ω
‡ Includes probe and jig capacitance

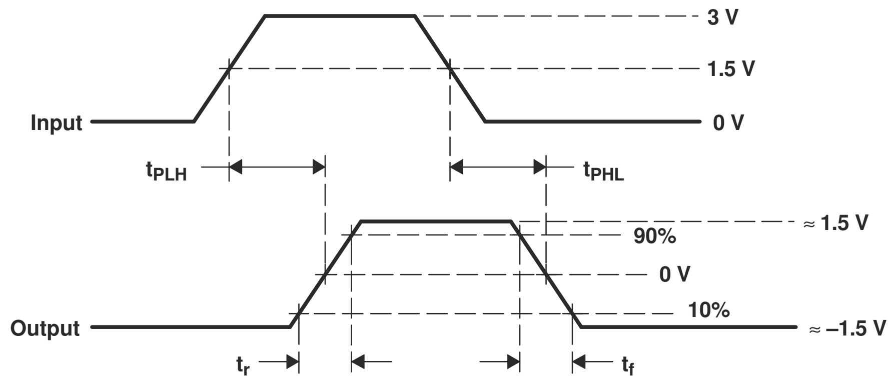
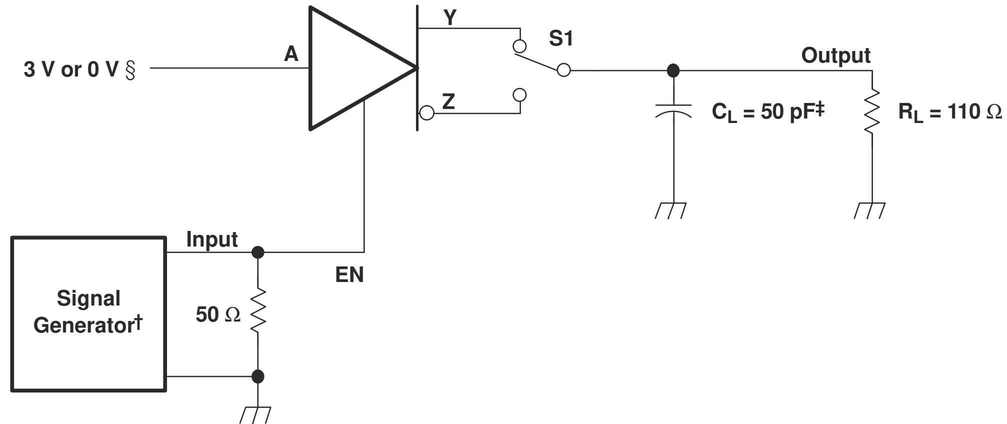


图 6-4. Output Switching Test Circuit and Waveforms



† PRR = 1 MHz, 50% Duty Cycle, t_r < 6 ns, t_f < 6 ns, Z_O = 50 Ω
‡ Includes probe and jig capacitance
§ 3 V if testing Y output, 0 V if testing Z output

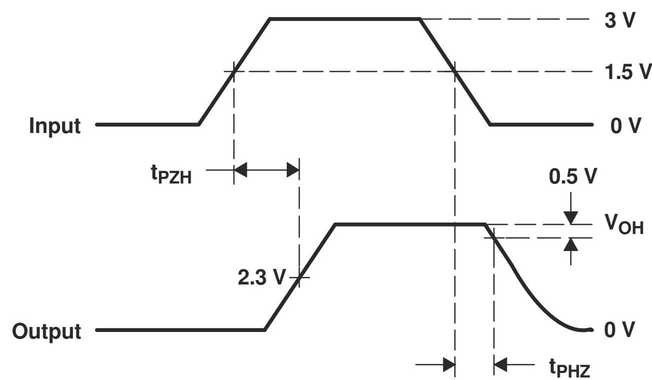


图 6-5. Enable Timing Test Circuit and Waveforms, t_{PZH} and t_{PHZ}

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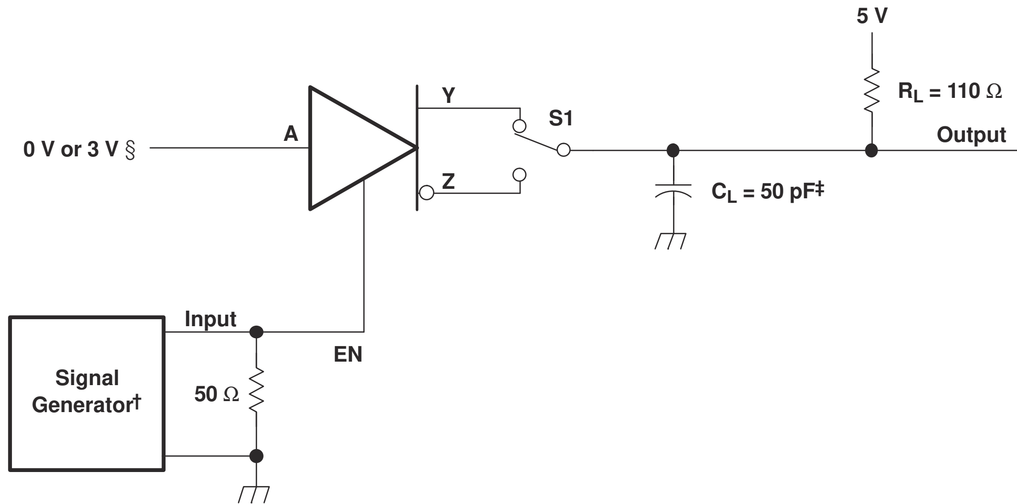

† PRR = 1 MHz, 50% Duty Cycle, t_r < 6 ns, t_f < 6 ns, Z_O = 50 Ω
‡ Includes probe and jig capacitance
§ 3 V if testing Y output, 0 V if testing Z output

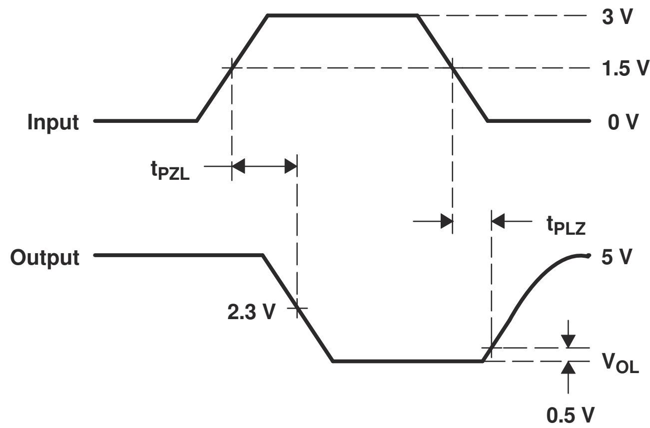

图 6-6. Enable Timing Test Circuit and Waveforms, t_{PZL} and t_{PLZ}

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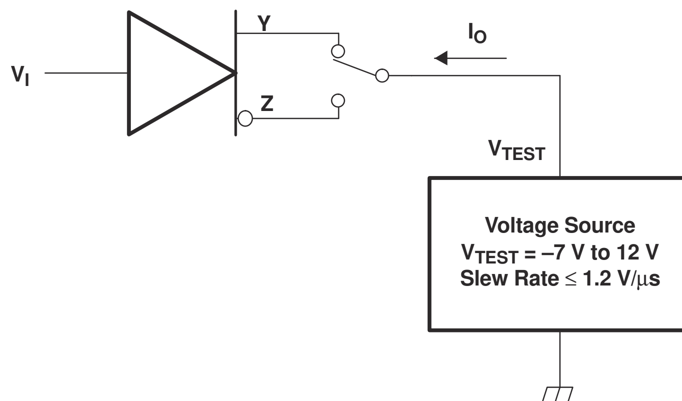

图 6-7. Test Circuit, Short-Circuit Output Current

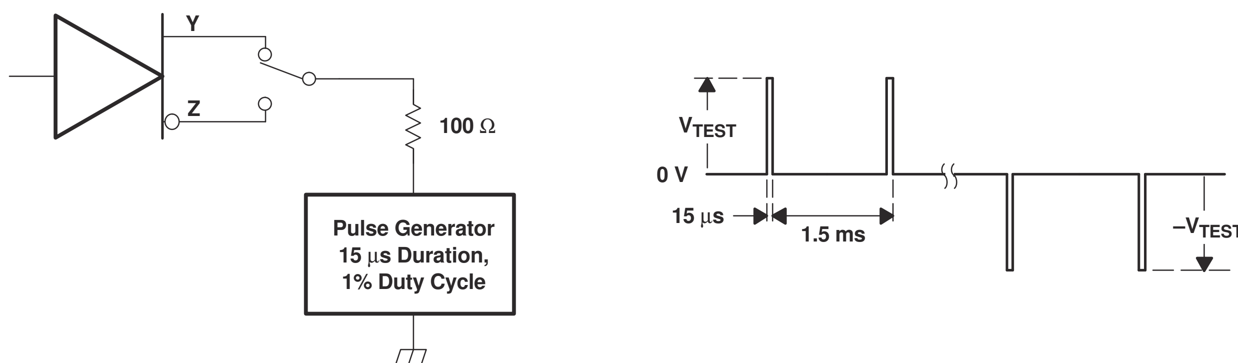

图 6-8. Test Circuit Waveform, Transient Overvoltage Test

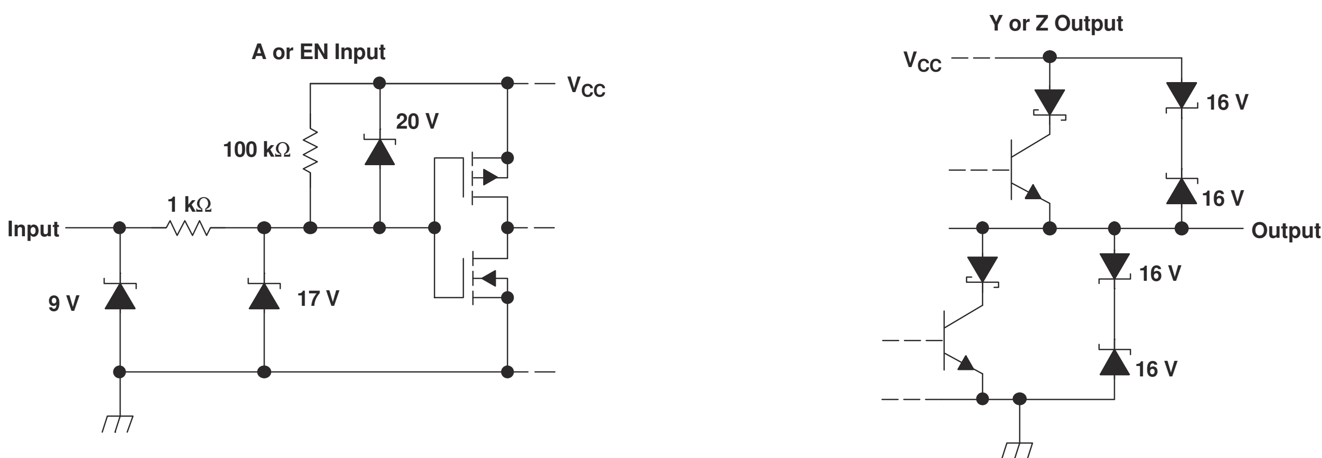

图 6-9. Equivalent Input and Output Schematic Diagrams

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7 Device Functional Modes

表 7-1. Function table (each driver)

INPUT[1]	ENABLE	OUTPUT	OUTPUT
A	**EN**	**Y**	**Z**
L	H	L	H
H	H	H	L
OPEN	H	H	L
L	OPEN	L	H
H	OPEN	H	L
OPEN	OPEN	H	L
X	L	Z	Z

(1) H = high level, L = low level, X = irrelevant, Z = high impedance (off)

8 Application and Implementation

备注

以下应用部分中的信息不属于 TI 器件规格的范围，TI 不担保其准确性和完整性。TI 的客 户应负责确定器件是否适用于其应用。客户应验证并测试其设计，以确保系统功能。

8.1 Application Information

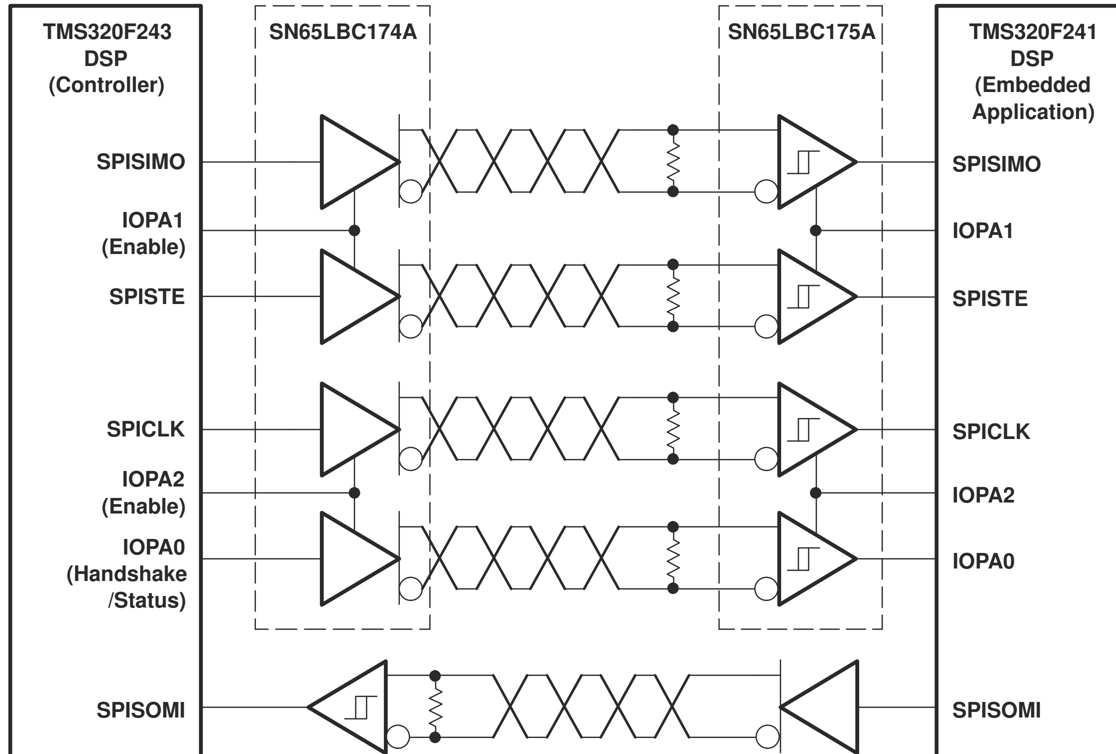

图 8-1. Typical Application Circuit, DSP-to-DSP Link via Serial Peripheral Interface

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9 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

9.1 接收文档更新通知

要接收文档更新通知，请导航至 ti.com 上的器件产品文件夹。点击*通知* 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

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TI E2E™ 中文支持论坛是工程师的重要参考资料，可直接从专家处获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题，获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的使用条款。

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9.4 静电放电警告

静电放电 (ESD) 会损坏这个集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

9.5 术语表

TI 术语表　　本术语表列出并解释了术语、首字母缩略词和定义。

10 Revision History

注：以前版本的页码可能与当前版本的页码不同

Changes from Revision F (October 2009) to Revision G (April 2024) — **Page**

- 更改了整个文档中的表格、图和交叉参考的编号格式 1
- Added the *Thermal Information* table 5

Changes from Revision E (July 2008) to Revision F (October 2009) — **Page**

- Added C_{IN} - Input Capacitance to the Electrical Characteristics table 6
- Changed the location of 图 6-9 8
- Changed 表 7-1 header From: ENABLE G To: ENABLE EN 13

Changes from Revision D (June 2008) to Revision E (July 2008) — **Page**

- 将“特性”要点从“输出 ESD 保护超过 11 kV”更改为“输出 ESD 保护：12kV” 1
- Changed Electrostatic discharge-Human body model-Y, Z, and GND From: 11kV To: 12kV 4
- From: A, G, $\overline{G}$ To: A, EN 6

Changes from Revision C (June 2008) to Revision D (July 2008) | **Page**

- Changed Electrostatic discharge-Human body model-Y, Z, and GND From: 13kV To: 11kV.............................4
- Changed the *Dissipation Rating Table* 4

Changes from Revision B (June 2001) to Revision C (May 2003) | **Page**

- 将“特性”要点从“输出 ESD 保护超过 13kV”更改为“输出 ESD 保护：11kV” 1
- 将业界通用的“特性”要点从“与 SN75174、MC3487 和 DS96174 兼容”更改为“与 SN75174、MC3487、DS96174、LTC487 和 MAX3042 兼容” 1

Changes from Revision A (February 2001) to Revision B (June 2001) | **Page**

- Changed DW Package appearance...3
- Added 图 5-5 7

Changes from Revision * (October 2000) to Revision A (February 2001) | **Page**

- 更改了整个数据表中的多个项目...1

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN65LBC174A16DW	OBSOLETE	SOIC	DW	16		TBD	Call TI	Call TI	-40 to 85	65LBC174A	
SN65LBC174A16DWR	ACTIVE	SOIC	DW	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	65LBC174A	Samples
SN65LBC174A16DWRG4	ACTIVE	SOIC	DW	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	65LBC174A	Samples
SN65LBC174ADW	OBSOLETE	SOIC	DW	20		TBD	Call TI	Call TI	-40 to 85	65LBC174A	
SN65LBC174ADWR	ACTIVE	SOIC	DW	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	65LBC174A	Samples
SN65LBC174AN	ACTIVE	PDIP	N	16	25	RoHS & Green	NIPDAU	N / A for Pkg Type	-40 to 85	65LBC174A	Samples
SN75LBC174A16DW	OBSOLETE	SOIC	DW	16		TBD	Call TI	Call TI	0 to 70	75LBC174A	
SN75LBC174A16DWR	OBSOLETE	SOIC	DW	16		TBD	Call TI	Call TI	0 to 70	75LBC174A	
SN75LBC174ADW	ACTIVE	SOIC	DW	20	25	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	75LBC174A	Samples
SN75LBC174ADWR	ACTIVE	SOIC	DW	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	75LBC174A	Samples
SN75LBC174AN	OBSOLETE	PDIP	N	16		TBD	Call TI	Call TI	0 to 70	75LBC174A	

[1] The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

[2] **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

[3] MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

[4] There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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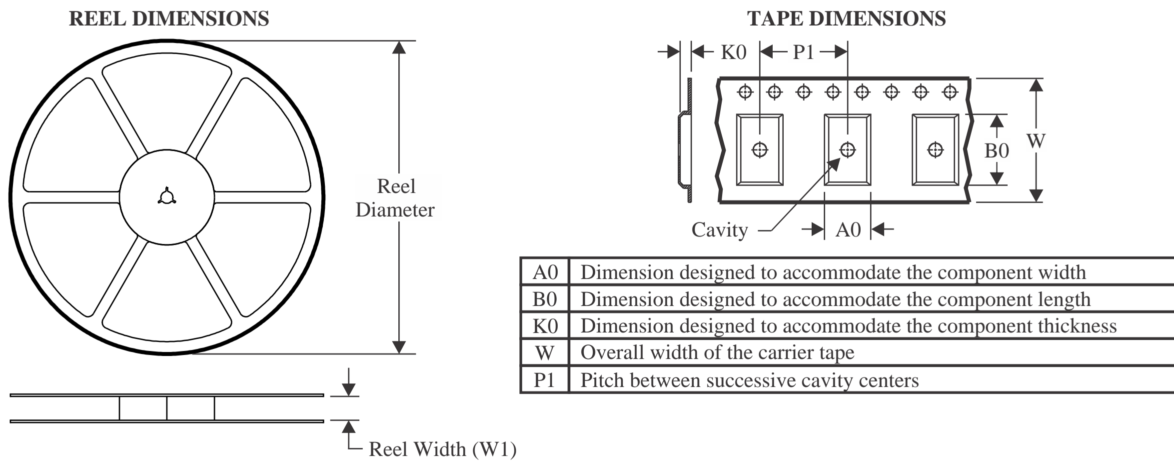
OTHER QUALIFIED VERSIONS OF SN65LBC174A :

- Enhanced Product : SN65LBC174A-EP

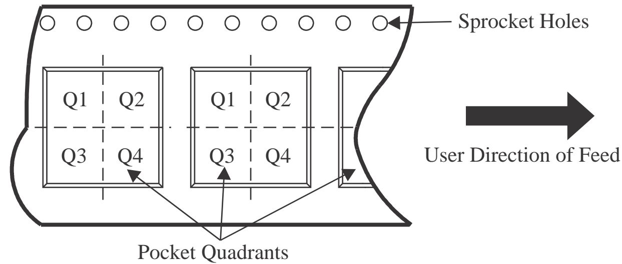
NOTE: Qualified Version Definitions:

- Enhanced Product - Supports Defense, Aerospace and Medical Applications

TAPE AND REEL INFORMATION



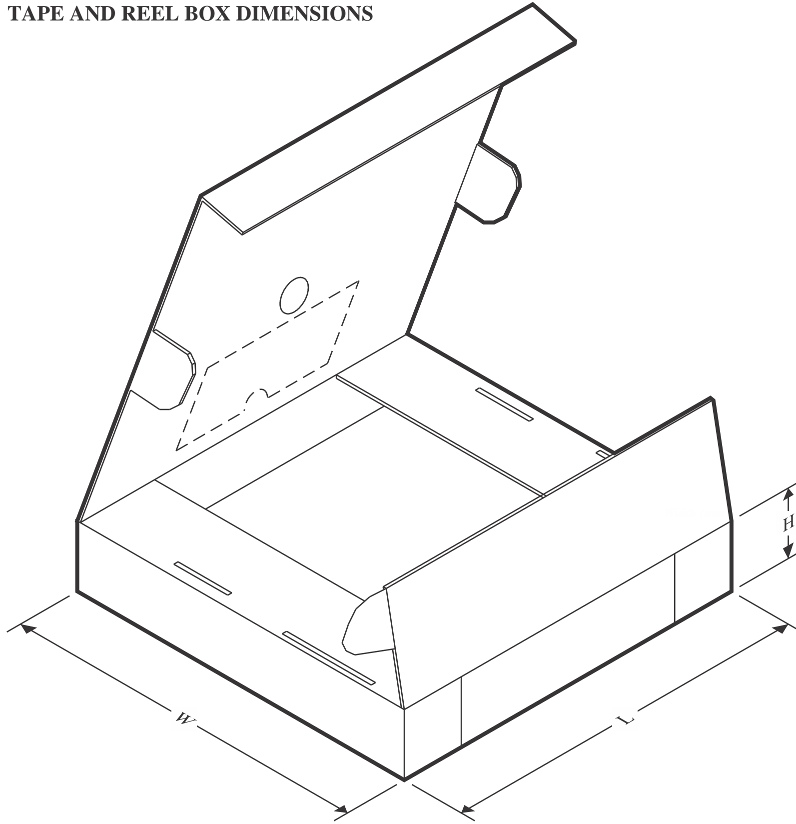
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN65LBC174A16DWR	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1
SN65LBC174ADWR	SOIC	DW	20	2000	330.0	24.4	10.8	13.3	2.7	12.0	24.0	Q1
SN65LBC174ADWR	SOIC	DW	20	2000	330.0	24.4	10.8	13.3	2.7	12.0	24.0	Q1
SN75LBC174ADWR	SOIC	DW	20	2000	330.0	24.4	10.8	13.3	2.7	12.0	24.0	Q1

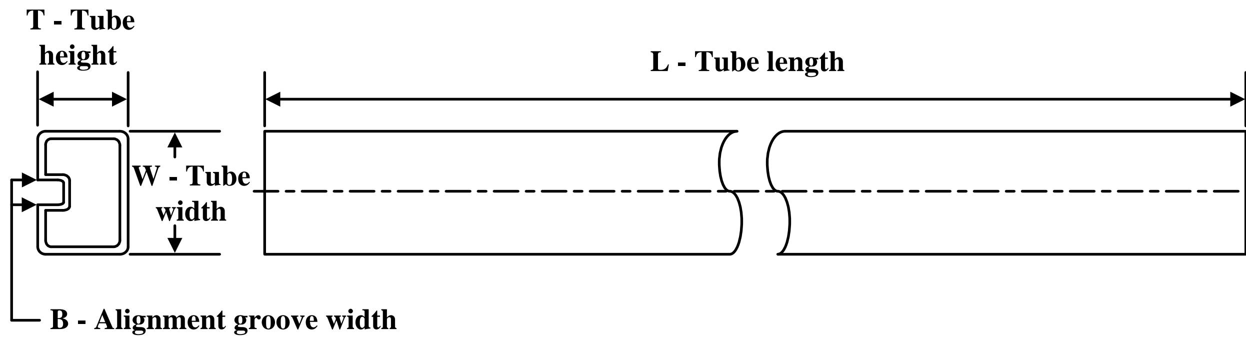
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN65LBC174A16DWR	SOIC	DW	16	2000	350.0	350.0	43.0
SN65LBC174ADWR	SOIC	DW	20	2000	367.0	367.0	45.0
SN65LBC174ADWR	SOIC	DW	20	2000	356.0	356.0	45.0
SN75LBC174ADWR	SOIC	DW	20	2000	350.0	350.0	43.0

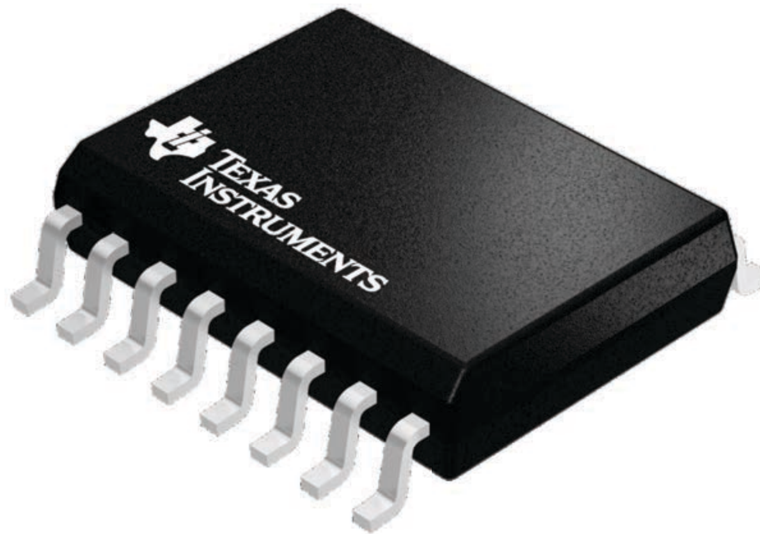
TUBE

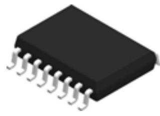


*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
SN65LBC174AN	N	PDIP	16	25	506	13.97	11230	4.32
SN75LBC174ADW	DW	SOIC	20	25	507	12.83	5080	6.6
SN75LBC174ADW	DW	SOIC	20	25	506.98	12.7	4826	6.6

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.





PACKAGE OUTLINE

DW0016A

SOIC - 2.65 mm max height

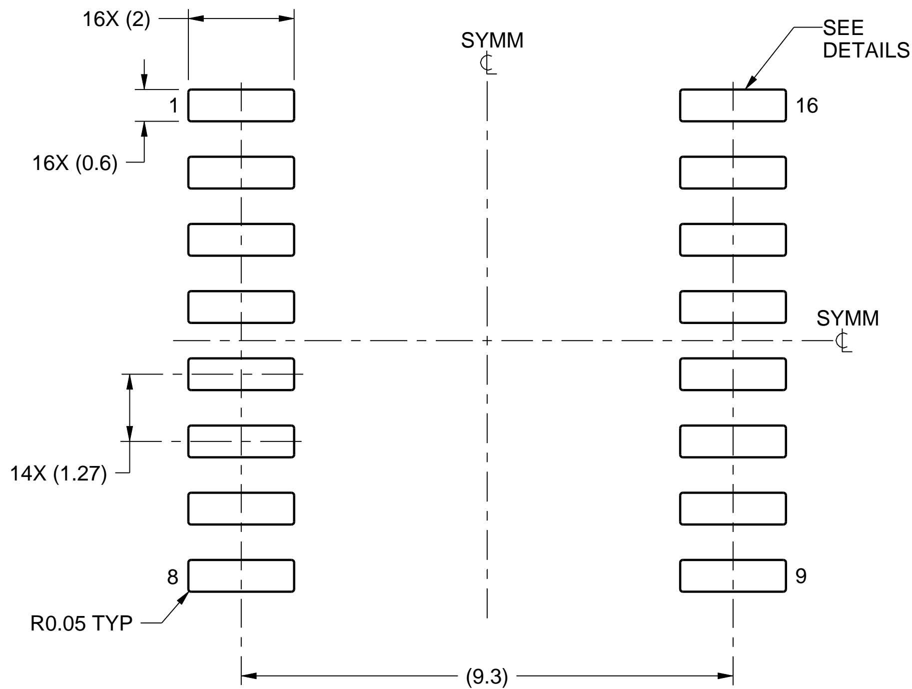
SOIC

C
SEATING PLANE
0.1 C
10.63
9.97 TYP
PIN 1 ID
AREA
A
14X 1.27
16
1
10.5
10.1
NOTE 3
2X
8.89
8
9
16X 0.51
0.31
0.25 Ⓜ C A B
B
7.6
7.4
NOTE 4
2.65 MAX
0.33
0.10 TYP
SEE DETAIL A
0.25
GAGE PLANE
0° - 8°
0.3
0.1
1.27
0.40
(1.4)
DETAIL A
TYPICAL

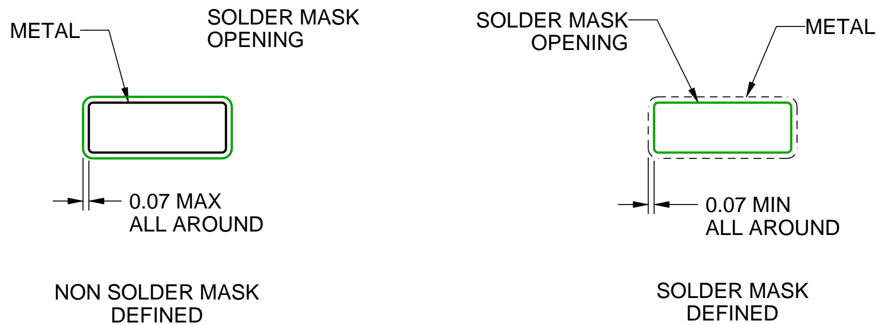
4220721/A 07/2016

NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.
5. Reference JEDEC registration MS-013.



LAND PATTERN EXAMPLE
SCALE:7X

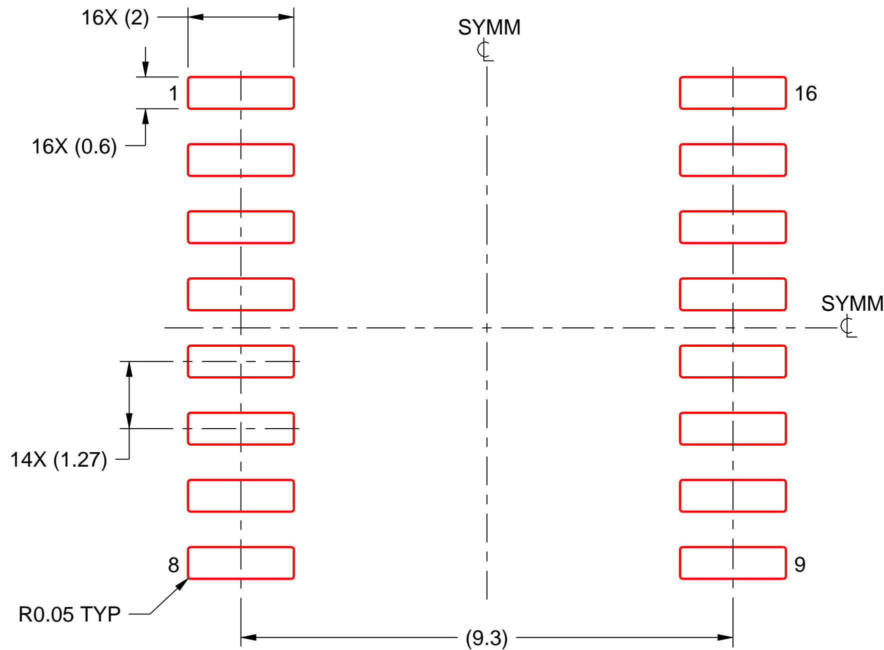


SOLDER MASK DETAILS

4220721/A 07/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:7X

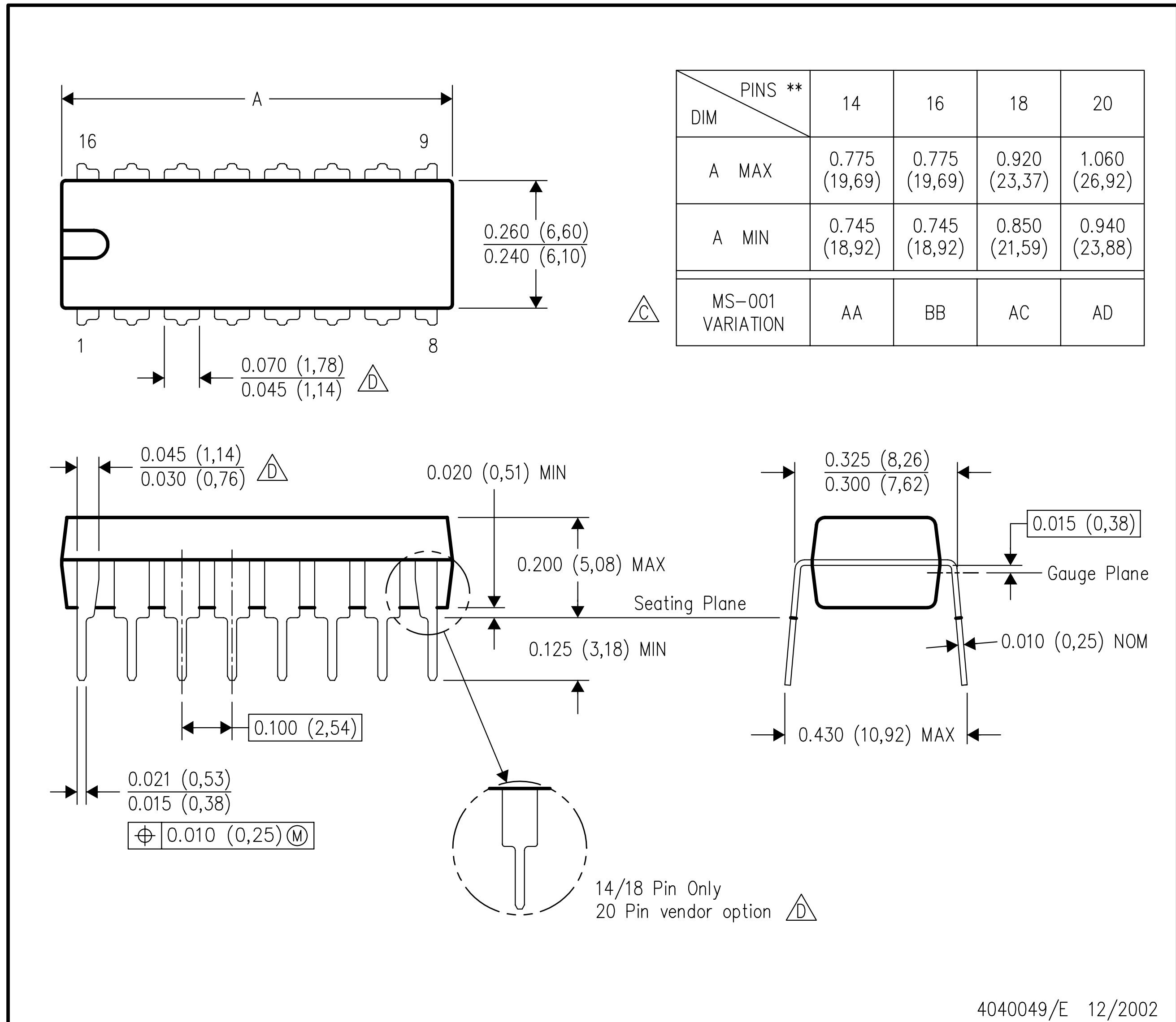
4220721/A 07/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

N (R–PDIP–T**) PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN

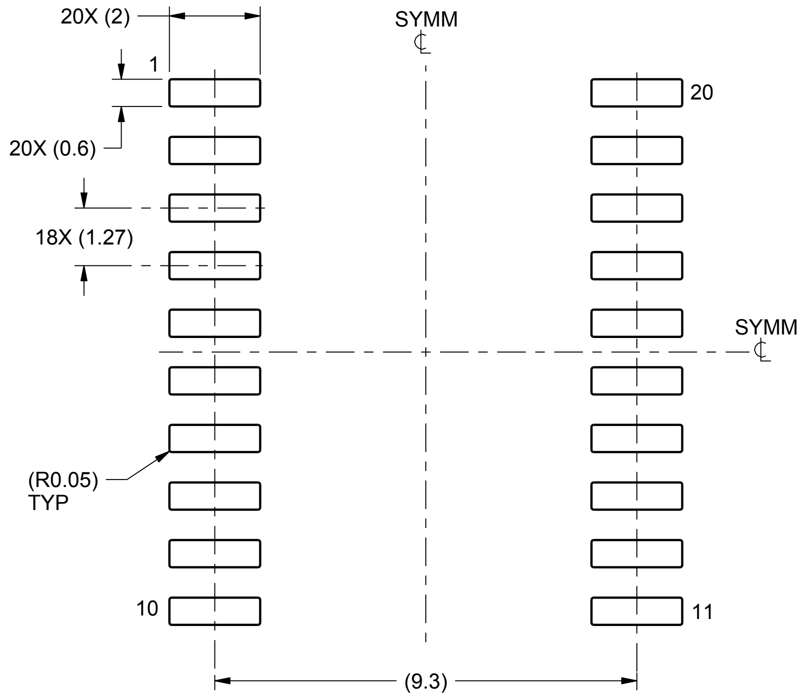


DIM \ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS–001 VARIATION	AA	BB	AC	AD

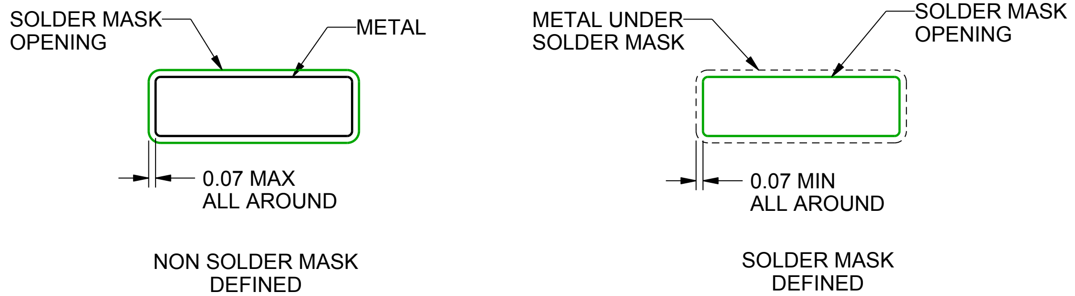
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm per side.
5. Reference JEDEC registration MS-013.



LAND PATTERN EXAMPLE
SCALE:6X



NON SOLDER MASK DEFINED

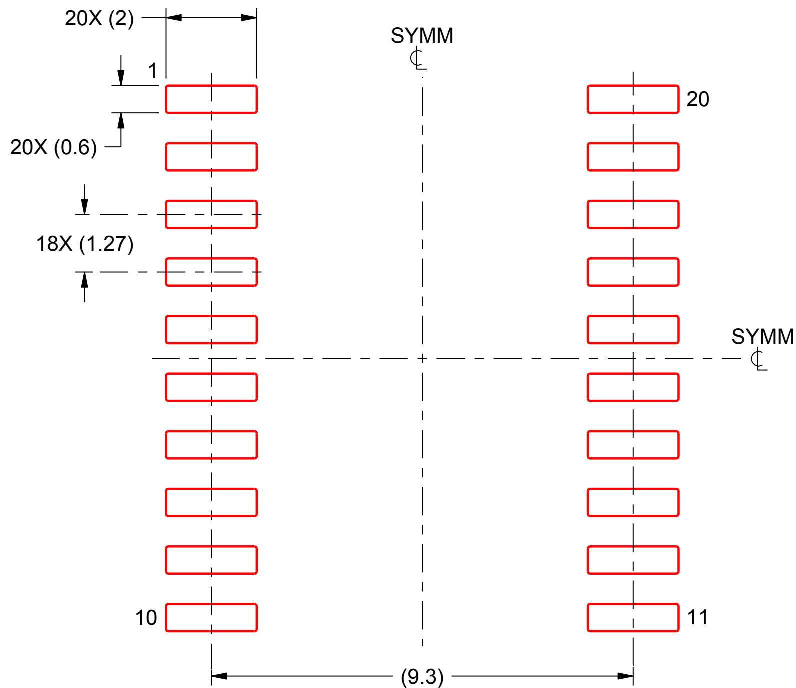
SOLDER MASK DEFINED

SOLDER MASK DETAILS

4220724/A 05/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

4220724/A 05/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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