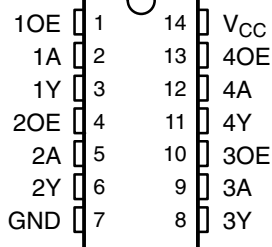


SN54ABT126, SN74ABT126 QUADRUPLE BUS BUFFER GATES WITH 3-STATE OUTPUTS

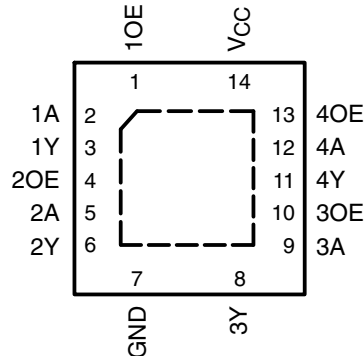
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- Typical V_{OLP} (Output Ground Bounce) <1 V at $V_{CC} = 5$ V, $T_A = 25^\circ\text{C}$
- High-Impedance State During Power Up and Power Down
- High-Drive Outputs ($-32\text{-mA } I_{OH}$, $64\text{-mA } I_{OL}$)
- I_{off} and Power-Up 3-State Support Hot Insertion
- Latch-Up Performance Exceeds 500 mA Per JESD 17
- ESD Protection Exceeds JESD 22
 - 2000-V Human-Body Model (A114-A)
 - 200-V Machine Model (A115-A)

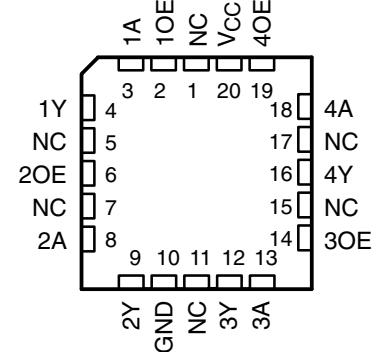
SN54ABT126 ... J PACKAGE
SN74ABT126 ... D, DB, N, NS,
OR PW PACKAGE
(TOP VIEW)



SN74ABT126 ... RGY PACKAGE
(TOP VIEW)



SN54ABT126 ... FK PACKAGE
(TOP VIEW)



NC – No internal connection

description/ordering information

The 'ABT126 bus buffer gates feature independent line drivers with 3-state outputs. Each output is disabled when the associated output-enable (OE) input is low.

When V_{CC} is between 0 and 2.1 V, the device is in the high-impedance state during power up or power down. However, to ensure the high-impedance state above 2.1 V, OE should be tied to GND through a pull-down resistor; the minimum value of the resistor is determined by the current-sourcing capability of the driver.

ORDERING INFORMATION

T_A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
-40°C to 85°C	QFN – RGY	Tape and reel	SN74ABT126RGYR	AB126
	PDIP – N	Tube	SN74ABT126N	SN74ABT126N
	SOIC – D	Tube	SN74ABT126D	ABT126
		Tape and reel	SN74ABT126DR	
	SOP – NS	Tape and reel	SN74ABT126NSR	ABT126
	SSOP – DB	Tape and reel	SN74ABT126DBR	AB126
	TSSOP – PW	Tube	SN74ABT126PW	AB126
		Tape and reel	SN74ABT126PWR	
-55°C to 125°C	CDIP – J	Tube	SNJ54ABT126J	SNJ54ABT126J
	LCCC – FK	Tube	SNJ54ABT126FK	SNJ54ABT126FK

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

UNLESS OTHERWISE NOTED this document contains PRODUCTION DATA information current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

 **TEXAS
INSTRUMENTS**

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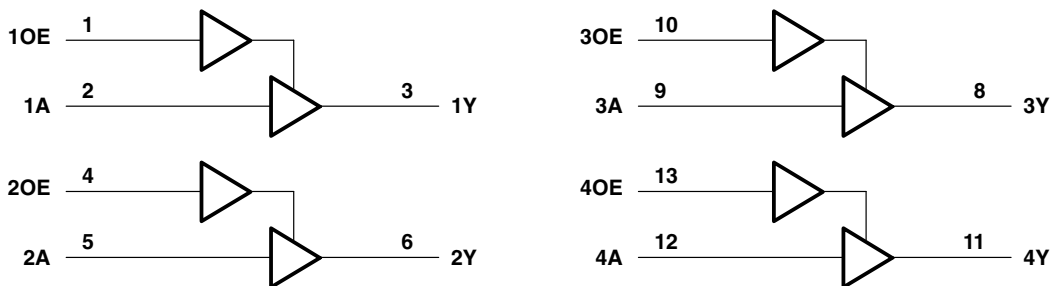
SN54ABT126, SN74ABT126 QUADRUPLE BUS BUFFER GATES WITH 3-STATE OUTPUTS

SCBS183H – FEBRUARY 1991 – REVISED MAY 2003

FUNCTION TABLE
(each buffer)

INPUTS		OUTPUT
OE	A	Y
H	H	H
H	L	L
L	X	Z

logic diagram (positive logic)



Pin numbers shown are for the D, DB, J, N, NS, PW, and RGY packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage range, V_{CC}	–0.5 V to 7 V
Input voltage range, V_I (see Note 1)	–0.5 V to 7 V
Voltage range applied to any output in the high or power-off state, V_O	–0.5 V to 5.5 V
Current into any output in the low state, I_O : SN54ABT126	96 mA
SN74ABT126	128 mA
Input clamp current, I_{IK} ($V_I < 0$)	–18 mA
Output clamp current, I_{OK} ($V_O < 0$)	–50 mA
Package thermal impedance, θ_{JA} (see Note 2): D package	86°C/W
(see Note 2): DB package	96°C/W
(see Note 2): N package	80°C/W
(see Note 2): NS package	76°C/W
(see Note 2): PW package	113°C/W
(see Note 3): RGY package	47°C/W
Storage temperature range, T_{stg}	–65°C to 150°C

[†] Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. The package thermal impedance is calculated in accordance with JESD 51-7.
3. The package thermal impedance is calculated in accordance with JESD 51-5.

SN54ABT126, SN74ABT126 QUADRUPLE BUS BUFFER GATES WITH 3-STATE OUTPUTS

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recommended operating conditions (see Note 4)

		SN54ABT126		SN74ABT126		UNIT
		MIN	MAX	MIN	MAX	
V _{CC}	Supply voltage	4.5	5.5	4.5	5.5	V
V _{IH}	High-level input voltage	2		2		V
V _{IL}	Low-level input voltage		0.8		0.8	V
V _I	Input voltage	0	V _{CC}	0	V _{CC}	V
I _{OH}	High-level output current		-24		-32	mA
I _{OL}	Low-level output current		48		64	mA
Δt/Δv	Input transition rise or fall rate		10		10	ns/V
Δt/ΔV _{CC}	Power-up ramp rate	200		200		μs/V
T _A	Operating free-air temperature	-55	125	-40	85	°C

NOTE 4: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	T _A = 25°C			SN54ABT126		SN74ABT126		UNIT	
		MIN	TYP†	MAX	MIN	MAX	MIN	MAX		
V _{IK}	V _{CC} = 4.5 V, I _I = -18 mA			-1.2	-1.2			-1.2	V	
V _{OH}	V _{CC} = 4.5 V, I _{OH} = -3 mA	2.5			2.5			2.5	V	
	V _{CC} = 5 V, I _{OH} = -3 mA	3			3			3		
	V _{CC} = 4.5 V	I _{OH} = -24 mA	2			2				
I _{OH} = -32 mA		2*						2		
V _{OL}	V _{CC} = 4.5 V	I _{OL} = 48 mA		0.55		0.55			V	
		I _{OL} = 64 mA		0.55*			0.55			
V _{hys}			100						mV	
I _I	V _{CC} = 0 to 5.5 V, V _I = V _{CC} or GND			±1		±1		±1	μA	
I _{OZPU}	V _{CC} = 0 to 2.1 V, V _O = 0.5 V to 2.7 V, OE = X [‡]			±50		±50		±50	μA	
I _{OZPD}	V _{CC} = 2.1 V to 0, V _O = 0.5 V to 2.7 V, OE = X [‡]			±50		±50		±50	μA	
I _{OZH}	V _{CC} = 2.1 V to 5.5 V, V _O = 2.7 V, OE ≤ 0.8 V			10		10		10	μA	
I _{OZL}	V _{CC} = 2.1 V to 5.5 V, V _O = 0.5 V, OE ≤ 0.8 V			-10		-10		-10	μA	
I _{off}	V _{CC} = 0, V _I or V _O ≤ 4.5 V			±100				±100	μA	
I _{CEX}	V _{CC} = 5.5 V, V _O = 5.5 V			50		50		50	μA	
I _O [§]	V _{CC} = 5.5 V, V _O = 2.5 V	-50	-100	-200	-50	-200	-50	-200	mA	
I _{CC}	V _{CC} = 5.5 V, I _O = 0, V _I = V _{CC} or GND	Outputs high	1	250		250		250	μA	
		Outputs low		24	30		30		30	mA
		Outputs disabled		0.5	250		250		250	μA
ΔI _{CC} [¶]	V _{CC} = 5.5 V, One input at 3.4 V, Other inputs at V _{CC} or GND	Outputs enabled		1.5		1.5		1.5	mA	
		Outputs disabled			50		50		50	μA
C _i	V _I = 2.5 V or 0.5 V			3					pF	
C _o	V _O = 2.5 V or 0.5 V			7					pF	

* On products compliant to MIL-PRF-38535, this parameter does not apply.

† All typical values are at V_{CC} = 5 V.

‡ For V_{CC} between 2.1 V and 4 V, OE should be less than or equal to 0.5 V to ensure a low state.

§ Not more than one output should be tested at a time, and the duration of the test should not exceed one second.

¶ This is the increase in supply current for each input that is at the specified TTL voltage level, rather than V_{CC} or GND.

PRODUCT PREVIEW information concerns products in the formative or design phase of development. Characteristic data and other specifications are design goals. Texas Instruments reserves the right to change or discontinue these products without notice.



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SN54ABT126, SN74ABT126
QUADRUPLE BUS BUFFER GATES
WITH 3-STATE OUTPUTS

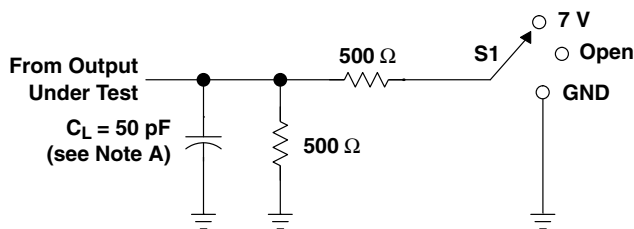
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switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Note 5 and Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 5\text{ V},$ $T_A = 25^\circ\text{C}$			SN54ABT126		SN74ABT126		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A	Y	1	2.9	4.9	1	7.3	1	6.3	ns
t_{PHL}			1	2.5	5.1	1	5.9	1	5.7	
t_{PZH}	OE	Y	1	4.4	5.8	1	5.3	1	6.5	ns
t_{PZL}			1	4.4	5.9	1	6.4	1	6.5	
t_{PHZ}	OE	Y	1	3	5.7	1	6.9	1	6.8	ns
t_{PLZ}			1	3	5.8	1	7.2	1	6.7	

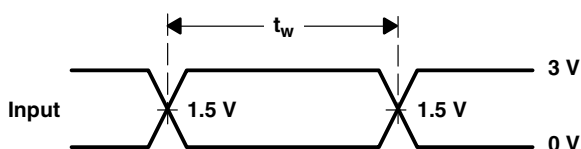
NOTE 5: Limits may vary among suppliers.

PARAMETER MEASUREMENT INFORMATION

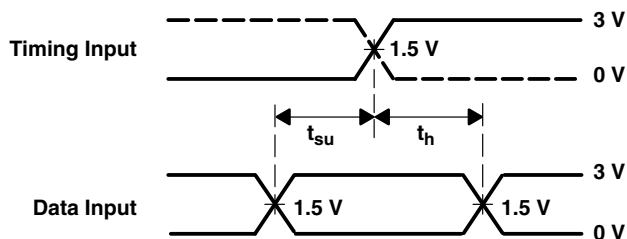


LOAD CIRCUIT

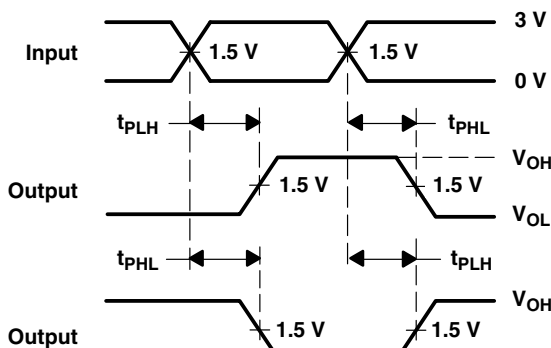
TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	7 V
t_{PHZ}/t_{PZH}	Open



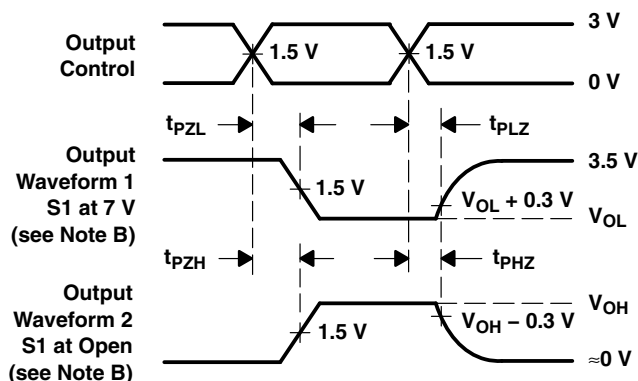
VOLTAGE WAVEFORMS
 PULSE DURATION



VOLTAGE WAVEFORMS
 SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
 PROPAGATION DELAY TIMES
 INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS
 ENABLE AND DISABLE TIMES
 LOW- AND HIGH-LEVEL ENABLING

- NOTES: A. C_L includes probe and jig capacitance.
 B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10$ MHz, $Z_O = 50 \Omega$, $t_r \leq 2.5$ ns, $t_f \leq 2.5$ ns.
 D. The outputs are measured one at a time with one transition per measurement.
 E. All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74ABT126D	ACTIVE	SOIC	D	14	50	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ABT126	Samples
SN74ABT126DBR	ACTIVE	SSOP	DB	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AB126	Samples
SN74ABT126DR	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ABT126	Samples
SN74ABT126N	ACTIVE	PDIP	N	14	25	RoHS & Green	NIPDAU	N / A for Pkg Type	-40 to 85	SN74ABT126N	Samples
SN74ABT126NSR	ACTIVE	SOP	NS	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ABT126	Samples
SN74ABT126PW	ACTIVE	TSSOP	PW	14	90	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AB126	Samples
SN74ABT126PWR	ACTIVE	TSSOP	PW	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AB126	Samples
SN74ABT126RGYR	ACTIVE	VQFN	RGY	14	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	AB126	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

⁽⁶⁾ Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74ABT126DBR	SSOP	DB	14	2000	330.0	16.4	8.35	6.6	2.4	12.0	16.0	Q1
SN74ABT126DR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
SN74ABT126NSR	SOP	NS	14	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1
SN74ABT126PWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74ABT126RGYR	VQFN	RGY	14	3000	330.0	12.4	3.75	3.75	1.15	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74ABT126DBR	SSOP	DB	14	2000	356.0	356.0	35.0
SN74ABT126DR	SOIC	D	14	2500	356.0	356.0	35.0
SN74ABT126NSR	SOP	NS	14	2000	356.0	356.0	35.0
SN74ABT126PWR	TSSOP	PW	14	2000	356.0	356.0	35.0
SN74ABT126RGYR	VQFN	RGY	14	3000	356.0	356.0	35.0

TUBE


*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
SN74ABT126D	D	SOIC	14	50	506.6	8	3940	4.32
SN74ABT126N	N	PDIP	14	25	506	13.97	11230	4.32
SN74ABT126N	N	PDIP	14	25	506	13.97	11230	4.32
SN74ABT126PW	PW	TSSOP	14	90	530	10.2	3600	3.5

DB0014A



PACKAGE OUTLINE

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-150.

EXAMPLE BOARD LAYOUT

DB0014A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



4220762/A 05/2024

NOTES: (continued)

- 5. Publication IPC-7351 may have alternate designs.
- 6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DB0014A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220762/A 05/2024

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

N (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
 - The 20 pin end lead shoulder width is a vendor option, either half or full width.

PW0014A



PACKAGE OUTLINE
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



4220202/B 12/2023

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

EXAMPLE BOARD LAYOUT

PW0014A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



4220202/B 12/2023

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

PW0014A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220202/B 12/2023

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

GENERIC PACKAGE VIEW

RGY 14

VQFN - 1 mm max height

3.5 x 3.5, 0.5 mm pitch

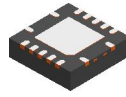
PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4231541/A

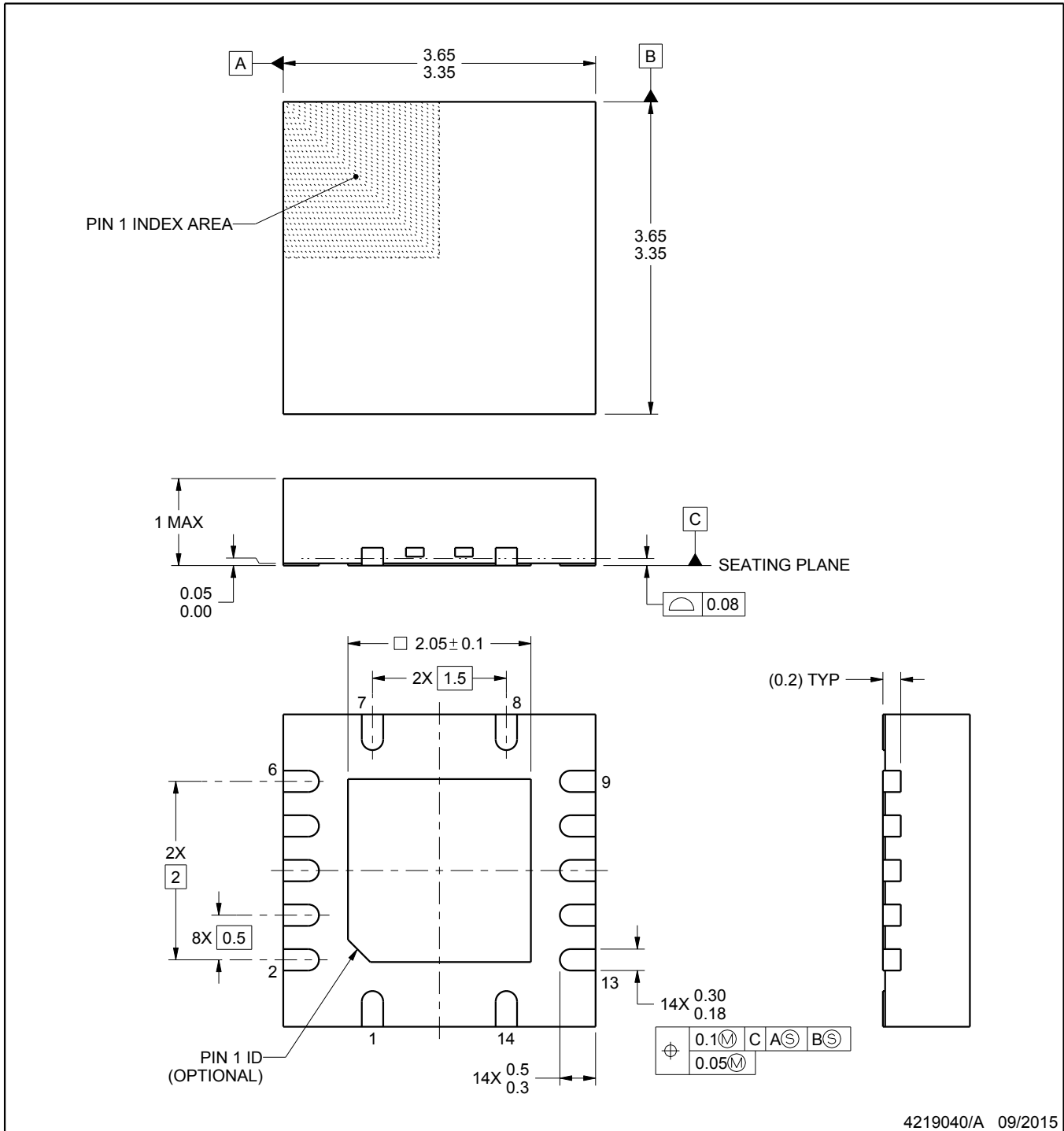
RGY0014A



PACKAGE OUTLINE

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



4219040/A 09/2015

NOTES:

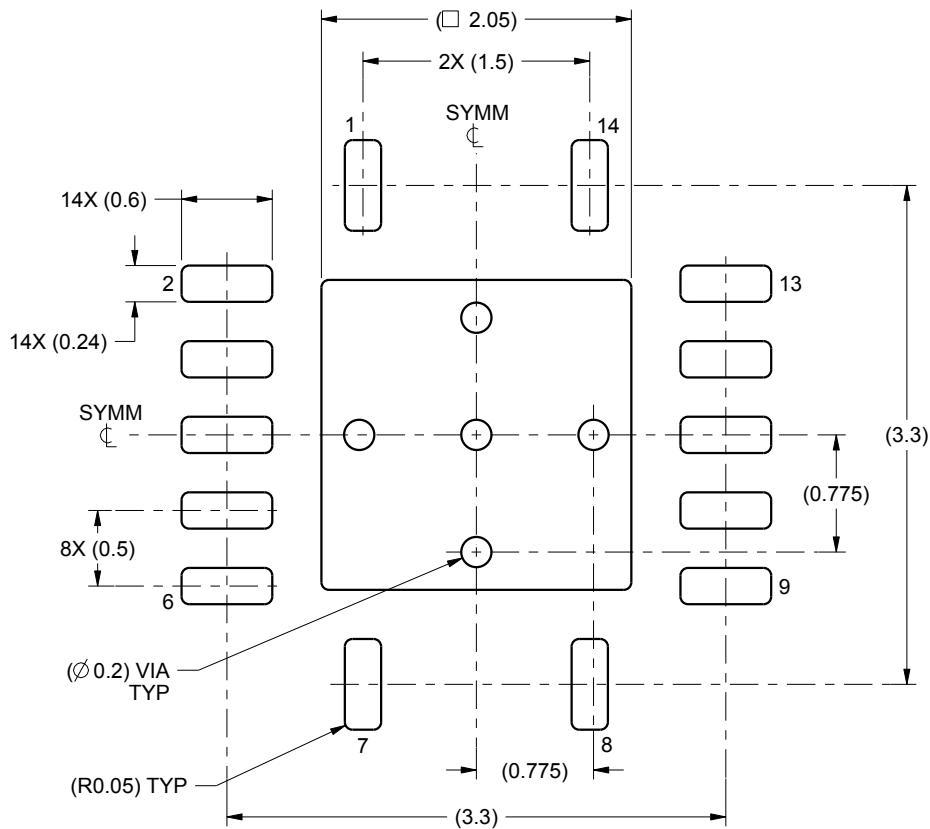
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

EXAMPLE BOARD LAYOUT

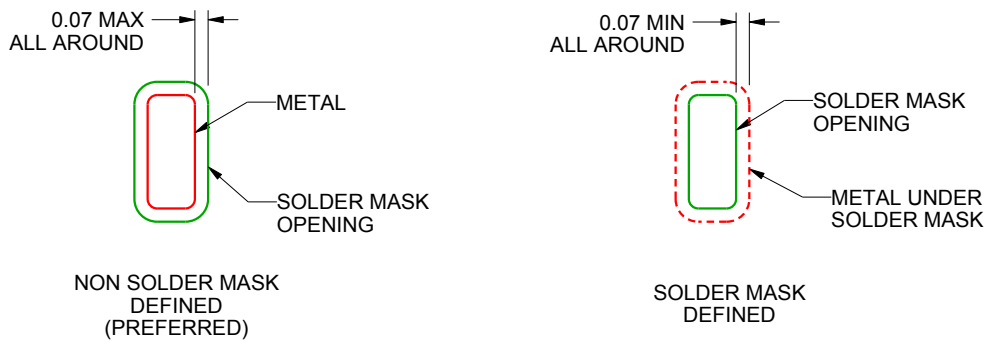
RGY0014A

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



LAND PATTERN EXAMPLE
SCALE:20X



SOLDER MASK DETAILS

4219040/A 09/2015

NOTES: (continued)

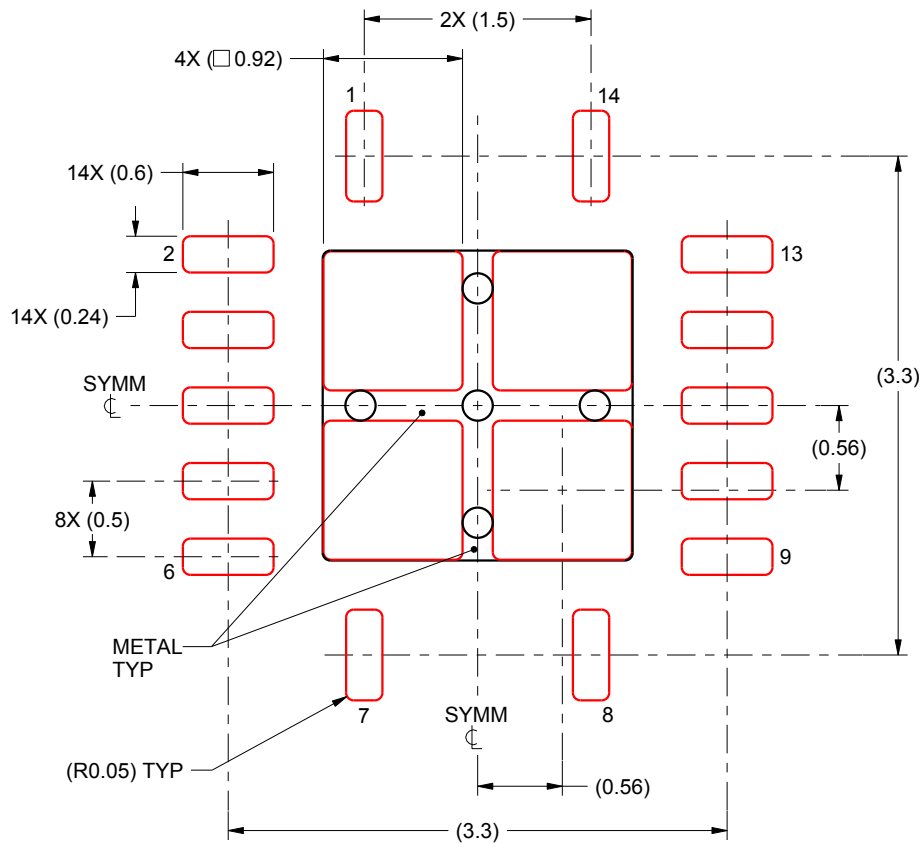
4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).

EXAMPLE STENCIL DESIGN

RGY0014A

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
80% PRINTED SOLDER COVERAGE BY AREA
SCALE:20X

4219040/A 09/2015

NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.



D0014A

PACKAGE OUTLINE

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



4220718/A 09/2016

NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm, per side.
5. Reference JEDEC registration MS-012, variation AB.

EXAMPLE BOARD LAYOUT

D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE
SCALE:8X



SOLDER MASK DETAILS

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NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:8X

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NOTES: (continued)

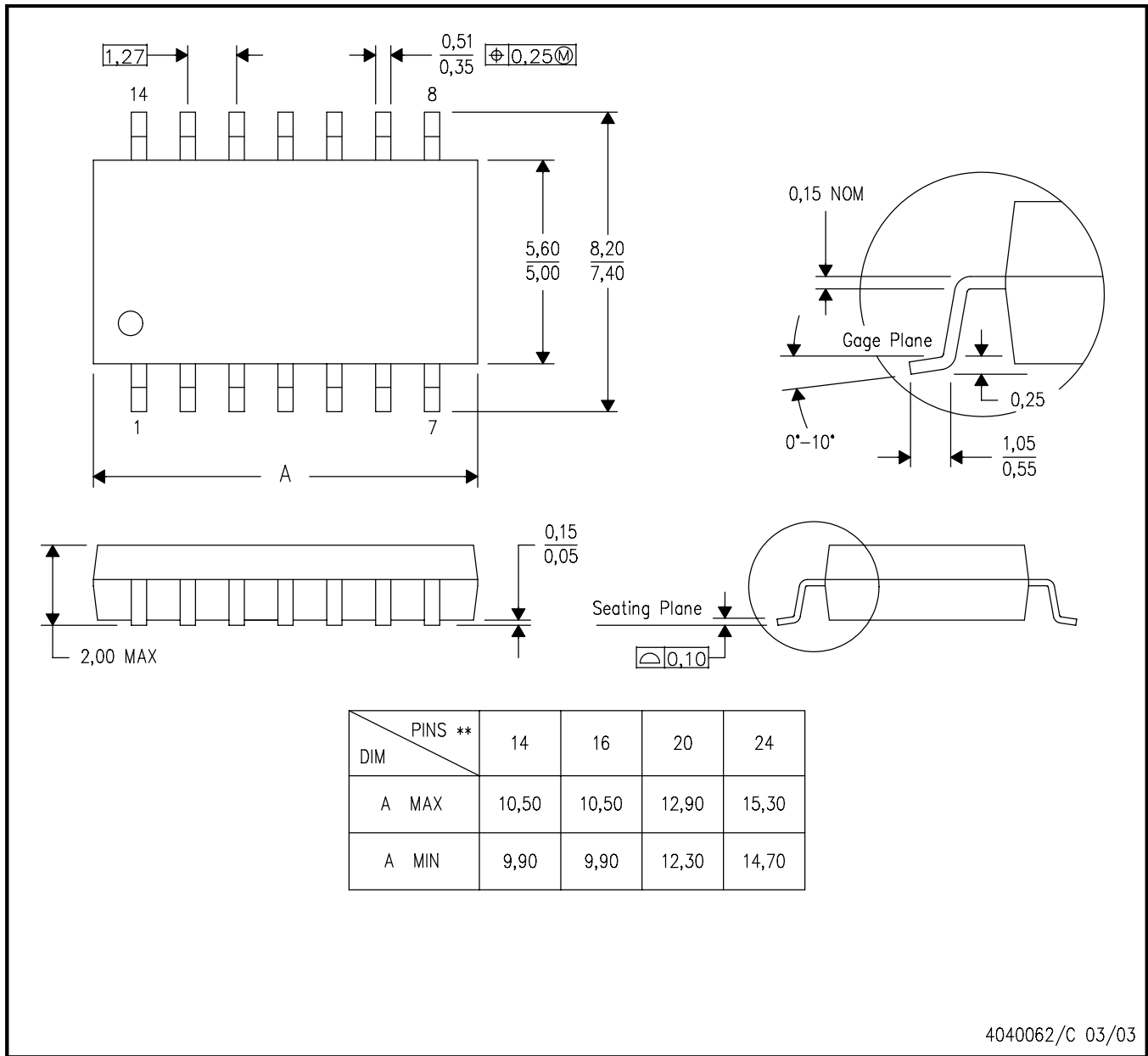
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

MECHANICAL DATA

NS (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

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