

SNx4AC240 具有三态输出的八路缓冲器/驱动器

1 特性

- V_{CC} 工作范围为 2V 至 6V
- 5V 时, t_{pd} 最大值为 6.5ns
- 输入电压高达 6V

2 应用

- 手持终端：智能手机
- 网络交换机
- 健康与健身/可穿戴设备

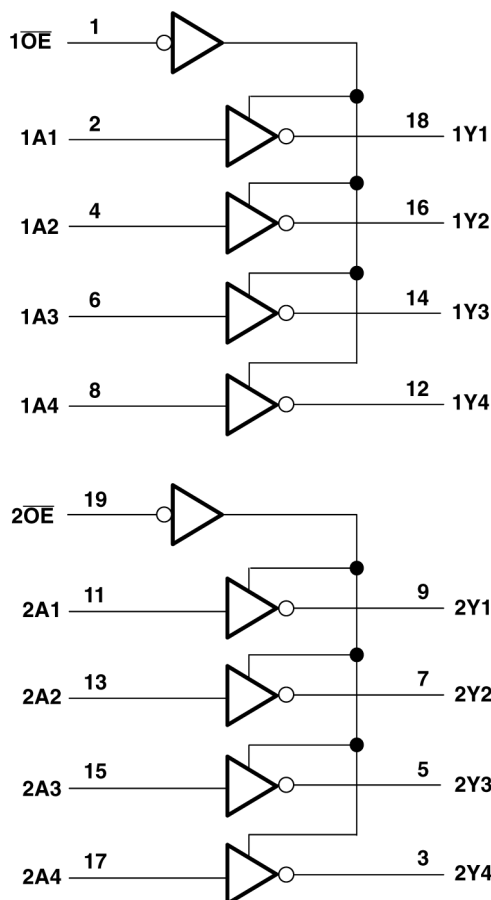
3 说明

这些八通道缓冲器和线路驱动器专门设计用于提高三态存储器地址驱动器、时钟驱动器以及总线用接收器和发送器的性能和密度。

封装信息

| 器件型号 | 封装 ⁽¹⁾ | 封装尺寸 ⁽²⁾ | 本体尺寸 ⁽³⁾ |
|-----------|-------------------|---------------------|---------------------|
| SN54AC240 | J (CDIP, 20) | 24.2mm x 7.62mm | 24.2mm x 6.92mm |
| | W (CFP, 20) | 13.09mm x 8.13mm | 13.09mm x 6.92mm |
| SN74AC240 | N (PDIP, 20) | 24.33mm x 9.4mm | 24.33mm x 6.35mm |
| | DW (SOIC, 20) | 12.8mm x 10.3mm | 12.8mm x 7.5mm |
| | NS (SOP, 20) | 12.6mm x 7.8mm | 12.6mm x 5.3mm |
| | DB (SSOP, 20) | 7.2mm x 7.8mm | 7.2mm x 5.3mm |
| | PW (TSSOP, 20) | 6.5mm x 6.4mm | 6.5mm x 4.4mm |

- (1) 有关更多信息, 请参阅第 11 节。
- (2) 封装尺寸 (长 × 宽) 为标称值, 并包括引脚 (如适用)。
- (3) 本体尺寸 (长 × 宽) 为标称值, 不包括引脚。



逻辑图 (正逻辑)



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4 Pin Configuration and Functions

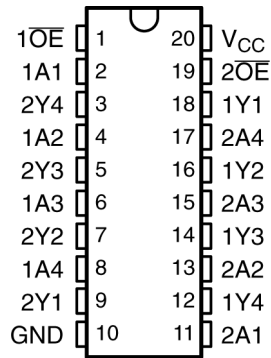


图 4-1. SN54AC240 J or W Package; SN74AC240 DB, DW, N, NS, or PW Package (Top View)

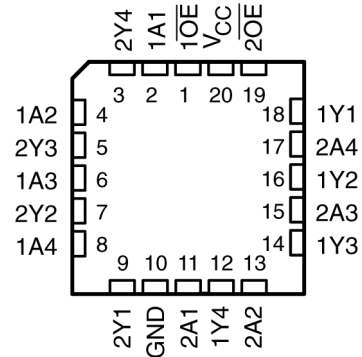


图 4-2. SN54AC240 FK Package (Top View)

表 4-1. Pin Functions

| NAME ⁽¹⁾ | PIN | TYPE | DESCRIPTION |
|---------------------|-----|------|-----------------|
| 1OE | 1 | I | Output enable 1 |
| 1A1 | 2 | I | 1A1 input |
| 2Y4 | 3 | O | 2Y4 output |
| 1A2 | 4 | I | 1A2 input |
| 2Y3 | 5 | O | 2Y3 output |
| 1A3 | 6 | I | 1A3 input |
| 2Y2 | 7 | O | 2Y2 output |
| 1A4 | 8 | I | 1A4 input |
| 2Y1 | 9 | O | 2Y1 output |
| GND | 10 | — | Ground pin |
| 2A1 | 11 | I | 2A1 input |
| 1Y4 | 12 | O | 1Y4 output |
| 2A2 | 13 | I | 2A2 input |
| 1Y3 | 14 | O | 1Y3 output |
| 2A3 | 15 | I | 2A3 input |
| 1Y2 | 16 | O | 1Y2 output |
| 2A4 | 17 | I | 2A4 input |
| 1Y1 | 18 | O | 1Y1 output |
| 2OE | 19 | I | Output enable 2 |
| VCC | 20 | — | Power pin |

(1) Signal Types: I = Input, O = Output, I/O = Input or Output

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

| | | MIN | MAX | UNIT |
|-----------------------------|---|-------|----------------------|------|
| V _{CC} | Supply voltage range | - 0.5 | 7 | V |
| V _I ² | Input voltage range | - 0.5 | V _{CC} +0.5 | V |
| V _O ² | Output voltage range | - 0.5 | V _{CC} +0.5 | V |
| I _{IK} | Input clamp current (V _I < 0 or V _I > V _{CC}) | | ±20 | mA |
| I _{OK} | Output clamp current (V _O < 0 or V _O > V _{CC}) | | ±20 | mA |
| I _O | Continuous output current (V _O = 0 or V _{CC}) | | ±50 | mA |
| | Continuous current through V _{CC} or GND | | ±200 | mA |
| T _{stg} | Storage temperature range | -65 | 150 | °C |

- (1) Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

5.2 ESD Ratings

| | | VALUE | UNIT |
|--------------------|-------------------------|--|-------|
| V _(ESD) | Electrostatic discharge | Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾ | ±2000 |
| | | Charged-device model (CDM), per JEDEC specification JESD22-C101 ⁽²⁾ | ±1000 |
| | | Machine model (A115-A) | ±200 |

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

over recommended operating free-air temperature range (unless otherwise noted)¹

| | | SN54AC240 | | SN74AC240 | | UNIT |
|-----------------|------------------------------------|-------------------------|-----------------|-----------|-----------------|------|
| | | MIN | MAX | MIN | MAX | |
| V _{CC} | Supply voltage | 2 | 6 | 2 | 6 | V |
| V _{IH} | High-level input voltage | V _{CC} = 3 V | 2.1 | 2.1 | | V |
| | | V _{CC} = 4.5 V | 3.15 | 3.15 | | |
| | | V _{CC} = 5.5 V | 3.85 | 3.85 | | |
| V _{IL} | Low-level input voltage | V _{CC} = 3 V | | 0.9 | 0.9 | V |
| | | V _{CC} = 4.5 V | | 1.35 | 1.35 | |
| | | V _{CC} = 5.5 V | | 1.65 | 1.65 | |
| V _I | Input voltage | 0 | V _{CC} | 0 | V _{CC} | V |
| V _O | Output voltage | 0 | V _{CC} | 0 | V _{CC} | V |
| I _{OH} | High-level output current | V _{CC} = 3 V | | -12 | -12 | mA |
| | | V _{CC} = 4.5 V | | -24 | -24 | |
| | | V _{CC} = 5.5 V | | -24 | -24 | |
| I _{OL} | Low-level output current | V _{CC} = 3 V | | 12 | 12 | mA |
| | | V _{CC} = 4.5 V | | 24 | 24 | |
| | | V _{CC} = 5.5 V | | 24 | 24 | |
| Δt/Δv | Input transition rise or fall rate | | 8 | | 8 | ns/V |

over recommended operating free-air temperature range (unless otherwise noted)¹

| | | SN54AC240 | | SN74AC240 | | UNIT |
|----------------|--------------------------------|-----------|-----|-----------|-----|------|
| | | MIN | MAX | MIN | MAX | |
| T _a | Operating free-air temperature | -55 | 125 | -40 | 85 | °C |

(1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

5.4 Thermal Information

| THERMAL METRIC ⁽¹⁾ | | DB (SSOP) | DW (SOIC) | N (PDIP) | NS (SOP) | PW (TSSOP) | UNIT |
|-------------------------------|--|--------------|--------------|-------------|-------------|---------------|------|
| | | 20 PINS | 20 PINS | 20 PINS | 20 PINS | 20 PINS | |
| R _{θJA} | Junction-to-ambient thermal resistance | 70 | 101.2 | 69 | 106.2 | 126.2 | °C/W |

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, [SPRA953](#).

5.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | V _{CC} | T _A = 25°C | | | SN54AC240 | | SN74AC240 | | UNIT |
|--|---|---|-----------------------|-------|------|-----------|------|-----------|------|------|
| | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| V _{OH} | I _{oh} = -50 μA | 3 V | 2.9 | | | 2.9 | | 2.9 | | V |
| | | 4.5 V | 4.4 | | | 4.4 | | 4.4 | | |
| | | 5.5 V | 5.4 | | | 5.4 | | 5.4 | | |
| | I _{oh} = -12 mA | 3 V | 2.56 | | | 2.4 | | 2.46 | | |
| | | 4.5 V | 3.86 | | | 3.7 | | 3.76 | | |
| | I _{oh} = -24 mA | 5.5 V | 4.86 | | | 4.7 | | 4.76 | | |
| V _{OL} | I _{ol} = 50 μA | 3 V | 0.1 | | | 0.1 | | 0.1 | | V |
| | | 4.5 V | 0.1 | | | 0.1 | | 0.1 | | |
| | | 5.5 V | 0.1 | | | 0.1 | | 0.1 | | |
| | I _{ol} = 12 mA | 3 V | 0.36 | | | 0.5 | | 0.44 | | |
| | | 4.5 V | 0.36 | | | 0.5 | | 0.44 | | |
| | I _{ol} = 24 mA | 5.5 V | 0.36 | | | 0.5 | | 0.44 | | |
| I _{ol} = 50 mA ⁽¹⁾ | 5.5 V | | | | 3.85 | | | | | |
| | 5.5 V | | | | | | 3.85 | | | |
| I _I | Data inputs | V _I = V _{CC} or GND | ±0.1 | | | ±1 | | ±1 | | μA |
| | Control inputs | V _I = V _{CC} or GND | ±0.1 | | | ±1 | | ±1 | | |
| I _{OZ} ⁽²⁾ | V _O = V _{CC} or GND, V _I (OE) = V _{IL} or V _{IH} | | 5.5 V | ±0.25 | | | ±5 | | ±2.5 | |
| I _{CC} | V _I = V _{CC} or GND, I _O = 0 | 5.5 V | 4 | | | 80 | | 40 | | |
| C _i | V _I = V _{CC} or GND | 5 V | 2.5 | | | | | | | |

(1) Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.

(2) For I/O ports, the parameter I_{OZ} includes the input leakage current.

5.6 Switching Characteristics, $V_{CC} = 3.3 V \pm 0.3 V$

over recommended operating free-air temperature range, $V_{CC} = 3.3 V \pm 0.3 V$ (unless otherwise noted) (see [Load Circuit and Voltage Waveforms](#))

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | $T_A = 25^\circ\text{C}$ | | | SN54AC240 | | SN74AC240 | | UNIT |
|-----------|-----------------|-------------|--------------------------|-----|------|-----------|------|-----------|------|------|
| | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| t_{PLH} | A | Y | 1.5 | 6 | 8 | 1 | 11 | 1 | 9 | ns |
| t_{PHL} | | | 1.5 | 5.5 | 8 | 1 | 10.5 | 1 | 8.5 | |
| t_{PZH} | \overline{OE} | Y | 1.5 | 6 | 10.5 | 1 | 11.5 | 1 | 11 | ns |
| t_{PZL} | | | 1.5 | 7 | 10 | 1 | 13 | 1 | 11 | |
| t_{PHZ} | \overline{OE} | Y | 1.5 | 7 | 10 | 1 | 12.5 | 1 | 10.5 | ns |
| t_{PLZ} | | | 1.5 | 7.5 | 10.5 | 1 | 13.5 | 1 | 11.5 | |

5.7 Switching Characteristics, $V_{CC} = 5 V \pm 0.5 V$

over recommended operating free-air temperature range, $V_{CC} = 5 V \pm 0.5 V$ (unless otherwise noted) (see [Load Circuit and Voltage Waveforms](#))

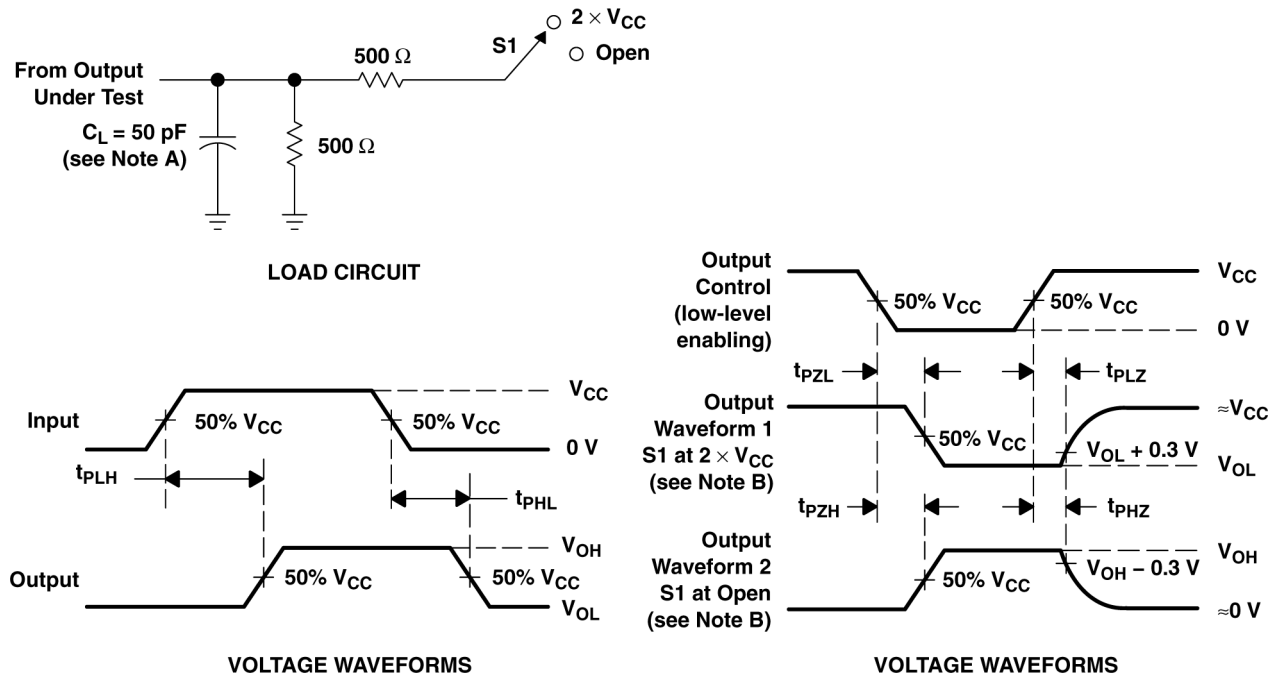
| PARAMETER | FROM (INPUT) | TO (OUTPUT) | $T_A = 25^\circ\text{C}$ | | | SN54AC240 | | SN74AC240 | | UNIT |
|-----------|-----------------|-------------|--------------------------|-----|-----|-----------|------|-----------|-----|------|
| | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| t_{PLH} | A | Y | 1.5 | 4.5 | 6.5 | 1 | 8.5 | 1 | 7 | ns |
| t_{PHL} | | | 1.5 | 4.5 | 6 | 1 | 8 | 1 | 6.5 | |
| t_{PZH} | \overline{OE} | Y | 1.5 | 5 | 7 | 1 | 9 | 1 | 8 | ns |
| t_{PZL} | | | 1.5 | 5.5 | 8 | 1 | 10.5 | 1 | 8.5 | |
| t_{PHZ} | \overline{OE} | Y | 2.5 | 6.5 | 9 | 1 | 10.5 | 1 | 9.5 | ns |
| t_{PLZ} | | | 2 | 6.5 | 9 | 1 | 11 | 1 | 9.5 | |

5.8 Operating Characteristics

$V_{CC} = 5 V$, $T_A = 25^\circ\text{C}$

| PARAMETER | TEST CONDITIONS | TYP | UNIT |
|--|---|-----|------|
| C_{pd} Power dissipation capacitance per buffer/driver | $C_I = 50 \text{ pF}$, $f = 1 \text{ MHz}$ | 45 | pF |

6 Parameter Measurement Information



- C_L includes probe and jig capacitance.
- Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- All input pulses are supplied by generators having the following characteristics: $PRR \leq 1 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r \leq 2.5 \text{ ns}$, $t_f \leq 2.5 \text{ ns}$.
- The outputs are measured one at a time with one input transition per measurement.

图 6-1. Load Circuit and Voltage Waveforms

| TEST | S1 |
|-------------------|-------------------|
| t_{PLH}/t_{PHL} | Open |
| t_{PLZ}/t_{PZL} | $2 \times V_{CC}$ |
| t_{PHZ}/t_{PZH} | Open |

7 Detailed Description

7.1 Overview

The 'AC240 devices are organized as two 4-bit buffers/drivers with separate output-enable (\overline{OE}) inputs. When \overline{OE} is low, the device passes inverted data from the A inputs to the Y outputs. When \overline{OE} is high, the outputs are in the high-impedance state.

To ensure the high-impedance state during power

up or power down, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

7.2 Functional Block Diagram

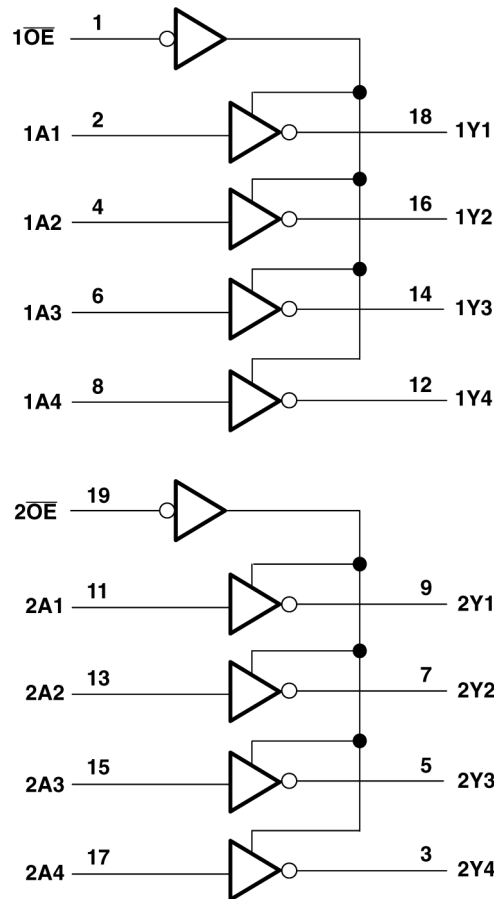


图 7-1. Logic Diagram (Positive Logic)

7.3 Device Functional Modes

表 7-1. Function Table (Each Buffer)

| INPUTS | | OUTPUT |
|-----------------|---|--------|
| \overline{OE} | A | Y |
| L | H | L |
| L | L | H |
| H | X | Z |

8 Application and Implementation

备注

以下应用部分中的信息不属于 TI 器件规格的范围，TI 不担保其准确性和完整性。TI 的客户应负责确定器件是否适用于其应用。客户应验证并测试其设计，以确保系统功能。

8.1 Power Supply Recommendations

The power supply can be any voltage between the min and max supply voltage rating located in [节 5.3](#).

Each V_{CC} terminal should have a good bypass capacitor to prevent power disturbance. For devices with a single supply, TI recommends $0.1\ \mu\text{F}$ and if there are multiple V_{CC} terminals, then TI recommends $.01\ \mu\text{F}$ or $.022\ \mu\text{F}$ for each power terminal. It is okay to parallel multiple bypass capacitors to reject different frequencies of noise. A $0.1\ \mu\text{F}$ and $1\ \mu\text{F}$ are commonly used in parallel. The bypass capacitor should be installed as close to the power terminal as possible for best results.

8.2 Layout

8.2.1 Layout Guidelines

When using multiple bit logic devices inputs should not ever float.

In many cases, functions or parts of functions of digital logic devices are unused, for example, when only two inputs of a triple-input AND gate are used or only 3 of the 4 buffer gates are used. Such input pins should not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. Specified below are the rules that must be observed under all circumstances. All unused inputs of digital logic devices must be connected to a high or low bias to prevent them from floating. The logic level that should be applied to any particular unused input depends on the function of the device. Generally they will be tied to GND or V_{CC} whichever make more sense or is more convenient. It is generally okay to float outputs unless the part is a transceiver. If the transceiver has an output enable pin it will disable the outputs section of the part when asserted. This does not disable the input section of the IOs so they cannot float when disabled.

8.2.1.1 Layout Example

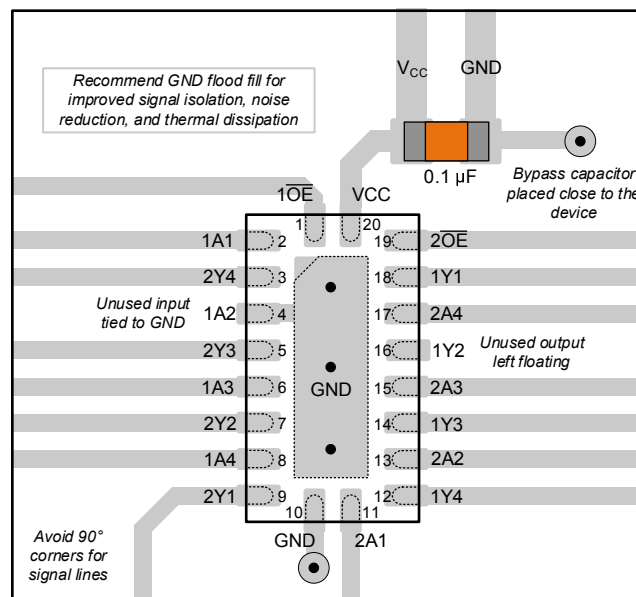


图 8-1. Layout example for the SNx4AC240

9 Device and Documentation Support

9.1 Documentation Support

9.1.1 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

表 9-1. Related Links

| PARTS | PRODUCT FOLDER | SAMPLE & BUY | TECHNICAL DOCUMENTS | TOOLS & SOFTWARE | SUPPORT & COMMUNITY |
|-----------|----------------------------|----------------------------|----------------------------|----------------------------|----------------------------|
| SN54AC240 | Click here | Click here | Click here | Click here | Click here |
| SN74AC240 | Click here | Click here | Click here | Click here | Click here |

9.2 接收文档更新通知

要接收文档更新通知，请导航至 ti.com 上的器件产品文件夹。点击 [通知](#) 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

9.3 支持资源

[TI E2E™ 中文支持论坛](#) 是工程师的重要参考资料，可直接从专家处获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题，获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的 [使用条款](#)。

9.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.
所有商标均为其各自所有者的财产。

9.5 静电放电警告



静电放电 (ESD) 会损坏这个集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

9.6 术语表

[TI 术语表](#) 本术语表列出并解释了术语、首字母缩略词和定义。

10 Revision History

注：以前版本的页码可能与当前版本的页码不同

| Changes from Revision F (April 2023) to Revision G (March 2024) | Page |
|---|-------------|
| • 向封装信息表中增加了封装尺寸..... | 1 |
| • Updated high-level input voltage values in <i>Recommended Operating Conditions</i> table..... | 4 |
| • Updated R ^θ JA values: DW = 58 to 101.2, NS = 60 to 106.2, PW = 83 to 126.2, all values in °C/W..... | 5 |
| • Added <i>Application and Implementation</i> section..... | 9 |

| Changes from Revision E (October 2003) to Revision F (April 2023) | Page |
|---|-------------|
| • 添加了应用、封装信息表、引脚功能表、ESD 等级表、热性能信息表、器件功能模式、应用和实施部分、电源相关建议部分、布局部分、器件和文档支持部分以及机械、封装和可订购信息部分..... | 1 |

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

| Orderable part number | Status (1) | Material type (2) | Package Pins | Package qty Carrier | RoHS (3) | Lead finish/ Ball material (4) | MSL rating/ Peak reflow (5) | Op temp (°C) | Part marking (6) |
|--------------------------------|---------------|----------------------|-----------------|-----------------------|-------------|--------------------------------------|-----------------------------------|--------------|--|
| 5962-87550012A | Active | Production | LCCC (FK) 20 | 55 TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | 5962- 87550012A SNJ54AC 240FK |
| 5962-8755001RA | Active | Production | CDIP (J) 20 | 20 TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | 5962-8755001RA SNJ54AC240J |
| 5962-8755001SA | Active | Production | CFP (W) 20 | 25 TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | 5962-8755001SA SNJ54AC240W |
| SN74AC240DBR | Active | Production | SSOP (DB) 20 | 2000 LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | AC240 |
| SN74AC240DBR.A | Active | Production | SSOP (DB) 20 | 2000 LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | AC240 |
| SN74AC240DW | Obsolete | Production | SOIC (DW) 20 | - | - | Call TI | Call TI | -40 to 85 | AC240 |
| SN74AC240DWR | Active | Production | SOIC (DW) 20 | 2000 LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | AC240 |
| SN74AC240DWR.A | Active | Production | SOIC (DW) 20 | 2000 LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | AC240 |
| SN74AC240N | Active | Production | PDIP (N) 20 | 20 TUBE | Yes | NIPDAU | N/A for Pkg Type | -40 to 85 | SN74AC240N |
| SN74AC240N.A | Active | Production | PDIP (N) 20 | 20 TUBE | Yes | NIPDAU | N/A for Pkg Type | -40 to 85 | SN74AC240N |
| SN74AC240NSR | Active | Production | SOP (NS) 20 | 2000 LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | AC240 |
| SN74AC240NSR.A | Active | Production | SOP (NS) 20 | 2000 LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | AC240 |
| SN74AC240PW | Obsolete | Production | TSSOP (PW) 20 | - | - | Call TI | Call TI | -40 to 85 | AC240 |
| SN74AC240PWR | Active | Production | TSSOP (PW) 20 | 2000 LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | AC240 |
| SN74AC240PWR.A | Active | Production | TSSOP (PW) 20 | 2000 LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | AC240 |
| SN74AC240PWRE4 | Active | Production | TSSOP (PW) 20 | 2000 LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | AC240 |
| SNJ54AC240FK | Active | Production | LCCC (FK) 20 | 55 TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | 5962- 87550012A SNJ54AC 240FK |
| SNJ54AC240FK.A | Active | Production | LCCC (FK) 20 | 55 TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | 5962- 87550012A SNJ54AC 240FK |
| SNJ54AC240J | Active | Production | CDIP (J) 20 | 20 TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | 5962-8755001RA SNJ54AC240J |

| Orderable part number | Status (1) | Material type (2) | Package Pins | Package qty Carrier | RoHS (3) | Lead finish/ Ball material (4) | MSL rating/ Peak reflow (5) | Op temp (°C) | Part marking (6) |
|-----------------------------|---------------|----------------------|----------------|-----------------------|-------------|--------------------------------------|-----------------------------------|--------------|-------------------------------|
| SNJ54AC240J.A | Active | Production | CDIP (J) 20 | 20 TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | 5962-8755001RA SNJ54AC240J |
| SNJ54AC240W | Active | Production | CFP (W) 20 | 25 TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | 5962-8755001SA SNJ54AC240W |
| SNJ54AC240W.A | Active | Production | CFP (W) 20 | 25 TUBE | No | SNPB | N/A for Pkg Type | -55 to 125 | 5962-8755001SA SNJ54AC240W |

(1) **Status:** For more details on status, see our [product life cycle](#).

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "-" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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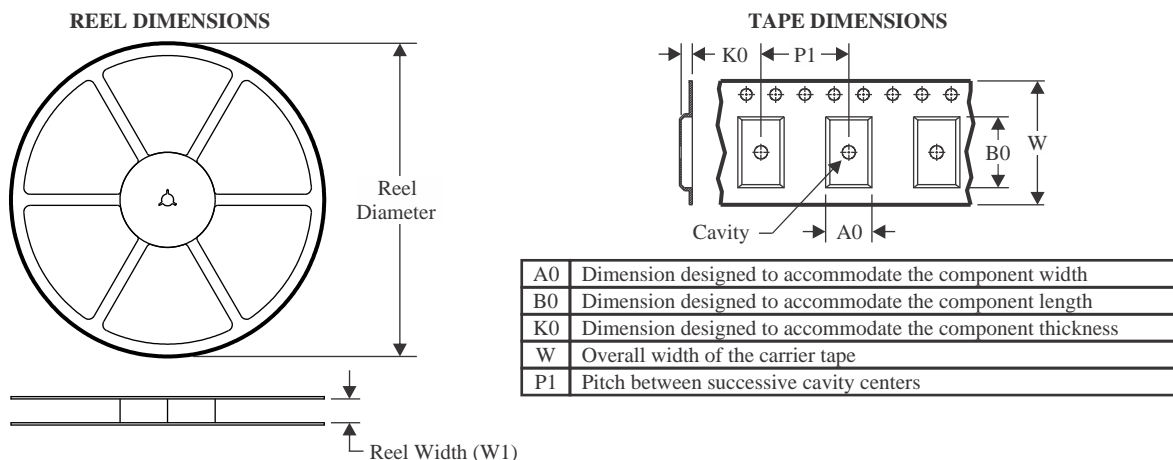
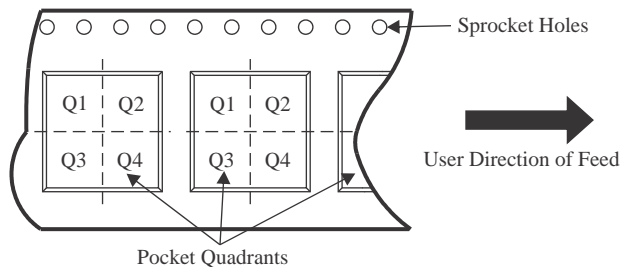
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF SN54AC240, SN74AC240 :

- Catalog : [SN74AC240](#)
- Automotive : [SN74AC240-Q1](#), [SN74AC240-Q1](#)
- Military : [SN54AC240](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects
- Military - QML certified for Military and Defense Applications

TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|--------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| SN74AC240DBR | SSOP | DB | 20 | 2000 | 330.0 | 16.4 | 8.2 | 7.5 | 2.5 | 12.0 | 16.0 | Q1 |
| SN74AC240DWR | SOIC | DW | 20 | 2000 | 330.0 | 24.4 | 10.9 | 13.3 | 2.7 | 12.0 | 24.0 | Q1 |
| SN74AC240DWR | SOIC | DW | 20 | 2000 | 330.0 | 24.4 | 10.8 | 13.3 | 2.7 | 12.0 | 24.0 | Q1 |
| SN74AC240NSR | SOP | NS | 20 | 2000 | 330.0 | 24.4 | 8.4 | 13.0 | 2.5 | 12.0 | 24.0 | Q1 |
| SN74AC240PWR | TSSOP | PW | 20 | 2000 | 330.0 | 16.4 | 6.95 | 7.0 | 1.4 | 8.0 | 16.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|--------------|--------------|-----------------|------|------|-------------|------------|-------------|
| SN74AC240DBR | SSOP | DB | 20 | 2000 | 353.0 | 353.0 | 32.0 |
| SN74AC240DWR | SOIC | DW | 20 | 2000 | 356.0 | 356.0 | 45.0 |
| SN74AC240DWR | SOIC | DW | 20 | 2000 | 356.0 | 356.0 | 45.0 |
| SN74AC240NSR | SOP | NS | 20 | 2000 | 356.0 | 356.0 | 45.0 |
| SN74AC240PWR | TSSOP | PW | 20 | 2000 | 353.0 | 353.0 | 32.0 |

TUBE


*All dimensions are nominal

| Device | Package Name | Package Type | Pins | SPQ | L (mm) | W (mm) | T (μm) | B (mm) |
|----------------|--------------|--------------|------|-----|--------|--------|--------|--------|
| 5962-87550012A | FK | LCCC | 20 | 55 | 506.98 | 12.06 | 2030 | NA |
| 5962-8755001SA | W | CFP | 20 | 25 | 506.98 | 26.16 | 6220 | NA |
| SN74AC240N | N | PDIP | 20 | 20 | 506 | 13.97 | 11230 | 4.32 |
| SN74AC240N.A | N | PDIP | 20 | 20 | 506 | 13.97 | 11230 | 4.32 |
| SNJ54AC240FK | FK | LCCC | 20 | 55 | 506.98 | 12.06 | 2030 | NA |
| SNJ54AC240FK.A | FK | LCCC | 20 | 55 | 506.98 | 12.06 | 2030 | NA |
| SNJ54AC240W | W | CFP | 20 | 25 | 506.98 | 26.16 | 6220 | NA |
| SNJ54AC240W.A | W | CFP | 20 | 25 | 506.98 | 26.16 | 6220 | NA |

DB0020A



PACKAGE OUTLINE

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



4214851/B 08/2019

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-150.

EXAMPLE BOARD LAYOUT

DB0020A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



4214851/B 08/2019

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DB0020A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4214851/B 08/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

MECHANICAL DATA

NS (R-PDSO-G)**

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

J (R-GDIP-T**)

14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



| DIM \ PINS ** | 14 | 16 | 18 | 20 |
|---------------|------------------------|------------------------|------------------------|------------------------|
| A | 0.300 (7,62) BSC | 0.300 (7,62) BSC | 0.300 (7,62) BSC | 0.300 (7,62) BSC |
| B MAX | 0.785 (19,94) | .840 (21,34) | 0.960 (24,38) | 1.060 (26,92) |
| B MIN | — | — | — | — |
| C MAX | 0.300 (7,62) | 0.300 (7,62) | 0.310 (7,87) | 0.300 (7,62) |
| C MIN | 0.245 (6,22) | 0.245 (6,22) | 0.220 (5,59) | 0.245 (6,22) |



4040083/F 03/03

- NOTES:
- All linear dimensions are in inches (millimeters).
 - This drawing is subject to change without notice.
 - This package is hermetically sealed with a ceramic lid using glass frit.
 - Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
 - Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

GENERIC PACKAGE VIEW

FK 20

LCCC - 2.03 mm max height

8.89 x 8.89, 1.27 mm pitch

LEADLESS CERAMIC CHIP CARRIER

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4229370VA\

N (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
 - The 20 pin end lead shoulder width is a vendor option, either half or full width.

DW0020A



PACKAGE OUTLINE

SOIC - 2.65 mm max height

SOIC



4220724/A 05/2016

EXAMPLE BOARD LAYOUT

DW0020A

SOIC - 2.65 mm max height

SOIC



LAND PATTERN EXAMPLE
SCALE:6X



SOLDER MASK DETAILS

4220724/A 05/2016

NOTES: (continued)

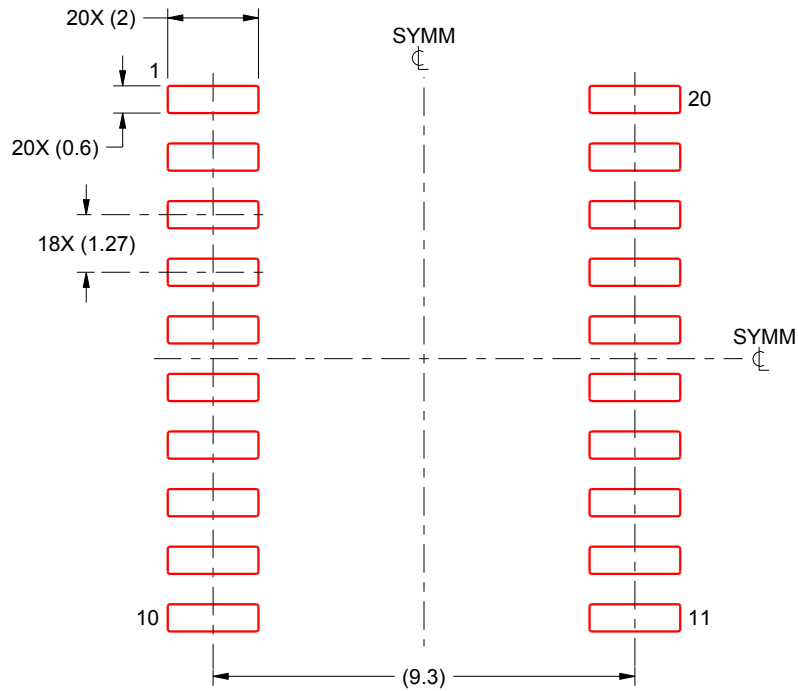
- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DW0020A

SOIC - 2.65 mm max height

SOIC



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

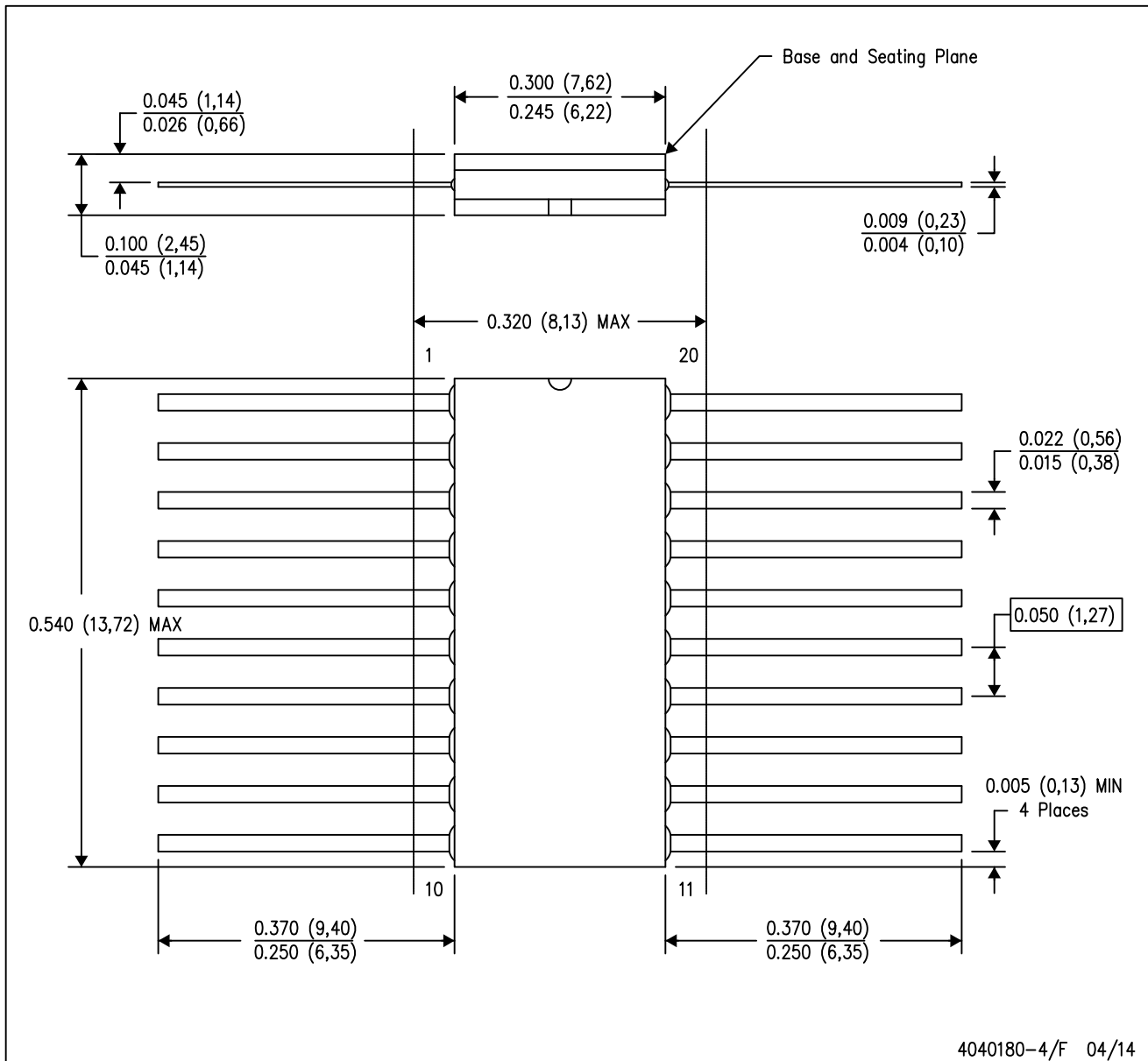
4220724/A 05/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

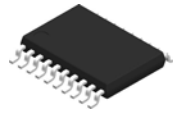
W (R-GDFP-F20)

CERAMIC DUAL FLATPACK



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. This package can be hermetically sealed with a ceramic lid using glass frit.
 - D. Index point is provided on cap for terminal identification only.
 - E. Falls within Mil-Std 1835 GDFP2-F20

PW0020A



PACKAGE OUTLINE

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



4220206/A 02/2017

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

EXAMPLE BOARD LAYOUT

PW0020A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



SOLDER MASK DETAILS

4220206/A 02/2017

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

PW0020A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220206/A 02/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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