

# SN74AHC1G86-Q1 汽车类单通道双输入异或门

## 1 特性

- 符合汽车应用要求
- 具有符合 AEC-Q100 标准的下列特性：
  - ±4000V 人体放电模型 (HBM) ESD 分类等级 3A
  - ±1000V 充电器件模型 (CDM) ESD 分级等级 C5
- 工作电压范围为 2V 至 5.5V
- 5V 时,  $t_{pd}$  最大值为 10ns
- 低功耗,  $I_{CC}$  最大值为 10  $\mu$ A
- 5V 时, 输出驱动为 ±8mA
- 所有输入端均采用施密特触发器, 使得电路能够承受较慢的输入上升和下降时间

## 2 应用

- 无线耳机
- 电机驱动与控制
- 电视
- 机顶盒
- 音频

## 3 说明

SN74AHC1G86-Q1 是一款单通道双输入异或门。该器件执行布尔函数  $Y = A \oplus B$  或  $Y = \overline{AB} + A\overline{B}$ 。

常用作真/补元件。如果一个输入为低电平, 则可在输出时重新生成真实形态的其他输入。如果一个输入为高电平, 另一个输入的信号则可在输出时重新生成反向信号。

### 封装信息

器件型号	封装 <sup>(1)</sup>	封装尺寸 <sup>(2)</sup>	封装尺寸 <sup>(3)</sup>
SN74AHC1G86-Q1	DBV ( SOT-23 , 5 )	2.90mm × 2.8mm	2.90mm × 1.60mm

- 有关更多信息, 请参阅第 11 节。
- 封装尺寸 (长 × 宽) 为标称值, 并包括引脚 (如适用)。
- 封装尺寸 (长 × 宽) 为标称值, 不包括引脚。



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功能方框图

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## 4 Pin Configuration and Functions

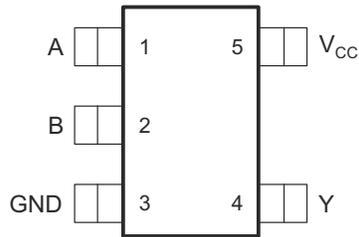


图 4-1. DBV Package 5-Pin SOT-23 Top View

表 4-1. Pin Functions

PIN		I/O	DESCRIPTION
NO.	NAME		
1	A	I	Input A
2	B	I	Input B
3	GND	—	Ground
4	Y	O	Output Y
5	V <sub>CC</sub>	—	Positive Supply

## 5 Specifications

### 5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

		MIN	MAX	UNIT
V <sub>CC</sub>	Supply voltage range	- 0.5	7	V
V <sub>I</sub>	Input voltage range <sup>(2)</sup>	- 0.5	7	V
V <sub>O</sub>	Output voltage range applied in the high- or low-state <sup>(2)</sup>	- 0.5	V <sub>CC</sub> + 0.5	V
I <sub>IK</sub>	Input clamp current	(V <sub>I</sub> < 0V)	- 20	V
I <sub>OK</sub>	Output clamp current	(V <sub>O</sub> < 0V or V <sub>O</sub> > V <sub>CC</sub> )	±20	mA
I <sub>O</sub>	Continuous output current	(V <sub>O</sub> = 0V to V <sub>CC</sub> )	±25	mA
	Continuous current through V <sub>CC</sub> or GND		±50	mA
T <sub>J</sub>	Junction temperature		150	°C
T <sub>stg</sub>	Storage temperature range	- 65	150	°C

- (1) Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

### 5.2 ESD Ratings

		VALUE	UNIT
V <sub>(ESD)</sub>	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002 <sup>(1)</sup>	±4000
		Charged-device model (CDM), per AEC Q100-011	±1000

- (1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

### 5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

		MIN	MAX	UNIT
V <sub>CC</sub>	Supply voltage	2	5.5	V
V <sub>IH</sub>	High-level input voltage	V <sub>CC</sub> = 2V	1.5	V
		V <sub>CC</sub> = 3V	2.1	
		V <sub>CC</sub> = 5.5V	3.85	
V <sub>IL</sub>	Low-level input voltage	V <sub>CC</sub> = 2V	0.5	V
		V <sub>CC</sub> = 3V	0.9	
		V <sub>CC</sub> = 5.5V	1.65	
V <sub>I</sub>	Input voltage	0	5.5	V
V <sub>O</sub>	Output voltage	0	V <sub>CC</sub>	V
I <sub>OH</sub>	High-level output current	V <sub>CC</sub> = 2V	- 50	μA
		V <sub>CC</sub> = 3.3V ±0.3V	- 4	mA
		V <sub>CC</sub> = 5V ±0.5V	- 8	
I <sub>OL</sub>	Low-level output current	V <sub>CC</sub> = 2V	50	μA
		V <sub>CC</sub> = 3.3V ±0.3V	4	mA
		V <sub>CC</sub> = 5V ±0.5V	8	
Δt/ΔV	Input transition rise or fall rate	V <sub>CC</sub> = 3.3V ±0.3V	100	ns/V
		V <sub>CC</sub> = 5V ±0.5V	20	
T <sub>A</sub>	Operating free-air temperature	- 40	125	°C

- (1) All unused inputs of the device must be held at V<sub>CC</sub> or GND to ensure proper device operation.

## 5.4 Thermal Information

THERMAL METRIC <sup>(1)</sup>		SN74AHC1G86-Q1	UNIT
		DBV (SOT-23)	
		5 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	278	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	180.5	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	184.4	°C/W
$\psi_{JT}$	Junction-to-top characterization parameter	115.4	°C/W
$\psi_{JB}$	Junction-to-board characterization parameter	183.4	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

## 5.5 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	$V_{CC}$	$T_A = 25^\circ\text{C}$			MIN	MAX	UNIT
			MIN	TYP	MAX			
$V_{OH}$	$I_{OH} = -50 \mu\text{A}$	2V	1.9	2		1.9	V	
		3V	2.9	3		2.9		
		4.5V	4.4	4.5		4.4		
$V_{OL}$	$I_{OL} = 50 \mu\text{A}$	2V			0.1	0.1	V	
		3V			0.1	0.1		
		4.5V			0.1	0.1		
$V_{OL}$	$I_{OL} = 4\text{mA}$	3V			0.36	0.44	V	
		4.5V			0.36	0.44		
$I_I$	$V_I = 5.5\text{V}$ or GND	0V to 5.5V			$\pm 0.1$	$\pm 1$	$\mu\text{A}$	
$I_{CC}$	$V_I = V_{CC}$ or GND, $I_O = 0\text{A}$	5.5V			1	10	$\mu\text{A}$	
$C_I$	$V_I = V_{CC}$ or GND	5V		4	10	10	pF	

## 5.6 Switching Characteristics, $V_{CC} = 3.3\text{V} \pm 0.3\text{V}$

over recommended operating free-air temperature range,  $V_{CC} = 3.3\text{V} \pm 0.3\text{V}$ ,  $T_A = -40^\circ\text{C}$  to  $125^\circ\text{C}$ , see [Load Circuit and Voltage Waveforms](#)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	$T_A = 25^\circ\text{C}$			MIN	MAX	UNIT
				MIN	TYP	MAX			
$t_{PLH}$	A or B	Y	$C_L = 50\text{pF}$		9.5	14.5	1	16.5	ns
$t_{PHL}$					9.5	14.5	1	16.5	

## 5.7 Switching Characteristics, $V_{CC} = 5\text{V} \pm 0.5\text{V}$

over recommended operating free-air temperature range,  $V_{CC} = 5\text{V} \pm 0.5\text{V}$ ,  $T_A = -40^\circ\text{C}$  to  $125^\circ\text{C}$ , see [Load Circuit and Voltage Waveforms](#)

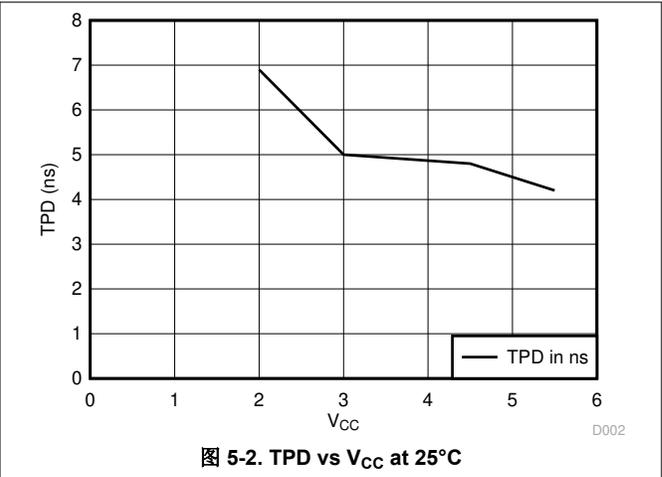
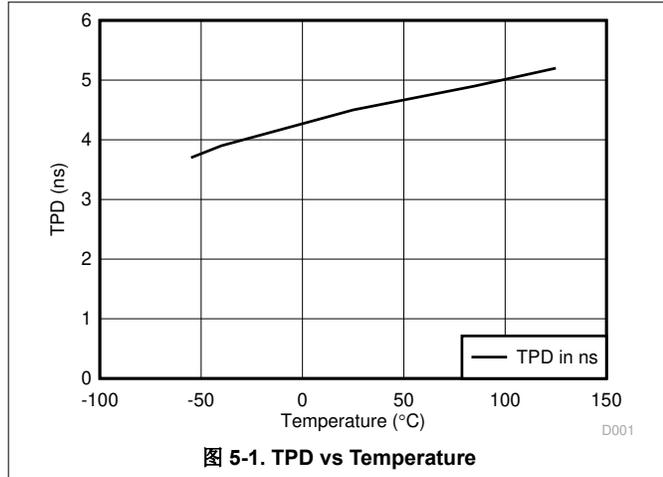
PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	$T_A = 25^\circ\text{C}$			MIN	MAX	UNIT
				MIN	TYP	MAX			
$t_{PLH}$	A or B	Y	$C_L = 50\text{pF}$		6.3	8.8	1	10	ns
$t_{PHL}$					6.3	8.8	1	10	

### 5.8 Operating Characteristics

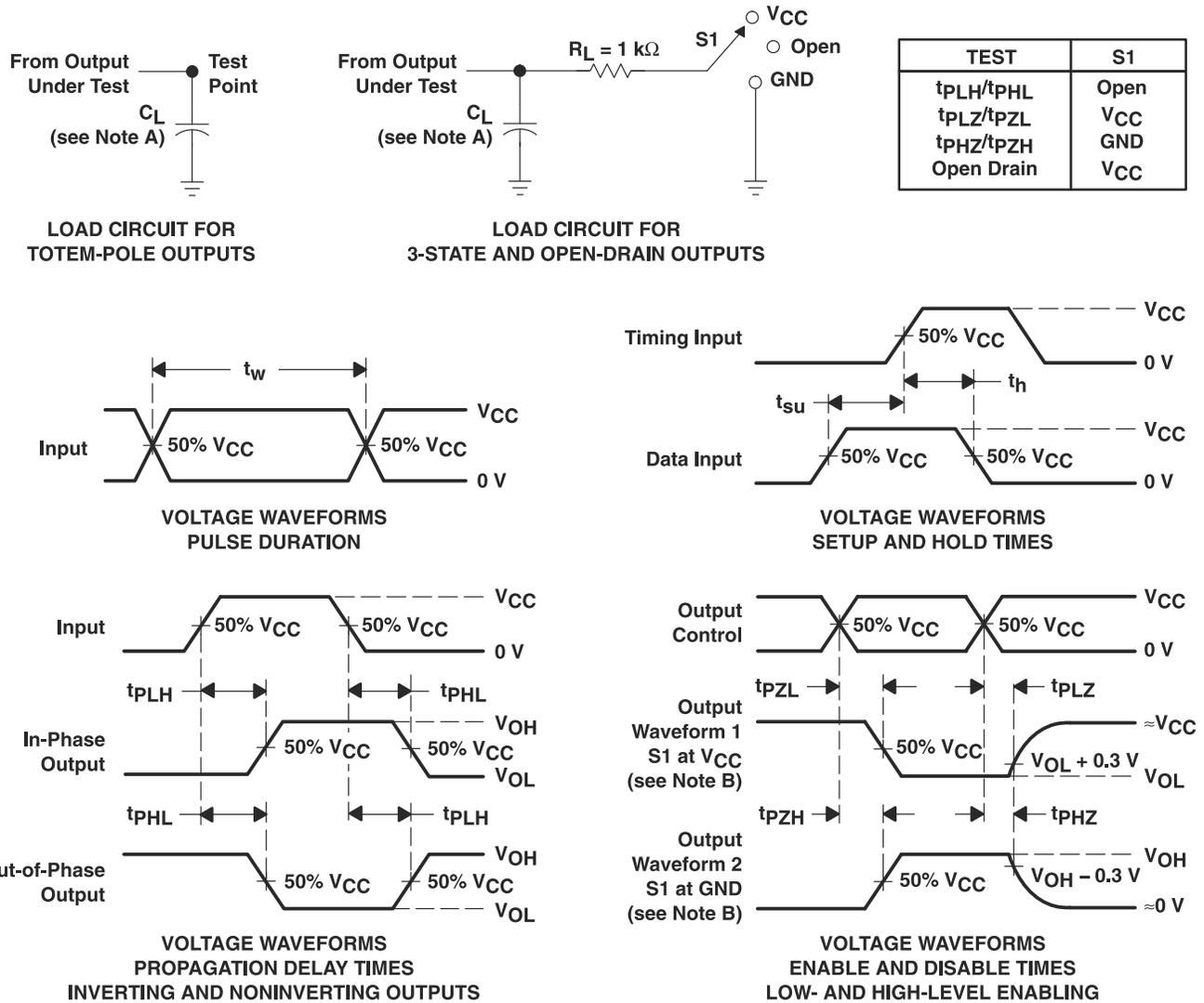
$V_{CC} = 5V, T_A = 25^\circ C$

PARAMETER	TEST CONDITIONS	TYP	UNIT
$C_{pd}$ Power dissipation capacitance	No load, $f = 1MHz$	18	pF

### 5.9 Typical Characteristics



## 6 Parameter Measurement Information



- NOTES: A.  $C_L$  includes probe and jig capacitance.  
 B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.  
 C. All input pulses are supplied by generators having the following characteristics: PRR  $\leq$  1 MHz,  $Z_O = 50 \Omega$ ,  $t_r \leq 3$  ns,  $t_f \leq 3$  ns.  
 D. The outputs are measured one at a time, with one input transition per measurement.

图 6-1. Load Circuit and Voltage Waveforms

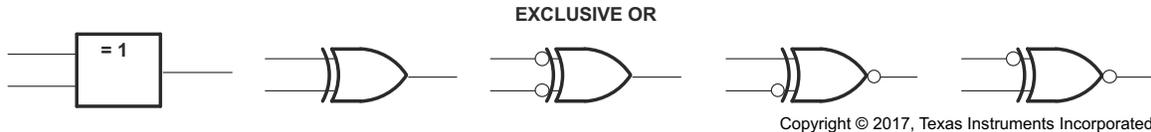
## 7 Detailed Description

### 7.1 Overview

The SN74AHC1G86-Q1 is an automotive qualified device that performs the Boolean function  $Y = \bar{A}B + A\bar{B}$  in positive logic. This single 2-input exclusive-OR gate is designed for 2V to 5.5V  $V_{CC}$  operation.

A common application is as a true or complementary element. If one of the inputs is low, the other input is reproduced in true form at the output. If one of the inputs is high, the signal on the other input is reproduced inverted at the output.

### 7.2 Functional Block Diagram



These are five equivalent exclusive-OR symbols valid for an SN74AHC1G86-Q1 gate in positive logic; negation may be shown at any two ports.

### 7.3 Feature Description

#### 7.3.1 Balanced CMOS Push-Pull Outputs

A balanced output allows the device to sink and source similar currents. The drive capability of this device may create fast edges into light loads so routing and load conditions should be considered to prevent ringing. Additionally, the outputs of this device are capable of driving larger currents than the device can sustain without being damaged. It is important for the output power of the device to be limited to avoid damage due to over-current. The electrical and thermal limits defined in the must be followed at all times.

#### 7.3.2 Standard CMOS Inputs

Standard CMOS inputs are high impedance and are typically modeled as a resistor in parallel with the input capacitance given in the . The worst case resistance is calculated with the maximum input voltage, given in the , and the maximum input leakage current, given in the , using ohm's law ( $R = V \div I$ ).

Signals applied to the inputs need to have fast edge rates, as defined by  $\Delta t / \Delta v$  in to avoid excessive current consumption and oscillations. If a slow or noisy input signal is required, a device with a Schmitt-trigger input should be used to condition the input signal prior to the standard CMOS input.

#### 7.3.3 Clamping Diodes

The inputs have negative clamping diodes, and the outputs have positive and negative clamping diodes as depicted in [图 7-1](#).

#### 小心

Voltages beyond the values specified in the table can cause damage to the device. The input negative-voltage and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

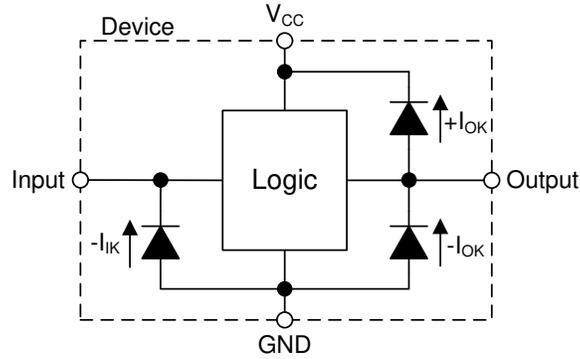


图 7-1. Electrical Placement of Clamping Diodes for Each Input and Output

### 7.3.4 Over-voltage Tolerant Inputs

Input signals to this device can be driven above the supply voltage so long as they remain below the maximum input voltage value specified in the .

### 7.4 Device Functional Modes

表 7-1 lists the functional modes of the SN74AHC1G86-Q1 device.

表 7-1. Function Table

INPUTS		OUTPUT Y
A	B	
L	L	L
L	H	H
H	L	H
H	H	L

## 8 Application and Implementation

### 备注

以下应用部分中的信息不属于 TI 器件规格的范围，TI 不担保其准确性和完整性。TI 的客户应负责确定器件是否适用于其应用。客户应验证并测试其设计，以确保系统功能。

### 8.1 Application Information

The SN74AHC1G86-Q1 is a low-drive CMOS device that can be used for a multitude of bus interface type applications where output ringing is a concern. The low drive and slow edge rates will minimize overshoot and undershoot on the outputs. The inputs can accept voltages to 5.5V at any valid  $V_{CC}$  making it ideal for down translation.

### 8.2 Typical Application

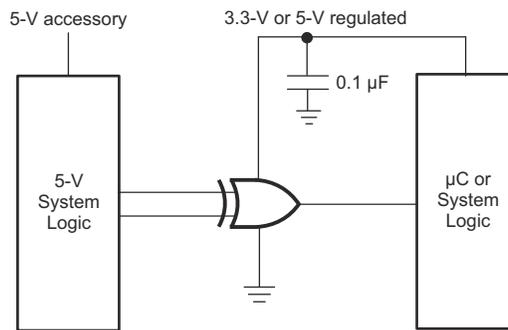


图 8-1. Typical Application Schematic

#### 8.2.1 Design Requirements

This device uses CMOS technology and has balanced output drive. Take care to avoid bus contention because it can drive currents that would exceed maximum limits.

#### 8.2.2 Detailed Design Procedure

1. Recommended Input Conditions
  - For rise time and fall time specifications, see  $\Delta t / \Delta V$  in the table.
  - For specified High and low levels, see  $V_{IH}$  and  $V_{IL}$  in the table.
  - Inputs are overvoltage tolerant allowing them to go as high as 5.5V at any valid  $V_{CC}$ .
2. Recommended Output Conditions
  - Load currents should not exceed 8mA per output.
  - Outputs should not be pulled above  $V_{CC}$ .

### 8.2.3 Application Curve

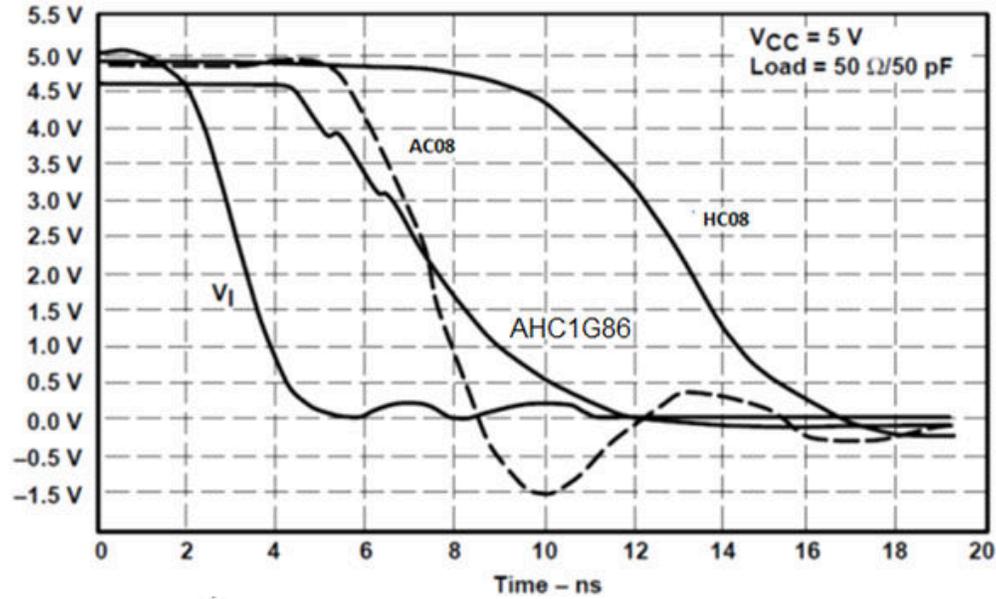


图 8-2. Switching Characteristics Comparison

### 8.3 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in the table.

Each  $V_{CC}$  pin must have a good bypass capacitor to prevent power disturbance. For devices with a single supply,  $0.1\mu F$  is recommended. If there are multiple  $V_{CC}$  pins,  $0.01\mu F$  or  $0.022\mu F$  is recommended for each power pin. It is acceptable to parallel multiple bypass caps to reject different frequencies of noise. A  $0.1\mu F$  and  $1\mu F$  are commonly used in parallel. The bypass capacitor must be installed as close to the power pin as possible for best results.

### 8.4 Layout

#### 8.4.1 Layout Guidelines

Even low data rate digital signals can have high frequency signal components due to fast edge rates. When a PCB trace turns a corner at a  $90^\circ$  angle, a reflection can occur. A reflection occurs primarily because of the change of width of the trace. At the apex of the turn, the trace width increases to 1.414 times the width. This increase upsets the transmission-line characteristics, especially the distributed capacitance and self-inductance of the trace which results in the reflection. Not all PCB traces can be straight and therefore some traces must turn corners. shows progressively better techniques of rounding corners. Only the last example (BEST) maintains constant trace width and minimizes reflections.

### 8.4.2 Layout Example

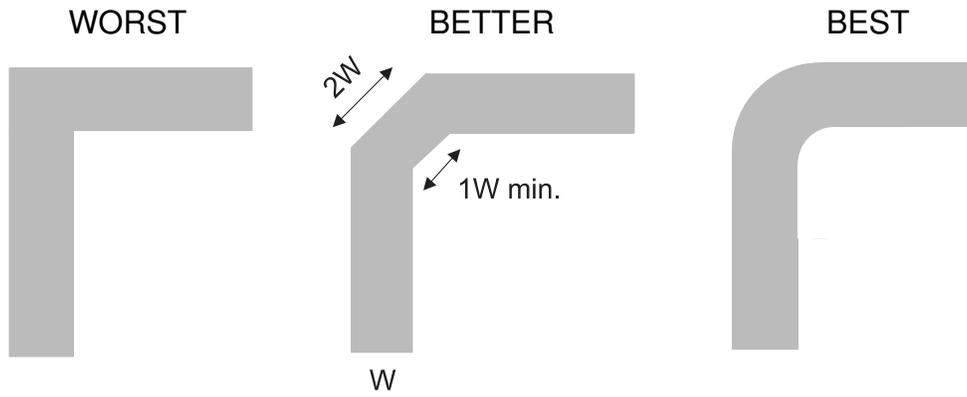


图 8-3. Trace Example

## 9 Device and Documentation Support

### 9.1 Community Resources

#### 9.2 接收文档更新通知

要接收文档更新通知，请导航至 [ti.com](http://ti.com) 上的器件产品文件夹。点击 [通知](#) 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

#### 9.3 支持资源

[TI E2E™ 中文支持论坛](#) 是工程师的重要参考资料，可直接从专家处获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题，获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的 [使用条款](#)。

#### 9.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.

所有商标均为其各自所有者的财产。

#### 9.5 静电放电警告



静电放电 (ESD) 会损坏这个集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

#### 9.6 术语表

[TI 术语表](#) 本术语表列出并解释了术语、首字母缩略词和定义。

## 10 Revision History

注：以前版本的页码可能与当前版本的页码不同

Changes from Revision A (May 2019) to Revision B (February 2024)	Page
• 更新了整个文档中的表格、图和交叉参考的编号格式.....	1
• Updated thermal values for DBV package from $R_{\theta JA} = 224.1$ to 278, $R_{\theta JC(top)} = 152.8$ to 180.5, $R_{\theta JB} = 131.8$ to 184.4, $\Psi_{JT} = 65.7$ to 115.4, $\Psi_{JB} = 131.0$ to 183.4, $R_{\theta JC(bot)} = N/A$ , all values in $^{\circ}C/W$ .....	5

Changes from Revision * (April 2011) to Revision A (May 2019)	Page
• 更改了“特性”部分.....	1
• 添加了“应用”部分.....	1
• 更改了“说明”部分.....	1
• Changed Pin Configuration and Functions section.....	3
• Added $T_J$ spec to Absolute Maximum Ratings table.....	4
• Changed $T_{stg}$ to $-65^{\circ}$ (min) and $150^{\circ}C$ (max) from $-40^{\circ}C$ (min) and $125^{\circ}C$ (max).....	4
• Added ESD Ratings table.....	4
• Added Thermal Information table.....	5
• Added Typical Characteristics section.....	6
• Added Application and Implementation section .....	10
• Added Power Supply Recommendations section .....	11

## 11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

**PACKAGING INFORMATION**

Orderable part number	Status (1)	Material type (2)	Package   Pins	Package qty   Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SN74AHC1G86QDBVRQ1	Active	Production	SOT-23 (DBV)   5	3000   LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	(39KH, ACYU)
SN74AHC1G86QDBVRQ1.A	Active	Production	SOT-23 (DBV)   5	3000   LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	(39KH, ACYU)

(1) **Status:** For more details on status, see our [product life cycle](#).

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "-" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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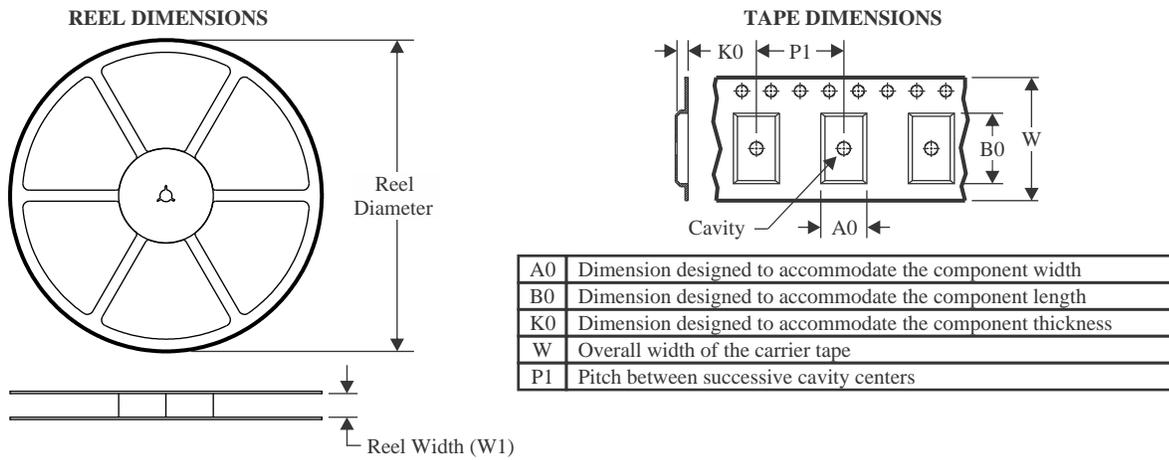
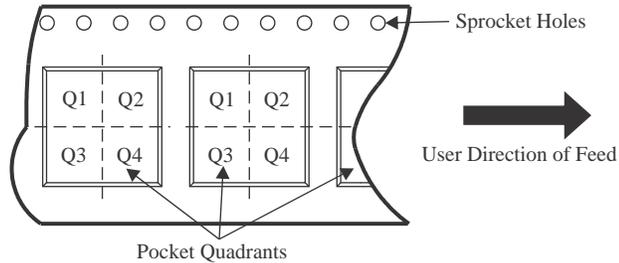
**OTHER QUALIFIED VERSIONS OF SN74AHC1G86-Q1 :**

- Catalog : [SN74AHC1G86](#)

- Enhanced Product : [SN74AHC1G86-EP](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Enhanced Product - Supports Defense, Aerospace and Medical Applications

**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74AHC1G86QDBVRQ1	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
SN74AHC1G86QDBVRQ1	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74AHC1G86QDBVRQ1	SOT-23	DBV	5	3000	210.0	185.0	35.0
SN74AHC1G86QDBVRQ1	SOT-23	DBV	5	3000	210.0	185.0	35.0

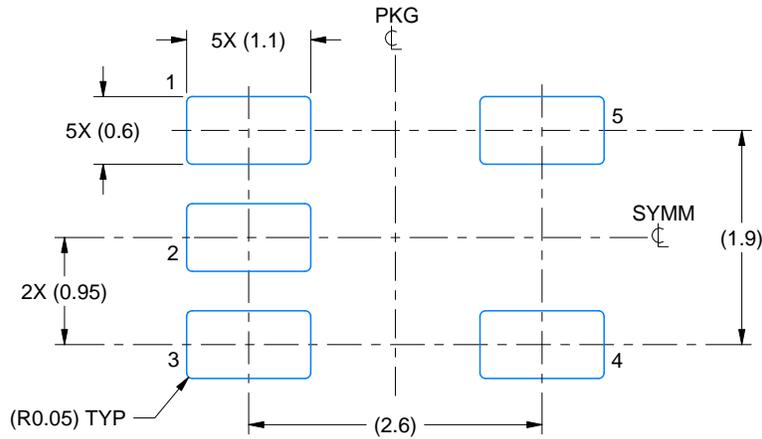


# EXAMPLE BOARD LAYOUT

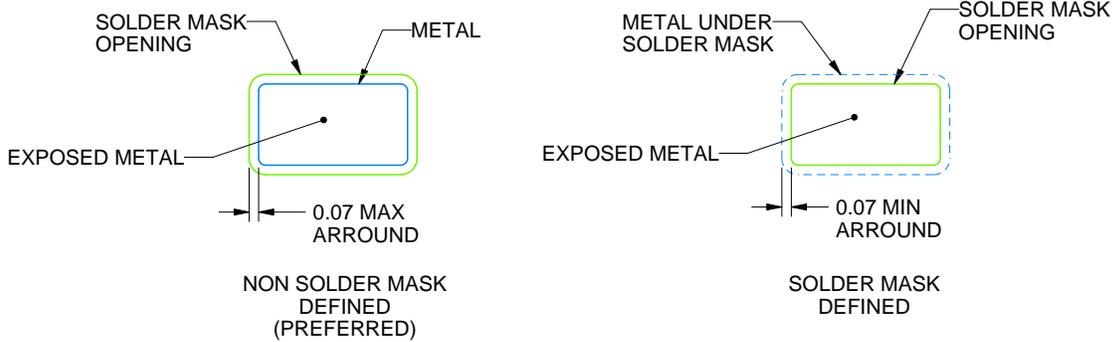
DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE:15X



SOLDER MASK DETAILS

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NOTES: (continued)

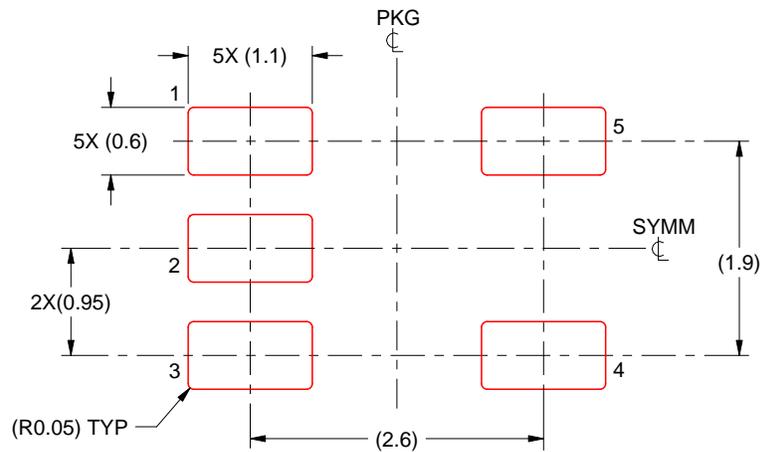
- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:15X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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