

SNx4AHC244 具有三态输出的八路缓冲器/驱动器

1 特性

- 在 2V 至 5.5V V_{CC} 范围内运行
- 门锁性能超过 250mA，符合 JESD 17 规范
- 对于符合 MIL-PRF-38535 标准的产品，所有参数均经过测试，除非另外注明。对于所有其他产品，生产流程不一定包含对所有参数的测试。

2 应用

- 网络交换机
- 电力基础设施
- PC 和笔记本电脑
- 可穿戴保健和健身设备
- 测试和测量

3 说明

这些八通道缓冲器和驱动器专门设计用于提高三态存储器地址驱动器、时钟驱动器以及总线导向接收器和发送器的性能和密度。

器件信息

| 器件型号 | 封装 ⁽¹⁾ | 封装尺寸 ⁽²⁾ | 本体尺寸 ⁽³⁾ |
|------------|--------------------|---------------------|---------------------|
| SN54AHC244 | J (CDIP , 20) | 24.2mm x 7.62mm | 24.2mm x 6.92mm |
| | W (CFP , 20) | 13.09mm x 8.13mm | 13.09mm x 6.92mm |
| | FK (LCCC , 20) | 8.89mm x 8.89mm | 8.89mm x 8.89mm |
| SN74AHC244 | DB (SSOP , 20) | 7.2mm x 7.8mm | 7.50mm x 5.30mm |
| | DW (SOIC , 20) | 12.80mm x 10.3mm | 12.8mm x 7.5mm |
| | N (PDIP , 20) | 24.33mm x 9.4mm | 25.40mm x 6.35mm |
| | NS (SOP , 20) | 12.60mm x 7.8mm | 12.6mm x 5.30mm |
| | DGV (TVSOP , 20) | 5.00mm x 6.4mm | 5.00mm x 4.40mm |
| | PW (TSSOP , 20) | 6.50mm x 6.4mm | 6.50mm x 4.40mm |

(1) 有关更多信息，请参阅节 11。

(2) 封装尺寸 (长 × 宽) 为标称值，并包括引脚 (如适用)。

(3) 本体尺寸 (长 × 宽) 为标称值，不包括引脚。

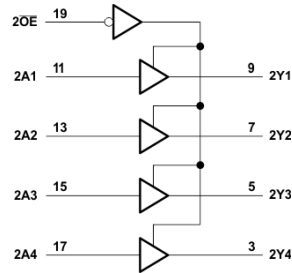
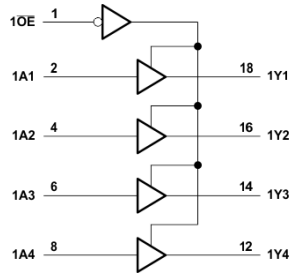
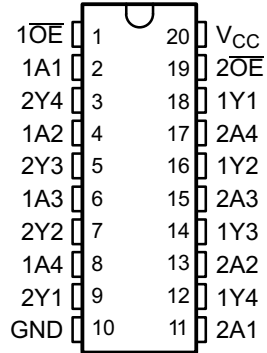


Table of Contents

| | | | |
|---|---|--|----|
| 1 特性 | 1 | 7.1 Overview..... | 9 |
| 2 应用 | 1 | 7.2 Functional Block Diagram..... | 9 |
| 3 说明 | 1 | 7.3 Feature Description..... | 9 |
| 4 Pin Configuration and Functions | 3 | 7.4 Device Functional Modes..... | 9 |
| 5 Specifications | 4 | 8 Application and Implementation | 10 |
| 5.1 Absolute Maximum Ratings..... | 4 | 8.1 Power Supply Recommendations..... | 10 |
| 5.2 ESD Ratings..... | 4 | 8.2 Layout..... | 10 |
| 5.3 Recommended Operating Conditions..... | 4 | 9 Device and Documentation Support | 11 |
| 5.4 Thermal Information..... | 5 | 9.1 Documentation Support..... | 11 |
| 5.5 Electrical Characteristics..... | 5 | 9.2 接收文档更新通知..... | 11 |
| 5.6 Switching Characteristics, $V_{CC} = 3.3V \pm 0.3V$ | 6 | 9.3 支持资源..... | 11 |
| 5.7 Switching Characteristics, $V_{CC} = 5V \pm 0.5V$ | 6 | 9.4 Trademarks..... | 11 |
| 5.8 Noise Characteristics..... | 7 | 9.5 静电放电警告..... | 11 |
| 5.9 Operating Characteristics..... | 7 | 9.6 术语表..... | 11 |
| 5.10 Typical Characteristics..... | 7 | 10 Revision History | 11 |
| 6 Parameter Measurement Information | 8 | 11 Mechanical, Packaging, and Orderable Information | 12 |
| 7 Detailed Description | 9 | | |

4 Pin Configuration and Functions

SN54AHC244 . . . J OR W PACKAGE
SN74AHC244 . . . DB, DGV, DW, N, NS, OR PW PACKAGE
(TOP VIEW)



SN54AHC244 . . . FK PACKAGE
(TOP VIEW)

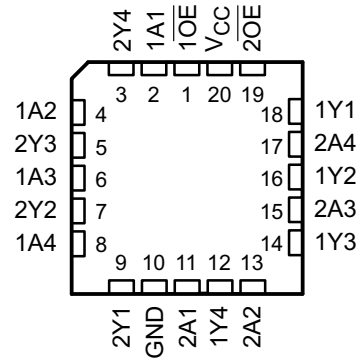


表 4-1. Pin Functions

| PIN | | I/O | DESCRIPTION |
|-----|-------------------|-----|-----------------|
| NO. | NAME | | |
| 1 | 1 \overline{OE} | I | Output Enable 1 |
| 2 | 1A1 | I | 1A1 Input |
| 3 | 2Y4 | O | 2Y4 Output |
| 4 | 1A2 | I | 1A2 Input |
| 5 | 2Y3 | O | 2Y3 Output |
| 6 | 1A3 | I | 1A3 Input |
| 7 | 2Y2 | O | 2Y2 Output |
| 8 | 1A4 | I | 1A4 Input |
| 9 | 2Y1 | O | 2Y1 Output |
| 10 | GND | — | Ground pin |
| 11 | 2A1 | I | 2A1 Input |
| 12 | 1Y4 | O | 1Y4 Output |
| 13 | 2A2 | I | 2A2 Input |
| 14 | 1Y3 | O | 1Y3 Output |
| 15 | 2A3 | I | 2A3 Input |
| 16 | 1Y2 | O | 1Y2 Output |
| 17 | 2A4 | I | 2A4 Input |
| 18 | 1Y1 | O | 1Y1 Output |
| 19 | 2 \overline{OE} | I | Output Enable 2 |
| 20 | VCC | — | Power Pin |

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

| | | MIN | MAX | UNIT |
|--|-------------------------------------|--|-----------------------|--------|
| V _{CC} | Supply voltage | -0.5 | 7 | V |
| V _I | Input voltage ⁽²⁾ | -0.5 | 7 | V |
| V _O | Output voltage range ⁽³⁾ | -0.5 | V _{CC} + 0.5 | V |
| I _{IK} | Input clamp current | V _I < 0 | | -20 mA |
| I _{OK} | Output clamp current | V _O < 0 or V _O > V _{CC} | | ±20 mA |
| I _O | Continuous output current | V _O = 0 to V _{CC} | | ±25 mA |
| Continuous current through each V _{CC} or GND | | | | ±50 mA |
| T _{stg} | Storage temperature | -65 | 150 | °C |

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
- (3) The package thermal impedance is calculated in accordance with JESD 51-7.

5.2 ESD Ratings

| | | VALUE | UNIT |
|--------------------|-------------------------|-------|------|
| V _(ESD) | Electrostatic discharge | ±2000 | V |
| | | ±1500 | |

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

| | | SN54AHC244 | | SN74AHC244 | | UNIT |
|-----------------|------------------------------------|---------------------------------|-----------------|------------|-----------------|------|
| | | MIN | MAX | MIN | MAX | |
| V _{CC} | Supply voltage | 2 | 5.5 | 2 | 5.5 | V |
| V _{IH} | High-level input voltage | V _{CC} = 2 V | | 1.5 | | V |
| | | V _{CC} = 3 V | | 2.1 | | |
| | | V _{CC} = 5.5 V | | 3.85 | | |
| V _{IL} | Low level input voltage | V _{CC} = 2 V | | 0.5 | | V |
| | | V _{CC} = 3 V | | 0.9 | | |
| | | V _{CC} = 5.5 V | | 1.65 | | |
| V _I | Input voltage | 0 | 5.5 | 0 | 5.5 | V |
| V _O | Output voltage | 0 | V _{CC} | 0 | V _{CC} | V |
| I _{OH} | High-level output current | V _{CC} = 2 V | | -50 | | μA |
| | | V _{CC} = 3.3 V ± 0.3 V | | -4 | | mA |
| | | V _{CC} = 5 V ± 0.5 V | | -8 | | |
| I _{OL} | Low level output current | V _{CC} = 2 V | | 50 | | μA |
| | | V _{CC} = 3.3 V ± 0.3 V | | 4 | | mA |
| | | V _{CC} = 5 V ± 0.5 V | | 8 | | |
| Δt/Δv | Input transition rise or fall rate | V _{CC} = 3.3 V ± 0.3 V | | 100 | | ns/V |
| | | V _{CC} = 5 V ± 0.5 V | | 20 | | |

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

| | | SN54AHC244 | | SN74AHC244 | | UNIT |
|----------------|--------------------------------|------------|-----|------------|-----|------|
| | | MIN | MAX | MIN | MAX | |
| T _A | Operating free-air temperature | -55 | 125 | -40 | 125 | °C |

(1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number [SCBA004](#).

5.4 Thermal Information

| THERMAL METRIC ⁽¹⁾ | SN74AHC244 | | | | | | UNIT | |
|-------------------------------|--|---------|---------|---------|---------|---------|-------|------|
| | DB | DGV | DW | N | NS | PW | | |
| | 20 PINS | 20 PINS | 20 PINS | 20 PINS | 20 PINS | 20 PINS | | |
| R _{θJA} | Junction-to-ambient thermal resistance | 99.9 | 119.2 | 81.1 | 54.9 | 77.6 | 116.8 | °C/W |
| R _{θJC(top)} | Junction-to-case (top) thermal resistance | 61.7 | 34.5 | 48.9 | 41.7 | 42.7 | 58.5 | |
| R _{θJB} | Junction-to-board thermal resistance | 55.2 | 60.7 | 53.8 | 35.8 | 45.7 | 78.7 | |
| ψ _{JT} | Junction-to-top characterization parameter | 22.6 | 1.2 | 19.5 | 27.9 | 10.2 | 12.6 | |
| ψ _{JB} | Junction-to-board characterization parameter | 54.8 | 60.0 | 53.1 | 35.7 | 45.2 | 77.9 | |
| R _{θJC(bot)} | Junction-to-case (bottom) thermal resistance | n/a | n/a | N/A | n/a | N/A | N/A | |

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, [SPRA953](#).

5.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | V _{CC} | T _A = 25°C | | | SN54AHC244 | | SN74AHC244 | | UNIT |
|-----------------|--|-----------------|-----------------------|-----|-------|-------------------|------|------------|-----|------|
| | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| V _{OH} | I _{OH} = -50 μA | 2 V | 1.9 | 2 | 1.9 | 1.9 | 1.9 | 1.9 | V | |
| | | 3 V | 2.9 | 3 | 2.9 | 2.9 | 2.9 | 2.9 | | |
| | | 4.5 V | 4.4 | 4.5 | 4.4 | 4.4 | 4.4 | 4.4 | | |
| | I _{OH} = -4 mA | 3 V | 2.58 | | 2.48 | 2.48 | 2.48 | 2.48 | | |
| | I _{OH} = -8 mA | 4.5 V | 3.94 | | 3.8 | 3.8 | 3.8 | 3.8 | | |
| V _{OL} | I _{OL} = 50 μA | 2 V | | | 0.1 | 0.1 | 0.1 | 0.1 | V | |
| | | 3 V | | | 0.1 | 0.1 | 0.1 | 0.1 | | |
| | | 4.5 V | | | 0.1 | 0.1 | 0.1 | 0.1 | | |
| | I _{OL} = 4 mA | 3 V | | | 0.36 | 0.5 | 0.44 | 0.44 | | |
| | I _{OL} = 8 mA | 4.5 V | | | 0.36 | 0.5 | 0.44 | 0.44 | | |
| I _I | V _I = 5.5 V or GND | 0 V to 5.5 V | | | ±0.1 | ±1 ⁽¹⁾ | ±1 | ±1 | μA | |
| I _{OZ} | V _O = V _{CC} or GND, V _I (OE) = V _{IL} or V _{IH} | 5.5 V | | | ±0.25 | ±2.5 | ±2.5 | ±2.5 | μA | |
| I _{CC} | V _I = V _{CC} or GND, I _O = 0 | 5.5 V | | | 4 | 40 | 40 | 40 | μA | |
| C _i | V _I = V _{CC} or GND | 5 V | | | 2 | 10 | | 10 | pF | |
| C _o | V _O = V _{CC} or GND | 5 V | | | 3.5 | | | | pF | |

(1) On products compliant to MIL-PRF-38535, this parameter is not production tested at V_{CC} = 0 V.

5.6 Switching Characteristics, $V_{CC} = 3.3V \pm 0.3V$

over recommended operating free-air temperature range, $V_{CC} = 3.3V \pm 0.3V$ (unless otherwise noted) (see [Load Circuit and Voltage Waveforms](#))

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | LOAD CAPACITANCE | $T_A = 25^\circ\text{C}$ | | | SN54AHC244 | | SN74AHC244 | | UNIT |
|-------------|-----------------|-------------|---------------------|--------------------------|---------------------|------------------|---------------------|-----|------------|-----|------|
| | | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| t_{PLH} | A | Y | $C_L = 15\text{pF}$ | 5.8 ⁽¹⁾ | 8.4 ⁽¹⁾ | 1 ⁽¹⁾ | 10 ⁽¹⁾ | 1 | 10 | ns | |
| t_{PHL} | | | | 5.8 ⁽¹⁾ | 8.4 ⁽¹⁾ | 1 ⁽¹⁾ | 10 ⁽¹⁾ | 1 | 10 | | |
| t_{PZH} | \overline{OE} | Y | $C_L = 15\text{pF}$ | 6.6 ⁽¹⁾ | 10.6 ⁽¹⁾ | 1 ⁽¹⁾ | 12.5 ⁽¹⁾ | 1 | 12.5 | ns | |
| t_{PZL} | | | | 6.6 ⁽¹⁾ | 10.6 ⁽¹⁾ | 1 ⁽¹⁾ | 12.5 ⁽¹⁾ | 1 | 12.5 | | |
| t_{PHZ} | \overline{OE} | Y | $C_L = 15\text{pF}$ | 5 ⁽¹⁾ | 9.7 ⁽¹⁾ | 1 ⁽¹⁾ | 11 ⁽¹⁾ | 1 | 11 | ns | |
| t_{PLZ} | | | | 5 ⁽¹⁾ | 9.7 ⁽¹⁾ | 1 ⁽¹⁾ | 11 ⁽¹⁾ | 1 | 11 | | |
| t_{PLH} | A | Y | $C_L = 50\text{pF}$ | 8.3 | 11.9 | 1 | 13.5 | 1 | 13.5 | ns | |
| t_{PHL} | | | | 8.3 | 11.9 | 1 | 13.5 | 1 | 13.5 | | |
| t_{PZH} | \overline{OE} | Y | $C_L = 50\text{pF}$ | 9.1 | 14.1 | 1 | 16 | 1 | 16 | ns | |
| t_{PZL} | | | | 9.1 | 14.1 | 1 | 16 | 1 | 16 | | |
| t_{PHZ} | \overline{OE} | Y | $C_L = 50\text{pF}$ | 10.3 | 14 | 1 | 16 | 1 | 16 | ns | |
| t_{PLZ} | | | | 10.3 | 14 | 1 | 16 | 1 | 16 | | |
| $t_{sk(o)}$ | | | $C_L = 50\text{pF}$ | | 1.5 ⁽²⁾ | | | | 1.5 | ns | |

(1) On products compliant to MIL-PRF-38535, this parameter is not production tested.

(2) On products compliant to MIL-PRF-38535, this parameter does not apply.

5.7 Switching Characteristics, $V_{CC} = 5V \pm 0.5V$

over recommended operating free-air temperature range, $V_{CC} = 5V \pm 0.5V$ (unless otherwise noted) (see [Load Circuit and Voltage Waveforms](#))

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | LOAD CAPACITANCE | $T_A = 25^\circ\text{C}$ | | | SN54AHC244 | | SN74AHC244 | | UNIT |
|-------------|-----------------|-------------|---------------------|--------------------------|--------------------|------------------|--------------------|-----|------------|-----|------|
| | | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| t_{PLH} | A | Y | $C_L = 15\text{pF}$ | 3.9 ⁽¹⁾ | 5.5 ⁽¹⁾ | 1 ⁽¹⁾ | 6.5 ⁽¹⁾ | 1 | 6.5 | ns | |
| t_{PHL} | | | | 3.9 ⁽¹⁾ | 5.5 ⁽¹⁾ | 1 ⁽¹⁾ | 6.5 ⁽¹⁾ | 1 | 6.5 | | |
| t_{PZH} | \overline{OE} | Y | $C_L = 15\text{pF}$ | 4.7 ⁽¹⁾ | 7.3 ⁽¹⁾ | 1 ⁽¹⁾ | 8.5 ⁽¹⁾ | 1 | 8.5 | ns | |
| t_{PZL} | | | | 4.7 ⁽¹⁾ | 7.3 ⁽¹⁾ | 1 ⁽¹⁾ | 8.5 ⁽¹⁾ | 1 | 8.5 | | |
| t_{PHZ} | \overline{OE} | Y | $C_L = 15\text{pF}$ | 5 ⁽¹⁾ | 7.2 ⁽¹⁾ | 1 ⁽¹⁾ | 8.5 ⁽¹⁾ | 1 | 8.5 | ns | |
| t_{PLZ} | | | | 5 ⁽¹⁾ | 7.2 ⁽¹⁾ | 1 ⁽¹⁾ | 8.5 ⁽¹⁾ | 1 | 8.5 | | |
| t_{PLH} | A | Y | $C_L = 50\text{pF}$ | 5.4 | 7.5 | 1 | 8.5 | 1 | 8.5 | ns | |
| t_{PHL} | | | | 5.4 | 7.5 | 1 | 8.5 | 1 | 8.5 | | |
| t_{PZH} | \overline{OE} | Y | $C_L = 50\text{pF}$ | 6.2 | 9.3 | 1 | 10.5 | 1 | 10.5 | ns | |
| t_{PZL} | | | | 6.2 | 9.3 | 1 | 10.5 | 1 | 10.5 | | |
| t_{PHZ} | \overline{OE} | Y | $C_L = 50\text{pF}$ | 6.7 | 9.2 | 1 | 10.5 | 1 | 10.5 | ns | |
| t_{PLZ} | | | | 6.7 | 9.2 | 1 | 10.5 | 1 | 10.5 | | |
| $t_{sk(o)}$ | | | $C_L = 50\text{pF}$ | | 1 ⁽²⁾ | | | | 1 | ns | |

(1) On products compliant to MIL-PRF-38535, this parameter is not production tested.

(2) On products compliant to MIL-PRF-38535, this parameter does not apply.

5.8 Noise Characteristics

$V_{CC} = 5\text{ V}$, $C_L = 50\text{ pF}$, $T_A = 25^\circ\text{C}$ (1)

| PARAMETER | | SN74AHC244 | | | UNIT |
|-------------|--|------------|------|-----|------|
| | | MIN | TYP | MAX | |
| $V_{OL(P)}$ | Quiet output, maximum dynamic V_{OL} | | 0.5 | | V |
| $V_{OL(V)}$ | Quiet output, minimum dynamic V_{OL} | | -0.2 | | V |
| $V_{OH(V)}$ | Quiet output, minimum dynamic V_{OH} | | 4.8 | | V |
| $V_{IH(D)}$ | High-level dynamic input voltage | 3.5 | | | V |
| $V_{IL(D)}$ | Low-level dynamic input voltage | | | 1.5 | V |

(1) Characteristics are for surface-mount packages only.

5.9 Operating Characteristics

$V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$

| PARAMETER | TEST CONDITIONS | TYP | UNIT |
|-----------|-----------------------------|-----|------|
| C_{pd} | No load, $f = 1\text{ MHz}$ | 8.6 | pF |

5.10 Typical Characteristics

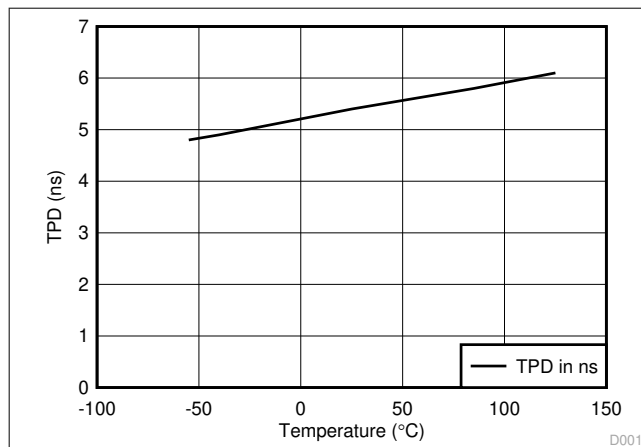


图 5-1. TPD vs Temperature

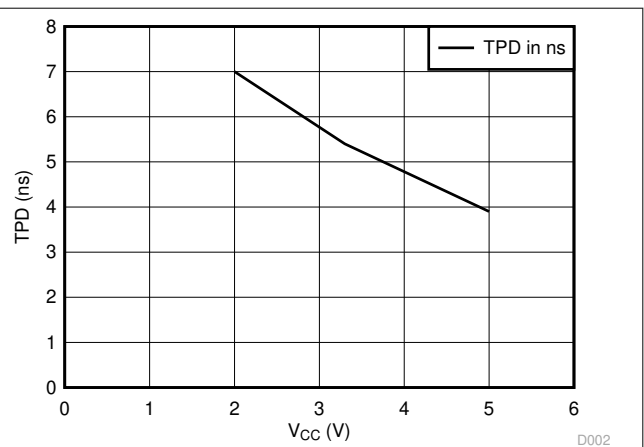
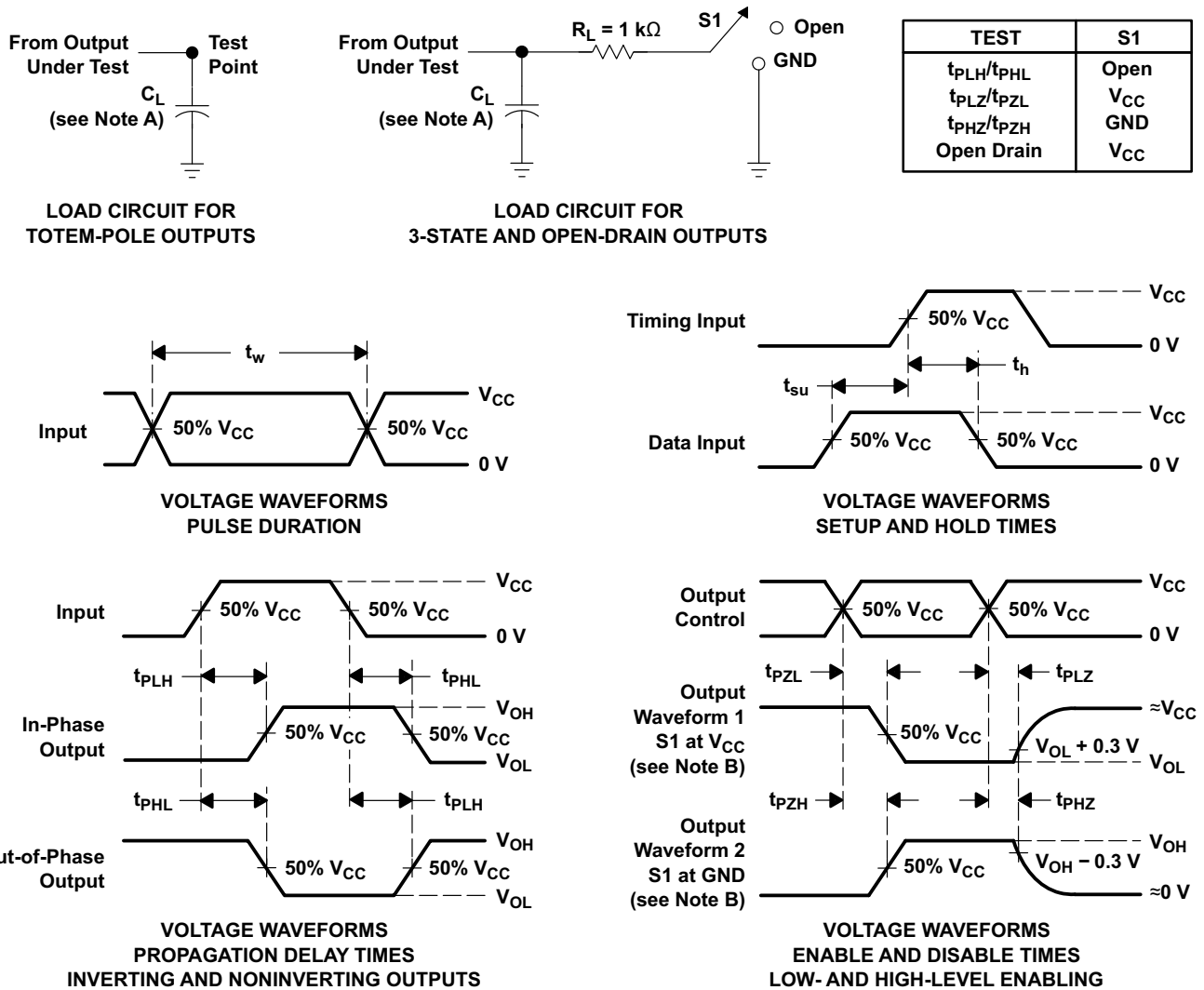


图 5-2. TPD vs V_{CC}

6 Parameter Measurement Information



- NOTES: A. C_L includes probe and jig capacitance.
 B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 1\text{ MHz}$, $Z_O = 50\ \Omega$, $t_r \leq 3\text{ ns}$, $t_f \leq 3\text{ ns}$.
 D. The outputs are measured one at a time with one input transition per measurement.
 E. All parameters and waveforms are not applicable to all devices.

图 6-1. Load Circuit and Voltage Waveforms

7 Detailed Description

7.1 Overview

The SNx4AHC244 devices are organized as two 4-bit buffers/line drivers with separate output-enable (\overline{OE}) inputs. When \overline{OE} is low, the device passes data from the A inputs to the Y outputs. When \overline{OE} is high, the outputs are in the high-impedance state. To ensure the high-impedance state during power up or power down, OE should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

7.2 Functional Block Diagram

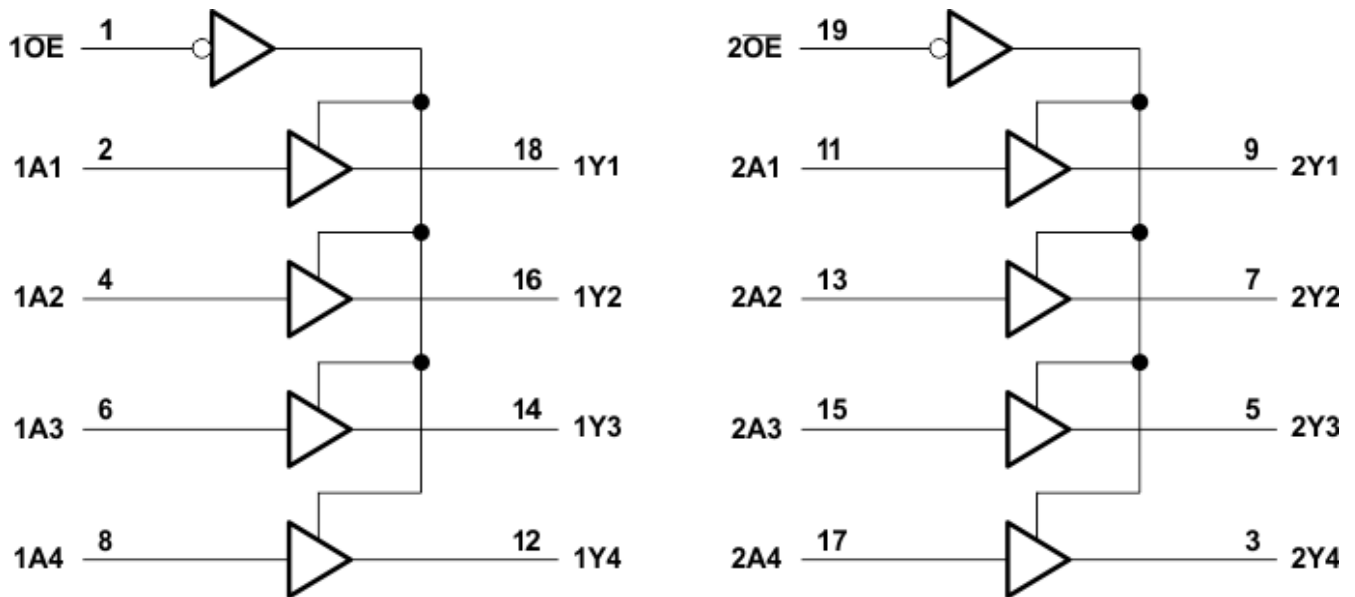


图 7-1. Logic Diagram (Positive Logic)

7.3 Feature Description

- V_{CC} is optimized at 5 V
- Allows down voltage translation
 - Inputs accept V_{IH} levels of 5.5 V
- Slow edge rates minimize output ringing

7.4 Device Functional Modes

表 7-1. Function Table
(Each 4-Bit Buffer/Driver)

| INPUTS | | OUTPUT Y |
|--------|---|-------------|
| OE | A | |
| L | H | H |
| L | L | L |
| H | X | Z |

8 Application and Implementation

备注

以下应用部分中的信息不属于 TI 器件规格的范围，TI 不担保其准确性和完整性。TI 的客户应负责确定器件是否适用于其应用。客户应验证并测试其设计，以确保系统功能。

8.1 Power Supply Recommendations

The power supply can be any voltage between the Min and Max supply voltage rating located in the [Recommended Operating Conditions](#) table.

Each V_{CC} pin should have a good bypass capacitor to prevent power disturbance. For devices with a single supply, 0.1 μF is recommended; if there are multiple V_{CC} pins, then 0.01 μF or 0.022 μF is recommended for each power pin. It is acceptable to parallel multiple bypass caps to reject different frequencies of noise. A 0.1 μF and a 1 μF are commonly used in parallel. The bypass capacitor should be installed as close to the power pin as possible for best results.

8.2 Layout

8.2.1 Layout Guidelines

When using multiple-bit logic devices, inputs should never float.

In many cases, functions or parts of functions of digital logic devices are unused, for example, when only two inputs of a triple-input AND gate are used or only 3 of the 4 buffer gates are used. Such input pins should not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. 图 8-1 specifies the rules that must be observed under all circumstances. All unused inputs of digital logic devices must be connected to a high or low bias to prevent them from floating. The logic level that should be applied to any particular unused input depends on the function of the device. Generally they will be tied to GND or V_{CC} , whichever makes more sense or is more convenient. It is generally acceptable to float outputs, unless the part is a transceiver. If the transceiver has an output enable pin, it will disable the output section of the part when asserted. This will not disable the input section of the I/Os, so they cannot float when disabled.

8.2.2 Layout Example

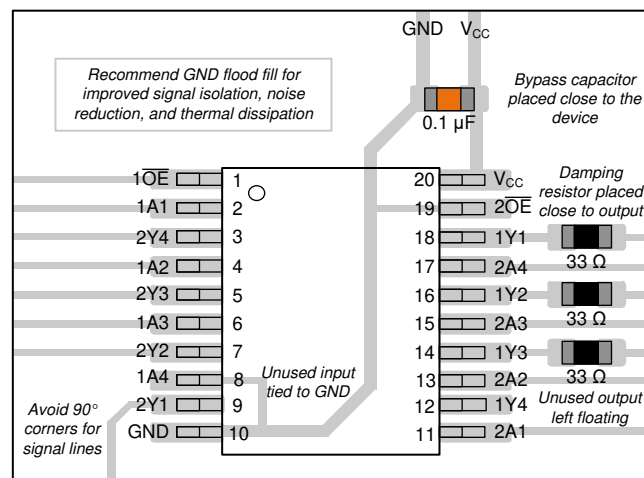


图 8-1. Example Layout for the SN74AHC244

9 Device and Documentation Support

9.1 Documentation Support

9.1.1 Related Documentation

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

表 9-1. Related Links

| PARTS | PRODUCT FOLDER | SAMPLE & BUY | TECHNICAL DOCUMENTS | TOOLS & SOFTWARE | SUPPORT & COMMUNITY |
|------------|----------------------------|----------------------------|----------------------------|----------------------------|----------------------------|
| SN54AHC244 | Click here | Click here | Click here | Click here | Click here |
| SN74AHC244 | Click here | Click here | Click here | Click here | Click here |

9.2 接收文档更新通知

要接收文档更新通知，请导航至 ti.com 上的器件产品文件夹。点击 [通知](#) 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

9.3 支持资源

[TI E2E™ 中文支持论坛](#) 是工程师的重要参考资料，可直接从专家处获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题，获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的 [使用条款](#)。

9.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.

所有商标均为其各自所有者的财产。

9.5 静电放电警告



静电放电 (ESD) 会损坏这个集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

9.6 术语表

[TI 术语表](#) 本术语表列出并解释了术语、首字母缩略词和定义。

10 Revision History

注：以前版本的页码可能与当前版本的页码不同

| Changes from Revision L (July 2024) to Revision M (January 2025) | Page |
|--|------|
| • Updated HBM and CDM values in <i>ESD Ratings</i> table..... | 4 |

| Changes from Revision K (July 2013) to Revision L (July 2024) | Page |
|---|------|
| • 根据当前标准更新了文档的结构布局..... | 1 |
| • 向 器件信息 表中添加了 SOP 和 TVSOP 封装、封装尺寸和军用级封装..... | 1 |
| • 删除了 器件信息 表中的 VQFN..... | 1 |
| • Updated RθJA values: PW = 105.4 to 116.8, DW = 83.0 to 81.1, NS = 80.4 to 77.6; Updated PW, DW, and NS packages for RθJC(top), RθJB, ΨJT, ΨJB, and RθJC(bot), all values in °C/W..... | 5 |

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead finish/ Ball material (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|------------------|---------------|--------------|-----------------|------|-------------|------------------|--------------------------------------|----------------------|--------------|-------------------------------------|-------------------------|
| 5962-9678201Q2A | ACTIVE | LCCC | FK | 20 | 55 | Non-RoHS & Green | SNPB | N / A for Pkg Type | -55 to 125 | 5962-9678201Q2A SNJ54AHC244FK | Samples |
| 5962-9678201QRA | ACTIVE | CDIP | J | 20 | 20 | Non-RoHS & Green | SNPB | N / A for Pkg Type | -55 to 125 | 5962-9678201QR A SNJ54AHC244J | Samples |
| 5962-9678201QSA | ACTIVE | CFP | W | 20 | 25 | Non-RoHS & Green | SNPB | N / A for Pkg Type | -55 to 125 | 5962-9678201QS A SNJ54AHC244W | Samples |
| 5962-9678201VRA | ACTIVE | CDIP | J | 20 | 20 | Non-RoHS & Green | SNPB | N / A for Pkg Type | -55 to 125 | 5962-9678201VR A SNV54AHC244J | Samples |
| 5962-9678201VSA | ACTIVE | CFP | W | 20 | 25 | Non-RoHS & Green | SNPB | N / A for Pkg Type | -55 to 125 | 5962-9678201VS A SNV54AHC244W | Samples |
| SN74AHC244DBR | ACTIVE | SSOP | DB | 20 | 2000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | HA244 | Samples |
| SN74AHC244DBRE4 | ACTIVE | SSOP | DB | 20 | 2000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | HA244 | Samples |
| SN74AHC244DGVR | ACTIVE | TVSOP | DGV | 20 | 2000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | HA244 | Samples |
| SN74AHC244DW | OBSOLETE | SOIC | DW | 20 | | TBD | Call TI | Call TI | -40 to 125 | AHC244 | |
| SN74AHC244DWR | ACTIVE | SOIC | DW | 20 | 2000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | AHC244 | Samples |
| SN74AHC244DWRG4 | ACTIVE | SOIC | DW | 20 | 2000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | AHC244 | Samples |
| SN74AHC244N | ACTIVE | PDIP | N | 20 | 20 | RoHS & Green | NIPDAU | N / A for Pkg Type | -40 to 125 | SN74AHC244N | Samples |
| SN74AHC244NSR | ACTIVE | SOP | NS | 20 | 2000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | AHC244 | Samples |
| SN74AHC244PW | OBSOLETE | TSSOP | PW | 20 | | TBD | Call TI | Call TI | -40 to 125 | HA244 | |
| SN74AHC244PWR | ACTIVE | TSSOP | PW | 20 | 2000 | RoHS & Green | NIPDAU SN | Level-1-260C-UNLIM | -40 to 85 | HA244 | Samples |
| SN74AHC244PWRE4 | ACTIVE | TSSOP | PW | 20 | 2000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | HA244 | Samples |

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead finish/ Ball material (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|------------------|---------------|--------------|-----------------|------|-------------|------------------|--------------------------------------|----------------------|--------------|-------------------------------------|-------------------------|
| SN74AHC244PWRG4 | ACTIVE | TSSOP | PW | 20 | 2000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | HA244 | Samples |
| SNJ54AHC244FK | ACTIVE | LCCC | FK | 20 | 55 | Non-RoHS & Green | SNPB | N / A for Pkg Type | -55 to 125 | 5962-9678201Q2A SNJ54AHC244FK | Samples |
| SNJ54AHC244J | ACTIVE | CDIP | J | 20 | 20 | Non-RoHS & Green | SNPB | N / A for Pkg Type | -55 to 125 | 5962-9678201QR A SNJ54AHC244J | Samples |
| SNJ54AHC244W | ACTIVE | CFP | W | 20 | 25 | Non-RoHS & Green | SNPB | N / A for Pkg Type | -55 to 125 | 5962-9678201QS A SNJ54AHC244W | Samples |

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer:The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF SN54AHC244, SN54AHC244-SP, SN74AHC244 :

- Catalog : [SN74AHC244](#), [SN54AHC244](#)

- Automotive : [SN74AHC244-Q1](#), [SN74AHC244-Q1](#)

- Enhanced Product : [SN74AHC244-EP](#), [SN74AHC244-EP](#)

- Military : [SN54AHC244](#)

- Space : [SN54AHC244-SP](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

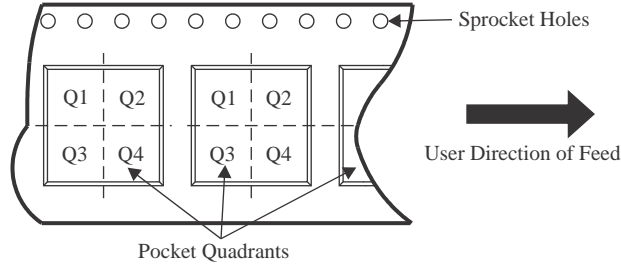
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

- Enhanced Product - Supports Defense, Aerospace and Medical Applications

- Military - QML certified for Military and Defense Applications

- Space - Radiation tolerant, ceramic packaging and qualified for use in Space-based application

TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|-----------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| SN74AHC244DBR | SSOP | DB | 20 | 2000 | 330.0 | 16.4 | 8.2 | 7.5 | 2.5 | 12.0 | 16.0 | Q1 |
| SN74AHC244DGVR | TVSOP | DGV | 20 | 2000 | 330.0 | 12.4 | 6.9 | 5.6 | 1.6 | 8.0 | 12.0 | Q1 |
| SN74AHC244DWR | SOIC | DW | 20 | 2000 | 330.0 | 24.4 | 10.8 | 13.3 | 2.7 | 12.0 | 24.0 | Q1 |
| SN74AHC244DWR | SOIC | DW | 20 | 2000 | 330.0 | 24.4 | 10.9 | 13.3 | 2.7 | 12.0 | 24.0 | Q1 |
| SN74AHC244NSR | SOP | NS | 20 | 2000 | 330.0 | 24.4 | 8.4 | 13.0 | 2.5 | 12.0 | 24.0 | Q1 |
| SN74AHC244NSR | SOP | NS | 20 | 2000 | 330.0 | 24.4 | 8.4 | 13.0 | 2.5 | 12.0 | 24.0 | Q1 |
| SN74AHC244PWR | TSSOP | PW | 20 | 2000 | 330.0 | 16.4 | 6.95 | 7.0 | 1.4 | 8.0 | 16.0 | Q1 |
| SN74AHC244PWR | TSSOP | PW | 20 | 2000 | 330.0 | 16.4 | 6.95 | 7.0 | 1.4 | 8.0 | 16.0 | Q1 |
| SN74AHC244PWRG4 | TSSOP | PW | 20 | 2000 | 330.0 | 16.4 | 6.95 | 7.0 | 1.4 | 8.0 | 16.0 | Q1 |
| SN74AHC244PWRG4 | TSSOP | PW | 20 | 2000 | 330.0 | 16.4 | 6.95 | 7.0 | 1.4 | 8.0 | 16.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|-----------------|--------------|-----------------|------|------|-------------|------------|-------------|
| SN74AHC244DBR | SSOP | DB | 20 | 2000 | 356.0 | 356.0 | 35.0 |
| SN74AHC244DGVR | TVSOP | DGV | 20 | 2000 | 356.0 | 356.0 | 35.0 |
| SN74AHC244DWR | SOIC | DW | 20 | 2000 | 356.0 | 356.0 | 45.0 |
| SN74AHC244DWR | SOIC | DW | 20 | 2000 | 367.0 | 367.0 | 45.0 |
| SN74AHC244NSR | SOP | NS | 20 | 2000 | 367.0 | 367.0 | 45.0 |
| SN74AHC244NSR | SOP | NS | 20 | 2000 | 356.0 | 356.0 | 45.0 |
| SN74AHC244PWR | TSSOP | PW | 20 | 2000 | 353.0 | 353.0 | 32.0 |
| SN74AHC244PWR | TSSOP | PW | 20 | 2000 | 356.0 | 356.0 | 35.0 |
| SN74AHC244PWRG4 | TSSOP | PW | 20 | 2000 | 353.0 | 353.0 | 32.0 |
| SN74AHC244PWRG4 | TSSOP | PW | 20 | 2000 | 367.0 | 367.0 | 38.0 |

TUBE


*All dimensions are nominal

| Device | Package Name | Package Type | Pins | SPQ | L (mm) | W (mm) | T (μm) | B (mm) |
|-----------------|--------------|--------------|------|-----|--------|--------|--------|--------|
| 5962-9678201Q2A | FK | LCCC | 20 | 55 | 506.98 | 12.06 | 2030 | NA |
| 5962-9678201QSA | W | CFP | 20 | 25 | 506.98 | 26.16 | 6220 | NA |
| 5962-9678201VSA | W | CFP | 20 | 25 | 506.98 | 26.16 | 6220 | NA |
| SN74AHC244N | N | PDIP | 20 | 20 | 506 | 13.97 | 11230 | 4.32 |
| SNJ54AHC244FK | FK | LCCC | 20 | 55 | 506.98 | 12.06 | 2030 | NA |
| SNJ54AHC244W | W | CFP | 20 | 25 | 506.98 | 26.16 | 6220 | NA |

W (R-GDFP-F20)

CERAMIC DUAL FLATPACK



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. This package can be hermetically sealed with a ceramic lid using glass frit.
 - D. Index point is provided on cap for terminal identification only.
 - E. Falls within Mil-Std 1835 GDFP2-F20

PW0020A



PACKAGE OUTLINE

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



4220206/A 02/2017

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

EXAMPLE BOARD LAYOUT

PW0020A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



SOLDER MASK DETAILS

4220206/A 02/2017

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

PW0020A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220206/A 02/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

DB0020A



PACKAGE OUTLINE

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



4214851/B 08/2019

EXAMPLE BOARD LAYOUT

DB0020A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



4214851/B 08/2019

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DB0020A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4214851/B 08/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

MECHANICAL DATA

NS (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

J (R-GDIP-T**)

14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



| DIM \ PINS ** | 14 | 16 | 18 | 20 |
|---------------|------------------------|------------------------|------------------------|------------------------|
| A | 0.300 (7,62) BSC | 0.300 (7,62) BSC | 0.300 (7,62) BSC | 0.300 (7,62) BSC |
| B MAX | 0.785 (19,94) | .840 (21,34) | 0.960 (24,38) | 1.060 (26,92) |
| B MIN | — | — | — | — |
| C MAX | 0.300 (7,62) | 0.300 (7,62) | 0.310 (7,87) | 0.300 (7,62) |
| C MIN | 0.245 (6,22) | 0.245 (6,22) | 0.220 (5,59) | 0.245 (6,22) |



4040083/F 03/03

- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. This package is hermetically sealed with a ceramic lid using glass frit.
 - D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
 - E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

DGV (R-PDSO-G**)

PLASTIC SMALL-OUTLINE

24 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.
 D. Falls within JEDEC: 24/48 Pins – MO-153
 14/16/20/56 Pins – MO-194

GENERIC PACKAGE VIEW

FK 20

LCCC - 2.03 mm max height

8.89 x 8.89, 1.27 mm pitch

LEADLESS CERAMIC CHIP CARRIER

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4229370VA\

N (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
 - The 20 pin end lead shoulder width is a vendor option, either half or full width.

DW0020A



PACKAGE OUTLINE SOIC - 2.65 mm max height

SOIC



NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm per side.
5. Reference JEDEC registration MS-013.

EXAMPLE BOARD LAYOUT

DW0020A

SOIC - 2.65 mm max height

SOIC



LAND PATTERN EXAMPLE
SCALE:6X



SOLDER MASK DETAILS

4220724/A 05/2016

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DW0020A

SOIC - 2.65 mm max height

SOIC



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

4220724/A 05/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

重要通知和免责声明

TI“按原样”提供技术和可靠性数据（包括数据表）、设计资源（包括参考设计）、应用或其他设计建议、网络工具、安全信息和其他资源，不保证没有瑕疵且不做任何明示或暗示的担保，包括但不限于对适销性、某特定用途方面的适用性或不侵犯任何第三方知识产权的暗示担保。

这些资源可供使用 TI 产品进行设计的熟练开发人员使用。您将自行承担以下全部责任：(1) 针对您的应用选择合适的 TI 产品，(2) 设计、验证并测试您的应用，(3) 确保您的应用满足相应标准以及任何其他功能安全、信息安全、监管或其他要求。

这些资源如有变更，恕不另行通知。TI 授权您仅可将这些资源用于研发本资源所述的 TI 产品的相关应用。严禁以其他方式对这些资源进行复制或展示。您无权使用任何其他 TI 知识产权或任何第三方知识产权。您应全额赔偿因在这些资源的使用中对 TI 及其代表造成的任何索赔、损害、成本、损失和债务，TI 对此概不负责。

TI 提供的产品受 [TI 的销售条款](#) 或 [ti.com](#) 上其他适用条款/TI 产品随附的其他适用条款的约束。TI 提供这些资源并不会扩展或以其他方式更改 TI 针对 TI 产品发布的适用的担保或担保免责声明。

TI 反对并拒绝您可能提出的任何其他或不同的条款。

邮寄地址：Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
版权所有 © 2025，德州仪器 (TI) 公司