

## SN74AHC541-Q1 具有三态输出的八路缓冲器/驱动器

### 1 特性

- 符合汽车应用要求
- 工作范围为 2V 至 5.5V  $V_{CC}$
- 闩锁性能超过 250mA，符合 JESD 17 规范

### 2 应用

- 启用或禁用数字信号
- 消除慢速或高噪声输入信号
- 在控制器复位期间保持信号
- 对开关进行去抖

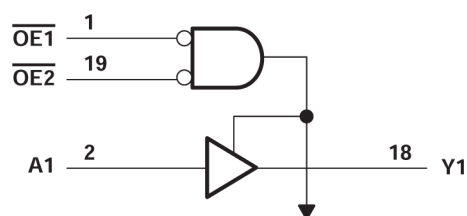
### 3 说明

SN74AHC541 八路缓冲器/驱动器非常适合用于驱动总线或缓冲存储器地址寄存器。该器件在封装的相对两侧具有输入端和输出端，有助于印刷电路板布局布线。

#### 封装信息

器件型号	封装 <sup>(1)</sup>	封装尺寸 <sup>(2)</sup>	本体尺寸 <sup>(3)</sup>
SN74AHC541-Q1	PW ( TSSOP , 20 )	6.5mm × 6.4mm	6.5mm × 4.4mm

- 有关更多信息，请参阅节 11。
- 封装尺寸 (长 × 宽) 为标称值，并包括引脚 (如适用)。
- 本体尺寸 (长 × 宽) 为标称值，不包括引脚。



To Seven Other Channels  
逻辑图 (正逻辑)



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## 4 Pin Configuration and Functions

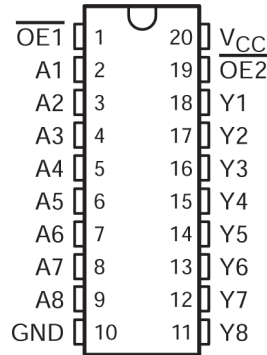


图 4-1. D or PW Package (Top View)

表 4-1. Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
OE1	1	I	Output Enable 1
A1	2	I	A1 Input
A2	3	I	A2 Input
A3	4	I	A3 Input
A4	5	I	A4 Input
A5	6	I	A5 Input
A6	7	I	A6 Input
A7	8	I	A7 Input
A8	9	I	A8 Input
GND	10	—	Ground
Y8	11	O	Y8 Output
Y7	12	O	Y7 Output
Y6	13	O	Y6 Output
Y5	14	O	Y4 Output
Y4	15	O	Y3 Output
Y3	16	O	Y2 Output
Y2	17	O	Y1 Output
Y1	18	O	Y1 Output
OE2	19	I	Output Enable 2
V <sub>CC</sub>	20	—	Power Pin

## 5 Specifications

### 5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

		MIN	MAX	UNIT
$V_{CC}$	Supply voltage range	-0.5	7	V
$V_I$ <sup>(2)</sup>	Input voltage range	-0.5	7	V
$V_O$ <sup>(2)</sup>	Output voltage range	-0.5	$V_{CC} + 0.5$	V
$I_{IK}$ ( $V_I < 0$ )	Input clamp current		-20	mA
$I_{OK}$ ( $V_O < 0$ or $V_O > V_{CC}$ )	Output clamp current		$\pm 20$	mA
$I_O$ ( $V_O = 0$ to $V_{CC}$ )	Continuous output current		$\pm 25$	mA
	Continuous current through $V_{CC}$ or GND		$\pm 75$	mA
$T_{stg}$	Storage temperature range	-65	150	°C

- (1) Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

### 5.2 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

		MIN	MAX	UNIT
$V_{CC}$	Supply voltage	2	5.5	V
$V_{IH}$	High-level input voltage	$V_{CC} = 2\text{ V}$	1.5	V
		$V_{CC} = 3\text{ V}$	2.1	
		$V_{CC} = 5.5\text{ V}$	3.85	
$V_{IL}$	Low-level input voltage	$V_{CC} = 2\text{ V}$	0.5	V
		$V_{CC} = 3\text{ V}$	0.9	
		$V_{CC} = 5.5\text{ V}$	1.65	
$V_I$	Input voltage	0	5.5	V
$V_O$	Output voltage	0	$V_{CC}$	V
$I_{OH}$	High-level output current	$V_{CC} = 2\text{ V}$	-50	mA
		$V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$	-4	
		$V_{CC} = 5\text{ V} \pm 0.5\text{ V}$	-8	
$I_{OL}$	Low-level output current	$V_{CC} = 2\text{ V}$	50	mA
		$V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$	4	
		$V_{CC} = 5\text{ V} \pm 0.5\text{ V}$	8	
$\Delta t/\Delta v$	Input transition rise or fall rate	$V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$	100	ns/V
		$V_{CC} = 5\text{ V} \pm 0.5\text{ V}$	20	
$T_A$	Operating free-air temperature	-40	125	°C

- (1) All unused inputs of the device must be held at  $V_{CC}$  or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

### 5.3 Thermal Information

THERMAL METRIC <sup>(1)</sup>		SN74AHC541-Q1		UNIT
		DW (SOIC)	PW (TSSOP)	
		20 PINS	20 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	58	116.8	°C/W

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, (SPRA953).

### 5.4 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	$V_{CC}$	$T_A = 25^\circ\text{C}$			$T_A = -40^\circ\text{C TO } 125^\circ\text{C}$		$T_A = -40^\circ\text{C TO } 85^\circ\text{C}$		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
$V_{OH}$	$I_{OH} = -50\text{ mA}$	2 V	1.9	2		1.9		1.9	V	
		3 V	2.9	3		2.9		2.9		
		4.5 V	4.4	4.5		4.4		4.4		
	$I_{OH} = -4\text{ mA}$	3 V	2.58		2.48		2.48			
	$I_{OH} = -8\text{ mA}$	4.5 V	3.94		3.8		3.8			
$V_{OL}$	$I_{OL} = 50\text{ mA}$	2 V			0.1		0.1		0.1	V
		3 V			0.1		0.1		0.1	
		4.5 V			0.1		0.1		0.1	
	$I_{OL} = 4\text{ mA}$	3 V		0.36		0.5		0.44		
	$I_{OL} = 8\text{ mA}$	4.5 V		0.36		0.5		0.44		
$I_I$	$V_I = 5.5\text{ V or GND}$	0 V to 5.5 V			$\pm 0.1$		$\pm 1$		$\pm 1$	$\mu\text{ A}$
$I_{OZ}$ <sup>(1)</sup>	$V_O = V_{CC}$ or GND, $V_I (\text{OE}) = V_{IL}$ or $V_{IH}$	5.5 V			$\pm 0.25$		$\pm 2.5$		$\pm 2.5$	$\mu\text{ A}$
$I_{CC}$	$V_I = V_{CC}$ or GND, $I_O = 0$	5.5 V			4		40		40	$\mu\text{ A}$
$C_i$	$V_I = V_{CC}$ or GND	5 V		2	10				10	pF
$C_o$	$V_O = V_{CC}$ or GND	5 V		4						pF

(1) For input and output,  $I_{OZ}$  includes the input leakage current.

### 5.5 Switching Characteristics, $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$

over recommended operating free-air temperature range,  $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$  (unless otherwise noted) (see 图 6-1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	$T_A = 25^\circ\text{C}$			$T_A = -40^\circ\text{C TO } 125^\circ\text{C}$		$T_A = -40^\circ\text{C TO } 85^\circ\text{C}$		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
$t_{PLH}$	A	Y	$C_L = 15\text{ pF}$	5	7		1	8.5	1	8.5	ns
$t_{PHL}$				5	7		1	8.5	1	8.5	
$t_{PZH}$	$\overline{\text{OE}}$	Y	$C_L = 15\text{ pF}$	6	10.5		1	11	1	11	ns
$t_{PZL}$				6	10.5		1	11	1	11	
$t_{PHZ}$	$\overline{\text{OE}}$	Y	$C_L = 15\text{ pF}$	7	11		1	12	1	12	ns
$t_{PLZ}$				7	11		1	12	1	12	
$t_{PLH}$	A	Y	$C_L = 50\text{ pF}$	7.5	10.5		1	12	1	12	ns
$t_{PHL}$				7.5	10.5		1	12	1	12	
$t_{PZH}$	$\overline{\text{OE}}$	Y	$C_L = 50\text{ pF}$	8	14		1	16	1	16	ns
$t_{PZL}$				8	14		1	16	1	16	
$t_{PHZ}$	$\overline{\text{OE}}$	Y	$C_L = 50\text{ pF}$	9	15.4		1	17.5	1	17.5	ns
$t_{PLZ}$				9	15.4		1	17.5	1	17.5	

over recommended operating free-air temperature range,  $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$  (unless otherwise noted) (see [图 6-1](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	$T_A = 25^\circ\text{C}$			$T_A = -40^\circ\text{C TO } 125^\circ\text{C}$		$T_A = -40^\circ\text{C TO } 85^\circ\text{C}$		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
tsk(o)			$C_L = 50\text{ pF}$			1.5				1.5	ns

## 5.6 Switching Characteristics, $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$

over recommended operating free-air temperature range,  $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$  (unless otherwise noted) (see [图 6-1](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	$T_A = 25^\circ\text{C}$			$T_A = -40^\circ\text{C TO } 125^\circ\text{C}$		$T_A = -40^\circ\text{C TO } 85^\circ\text{C}$		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
$t_{PLH}$	A	Y	$C_L = 15\text{ pF}$		3.5	5	1	6	1	6	ns
$t_{PHL}$					3.5	5	1	6	1	6	
$t_{PZH}$	$\overline{OE}$	Y	$C_L = 15\text{ pF}$		4.7	7.2	1	8.5	1	8.5	ns
$t_{PZL}$					4.7	7.2	1	8.5	1	8.5	
$t_{PHZ}$	$\overline{OE}$	Y	$C_L = 15\text{ pF}$		5	7.5	1	8	1	8	ns
$t_{PLZ}$					5	7.5	1	8	1	8	
$t_{PLH}$	A	Y	$C_L = 50\text{ pF}$		5	7	1	8	1	8	ns
$t_{PHL}$					5	7	1	8	1	8	
$t_{PZH}$	$\overline{OE}$	Y	$C_L = 50\text{ pF}$		6.2	9.2	1	10.5	1	10.5	ns
$t_{PZL}$					6.2	9.2	1	10.5	1	10.5	
$t_{PHZ}$	$\overline{OE}$	Y	$C_L = 50\text{ pF}$		6	8.8	1	10	1	10	ns
$t_{PLZ}$					6	8.8	1	10	1	10	
tsk(o)			$C_L = 50\text{ pF}$			1			1	ns	

## 5.7 Noise Characteristics

$V_{CC} = 5\text{ V}$ ,  $C_L = 50\text{ pF}$ ,  $T_A = 25^\circ\text{C}$  <sup>(1)</sup>

PARAMETER	DESCRIPTION	MIN	MAX	UNIT
$V_{OL(P)}$	Quiet output, maximum dynamic $V_{OL}$		0.8	V
$V_{OL(V)}$	Quiet output, minimum dynamic $V_{OL}$		-0.8	V
$V_{OH(V)}$	Quiet output, minimum dynamic $V_{OH}$	4.7		V
$V_{IH(D)}$	High-level dynamic input voltage	3.5		V
$V_{IL(D)}$	Low-level dynamic input voltage		1.5	V

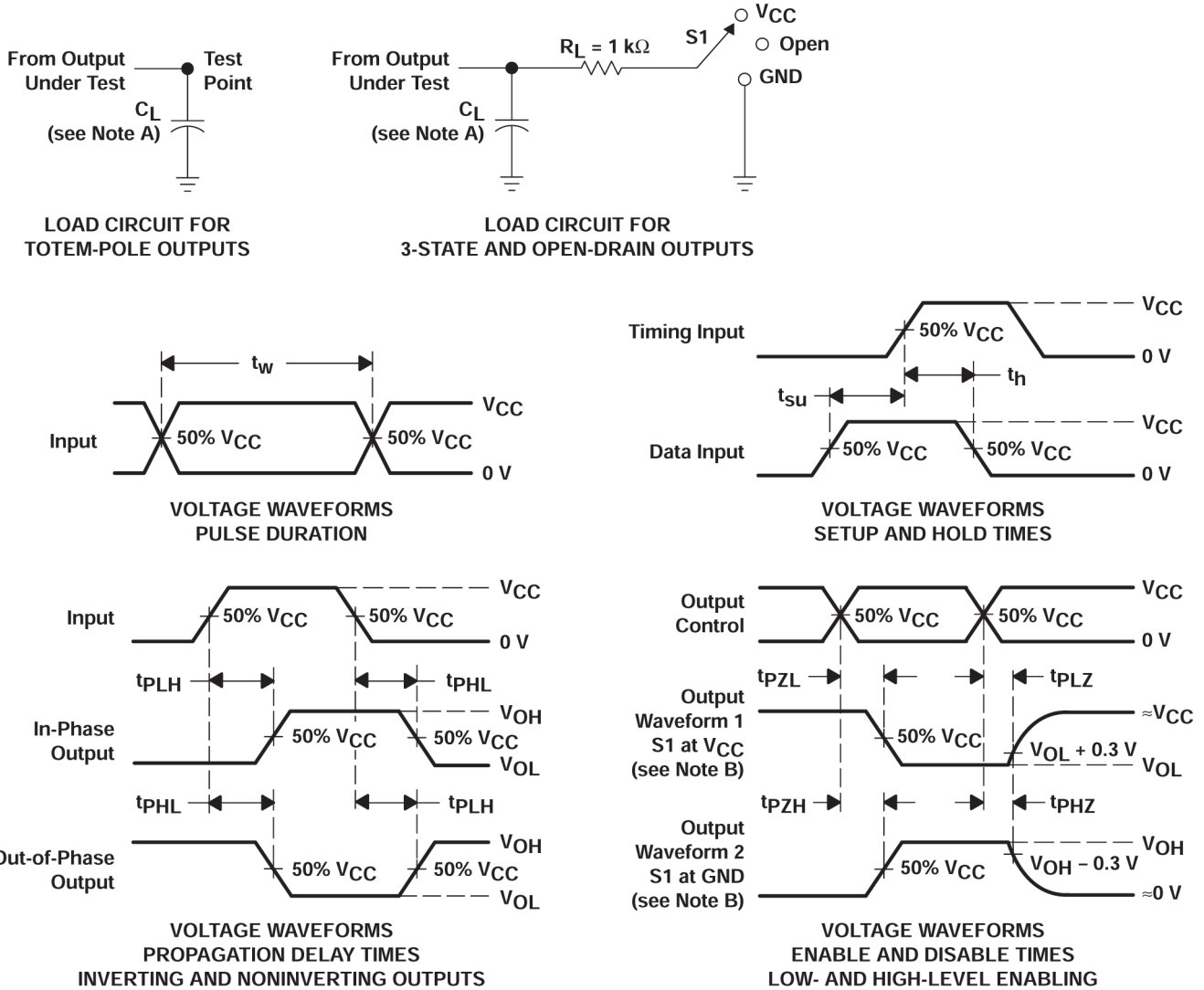
(1) Characteristics are for surface-mount packages only.

## 5.8 Operating Characteristics

$V_{CC} = 5\text{ V}$ ,  $T_A = 25^\circ\text{C}$

PARAMETER	DESCRIPTION	TEST CONDITIONS	TYP	UNIT
$C_{pd}$	Power dissipation capacitance	No load, $f = 1\text{ MHz}$	12	pF

## 6 Parameter Measurement Information



- A.  $C_L$  includes probe and jig capacitance.
- B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 1$  MHz,  $Z_O = 50 \Omega$ ,  $t_r \leq 3$  ns,  $t_f \leq 3$  ns.
- D. The outputs are measured one at a time, with one input transition per measurement.
- E. All parameters and waveforms are not applicable to all devices.

图 6-1. Load Circuit and Voltage Waveforms

TEST	S1
$t_{PLH}/t_{PHL}$	Open
$t_{PLZ}/t_{PZL}$	$V_{CC}$
$t_{PHZ}/t_{PZH}$	GND
Open Drain	$V_{CC}$

## 7 Detailed Description

### 7.1 Overview

The 3-state control gate is a two-input AND gate with active-low inputs so that if either output-enable ( $\overline{OE1}$  or  $\overline{OE2}$ ) input is high, all corresponding outputs are in the high-impedance state. The outputs provide noninverted data when they are not in the high-impedance state.

To ensure the high-impedance state during power up or power down,  $\overline{OE}$  should be tied to  $V_{CC}$  through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

### 7.2 Functional Block Diagram

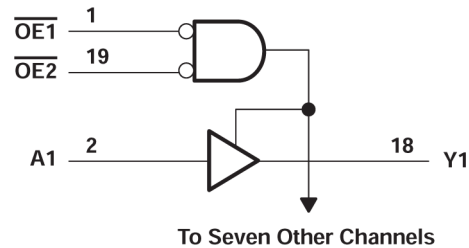


图 7-1. Logic Diagram (Positive Logic)

### 7.3 Device Functional Modes

表 7-1. (Each Buffer/Driver)

INPUTS			OUTPUT
$\overline{OE1}$	$\overline{OE2}$	A	Y
L	L	L	L
L	L	H	H
H	X	X	Z
X	H	X	Z



## 8 Application and Implementation

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### 备注

以下应用部分中的信息不属于 TI 器件规格的范围，TI 不担保其准确性和完整性。TI 的客户应负责确定器件是否适用于其应用。客户应验证并测试其设计，以确保系统功能。

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### 8.1 Power Supply Recommendations

The power supply can be any voltage between the MIN and MAX supply voltage rating located in the [Recommended Operating Conditions](#) table.

Each  $V_{CC}$  pin should have a good bypass capacitor to prevent power disturbance. For devices with a single supply, 0.1  $\mu$ F is recommended. If there are multiple  $V_{CC}$  pins, 0.01  $\mu$ F or 0.022  $\mu$ F is recommended for each power pin. It is acceptable to parallel multiple bypass caps to reject different frequencies of noise. A 0.1  $\mu$ F and 1  $\mu$ F are commonly used in parallel. The bypass capacitor should be installed as close to the power pin as possible for best results.

### 8.2 Layout

#### 8.2.1 Layout Guidelines

When using multiple bit logic devices inputs should not ever float.

In many cases, functions or parts of functions of digital logic devices are unused, for example, when only two inputs of a triple-input AND gate are used or only 3 of the 4 buffer gates are used. Such input pins should not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. Specified in [Layout Diagram](#) are the rules that must be observed under all circumstances. All unused inputs of digital logic devices must be connected to a high or low bias to prevent them from floating. The logic level that should be applied to any particular unused input depends on the function of the device. Generally they will be tied to GND or  $V_{CC}$ ; whichever makes more sense or is more convenient. It is generally acceptable to float outputs unless the part is a transceiver. If the transceiver has an output enable pin, it will disable the outputs section of the part when asserted. This will not disable the input section of the IOs, so they cannot float when disabled.

8.2.1.1 Layout Example

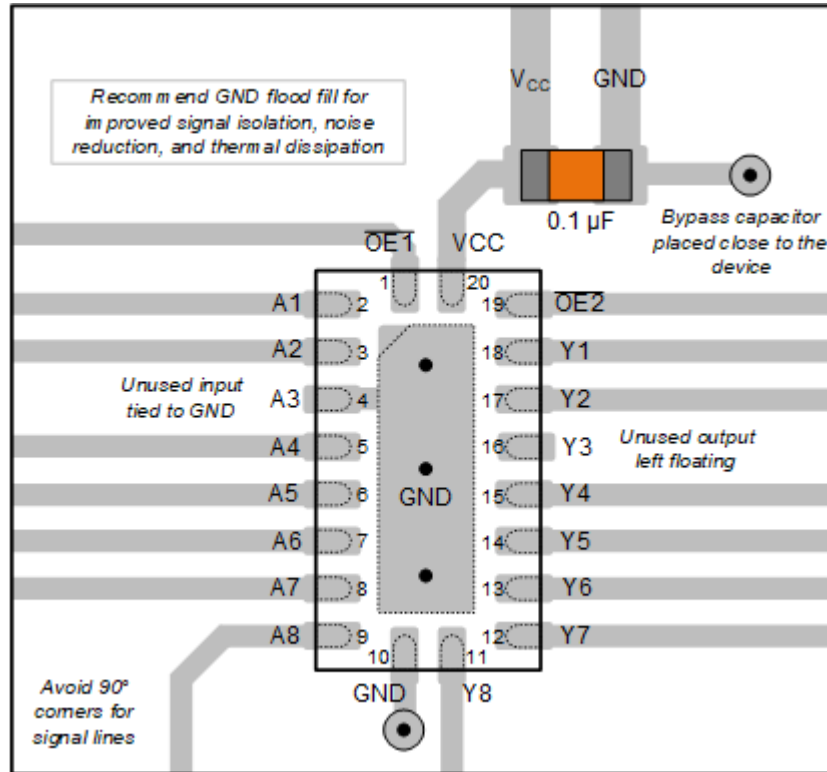


图 8-1. Layout Diagram

## 9 Device and Documentation Support

### 9.1 Document Support (Analog)

#### 9.1.1 Related Documentation

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

**表 9-1. Related Links**

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
SN74AHC541-Q1	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>

### 9.2 接收文档更新通知

要接收文档更新通知，请导航至 [ti.com](https://www.ti.com) 上的器件产品文件夹。点击 [通知](#) 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

### 9.3 支持资源

[TI E2E™ 中文支持论坛](#) 是工程师的重要参考资料，可直接从专家处获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题，获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的 [使用条款](#)。

### 9.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.

所有商标均为其各自所有者的财产。

### 9.5 静电放电警告



静电放电 (ESD) 会损坏这个集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

### 9.6 术语表

[TI 术语表](#) 本术语表列出并解释了术语、首字母缩略词和定义。

## 10 Revision History

注：以前版本的页码可能与当前版本的页码不同

Changes from Revision B (April 2023) to Revision C (July 2024)	Page
• Updated thermal values for PW package from $R_{\theta JA} = 58$ to 116.8, all values in °C/W .....	5

Changes from Revision A (April 2008) to Revision B (April 2023)	Page
• 添加了应用、封装信息表、引脚功能表、ESD 等级表、热性能信息表、器件功能模式、应用和实施部分、电源相关建议部分、布局部分、器件和文档支持部分以及机械、封装和可订购信息部分 .....	1

## 11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74AHC541QPWRG4Q1	ACTIVE	TSSOP	PW	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	AHC541Q	<a href="#">Samples</a>
SN74AHC541QPWRQ1	ACTIVE	TSSOP	PW	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	AHC541Q	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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**OTHER QUALIFIED VERSIONS OF SN74AHC541-Q1 :**

- Catalog : [SN74AHC541](#)
- Military : [SN54AHC541](#)

## NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74AHC541QPWRG4Q1	TSSOP	PW	20	2000	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1
SN74AHC541QPWRQ1	TSSOP	PW	20	2000	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74AHC541QPWRG4Q1	TSSOP	PW	20	2000	356.0	356.0	35.0
SN74AHC541QPWRQ1	TSSOP	PW	20	2000	356.0	356.0	35.0



# PW0020A



# PACKAGE OUTLINE

## TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



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### NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

# EXAMPLE BOARD LAYOUT

PW0020A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 10X



SOLDER MASK DETAILS

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NOTES: (continued)

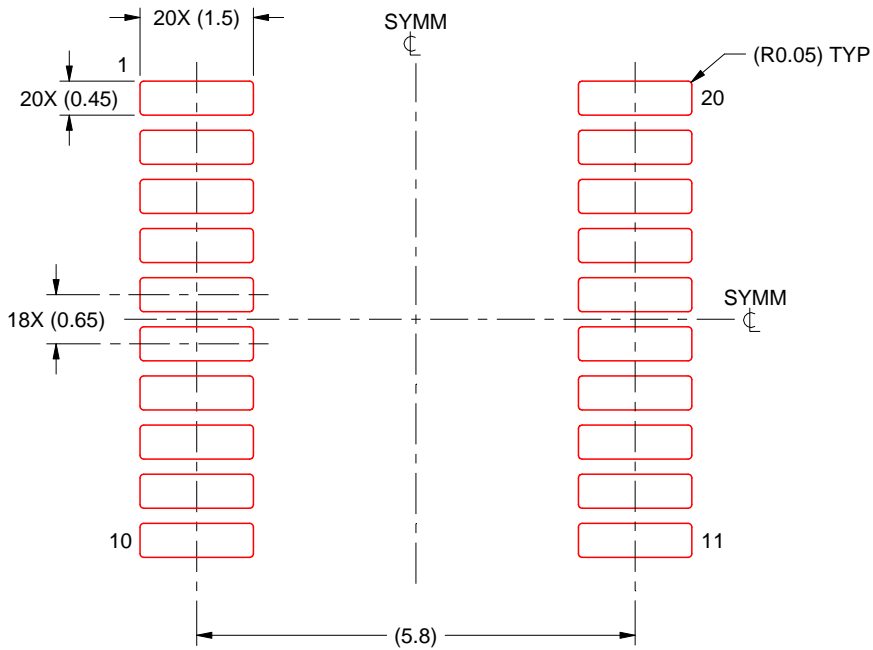
- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

PW0020A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE: 10X

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NOTES: (continued)

- 8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 9. Board assembly site may have different recommendations for stencil design.

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