

SN74AHCT1G125-Q1 具有三态输出的汽车类单路总线缓冲门

1 特性

- 符合汽车应用要求
- 工作电压范围为 3V 至 5.5V
- t_{pd} 最大值为 6ns (5V 时)
- 低功耗, I_{CC} 最大值为 10 μ A
- 5V 下的输出驱动为 ± 8 mA
- 输入兼容 TTL 电压

2 应用

- [启用或禁用数字信号](#)
- [控制指示灯 LED](#)
- [通信模块和系统控制器之间的转换](#)

3 说明

SN74AHCT1G125-Q1 是一款具有三态输出的单通道总线缓冲门/线路驱动器。当输出使能 (\overline{OE}) 输入为高电平时, 该输出被禁用。当 \overline{OE} 为低电平时, 真实数据从 A 输入传递到 Y 输出。

封装信息

器件型号	封装 ⁽¹⁾	封装尺寸 ⁽²⁾	本体尺寸 ⁽³⁾
SN74AHCT1G125-Q1	DBV (SOT-23, 5)	2.9mm × 2.8mm	2.9mm × 1.6mm
	DCK (SC70, 5)	2.0mm × 2.1mm	2mm × 1.25mm
	DTX (X2SON, 5)	1.1mm × 0.85mm	1.1mm × 0.85mm

- (1) 如需了解更多信息, 请参阅[机械、封装和可订购信息](#)。
- (2) 封装尺寸 (长 × 宽) 为标称值, 并包括引脚 (如适用)。
- (3) 本体尺寸 (长 × 宽) 为标称值, 不包括引脚。

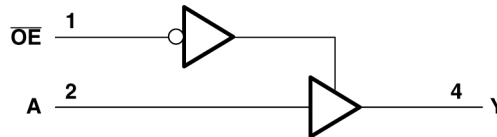


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4 Pin Configuration and Functions

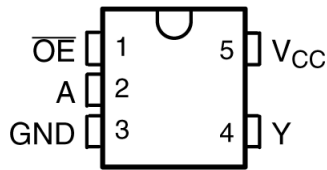


图 4-1. DBV Package, 5-Pin SOT-23; DCK Package (Top View)

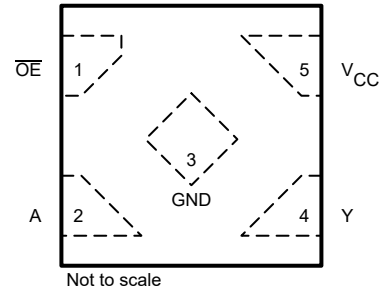


图 4-2. DTX Package, 5-Pin X2SON (Top View)

表 4-1. Pin Functions

PIN		TYPE ⁽¹⁾	DESCRIPTION
NO.	NAME		
1	\overline{OE}	I	Output Enable
2	A	I	Input A
3	GND	—	Ground Pin
4	Y	O	Output Y
5	V _{CC}	—	Power Pin

(1) Signal Types: I = Input, O = Output, I/O = Input or Output

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) ⁽¹⁾

		MIN	MAX	UNIT
V_{CC}	Supply voltage range	- 0.5	7	V
V_I ⁽²⁾	Input voltage range	- 0.5	7	V
V_O ⁽²⁾	Output voltage range	- 0.5	$V_{CC} + 0.5$	V
I_{IK}	Input clamp current	$(V_I < 0)$		- 20 mA
I_{OK}	Output clamp current	$(V_O < 0 \text{ or } V_O > V_{CC})$		± 20 mA
I_O	Continuous output current	$(V_O = 0 \text{ to } V_{CC})$		± 25 mA
	Continuous current through V_{CC} or GND			± 50 mA
T_{stg}	Storage temperature range	- 65	150	$^{\circ}\text{C}$

- (1) Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

5.2 ESD Ratings

		VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per AEC Q100-002 ⁽¹⁾	± 2000 V

- (1) AEC Q100-002 indicates that HBM stressing must be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

		MIN	MAX	UNIT
V_{CC}	Supply voltage	3	5.5	V
V_{IH}	High-level input voltage	$V_{CC} = 3.0 \text{ V}$	1.4	V
		$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$	2	
V_{IL}	Low-level input voltage	$V_{CC} = 3.0 \text{ V}$	0.53	V
		$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$	0.8	
V_I	Input voltage	0	5.5	V
V_O	Output voltage	0	V_{CC}	V
I_{OH}	High-level output current		- 8	mA
I_{OL}	Low-level output current		8	mA
$\Delta t / \Delta v$	Input transition rise or fall rate		20	ns/V
T_A	Operating free-air temperature	- 40	125	$^{\circ}\text{C}$

- (1) All unused inputs of the device must be held at V_{CC} or GND for specified device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

5.4 Thermal Information

THERMAL METRIC ⁽¹⁾		SN74AHCT1G125-Q1			UNIT
		DBV (SOT-23)	DCK (SC-70)	DTX (X2SON)	
		5	5	5	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	278.0	293.4	184.7	°C/W

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report (SPRA953).

5.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	$T_A = 25^\circ\text{C}$			MIN	MAX	UNIT
			MIN	TYP	MAX			
V_{OH}	$I_{OH} = -50 \mu\text{A}$	3 V	2.9	3		2.9	V	
		4.5 V	4.4	4.5		4.4		
	$I_{OH} = -4 \text{ mA}$	3 V	2.58			2.34		
		4.5 V	3.94			3.66		
V_{OL}	$I_{OL} = 50 \mu\text{A}$	3 V and 4.5 V	0.1			0.1	V	
	$I_{OL} = 4 \text{ mA}$	3 V	0.36			0.52		
	$I_{OL} = 8 \text{ mA}$	4.5 V	0.36			0.52		
I_I	$V_I = 5.5 \text{ V or GND}$	0 V to 5.5 V	± 0.1			± 1	μA	
I_{OZ}	$V_O = V_{CC} \text{ or GND}$	5.5 V	± 0.25			± 2.5	μA	
I_{CC}	$V_I = V_{CC} \text{ or GND, } I_O = 0,$ OE high or low	3 V and 5.5 V	1			10	μA	
$\Delta I_{CC}^{(1)}$	One input at 3.4 V, Other input at V_{CC} or GND	5.5 V	1.35			1.5	mA	
C_i	$V_I = V_{CC} \text{ or GND}$	5 V	4 10			10	pF	
C_o	$V_O = V_{CC} \text{ or GND}$	5 V	10				pF	

(1) This is the increase in supply current for each input at one of the specified TTL voltage levels, rather than 0 V or V_{CC} .

5.6 Switching Characteristics, $V_{CC} = 3\text{ V} \pm 0.3\text{ V}$

over recommended operating free-air temperature range, $V_{CC} = 3\text{ V} \pm 0.3\text{ V}$ (unless otherwise noted) (see [Load Circuit and Voltage Waveforms](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	$T_A = 25^\circ\text{C}$			MIN	MAX	UNIT
				MIN	TYP	MAX			
t_{PLH}	A	Y	$C_L = 15\text{ pF}$		5.6	8		12	ns
t_{PHL}					5.6	8		12	
t_{PZH}	$\overline{\text{OE}}$	Y	$C_L = 15\text{ pF}$		5.4	8		11.5	ns
t_{PZL}					5.4	8		11.5	
t_{PHZ}	$\overline{\text{OE}}$	Y	$C_L = 15\text{ pF}$		6.5	9.7		14.5	ns
t_{PLZ}					6.5	9.7		14.5	
t_{PLH}	A	Y	$C_L = 50\text{ pF}$		8.1	11.5		16	ns
t_{PHL}					8.1	11.5		16	
t_{PZH}	$\overline{\text{OE}}$	Y	$C_L = 50\text{ pF}$		7.9	11.5		15	ns
t_{PZL}					7.9	11.5		15	
t_{PHZ}	$\overline{\text{OE}}$	Y	$C_L = 50\text{ pF}$		8	13.2		18	ns
t_{PLZ}					8	13.2		18	

5.7 Switching Characteristics, $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$

over recommended operating free-air temperature range, $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$ (unless otherwise noted) (see [Load Circuit and Voltage Waveforms](#))

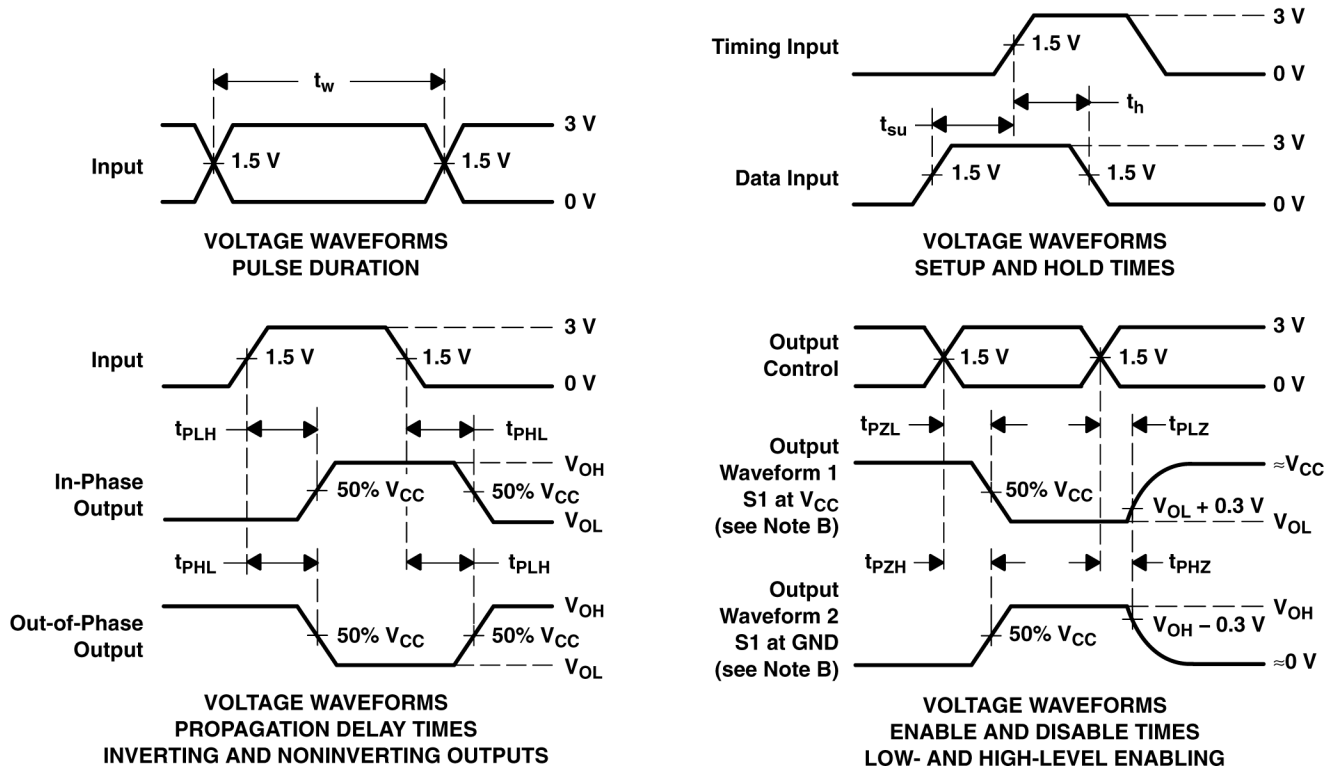
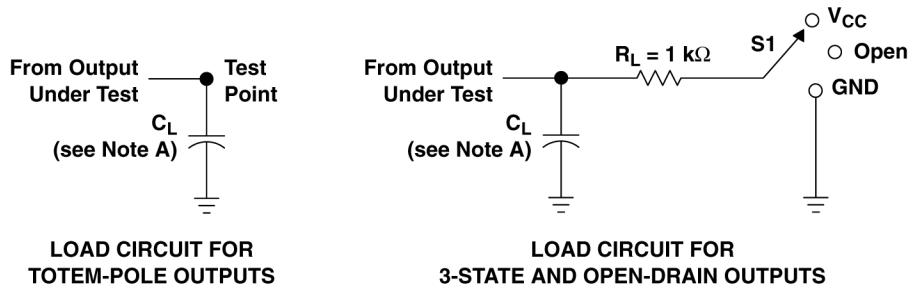
PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	$T_A = 25^\circ\text{C}$			MIN	MAX	UNIT
				MIN	TYP	MAX			
t_{PLH}	A	Y	$C_L = 15\text{ pF}$		3.8	5.5		8.5	ns
t_{PHL}					3.8	5.5		8.5	
t_{PZH}	$\overline{\text{OE}}$	Y	$C_L = 15\text{ pF}$		3.6	5.1		7.5	ns
t_{PZL}					3.6	5.1		7.5	
t_{PHZ}	$\overline{\text{OE}}$	Y	$C_L = 15\text{ pF}$		4.8	6.8		10	ns
t_{PLZ}					4.8	6.8		10	
t_{PLH}	A	Y	$C_L = 50\text{ pF}$		5.3	7.5		10.5	ns
t_{PHL}					5.3	7.5		10.5	
t_{PZH}	$\overline{\text{OE}}$	Y	$C_L = 50\text{ pF}$		5.1	7.1		9.5	ns
t_{PZL}					5.1	7.1		9.5	
t_{PHZ}	$\overline{\text{OE}}$	Y	$C_L = 50\text{ pF}$		7	8.8		12	ns
t_{PLZ}					7	8.8		12	

5.8 Operating Characteristics

$V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$

PARAMETER	TEST CONDITIONS	TYP	UNIT
C_{pd} Power dissipation capacitance	No load, $f = 1\text{ MHz}$	14	pF

6 Parameter Measurement Information



- A. C_L includes probe and jig capacitance.
- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 1\text{ MHz}$, $Z_O = 50\ \Omega$, $t_r \leq 3\text{ ns}$, $t_f \leq 3\text{ ns}$.
- D. The outputs are measured one at a time with one input transition per measurement.
- E. All parameters and waveforms are not applicable to all devices.

图 6-1. Load Circuit and Voltage Waveforms

TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	V_{CC}
t_{PHZ}/t_{PZH}	GND
Open Drain	V_{CC}

7 Detailed Description

7.1 Overview

For specified high-impedance state during power up or power down, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

7.2 Functional Block Diagram

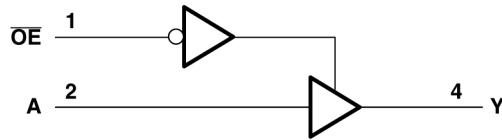


图 7-1. Logic Diagram (Positive Logic)

7.3 Device Functional Modes

表 7-1. Function Table

INPUTS		OUTPUT
\overline{OE}	A	Y
L	H	H
L	L	L
H	X	Z

8 Application and Implementation

备注

以下应用部分中的信息不属于 TI 元件规格，TI 不担保其准确性和完整性。TI 的客户负责确定元件是否适合其用途，以及验证和测试其设计实现以确认系统功能。

8.1 Application Information

In this application, three 2-input AND gates are combined to produce a 4-input AND gate function as shown in [图 8-1](#). The fourth gate can be used for another application in the system, or the inputs can be grounded and the channel left unused.

The SN74AHCT1G125-Q1 is used to directly control the $\overline{\text{RESET}}$ pin of a motor controller. The controller requires four input signals to all be HIGH before being enabled, and should be disabled in the event that any one signal goes LOW. The 4-input AND gate function combines the four individual reset signals into a single active-low reset signal.

8.2 Typical Application

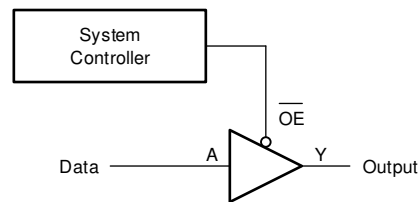


图 8-1. Typical Application Block Diagram

8.3 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in the *Recommended Operating Conditions*. Each V_{CC} terminal should have a good bypass capacitor to prevent power disturbance. A 0.1- μF capacitor is recommended for this device. It is acceptable to parallel multiple bypass capacitors to reject different frequencies of noise. The 0.1- μF and 1- μF capacitors are commonly used in parallel. The bypass capacitor should be installed as close to the power terminal as possible for best results, as shown in the following layout example.

8.4 Layout

8.4.1 Layout Guidelines

When using multiple-input and multiple-channel logic devices, inputs must never be left floating. In many cases, functions or parts of functions of digital logic devices are unused (for example, when only two inputs of a triple-input AND gate are used or only 3 of the 4 buffer gates are used). Such unused input pins must not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. All unused inputs of digital logic devices must be connected to a logic high or logic low voltage, as defined by the input voltage specifications, to prevent them from floating. The logic level that must be applied to any particular unused input depends on the function of the device. Generally, the inputs are tied to GND or V_{CC} , whichever makes more sense for the logic function or is more convenient.

8.4.2 Layout Example

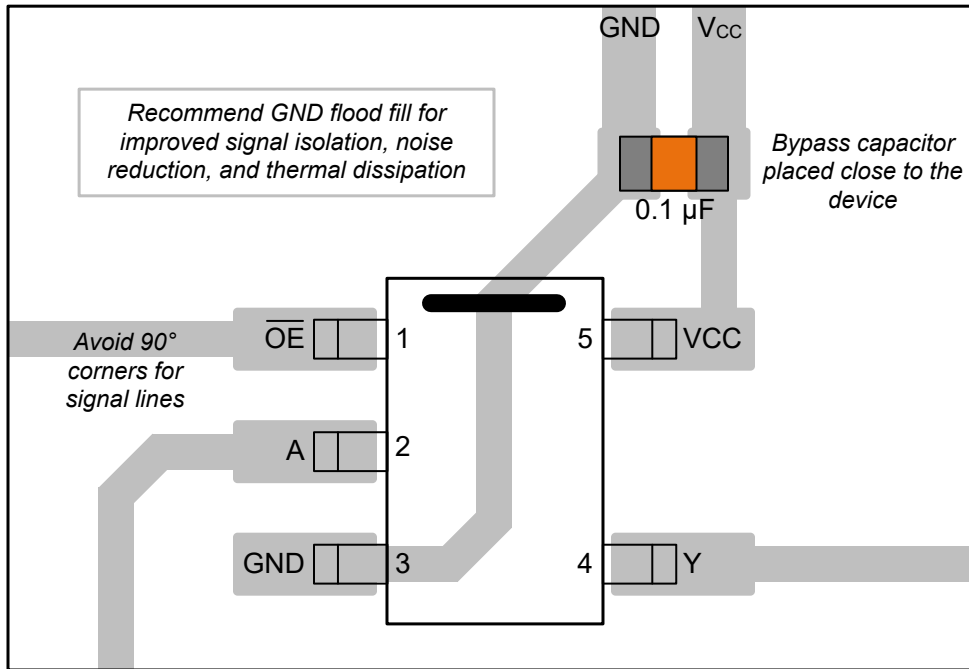


图 8-2. Example Layout for the SN74AHCT1G125-Q1

9 Device and Documentation Support

9.1 Documentation Support (Analog)

9.1.1 Related Documentation

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

表 9-1. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
SN74AHCT1G125-Q1	Click here	Click here	Click here	Click here	Click here

9.2 接收文档更新通知

要接收文档更新通知，请导航至 ti.com 上的器件产品文件夹。点击 [通知](#) 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

9.3 支持资源

[TI E2E™ 中文支持论坛](#) 是工程师的重要参考资料，可直接从专家处获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题，获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的 [使用条款](#)。

9.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.

所有商标均为其各自所有者的财产。

9.5 静电放电警告



静电放电 (ESD) 会损坏这个集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

9.6 术语表

[TI 术语表](#) 本术语表列出并解释了术语、首字母缩略词和定义。

10 Revision History

Changes from Revision D (October 2023) to Revision E (October 2024)	Page
• 更新了 封装信息 表中的 DTX 本体尺寸和 DBV 封装尺寸.....	1

Changes from Revision C (July 2023) to Revision D (October 2023)	Page
• 添加了 应用 部分.....	1
• 向 器件信息 表添加了 DBV 和 DTX 封装.....	1
• Added DBV and DTX packages to <i>Pin Configuration and Functions</i> section.....	3
• Updated R _θ JA values: DBV = 278.0, DTX = 184.7, all values in °C/W	5
• Added <i>Application and Implementation</i> section.....	9

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
CAHCT1G125QDBVRQ1	Active	Production	SOT-23 (DBV) 5	3000 LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	37PH
CAHCT1G125QDBVRQ1.A	Active	Production	SOT-23 (DBV) 5	3000 LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	37PH
CAHCT1G125QDCKRG4Q	Active	Production	SC70 (DCK) 5	3000 LARGE T&R	Yes	Call TI Nipdau	Level-1-260C-UNLIM	-40 to 125	BMS
CAHCT1G125QDCKRG4Q.A	Active	Production	SC70 (DCK) 5	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	BMS
CAHCT1G125QDCKRQ1	Active	Production	SC70 (DCK) 5	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	BMS
CAHCT1G125QDCKRQ1.A	Active	Production	SC70 (DCK) 5	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	BMS
CAHCT1G125WDTXRQ1	Active	Production	X2SON (DTX) 5	3000 LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	7
CAHCT1G125WDTXRQ1.A	Active	Production	X2SON (DTX) 5	3000 LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	7
PCAHCT1G125QDTXRQ1	Active	Preproduction	X2SON (DTX) 5	3000 LARGE T&R	-	Call TI	Call TI	-40 to 125	
PCAHCT1G125QDTXRQ1.A	Active	Preproduction	X2SON (DTX) 5	3000 LARGE T&R	-	Call TI	Call TI	-40 to 125	

(1) **Status:** For more details on status, see our [product life cycle](#).

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative

and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF SN74AHCT1G125-Q1 :

- Catalog : [SN74AHCT1G125](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CAHCT1G125QDBVRQ1	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
CAHCT1G125QDCKRQ1	SC70	DCK	5	3000	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
CAHCT1G125WDTXRQ1	X2SON	DTX	5	3000	180.0	8.4	1.0	1.25	0.48	2.0	8.0	Q1

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CAHCT1G125QDBVRQ1	SOT-23	DBV	5	3000	210.0	185.0	35.0
CAHCT1G125QDCKRQ1	SC70	DCK	5	3000	190.0	190.0	30.0
CAHCT1G125WDTXRQ1	X2SON	DTX	5	3000	210.0	185.0	35.0

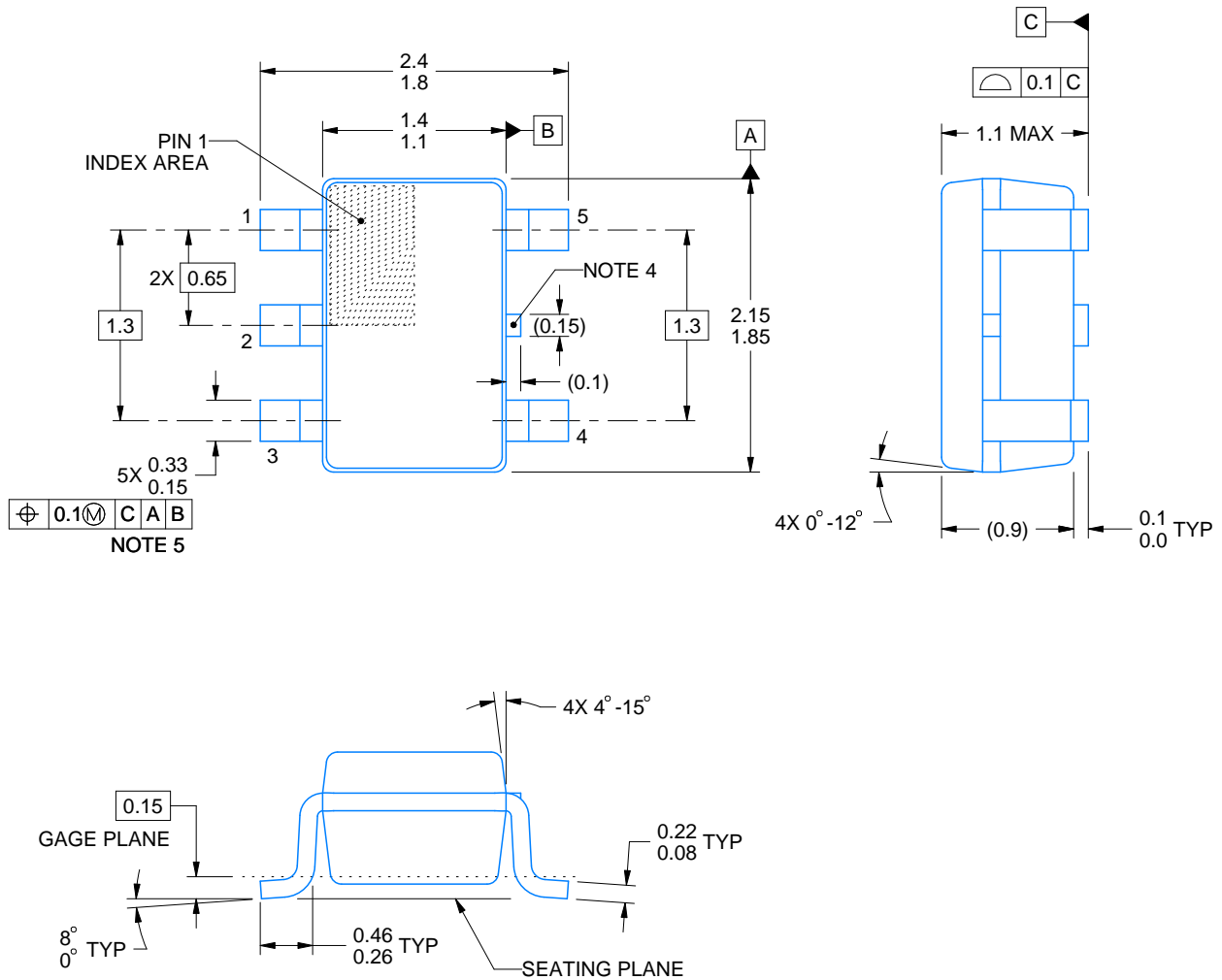
DCK0005A



PACKAGE OUTLINE

SOT - 1.1 max height

SMALL OUTLINE TRANSISTOR



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NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC MO-203.
4. Support pin may differ or may not be present.
5. Lead width does not comply with JEDEC.
6. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25mm per side

EXAMPLE BOARD LAYOUT

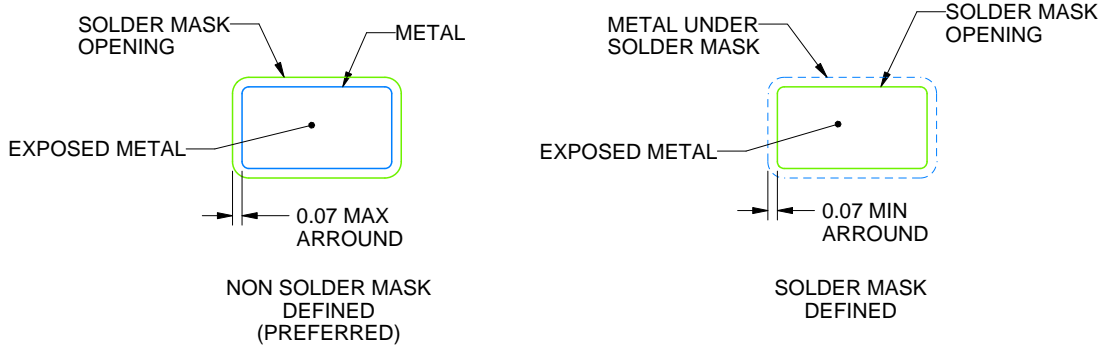
DCK0005A

SOT - 1.1 max height

SMALL OUTLINE TRANSISTOR



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:18X



SOLDER MASK DETAILS

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NOTES: (continued)

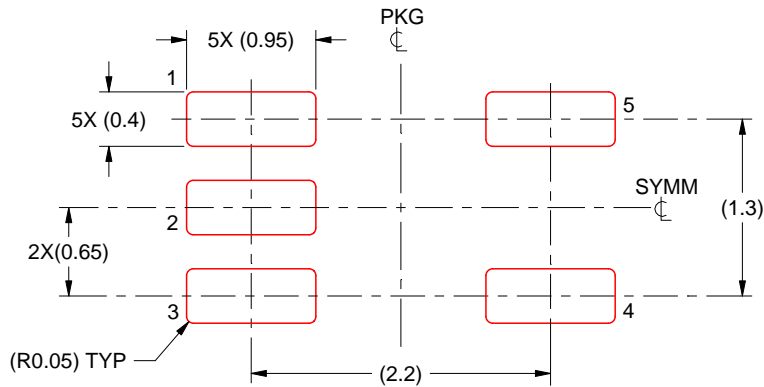
- 7. Publication IPC-7351 may have alternate designs.
- 8. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DCK0005A

SOT - 1.1 max height

SMALL OUTLINE TRANSISTOR



SOLDER PASTE EXAMPLE
BASED ON 0.125 THICK STENCIL
SCALE: 18X

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NOTES: (continued)

9. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
10. Board assembly site may have different recommendations for stencil design.

EXAMPLE BOARD LAYOUT

DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



SOLDER MASK DETAILS

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NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR

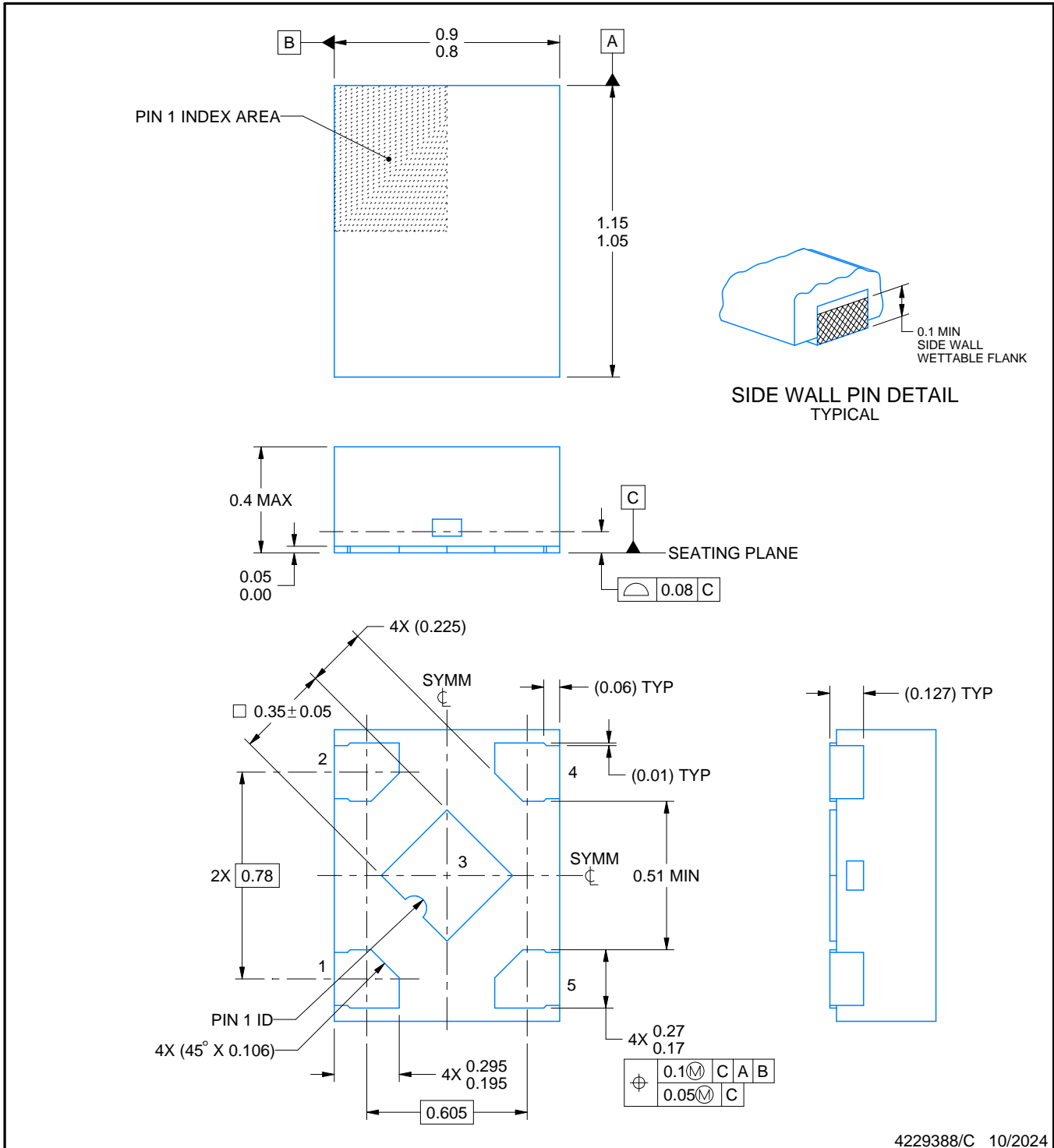
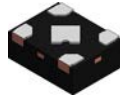


SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.



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NOTES:

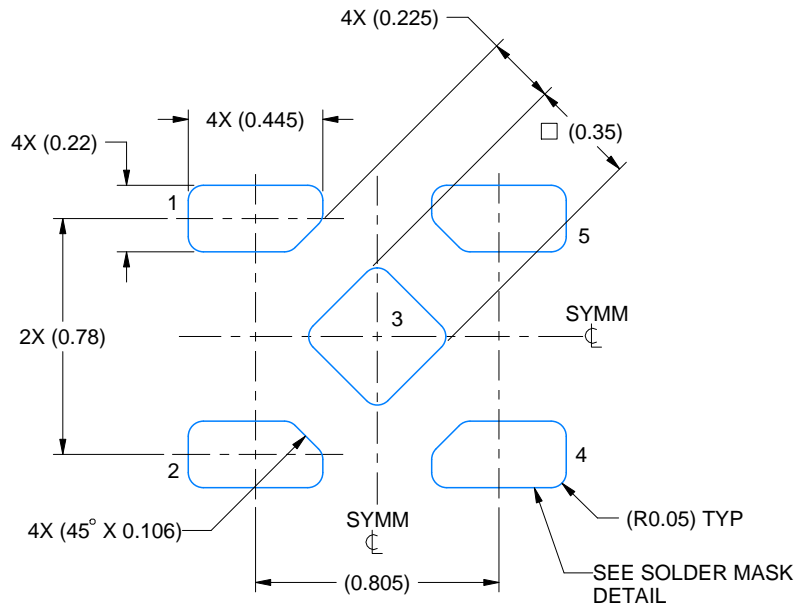
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

EXAMPLE BOARD LAYOUT

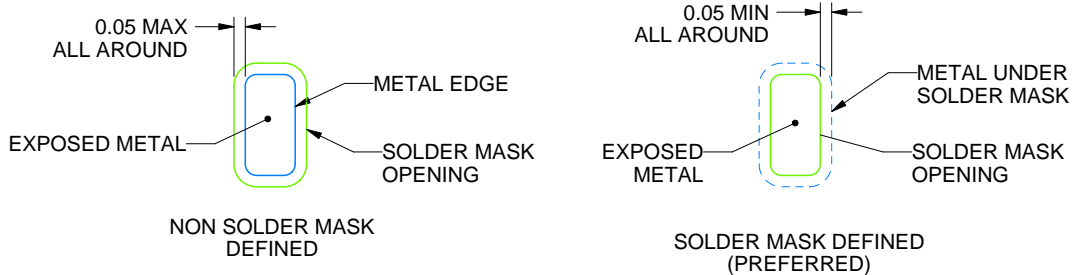
DTX0005A

X2SON - 0.4 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 40X



SOLDER MASK DETAILS

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NOTES: (continued)

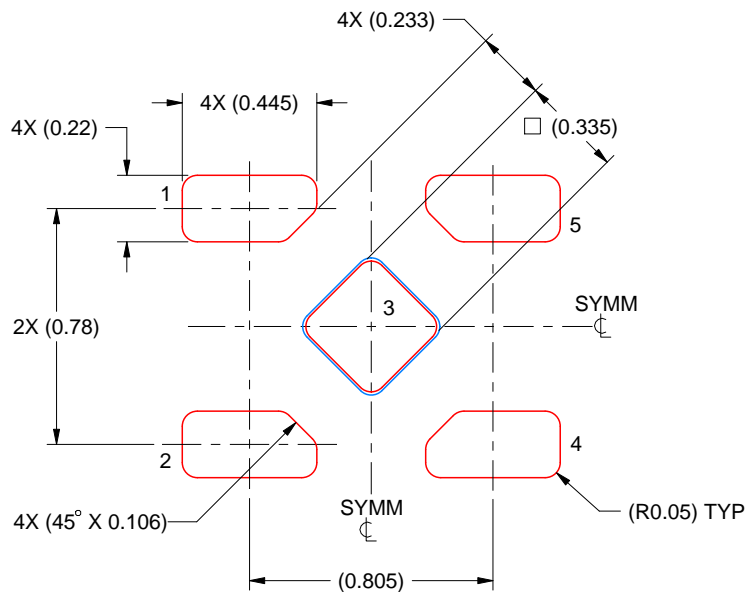
4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).

EXAMPLE STENCIL DESIGN

DTX0005A

X2SON - 0.4 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE: 40X

PRINTED SOLDER PASTE COVERAGE BY AREA UNDER PACKAGE
PAD 5: 92%

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NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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最后更新日期：2025 年 10 月