

## SN74AHCT273 具有清零功能的八路 D 类触发器

### 1 特性

- 输入兼容 TTL 电压
- 包含 8 个具有单轨输出的触发器
- 直接清零输入
- 为每个触发器提供单独的数据输入
- 闩锁性能超过 250mA，符合 JESD 17 规范
- ESD 保护性能超过 JESD 22 规范要求
  - 2000V 人体放电模型 (A114-A)
  - 200V 机器放电模型 (A115-A)
  - 1000V 充电器件模型 (C101)

### 2 应用

- 缓冲器和存储寄存器
- 移位寄存器
- 图形发生器
- 服务器
- PC 和笔记本电脑
- 网络交换机
- 存储器系统
- 数据库

### 3 说明

这些器件是正边沿触发式 D 类触发器，具有直接清零 ( $\overline{\text{CLR}}$ ) 输入。

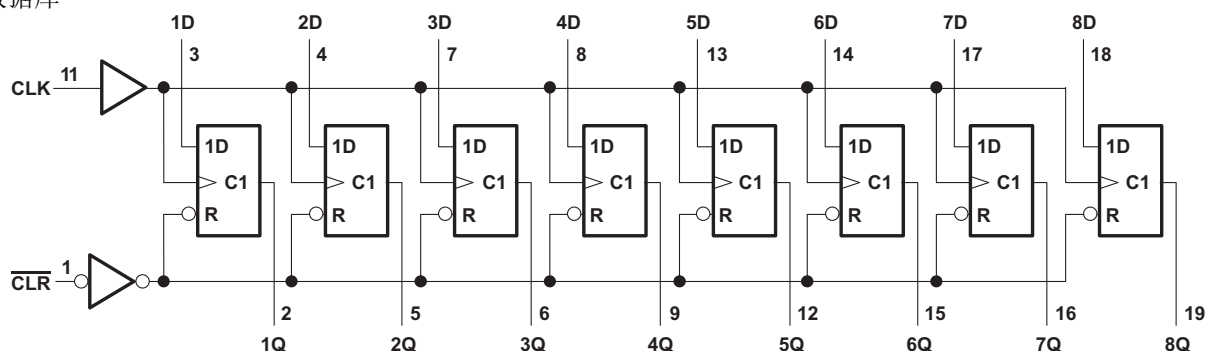
#### 器件信息

器件型号	封装 <sup>(1)</sup>	封装尺寸 <sup>(2)</sup>	本体尺寸 <sup>(3)</sup>
SN74AHCT273	DB (SSOP, 20)	7.2mm × 7.8mm	7.2mm × 5.30mm
	DW (SOIC, 20)	12.80mm × 10.3mm	12.8mm × 7.5mm
	N (PDIP, 20)	24.33mm × 9.4mm	24.33mm × 6.35mm
	PW (TSSOP, 20)	6.50mm × 6.4mm	6.50mm × 4.40mm
	NS (SOP, 20)	12.6mm × 7.8mm	12.6mm × 5.3mm

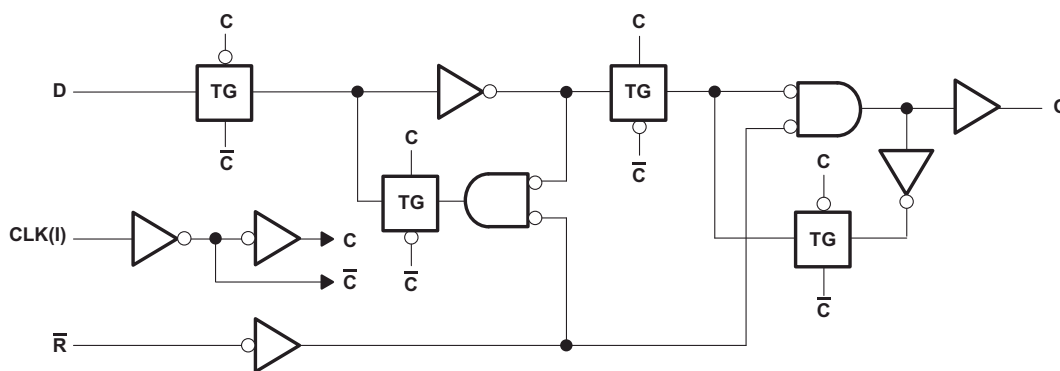
(1) 有关更多信息，请参阅节 11。

(2) 封装尺寸 (长 × 宽) 为标称值，并包括引脚 (如适用)。

(3) 本体尺寸 (长 × 宽) 为标称值，不包括引脚。



简化原理图



简化原理图



## Table of Contents

<b>1 特性</b> .....	<b>1</b>	7.2 Functional Block Diagrams.....	<b>8</b>
<b>2 应用</b> .....	<b>1</b>	7.3 Feature Description.....	<b>9</b>
<b>3 说明</b> .....	<b>1</b>	7.4 Device Functional Modes.....	<b>9</b>
<b>4 Pin Configuration and Functions</b> .....	<b>3</b>	<b>8 Application and Implementation</b> .....	<b>10</b>
<b>5 Specifications</b> .....	<b>4</b>	8.1 Application Information.....	<b>10</b>
5.1 Absolute Maximum Ratings.....	<b>4</b>	8.2 Typical Application.....	<b>10</b>
5.2 Handling Ratings.....	<b>4</b>	8.3 Power Supply Recommendations.....	<b>11</b>
5.3 Recommended Operating Conditions.....	<b>4</b>	8.4 Layout.....	<b>11</b>
5.4 Thermal Information.....	<b>5</b>	<b>9 Device and Documentation Support</b> .....	<b>13</b>
5.5 Electrical Characteristics.....	<b>5</b>	9.1 Documentation Support.....	<b>13</b>
5.6 Timing Requirements.....	<b>5</b>	9.2 接收文档更新通知.....	<b>13</b>
5.7 Switching Characteristics.....	<b>6</b>	9.3 支持资源.....	<b>13</b>
5.8 Noise Characteristics.....	<b>6</b>	9.4 Trademarks.....	<b>13</b>
5.9 Operating Characteristics.....	<b>6</b>	9.5 静电放电警告.....	<b>13</b>
5.10 Typical Characteristics.....	<b>6</b>	9.6 术语表.....	<b>13</b>
<b>6 Parameter Measurement Information</b> .....	<b>7</b>	<b>10 Revision History</b> .....	<b>13</b>
<b>7 Detailed Description</b> .....	<b>8</b>	<b>11 Mechanical, Packaging, and Orderable Information</b> .....	<b>14</b>
7.1 Overview.....	<b>8</b>		

## 4 Pin Configuration and Functions

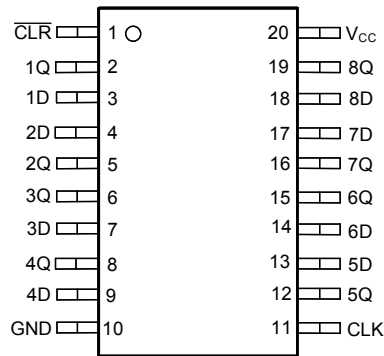


图 4-1. SN74AHCT273 DB, DW, N, NS, or PW Packages; 20-Pin SSOP, SOIC, PDIP, SOP, or TSSOP

表 4-1. Pin Functions

PIN		I/O	DESCRIPTION
NO.	NAME		
1	CLR	I	Clear Pin
2	1Q	O	1Q Output
3	1D	I	1D Input
4	2D	I	2D Input
5	2Q	O	2Q Output
6	3Q	O	3Q Output
7	3D	I	3D Input
8	4D	I	4D Input
9	4Q	O	4Q Output
10	GND	—	Ground Pin
11	CLK	I	Clock Pin
12	5Q	O	5Q Output
13	5D	I	5D Input
14	6D	I	6D Input
15	6Q	O	6Q Output
16	7Q	O	7Q Output
17	7D	I	7D Input
18	8D	I	8D Input
19	8Q	O	8Q Output
20	V <sub>CC</sub>	—	Power Pin

## 5 Specifications

### 5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

		MIN	MAX	UNIT
V <sub>CC</sub>	Supply voltage range	- 0.5	7	V
V <sub>I</sub>	Input voltage range <sup>(2)</sup>	- 0.5	7	V
V <sub>O</sub>	Output voltage range <sup>(2)</sup>	- 0.5	V <sub>CC</sub> + 0.5	V
I <sub>IK</sub>	Input clamp current	V <sub>I</sub> < 0	- 20	mA
I <sub>OK</sub>	Output clamp current	V <sub>O</sub> < 0 or V <sub>O</sub> > V <sub>CC</sub>	±20	mA
I <sub>O</sub>	Continuous output current	V <sub>O</sub> = 0 to V <sub>CC</sub>	±25	mA
Continuous current through V <sub>CC</sub> or GND			±75	mA

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

### 5.2 Handling Ratings

		MIN	MAX	UNIT	
T <sub>stg</sub>	Storage temperature range	- 65	150	°C	
V <sub>(ESD)</sub>	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins <sup>(1)</sup>	0	2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins <sup>(2)</sup>	0	1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

### 5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

		SN74AHCT273		UNIT
		MIN	MAX	
V <sub>CC</sub>	Supply voltage	4.5	5.5	V
V <sub>IH</sub>	High-level input voltage	2		V
V <sub>IL</sub>	Low-level input voltage		0.8	V
V <sub>I</sub>	Input voltage	0	5.5	V
V <sub>O</sub>	Output voltage	0	V <sub>CC</sub>	V
I <sub>OH</sub>	High-level output current		- 8	mA
I <sub>OL</sub>	Low-level output current		8	mA
Δt / Δv	Input transition rise or fall rate		20	ns/V
T <sub>A</sub>	Operating free-air temperature	- 40	125	°C

(1) All unused inputs of the device must be held at V<sub>CC</sub> or GND to ensure proper device operation. Refer to the TI Application Report, *Implications of Slow or Floating CMOS Inputs* (SCBA004).

## 5.4 Thermal Information

THERMAL METRIC <sup>(1)</sup>		SN74AHCT273						UNIT
		DB (SSOP)	DW (SOIC)	DGV (TVSOP)	N (PDIP)	NS (SOP)	PW (TSSOP)	
		20 PINS						
$R_{\theta JA}$	Junction-to-ambient thermal resistance	87.2	81.1	118.1	53.9	77.6	116.8	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	49.1	48.9	33.4	38.8	42.7	58.5	
$R_{\theta JB}$	Junction-to-board thermal resistance	51.8	53.8	59.6	34.7	45.7	78.7	
$\psi_{JT}$	Junction-to-top characterization parameter	11.6	19.5	1.1	26.9	10.2	12.6	
$\psi_{JB}$	Junction-to-board characterization parameter	51.2	53.1	58.9	34.7	45.2	77.9	
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	N/A	N/A	N/A	N/A	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, (SPRA953).

## 5.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	$V_{CC}$	$T_A = 25^\circ\text{C}$			SN74AHCT273		UNIT
			MIN	TYP	MAX	MIN	MAX	
$V_{OH}$	$I_{OH} = -50 \mu\text{A}$	4.5 V	4.4	4.5		4.4		V
	$I_{OH} = -8 \text{mA}$		3.94			3.8		
$V_{OL}$	$I_{OL} = 50 \mu\text{A}$	4.5 V			0.1		0.1	V
	$I_{OL} = 8 \text{mA}$				0.36		0.44	
$I_I$	$V_I = 5.5 \text{V}$ or GND	0 V to 5.5 V			$\pm 0.1$		$\pm 1$	$\mu\text{A}$
$I_{CC}$	$V_I = V_{CC}$ or GND $I_O = 0$	5.5 V			4		40	$\mu\text{A}$
$\Delta I_{CC}^{(1)}$	One input at 3.4 V, Other inputs at $V_{CC}$ or GND	5.5 V			1.35		1.5	mA
$C_i$	$V_I = V_{CC}$ or GND	5 V		2.5	10		10	pF

(1) This is the increase in supply current for each input at one of the specified TTL voltage levels, rather than 0 V or  $V_{CC}$ .

## 5.6 Timing Requirements

over recommended operating free-air temperature range,  $V_{CC} = 5 \text{V} \pm 0.5 \text{V}$  (unless otherwise noted) (see [Load Circuit and Voltage Waveforms](#))

		$T_A = 25^\circ\text{C}$		SN74AHCT273		UNIT
		MIN	MAX	MIN	MAX	
$t_w$	Pulse duration	CLR low	5		6	ns
		CLK high or low	5		6.5	
$t_{su}$	Setup time	Data before CLK $\uparrow$	5		5	ns
		CLR before CLK $\uparrow$	2.5		2.5	
$t_h$	Hold time, data after CLK $\uparrow$		0		0	ns

### 5.7 Switching Characteristics

over recommended operating free-air temperature range,  $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$  (unless otherwise noted) (see [Load Circuit and Voltage Waveforms](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	$T_A = 25^\circ\text{C}$			SN74AHCT273		UNIT
				MIN	TYP	MAX	MIN	MAX	
$f_{\text{max}}$			$C_L = 15\text{ pF}$	75 <sup>(1)</sup>	120 <sup>(1)</sup>		65		MHz
			$C_L = 50\text{ pF}$	50	75		45		
$t_{\text{PHL}}$	$\overline{\text{CLR}}$	Q	$C_L = 15\text{ pF}$		7.5 <sup>(1)</sup>	10 <sup>(1)</sup>	1	11.6	ns
$t_{\text{PLH}}$	CLK	Q	$C_L = 15\text{ pF}$		5.5 <sup>(1)</sup>	7.5 <sup>(1)</sup>	1	8.8	ns
$t_{\text{PHL}}$					5.8 <sup>(1)</sup>	8.2 <sup>(1)</sup>	1	10	
$t_{\text{PHL}}$	$\overline{\text{CLR}}$	Q	$C_L = 50\text{ pF}$		8.5	11	1	12.6	ns
$t_{\text{PLH}}$	CLK	Q	$C_L = 50\text{ pF}$		6.5	8.5	1	9.8	ns
$t_{\text{PHL}}$					6.8	9.2	1	11	
$t_{\text{sk(o)}}$			$C_L = 50\text{ pF}$			1 <sup>(2)</sup>		1	ns

(1) On products compliant to MIL-PRF-38535, this parameter is not production tested.

(2) On products compliant to MIL-PRF-38535, this parameter does not apply.

### 5.8 Noise Characteristics

$V_{CC} = 5\text{ V}$ ,  $C_L = 50\text{ pF}$ ,  $T_A = 25^\circ\text{C}$ <sup>(1)</sup>

PARAMETER	DESCRIPTION	SN74AHCT273			UNIT
		MIN	TYP	MAX	
$V_{\text{OL(P)}}$	Quiet output, maximum dynamic $V_{\text{OL}}$		7.6		V
$V_{\text{OL(V)}}$	Quiet output, minimum dynamic $V_{\text{OL}}$		-0.48		V
$V_{\text{OH(V)}}$	Quiet output, minimum dynamic $V_{\text{OH}}$	4.4			V
$V_{\text{IH(D)}}$	High-level dynamic input voltage	2			V
$V_{\text{IL(D)}}$	Low-level dynamic input voltage			0.8	V

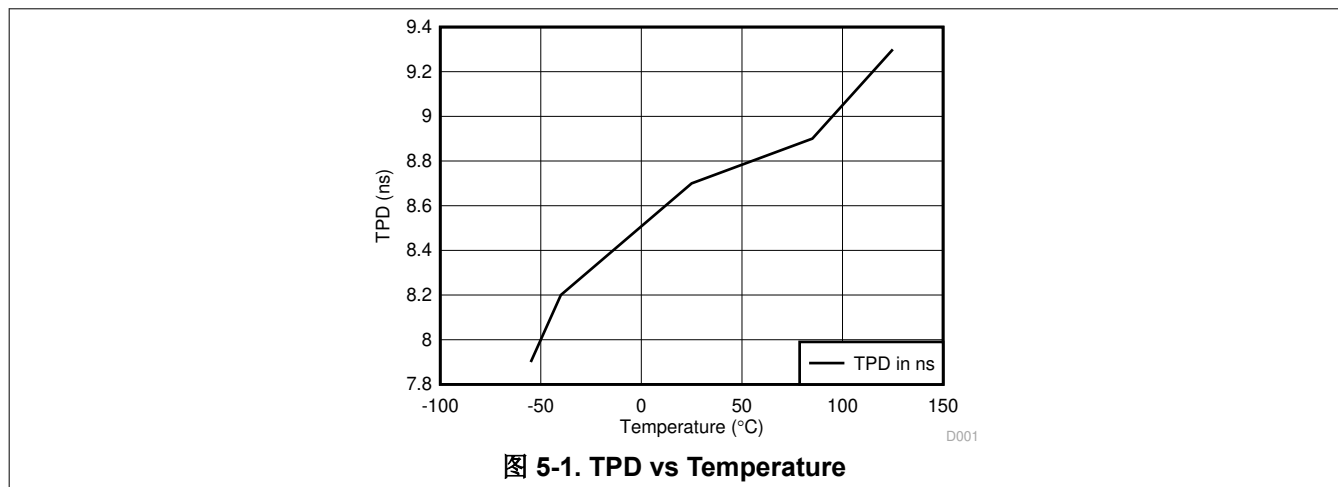
(1) Characteristics are for surface-mount packages only.

### 5.9 Operating Characteristics

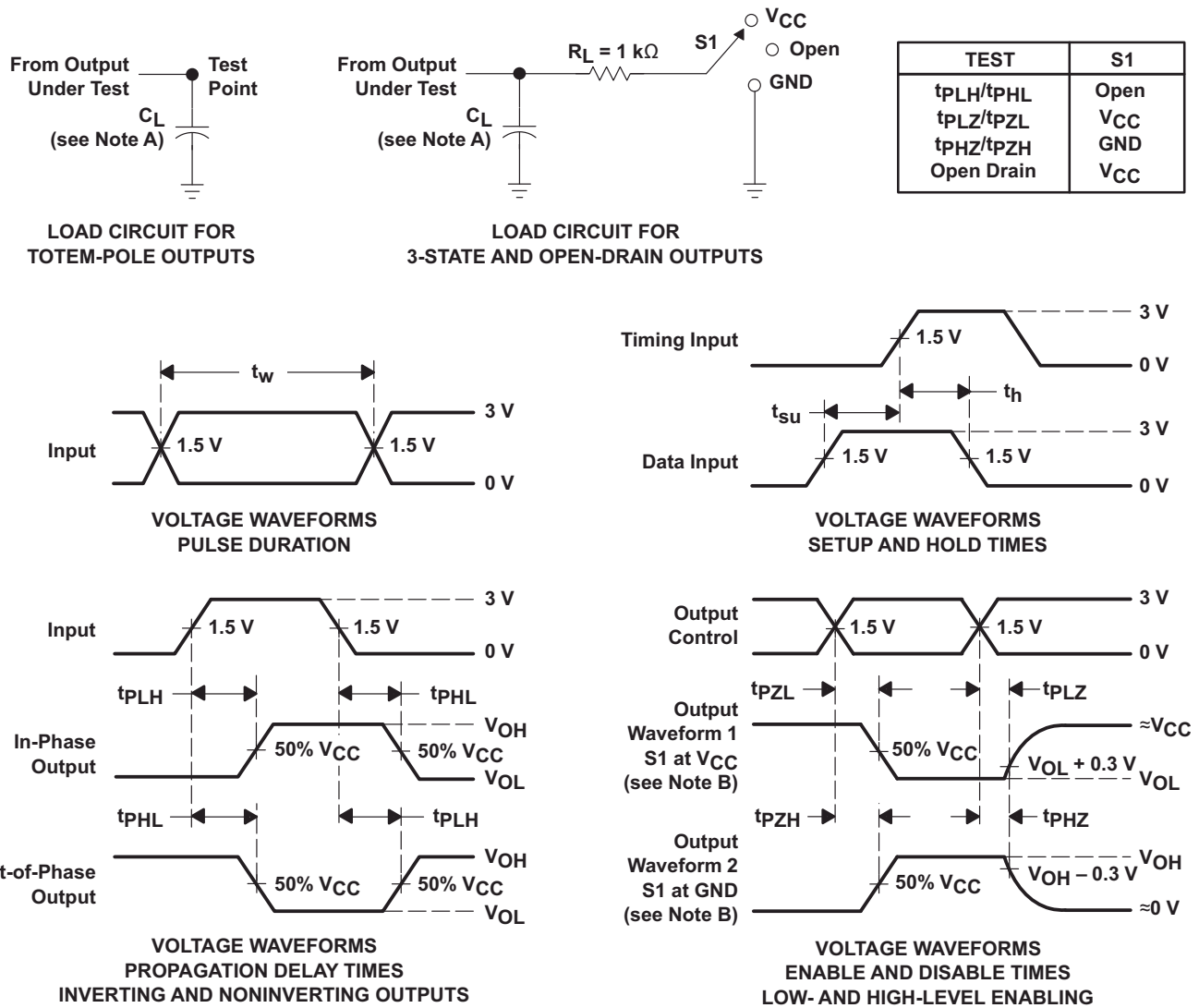
$T_A = 25^\circ\text{C}$

PARAMETER	TEST CONDITIONS	TYP	UNIT
$C_{\text{pd}}$	No load, $f = 1\text{ MHz}$	27	pF

### 5.10 Typical Characteristics



## 6 Parameter Measurement Information



- NOTES: A.  $C_L$  includes probe and jig capacitance.  
 B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.  
 C. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 1$  MHz,  $Z_O = 50 \Omega$ ,  $t_r \leq 3$  ns,  $t_f \leq 3$  ns.  
 D. The outputs are measured one at a time with one input transition per measurement.

图 6-1. Load Circuit and Voltage Waveforms

## 7 Detailed Description

### 7.1 Overview

These circuits are positive-edge-triggered D-type flip-flops with a direct clear ( $\overline{\text{CLR}}$ ) input. Information at the data (D) inputs meeting the setup time requirements is transferred to the Q outputs on the positive-going edge of the clock (CLK) pulse. Clock triggering occurs at a particular voltage level and is not directly related to the transition time of the positive-going pulse. When CLK is at either the high or low level, the D input has no effect at the output.

The inputs are TTL compatible with  $V_{IL}$  at 0.8 V and  $V_{IH}$  at 2 V. This feature allows the use of these devices as up translators in a mixed 3.3 V to 5 V system environment.

### 7.2 Functional Block Diagrams

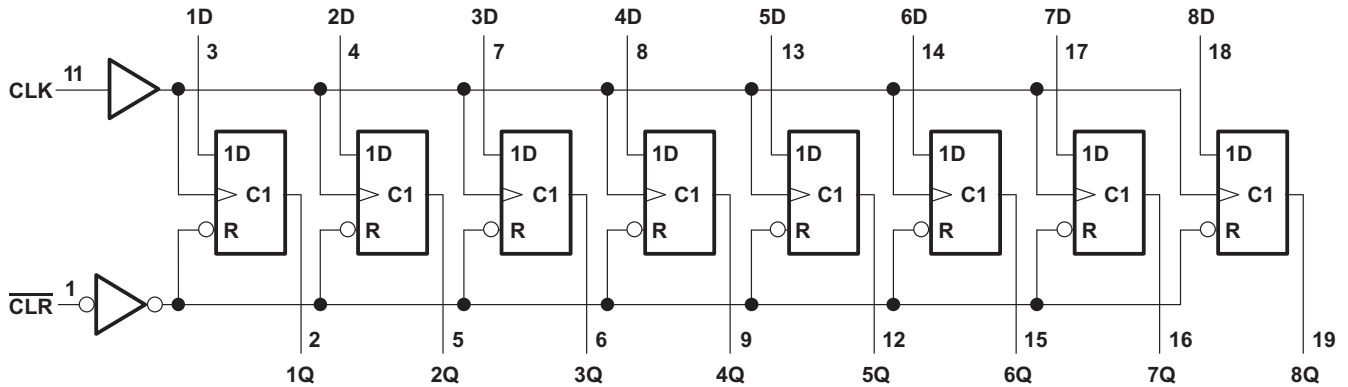


图 7-1. Logic Diagram (Positive Logic)

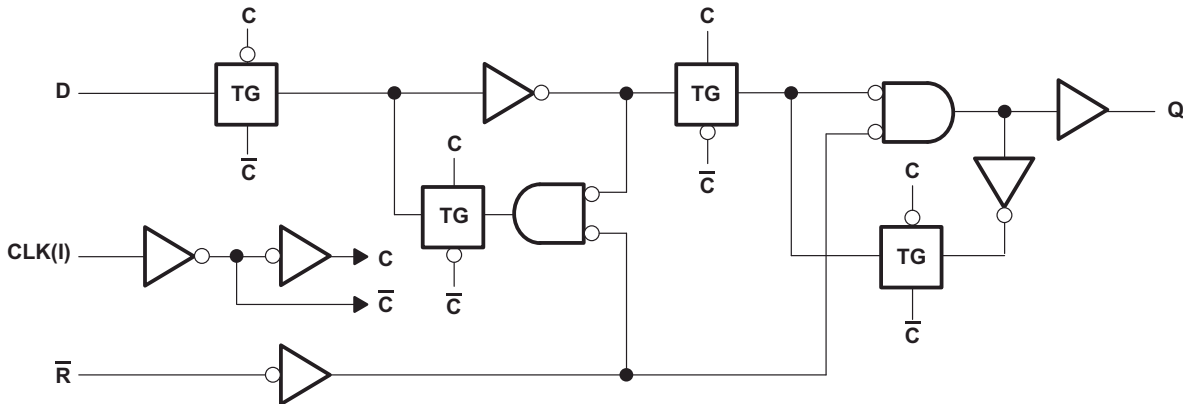


图 7-2. Logic Diagram, Each Flip-flop (Positive Logic)



### 7.3 Feature Description

- Allow up voltage translation from 3.3 V to 5 V
  - Inputs accept TTL voltage levels
- Slow edge rates minimize output ringing

### 7.4 Device Functional Modes

表 7-1. Function Table  
(Each Flip-flop)

INPUTS			OUTPUT Q
CLR	CLK	D	
L	X	X	L
H	↑	H	H
H	↑	L	L
H	L	X	Q <sub>0</sub>

## 8 Application and Implementation

### 备注

以下应用部分中的信息不属于 TI 器件规格的范围，TI 不担保其准确性和完整性。TI 的客户应负责确定器件是否适用于其应用。客户应验证并测试其设计，以确保系统功能。

### 8.1 Application Information

The SNx4AHCT273 is a low-drive CMOS device that can be used for a multitude of applications where output ringing is a concern. The low drive and slow edge rates will minimize overshoot and undershoot on the outputs. The inputs are TTL compatible. This feature makes it ideal for translating up from 3.3 V to 5 V. 图 8-2 shows the reduction in ringing compared to higher drive parts such as AC.

### 8.2 Typical Application

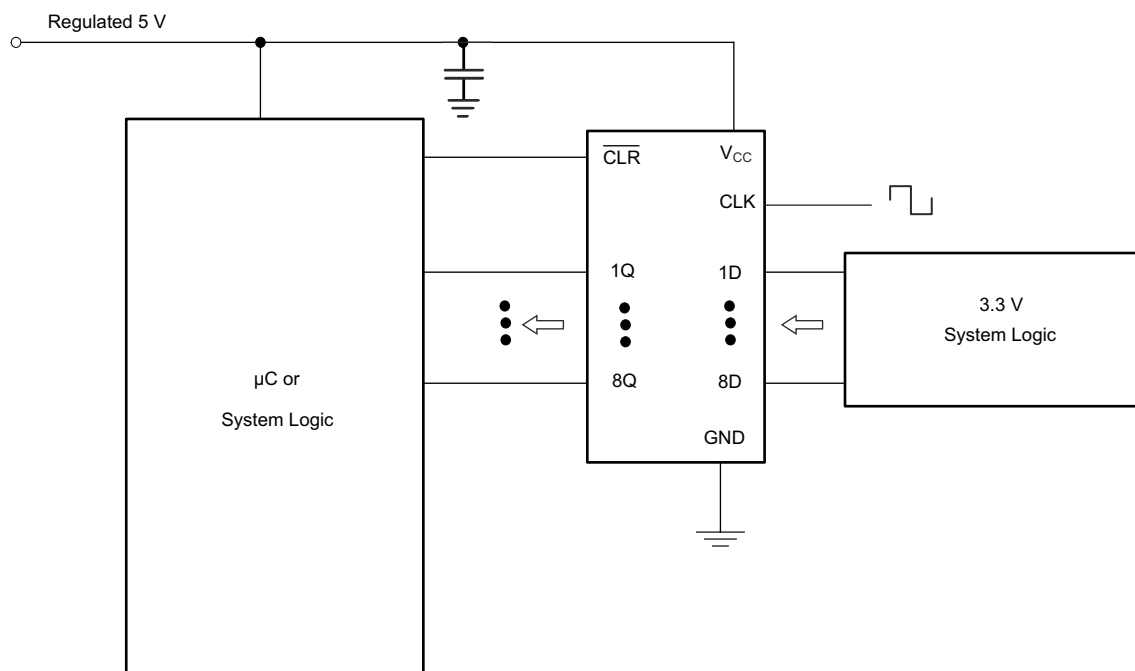


图 8-1. Typical Application Schematic

#### 8.2.1 Design Requirements

This device uses CMOS technology and has balanced output drive. Care should be taken to avoid bus contention because it can drive currents that would exceed maximum limits. The high drive will also create fast edges into light loads, so routing and load conditions should be considered to prevent ringing.

#### 8.2.2 Detailed Design Procedure

- Recommended input conditions
  - Rise time and fall time specs: See ( $\Delta t / \Delta V$ ) in the 节 5.3 table.
  - Specified High and low levels: See ( $V_{IH}$  and  $V_{IL}$ ) in the 节 5.3 table.
  - Inputs are overvoltage tolerant allowing them to go as high as 5.5 V at any valid  $V_{CC}$
- Recommend output conditions
  - Load currents should not exceed 25 mA per output and 75 mA total for the part
  - Outputs should not be pulled above  $V_{CC}$

### 8.2.3 Application Curves

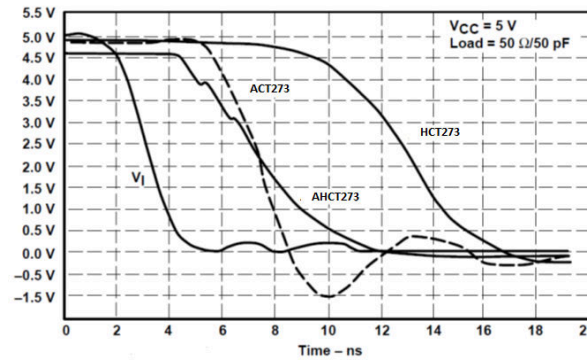


图 8-2. Switching Characteristics Comparison

### 8.3 Power Supply Recommendations

The power supply can be any voltage between the MIN and MAX supply voltage rating located in the [表 5.3](#) table.

Each  $V_{CC}$  pin should have a good bypass capacitor to prevent power disturbance. For devices with a single supply, 0.1  $\mu F$  is recommended. If there are multiple  $V_{CC}$  pins, 0.01  $\mu F$  or 0.022  $\mu F$  is recommended for each power pin. It is acceptable to parallel multiple bypass caps to reject different frequencies of noise. A 0.1  $\mu F$  and 1  $\mu F$  are commonly used in parallel. The bypass capacitor should be installed as close to the power pin as possible for best results.

### 8.4 Layout

#### 8.4.1 Layout Guidelines

When using multiple bit logic devices inputs should not ever float.

In many cases, functions or parts of functions of digital logic devices are unused, for example, when only two inputs of a triple-input AND gate are used or only 3 of the 4 buffer gates are used. Such input pins should not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. Specified in [图 8-3](#) are the rules that must be observed under all circumstances. All unused inputs of digital logic devices must be connected to a high or low bias to prevent them from floating. The logic level that should be applied to any particular unused input depends on the function of the device. Generally inputs will be tied to GND or  $V_{CC}$ , whichever makes more sense or is more convenient. It is generally acceptable to float outputs unless the part is a transceiver.

### 8.4.2 Layout Example

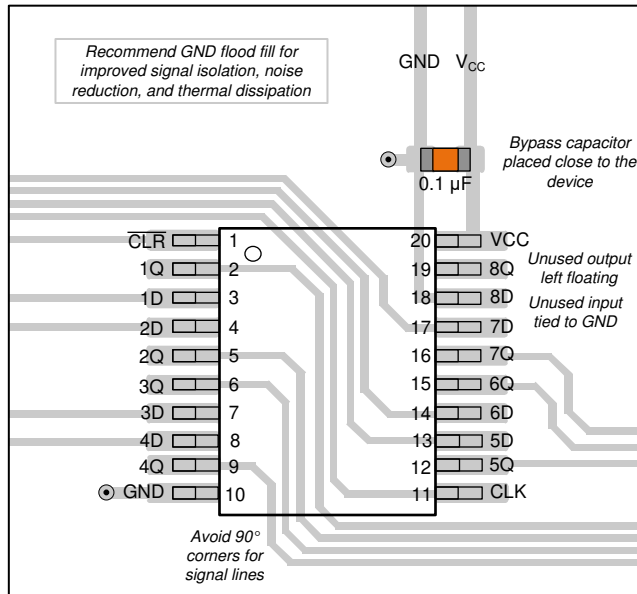


图 8-3. Layout Diagram

## 9 Device and Documentation Support

### 9.1 Documentation Support

#### 9.1.1 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

**表 9-1. Related Links**

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
SN74AHCT273	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>

### 9.2 接收文档更新通知

要接收文档更新通知，请导航至 [ti.com](http://ti.com) 上的器件产品文件夹。点击 [通知](#) 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

### 9.3 支持资源

[TI E2E™ 中文支持论坛](#) 是工程师的重要参考资料，可直接从专家处获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题，获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的 [使用条款](#)。

### 9.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.

所有商标均为其各自所有者的财产。

### 9.5 静电放电警告



静电放电 (ESD) 会损坏这个集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

### 9.6 术语表

[TI 术语表](#) 本术语表列出并解释了术语、首字母缩略词和定义。

## 10 Revision History

Changes from Revision F (July 2014) to Revision G (August 2024)	Page
• 向 <a href="#">封装信息</a> 表中添加了封装尺寸.....	1
• 删除了整个数据表中对军用级器件的引用.....	1
• Updated R <sup>θ</sup> JA values: PW = 104.7 to 116.8, DB = 98.7 to 87.2, DW = 81.8 to 81.1, NS = 79.4 to 77.6; Updated PW, DB, DW, and NS packages for R <sup>θ</sup> JC(top), R <sup>θ</sup> JB, ΨJT, ΨJB, and R <sup>θ</sup> JC(bot), all values in °C/W .....	5
• Updated <i>Layout Example</i> image.....	12

Changes from Revision E (April 2002) to Revision F (July 2014)	Page
• 根据新的 TI 数据表标准更新了文档.....	1
• 删除了“订购信息”表.....	1

- 添加了“应用” ..... 1
- Added Handling Ratings table. ....4
- Changed MAX operating temperature to 125°C in Recommended Operating Conditions table. ....4
- Added Typical Characteristics section. ....6
- Added Application and Implementation section. ....10

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## 11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74AHCT273DBR	ACTIVE	SSOP	DB	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	(AHCT273, HB273)	<a href="#">Samples</a>
SN74AHCT273DW	OBSOLETE	SOIC	DW	20		TBD	Call TI	Call TI	-40 to 125	AHCT273	
SN74AHCT273DWR	ACTIVE	SOIC	DW	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	AHCT273	<a href="#">Samples</a>
SN74AHCT273N	ACTIVE	PDIP	N	20	20	RoHS & Green	NIPDAU	N / A for Pkg Type	-40 to 125	SN74AHCT273N	<a href="#">Samples</a>
SN74AHCT273NSR	ACTIVE	SOP	NS	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	AHCT273	<a href="#">Samples</a>
SN74AHCT273PWR	ACTIVE	TSSOP	PW	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HB273	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74AHCT273DBR	SSOP	DB	20	2000	330.0	16.4	8.2	7.5	2.5	12.0	16.0	Q1
SN74AHCT273DBR	SSOP	DB	20	2000	330.0	16.4	8.2	7.5	2.5	12.0	16.0	Q1
SN74AHCT273DWR	SOIC	DW	20	2000	330.0	24.4	10.8	13.3	2.7	12.0	24.0	Q1
SN74AHCT273DWR	SOIC	DW	20	2000	330.0	24.4	10.9	13.3	2.7	12.0	24.0	Q1
SN74AHCT273NSR	SOP	NS	20	2000	330.0	24.4	8.4	13.0	2.5	12.0	24.0	Q1
SN74AHCT273NSR	SOP	NS	20	2000	330.0	24.4	8.4	13.0	2.5	12.0	24.0	Q1
SN74AHCT273PWR	TSSOP	PW	20	2000	330.0	16.4	6.95	7.0	1.4	8.0	16.0	Q1
SN74AHCT273PWR	TSSOP	PW	20	2000	330.0	16.4	6.95	7.0	1.4	8.0	16.0	Q1

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74AHCT273DBR	SSOP	DB	20	2000	356.0	356.0	35.0
SN74AHCT273DBR	SSOP	DB	20	2000	353.0	353.0	32.0
SN74AHCT273DWR	SOIC	DW	20	2000	367.0	367.0	45.0
SN74AHCT273DWR	SOIC	DW	20	2000	356.0	356.0	45.0
SN74AHCT273NSR	SOP	NS	20	2000	367.0	367.0	45.0
SN74AHCT273NSR	SOP	NS	20	2000	356.0	356.0	45.0
SN74AHCT273PWR	TSSOP	PW	20	2000	353.0	353.0	32.0
SN74AHCT273PWR	TSSOP	PW	20	2000	356.0	356.0	35.0

**TUBE**


\*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
SN74AHCT273N	N	PDIP	20	20	506	13.97	11230	4.32

PW0020A



# PACKAGE OUTLINE

## TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



4220206/A 02/2017

NOTES:

- All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
- This drawing is subject to change without notice.
- This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
- This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
- Reference JEDEC registration MO-153.

# EXAMPLE BOARD LAYOUT

PW0020A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 10X



SOLDER MASK DETAILS

4220206/A 02/2017

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

PW0020A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE: 10X

4220206/A 02/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

# DB0020A



# PACKAGE OUTLINE

## SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



4214851/B 08/2019

### NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-150.

# EXAMPLE BOARD LAYOUT

DB0020A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 10X



4214851/B 08/2019

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



# EXAMPLE STENCIL DESIGN

DB0020A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE: 10X

4214851/B 08/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

# MECHANICAL DATA

NS (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

N (R-PDIP-T\*\*)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
  - The 20 pin end lead shoulder width is a vendor option, either half or full width.

# DW0020A



# PACKAGE OUTLINE

## SOIC - 2.65 mm max height

SOIC



**NOTES:**

- All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
- This drawing is subject to change without notice.
- This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
- This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm per side.
- Reference JEDEC registration MS-013.

# EXAMPLE BOARD LAYOUT

DW0020A

SOIC - 2.65 mm max height

SOIC



LAND PATTERN EXAMPLE  
SCALE:6X



SOLDER MASK DETAILS

4220724/A 05/2016

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

DW0020A

SOIC - 2.65 mm max height

SOIC



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:6X

4220724/A 05/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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