

## SN74AHCT367 具有三态输出的六通道缓冲器和线路驱动器

### 1 特性

- 输入兼容 TTL 电压
- 真实输出
- 闩锁性能超过 100mA，符合 JESD 78 II 级规范
- ESD 保护性能超过 JESD 22 规范要求
  - 2000V 人体放电模型
  - 2000V 充电器件模型

### 2 应用

- 电信基础设施
- 电视
- 机顶盒
- 网络交换机
- 无线基础设施
- 电子销售终端

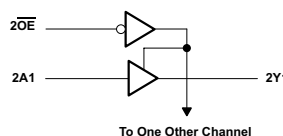
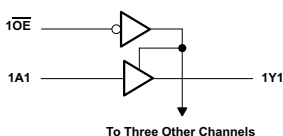
### 3 说明

SN74AHCT367 器件专门设计用于提高三态存储器地址驱动器、时钟驱动器以及总线导向接收器和发射器的性能和密度。

#### 封装信息

器件型号	封装 <sup>(1)</sup>	封装尺寸 <sup>(2)</sup>	本体尺寸 <sup>(3)</sup>
SN74AHCT367	D ( SOIC , 16 )	9.9mm × 6mm	9.9mm x 3.90mm
	DB ( SSOP , 16 )	6.2mm × 7.8mm	6.2mm x 5.30mm
	DGV ( TVSOP , 16 )	3.6mm × 6.4mm	3.6mm x 4.4mm
	PW ( TSSOP , 16 )	5mm × 6.4mm	5.00mm x 4.40mm

- (1) 如需了解更多信息，请参阅[机械、封装和可订购信息](#)。
- (2) 封装尺寸 (长 × 宽) 为标称值，并包括引脚 (如适用)。
- (3) 本体尺寸 (长 × 宽) 为标称值，不包括引脚。



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## 4 Pin Configuration and Functions

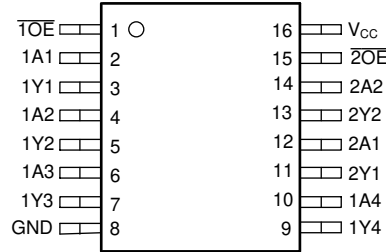


图 4-1. D, DB, DGV, or PW Package; 16-Pin SOIC, SSOP, TVSOP, or TSSOP (Top View)

表 4-1. Pin Functions

PIN		TYPE	DESCRIPTION
NO.	NAME		
1	1 $\overline{OE}$	I	Output Enable 1
2	1A1	I	1A1 Input
3	1Y1	O	1Y1 Output
4	1A2	I	1A2 Input
5	1Y2	O	1Y2 Output
6	1A3	I	1A3 Input
7	1Y3	O	1Y3 Output
8	GND	—	Ground Pin
9	1Y4	O	1Y4 Output
10	1A4	I	1A4 Input
11	2Y1	O	2Y1 Output
12	2A1	I	2A1 Input
13	2Y2	O	2Y2 Output
14	2A2	I	2A2 Input
15	2 $\overline{OE}$	I	Output Enable 2
16	V <sub>CC</sub>	—	Power Pin

## 5 Specifications

### 5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

		MIN	MAX	UNIT
V <sub>CC</sub>	Supply voltage range	- 0.5	7	V
V <sub>I</sub>	Input voltage range <sup>(2)</sup>	- 0.5	7	V
V <sub>O</sub>	Output voltage range <sup>(2)</sup>	- 0.5	V <sub>CC</sub> + 0.5	V
I <sub>IK</sub>	Input clamp current	V <sub>I</sub> < 0	- 20	mA
I <sub>OK</sub>	Output clamp current	V <sub>O</sub> < 0 or V <sub>O</sub> > V <sub>CC</sub>	±20	mA
I <sub>O</sub>	Continuous output current	V <sub>O</sub> = 0 to V <sub>CC</sub>	±25	mA
Continuous current through V <sub>CC</sub> or GND			±75	mA
T <sub>stg</sub>	Storage temperature range	- 65	150	°C

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under [# 5.3](#). Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

### 5.2 ESD Ratings

		VALUE	UNIT
V <sub>(ESD)</sub>	Electrostatic discharge	±2000	V
		±2000	

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

### 5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

		SN74AHCT367		UNIT
		MIN	MAX	
V <sub>CC</sub>	Supply voltage	4.5	5.5	V
V <sub>IH</sub>	High-level input voltage	2		V
V <sub>IL</sub>	Low-level Input voltage		0.8	V
V <sub>I</sub>	Input voltage	0	5.5	V
V <sub>O</sub>	Output voltage	0	V <sub>CC</sub>	V
I <sub>OH</sub>	High-level output current		- 8	mA
I <sub>OL</sub>	Low-level output current		8	mA
Δt/Δv	Input transition rise or fall rate		20	ns/V
T <sub>A</sub>	Operating free-air temperature	- 40	125	°C

- (1) All unused inputs of the device must be held at V<sub>CC</sub> or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs* ([SCBA004](#)).

## 5.4 Thermal Information

THERMAL METRIC <sup>(1)</sup>		SN74AHCT367				UNIT
		D	DB	DGV	PW	
		16 PINS				
R <sub>θJA</sub>	Junction-to-ambient thermal resistance	93.8	103.9	124.5	135.9	°C/W
R <sub>θJC(top)</sub>	Junction-to-case (top) thermal resistance	54.7	54.3	49.8	70.3	
R <sub>θJB</sub>	Junction-to-board thermal resistance	50.9	54.6	56.2	81.3	
ψ <sub>JT</sub>	Junction-to-top characterization parameter	20.8	14.3	5.8	22.5	
ψ <sub>JB</sub>	Junction-to-board characterization parameter	50.7	54.0	55.7	80.8	
R <sub>θJC(bot)</sub>	Junction-to-case (bottom) thermal resistance	N/A	N/A	N/A	N/A	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report (SPRA953).

## 5.5 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V <sub>CC</sub>	T <sub>A</sub> = 25°C			- 40°C to 85°C		- 40°C to 125°C		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V <sub>OH</sub>	I <sub>OH</sub> = - 50 μA	4.5 V	4.4	4.5		4.4		4.4	V	
	I <sub>OH</sub> = - 8 mA		3.94			3.8		3.8		
V <sub>OL</sub>	I <sub>OL</sub> = 50 μA	4.5 V			0.1			0.1	V	
	I <sub>OH</sub> = 8 mA				0.36		0.44	0.44		
I <sub>I</sub>	V <sub>I</sub> = 5.5 V or GND	0 V to 5.5 V			±0.1 <sup>(1)</sup>		±1 <sup>(1)</sup>		±1	μA
I <sub>OZ</sub>	V <sub>O</sub> = V <sub>CC</sub> or GND V <sub>I</sub> (OE) = V <sub>IL</sub> or V <sub>IH</sub>	5.5 V			±0.25		±2.5		±2.5	μA
I <sub>CC</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND, I <sub>O</sub> = 0	5.5 V			4		40		40	μA
Δ I <sub>CC</sub> <sup>(2)</sup>	One input at 3.4 V, Other inputs at V <sub>CC</sub> or GND	5.5 V			1.35		1.5		1.5	mA
C <sub>i</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND	5 V			2.5		10		10	pF
C <sub>O</sub>	V <sub>O</sub> = V <sub>CC</sub> or GND	5 V			5					pF

(1) On products compliant to MIL-PRF-38535, this parameter is not production tested at V<sub>CC</sub> = 0 V.

(2) This is the increase in supply current for each input at one of the specified TTL voltage levels, rather than 0 V or V<sub>CC</sub>.

## 5.6 Switching Characteristics

over recommended operating free-air temperature range, V<sub>CC</sub> = 5 V ± 0.5 V (unless otherwise noted) (see [Load Circuit and Voltage Waveforms](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T <sub>A</sub> = 25°C		- 40°C to 85°C		- 40°C to 125°C		UNIT
				TYP	MAX	MIN	MAX	MIN	MAX	
t <sub>PLH</sub>	A	Y	C <sub>L</sub> = 15 pF	2.5 <sup>(1)</sup>	4.8 <sup>(1)</sup>	1	6.5	1	8.5	ns
t <sub>PHL</sub>				2.5 <sup>(1)</sup>	4.8 <sup>(1)</sup>	1	6.5	1	8.5	
t <sub>PZH</sub>	OE	Y	C <sub>L</sub> = 15 pF	3.5 <sup>(1)</sup>	8 <sup>(1)</sup>	1	9.5	1	9	ns
t <sub>PZL</sub>				2.8 <sup>(1)</sup>	7 <sup>(1)</sup>	1	8.5 <sup>(1)</sup>	1	8	
t <sub>PHZ</sub>	OE	Y	C <sub>L</sub> = 15 pF	3.1 <sup>(1)</sup>	8 <sup>(1)</sup>	1	9.5	1	9	ns
t <sub>PLZ</sub>				2.8 <sup>(1)</sup>	7 <sup>(1)</sup>	1	8.5	1	8	
t <sub>PLH</sub>	A	Y	C <sub>L</sub> = 50 pF	3.5	5.8	1	7.5	1	9.5	ns
t <sub>PHL</sub>				3.3	5.8	1	7.5	1	9.5	
t <sub>PZH</sub>	OE	Y	C <sub>L</sub> = 50 pF	4.5	9	1	10.5	1	10	ns
t <sub>PZL</sub>				3.7	8	1	9.5	1	9	
t <sub>PHZ</sub>	OE	Y	C <sub>L</sub> = 50 pF	4.1	9	1	10.5	1	10	ns
t <sub>PLZ</sub>				3.6	8	1	9.5	1	9	

(1) On products compliant to MIL-PRF-38535, this parameter is not production tested.

### 5.7 Noise Characteristics

$V_{CC} = 5\text{ V}$ ,  $C_L = 50\text{ pF}$ ,  $T_A = 25^\circ\text{C}$ <sup>(1)</sup>

PARAMETER	SN74AHCT367			UNIT
	MIN	TYP	MAX	
$V_{OL(P)}$ Quiet output, maximum dynamic $V_{OL}$		0.4		V
$V_{OL(V)}$ Quiet output, minimum dynamic $V_{OL}$		- 0.4		V
$V_{OH(V)}$ Quiet output, minimum dynamic $V_{OH}$		4.7		V
$V_{IH(D)}$ High-level dynamic input voltage	2			V
$V_{IL(D)}$ Low-level dynamic input voltage			0.8	V

(1) Characteristics are for surface-mount packages only.

### 5.8 Operating Characteristics

$V_{CC} = 5\text{ V}$ ,  $T_A = 25^\circ\text{C}$

PARAMETER	TEST CONDITIONS	TYP	UNIT
$C_{pd}$ Power dissipation capacitance	No load, $f = 1\text{ MHz}$	22	pF

### 5.9 Typical Characteristics

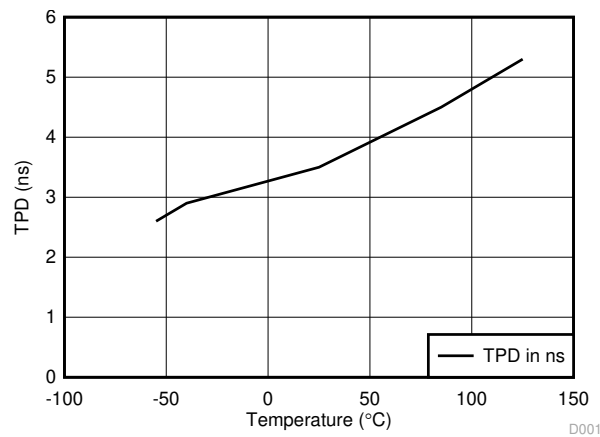
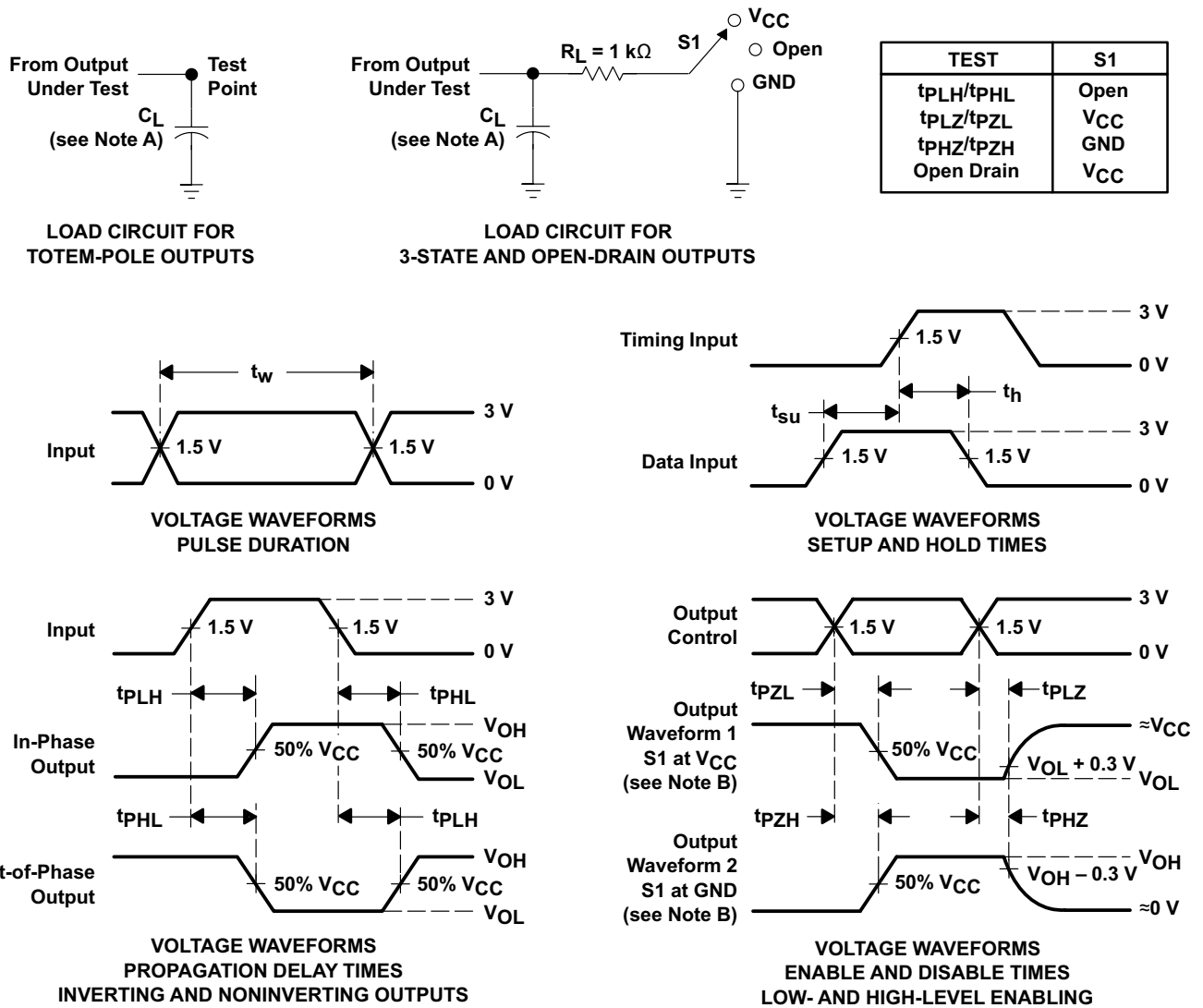


图 5-1. TPD vs Temperature, 50 pF Load

## 6 Parameter Measurement Information



- NOTES: A.  $C_L$  includes probe and jig capacitance.  
 B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.  
 C. All input pulses are supplied by generators having the following characteristics: PRR  $\leq 1\text{ MHz}$ ,  $Z_O = 50\ \Omega$ ,  $t_r \leq 3\text{ ns}$ ,  $t_f \leq 3\text{ ns}$ .  
 D. The outputs are measured one at a time with one input transition per measurement.  
 E. All parameters and waveforms are not applicable to all devices.

图 6-1. Load Circuit and Voltage Waveforms

## 7 Detailed Description

### 7.1 Overview

The SN74AHCT367 device is designed specifically to improve both the performance and density of 3-state memory address drivers, clock drivers, and bus-oriented receivers and transmitters. This device is organized as a dual 4-line and 2-line buffer/driver with active-low output-enable (1  $\overline{OE}$  and 2  $\overline{OE}$ ) inputs. When  $\overline{OE}$  is low, the device passes noninverted data from the A inputs to the Y outputs. When  $\overline{OE}$  is high, the outputs are in the high-impedance state.

To ensure the high-impedance state during power up or power down,  $\overline{OE}$  should be tied to  $V_{CC}$  through a pull-up resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

### 7.2 Functional Block Diagram

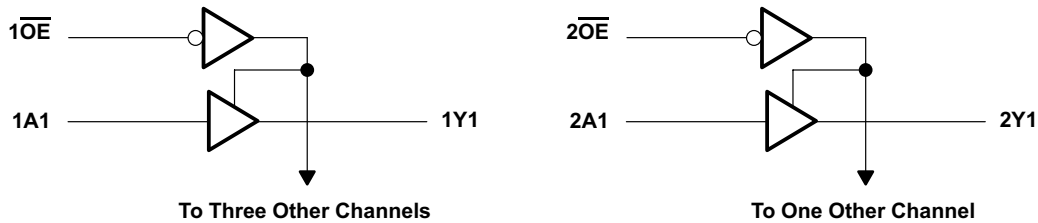


图 7-1. Logic Diagram (Positive Logic)

### 7.3 Feature Description

- $V_{CC}$  is optimized at 5 V
- Allows up voltage translation from 3.3 V to 5 V
  - Inputs Accept  $V_{IH}$  levels of 2 V
- Slow edge rates minimize output ringing
- Inputs are TTL-Voltage compatible

### 7.4 Device Functional Modes

表 7-1. Function Table  
(Each Buffer/Driver)

INPUTS		OUTPUT Y
$\overline{OE}$	A	
H	X	Z
L	H	H
L	L	L



## 8 Application and Implementation

### 备注

以下应用部分中的信息不属于 TI 器件规格的范围，TI 不担保其准确性和完整性。TI 的客户应负责确定器件是否适用于其应用。客户应验证并测试其设计，以确保系统功能。

### 8.1 Application Information

SN74AHCT367 is a low-drive CMOS device that can be used for a multitude of bus interface type applications where output ringing is a concern. The low drive and slow edge rates will minimize overshoot and undershoot on the outputs. The input switching levels have been lowered to accommodate TTL inputs of 0.8-V  $V_{IL}$  and 2-V  $V_{IH}$ . This feature makes it ideal for translating up from 3.3 V to 5 V. 图 8-2 shows this type of translation.

### 8.2 Typical Application

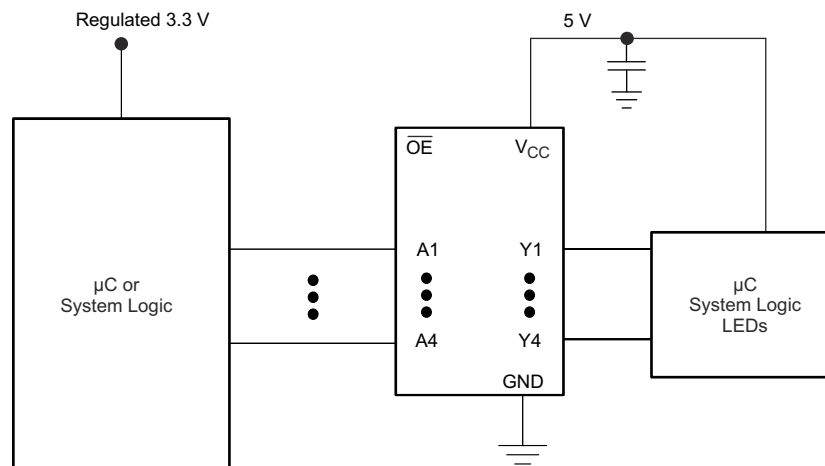


图 8-1. Typical Application Schematic

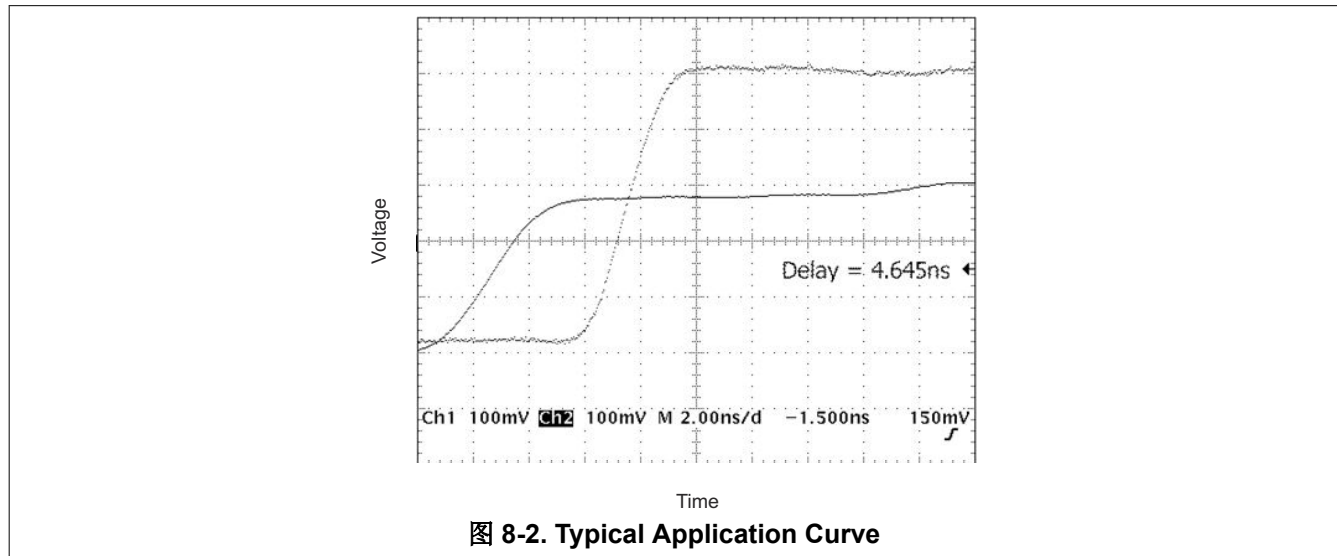
#### 8.2.1 Design Requirements

This device uses CMOS technology and has balanced output drive. Care should be taken to avoid bus contention because it can drive currents that would exceed maximum limits. The high drive will also create fast edges into light loads, so routing and load conditions should be considered to prevent ringing.

#### 8.2.2 Detailed Design Procedure

1. Recommended Input Conditions
  - For rise time and fall time specifications, see  $\Delta t / \Delta V$  in the 节 5.3 table.
  - For specified High and low levels, see  $V_{IH}$  and  $V_{IL}$  in the 节 5.3 table.
  - Inputs are overvoltage tolerant allowing them to go as high as 5.5 V at any valid  $V_{CC}$ .
2. Recommend Output Conditions
  - Load currents should not exceed 25 mA per output and 75 mA total for the part.
  - Outputs should not be pulled above  $V_{CC}$ .

### 8.2.3 Application Curves



## 8.3 Power Supply Recommendations

### 8.4 Layout

#### 8.4.1 Layout Guidelines

When using multiple bit logic devices, inputs should not float. In many cases, functions or parts of functions of digital logic devices are unused. Some examples are when only two inputs of a triple-input AND gate are used, or when only 3 of the 4-buffer gates are used. Such input pins should not be left unconnected because the undefined voltages at the outside connections result in undefined operational states.

Specified in 图 8-3 are rules that must be observed under all circumstances. All unused inputs of digital logic devices must be connected to a high or low bias to prevent them from floating. The logic level that should be applied to any particular unused input depends on the function of the device. Generally they will be tied to GND or  $V_{CC}$ , whichever makes more sense or is more convenient. It is acceptable to float outputs unless the part is a transceiver. If the transceiver has an output enable pin, it will disable the outputs section of the part when asserted. This will not disable the input section of the I/Os so they also cannot float when disabled.

### 8.4.2 Layout Example

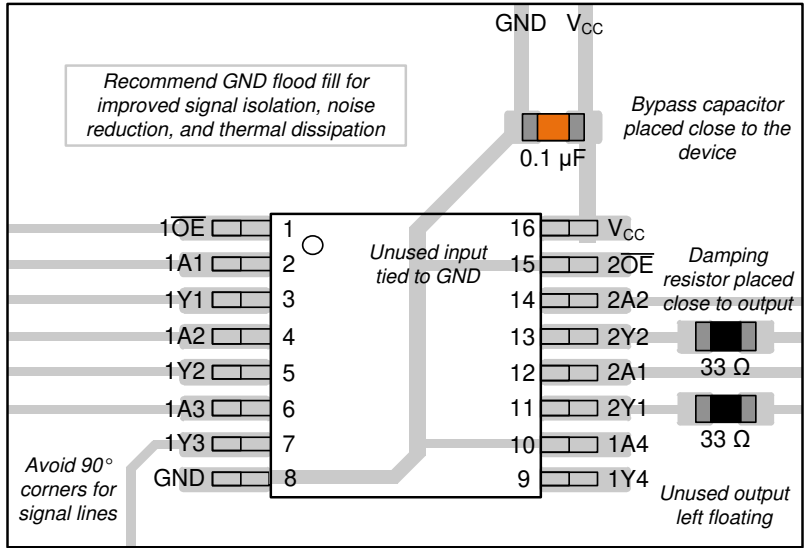


图 8-3. Example Layout for the SN74AHCT367 in the PW Package

## 9 Device and Documentation Support

### 9.1 Documentation Support

#### 9.1.1 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

表 9-1. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
SN74AHCT367	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>

### 9.2 接收文档更新通知

要接收文档更新通知，请导航至 [ti.com](http://ti.com) 上的器件产品文件夹。点击 [通知](#) 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

### 9.3 支持资源

[TI E2E™ 中文支持论坛](#) 是工程师的重要参考资料，可直接从专家处获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题，获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的 [使用条款](#)。

### 9.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.

所有商标均为其各自所有者的财产。

### 9.5 静电放电警告



静电放电 (ESD) 会损坏这个集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

### 9.6 术语表

[TI 术语表](#) 本术语表列出并解释了术语、首字母缩略词和定义。

## 10 Revision History

Changes from Revision H (December 2014) to Revision I (July 2024)	Page
• 删除了 <i>特性</i> 部分中的机器放电模型.....	1
• 更新了封装并向 <i>封装信息</i> 表中添加了封装尺寸.....	1
• 根据当前标准更新了数据表的结构布局.....	1
• Updated R <sup>θ</sup> JA values: D = 85.1 to 93.8, PW = 111.5 to 135.9; Updated D and PW packages for R <sup>θ</sup> JC(top), R <sup>θ</sup> JB, ΨJT, ΨJB, and R <sup>θ</sup> JC(bot), all values in °C/W .....	5
• Updated <i>Layout Example</i> figure.....	11

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**Changes from Revision G (July 2003) to Revision H (December 2014) Page**

- 添加了应用、器件信息表、引脚功能表、ESD 等级表、热性能信息表、典型特性、特性说明部分、器件功能模式、应用和实施部分、电源相关建议部分、布局部分、器件和文档支持部分以及机械、封装和可订购信息部分.....1
- 删除了订购信息表.....1
- MAX operating temperature to 125°C in *Recommended Operating Conditions* table.....4

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## 11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74AHCT367D	OBSOLETE	SOIC	D	16		TBD	Call TI	Call TI	-40 to 125	AHCT367	
SN74AHCT367DBR	ACTIVE	SSOP	DB	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HB367	Samples
SN74AHCT367DGVR	ACTIVE	TVSOP	DGV	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HB367	Samples
SN74AHCT367DR	ACTIVE	SOIC	D	16	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	AHCT367	Samples
SN74AHCT367PW	OBSOLETE	TSSOP	PW	16		TBD	Call TI	Call TI	-40 to 125	HB367	
SN74AHCT367PWR	ACTIVE	TSSOP	PW	16	2000	RoHS & Green	NIPDAU   SN	Level-1-260C-UNLIM	-40 to 125	HB367	Samples
SN74AHCT367PWRG4	ACTIVE	TSSOP	PW	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HB367	Samples

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74AHCT367DBR	SSOP	DB	16	2000	330.0	16.4	8.35	6.6	2.4	12.0	16.0	Q1
SN74AHCT367DGV	TVSOP	DGV	16	2000	330.0	12.4	6.8	4.0	1.6	8.0	12.0	Q1
SN74AHCT367DR	SOIC	D	16	2500	330.0	12.4	3.75	3.75	1.15	8.0	12.0	Q1
SN74AHCT367DR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
SN74AHCT367DR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
SN74AHCT367PWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74AHCT367PWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74AHCT367PWRG4	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74AHCT367PWRG4	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1



**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74AHCT367DBR	SSOP	DB	16	2000	356.0	356.0	35.0
SN74AHCT367DGVR	TVSOP	DGV	16	2000	356.0	356.0	35.0
SN74AHCT367DR	SOIC	D	16	2500	340.5	336.1	32.0
SN74AHCT367DR	SOIC	D	16	2500	353.0	353.0	32.0
SN74AHCT367DR	SOIC	D	16	2500	353.0	353.0	32.0
SN74AHCT367PWR	TSSOP	PW	16	2000	353.0	353.0	32.0
SN74AHCT367PWR	TSSOP	PW	16	2000	356.0	356.0	35.0
SN74AHCT367PWRG4	TSSOP	PW	16	2000	353.0	353.0	32.0
SN74AHCT367PWRG4	TSSOP	PW	16	2000	356.0	356.0	35.0

DGV (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE

24 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.  
 D. Falls within JEDEC: 24/48 Pins – MO-153  
 14/16/20/56 Pins – MO-194

D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



4040047-6/M 06/11

- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  -  Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
  -  Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
  - E. Reference JEDEC MS-012 variation AC.



4220204/A 02/2017

**NOTES:**

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

# EXAMPLE BOARD LAYOUT

PW0016A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 10X



4220204/A 02/2017

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

PW0016A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE: 10X

4220204/A 02/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

# DB0016A



# PACKAGE OUTLINE

## SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



4220763/A 05/2022

### NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-150.

# EXAMPLE BOARD LAYOUT

DB0016A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 10X



4220763/A 05/2022

NOTES: (continued)

- 5. Publication IPC-7351 may have alternate designs.
- 6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



# EXAMPLE STENCIL DESIGN

DB0016A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE: 10X

4220763/A 05/2022

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

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