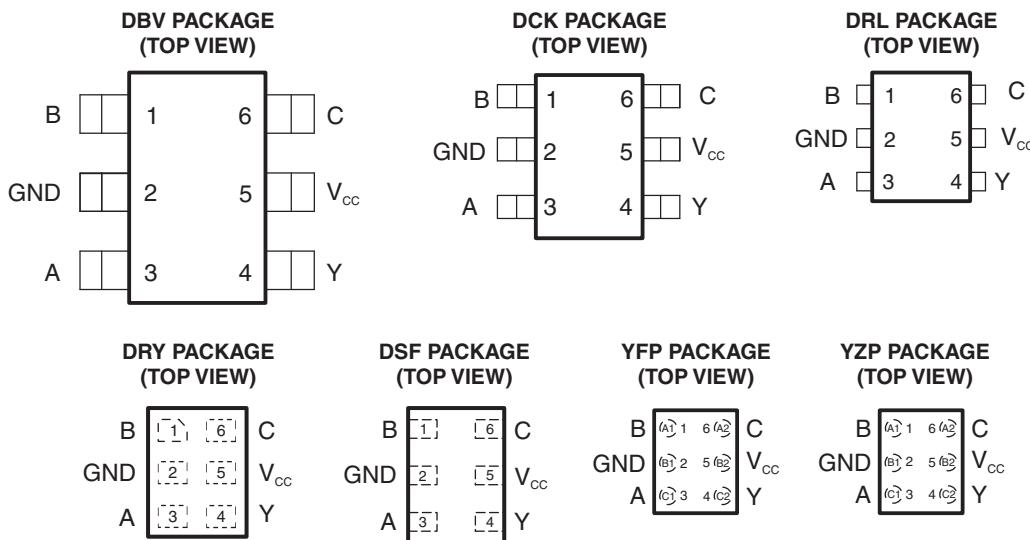


## LOW-POWER CONFIGURABLE MULTIPLE-FUNCTION GATE

Check for Samples: [SN74AUP1G97](#)

### FEATURES

- Available in the Texas Instruments NanoStar™ Package
- Low Static-Power Consumption ( $I_{cc} = 0.9 \mu A$  Max)
- Low Dynamic-Power Consumption ( $C_{pd} = 4.8 \text{ pF}$  Typ at 3.3 V)
- Low Input Capacitance ( $C_I = 1.5 \text{ pF}$  Typ)
- Low Noise – Overshoot and Undershoot <10% of  $V_{CC}$
- $I_{off}$  Supports Partial-Power-Down Mode Operation
- Includes Schmitt-Trigger Inputs
- Wide Operating  $V_{CC}$  Range of 0.8 V to 3.6 V
- Optimized for 3.3-V Operation
- 3.6-V I/O Tolerant to Support Mixed-Mode Signal Operation
- $t_{pd} = 5.6 \text{ ns}$  Max at 3.3 V
- Suitable for Point-to-Point Applications
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Performance Tested Per JESD 22
  - 2000-V Human-Body Model (A114-B, Class II)
  - 1000-V Charged-Device Model (C101)



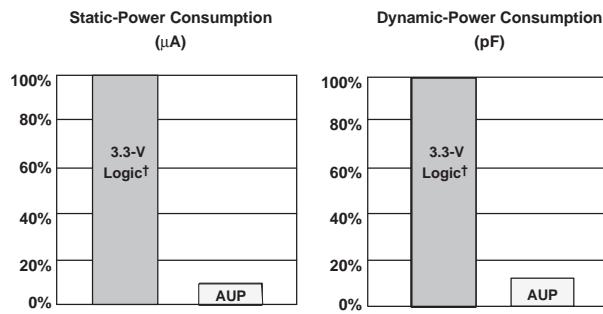
See mechanical drawings for dimensions.

### DESCRIPTION/ORDERING INFORMATION

The AUP family is TI's premier solution to the industry's low-power needs in battery-powered portable applications. This family ensures a very low static- and dynamic-power consumption across the entire  $V_{CC}$  range of 0.8 V to 3.6 V, resulting in increased battery life (see Figure 1). This product also maintains excellent signal integrity (see the very low undershoot and overshoot characteristics shown in Figure 2).

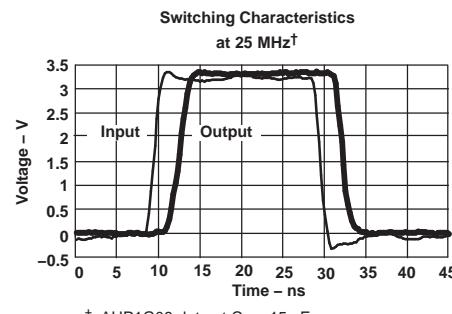


Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.



† Single, dual, and triple gates

**Figure 1. AUP – The Lowest-Power Family**



† AUP1G08 data at  $C_L = 15 \text{ pF}$

**Figure 2. Excellent Signal Integrity**

The SN74AUP1G97 features configurable multiple functions. The output state is determined by eight patterns of 3-bit input. The user can choose the logic functions MUX, AND, OR, NAND, NOR, inverter, and noninverter. All inputs can be connected to  $V_{CC}$  or GND.

The device functions as an independent gate with Schmitt-trigger inputs, which allows for slow input transition and better switching-noise immunity at the input.

NanoStar™ package technology is a major breakthrough in IC packaging concepts, using the die as the package.

This device is fully specified for partial-power-down applications using  $I_{off}$ . The  $I_{off}$  circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

### ORDERING INFORMATION<sup>(1)</sup>

$T_A$	PACKAGE <sup>(2)</sup>	ORDERABLE PART NUMBER	TOP-SIDE MARKING <sup>(3)</sup>
$-40^{\circ}\text{C}$ to $85^{\circ}\text{C}$	NanoStar™ – W CSP (DSBGA) 0.23-mm Large Bump – YFP (Pb-free)	Reel of 3000	SN74AUP1G97YFPR
	NanoStar™ – W CSP (DSBGA) 0.23-mm Large Bump – YZP (Pb-free)	Reel of 3000	SN74AUP1G97YZPR
	QFN – DRY	Reel of 5000	SN74AUP1G97DRYR
	uQFN – DSF	Reel of 5000	SN74AUP1G97DSFR
	SOT (SOT-23) – DBV	Reel of 3000	SN74AUP1G97DBVR
	SOT (SC-70) – DCK	Reel of 3000	SN74AUP1G97DCKR
	SOT (SOT-553) – DRL	Reel of 4000	SN74AUP1G97DRLR

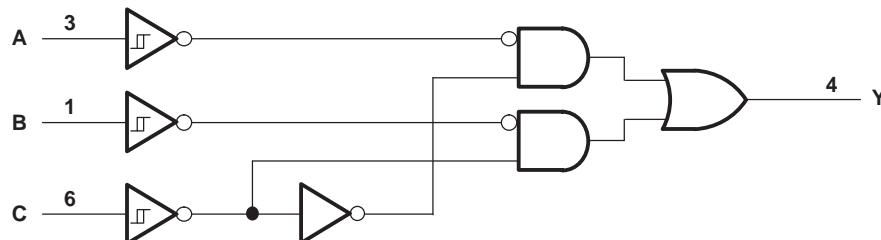
(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at [www.ti.com](http://www.ti.com).

(2) Package drawings, thermal data, and symbolization are available at [www.ti.com/packaging](http://www.ti.com/packaging).

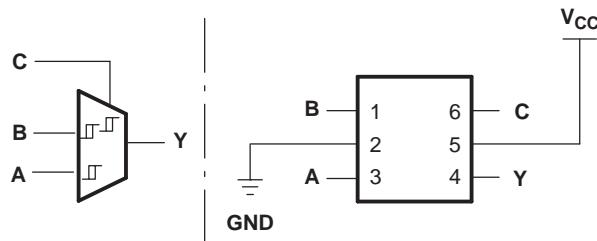
(3) DBV/DCK/DRL: The actual top-side marking has one additional character that designates the wafer fab/assembly site. YFP/YZP: The actual top-side marking has three preceding characters to denote year, month, and sequence code, and one following character to designate the wafer fab/assembly site. Pin 1 identifier indicates solder-bump composition (1 = SnPb, • = Pb-free).

### FUNCTION TABLE

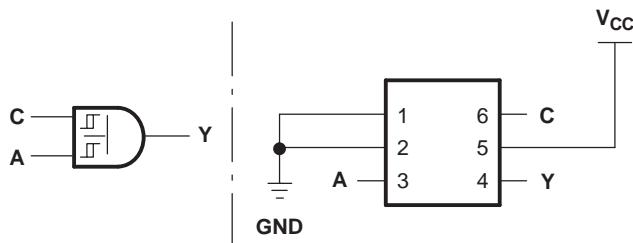
INPUTS			OUTPUT
C	B	A	Y
L	L	L	L
L	L	H	L
L	H	L	H
L	H	H	H
H	L	L	L
H	L	H	H
H	H	L	L
H	H	H	H

**LOGIC DIAGRAM (POSITIVE LOGIC)**

**FUNCTION SELECTION TABLE**

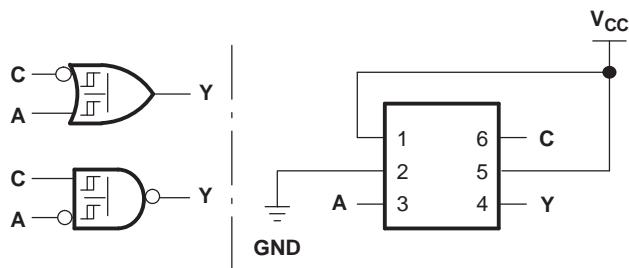
LOGIC FUNCTION	FIGURE NO.
2-to-1 data selector	3
2-input AND gate	4
2-input OR gate with one inverted input	5
2-input NAND gate with one inverted input	5
2-input AND gate with one inverted input	6
2-input NOR gate with one inverted input	6
2-input OR gate	7
Inverter	8
Noninverted buffer	9

**LOGIC CONFIGURATIONS**


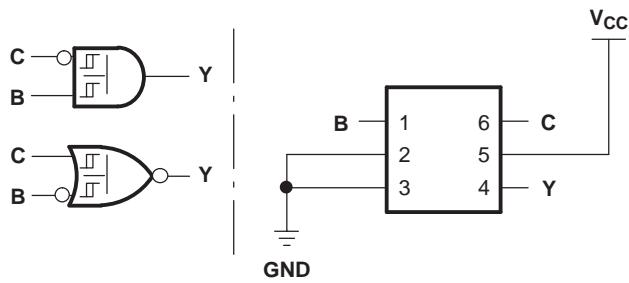
**Figure 3. 2-to-1 Data Selector**  
When C is L, Y = B; When C is H, Y = A



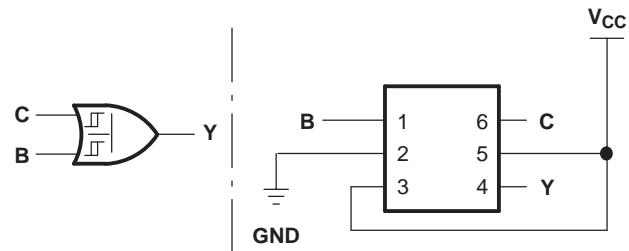
**Figure 4. 2-Input AND Gate**



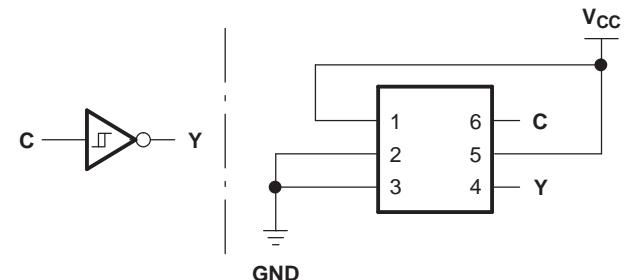
**Figure 5. Input OR Gate With One Inverted Input  
2-Input NAND Gate With One Inverted Input**



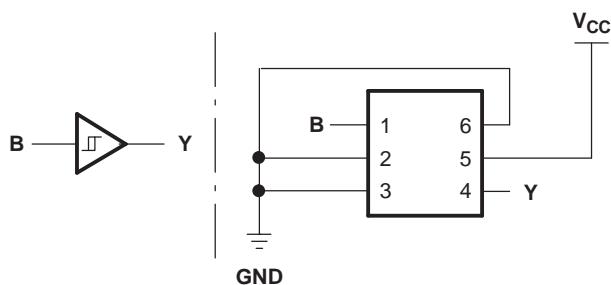
**Figure 6. 2-Input AND Gate With One Inverted Input  
2-Input NOR Gate With One Inverted Input**



**Figure 7. 2-Input OR Gate**



**Figure 8. Inverter**



**Figure 9. Noninverted Buffer**

**ABSOLUTE MAXIMUM RATINGS<sup>(1)</sup>**

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
$V_{CC}$	Supply voltage range	-0.5	4.6	V
$V_I$	Input voltage range <sup>(2)</sup>	-0.5	4.6	V
$V_O$	Voltage range applied to any output in the high-impedance or power-off state <sup>(2)</sup>	-0.5	4.6	V
$V_O$	Output voltage range in the high or low state <sup>(2)</sup>	-0.5	$V_{CC} + 0.5$	V
$I_{IK}$	Input clamp current	$V_I < 0$		-50 mA
$I_{OK}$	Output clamp current	$V_O < 0$		-50 mA
$I_O$	Continuous output current			$\pm 20$ mA
Continuous current through $V_{CC}$ or GND			$\pm 50$ mA	
$\theta_{JA}$	Package thermal impedance <sup>(3)</sup>	DBV package	165	°C/W
		DCK package	259	
		DRL package	142	
		DSF package	300	
		DRY package	234	
		YFP package	123	
		YZP package	123	
$T_{stg}$	Storage temperature range	-65		150 °C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.

(3) The package thermal impedance is calculated in accordance with JESD 51-7.

**RECOMMENDED OPERATING CONDITIONS<sup>(1)</sup>**

		MIN	MAX	UNIT
$V_{CC}$	Supply voltage	0.8	3.6	V
$V_I$	Input voltage	0	3.6	V
$V_O$	Output voltage	0	$V_{CC}$	V
$I_{OH}$	High-level output current	$V_{CC} = 0.8$ V	-20	$\mu A$
		$V_{CC} = 1.1$ V	-1.1	mA
		$V_{CC} = 1.4$ V	-1.7	
		$V_{CC} = 1.65$	-1.9	
		$V_{CC} = 2.3$ V	-3.1	
		$V_{CC} = 3$ V	-4	
$I_{OL}$	Low-level output current	$V_{CC} = 0.8$ V	20	$\mu A$
		$V_{CC} = 1.1$ V	1.1	mA
		$V_{CC} = 1.4$ V	1.7	
		$V_{CC} = 1.65$ V	1.9	
		$V_{CC} = 2.3$ V	3.1	
		$V_{CC} = 3$ V	4	
$T_A$	Operating free-air temperature	-40		85 °C

(1) All unused inputs of the device must be held at  $V_{CC}$  or GND to ensure proper device operation. See the TI application report *Implications of Slow or Floating CMOS Inputs*, literature number [SCBA004](#).

## ELECTRICAL CHARACTERISTICS

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V <sub>CC</sub>	T <sub>A</sub> = 25°C			T <sub>A</sub> = -40°C to 85°C		UNIT
			MIN	TYP	MAX	MIN	MAX	
V <sub>T+</sub> Positive-going input threshold voltage		0.8 V	0.3	0.6	0.6	0.3	0.6	V
		1.1 V	0.53	0.9	0.9	0.53	0.9	
		1.4 V	0.74	1.11	1.11	0.74	1.11	
		1.65 V	0.91	1.29	1.29	0.91	1.29	
		2.3 V	1.37	1.77	1.77	1.37	1.77	
		3 V	1.88	2.29	2.29	1.88	2.29	
V <sub>T-</sub> Negative-going input threshold voltage		0.8 V	0.1	0.6	0.6	0.1	0.6	V
		1.1 V	0.26	0.65	0.65	0.26	0.65	
		1.4 V	0.39	0.75	0.75	0.39	0.75	
		1.65 V	0.47	0.84	0.84	0.47	0.84	
		2.3 V	0.69	1.04	1.04	0.69	1.04	
		3 V	0.88	1.24	1.24	0.88	1.24	
ΔV <sub>T</sub> Hysteresis (V <sub>T+</sub> – V <sub>T-</sub> )		0.8 V	0.07	0.5	0.5	0.07	0.5	V
		1.1 V	0.08	0.46	0.46	0.08	0.46	
		1.4 V	0.18	0.56	0.56	0.18	0.56	
		1.65 V	0.27	0.66	0.66	0.27	0.66	
		2.3 V	0.53	0.92	0.92	0.53	0.92	
		3 V	0.79	1.31	1.31	0.79	1.31	
V <sub>OH</sub>	I <sub>OH</sub> = -20 μA	0.8 V to 3.6 V	V <sub>CC</sub> – 0.1		V <sub>CC</sub> – 0.1			V
	I <sub>OH</sub> = -1.1 mA	1.1 V	0.75 × V <sub>CC</sub>		0.7 × V <sub>CC</sub>			
	I <sub>OH</sub> = -1.7 mA	1.4 V	1.11		1.03			
	I <sub>OH</sub> = -1.9 mA	1.65 V	1.32		1.3			
	I <sub>OH</sub> = -2.3 mA	2.3 V	2.05		1.97			
	I <sub>OH</sub> = -3.1 mA		1.9		1.85			
	I <sub>OH</sub> = -2.7 mA	3 V	2.72		2.67			
	I <sub>OH</sub> = -4 mA		2.6		2.55			
V <sub>OL</sub>	I <sub>OL</sub> = 20 μA	0.8 V to 3.6 V		0.1		0.1		V
	I <sub>OL</sub> = 1.1 mA	1.1 V		0.3 × V <sub>CC</sub>		0.3 × V <sub>CC</sub>		
	I <sub>OL</sub> = 1.7 mA	1.4 V		0.31		0.37		
	I <sub>OL</sub> = 1.9 mA	1.65 V		0.31		0.35		
	I <sub>OL</sub> = 2.3 mA	2.3 V		0.31		0.33		
	I <sub>OL</sub> = 3.1 mA			0.44		0.45		
	I <sub>OL</sub> = 2.7 mA	3 V		0.31		0.33		
	I <sub>OL</sub> = 4 mA			0.44		0.45		
I <sub>I</sub>	All inputs	V <sub>I</sub> = GND to 3.6 V	0 V to 3.6 V		0.1		0.5	μA
I <sub>off</sub>		V <sub>I</sub> or V <sub>O</sub> = 0 V to 3.6 V	0 V		0.2		0.6	μA
ΔI <sub>off</sub>		V <sub>I</sub> or V <sub>O</sub> = 0 V to 3.6 V	0 V to 0.2 V		0.2		0.6	μA
I <sub>CC</sub>		V <sub>I</sub> = GND or (V <sub>CC</sub> to 3.6 V), I <sub>O</sub> = 0	0.8 V to 3.6 V		0.5		0.9	μA
ΔI <sub>CC</sub>		V <sub>I</sub> = V <sub>CC</sub> – 0.6 V <sup>(1)</sup> , I <sub>O</sub> = 0	3.3 V		40		50	μA
C <sub>i</sub>		V <sub>I</sub> = V <sub>CC</sub> or GND	0 V		1.5			pF
			3.6 V		1.5			
C <sub>o</sub>		V <sub>O</sub> = GND	0 V		3			pF

(1) One input at V<sub>CC</sub> – 0.6 V, other inputs at V<sub>CC</sub> or GND.

## SWITCHING CHARACTERISTICS

over recommended operating free-air temperature range,  $C_L = 5 \text{ pF}$  (unless otherwise noted) (see [Figure 10](#) and [Figure 11](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC}$	$T_A = 25^\circ\text{C}$			$T_A = -40^\circ\text{C} \text{ to } 85^\circ\text{C}$		UNIT
				MIN	TYP	MAX	MIN	MAX	
$t_{pd}$	A, B, or C	Y	0.8 V		23.1				ns
			$1.2 \text{ V} \pm 0.1 \text{ V}$	3.1	9.1	13.9	2.6	17.6	
			$1.5 \text{ V} \pm 0.1 \text{ V}$	2.1	6.4	9.4	1.6	11.4	
			$1.8 \text{ V} \pm 0.15 \text{ V}$	1.6	5.1	7.5	1.1	9.2	
			$2.5 \text{ V} \pm 0.2 \text{ V}$	1.1	3.6	5.7	0.6	6.8	
			$3.3 \text{ V} \pm 0.3 \text{ V}$	1	2.8	4.7	0.5	5.6	

## SWITCHING CHARACTERISTICS

over recommended operating free-air temperature range,  $C_L = 10 \text{ pF}$  (unless otherwise noted) (see [Figure 10](#) and [Figure 11](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC}$	$T_A = 25^\circ\text{C}$			$T_A = -40^\circ\text{C} \text{ to } 85^\circ\text{C}$		UNIT
				MIN	TYP	MAX	MIN	MAX	
$t_{pd}$	A, B, or C	Y	0.8 V		26.2				ns
			$1.2 \text{ V} \pm 0.1 \text{ V}$	5.2	10.4	15.4	4.7	19.2	
			$1.5 \text{ V} \pm 0.1 \text{ V}$	4	7.4	10.7	3.5	12.7	
			$1.8 \text{ V} \pm 0.15 \text{ V}$	3.1	6	8.6	2.6	10.5	
			$2.5 \text{ V} \pm 0.2 \text{ V}$	2.7	4.3	6.5	2.2	7.8	
			$3.3 \text{ V} \pm 0.3 \text{ V}$	2.5	3.4	5.4	2	6.4	

## SWITCHING CHARACTERISTICS

over recommended operating free-air temperature range,  $C_L = 15 \text{ pF}$  (unless otherwise noted) (see [Figure 10](#) and [Figure 11](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC}$	$T_A = 25^\circ\text{C}$			$T_A = -40^\circ\text{C} \text{ to } 85^\circ\text{C}$		UNIT
				MIN	TYP	MAX	MIN	MAX	
$t_{pd}$	A, B, or C	Y	0.8 V		28.9				ns
			$1.2 \text{ V} \pm 0.1 \text{ V}$	4.1	11.5	16.8	3.6	21.3	
			$1.5 \text{ V} \pm 0.1 \text{ V}$	3	8.3	11.8	2.5	14.1	
			$1.8 \text{ V} \pm 0.15 \text{ V}$	2.3	6.7	9.5	1.8	11.6	
			$2.5 \text{ V} \pm 0.2 \text{ V}$	1.7	4.8	7.2	1.2	8.6	
			$3.3 \text{ V} \pm 0.3 \text{ V}$	1.4	3.9	6	0.9	7.1	

## SWITCHING CHARACTERISTICS

over recommended operating free-air temperature range,  $C_L = 30 \text{ pF}$  (unless otherwise noted) (see [Figure 10](#) and [Figure 11](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC}$	$T_A = 25^\circ\text{C}$			$T_A = -40^\circ\text{C} \text{ to } 85^\circ\text{C}$		UNIT
				MIN	TYP	MAX	MIN	MAX	
$t_{pd}$	A, B, or C	Y	0.8 V		36.7				ns
			$1.2 \text{ V} \pm 0.1 \text{ V}$	5.5	14.6	21.4	5	26.7	
			$1.5 \text{ V} \pm 0.1 \text{ V}$	4.1	10.5	14.8	3.6	17.7	
			$1.8 \text{ V} \pm 0.15 \text{ V}$	3.3	8.6	11.8	2.8	14.5	
			$2.5 \text{ V} \pm 0.2 \text{ V}$	2.5	6.3	8.8	2	10.6	
			$3.3 \text{ V} \pm 0.3 \text{ V}$	2.1	5.1	7.3	1.6	8.8	

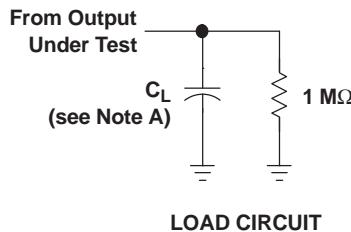
## OPERATING CHARACTERISTICS

 $T_A = 25^\circ\text{C}$ 

PARAMETER	TEST CONDITIONS	V <sub>CC</sub>	TYP	UNIT
C <sub>pd</sub> Power dissipation capacitance	f = 10 MHz	0.8 V	4	pF
		1.2 V $\pm$ 0.1 V	4	
		1.5 V $\pm$ 0.1 V	4	
		1.8 V $\pm$ 0.15 V	4	
		2.5 V $\pm$ 0.2 V	4.4	
		3.3 V $\pm$ 0.3 V	4.8	

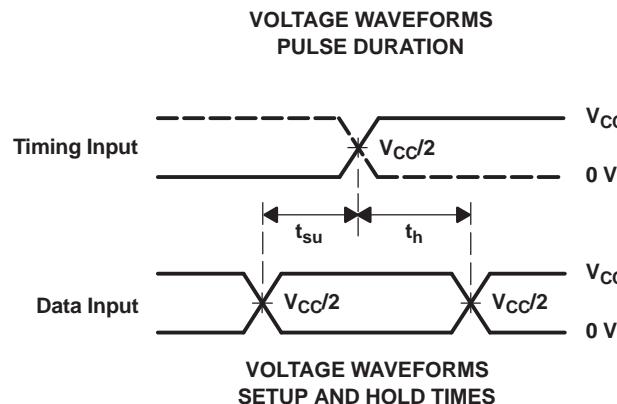
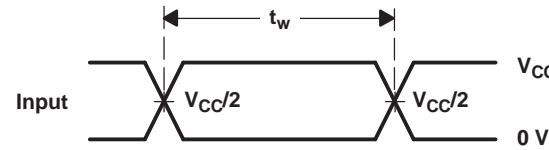
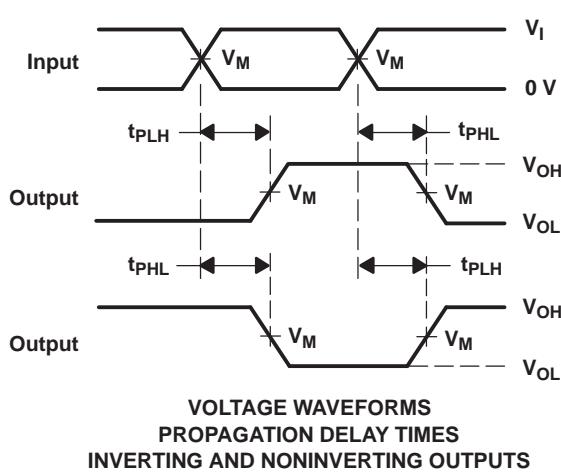
### PARAMETER MEASUREMENT INFORMATION

(Propagation Delays, Setup and Hold Times, and Pulse Duration)



LOAD CIRCUIT

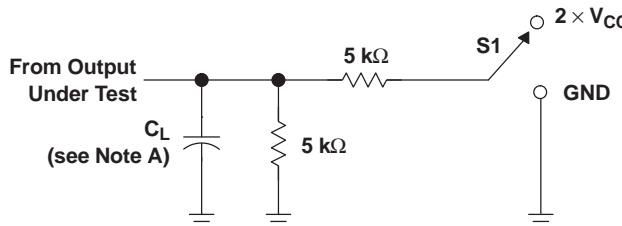
	$V_{CC} = 0.8 \text{ V}$	$V_{CC} = 1.2 \text{ V} \pm 0.1 \text{ V}$	$V_{CC} = 1.5 \text{ V} \pm 0.1 \text{ V}$	$V_{CC} = 1.8 \text{ V} \pm 0.15 \text{ V}$	$V_{CC} = 2.5 \text{ V} \pm 0.2 \text{ V}$	$V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$
$C_L$	5, 10, 15, 30 pF	5, 10, 15, 30 pF	5, 10, 15, 30 pF	5, 10, 15, 30 pF	5, 10, 15, 30 pF	5, 10, 15, 30 pF
$V_M$	$V_{CC}/2$	$V_{CC}/2$	$V_{CC}/2$	$V_{CC}/2$	$V_{CC}/2$	$V_{CC}/2$
$V_I$	$V_{CC}$	$V_{CC}$	$V_{CC}$	$V_{CC}$	$V_{CC}$	$V_{CC}$



NOTES:

- $C_L$  includes probe and jig capacitance.
- All input pulses are supplied by generators having the following characteristics: PRR  $\leq 10 \text{ MHz}$ ,  $Z_O = 50 \Omega$ , slew rate  $\geq 1 \text{ V/ns}$ .
- The outputs are measured one at a time, with one transition per measurement.
- $t_{PLH}$  and  $t_{PHL}$  are the same as  $t_{pd}$ .
- All parameters and waveforms are not applicable to all devices.

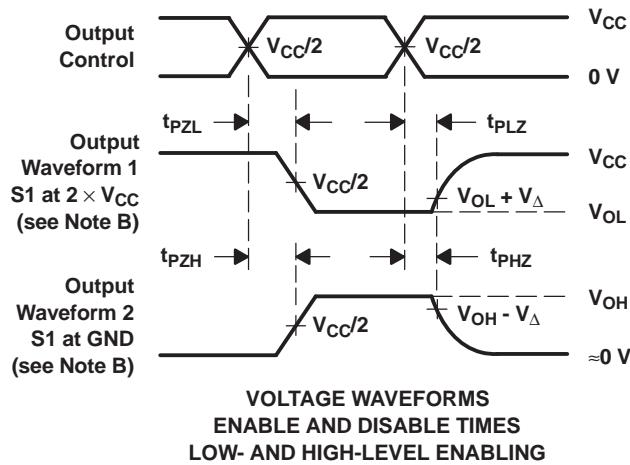
Figure 10. Load Circuit and Voltage Waveforms

**PARAMETER MEASUREMENT INFORMATION  
(Enable and Disable Times)**


TEST	S1
$t_{PLZ}/t_{PZL}$	$2 \times V_{CC}$
$t_{PHZ}/t_{PZH}$	GND

**LOAD CIRCUIT**

	$V_{CC} = 0.8 \text{ V}$	$V_{CC} = 1.2 \text{ V} \pm 0.1 \text{ V}$	$V_{CC} = 1.5 \text{ V} \pm 0.1 \text{ V}$	$V_{CC} = 1.8 \text{ V} \pm 0.15 \text{ V}$	$V_{CC} = 2.5 \text{ V} \pm 0.2 \text{ V}$	$V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$
$C_L$	5, 10, 15, 30 pF	5, 10, 15, 30 pF	5, 10, 15, 30 pF	5, 10, 15, 30 pF	5, 10, 15, 30 pF	5, 10, 15, 30 pF
$V_M$	$V_{CC}/2$	$V_{CC}/2$	$V_{CC}/2$	$V_{CC}/2$	$V_{CC}/2$	$V_{CC}/2$
$V_I$	$V_{CC}$	$V_{CC}$	$V_{CC}$	$V_{CC}$	$V_{CC}$	$V_{CC}$
$V_\Delta$	0.1 V	0.1 V	0.1 V	0.15 V	0.15 V	0.3 V


**VOLTAGE WAVEFORMS  
ENABLE AND DISABLE TIMES  
LOW- AND HIGH-LEVEL ENABLING**

NOTES:

- $C_L$  includes probe and jig capacitance.
- Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
- All input pulses are supplied by generators having the following characteristics:  $PRR \leq 10 \text{ MHz}$ ,  $Z_O = 50 \Omega$ , slew rate  $\geq 1 \text{ V/ns}$ .
- The outputs are measured one at a time, with one transition per measurement.
- $t_{PLZ}$  and  $t_{PHZ}$  are the same as  $t_{dis}$ .
- $t_{PZL}$  and  $t_{PZH}$  are the same as  $t_{en}$ .
- All parameters and waveforms are not applicable to all devices.

**Figure 11. Load Circuit and Voltage Waveforms**

**PACKAGING INFORMATION**

Orderable part number	Status (1)	Material type (2)	Package   Pins	Package qty   Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
<a href="#">SN74AUP1G97DBVR</a>	Active	Production	SOT-23 (DBV)   6	3000   LARGE T&R	Yes	NIPDAU   SN	Level-1-260C-UNLIM	-40 to 85	(H97F, H97R)
SN74AUP1G97DBVR.B	Active	Production	SOT-23 (DBV)   6	3000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	(H97F, H97R)
<a href="#">SN74AUP1G97DBVT</a>	Active	Production	SOT-23 (DBV)   6	250   SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	H97R
SN74AUP1G97DBVT.B	Active	Production	SOT-23 (DBV)   6	250   SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	H97R
<a href="#">SN74AUP1G97DCKR</a>	Active	Production	SC70 (DCK)   6	3000   LARGE T&R	Yes	NIPDAU   SN	Level-1-260C-UNLIM	-40 to 85	(HP5, HPF, HPR)
SN74AUP1G97DCKR.B	Active	Production	SC70 (DCK)   6	3000   LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	(HP5, HPF, HPR)
<a href="#">SN74AUP1G97DCKT</a>	Active	Production	SC70 (DCK)   6	250   SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	(HP5, HPR)
SN74AUP1G97DCKT.B	Active	Production	SC70 (DCK)   6	250   SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	(HP5, HPR)
SN74AUP1G97DCKTG4	Active	Production	SC70 (DCK)   6	250   SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	(HP5, HPR)
<a href="#">SN74AUP1G97DRLR</a>	Active	Production	SOT-5X3 (DRL)   6	4000   LARGE T&R	Yes	NIPDAU   NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	(1K9, HP7, HPR)
SN74AUP1G97DRLR.B	Active	Production	SOT-5X3 (DRL)   6	4000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	(1K9, HP7, HPR)
SN74AUP1G97DRLRG4	Active	Production	SOT-5X3 (DRL)   6	4000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	(1K9, HP7, HPR)
<a href="#">SN74AUP1G97DRYR</a>	Active	Production	SON (DRY)   6	5000   LARGE T&R	Yes	NIPDAU   NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	HP
SN74AUP1G97DRYR.B	Active	Production	SON (DRY)   6	5000   LARGE T&R	Yes	NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	HP
SN74AUP1G97DRYRG4	Active	Production	SON (DRY)   6	5000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HP
SN74AUP1G97DRYRG4.B	Active	Production	SON (DRY)   6	5000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HP
<a href="#">SN74AUP1G97DSFR</a>	Active	Production	SON (DSF)   6	5000   LARGE T&R	Yes	NIPDAU   NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	HP
SN74AUP1G97DSFR.B	Active	Production	SON (DSF)   6	5000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HP
SN74AUP1G97DSFRG4	Active	Production	SON (DSF)   6	5000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HP
SN74AUP1G97DSFRG4.B	Active	Production	SON (DSF)   6	5000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HP
<a href="#">SN74AUP1G97YFPR</a>	Active	Production	DSBGA (YFP)   6	3000   LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-	HPN
SN74AUP1G97YFPR.B	Active	Production	DSBGA (YFP)   6	3000   LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 85	HPN
<a href="#">SN74AUP1G97YZPR</a>	Active	Production	DSBGA (YZP)   6	3000   LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 85	HPN
SN74AUP1G97YZPR.B	Active	Production	DSBGA (YZP)   6	3000   LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 85	HPN

<sup>(1)</sup> **Status:** For more details on status, see our [product life cycle](#).

<sup>(2)</sup> **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

<sup>(3)</sup> **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

<sup>(4)</sup> **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

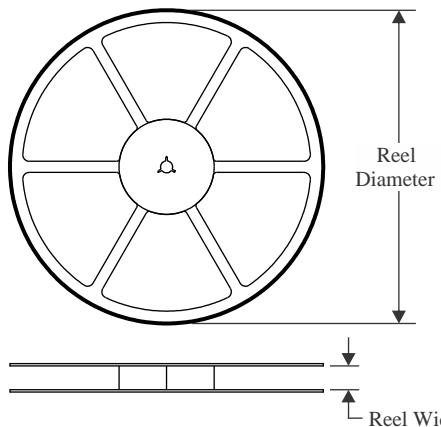
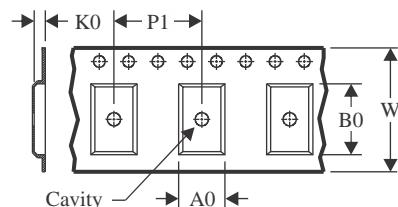
<sup>(5)</sup> **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

<sup>(6)</sup> **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

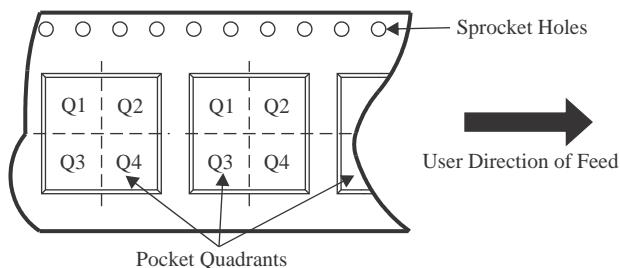
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

**Important Information and Disclaimer:** The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

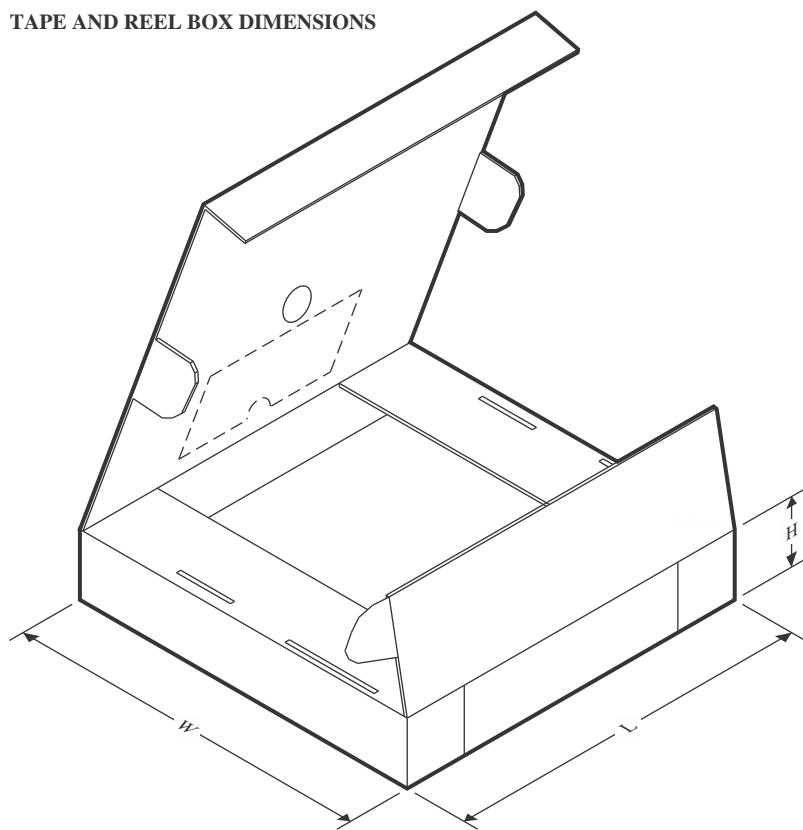
**TAPE AND REEL INFORMATION**
**REEL DIMENSIONS**

**TAPE DIMENSIONS**


A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74AUP1G97DBVR	SOT-23	DBV	6	3000	180.0	8.4	3.23	3.17	1.37	4.0	8.0	Q3
SN74AUP1G97DBVR	SOT-23	DBV	6	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
SN74AUP1G97DBVT	SOT-23	DBV	6	250	180.0	8.4	3.23	3.17	1.37	4.0	8.0	Q3
SN74AUP1G97DCKR	SC70	DCK	6	3000	178.0	8.4	2.25	2.45	1.2	4.0	8.0	Q3
SN74AUP1G97DCKT	SC70	DCK	6	250	178.0	9.2	2.4	2.4	1.22	4.0	8.0	Q3
SN74AUP1G97DCKT	SC70	DCK	6	250	180.0	8.4	2.41	2.41	1.2	4.0	8.0	Q3
SN74AUP1G97DRLR	SOT-5X3	DRL	6	4000	180.0	8.4	2.0	1.8	0.75	4.0	8.0	Q3
SN74AUP1G97DRYR	SON	DRY	6	5000	180.0	9.5	1.15	1.6	0.75	4.0	8.0	Q1
SN74AUP1G97DRYRG4	SON	DRY	6	5000	180.0	9.5	1.15	1.6	0.75	4.0	8.0	Q1
SN74AUP1G97DSFR	SON	DSF	6	5000	180.0	8.4	1.16	1.16	0.5	4.0	8.0	Q2
SN74AUP1G97DSFRG4	SON	DSF	6	5000	180.0	8.4	1.16	1.16	0.5	4.0	8.0	Q2
SN74AUP1G97YFPR	DSBGA	YFP	6	3000	178.0	9.2	0.89	1.29	0.62	4.0	8.0	Q1
SN74AUP1G97YZPR	DSBGA	YZP	6	3000	178.0	9.2	1.02	1.52	0.63	4.0	8.0	Q1

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74AUP1G97DBVR	SOT-23	DBV	6	3000	202.0	201.0	28.0
SN74AUP1G97DBVR	SOT-23	DBV	6	3000	180.0	180.0	18.0
SN74AUP1G97DBVT	SOT-23	DBV	6	250	202.0	201.0	28.0
SN74AUP1G97DCKR	SC70	DCK	6	3000	208.0	191.0	35.0
SN74AUP1G97DCKT	SC70	DCK	6	250	180.0	180.0	18.0
SN74AUP1G97DCKT	SC70	DCK	6	250	202.0	201.0	28.0
SN74AUP1G97DRLR	SOT-5X3	DRL	6	4000	210.0	185.0	35.0
SN74AUP1G97DRYR	SON	DRY	6	5000	184.0	184.0	19.0
SN74AUP1G97DRYRG4	SON	DRY	6	5000	184.0	184.0	19.0
SN74AUP1G97DSFR	SON	DSF	6	5000	210.0	185.0	35.0
SN74AUP1G97DSFRG4	SON	DSF	6	5000	210.0	185.0	35.0
SN74AUP1G97YFPR	DSBGA	YFP	6	3000	220.0	220.0	35.0
SN74AUP1G97YZPR	DSBGA	YZP	6	3000	220.0	220.0	35.0

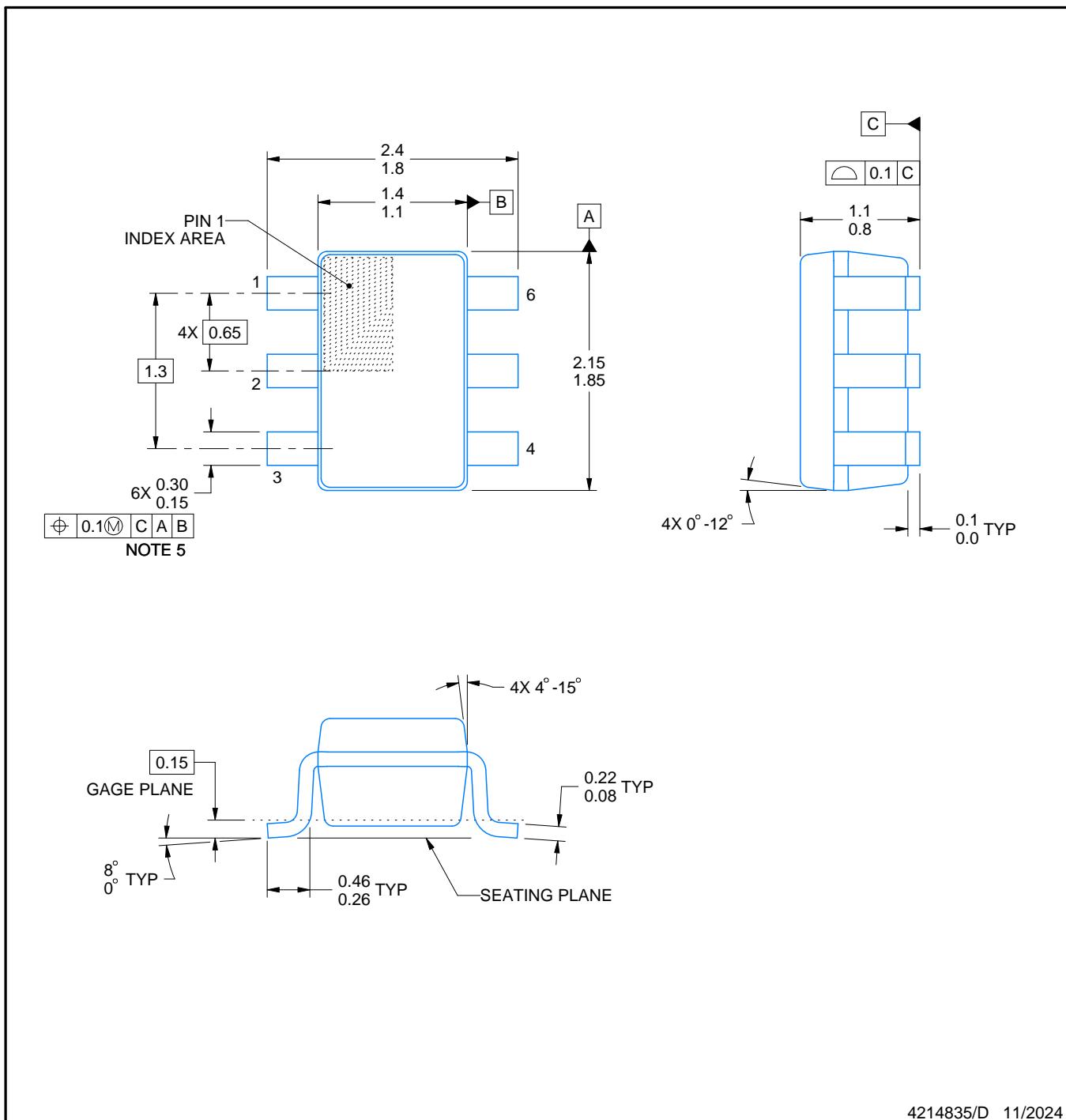
# PACKAGE OUTLINE

DCK0006A



SOT - 1.1 max height

SMALL OUTLINE TRANSISTOR



## NOTES:

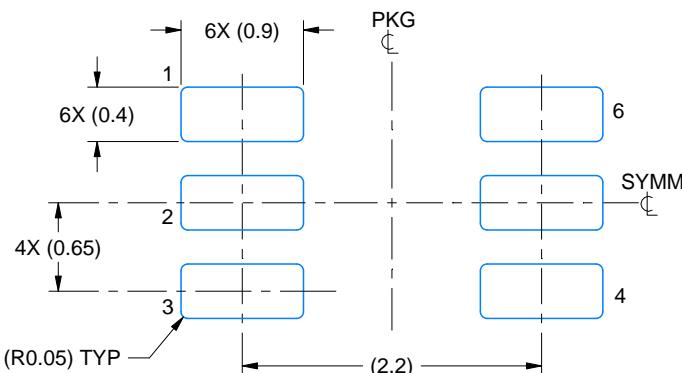
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
4. Falls within JEDEC MO-203 variation AB.

# EXAMPLE BOARD LAYOUT

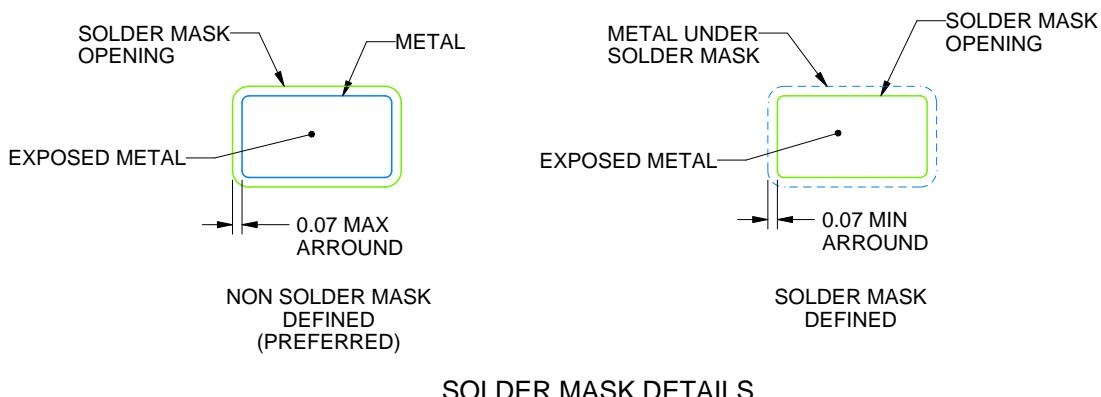
DCK0006A

SOT - 1.1 max height

SMALL OUTLINE TRANSISTOR



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE:18X



4214835/D 11/2024

NOTES: (continued)

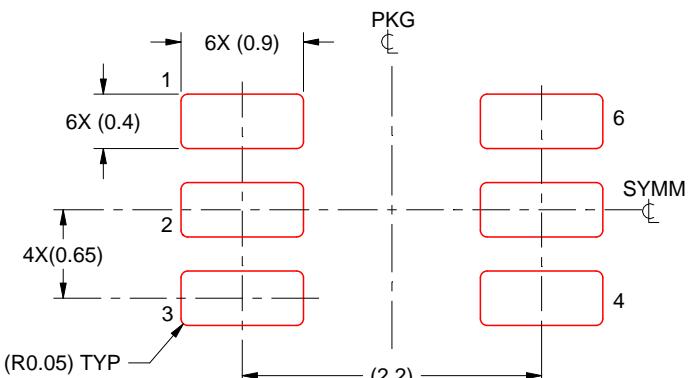
5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

DCK0006A

SOT - 1.1 max height

SMALL OUTLINE TRANSISTOR



SOLDER PASTE EXAMPLE  
BASED ON 0.125 THICK STENCIL  
SCALE:18X

4214835/D 11/2024

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

DRY 6

## GENERIC PACKAGE VIEW

### USON - 0.6 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



Images above are just a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.

4207181/G

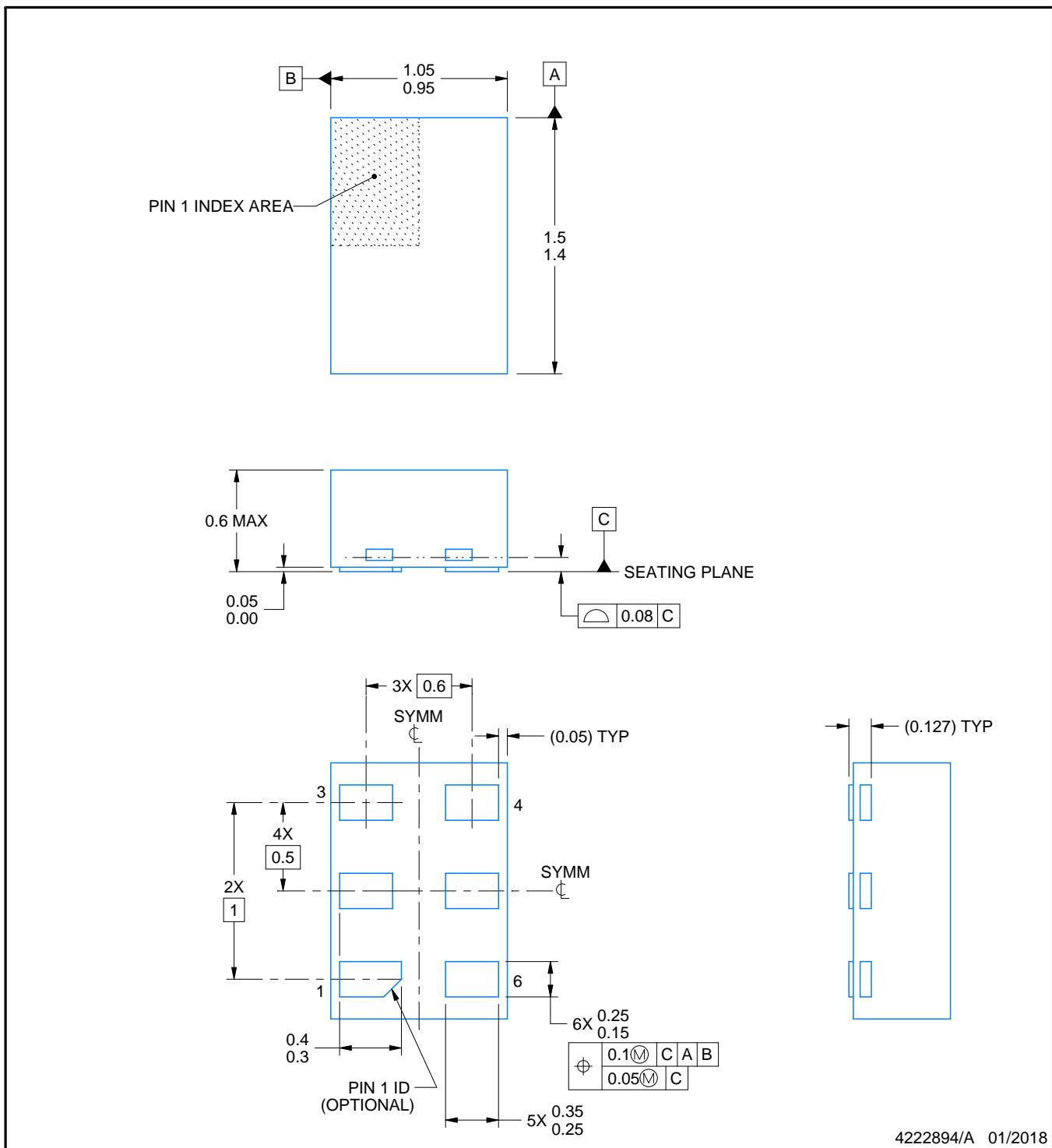
# PACKAGE OUTLINE

DRY0006A



USON - 0.6 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



4222894/A 01/2018

## NOTES:

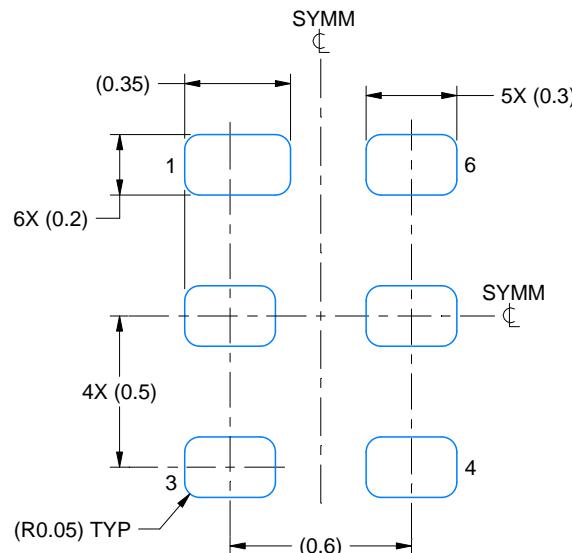
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

# EXAMPLE BOARD LAYOUT

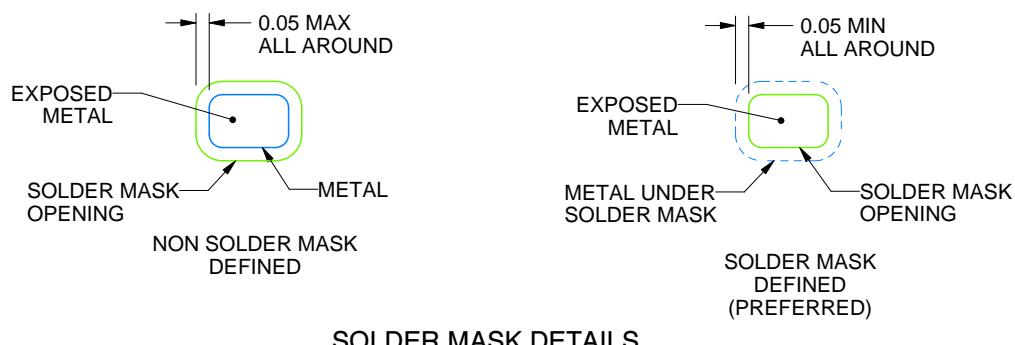
DRY0006A

USON - 0.6 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



LAND PATTERN EXAMPLE  
1:1 RATIO WITH PKG SOLDER PADS  
EXPOSED METAL SHOWN  
SCALE:40X



SOLDER MASK DETAILS

4222894/A 01/2018

NOTES: (continued)

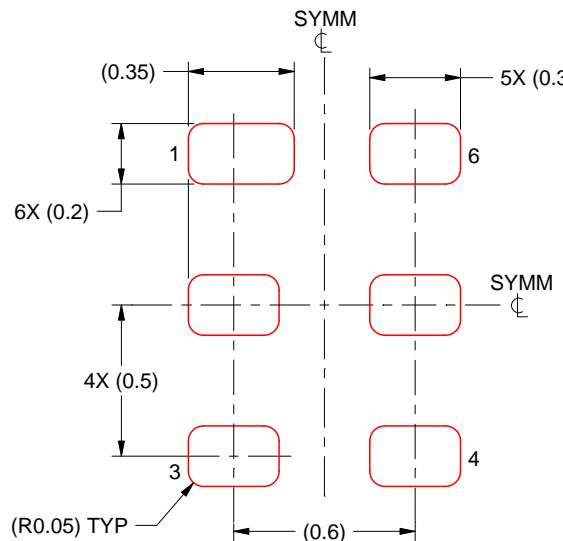
3. For more information, see QFN/SON PCB application report in literature No. SLUA271 ([www.ti.com/lit/slua271](http://www.ti.com/lit/slua271)).

# EXAMPLE STENCIL DESIGN

DRY0006A

USON - 0.6 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



SOLDER PASTE EXAMPLE  
BASED ON 0.075 - 0.1 mm THICK STENCIL  
SCALE:40X

4222894/A 01/2018

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

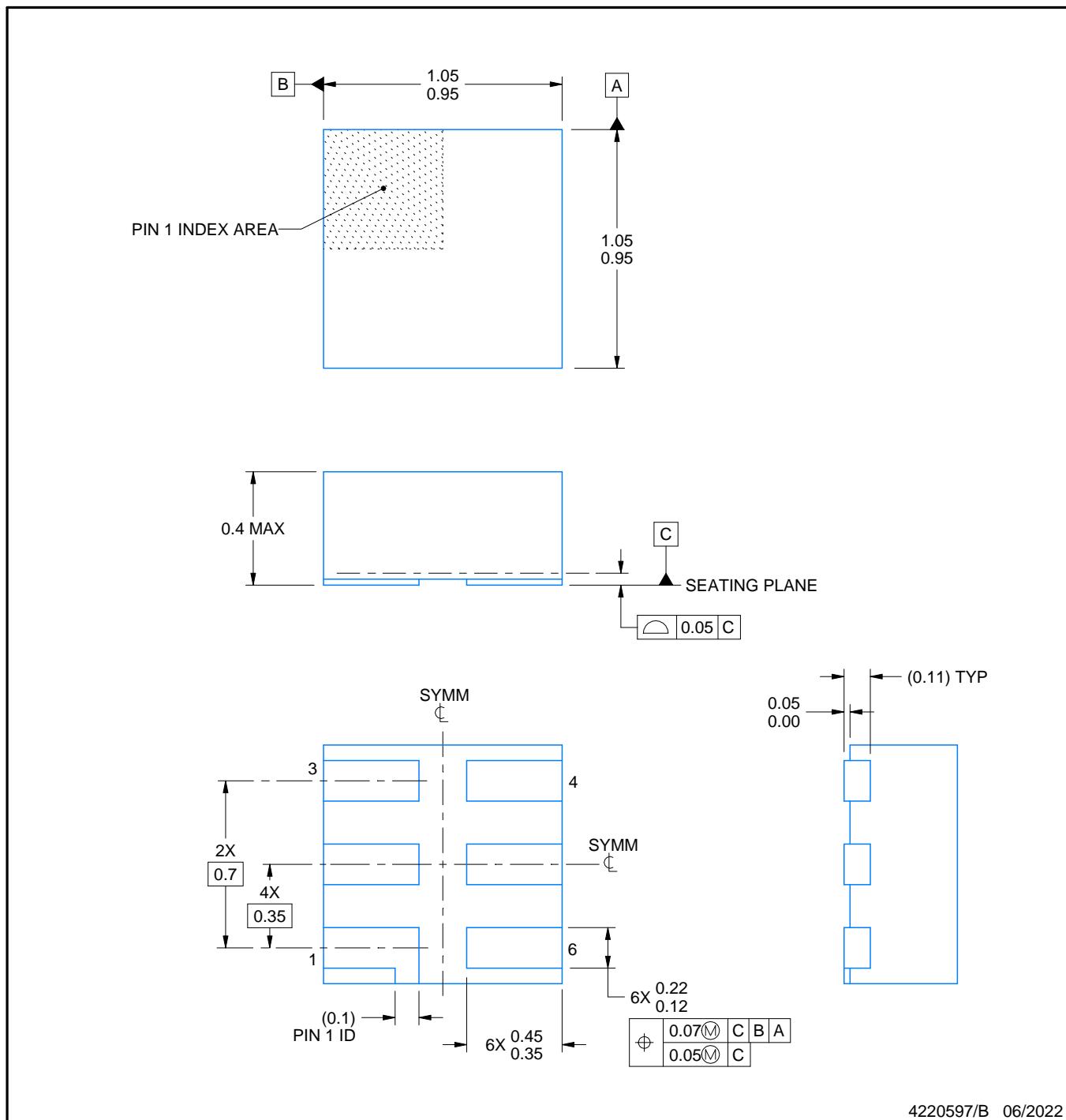


## PACKAGE OUTLINE

**DSF0006A**

## **X2SON - 0.4 mm max height**

## PLASTIC SMALL OUTLINE - NO LEAD



4220597/B 06/2022

## NOTES:

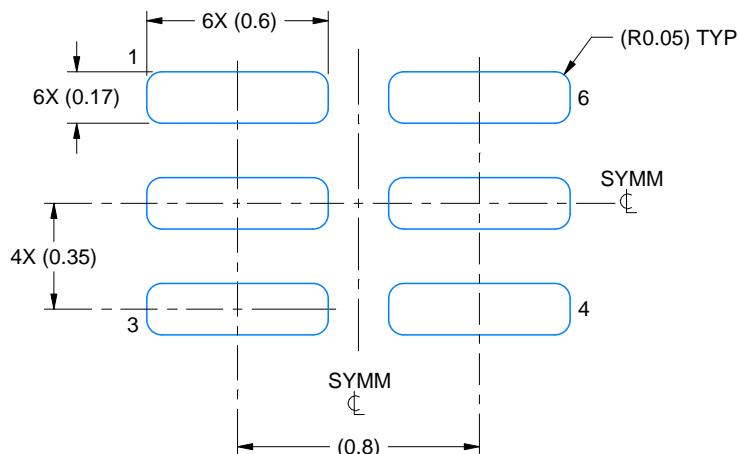
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC registration MO-287, variation X2AAF.

# EXAMPLE BOARD LAYOUT

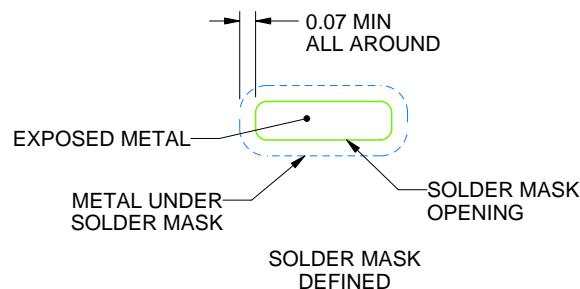
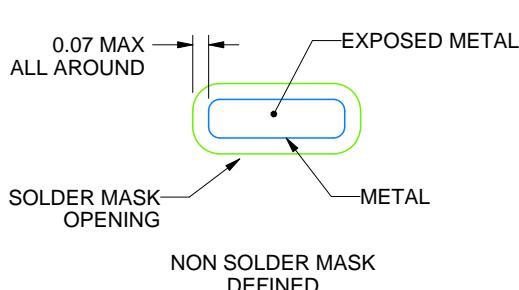
DSF0006A

X2SON - 0.4 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE:40X



SOLDER MASK DETAILS

4220597/B 06/2022

NOTES: (continued)

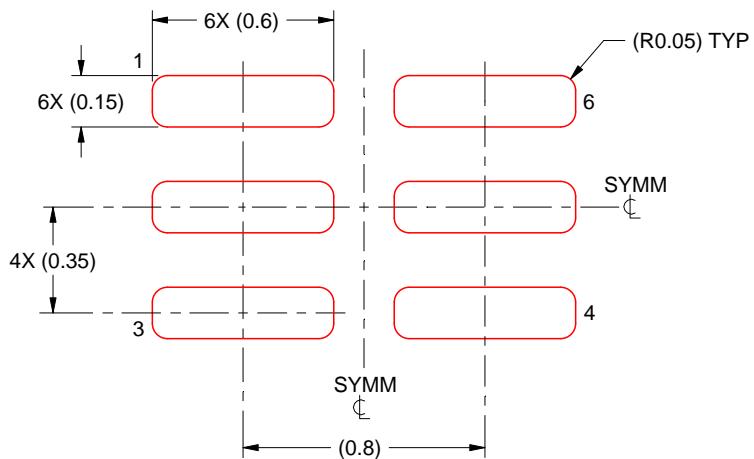
4. For more information, see Texas Instruments literature number SLUA271 ([www.ti.com/lit/slua271](http://www.ti.com/lit/slua271)).

# EXAMPLE STENCIL DESIGN

DSF0006A

X2SON - 0.4 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



SOLDER PASTE EXAMPLE  
BASED ON 0.09 mm THICK STENCIL

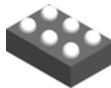
PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE  
SCALE:40X

4220597/B 06/2022

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

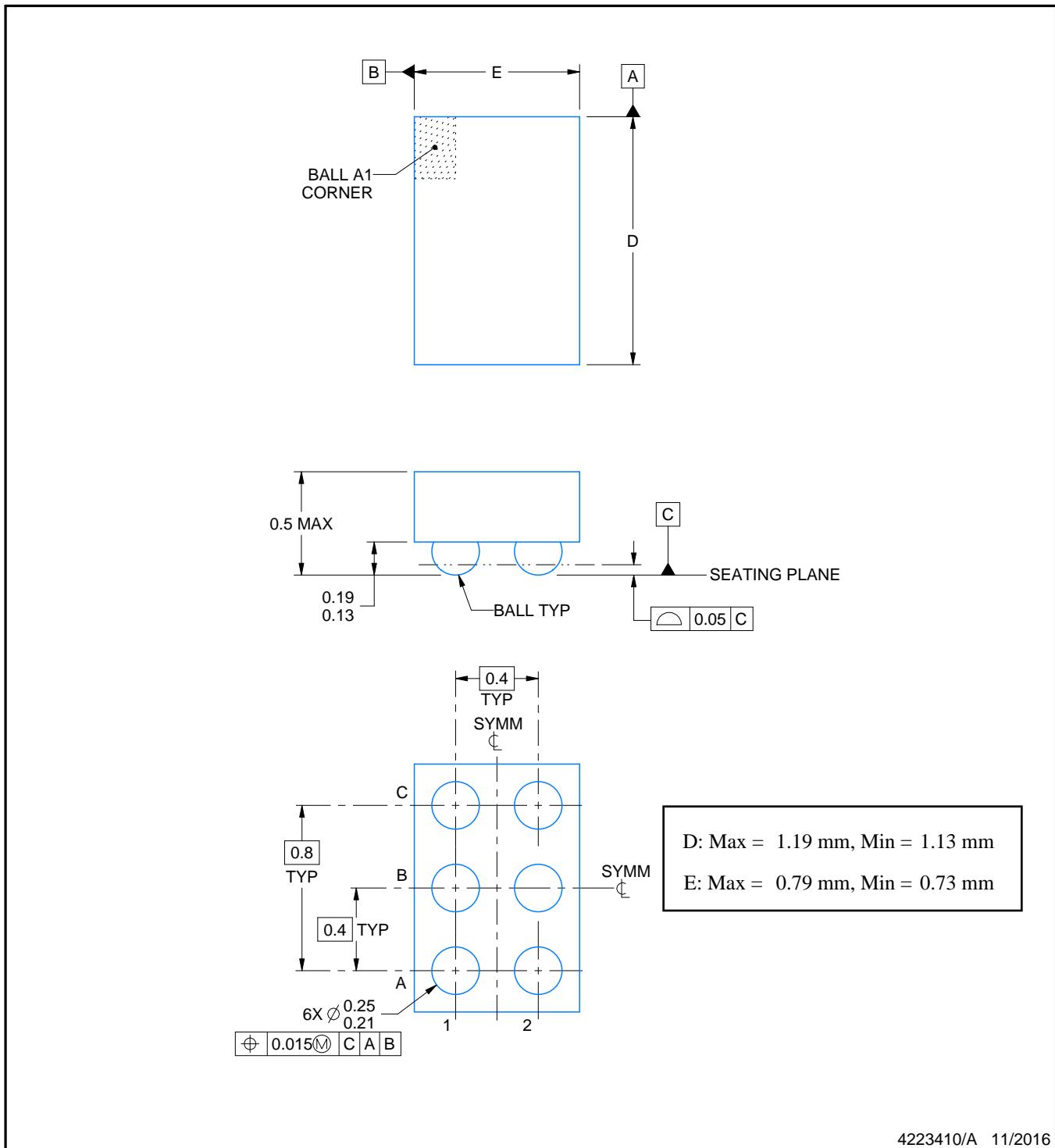
# PACKAGE OUTLINE

**YFP0006**



**DSBGA - 0.5 mm max height**

DIE SIZE BALL GRID ARRAY



4223410/A 11/2016

**NOTES:**

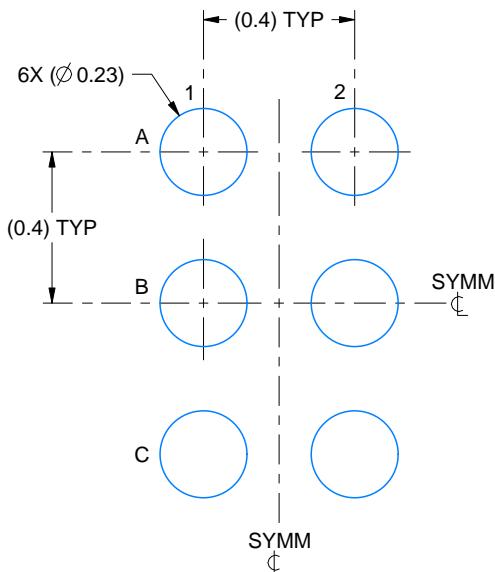
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

## EXAMPLE BOARD LAYOUT

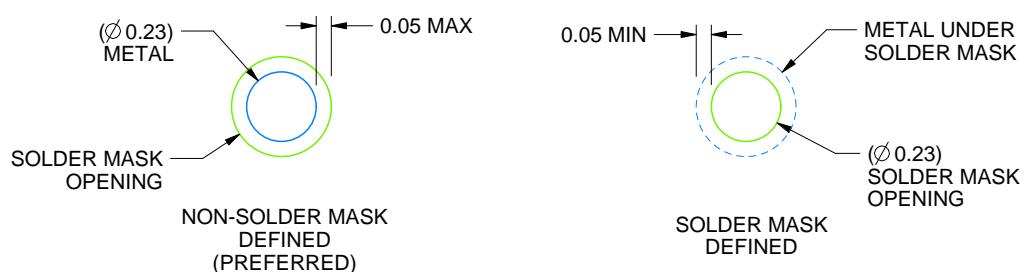
**YFP0006**

## DSBGA - 0.5 mm max height

## DIE SIZE BALL GRID ARRAY



## LAND PATTERN EXAMPLE



## SOLDER MASK DETAILS NOT TO SCALE

4223410/A 11/2016

#### NOTES: (continued)

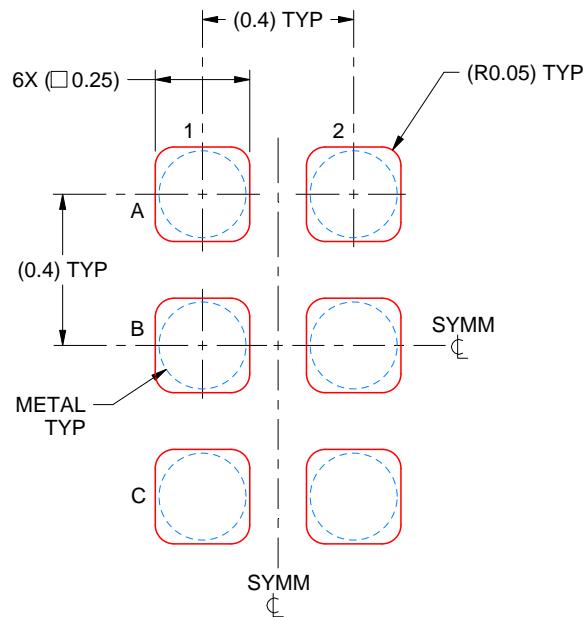
3. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. For more information, see Texas Instruments literature number SNVA009 ([www.ti.com/lit/snva009](http://www.ti.com/lit/snva009)).

# EXAMPLE STENCIL DESIGN

YFP0006

DSBGA - 0.5 mm max height

DIE SIZE BALL GRID ARRAY



SOLDER PASTE EXAMPLE  
BASED ON 0.1 mm THICK STENCIL  
SCALE:50X

4223410/A 11/2016

NOTES: (continued)

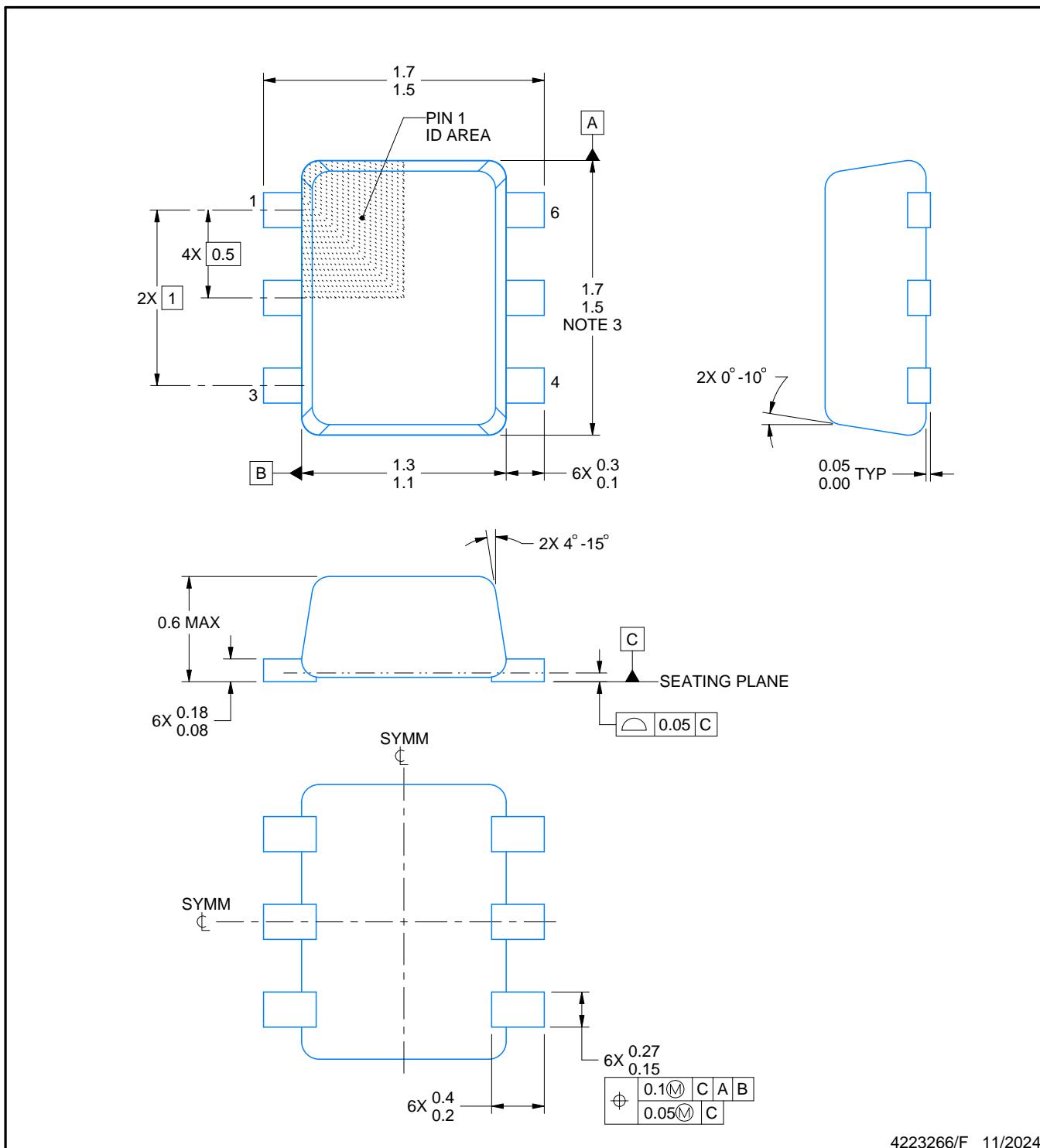
4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

# PACKAGE OUTLINE

## SOT - 0.6 mm max height

PLASTIC SMALL OUTLINE

DRL0006A



4223266/F 11/2024

### NOTES:

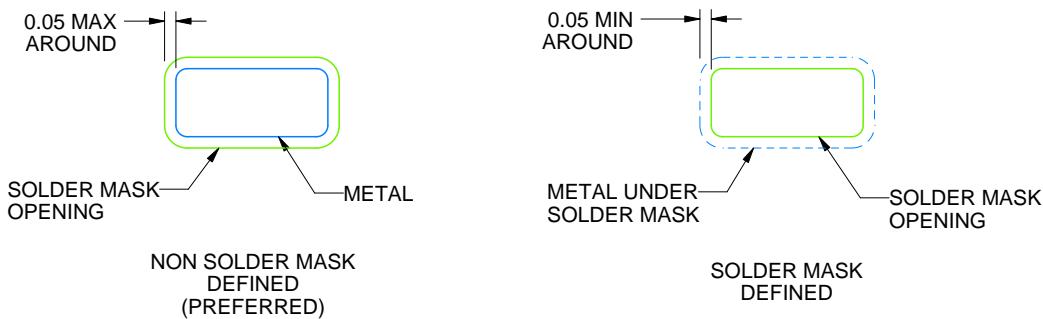
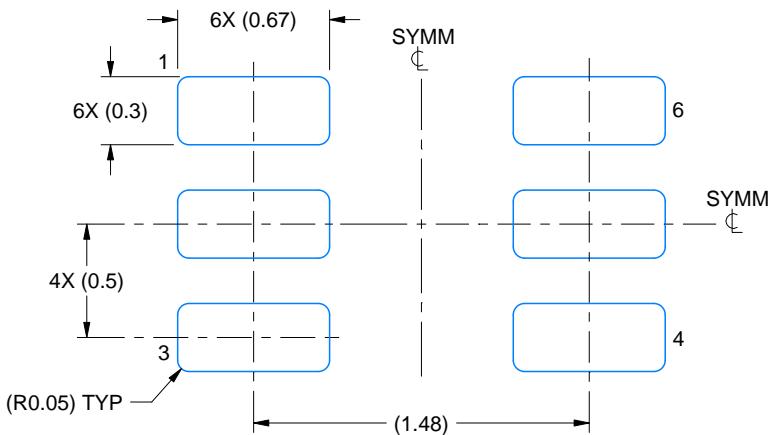
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-293 Variation UAAD

# EXAMPLE BOARD LAYOUT

DRL0006A

SOT - 0.6 mm max height

PLASTIC SMALL OUTLINE



4223266/F 11/2024

NOTES: (continued)

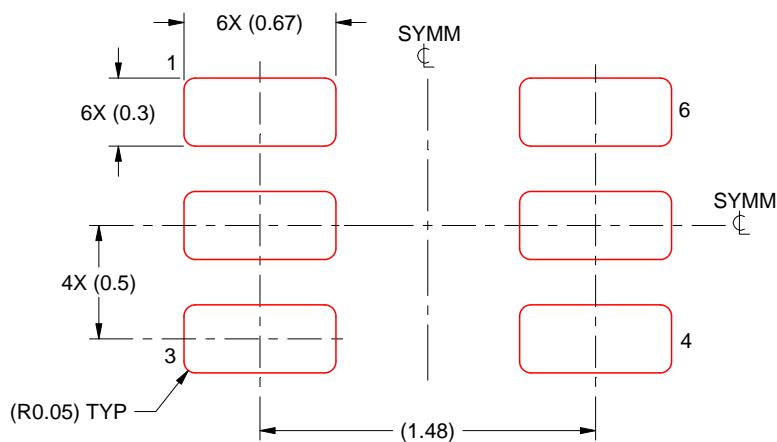
5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
7. Land pattern design aligns to IPC-610, Bottom Termination Component (BTC) solder joint inspection criteria.

# EXAMPLE STENCIL DESIGN

DRL0006A

SOT - 0.6 mm max height

PLASTIC SMALL OUTLINE



SOLDER PASTE EXAMPLE  
BASED ON 0.1 mm THICK STENCIL  
SCALE:30X

4223266/F 11/2024

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

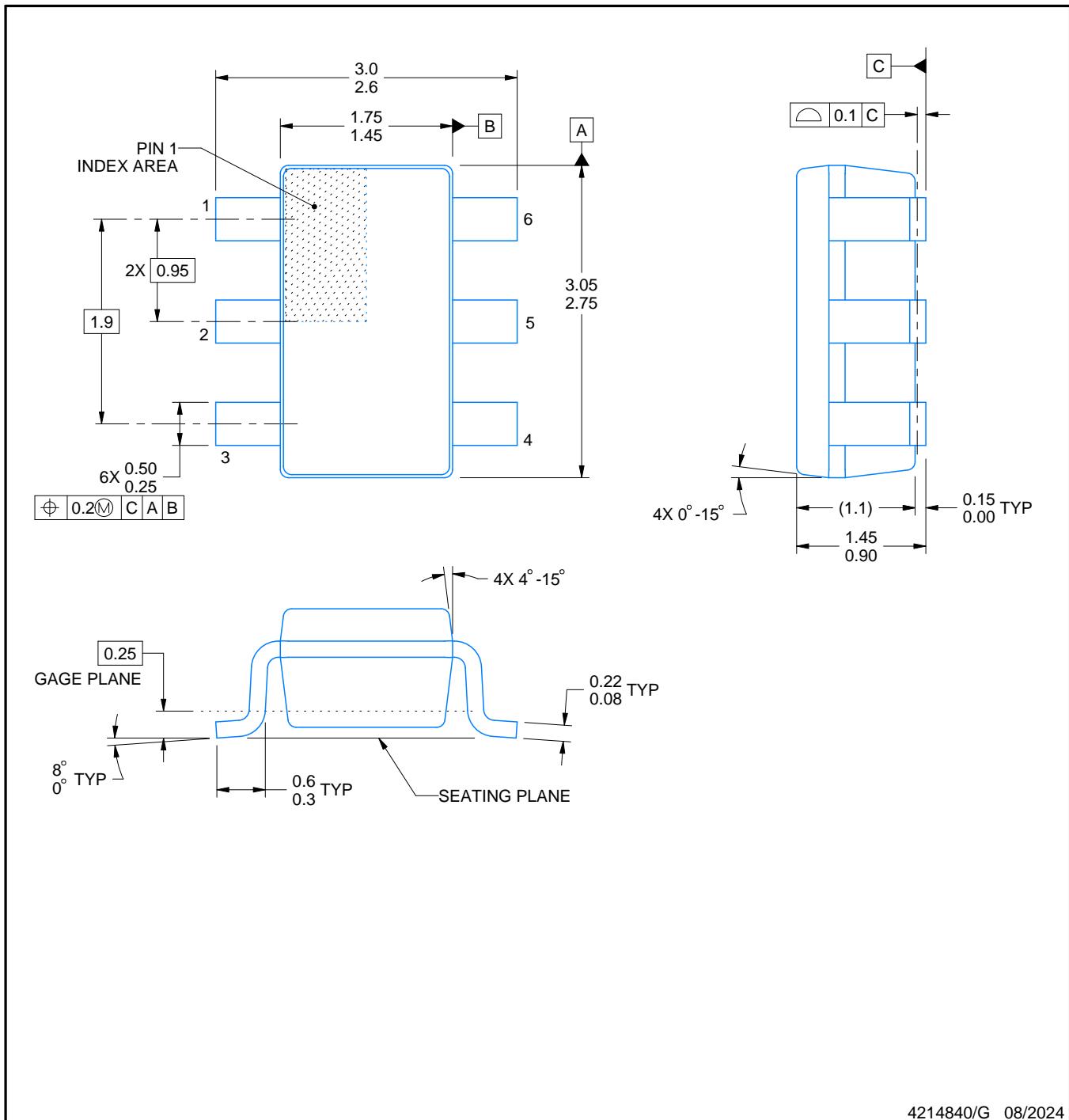
## PACKAGE OUTLINE

**DBV0006A**



## **SOT-23 - 1.45 mm max height**

## SMALL OUTLINE TRANSISTOR



4214840/G 08/2024

## NOTES:

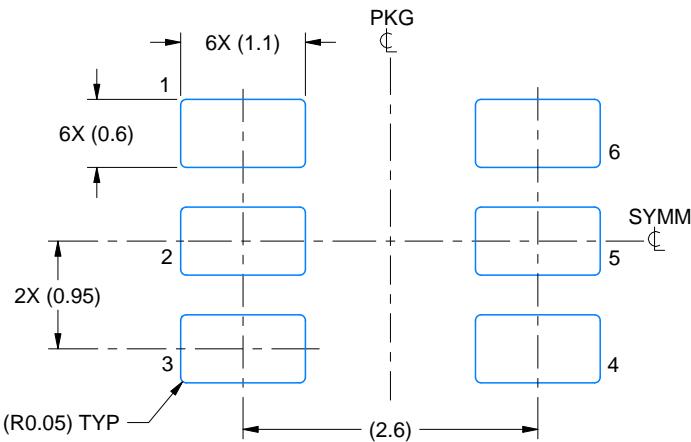
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.25 per side.
4. Leads 1,2,3 may be wider than leads 4,5,6 for package orientation.
5. Reference JEDEC MO-178.

# EXAMPLE BOARD LAYOUT

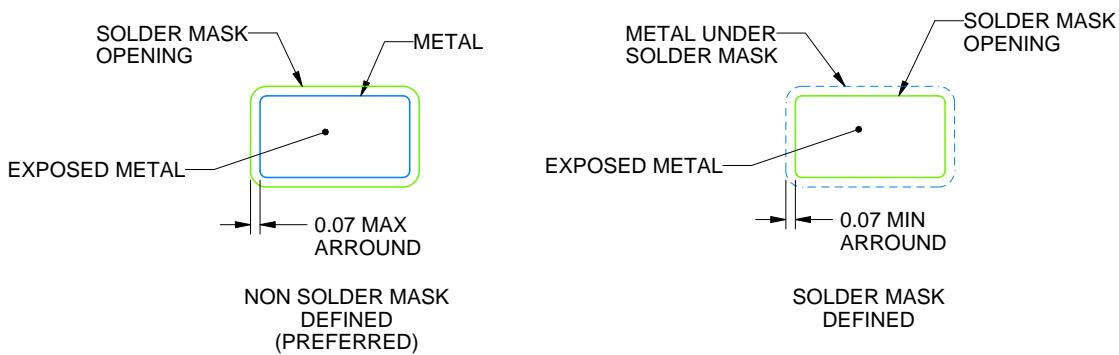
DBV0006A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE:15X



SOLDER MASK DETAILS

4214840/G 08/2024

NOTES: (continued)

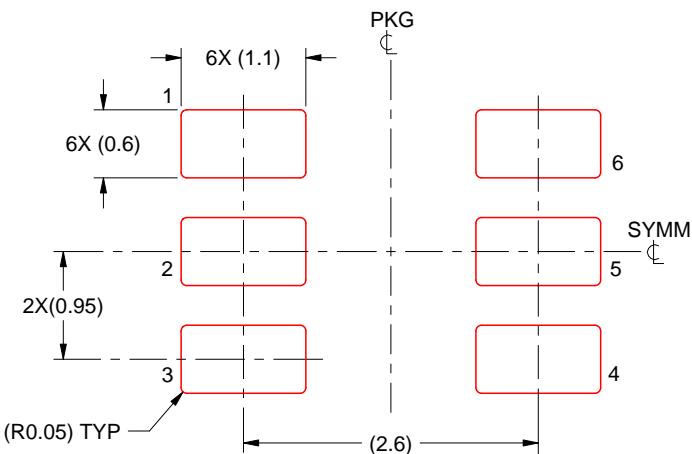
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

DBV0006A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR

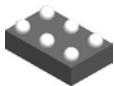


SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:15X

4214840/G 08/2024

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

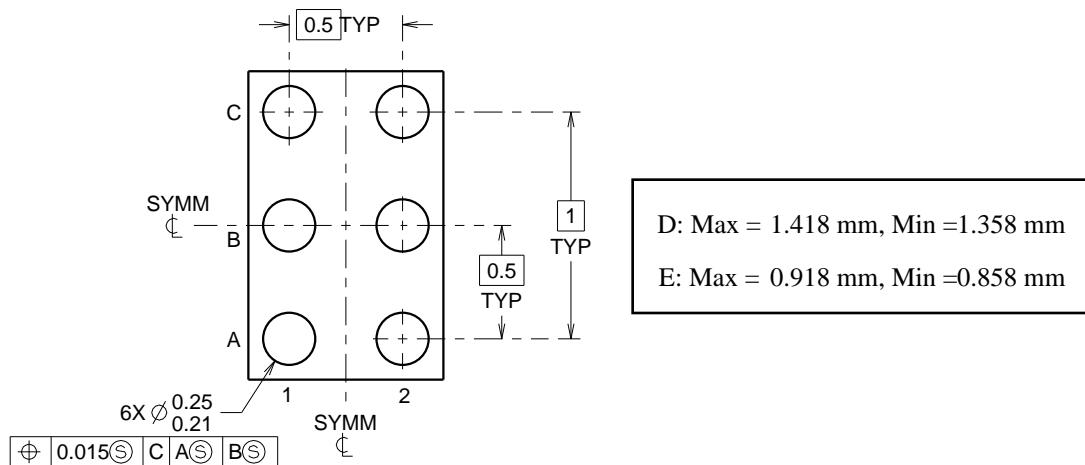
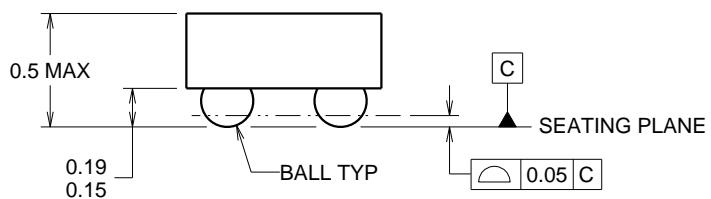
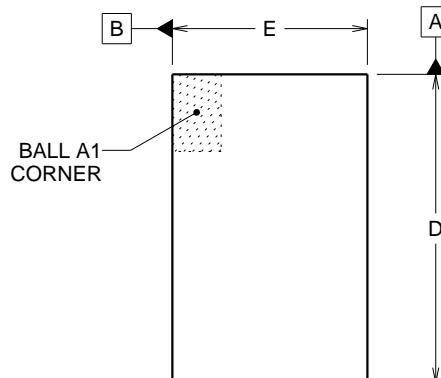


# PACKAGE OUTLINE

YZP0006

DSBGA - 0.5 mm max height

DIE SIZE BALL GRID ARRAY



4219524/A 06/2014

NOTES:

NanoFree is a trademark of Texas Instruments.

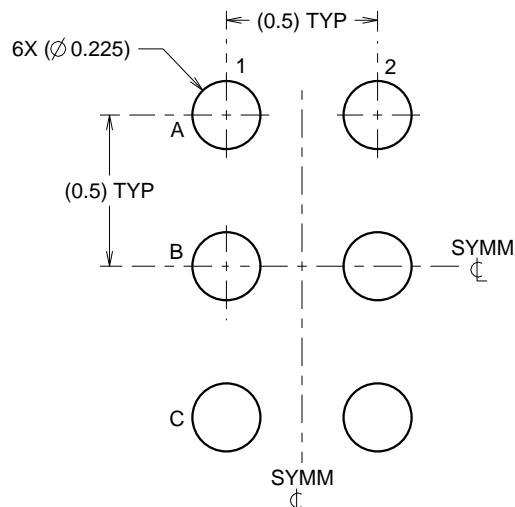
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. NanoFree™ package configuration.

# EXAMPLE BOARD LAYOUT

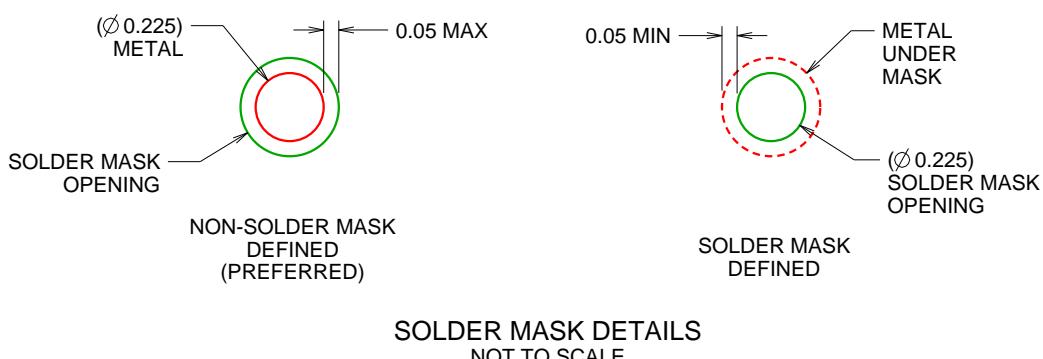
YZP0006

DSBGA - 0.5 mm max height

DIE SIZE BALL GRID ARRAY



LAND PATTERN EXAMPLE  
SCALE:40X



SOLDER MASK DETAILS  
NOT TO SCALE

4219524/A 06/2014

NOTES: (continued)

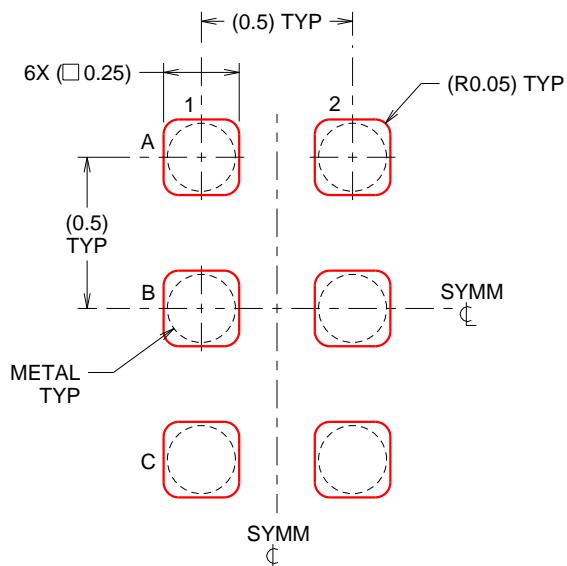
4. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. For more information, see Texas Instruments literature number SBVA017 ([www.ti.com/lit/sbva017](http://www.ti.com/lit/sbva017)).

# EXAMPLE STENCIL DESIGN

YZP0006

DSBGA - 0.5 mm max height

DIE SIZE BALL GRID ARRAY



SOLDER PASTE EXAMPLE  
BASED ON 0.1 mm THICK STENCIL  
SCALE:40X

4219524/A 06/2014

NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

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