SN74AVC4T245-Q1 具有可配置电压转换和三态输出的汽车级 4 位双电源总线收发器

1 特性

- 符合汽车应用要求
- 具有符合 AEC-Q100 标准的下列特性：
  - 器件温度等级 1：–40°C 至 125°C 环境工作温度范围
  - 器件 HBM ESD 分类等级 H3B (JESD 22 A114-A)
  - 器件 CDM ESD 分类等级 C5 (JESD 22 C101)
- 功能安全型
- 控制输入 V_{IH} 和 V_{IL} 电平以 V_{CCA} 电压为基准
- 完全可配置的双轨设计，支持各个端口在 1.2V 至 3.6V 的整个电源电压范围内运行
- I/O 可承受 4.6V 的电压
- I_{off} 支持局部断电模式运行
- 最大数据速率：
  - 380Mbps（1.8V 至 3.3V 转换）
  - 200Mbps（<1.8V 至 3.3V 转换）
  - 200Mbps（转换至 2.5V 或 1.8V）
  - 150Mbps（转换至 1.5V）
  - 100Mbps（转换至 1.2V）
- 闩锁性能超过 100mA，符合 JESD 78 II 类规范的要求

2 应用

- 远程信息处理
- 仪表组
- 音响主机
- 导航系统

3 说明

这款 4 位同相总线收发器使用两个独立的可配置电源轨。A 端口旨在跟踪 V_{CCA}。V_{CCA} 可接受 1.2V 至 3.6V 的任何电源电压。B 端口旨在用于跟踪 V_{CCB}。V_{CCB} 可接受 1.2V 至 3.6V 的
任何电源电压。SN74AVC4T245-Q1 经过优化，可在 V_{CCA}/V_{CCB} 设置为 1.4V 至 3.6V 的范围内正常运行。该器件可在 V_{CCA}/V_{CCB} 低至 1.2V 的情况下正常运行，因此可在 1.2V、1.5V、1.8V、2.5V 和 3.3V 电压节点之间进行通用的低电压双向转换。

SN74AVC4T245-Q1 旨在实现两条数据总线间的异步通信。方向控制 (DIR) 输入和输出使能 ($\overline{OE}$) 输入的逻辑电平激活 B 端口输出或者 A 端口输出，或者将两个输出端口都置于高阻抗模式。当 B 端口输出被激活时，此器件将数据从 A 总线发送到 B 总线，而当 A 端口输出被激活时，此器件将数据从 B 总线发送到 A 总线。A 端口和 B 端口上的输入电路一直处于激活状态并且必须施加一个逻辑高或低电平，从而防止过大的 I_{CC} 和 I_{CCZ}。

SN74AVC4T245-Q1 的设计方式决定了控制引脚（1DIR、2DIR、1 $\overline{OE}$ 和 2 $\overline{OE}$）由 V_{CCA} 供电。

该器件专用于使用 I_{off} 的局部断电应用。I_{off} 电路可禁用输出，以防在器件断电时电流回流对器件造成损坏。

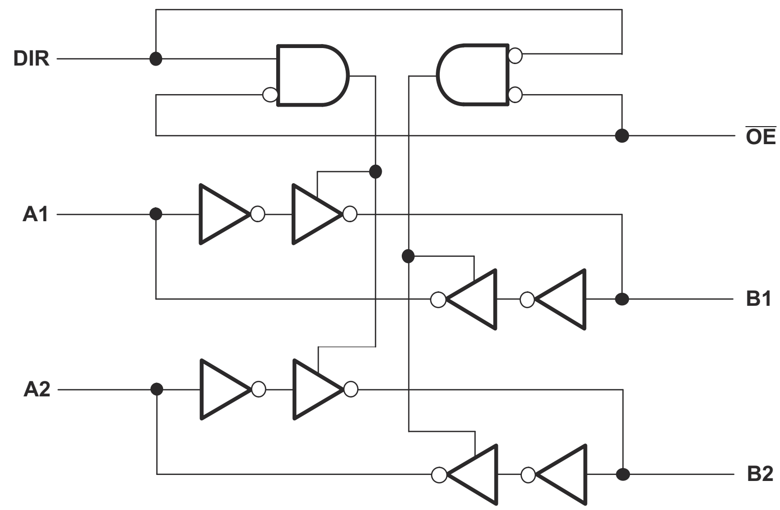
V_{CC} 隔离特性可在任何一个 V_{CC} 输入接地的情况下，将两个端口均置于高阻抗状态。

要在上电或断电期间将器件置于高阻抗状态，应通过一个上拉电阻器将 $\overline{OE}$ 连接至 V_{CC}；该电阻器的最小值由驱动器的电流灌入能力决定。

封装信息

器件型号	封装[(1)]	封装尺寸[(2)]
SN74AVC4T245-Q1	RGY（VQFN，16）	4mm x 3.5mm
	PW（TSSOP，16）	5mm x 6.4mm
	BQB（WQFN，16）	3.5mm x 2.5mm
	DYY（SOT，16）	4.2mm x 2mm

(1) 有关更多信息，请参阅节 11
(2) 封装尺寸（长 × 宽）为标称值，并包括引脚（如适用）。



SN74AVC4T245-Q1 半侧逻辑图（正逻辑）：

Table of Contents

4 Pin Configuration and Functions

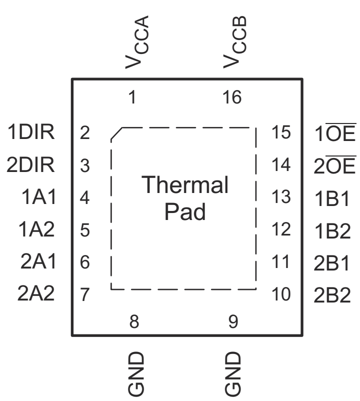


图 4-1. RGY Package 16-Pin VQFN With Exposed Thermal Pad (Top View)

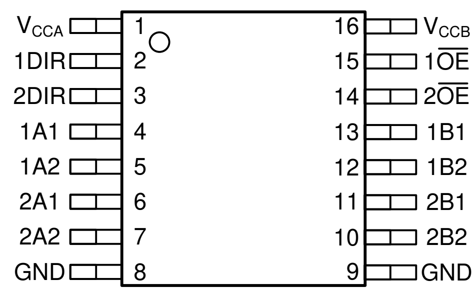


图 4-2. PW Package, 16-Pin TSSOP (Top View)

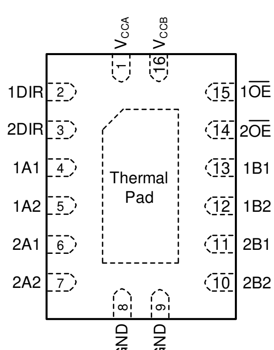


图 4-3. BQB/WBQB Package, 16-Pin WQFN (Transparent Top View)

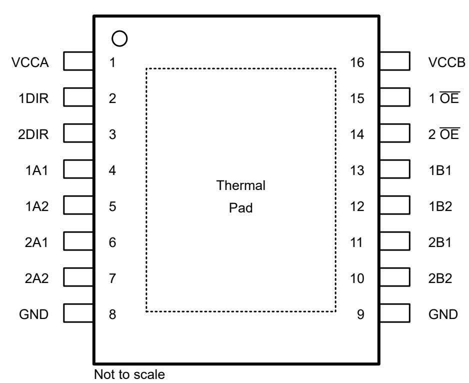


图 4-4. DYY Package, 16-Pin SOT (Top View)

表 4-1. Pin Functions

PIN		TYPE(1)	DESCRIPTION
NAME	NO.		
1A1	4	I/O	Input/output 1A1. Referenced to V_{CCA}.
1A2	5	I/O	Input/output 1A2. Referenced to V_{CCA}.
1B1	13	I/O	Input/output 1B1. Referenced to V_{CCB}.
1B2	12	I/O	Input/output 1B2. Referenced to V_{CCB}.
1DIR	2	I	Direction-control input for 1 ports
1 $\overline{OE}$	15	I	3-state output-mode enable. Pull $\overline{OE}$ high to place ‘1’ outputs in 3-state mode. Referenced to V_{CCA}.
2A1	6	I/O	Input/output 2A1. Referenced to V_{CCA}.
2A2	7	I/O	Input/output 2A2. Referenced to V_{CCA}.
2B1	11	I/O	Input/output 2B1. Referenced to V_{CCB}.
2B2	10	I/O	Input/output 2B2. Referenced to V_{CCB}.
2DIR	3	I	Direction-control input for 2 ports
2 $\overline{OE}$	14	I	3-state output-mode enable. Pull $\overline{OE}$ high to place ‘2’ outputs in 3-state mode. Referenced to V_{CCA}.
GND	8, 9	—	Ground
V_{CCA}	1	I	A-port power supply voltage. $1.2V \leqslant V_{CCA} \leqslant 3.6V$
V_{CCB}	16	I	B-port power supply voltage. $1.2V \leqslant V_{CCB} \leqslant 3.6V$
Thermal pad		—	The exposed thermal pad must be connected as a secondary GND or be left electrically open.

(1) I = input, O = output

5 Specifications

5.1 Absolute Maximum Ratings

over operating ambient temperature range (unless otherwise noted) [(1)]

			MIN	MAX	UNIT
V_{CCA} V_{CCB}	Supply voltage		–0.5	4.6	V
V_I	Input voltage[(2)]	I/O ports (A port)	–0.5	4.6	V
		I/O ports (B port)	–0.5	4.6	
		Control inputs	–0.5	4.6	
V_O	Voltage applied to any output in the high-impedance or power-off state[(2)]	A port	–0.5	4.6	V
		B port	–0.5	4.6	
V_O	Voltage applied to any output in the high or low state[(2) (3)]	A port	–0.5	V_{CCA} + 0.5	V
		B port	–0.5	V_{CCB} + 0.5	
I_{IK}	Input clamp current	V_I < 0		–50	mA
I_{OK}	Output clamp current	V_O < 0		–50	mA
I_O	Continuous output current			±50	mA
	Continuous current through V_{CCA}, V_{CCB}, or GND			±100	mA
T_{stg}	Storage temperature		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The input voltage and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.
(3) The output positive-voltage rating may be exceeded up to 4.6V maximum if the output current rating is observed.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins[(1)]	±8000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins[(2)]	±1000	
		Machine model (C101)	±150	

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

			V_{CCI}	V_{CCO}	MIN	MAX	UNIT
V_{CCA}	Supply voltage				1.2	3.6	V
V_{CCB}	Supply voltage				1.2	3.6	V
V_{IH}	High-level input voltage	Data inputs[(1)]	1.2V to 1.95V		V_{CCI} × 0.65		V
			1.95V to 2.7V		1.6		
			2.7V to 3.6V		2		
V_{IL}	Low-level input voltage	Data inputs[(1)]	1.2V to 1.95V			V_{CCI} × 0.35	V
			1.95V to 2.7V			0.7	
			2.7V to 3.6V			0.8	
V_{IH}	High-level input voltage	DIR (referenced to V_{CCA})[(2)]	1.2V to 1.95V		V_{CCA} × 0.65		V
			1.95V to 2.7V		1.6		
			2.7V to 3.6V		2		

5.3 Recommended Operating Conditions（续）

			V_{CCI}	V_{CCO}	MIN	MAX	UNIT
V_{IL}	Low-level input voltage	DIR (referenced to V_{CCA})[2]	1.2V to 1.95V			V_{CCA} × 0.35	V
			1.95V to 2.7V			0.7	
			2.7V to 3.6V			0.8	
V_I	Input voltage				0	3.6	V
V_O	Output voltage	Active state			0	V_{CCO}	V
		3-state			0	3.6	
I_{OH}	High-level output current			1.2V		–3	mA
				1.4V to 1.6V		–6	
				1.65V to 1.95V		–8	
				2.3V to 2.7V		–9	
				3V to 3.6V		–12	
I_{OL}	Low-level output current			1.1V to 1.2V		3	mA
				1.4V to 1.6V		6	
				1.65V to 1.95V		8	
				2.3V to 2.7V		9	
				3V to 3.6V		12	
$\Delta t/\Delta v$	Input transition rise or fall rate					5	ns/V
T_A	Operating ambient temperature				–40	125	°C

(1) For V_{CCI} values not specified in the data sheet, V_{IH} min = V_{CCI} × 0.7V, V_{IL} max = V_{CCI} × 0.3V
(2) For V_{CCI} values not specified in the data sheet, V_{IH} min = V_{CCA} × 0.7V, V_{IL} max = V_{CCA} × 0.3V

5.4 Thermal Information

THERMAL METRIC[1]		SN74AVC4T245-Q1				UNIT
		RGY (VQFN)	PW (TSSOP)	BQB (WQFN)	DYY (SOT)	
		16 PINS	16 PINS	16 PINS	16 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	37.5	101.8	80.8	163.4	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	54.5	37.2	77.9	90.0	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	15.6	60.6	50.7	93.1	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.5	1.6	7.4	10.9	°C/W
ψ_{JB}	Junction-to-board characterization parameter	15.8	60.0	50.6	92.1	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	3.5	N/A	28.4	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report (SPRA953).

5.5 Electrical Characteristics

over recommended operating ambient temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		V_{CCA}	V_{CCB}	T_A	MIN	TYP	MAX	UNIT
V_{OH}		I_{OH} = –100 μA	$V_I = V_{IH}$	1.2V to 3.6V	1.2V to 3.6V	T_A = –40°C to 125°C	V_{CCO} – 0.2			V
		I_{OH} = –3mA		1.2V	1.2V	T_A = 25°C		0.95		
		I_{OH} = –6mA		1.4V	1.4V	T_A = –40°C to 125°C	1.05			
		I_{OH} = –8mA		1.65V	1.65V	T_A = –40°C to 125°C	1.2			
		I_{OH} = –9mA		2.3V	2.3V	T_A = –40°C to 125°C	1.75			
		I_{OH} = –12mA		3V	3V	T_A = –40°C to 125°C	2.3			
V_{OL}		I_{OL} = 100 μA	$V_I = V_{IL}$	1.2V to 3.6V	1.2V to 3.6V	T_A = –40°C to 125°C			0.2	V
		I_{OL} = 3mA		1.2V	1.2V	T_A = 25°C		0.25		
		I_{OL} = 6mA		1.4V	1.4V	T_A = –40°C to 125°C			0.35	
		I_{OL} = 8mA		1.65V	1.65V	T_A = –40°C to 125°C			0.45	
		I_{OL} = 9mA		2.3V	2.3V	T_A = –40°C to 125°C			0.55	
		I_{OL} = 12mA		3V	3V	T_A = –40°C to 125°C			0.7	
I_I (1)	Control inputs	$V_I = V_{CCA}$ or GND		1.2V to 3.6V	1.2V to 3.6V	T_A = 25°C		±0.025	±0.25	μA
						T_A = –40°C to 125°C			±1.5	
I_{off}	A or B port	V_I or V_O = 0 to 3.6V		0V	0V to 3.6V	T_A = 25°C		±0.1	±1	μA
						T_A = –40°C to 125°C			±5	
				0V to 3.6V	0V	T_A = 25°C		±0.1	±1	
						T_A = –40°C to 125°C			±5	
I_{OZ}	A or B port	$V_O = V_{CCO}$ or GND, $V_I = V_{CCI}$ or GND, $\overline{OE} = V_{IH}$		3.6V	3.6V	T_A = 25°C		±0.5	±2.5	μA
						T_A = –40°C to 125°C			±5	
I_{CCA} (1)		$V_I = V_{CCI}$ or GND, I_O = 0		1.2V to 3.6V	1.2V to 3.6V	T_A = –40°C to 125°C			8	μA
				0V	0V to 3.6V	T_A = 25°C			–2	
						T_A = –40°C to 125°C			–11	
				0V to 3.6V	0V	T_A = –40°C to 125°C			8	
I_{CCB} (1)		$V_I = V_{CCI}$ or GND, I_O = 0		1.2V to 3.6V	1.2V to 3.6V	T_A = –40°C to 125°C			8	μA
				0V	0V to 3.6V	T_A = –40°C to 125°C			8	
				0V to 3.6V	0V	T_A = 25°C			–2	
						T_A = –40°C to 125°C			–11	

5.5 Electrical Characteristics （续）

over recommended operating ambient temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CCA}	V_{CCB}	T_A	MIN	TYP	MAX	UNIT
$I_{CCA} + I_{CCB}$		$V_I = V_{CCI}$ or GND, $I_O = 0$	1.2V to 3.6V	1.2V to 3.6V	T_A = –40°C to 125°C			16	µA
C_i	Control inputs	V_I = 3.3V or GND	3.3V	3.3V	T_A = 25°C		3.5	4.5	pF
					T_A = –40°C to 125°C			7	
C_{io}	A or B port	V_O = 3.3V or GND	3.3V	3.3V	T_A = 25°C		6		pF
					T_A = –40°C to 125°C				

(1) All unused data inputs of the device must be held at V_{CCI} or GND for proper device operation. See the TI application report, *Implications of Slow or Floating CMOS Inputs*, SCBA004.

5.6 Switching Characteristics: V_{CCA} = 1.2V

over recommended operating ambient temperature range, V_{CCA} = 1.2V (unless otherwise noted) (see 图 6-1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CCB}	TYP	UNIT
t_{PHL}, t_{PLH}	A	B	V_{CCB} = 1.2V	3.4	ns
			V_{CCB} = 1.5V ± 0.1V	2.9	
			V_{CCB} = 1.8V ± 0.15V	2.7	
			V_{CCB} = 2.5V ± 0.2V	2.6	
			V_{CCB} = 3.3V ± 0.3V	2.8	
t_{PHL}, t_{PLH}	B	A	V_{CCB} = 1.2V	3.6	ns
			V_{CCB} = 1.5V ± 0.1V	3.1	
			V_{CCB} = 1.8V ± 0.15V	2.8	
			V_{CCB} = 2.5V ± 0.2V	2.6	
			V_{CCB} = 3.3V ± 0.3V	2.6	
t_{PHZ}, t_{PLZ}	$\overline{OE}$	A	V_{CCB} = 1.2V	5.6	ns
			V_{CCB} = 1.5V ± 0.1V	4.7	
			V_{CCB} = 1.8V ± 0.15V	4.3	
			V_{CCB} = 2.5V ± 0.2V	3.9	
			V_{CCB} = 3.3V ± 0.3V	3.7	
t_{PZH}	$\overline{OE}$	B	V_{CCB} = 1.2V	5	ns
			V_{CCB} = 1.5V ± 0.1V	4.3	
			V_{CCB} = 1.8V ± 0.15V	3.9	
			V_{CCB} = 2.5V ± 0.2V	3.6	
			V_{CCB} = 3.3V ± 0.3V	36.6	
t_{PZL}	$\overline{OE}$	B	V_{CCB} = 1.2V	5	
			V_{CCB} = 1.5V ± 0.1V	4.3	
			V_{CCB} = 1.8V ± 0.15V	3.9	
			V_{CCB} = 2.5V ± 0.2V	3.6	
			V_{CCB} = 3.3V ± 0.3V	3.6	
t_{PHZ}, t_{PLZ}	$\overline{OE}$	A	V_{CCB} = 1.2V	6.2	ns
			V_{CCB} = 1.5V ± 0.1V	5.2	
			V_{CCB} = 1.8V ± 0.15V	5.2	
			V_{CCB} = 2.5V ± 0.2V	4.3	
			V_{CCB} = 3.3V ± 0.3V	4.8	

5.6 Switching Characteristics: V_{CCA} = 1.2V （续）

over recommended operating ambient temperature range, V_{CCA} = 1.2V (unless otherwise noted) (see 图 6-1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CCB}	TYP	UNIT
t_{PHZ}, t_{PLZ}	$\overline{OE}$	B	V_{CCB} = 1.2V	5.9	ns
			V_{CCB} = 1.5V ± 0.1V	5.1	
			V_{CCB} = 1.8V ± 0.15V	5	
			V_{CCB} = 2.5V ± 0.2V	4.7	
			V_{CCB} = 3.3V ± 0.3V	5.5	

5.7 Switching Characteristics, V_{CCA} = 1.5V ± 0.1V

over recommended operating ambient temperature range, V_{CCA} = 1.5V ± 0.1V (see 图 6-1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CCB}	MIN	TYP	MAX	UNIT
t_{PLH}, t_{PHL}	A	B	V_{CCB} = 1.2V		3.2		ns
			V_{CCB} = 1.5V ± 0.1V			11.3	
			V_{CCB} = 1.8V ± 0.15V			10.2	
			V_{CCB} = 2.5V ± 0.2V			9.2	
			V_{CCB} = 3.3V ± 0.3V			9.2	
t_{PLH}, t_{PHL}	B	A	V_{CCB} = 1.2V		3.3		ns
			V_{CCB} = 1.5V ± 0.1V			11.3	
			V_{CCB} = 1.8V ± 0.15V			11	
			V_{CCB} = 2.5V ± 0.2V			10.7	
			V_{CCB} = 3.3V ± 0.3V			10.6	
t_{PZH}, t_{PZL}	$\overline{OE}$	A	V_{CCB} = 1.2V		4.9		ns
			V_{CCB} = 1.5V ± 0.1V			14.6	
			V_{CCB} = 1.8V ± 0.15V			14.5	
			V_{CCB} = 2.5V ± 0.2V			14.4	
			V_{CCB} = 3.3V ± 0.3V			14.4	
t_{PZH}, t_{PZL}	$\overline{OE}$	B	V_{CCB} = 1.2V		4.5		ns
			V_{CCB} = 1.5V ± 0.1V			14.6	
			V_{CCB} = 1.8V ± 0.15V			12.7	
			V_{CCB} = 2.5V ± 0.2V			10.8	
			V_{CCB} = 3.3V ± 0.3V			10.6	
t_{PZH}, t_{PZL}	$\overline{OE}$	A	V_{CCB} = 1.2V		5.6		ns
			V_{CCB} = 1.5V ± 0.1V			15.2	
			V_{CCB} = 1.8V ± 0.15V			15.2	
			V_{CCB} = 2.5V ± 0.2V			15.2	
			V_{CCB} = 3.3V ± 0.3V			15.2	
t_{PZH}, t_{PZL}	$\overline{OE}$	B	V_{CCB} = 1.2V		5.2		ns
			V_{CCB} = 1.5V ± 0.1V			15.3	
			V_{CCB} = 1.8V ± 0.15V			14.1	
			V_{CCB} = 2.5V ± 0.2V			12.4	
			V_{CCB} = 3.3V ± 0.3V			12.6	

5.8 Switching Characteristics: V_{CCA} = 1.8V ± 0.15V

over recommended operating ambient temperature range, V_{CCA} = 1.8V ± 0.15V (see 图 6-1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CCB}	MIN	TYP	MAX	UNIT
t_{PLH}, t_{PHL}	A	B	V_{CCB} = 1.2V		2.9		ns
			V_{CCB} = 1.5V ± 0.1V			11	
			V_{CCB} = 1.8V ± 0.15V			9.9	
			V_{CCB} = 2.5V ± 0.2V			8.9	
			V_{CCB} = 3.3V ± 0.3V			8.9	
t_{PLH}, t_{PHL}	B	A	V_{CCB} = 1.2V		3		ns
			V_{CCB} = 1.5V ± 0.1V			10.3	
			V_{CCB} = 1.8V ± 0.15V			9.9	
			V_{CCB} = 2.5V ± 0.2V			9.6	
			V_{CCB} = 3.3V ± 0.3V			9.5	
t_{PZH}, t_{PZL}	$\overline{OE}$	A	V_{CCB} = 1.2V		4.4		ns
			V_{CCB} = 1.5V ± 0.1V			12.4	
			V_{CCB} = 1.8V ± 0.15V			12.3	
			V_{CCB} = 2.5V ± 0.2V			12.3	
			V_{CCB} = 3.3V ± 0.3V			12.2	
t_{PZH}, t_{PZL}	$\overline{OE}$	B	V_{CCB} = 1.2V		4.1		ns
			V_{CCB} = 1.5V ± 0.1V			14.2	
			V_{CCB} = 1.8V ± 0.15V			12.4	
			V_{CCB} = 2.5V ± 0.2V			10.3	
			V_{CCB} = 3.3V ± 0.3V			9.6	
t_{PZH}, t_{PZL}	$\overline{OE}$	A	V_{CCB} = 1.2V		5.4		ns
			V_{CCB} = 1.5V ± 0.1V			13.6	
			V_{CCB} = 1.8V ± 0.15V			13.7	
			V_{CCB} = 2.5V ± 0.2V			13.7	
			V_{CCB} = 3.3V ± 0.3V			13.7	
t_{PZH}, t_{PZL}	$\overline{OE}$	B	V_{CCB} = 1.2V		5		ns
			V_{CCB} = 1.5V ± 0.1V			14.9	
			V_{CCB} = 1.8V ± 0.15V			13.7	
			V_{CCB} = 2.5V ± 0.2V			11.9	
			V_{CCB} = 3.3V ± 0.3V			11.9	

5.9 Switching Characteristics: V_{CCA} = 2.5V ± 0.2V

over recommended operating ambient temperature range, V_{CCA} = 2.5V ± 0.2V (see 图 6-1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CCB}	MIN	TYP	MAX	UNIT
t_{PLH}, t_{PHL}	A	B	V_{CCB} = 1.2V		2.8		ns
			V_{CCB} = 1.5V ± 0.1V			10.7	
			V_{CCB} = 1.8V ± 0.15V			9.6	
			V_{CCB} = 2.5V ± 0.2V			8.5	
			V_{CCB} = 3.3V ± 0.3V			8.6	

5.9 Switching Characteristics: V_{CCA} = 2.5V ± 0.2V（续）

over recommended operating ambient temperature range, V_{CCA} = 2.5V ± 0.2V (see 图 6-1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CCB}	MIN	TYP	MAX	UNIT
t_{PLH}, t_{PHL}	B	A	V_{CCB} = 1.2V		2.7		ns
			V_{CCB} = 1.5V ± 0.1V			9.2	
			V_{CCB} = 1.8V ± 0.15V			8.9	
			V_{CCB} = 2.5V ± 0.2V			8.4	
			V_{CCB} = 3.3V ± 0.3V			8.3	
t_{PZH}, t_{PZL}	$\overline{OE}$	A	V_{CCB} = 1.2V		4		ns
			V_{CCB} = 1.5V ± 0.1V			11.5	
			V_{CCB} = 1.8V ± 0.15V			10.2	
			V_{CCB} = 2.5V ± 0.2V			9.8	
			V_{CCB} = 3.3V ± 0.3V			9.8	
t_{PZH}, t_{PZL}	$\overline{OE}$	B	V_{CCB} = 1.2V		3.8		ns
			V_{CCB} = 1.5V ± 0.1V			13.8	
			V_{CCB} = 1.8V ± 0.15V			12	
			V_{CCB} = 2.5V ± 0.2V			9.8	
			V_{CCB} = 3.3V ± 0.3V			9	
t_{PHZ}, t_{PLZ}	$\overline{OE}$	A	V_{CCB} = 1.2V		4.7		ns
			V_{CCB} = 1.5V ± 0.1V			13.4	
			V_{CCB} = 1.8V ± 0.15V			13.4	
			V_{CCB} = 2.5V ± 0.2V			11.2	
			V_{CCB} = 3.3V ± 0.3V			11.5	
t_{PHZ}, t_{PLZ}	$\overline{OE}$	B	V_{CCB} = 1.2V		4.5		ns
			V_{CCB} = 1.5V ± 0.1V			14.4	
			V_{CCB} = 1.8V ± 0.15V			13.2	
			V_{CCB} = 2.5V ± 0.2V			11.2	
			V_{CCB} = 3.3V ± 0.3V			10.2	

5.10 Switching Characteristics: V_{CCA} = 3.3V ± 0.3V

over recommended operating ambient temperature range, V_{CCA} = 3.3V ± 0.3V (see 图 6-1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CCB}	MIN	TYP	MAX	UNIT
t_{PLH}, t_{PHL}	A	B	V_{CCB} = 1.2V		2.9		ns
			V_{CCB} = 1.5V ± 0.1V			10.6	
			V_{CCB} = 1.8V ± 0.15V			9.5	
			V_{CCB} = 2.5V ± 0.2V			8.3	
			V_{CCB} = 3.3V ± 0.3V			7.9	
t_{PLH}, t_{PHL}	B	A	V_{CCB} = 1.2V		2.6		ns
			V_{CCB} = 1.5V ± 0.1V			9.2	
			V_{CCB} = 1.8V ± 0.15V			8.4	
			V_{CCB} = 2.5V ± 0.2V			8	
			V_{CCB} = 3.3V ± 0.3V			7.8	

5.10 Switching Characteristics: V_{CCA} = 3.3V ± 0.3V（续）

over recommended operating ambient temperature range, V_{CCA} = 3.3V ± 0.3V (see 图 6-1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CCB}	MIN	TYP	MAX	UNIT
t_{PHZ}, t_{PLZ}	$\overline{OE}$	A	V_{CCB} = 1.2V		3.8		ns
			V_{CCB} = 1.5V ± 0.1V			13.7	
			V_{CCB} = 1.8V ± 0.15V			10.2	
			V_{CCB} = 2.5V ± 0.2V			8.8	
			V_{CCB} = 3.3V ± 0.3V			8.8	
t_{PHZ}, t_{PLZ}	$\overline{OE}$	B	V_{CCB} = 1.2V		3.7		ns
			V_{CCB} = 1.5V ± 0.1V			13.7	
			V_{CCB} = 1.8V ± 0.15V			11.8	
			V_{CCB} = 2.5V ± 0.2V			9.7	
			V_{CCB} = 3.3V ± 0.3V			8.8	
t_{PHZ}, t_{PLZ}	$\overline{OE}$	A	V_{CCB} = 1.2V		4.8		ns
			V_{CCB} = 1.5V ± 0.1V			14.3	
			V_{CCB} = 1.8V ± 0.15V			13.3	
			V_{CCB} = 2.5V ± 0.2V			10.6	
			V_{CCB} = 3.3V ± 0.3V			11.6	
t_{PHZ}, t_{PLZ}	$\overline{OE}$	B	V_{CCB} = 1.2V		5.3		ns
			V_{CCB} = 1.5V ± 0.1V			14.3	
			V_{CCB} = 1.8V ± 0.15V			13.1	
			V_{CCB} = 2.5V ± 0.2V			11.4	
			V_{CCB} = 3.3V ± 0.3V			11.2	

5.11 Operating Characteristics

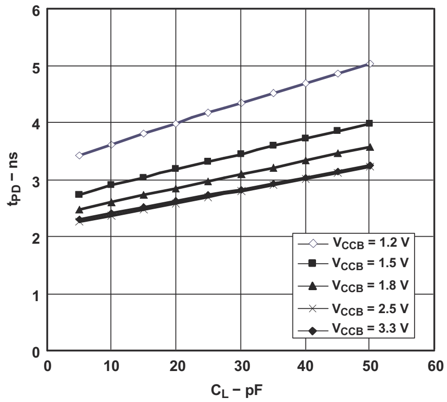
T_A = 25°C

PARAMETER			TEST CONDITIONS	V_{CCA}	TYP	UNIT
C_{pdA} (1)	A to B	Outputs enabled	C_L = 0, f = 10MHz, $t_r = t_f$ = 1ns	$V_{CCA} = V_{CCB}$ = 1.2V	1	pF
				$V_{CCA} = V_{CCB}$ = 1.5V	1	
				$V_{CCA} = V_{CCB}$ = 1.8V	1	
				$V_{CCA} = V_{CCB}$ = 2.5V	1.5	
				$V_{CCA} = V_{CCB}$ = 3.3V	2	
		Outputs disabled	C_L = 0, f = 10MHz, $t_r = t_f$ = 1ns	$V_{CCA} = V_{CCB}$ = 1.2V	1	
				$V_{CCA} = V_{CCB}$ = 1.5V		
				$V_{CCA} = V_{CCB}$ = 1.8V		
				$V_{CCA} = V_{CCB}$ = 2.5V		
				$V_{CCA} = V_{CCB}$ = 3.3V		
	B to A	Outputs enabled	C_L = 0, f = 10MHz, $t_r = t_f$ = 1ns	$V_{CCA} = V_{CCB}$ = 1.2V	12	
				$V_{CCA} = V_{CCB}$ = 1.5V	12.5	
				$V_{CCA} = V_{CCB}$ = 1.8V	13	
				$V_{CCA} = V_{CCB}$ = 2.5V	14	
				$V_{CCA} = V_{CCB}$ = 3.3V	15	
		Outputs disabled	C_L = 0, f = 10MHz, $t_r = t_f$ = 1ns	$V_{CCA} = V_{CCB}$ = 1.2V	1	
				$V_{CCA} = V_{CCB}$ = 1.5V		
				$V_{CCA} = V_{CCB}$ = 1.8V		
				$V_{CCA} = V_{CCB}$ = 2.5V		
				$V_{CCA} = V_{CCB}$ = 3.3V		
C_{pdB} (1)	A to B	Outputs enabled	C_L = 0, f = 10MHz, $t_r = t_f$ = 1ns	$V_{CCA} = V_{CCB}$ = 1.2V	12	pF
				$V_{CCA} = V_{CCB}$ = 1.5V	12.5	
				$V_{CCA} = V_{CCB}$ = 1.8V	13	
				$V_{CCA} = V_{CCB}$ = 2.5V	14	
				$V_{CCA} = V_{CCB}$ = 3.3V	15	
		Outputs disabled	C_L = 0, f = 10MHz, $t_r = t_f$ = 1ns	$V_{CCA} = V_{CCB}$ = 1.2V	1	
				$V_{CCA} = V_{CCB}$ = 1.5V		
				$V_{CCA} = V_{CCB}$ = 1.8V		
				$V_{CCA} = V_{CCB}$ = 2.5V		
				$V_{CCA} = V_{CCB}$ = 3.3V		
	B to A	Outputs enabled	C_L = 0, f = 10MHz, $t_r = t_f$ = 1ns	$V_{CCA} = V_{CCB}$ = 1.2V	1	
				$V_{CCA} = V_{CCB}$ = 1.5V	1	
				$V_{CCA} = V_{CCB}$ = 1.8V	1	
				$V_{CCA} = V_{CCB}$ = 2.5V	1	
				$V_{CCA} = V_{CCB}$ = 3.3V	2	
		Outputs disabled	C_L = 0, f = 10MHz, $t_r = t_f$ = 1ns	$V_{CCA} = V_{CCB}$ = 1.2V	1	
				$V_{CCA} = V_{CCB}$ = 1.5V		
				$V_{CCA} = V_{CCB}$ = 1.8V		
				$V_{CCA} = V_{CCB}$ = 2.5V		
				$V_{CCA} = V_{CCB}$ = 3.3V		

(1) Power dissipation capacitance per transceiver

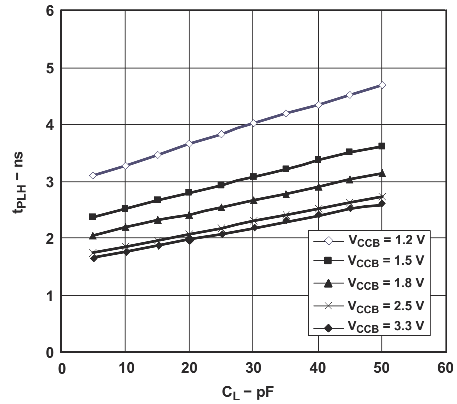
5.12 Typical Characteristics

T_A = 25°C



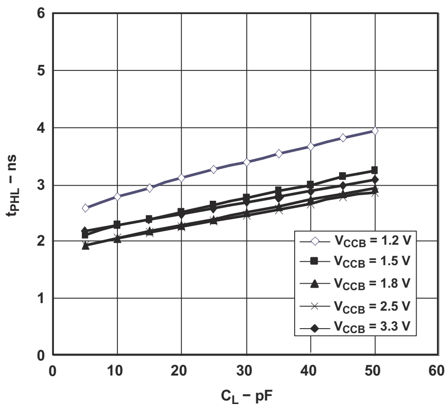
V_{CCA} = 1.2V

图 5-1. Typical Propagation Delay (A to B) vs Load Capacitance



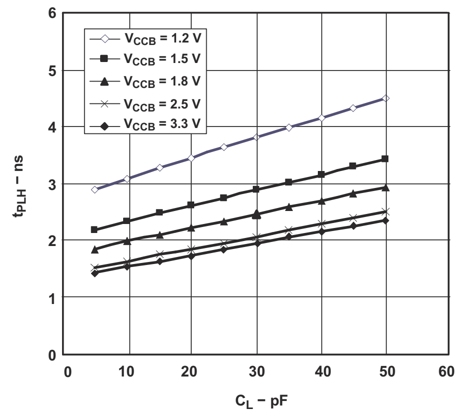
V_{CCA} = 1.5V

图 5-2. Typical Propagation Delay (A to B) vs Load Capacitance



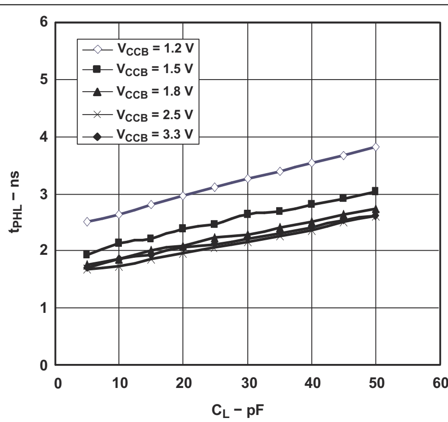
V_{CCA} = 1.5V

图 5-3. Typical Propagation Delay (A to B) vs Load Capacitance



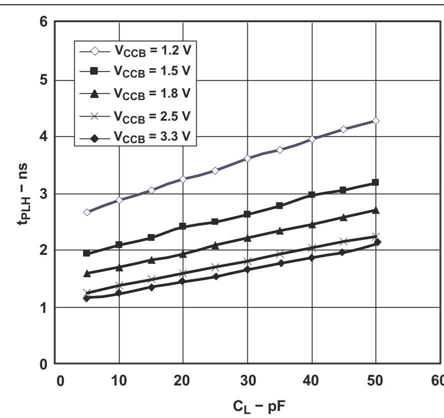
V_{CCA} = 1.8V

图 5-4. Typical Propagation Delay (A to B) vs Load Capacitance



V_{CCA} = 1.8V

图 5-5. Typical Propagation Delay (A to B) vs Load Capacitance

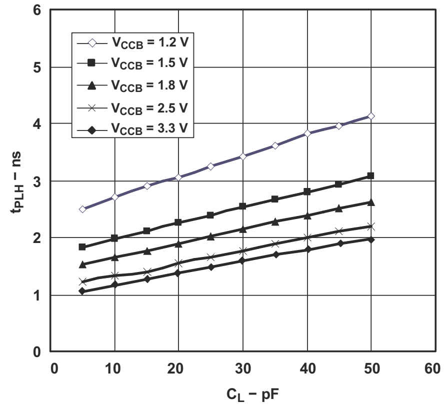


V_{CCA} = 2.5V

图 5-6. Typical Propagation Delay (A to B) vs Load Capacitance

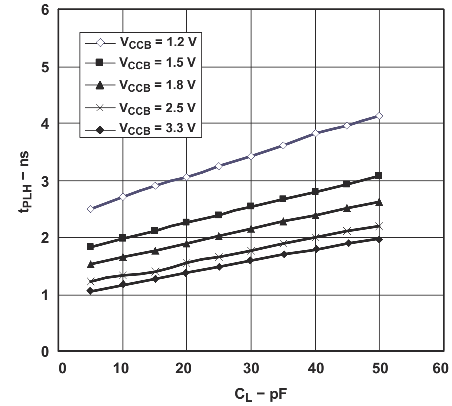
5.12 Typical Characteristics (continued)

T_A = 25°C



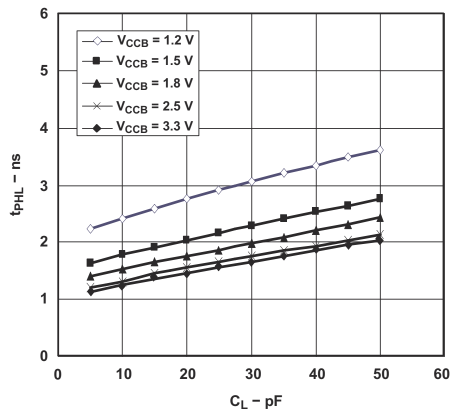
V_{CCA} = 2.5V

图 5-7. Typical Propagation Delay (A to B) vs Load Capacitance



V_{CCA} = 3.3V

图 5-8. Typical Propagation Delay (A to B) vs Load Capacitance



V_{CCA} = 3.3V

图 5-9. Typical Propagation Delay (A to B) vs Load Capacitance

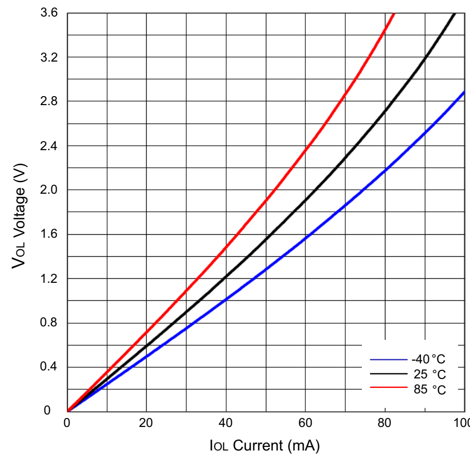


图 5-10. Low-Level Output Voltage (V_{OL}) vs Low-Level Current (I_{OL})

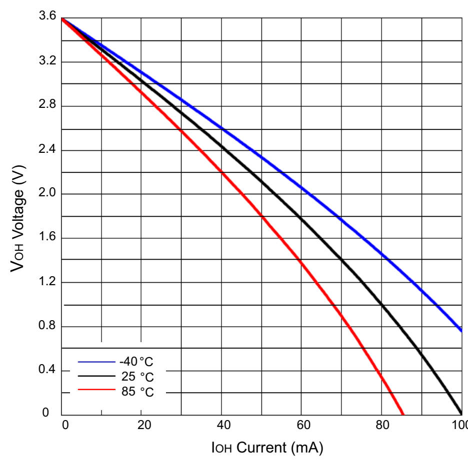
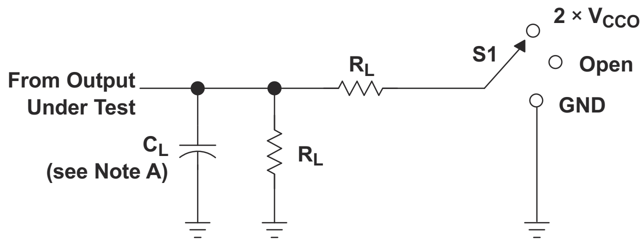


图 5-11. High-Level Output Voltage (V_{OH}) vs High-Level Current (I_{OH})

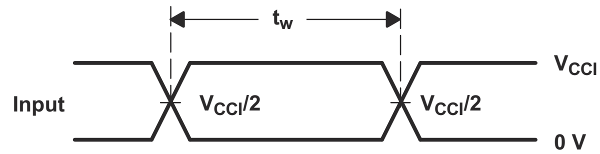
6 Parameter Measurement Information



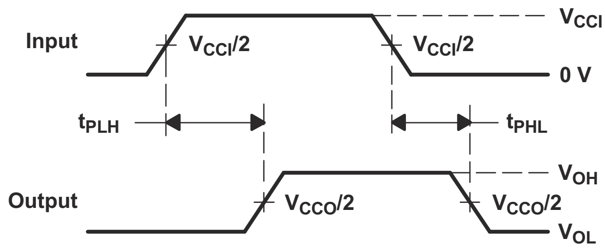
LOAD CIRCUIT

TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	2 × V_{CCO}
t_{PHZ}/t_{PZH}	GND

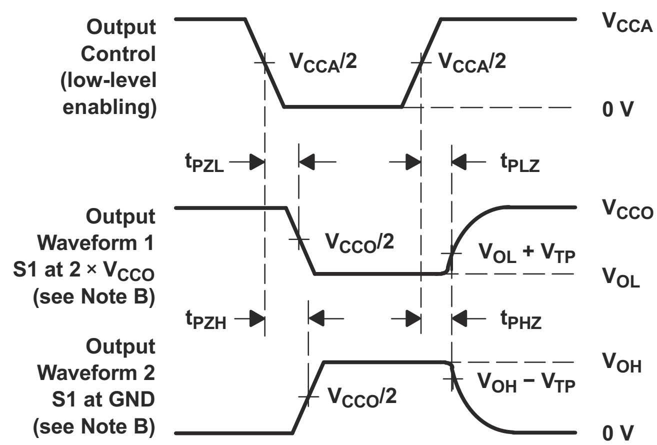
V_{CCO}	C_L	R_L	V_{TP}
1.2 V	15 pF	2 kΩ	0.1 V
1.5 V ± 0.1 V	15 pF	2 kΩ	0.1 V
1.8 V ± 0.15 V	15 pF	2 kΩ	0.15 V
2.5 V ± 0.2 V	15 pF	2 kΩ	0.15 V
3.3 V ± 0.3 V	15 pF	2 kΩ	0.3 V



VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

NOTES:
- A. C_L includes probe and jig capacitance.
- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, dv/dt ≥ 1 V/ns.
- D. The outputs are measured one at a time, with one transition per measurement.
- E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
- F. t_{PZL} and t_{PZH} are the same as t_{en}.
- G. t_{PLH} and t_{PHL} are the same as t_{pd}.
- H. V_{CCI} is the V_{CC} associated with the input port.
- I. V_{CCO} is the V_{CC} associated with the output port.

图 6-1. Load and Circuit and Voltage Waveforms

7 Detailed Description

7.1 Overview

The SN74AVC4T245-Q1 is a 4-bit, dual-supply noninverting bidirectional voltage level translation device. Ax pins and control pins (1DIR, 2DIR,1 $\overline{OE}$, and 2 $\overline{OE}$) are supported by V_{CCA}, and Bx pins are supported by V_{CCB}. The A port is able to accept I/O voltages ranging from 1.2V to 3.6V, while the B port can accept I/O voltages from 1.2V to 3.6V. A high on DIR allows data transmission from Ax to Bx and a low on DIR allows data transmission from Bx to Ax when $\overline{OE}$ is set to low. When $\overline{OE}$ is set to high, both Ax and Bx pins are in the high-impedance state.

7.2 Functional Block Diagram

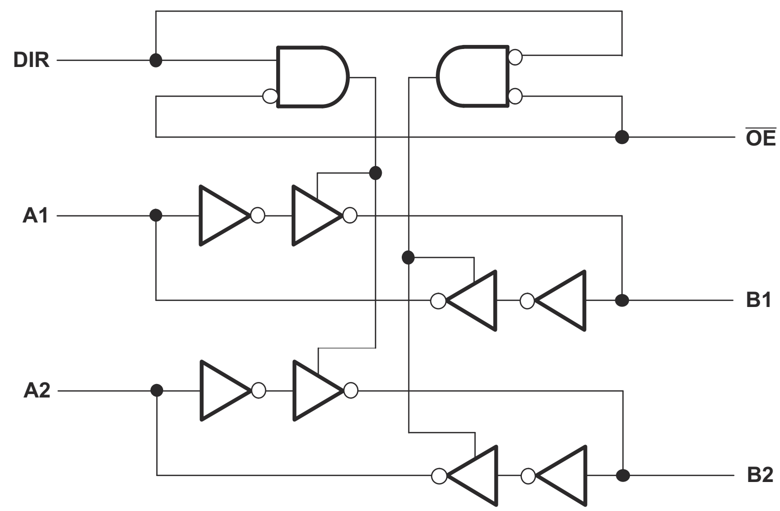


图 7-1. Logic Diagram (Positive Logic) for 1/2 of SN74AVC4T245-Q1

7.3 Feature Description

7.3.1 Fully Configurable Dual-Rail Design

Both V_{CCA} and V_{CCB} can be supplied at any voltage between 1.2V and 3.6V; thus, making the device suitable for translating between any of the low voltage nodes (1.2V, 1.8V, 2.5V, and 3.3V).

7.3.2 Supports High Speed Translation

The SN74AVC4T245-Q1 device can support high data rate applications. The translated signal data rate can be up to 380Mbps when the signal is translated from 1.8V to 3.3V.

7.3.3 I_{off} Supports Partial-Power-Down Mode Operation

I_{off} prevents backflow current by disabling I/O output circuits when the device is in partial-power-down mode.

7.4 Device Functional Modes

表 7-1 lists the functional modes of the SN74AVC4T245-Q1 device.

表 7-1. Function Table (Each 2-Bit Section)

CONTROL INPUTS		OUTPUT CIRCUITS		OPERATION
$\overline{OE}$	DIR	A PORT	B PORT	
L	L	Enabled	Hi-Z	B data to A bus
L	H	Hi-Z	Enabled	A data to B bus
H	X	Hi-Z	Hi-Z	Isolation

8 Application and Implementation

备注

以下应用部分中的信息不属于 TI 元件规格，TI 不担保其准确性和完整性。TI 的客户负责确定元件是否适合其用途，以及验证和测试其设计实现以确认系统功能。

8.1 Application Information

The SN74AVC4T245-Q1 device can be used in level-translation applications for interfacing devices or systems operating at different interface voltages with one another. The SN74AVC4T245-Q1 device is ideal for use in applications where a push-pull driver is connected to the data I/Os. The maximum data rate can be up to 380Mbps when the device translates a signal from 1.8V to 3.3V.

8.2 Typical Application

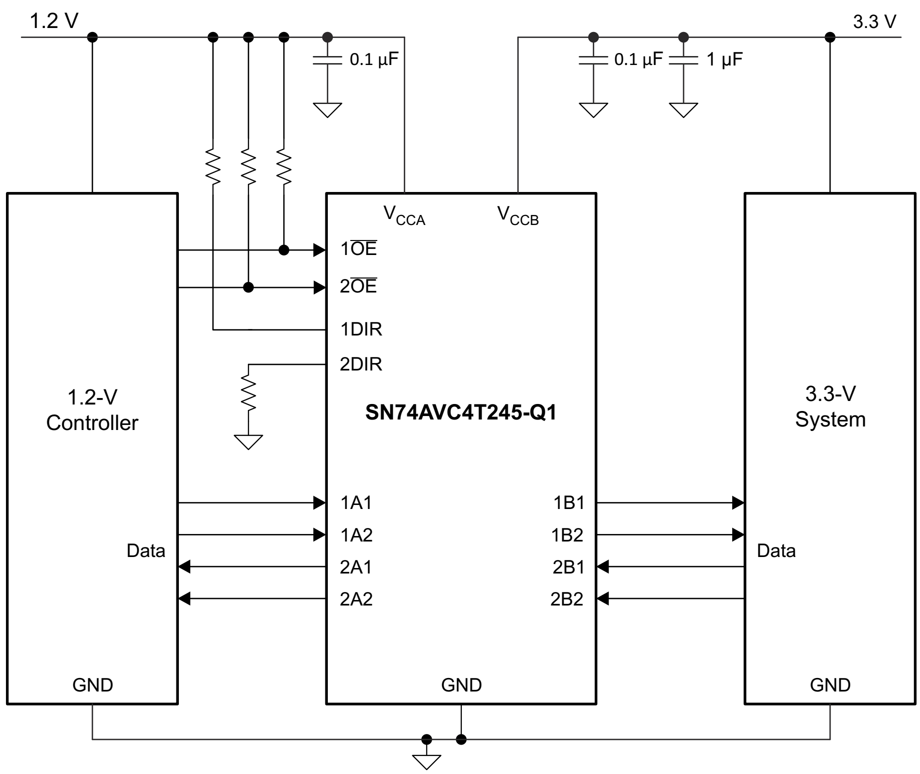


图 8-1. Typical Application Diagram

8.2.1 Design Requirements

表 8-1 lists the parameters for this design example.

表 8-1. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Input voltage range	1.2V
Output voltage range	3.3V

8.2.2 Detailed Design Procedure

To begin the design process, determine the following:

- Input voltage range
  - Use the supply voltage of the device that is driving the SN74AVC4T245-Q1 device to determine the input voltage range. For a valid logic high, the value must exceed the V_{IH} of the input port. For a valid logic low, the value must be less than the V_{IL} of the input port. For this example, the input voltage is 1.2V.
- Output voltage range
  - Use the supply voltage of the device that the SN74AVC4T245-Q1 device is driving to determine the output voltage range. For this example, the output voltage is 3.3V.

8.2.3 Application Curve

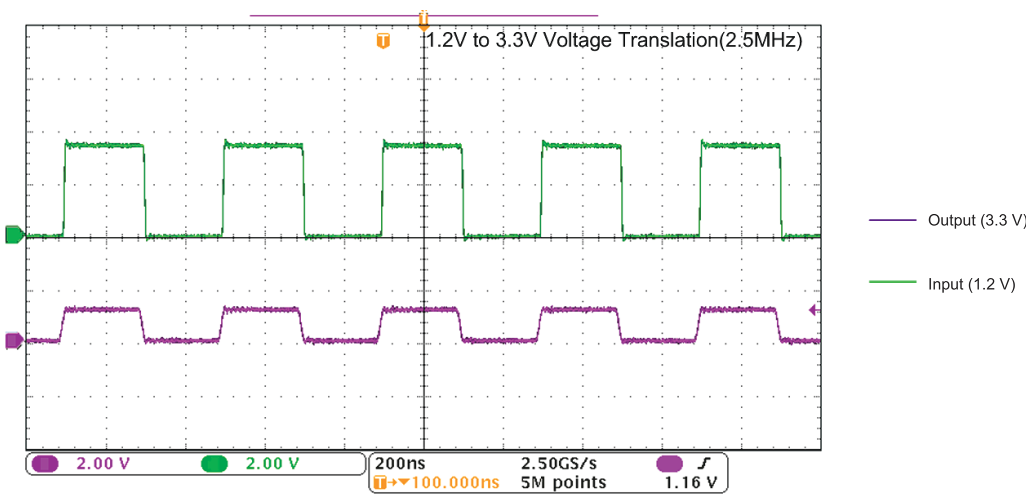


图 8-2. Translation Up (1.2V to 3.3V) at 2.5MHz

8.3 Power Supply Recommendations

The SN74AVC4T245-Q1 device uses two separate configurable power-supply rails: V_{CCA} and V_{CCB}. V_{CCA} accepts any supply voltage from 1.2V to 3.6V, and V_{CCB} accepts any supply voltage from 1.2V to 3.6V. The A port and B port are designed to track V_{CCA} and V_{CCB} respectively, allowing for low-voltage bidirectional translation between any of the 1.2V, 1.5V, 1.8V, 2.5V, and 3.3V voltage nodes.

The output-enable ($\overline{OE}$) input circuit is designed so that it is supplied by V_{CCA}; when the $\overline{OE}$ input is high, all outputs are placed in the high-impedance state. To place the outputs in the high-impedance state during power up or power down, tie the $\overline{OE}$ input pin to V_{CCA} through a pullup resistor and do not enable it until V_{CCA} and V_{CCB} are fully ramped and stable. The minimum value of the pullup resistor to V_{CCA} is determined by the current-sinking capability of the driver.

8.4 Layout

8.4.1 Layout Guidelines

For device reliability, it is recommended to follow common printed-circuit board layout guidelines such as:

- Use bypass capacitors on power supplies.
- Use short trace lengths to avoid excessive loading.
- Place pads on the signal paths for loading capacitors or pullup resistors to help adjust rise and fall times of signals, depending on the system requirements.

8.4.2 Layout Example

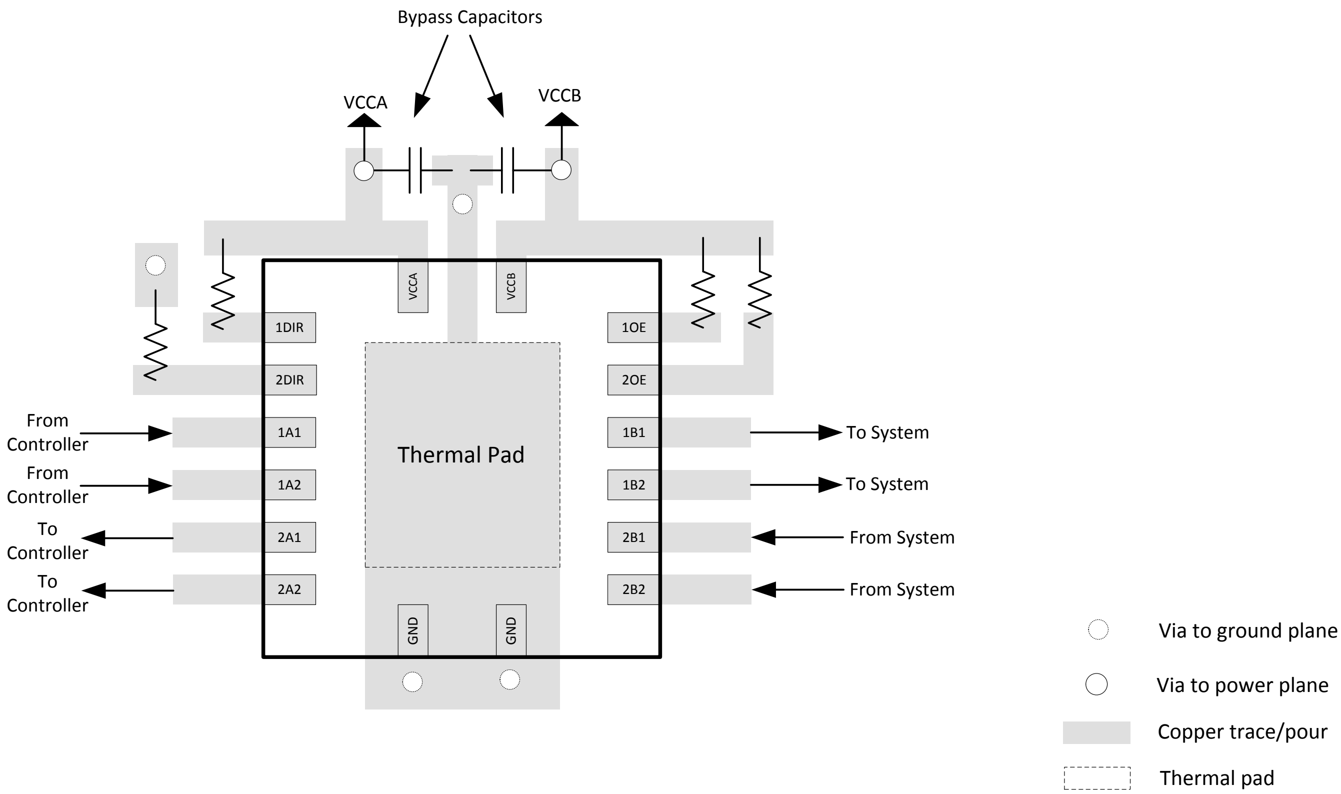


图 8-3. SN74AVC4T245-Q1 RGY Package Layout Diagram

9 Device and Documentation Support

9.1 Documentation Support

9.1.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, *IC Package Thermal Metrics*
- Texas Instruments, *Implications of Slow or Floating CMOS Inputs*

9.2 接收文档更新通知

要接收文档更新通知，请导航至 ti.com 上的器件产品文件夹。点击*通知* 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

9.3 支持资源

TI E2E™ 中文支持论坛是工程师的重要参考资料，可直接从专家处获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题，获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的使用条款。

9.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.
所有商标均为其各自所有者的财产。

9.5 静电放电警告

静电放电 (ESD) 会损坏这个集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

9.6 术语表

TI 术语表　　本术语表列出并解释了术语、首字母缩略词和定义。

10 Revision History

注：以前版本的页码可能与当前版本的页码不同

Changes from Revision B (March 2016) to Revision C (February 2024) — **Page**

- 向“特性”列表添加了功能安全链接 1
- 更新了“封装信息”表以包含封装引线尺寸 1
- 添加了 *PW*、*BQB* 和 *DYY* 封装 1

Changes from Revision A (October 2012) to Revision B (October 2015) — **Page**

- 添加了*应用* 部分 1
- 在整个数据表中向器件型号添加了 -Q1 1
- 向数据表中添加了*器件信息* 表 1
- 删除了数据表中的*订购信息* 表 1
- Added *Pin Functions* table to the data sheet 3
- Added *ESD Ratings* table to the data sheet 5
- Added *Thermal Information* table to the data sheet 6

- Added *Typical Characteristics* section to the data sheet... 14
- Added 图 5-1 through 图 5-9 to the *节 5.12* section 14
- Added all new content from *节 8.1* through the end of the data sheet... 17

Changes from Revision * (November 2009) to Revision A (October 2012) **Page**

- 向“特性”添加了 AEC-Q100 信息... 1
- 删除了"特性"中的“ESD 保护性能超过 JESD 22 规范要求（8000V 人体放电模型 (A114-A) 和 1000V 充电器件模型 (C101)）” 1

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most-current data available for the designated device. This data is subject to change without notice and without revision of this document. For browser-based versions of this data sheet, see the left-hand navigation pane.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
74AVC4T245QDYYRQ1	ACTIVE	SOT-23-THIN	DYY	16	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	WT245Q	Samples
74AVC4T245QPWRQ1	ACTIVE	TSSOP	PW	16	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	WT245Q	Samples
74AVC4T245QRGYRQ1	ACTIVE	VQFN	RGY	16	3000	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 125	4T245Q	Samples
74AVC4T245QWBQBRQ1	ACTIVE	WQFN	BQB	16	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	WT245Q	Samples

[1] The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

[2] **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

[3] MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

[4] There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

[5] Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

[6] Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF SN74AVC4T245-Q1 :

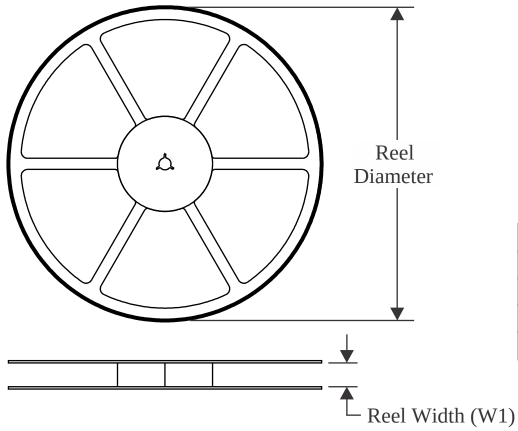
- Catalog : SN74AVC4T245

NOTE: Qualified Version Definitions:

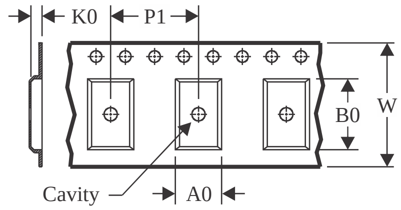
- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

REEL DIMENSIONS

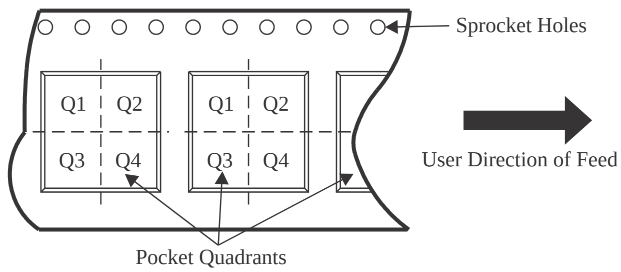


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

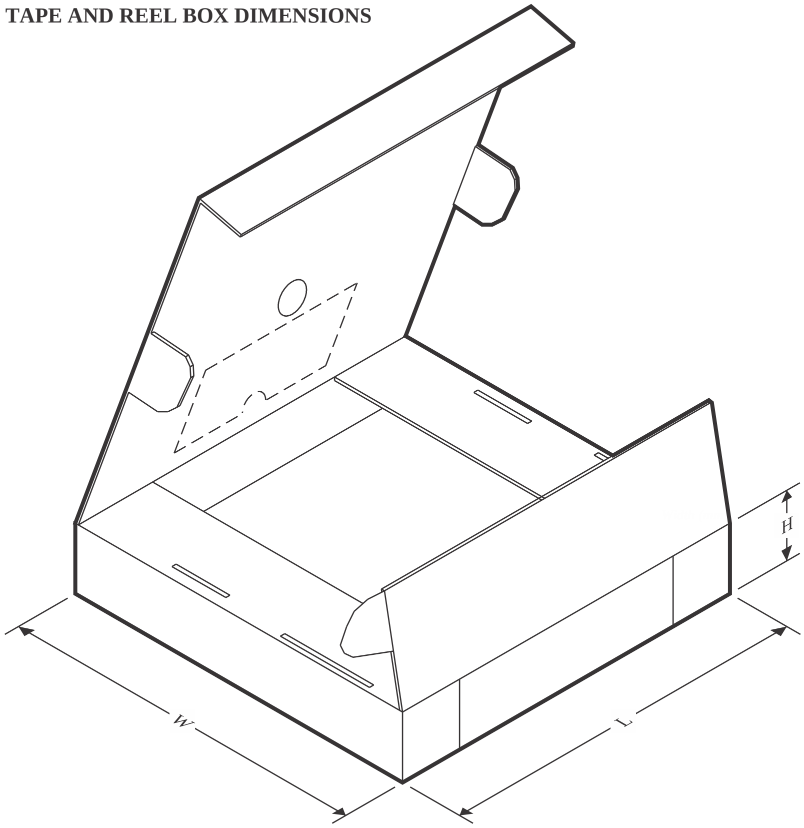
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

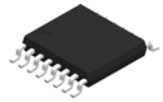
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
74AVC4T245QDYYRQ1	SOT-23-THIN	DYY	16	3000	330.0	12.4	4.8	3.6	1.6	8.0	12.0	Q3
74AVC4T245QPWRQ1	TSSOP	PW	16	3000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
74AVC4T245QRGYRQ1	VQFN	RGY	16	3000	330.0	12.4	3.8	4.3	1.5	8.0	12.0	Q1
74AVC4T245QWBQBRQ1	WQFN	BQB	16	3000	180.0	12.4	2.8	3.8	1.2	4.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

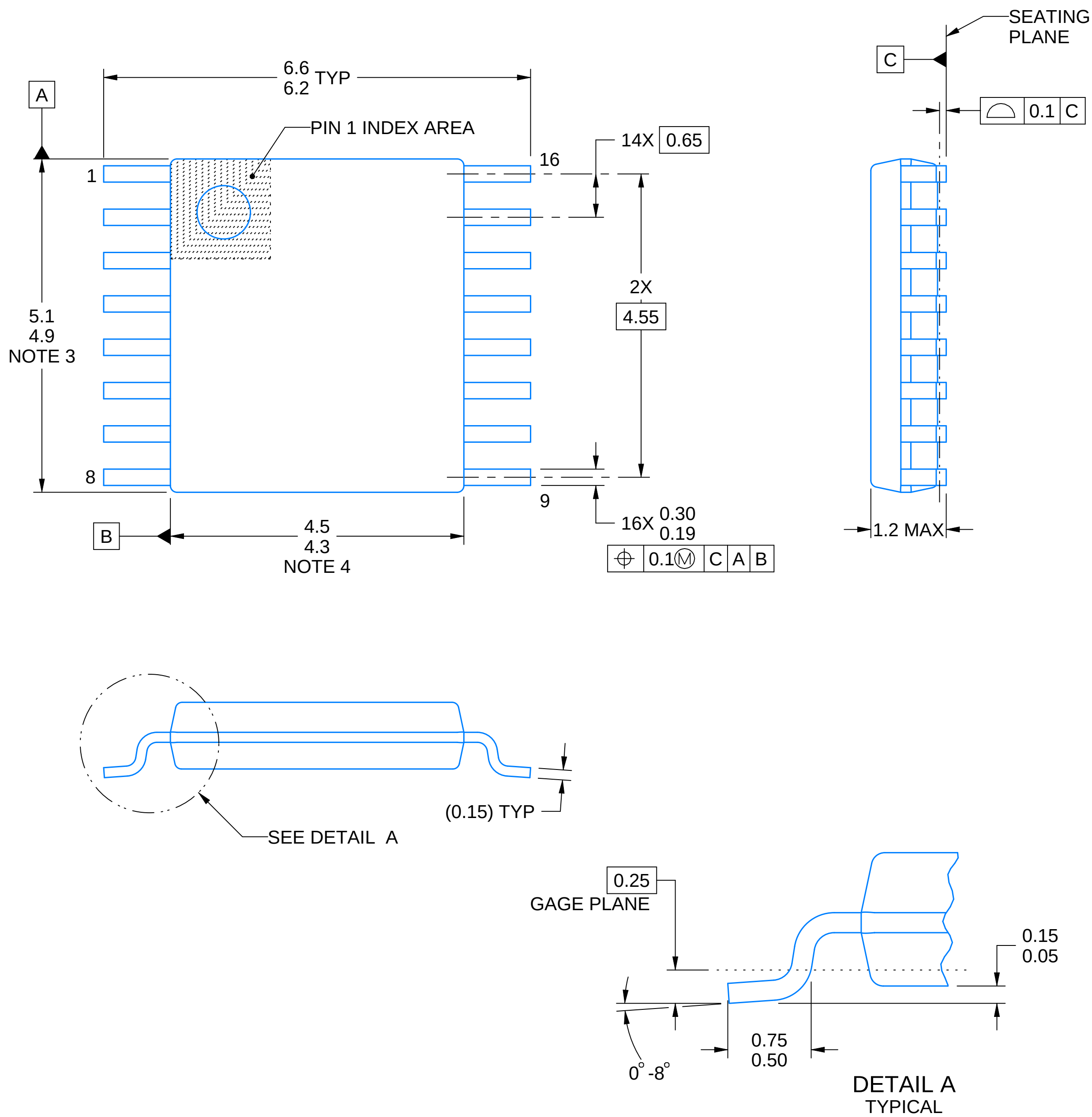
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
74AVC4T245QDYYRQ1	SOT-23-THIN	DYY	16	3000	336.6	336.6	31.8
74AVC4T245QPWRQ1	TSSOP	PW	16	3000	356.0	356.0	35.0
74AVC4T245QRGYRQ1	VQFN	RGY	16	3000	356.0	356.0	35.0
74AVC4T245QWBQBRQ1	WQFN	BQB	16	3000	210.0	185.0	35.0



PACKAGE OUTLINE

TSSOP - 1.2 mm max height

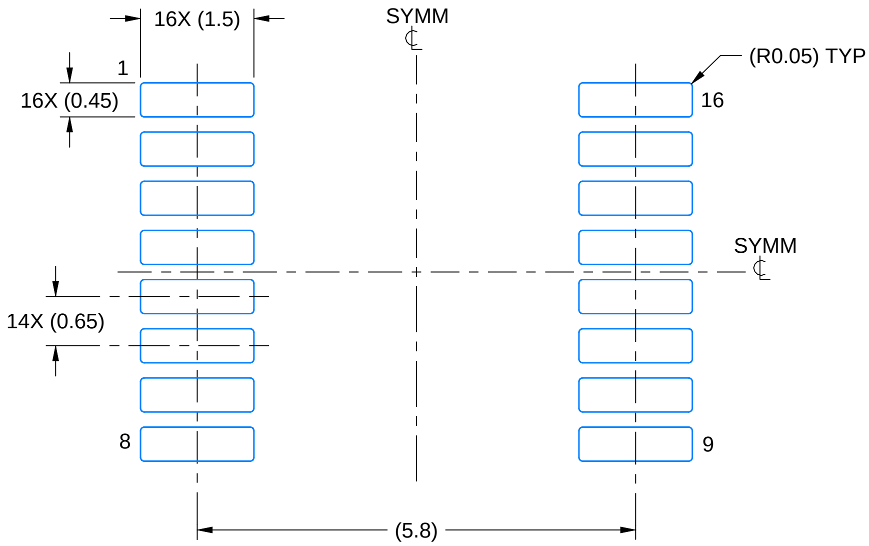
SMALL OUTLINE PACKAGE



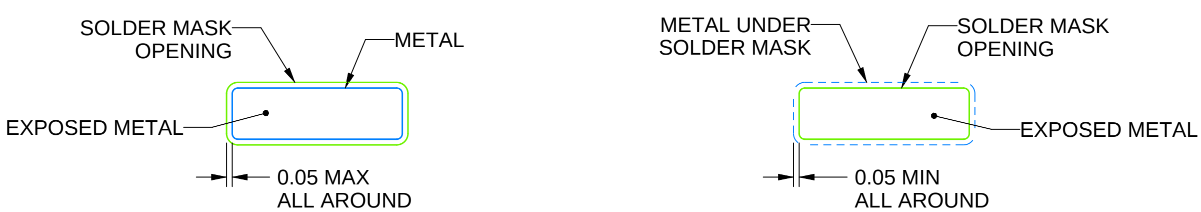
4220204/A 02/2017

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



NON-SOLDER MASK DEFINED (PREFERRED)

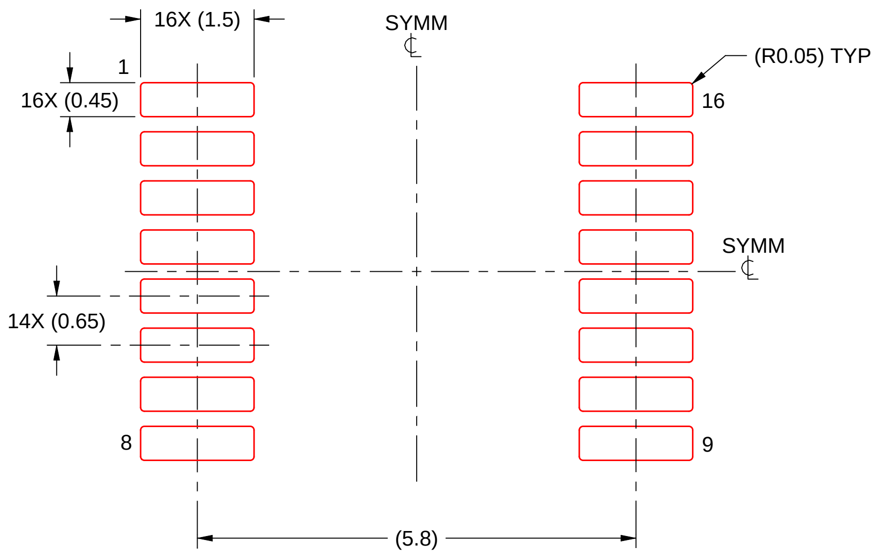
SOLDER MASK DEFINED

SOLDER MASK DETAILS

4220204/A 02/2017

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220204/A 02/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

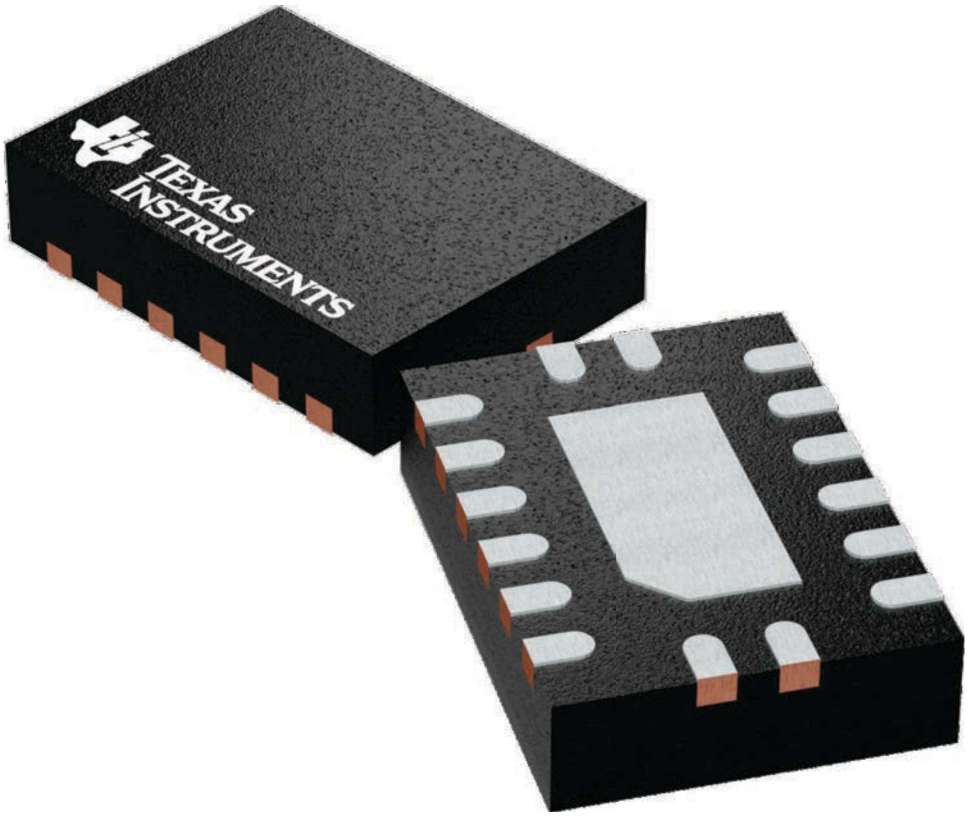
BQB 16

WQFN - 0.8 mm max height

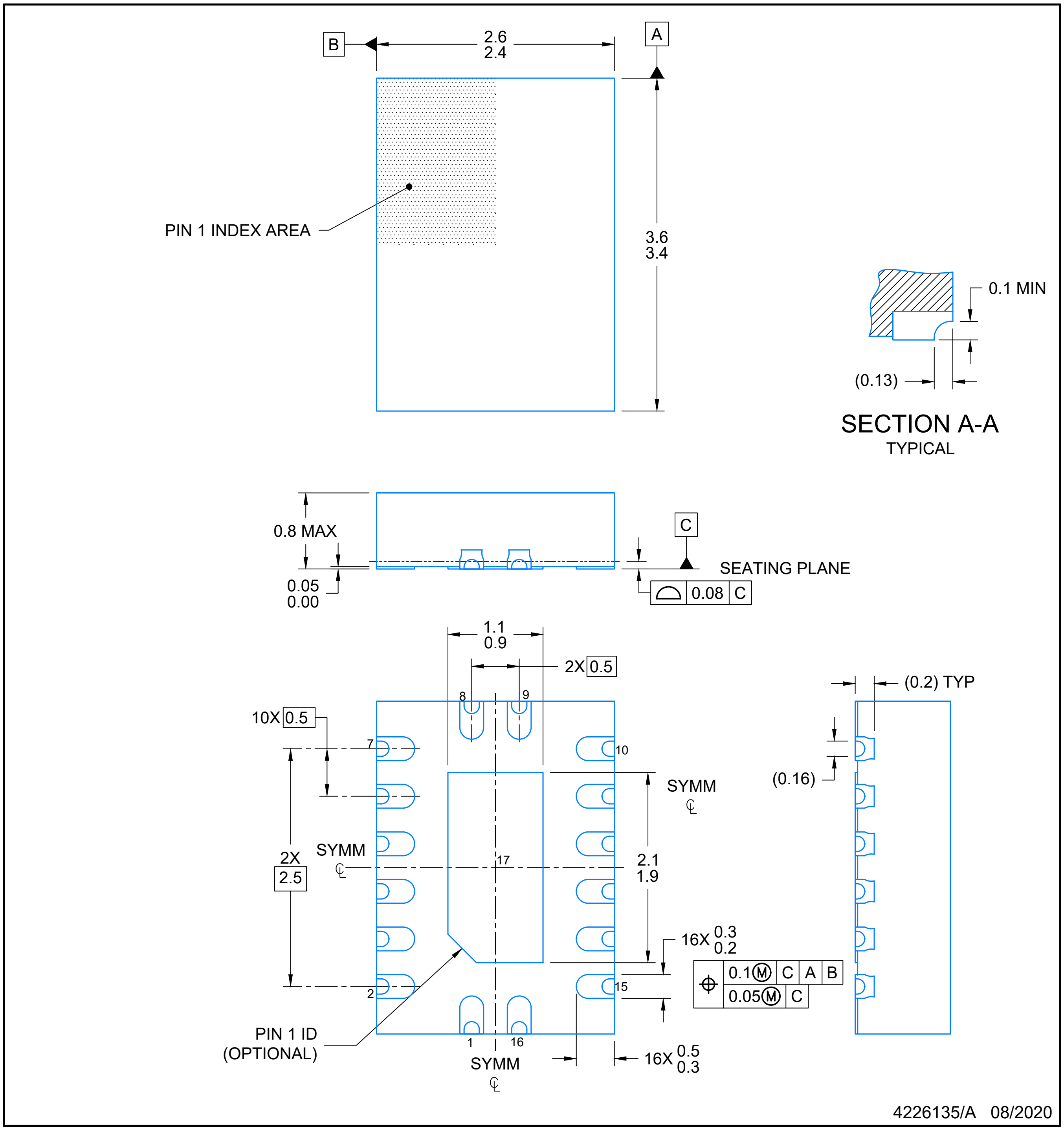
2.5 x 3.5, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

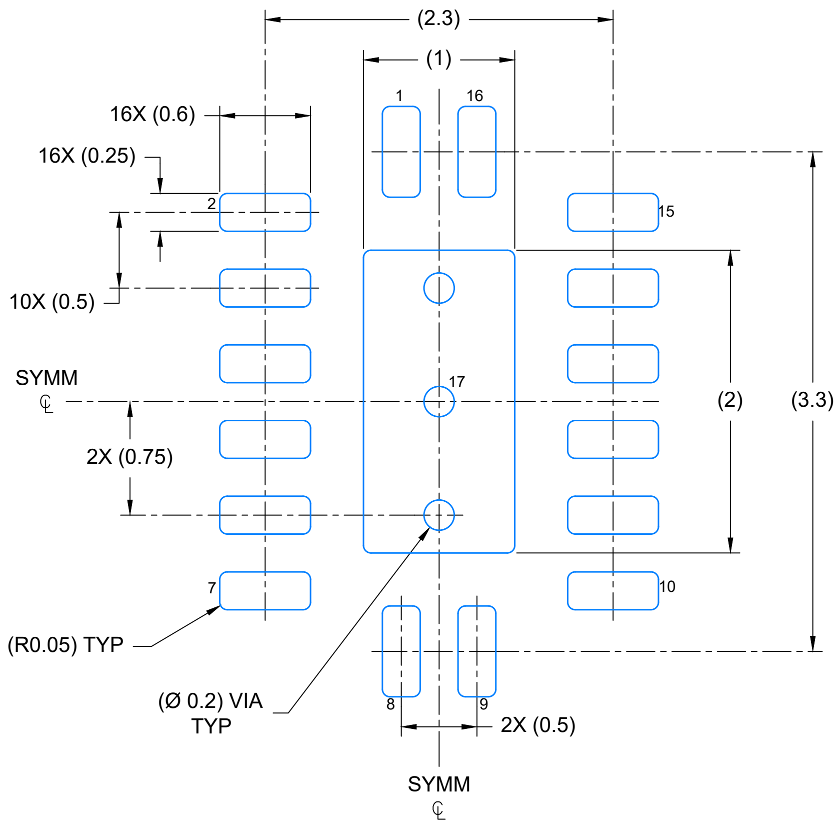


4226161/A



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.

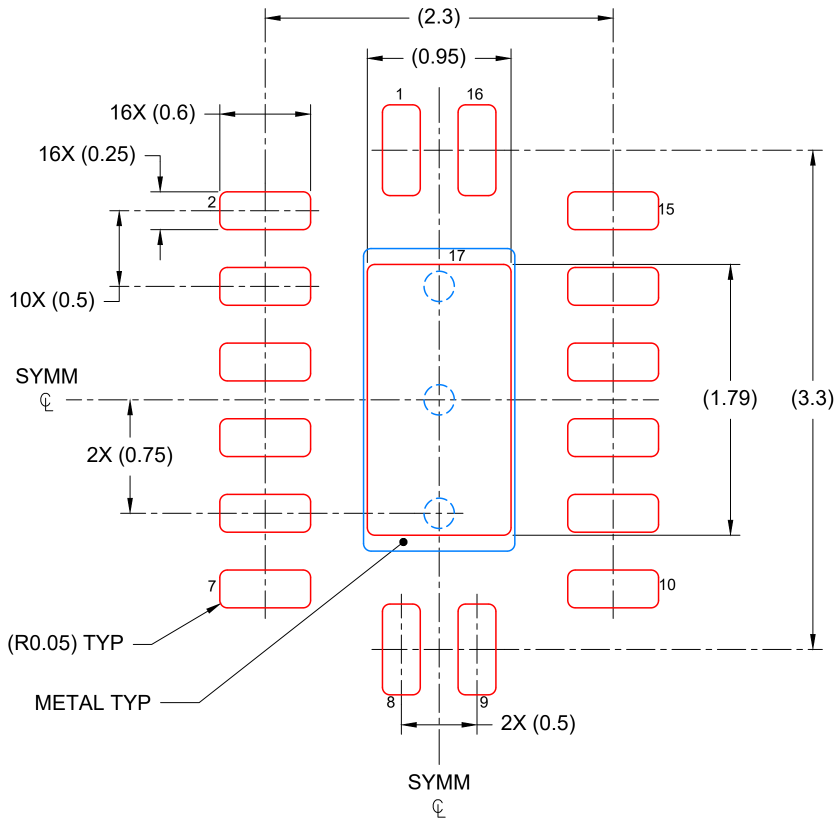


LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 20X

4226135/A 08/2020

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



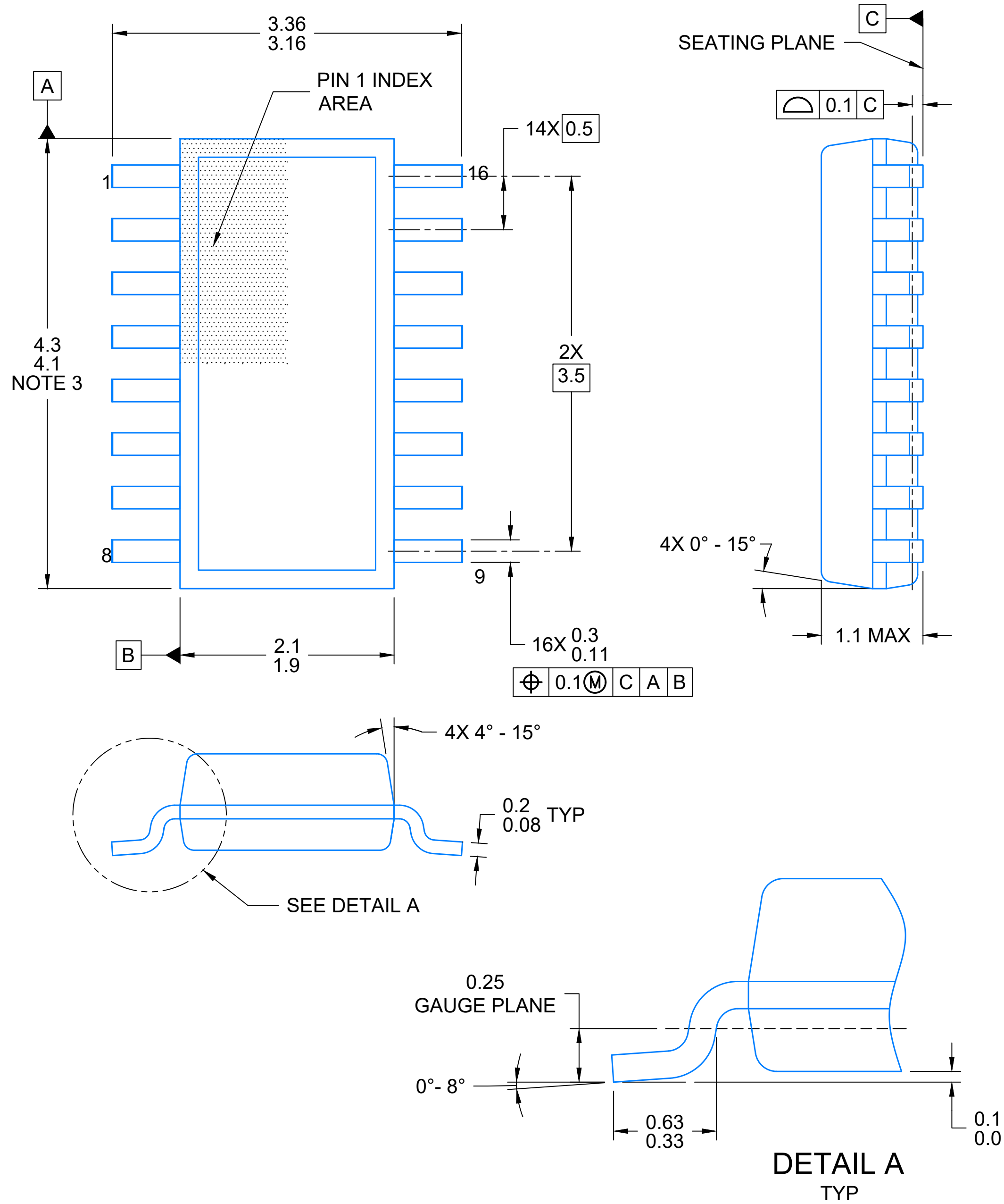
SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
85% PRINTED COVERAGE BY AREA
SCALE: 20X

4226135/A 08/2020

NOTES: (continued)

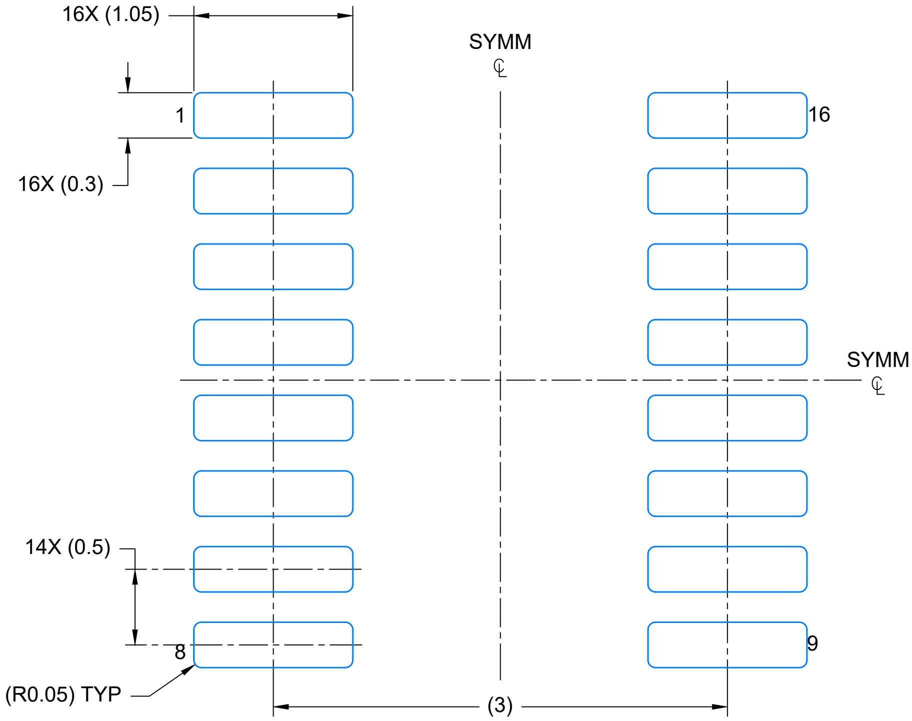
6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.



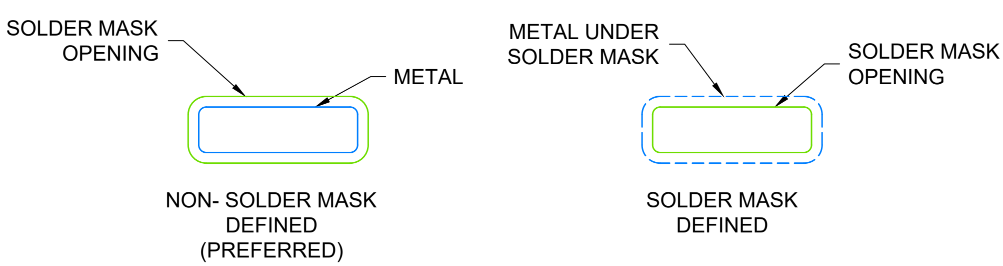
4224642/D 07/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
5. Reference JEDEC Registration MO-345, Variation AA



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 20X

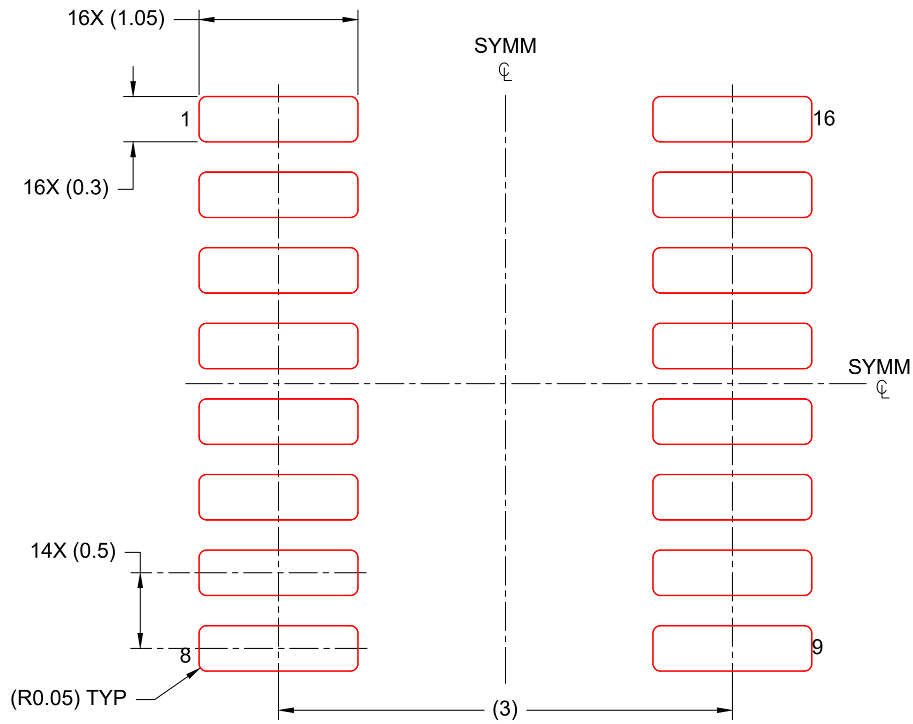


SOLDER MASK DETAILS

4224642/D 07/2024

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



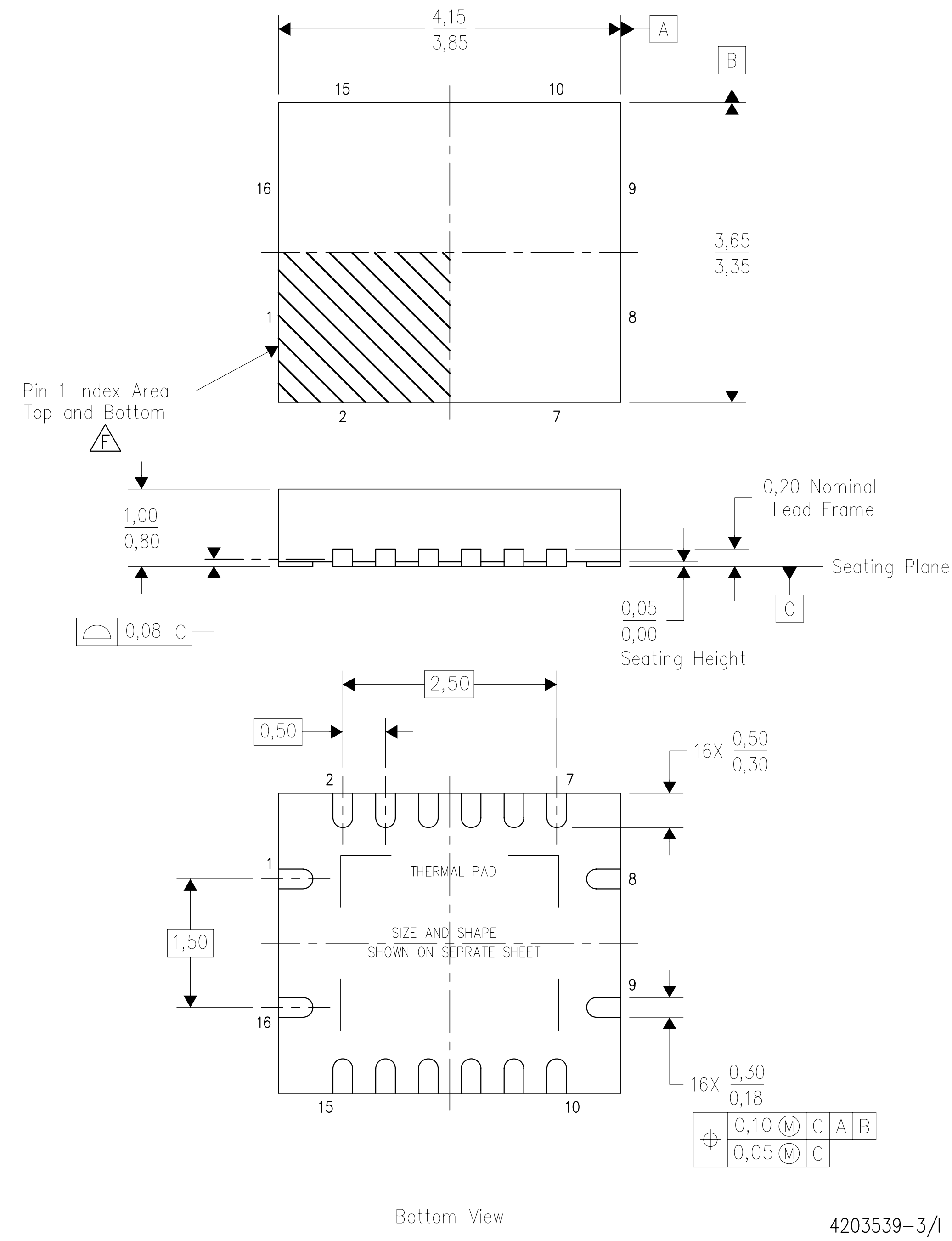
SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 20X

4224642/D 07/2024

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

RGY (R-PVQFN-N16) PLASTIC QUAD FLATPACK NO-LEAD



4203539-3/I 06/2011

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
B. This drawing is subject to change without notice.
C. QFN (Quad Flatpack No-Lead) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. Pin 1 identifiers are located on both top and bottom of the package and within the zone indicated. The Pin 1 identifiers are either a molded, marked, or metal feature.
G. Package complies to JEDEC MO-241 variation BA.

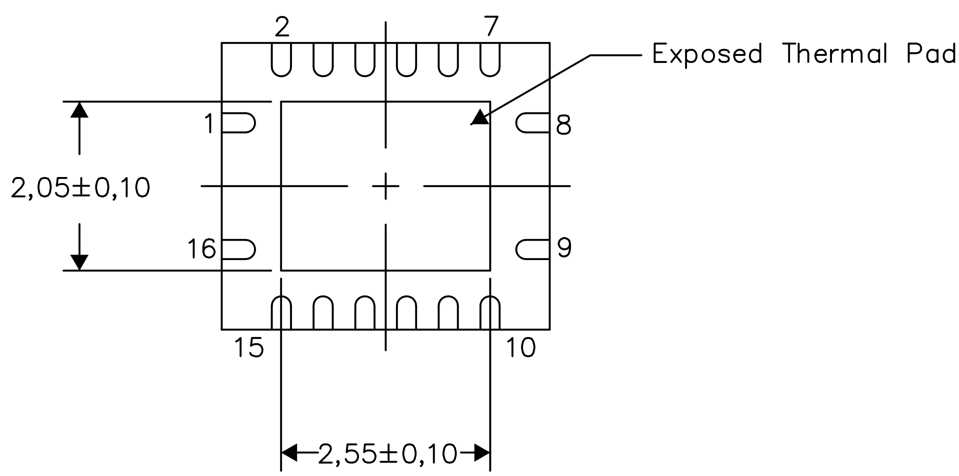
RGY (R–PVQFN–N16) PLASTIC QUAD FLATPACK NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



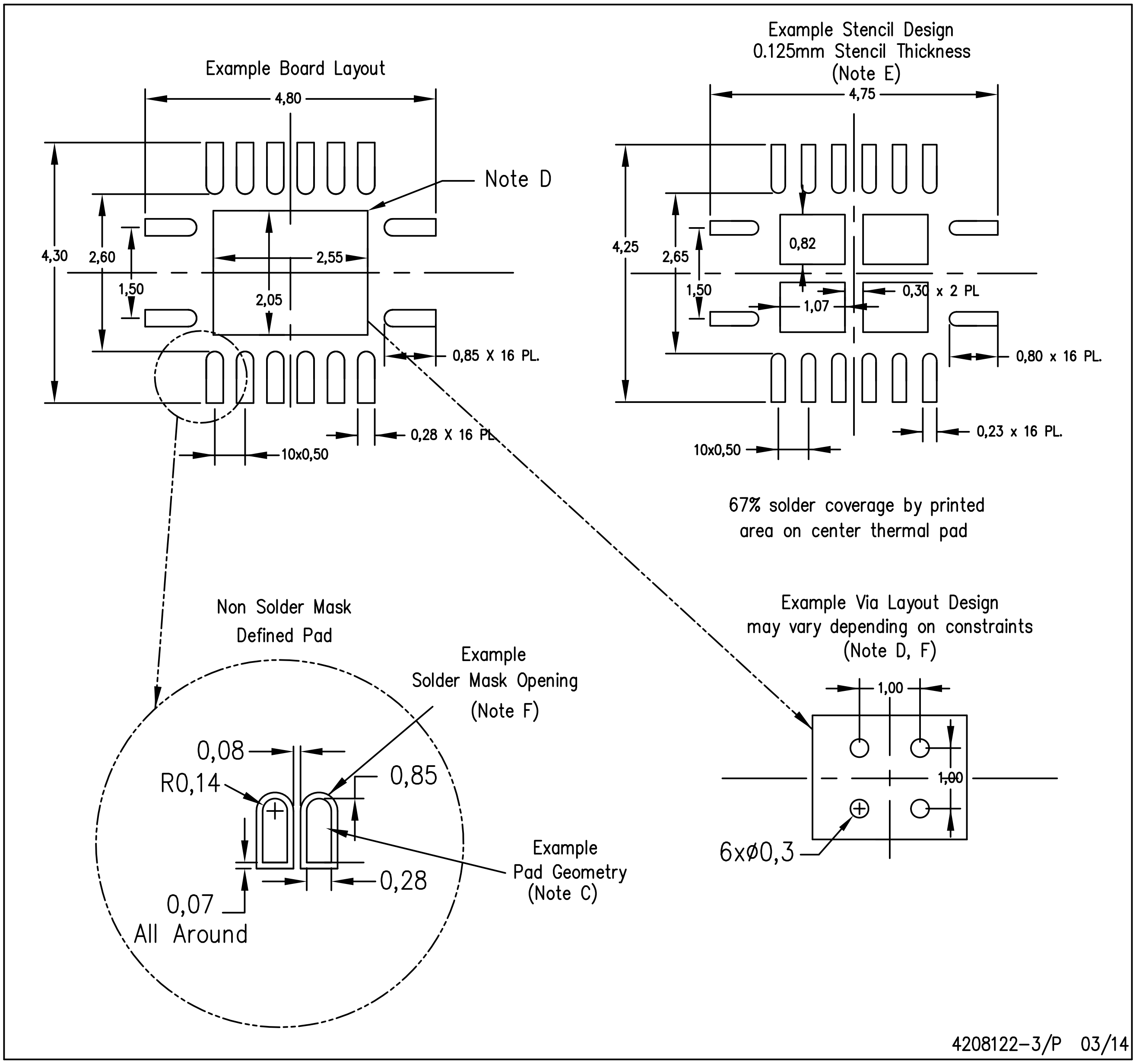
Bottom View

Exposed Thermal Pad Dimensions

4206353–3/P 03/14

NOTE: All linear dimensions are in millimeters

RGY (R–PVQFN–N16) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:

A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http: //www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.

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