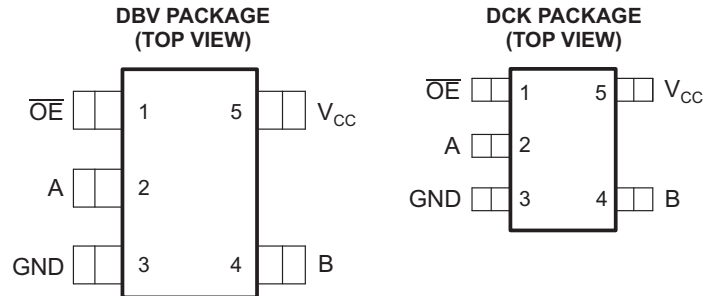


## FEATURES

- 5-Ω Switch Connection Between Two Ports
- TTL-Compatible Control Input Levels
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Protection Exceeds JESD 22
  - 2000-V Human-Body Model (A114-A)
  - 200-V Machine Model (A115-A)



See mechanical drawings for dimensions.

## DESCRIPTION/ORDERING INFORMATION

The SN74CBTD1G125 features a single high-speed line switch. The switch is disabled when the output-enable ( $\overline{OE}$ ) input is high. A diode to  $V_{CC}$  is integrated on the chip to allow for level shifting from 5-V signals at the device inputs to 3.3-V signals at the device outputs.

### ORDERING INFORMATION

$T_A$	PACKAGE <sup>(1)</sup>		ORDERABLE PART NUMBER	TOP-SIDE MARKING <sup>(2)</sup>
–40°C to 85°C	SOT (SOT-23) – DBV	Reel of 3000	SN74CBTD1G125DBVR	P25_
		Reel of 250	SN74CBTD1G125DBVT	
	SOT (SC-70) – DCK	Reel of 3000	SN74CBTD1G125DCKR	PM_
		Reel of 250	SN74CBTD1G125DCKT	

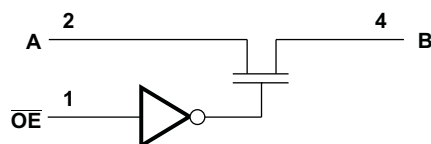
(1) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at [www.ti.com/sc/package](http://www.ti.com/sc/package).

(2) The actual top-side marking has one additional character that designates the assembly/test site.

### FUNCTION TABLE

INPUT $\overline{OE}$	FUNCTION
L	A port = B port
H	Disconnect

### LOGIC DIAGRAM (POSITIVE LOGIC)



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

# SN74CBTD1G125

## SINGLE FET BUS SWITCH

### WITH LEVEL SHIFTING

SCDS063L–JULY 1998–REVISED JUNE 2006

### Absolute Maximum Ratings<sup>(1)</sup>

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT	
V <sub>CC</sub>	Supply voltage range	–0.5	7	V	
V <sub>I</sub>	Input voltage range <sup>(2)</sup>	–0.5	7	V	
	Continuous channel current		128	mA	
I <sub>IK</sub>	Input clamp current	V <sub>I/O</sub> < 0		–50	mA
θ <sub>JA</sub>	Package thermal impedance <sup>(3)</sup>	DBV package		206	°C/W
		DCK package		252	
T <sub>stg</sub>	Storage temperature range	–65	150	°C	

- (1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
- (3) The package thermal impedance is calculated in accordance with JESD 51-7.

### Recommended Operating Conditions<sup>(1)</sup>

		MIN	MAX	UNIT
V <sub>CC</sub>	Supply voltage	4.5	5.5	V
V <sub>IH</sub>	High-level control input voltage <sup>(2)</sup>	2		V
V <sub>IL</sub>	Low-level control input voltage		0.8	V
T <sub>A</sub>	Operating free-air temperature	–40	85	°C

- (1) All unused control inputs of the device must be held at V<sub>CC</sub> or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.
- (2) In applications with fast edge rates, multiple outputs switching, and operating at high frequencies, the output may have little or no level-shifting effect.

### Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP <sup>(1)</sup>	MAX	UNIT
V <sub>IK</sub>		V <sub>CC</sub> = 4.5 V,	I <sub>I</sub> = –18 mA			–1.2	V
V <sub>OH</sub>		See <a href="#">Figure 2</a>					
I <sub>I</sub>		V <sub>CC</sub> = 5.5 V,	V <sub>I</sub> = 5.5 V or GND			±1	μA
I <sub>CC</sub>		V <sub>CC</sub> = 5.5 V,	I <sub>O</sub> = 0, V <sub>I</sub> = V <sub>CC</sub> or GND			1.5	mA
ΔI <sub>CC</sub> <sup>(2)</sup>	Control input	V <sub>CC</sub> = 5.5 V,	One input at 3.4 V, Other inputs at V <sub>CC</sub> or GND			2.5	mA
C <sub>i</sub>	Control input	V <sub>I</sub> = 3 V or 0				2	pF
C <sub>i(OFF)</sub>		V <sub>O</sub> = 3 V or 0,	$\overline{OE}$ = V <sub>CC</sub>			3.5	pF
r <sub>on</sub> <sup>(3)</sup>		V <sub>CC</sub> = 4.5 V	V <sub>I</sub> = 0	I <sub>I</sub> = 64 mA	5	7	Ω
				I <sub>I</sub> = 30 mA	5	7	
			V <sub>I</sub> = 2.4 V,	I <sub>I</sub> = 15 mA	35	50	

- (1) All typical values are at V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C.
- (2) This is the increase in supply current for each input that is at the specified TTL voltage level, rather than V<sub>CC</sub> or GND.
- (3) Measured by the voltage drop between the A and the B terminals at the indicated current through the switch. On-state resistance is determined by the lower voltage of the two (A or B) terminals.

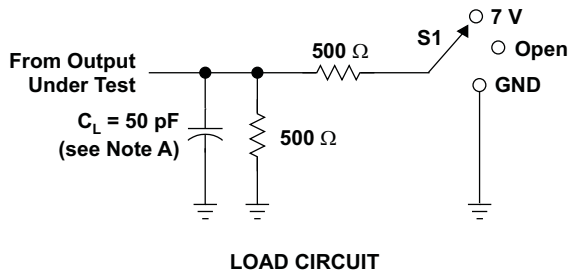
## Switching Characteristics

over recommended operating free-air temperature range,  $C_L = 50$  pF (unless otherwise noted) (see [Figure 1](#))

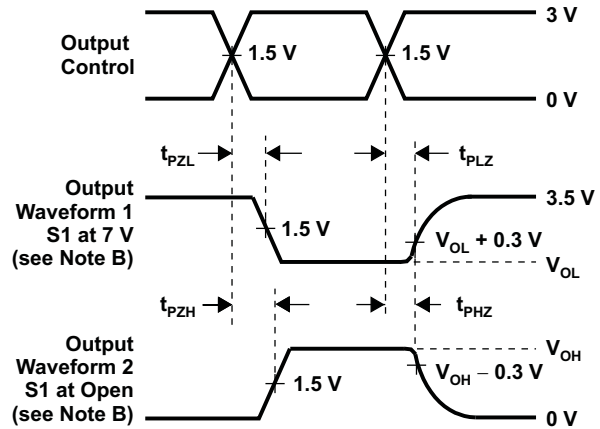
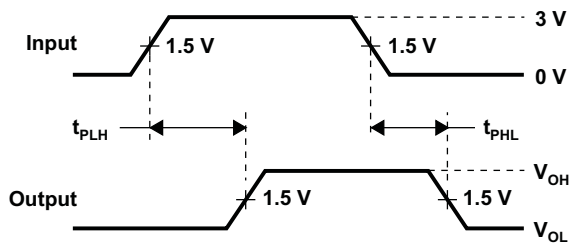
PARAMETER	FROM (INPUT)	TO (OUTPUT)	MIN MAX		UNIT
$t_{pd}^{(1)}$	A or B	B or A		0.25	ns
$t_{en}$	$\overline{OE}$	A or B	2	5.9	ns
$t_{dis}$	$\overline{OE}$	A or B	1	4.7	ns

- (1) The propagation delay is the calculated RC time constant of the typical on-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).

**PARAMETER MEASUREMENT INFORMATION**



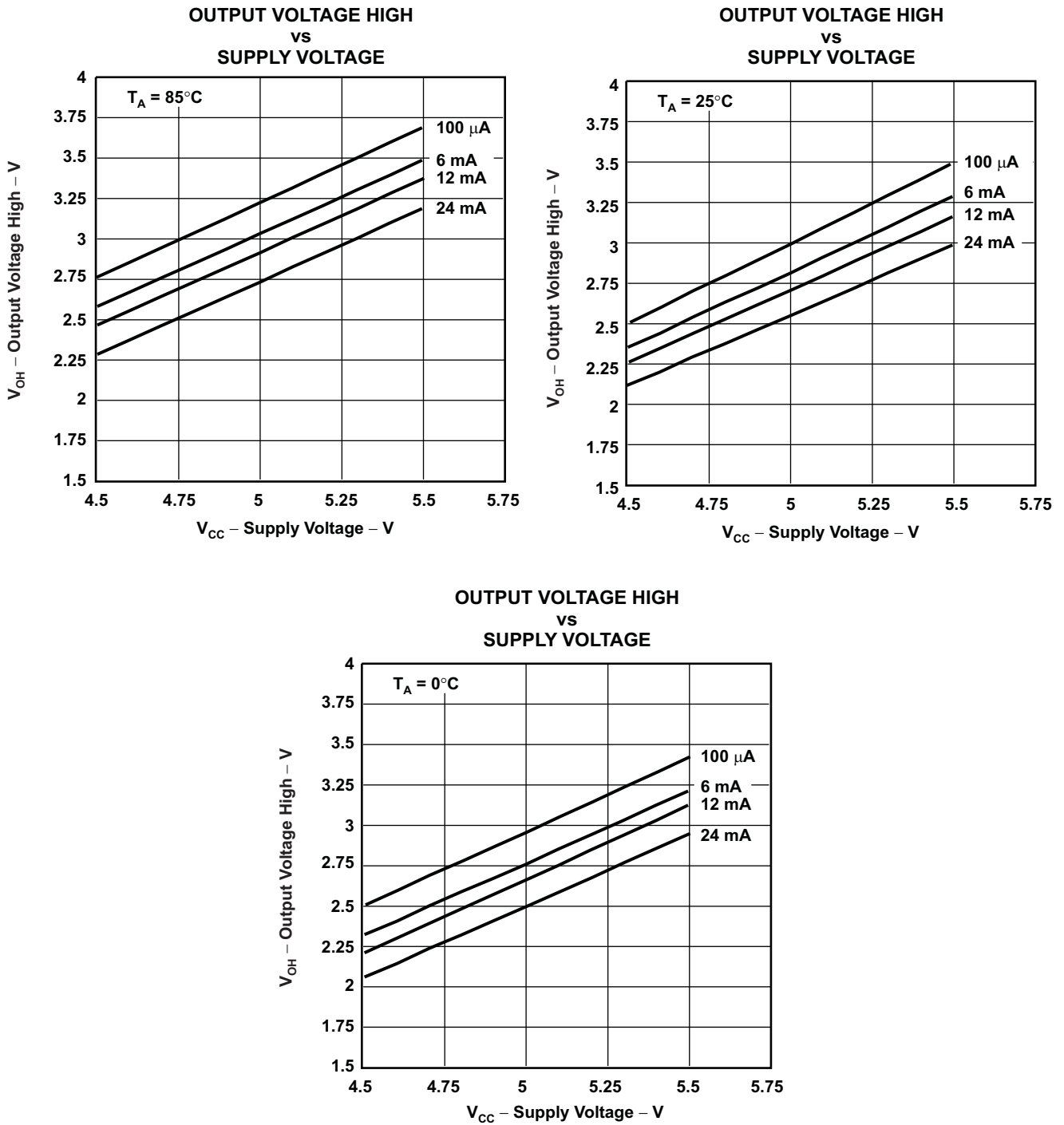
TEST	S1
$t_{pd}$	Open
$t_{PLZ}/t_{PZL}$	7 V
$t_{PHZ}/t_{PZH}$	Open



- NOTES: A.  $C_L$  includes probe and jig capacitance.  
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.  
C. All input pulses are supplied by generators having the following characteristics: PRR  $\leq$  10 MHz,  $Z_O = 50 \Omega$ ,  $t_r \leq 2.5$  ns,  $t_f \leq 2.5$  ns.  
D. The outputs are measured one at a time with one transition per measurement.  
E.  $t_{PLZ}$  and  $t_{PHZ}$  are the same as  $t_{dis}$ .  
F.  $t_{PZL}$  and  $t_{PZH}$  are the same as  $t_{en}$ .  
G.  $t_{PLH}$  and  $t_{PHL}$  are the same as  $t_{pd}$ .

**Figure 1. Load Circuit and Voltage Waveforms**

**TYPICAL CHARACTERISTICS**



**Figure 2.  $V_{OH}$  Values**

**PACKAGING INFORMATION**

Orderable part number	Status (1)	Material type (2)	Package   Pins	Package qty   Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
<a href="#">74CBTD1G125DCKRG4</a>	Active	Production	SC70 (DCK)   5	3000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	PMR
74CBTD1G125DCKRG4.A	Active	Production	SC70 (DCK)   5	3000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	PMR
<a href="#">SN74CBTD1G125DBVR</a>	Active	Production	SOT-23 (DBV)   5	3000   LARGE T&R	Yes	NIPDAU   SN	Level-1-260C-UNLIM	-40 to 85	(P25J, P25R)
SN74CBTD1G125DBVR.A	Active	Production	SOT-23 (DBV)   5	3000   LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	(P25J, P25R)
<a href="#">SN74CBTD1G125DBVT</a>	NRND	Production	SOT-23 (DBV)   5	250   SMALL T&R	Yes	NIPDAU   SN	Level-1-260C-UNLIM	-40 to 85	(P25J, P25R)
SN74CBTD1G125DBVT.A	NRND	Production	SOT-23 (DBV)   5	250   SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	(P25J, P25R)
<a href="#">SN74CBTD1G125DCKR</a>	NRND	Production	SC70 (DCK)   5	3000   LARGE T&R	Yes	NIPDAU   SN	Level-1-260C-UNLIM	-40 to 85	(PMJ, PMR)
SN74CBTD1G125DCKR.A	NRND	Production	SC70 (DCK)   5	3000   LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	(PMJ, PMR)
<a href="#">SN74CBTD1G125DCKT</a>	NRND	Production	SC70 (DCK)   5	250   SMALL T&R	Yes	NIPDAU   SN	Level-1-260C-UNLIM	-40 to 85	(PMJ, PMR)
SN74CBTD1G125DCKT.A	NRND	Production	SC70 (DCK)   5	250   SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	(PMJ, PMR)

(1) **Status:** For more details on status, see our [product life cycle](#).

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
74CBTD1G125DCKRG4	SC70	DCK	5	3000	180.0	8.4	2.47	2.3	1.25	4.0	8.0	Q3
SN74CBTD1G125DBVR	SOT-23	DBV	5	3000	178.0	9.0	3.3	3.2	1.4	4.0	8.0	Q3
SN74CBTD1G125DBVR	SOT-23	DBV	5	3000	180.0	8.4	3.23	3.17	1.37	4.0	8.0	Q3
SN74CBTD1G125DBVT	SOT-23	DBV	5	250	180.0	8.4	3.23	3.17	1.37	4.0	8.0	Q3
SN74CBTD1G125DBVT	SOT-23	DBV	5	250	178.0	9.0	3.3	3.2	1.4	4.0	8.0	Q3
SN74CBTD1G125DCKR	SC70	DCK	5	3000	180.0	8.4	2.47	2.3	1.25	4.0	8.0	Q3
SN74CBTD1G125DCKR	SC70	DCK	5	3000	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
SN74CBTD1G125DCKT	SC70	DCK	5	250	180.0	8.4	2.47	2.3	1.25	4.0	8.0	Q3
SN74CBTD1G125DCKT	SC70	DCK	5	250	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
74CBTD1G125DCKRG4	SC70	DCK	5	3000	202.0	201.0	28.0
SN74CBTD1G125DBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
SN74CBTD1G125DBVR	SOT-23	DBV	5	3000	202.0	201.0	28.0
SN74CBTD1G125DBVT	SOT-23	DBV	5	250	202.0	201.0	28.0
SN74CBTD1G125DBVT	SOT-23	DBV	5	250	180.0	180.0	18.0
SN74CBTD1G125DCKR	SC70	DCK	5	3000	202.0	201.0	28.0
SN74CBTD1G125DCKR	SC70	DCK	5	3000	180.0	180.0	18.0
SN74CBTD1G125DCKT	SC70	DCK	5	250	202.0	201.0	28.0
SN74CBTD1G125DCKT	SC70	DCK	5	250	180.0	180.0	18.0

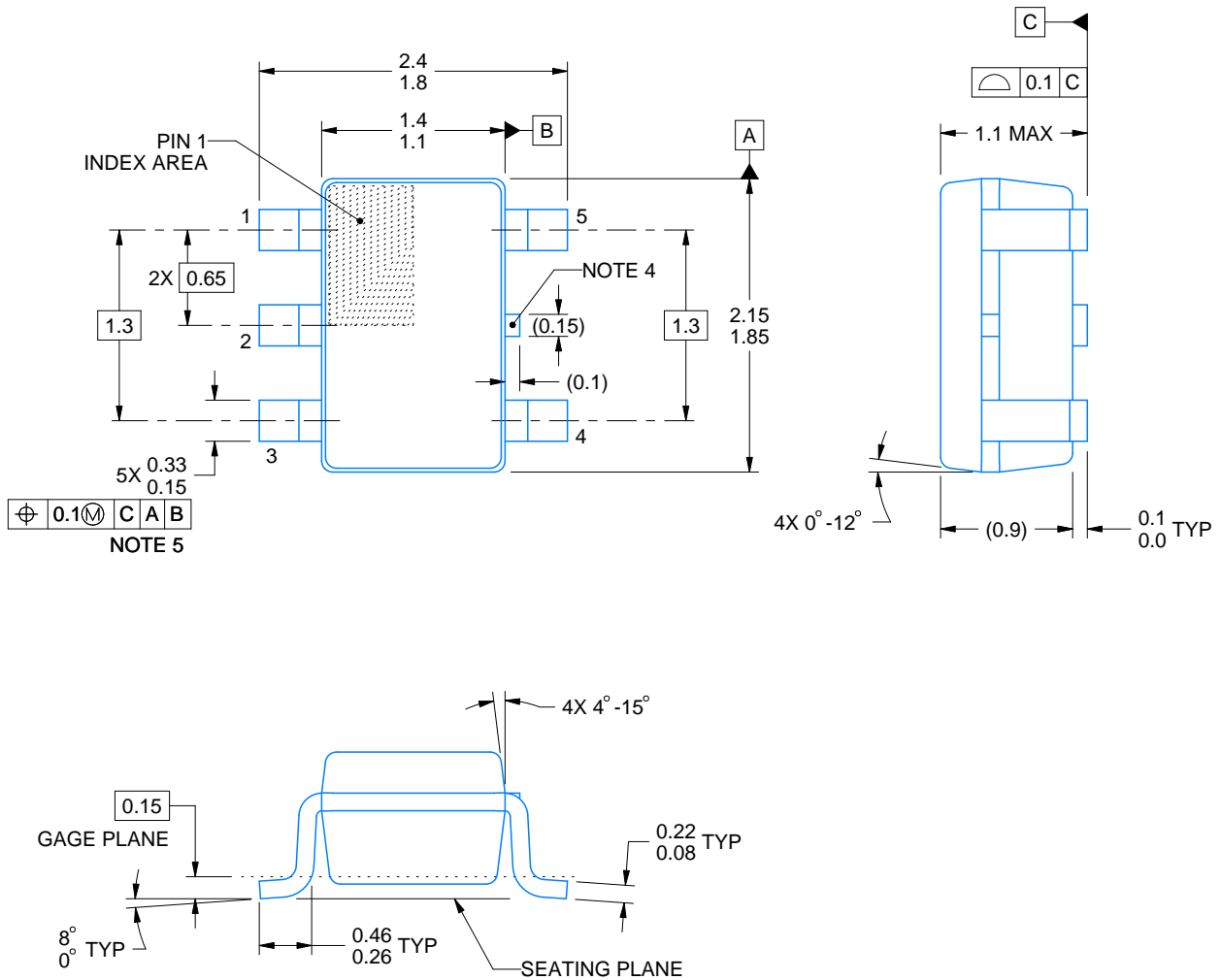
# DCK0005A



# PACKAGE OUTLINE

SOT - 1.1 max height

SMALL OUTLINE TRANSISTOR



4214834/G 11/2024

## NOTES:

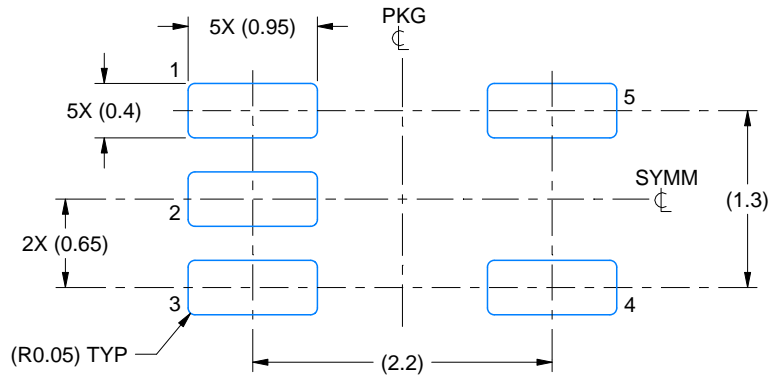
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC MO-203.
4. Support pin may differ or may not be present.
5. Lead width does not comply with JEDEC.
6. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25mm per side

# EXAMPLE BOARD LAYOUT

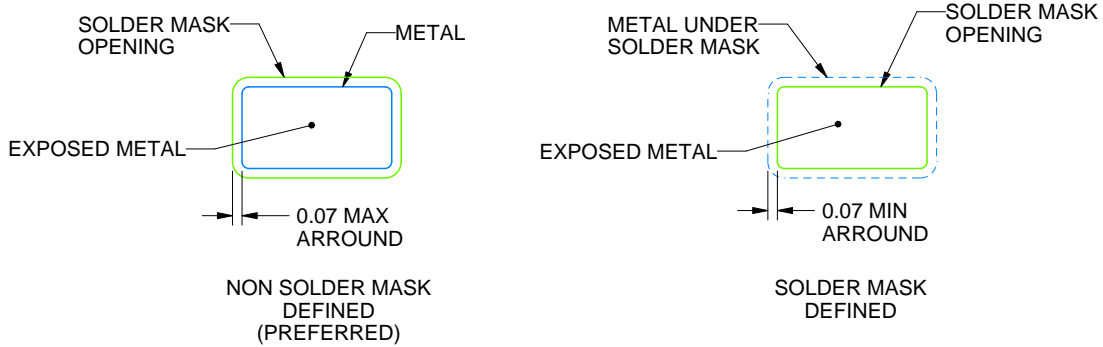
DCK0005A

SOT - 1.1 max height

SMALL OUTLINE TRANSISTOR



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE:18X



SOLDER MASK DETAILS

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NOTES: (continued)

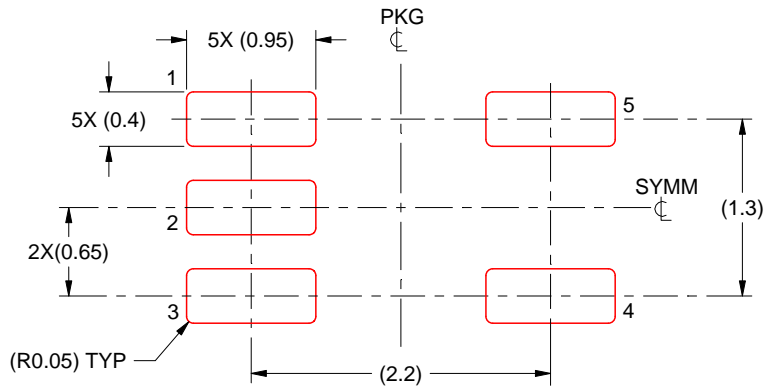
- 7. Publication IPC-7351 may have alternate designs.
- 8. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

DCK0005A

SOT - 1.1 max height

SMALL OUTLINE TRANSISTOR



SOLDER PASTE EXAMPLE  
BASED ON 0.125 THICK STENCIL  
SCALE: 18X

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NOTES: (continued)

9. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
10. Board assembly site may have different recommendations for stencil design.

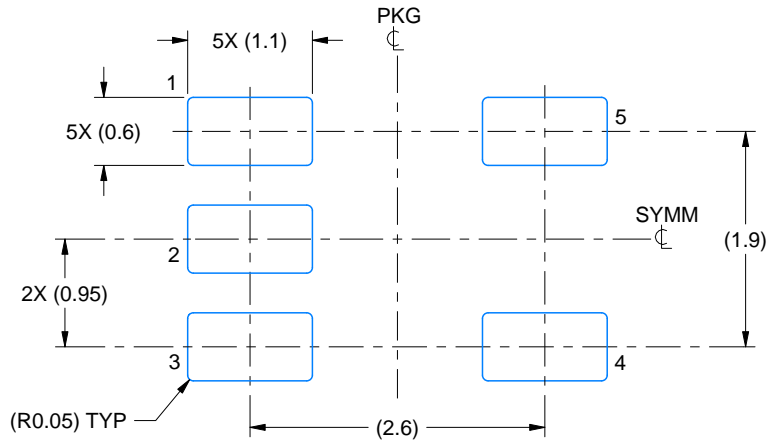


# EXAMPLE BOARD LAYOUT

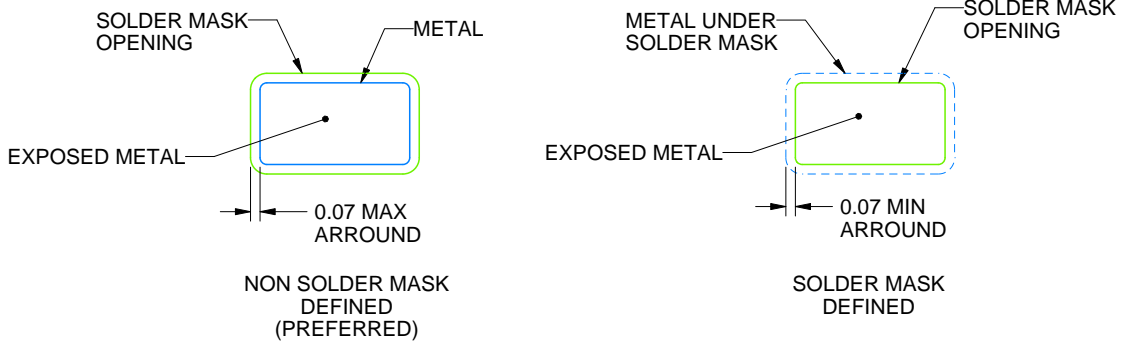
DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE:15X



SOLDER MASK DETAILS

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NOTES: (continued)

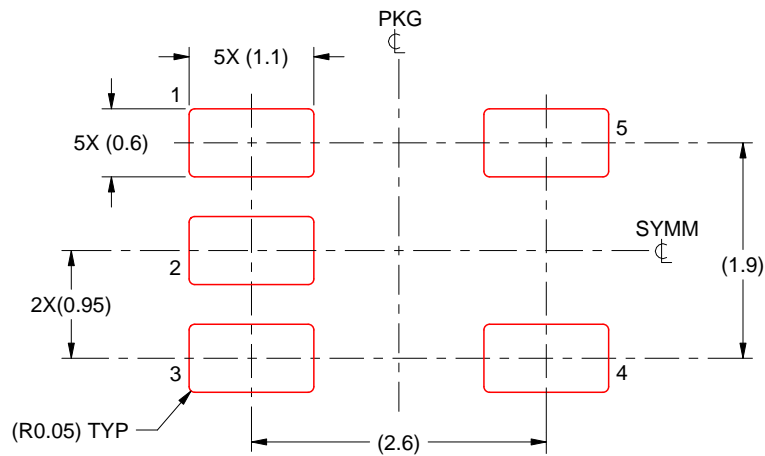
- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:15X

4214839/K 08/2024

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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