SN74LV139A 双路 2 线至 4 线解码器/解复用器

1 特性

- 2V 至 5.5V V_{CC} 运行
- 5V 时，t_{pd} 最大值为 7.5ns
- 所有端口上均支持混合模式电压运行
- 专门为高速存储器解码器和数据传输系统设计
- 包含两个使能输入以简化级联和/或数据接收
- I_{off} 支持局部省电模式运行
- 闩锁性能超过 250mA，符合 JESD 17 规范

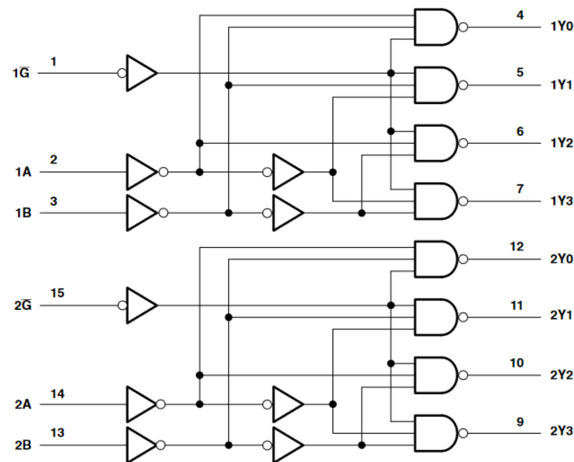
2 说明

SN74LV139A 器件是旨在于 2V 至 5.5V V_{CC} 下运行的双通道 2 线至 4 线解码器/多路信号分离器。

封装信息

器件型号	封装[1]	封装尺寸[2]	本体尺寸[3]
SN74LV139A	D（SOIC，16）	9.90mm × 6mm	9.90mm × 3.91mm
	DB（SSOP，16）	6.20mm × 7.8mm	6.20mm × 5.30mm
	DGV（TVSOP，16）	3.6mm × 6.4mm	3.6mm × 4.4mm
	PW（TSSOP，16）	5.00mm × 6.4mm	5.00mm × 4.40mm
	NS（SOP，16）	10.2mm x 7.8mm	10.20mm x 5.30mm
	RGY（VQFN，16）	4.00mm × 3.50mm	4.00mm × 3.50mm

(1) 如需了解更多信息，请参阅机械、封装和可订购信息。
(2) 封装尺寸（长 × 宽）为标称值，并包括引脚（如适用）。
(3) 本体尺寸（长 × 宽）为标称值，不包括引脚。



逻辑图（正逻辑）

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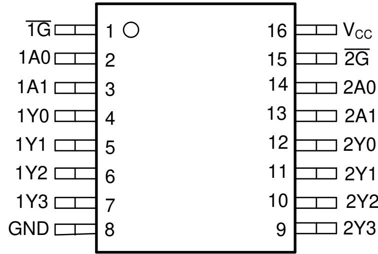
3 引脚配置和功能



SN74LV139A D、DB、DGV、NS 或 PW 封装；16 引脚 SOIC、SSOP、TVSOP、SOP 或 TSSOP（顶视图）

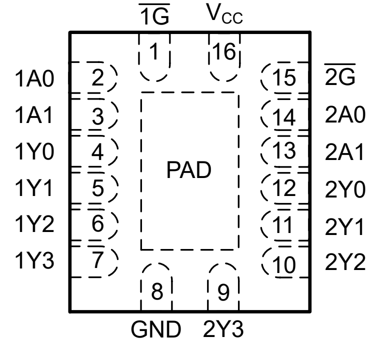


图 **3-1. SN74LV139A RGY 封装，16 引脚 VQFN**

表 **3-1.** 引脚功能

引脚		I/O	说明
编号	名称		
1	$\overline{1G}$	I	通道 1，输出使能，低电平有效
2	$1A_0$	I	通道 1，地址选择 0
3	$1A_1$	I	通道 1，地址选择 1
4	$1Y_0$	O	通道 1，输出 0
5	$1Y_1$	O	通道 1，输出 1
6	$1Y_2$	O	通道 1，输出 2
7	$1Y_3$	O	通道 1，输出 3
8	GND	—	接地
9	$2Y_3$	O	通道 2，输出 3
10	$2Y_2$	O	通道 2，输出 2
11	$2Y_1$	O	通道 2，输出 1
12	$2Y_0$	O	通道 2，输出 0
13	$2A_1$	I	通道 2，地址选择 1
14	$2A_0$	I	通道 2，地址选择 0
15	$\overline{2G}_0$	I	通道 2，输出使能，低电平有效
16	V_{CC}	—	正电源

4 规格

4.1 绝对最大额定值

在自然通风条件下的工作温度范围内测得（除非另有说明）(1)

			最小值	最大值	单位
V_{CC}	电源电压范围		-0.5	7	V
V_I (2)	输入电压范围		-0.5	7	V
V_O (2)	在高阻抗或断电状态对任一输出施加的电压范围		-0.5	7	V
V_O (2) (3)	输出电压范围		-0.5	V_{CC} + 0.5	V
I_{IK}	输入钳位电流	V_I < 0		-20	mA
I_{OK}	输出钳位电流	V_O < 0		-50	mA
I_O	持续输出电流	V_O = 0 至 V_{CC}		±25	mA
	通过 V_{CC} 或 GND 的持续电流			±50	mA
T_{stg}	贮存温度范围		-65	150	°C

(1) 超出“最大绝对额定值”下列出的值可能会对器件造成永久损坏。这些仅为在额定值下的工作情况，对于额定值下或者在超出“推荐的操作条件”下的任何其它情况下的器件功能性操作，在此并未说明。长时间处于绝对最大额定条件下可能会影响器件的可靠性。
(2) 如果遵守输入和输出电流额定值，则可能会超过输入和输出负电压额定值。
(3) 该值被限制为最大 5.5V。

4.2 ESD 等级

			值	单位
$V_{(ESD)}$	静电放电	人体放电模型 (HBM)，符合 ANSI/ESDA/JEDEC JS-001 标准(1)	±2000	V
		充电器件模型 (CDM)，符合 JEDEC 规范 JESD22-C101(2)	±1000	

(1) JEDEC 文档 JEP155 指出：500V HBM 时能够在标准 ESD 控制流程下安全生产。
(2) JEDEC 文档 JEP157 指出：250V CDM 时能够在标准 ESD 控制流程下安全生产。

4.3 建议运行条件

在自然通风条件下的工作温度范围内测得（除非另有说明）(1)

			SN74LV138A		单位
			最小值	最大值	
V_{CC}	电源电压		2	5.5	V
V_{IH}	高电平输入电压	V_{CC} = 2V	1.5		V
		V_{CC} = 2.3V 至 2.7V	V_{CC} × 0.7		
		V_{CC} = 3V 至 3.6V	V_{CC} × 0.7		
		V_{CC} = 4.5V 至 5.5V	V_{CC} × 0.7		
V_{IL}	低电平输入电压	V_{CC} = 2V		0.5	V
		V_{CC} = 2.3V 至 2.7V		V_{CC} × 0.3	
		V_{CC} = 3V 至 3.6V		V_{CC} × 0.3	
		V_{CC} = 4.5V 至 5.5V		V_{CC} × 0.3	
V_I	输入电压		0	5.5	V
V_O	输出电压		0	V_{CC}	V
I_{OH}	高电平输出电流	V_{CC} = 2V		-50	μA
		V_{CC} = 2.3V 至 2.7V		-2	mA
		V_{CC} = 3V 至 3.6V		-6	
		V_{CC} = 4.5V 至 5.5V		-12	

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在自然通风条件下的工作温度范围内测得（除非另有说明）[(1)]

			SN74LV138A		单位
			最小值	最大值	
I_{OL}	低电平输出电流	V_{CC} = 2V		50	μA
		V_{CC} = 2.3V 至 2.7V		2	mA
		V_{CC} = 3V 至 3.6V		6	
		V_{CC} = 4.5V 至 5.5V		12	
Δt/Δv	输入转换上升或下降速率	V_{CC} = 2.3V 至 2.7V		200	ns/V
		V_{CC} = 3V 至 3.6V		100	
		V_{CC} = 4.5V 至 5.5V		20	
T_A	自然通风条件下的工作温度范围		-40	85	°C

(1) 器件所有的未使用输入必须保持在 V_{CC} 或 GND 以确保器件正常运行。请参阅 TI 应用报告 *CMOS 输入缓慢变化或悬空的影响*，文献编号 SCBA004。

4.4 热性能信息

热指标[(1)]		SN74LV139A						单位
		D (SOIC)	DB (SSOP)	DGV (TVSOP)	NS (SOP)	PW (TSSOP)	RGY (VQFN)	
		16 引脚						
$R_{\theta JA}$	结至环境热阻	73	82	120	64	108	39	°C/W

(1) 有关新旧热指标的更多信息，请参阅 *IC 封装热指标* 应用报告 (SPRA953)。

4.5 电气特性

在自然通风条件下的建议运行温度范围内测得（除非另有说明）

参数		测试条件		V_{CC}	SN74LV139A			单位
					最小值	典型值	最大值	
V_{OH}	高电平输出电压	I_{OH} = –50μA		2V 至 5.5V	V_{CC} – 0.1			V
		I_{OH} = -2mA		2.3V	2			
		I_{OH} = -6mA		3V	2.48			
		I_{OH} = -12mA		4.5V	3.8			
V_{OL}	低电平输出电压	I_{OL} = 50μA		2V 至 5.5V			0.1	V
		I_{OL} = 2mA		2.3V			0.4	
		I_{OL} = 6mA		3V			0.44	
		I_{OL} = 12mA		4.5V			0.55	
I_I	输入电流	V_I = 5.5V 或 GND		0V 至 5.5V			±1	μA
I_{CC}	电源电流	V_I = V_{CC} 或 GND，	I_O = 0	5.5V			20	μA
I_{off}	输入/输出断电漏电流	V_I 或 V_O = 0V 至 5.5V		0			5	μA
C_i	输入电容	V_I = V_{CC} 或 GND		3.3V		1.9		pF

4.6 开关特性，V_{CC} = 2.5V ± 0.2V

在推荐的自然通风条件下的工作温度范围内测得，V_{CC} = 2.5V ± 0.2V（除非另有说明）（请参阅负载电路和电压波形）

参数	从（输入）	至（输出）	负载电容	T_A = 25°C			SN74LV139A		单位
				最小值	典型值	最大值	最小值	最大值	
t_{pd}	A 或 B	Y	C_L = 15pF		7.7[1]	17.6[1]	1	21	ns
	$\overline{G}$				7.4[1]	15.8[1]	1	19	
t_{pd}	A 或 B	Y	C_L = 50pF		10.2	22.5	1	26.5	ns
	$\overline{G}$				9.9	20.2	1	24	

(1) 对于符合 MIL-PRF-38535 标准的产品，此参数未经量产测试。

4.7 开关特性，V_{CC} = 3.3V ± 0.3V

在推荐的自然通风条件下的工作温度范围内测得，V_{CC} = 3.3V ± 0.3V（除非另有说明）（请参阅负载电路和电压波形）

参数	从（输入）	至（输出）	负载电容	T_A = 25°C			SN74LV139A		单位
				最小值	典型值	最大值	最小值	最大值	
t_{pd}	A 或 B	Y	C_L = 15pF		5.3[1]	11[1]	1	13	ns
	$\overline{G}$				5.1[1]	9.2[1]	1	11	
t_{pd}	A 或 B	Y	C_L = 50pF		7.3	14.5	1	16.5	ns
	$\overline{G}$				7	12.7	1	14.5	

(1) 对于符合 MIL-PRF-38535 标准的产品，此参数未经量产测试。

4.8 开关特性，V_{CC} = 5V ± 0.5V

在自然通风条件下的建议工作温度范围内测得，V_{CC} = 5V ± 0.5V（除非另有说明）（请参阅负载电路和电压波形）

参数	从（输入）	至（输出）	负载电容	T_A = 25°C			SN74LV139A		单位
				最小值	典型值	最大值	最小值	最大值	
t_{pd}	A 或 B	Y	C_L = 15pF		3.7[1]	7.2[1]	1	8.5	ns
	$\overline{G}$				3.5[1]	6.3[1]	1	7.5	
t_{pd}	A 或 B	Y	C_L = 50pF		5.2	9.2	1	10.5	ns
	$\overline{G}$				4.9	8.3	1	9.5	

(1) 对于符合 MIL-PRF-38535 标准的产品，此参数未经量产测试。

4.9 工作特性

T_A = 25°C

参数		测试条件	V_{CC}	典型值	单位
C_{pd}	功率耗散电容	C_L = 50pF， f = 10MHz	3.3V	17.3	pF
			5V	18.2	

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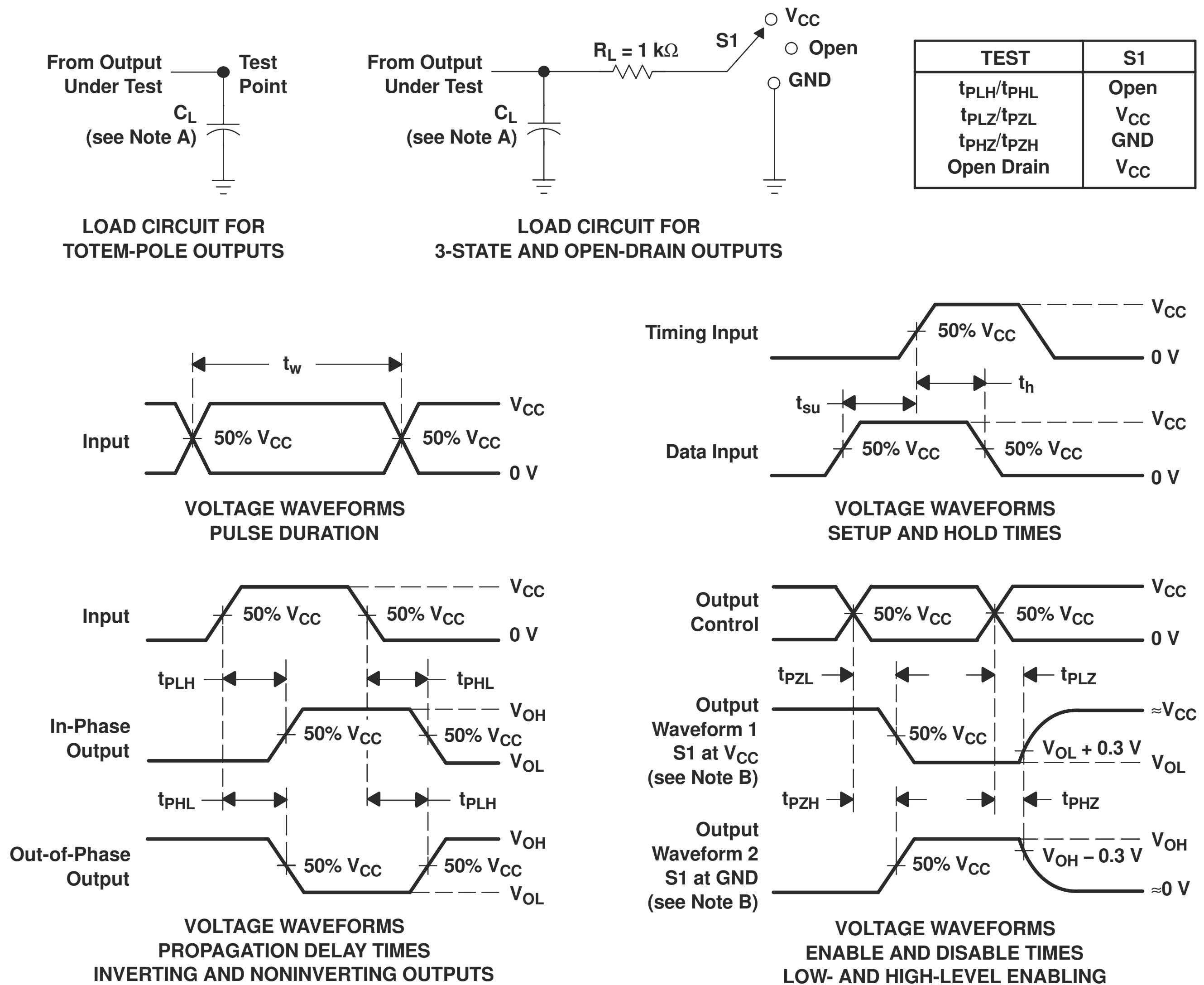
5 参数测量信息



NOTES:
A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r ≤ 3 ns, t_f ≤ 3 ns.
D. The outputs are measured one at a time, with one input transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
F. t_{PZL} and t_{PZH} are the same as t_{en}.
G. t_{PHL} and t_{PLH} are the same as t_{pd}.
H. All parameters and waveforms are not applicable to all devices.

图 **5-1.** 负载电路和电压波形

6 详细说明

6.1 概述

SNx4LV139A 器件是旨在于 2V 至 5.5V V_{CC} 下运行的 3 线至 8 线解码器/多路解复用器。

这些器件设计用于需要极短传播延迟时间的高性能存储器解码或数据路由应用。在高性能存储器系统中，可使用此类解码器来尽可能地消除系统解码的影响。与使用高速使能电路的高速存储器一同使用时，这些解码器的延迟时间和存储器的使能时间通常小于存储器的典型存取时间。这意味着解码器引起的有效系统延迟可以忽略不计。

LV139A 器件在单个封装中包含两个独立的 2 线至 4 线解码器。低电平有效使能 ($\overline{G}$) 输入可在多路信号分离应用中用作数据线路。这些解码器/多路信号分离器具有全缓冲输入，每个输入只代表其驱动电路的一个标准化负载。

这些器件专用于使用 I_{off} 的局部断电应用。I_{off} 电路会禁用输出，从而在器件断电时防止电流回流损坏器件。

6.2 功能方框图

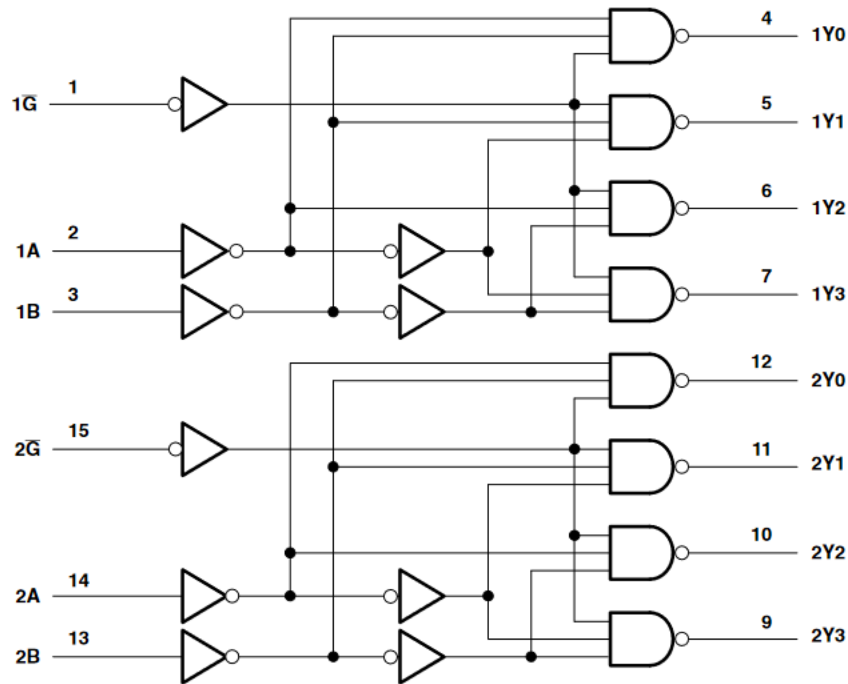


图 6-1. 逻辑图（正逻辑）

6.3 器件功能模式

功能表

输入			输出			
$\overline{G}$	选择					
	B	A	Y0	Y1	Y2	Y3
H	X	X	H	H	H	H
L	L	L	L	H	H	H
L	L	H	H	L	H	H
L	H	L	H	H	L	H
L	H	H	H	H	H	L

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7 应用和实施

备注

以下应用部分中的信息不属于 TI 器件规格的范围，TI 不担保其准确性和完整性。TI 的客 户应负责确定器件是否适用于其应用。客户应验证并测试其设计，以确保系统功能。

7.1 电源相关建议

电源可以是*建议运行条件* 中最小和最大电源电压额定值之间的任何电压。每个 V_{CC} 端子均应具有一个良好的旁路电容器，以防止功率干扰。建议为该器件使用 0.1µF 电容器。可以并联多个旁路电容器以抑制不同的噪声频率。0.1µF 和 1µF 电容器通常并联使用。为了获得最佳效果，旁路电容器必须尽可能靠近电源端子安装。

7.2 布局

7.2.1 布局指南

- 旁路电容器的放置
  - 靠近器件的正电源端子放置
  - 提供电气短接地返回路径
  - 使用宽布线以最大限度减小阻抗
  - 尽可能将器件、电容器和布线保持在电路板的同一面
- 信号布线几何形状
  - 8mil 至 12mil 布线宽度
  - 布线长度小于 12cm 可最大限度减轻传输线路影响
  - 避免信号布线出现 90° 角
  - 在信号布线下方使用不间断的接地平面
  - 通过接地对信号布线周围的区域进行泛洪填充
  - 对于长度超过 12cm 的布线
    - 使用阻抗受控的布线
    - 在输出端附近使用串联阻尼电阻进行源端接
    - 避免分支；对必须单独分支的信号进行缓冲

7.2.2 布局示例

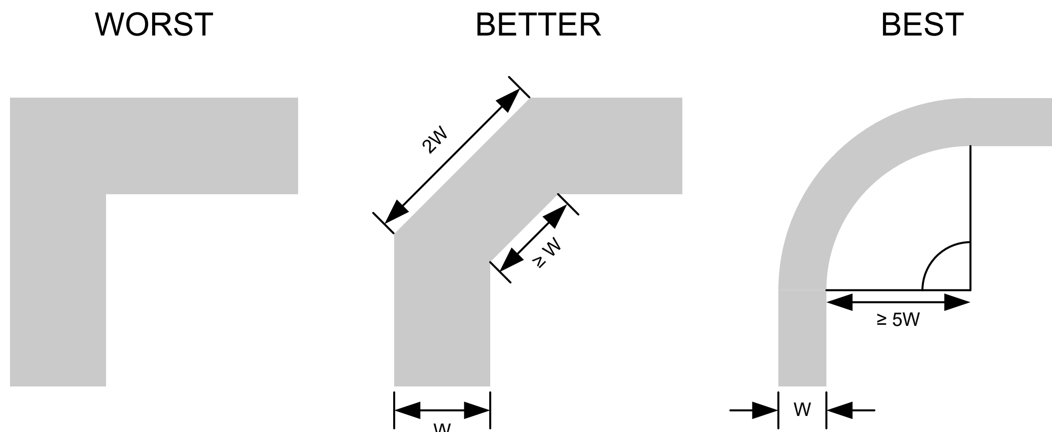

图 **7-1.** 可改善信号完整性的布线转角示例

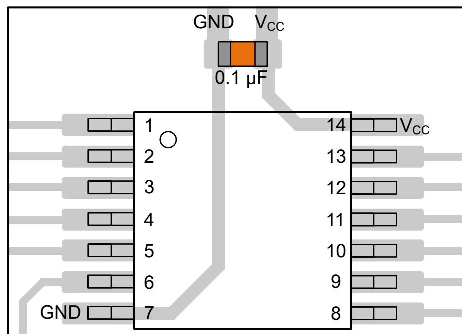

图 **7-2. TSSOP** 和类似封装的旁路电容器放置示例

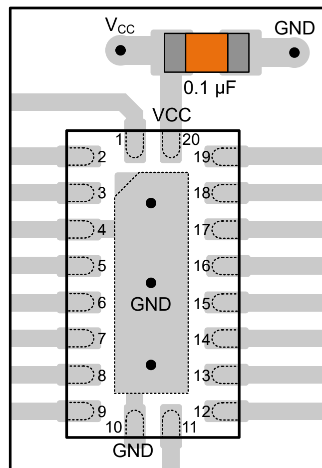

图 **7-3. WQFN** 和类似封装的旁路电容器放置示例

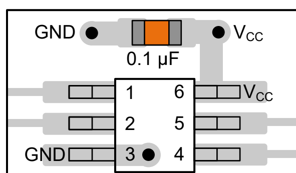

图 **7-4. SOT**、**SC70** 和类似封装的旁路电容器放置示例

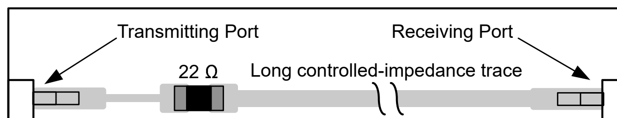

图 **7-5.** 可改善信号完整性的阻尼电阻放置示例

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8 器件和文档支持

TI 提供大量的开发工具。下面列出了用于评估器件性能、生成代码和开发解决方案的工具和软件。

8.1 文档支持

8.1.1 相关文档

请参阅如下相关文档：

- 德州仪器 (TI)，*CMOS 功耗与 C_{pd} 计算* 应用报告
- 德州仪器 (TI)，*使用逻辑器件进行设计* 应用报告
- 德州仪器 (TI)，*标准线性和逻辑 (SLL) 封装和器件的热特性* 应用报告

8.2 接收文档更新通知

要接收文档更新通知，请导航至 ti.com 上的器件产品文件夹。点击*通知* 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

8.3 支持资源

TI E2E™ 中文支持论坛是工程师的重要参考资料，可直接从专家处获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题，获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的使用条款。

8.4 商标

TI E2E™ is a trademark of Texas Instruments.
所有商标均为其各自所有者的财产。

8.5 静电放电警告

静电放电 (ESD) 会损坏这个集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

8.6 术语表

TI 术语表　　本术语表列出并解释了术语、首字母缩略词和定义。

9 修订历史记录

Changes from Revision I (April 2005) to Revision J (December 2024) — **Page**

- 添加了*封装信息* 表、*引脚功能* 表、*ESD 等级* 表、*热性能信息* 表、*器件功能模式*、“应用和实施”部分、*器件和文档支持* 部分以及*机械、封装和可订购信息* 部分 1
- 删除了对机器放电模型的引用 4

10 机械、封装和可订购信息

以下页面包含机械、封装和可订购信息。这些信息是指定器件可用的最新数据。数据如有变更，恕不另行通知，且不会对此文档进行修订。有关此数据表的浏览器版本，请查阅左侧的导航栏。

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74LV139AD	OBSOLETE	SOIC	D	16		TBD	Call TI	Call TI	-40 to 85	LV139A	
SN74LV139ADBR	ACTIVE	SSOP	DB	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LV139A	Samples
SN74LV139ADR	ACTIVE	SOIC	D	16	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LV139A	Samples
SN74LV139ANSR	ACTIVE	SOP	NS	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	74LV139A	Samples
SN74LV139ANSRE4	ACTIVE	SOP	NS	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	74LV139A	Samples
SN74LV139APW	OBSOLETE	TSSOP	PW	16		TBD	Call TI	Call TI	-40 to 85	LV139A	
SN74LV139APWR	ACTIVE	TSSOP	PW	16	2000	RoHS & Green	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 85	LV139A	Samples
SN74LV139APWRG4	ACTIVE	TSSOP	PW	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LV139A	Samples
SN74LV139ARGYR	ACTIVE	VQFN	RGY	16	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	LV139A	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

[6] Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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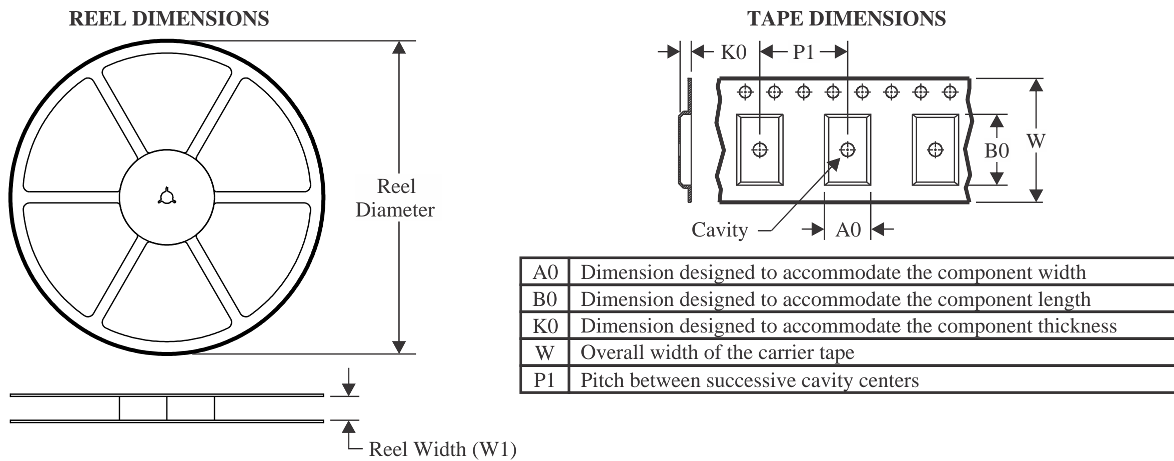
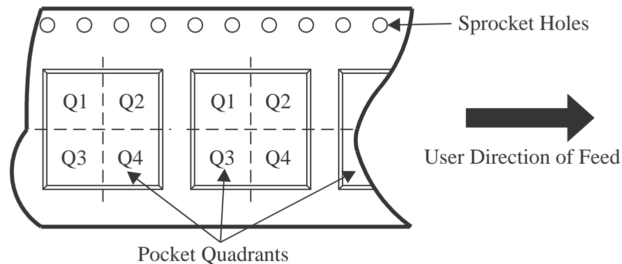
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

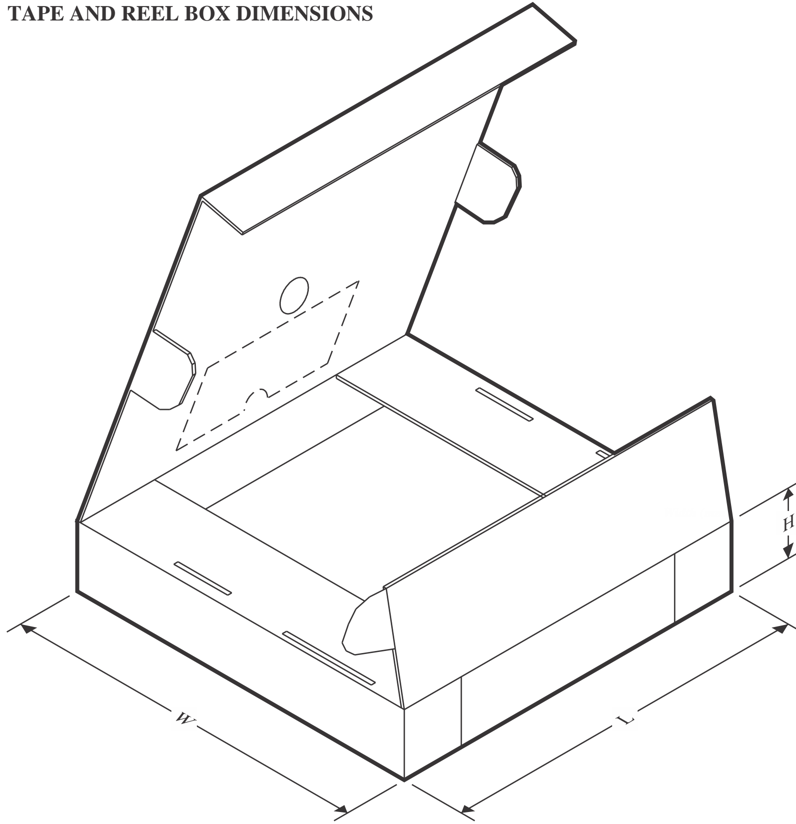




*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LV139ADBR	SSOP	DB	16	2000	330.0	16.4	8.35	6.6	2.4	12.0	16.0	Q1
SN74LV139ADR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
SN74LV139ANSR	SOP	NS	16	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1
SN74LV139APWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74LV139APWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74LV139APWRG4	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74LV139APWRG4	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74LV139ARGYR	VQFN	RGY	16	3000	330.0	12.4	3.8	4.3	1.5	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



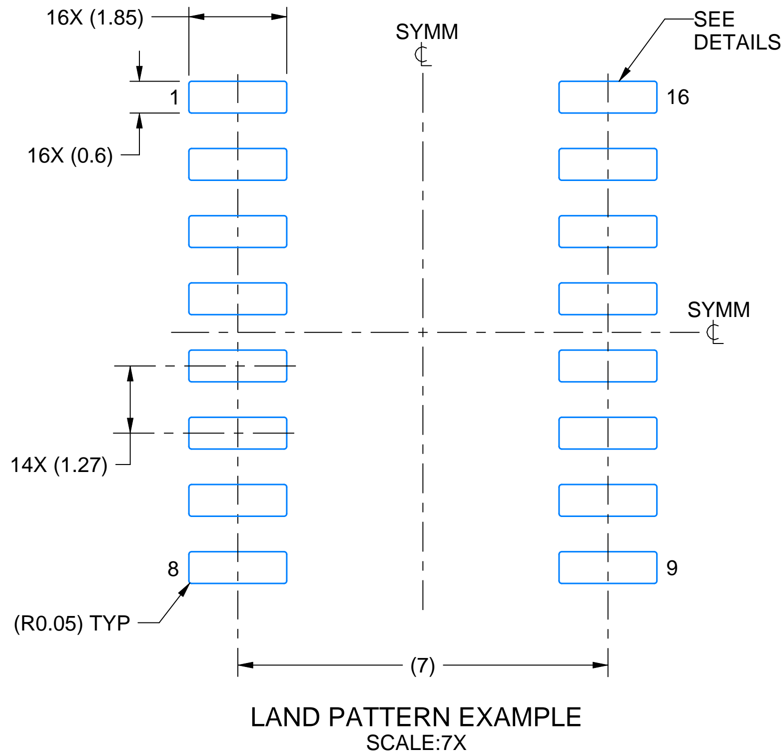
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LV139ADBR	SSOP	DB	16	2000	356.0	356.0	35.0
SN74LV139ADR	SOIC	D	16	2500	340.5	336.1	32.0
SN74LV139ANSR	SOP	NS	16	2000	356.0	356.0	35.0
SN74LV139APWR	TSSOP	PW	16	2000	356.0	356.0	35.0
SN74LV139APWR	TSSOP	PW	16	2000	356.0	356.0	35.0
SN74LV139APWRG4	TSSOP	PW	16	2000	356.0	356.0	35.0
SN74LV139APWRG4	TSSOP	PW	16	2000	356.0	356.0	35.0
SN74LV139ARGYR	VQFN	RGY	16	3000	356.0	356.0	35.0

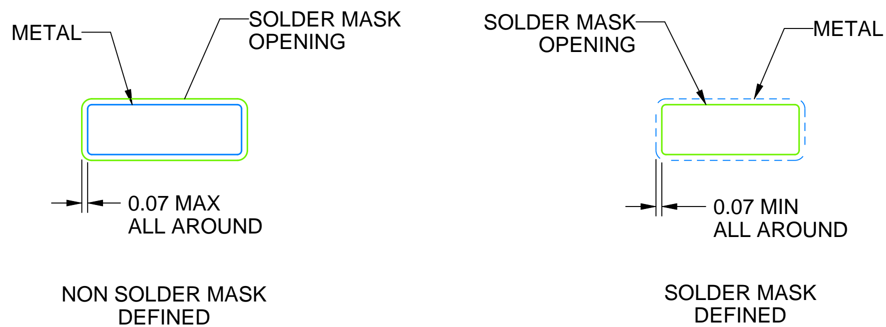
4220735/A 12/2021

NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.



LAND PATTERN EXAMPLE
SCALE:7X



NON SOLDER MASK DEFINED

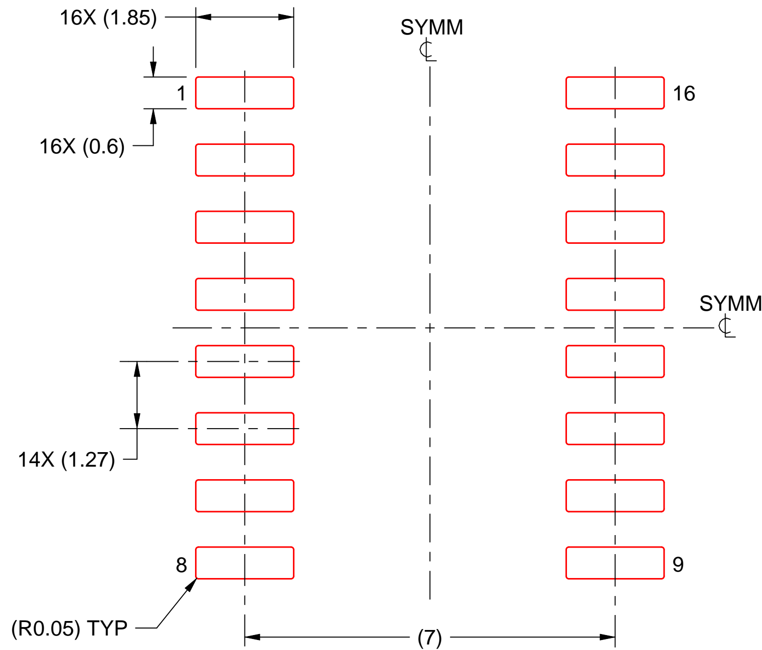
SOLDER MASK DEFINED

SOLDER MASK DETAILS

4220735/A 12/2021

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



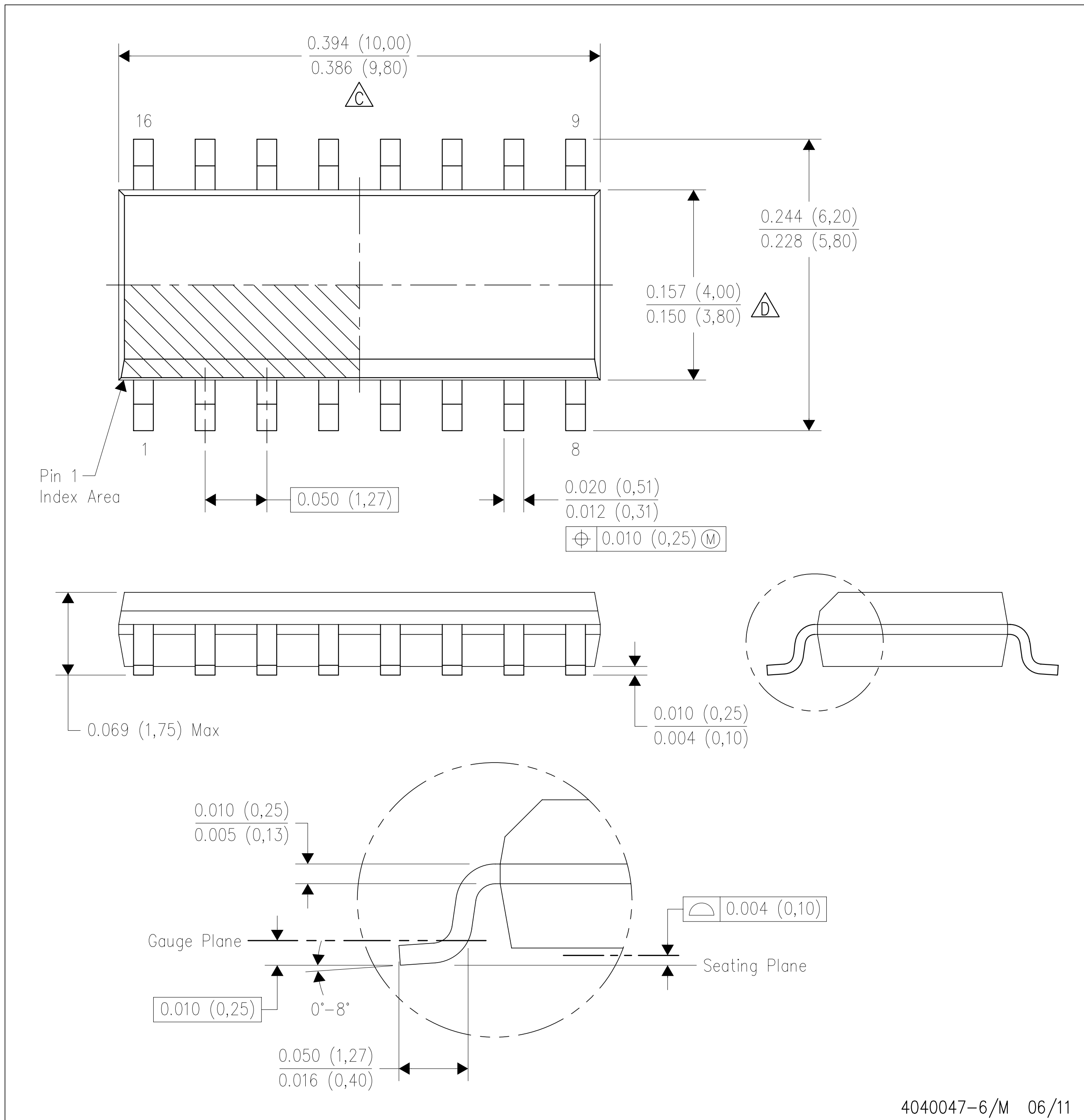
SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:7X

4220735/A 12/2021

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

D (R–PDSO–G16) PLASTIC SMALL OUTLINE

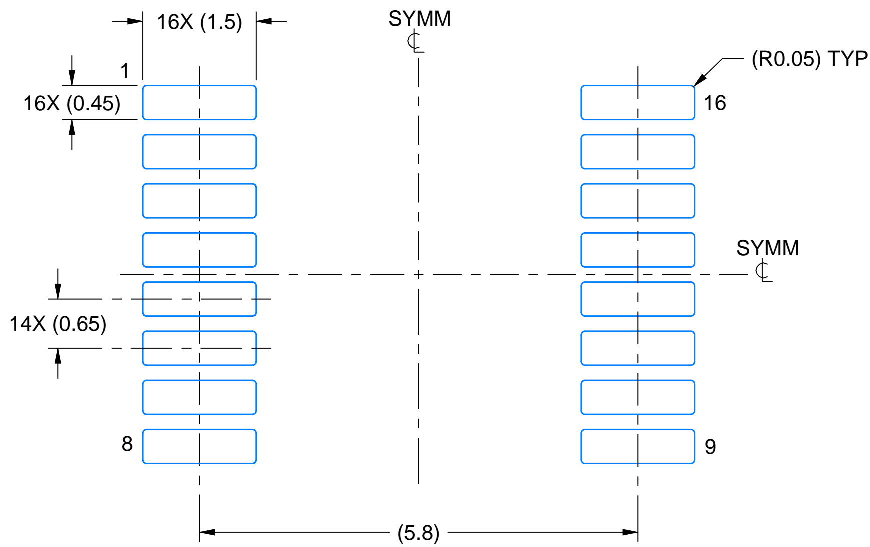


NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS-012 variation AC.

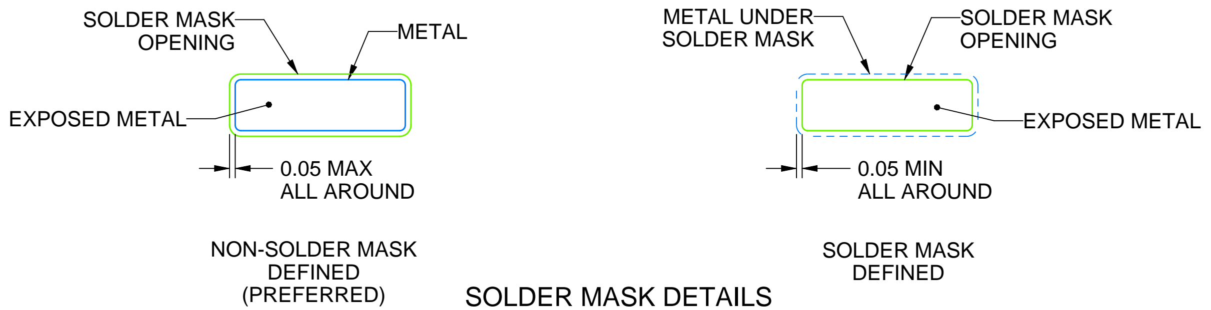
4220204/A 02/2017

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

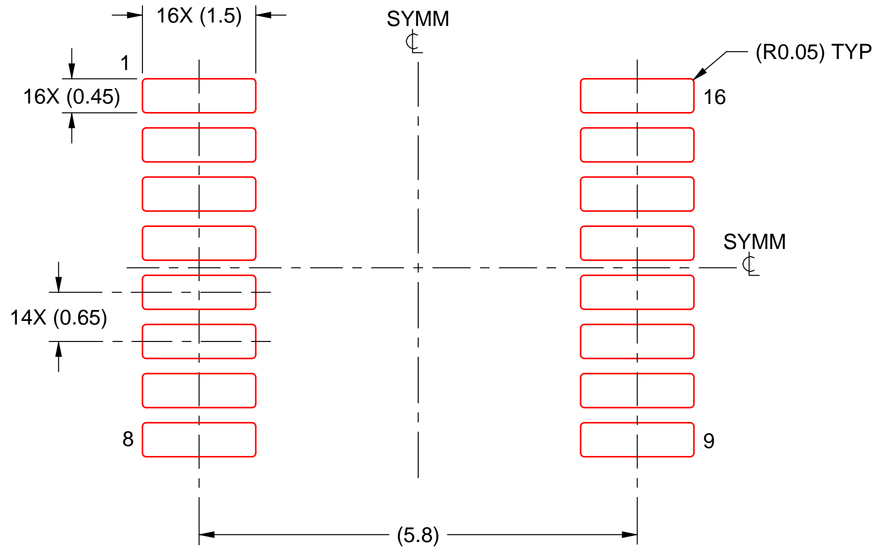


SOLDER MASK DETAILS

4220204/A 02/2017

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220204/A 02/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

C
0.1 C
SEATING PLANE
8.2
7.4 TYP
A
PIN 1 INDEX AREA
14X 0.65
16
1
2X
4.55
6.5
5.9
NOTE 3
8
9
16X 0.38
0.22
B
5.6
5.0
NOTE 4
0.1 Ⓜ C A B

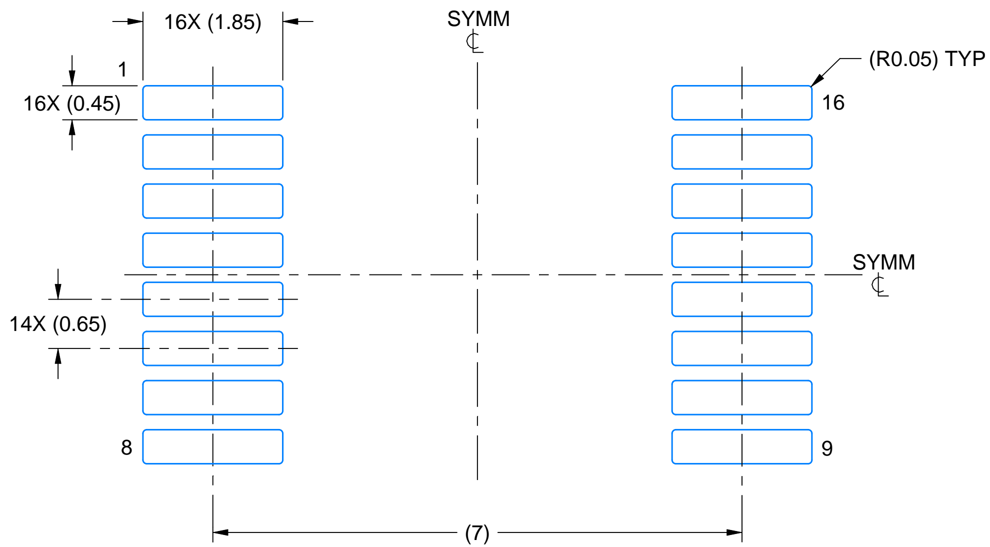
0.25
0.09
SEE DETAIL A
2 MAX
0.25
GAGE PLANE
0° -8°
0.95
0.55
0.05 MIN

DETAIL A
TYPICAL

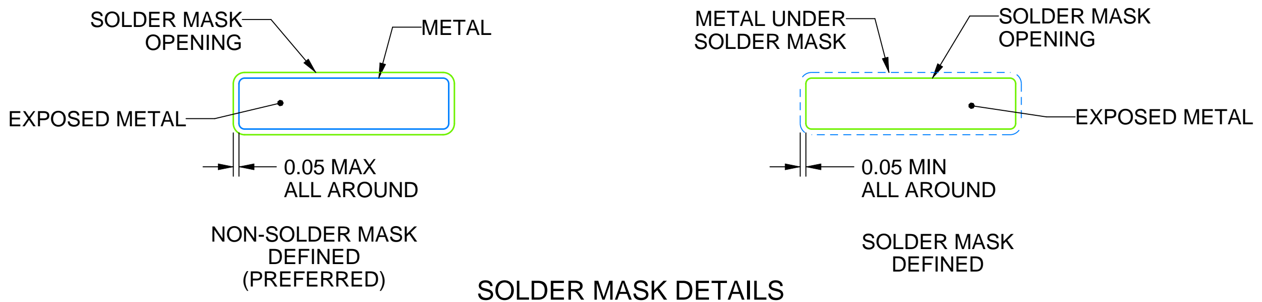
4220763/A 05/2022

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-150.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



NON-SOLDER MASK
DEFINED
(PREFERRED)

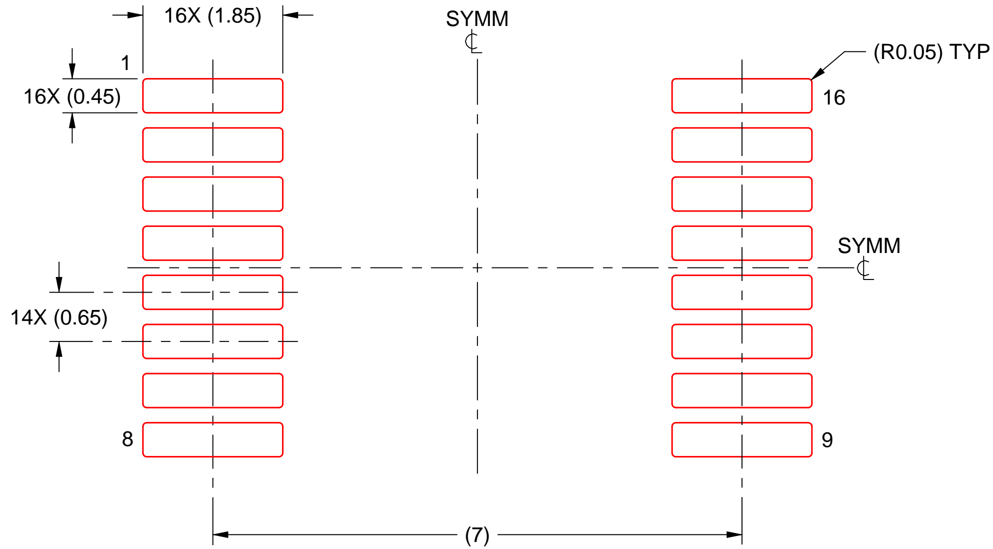
SOLDER MASK
DEFINED

SOLDER MASK DETAILS

4220763/A 05/2022

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220763/A 05/2022

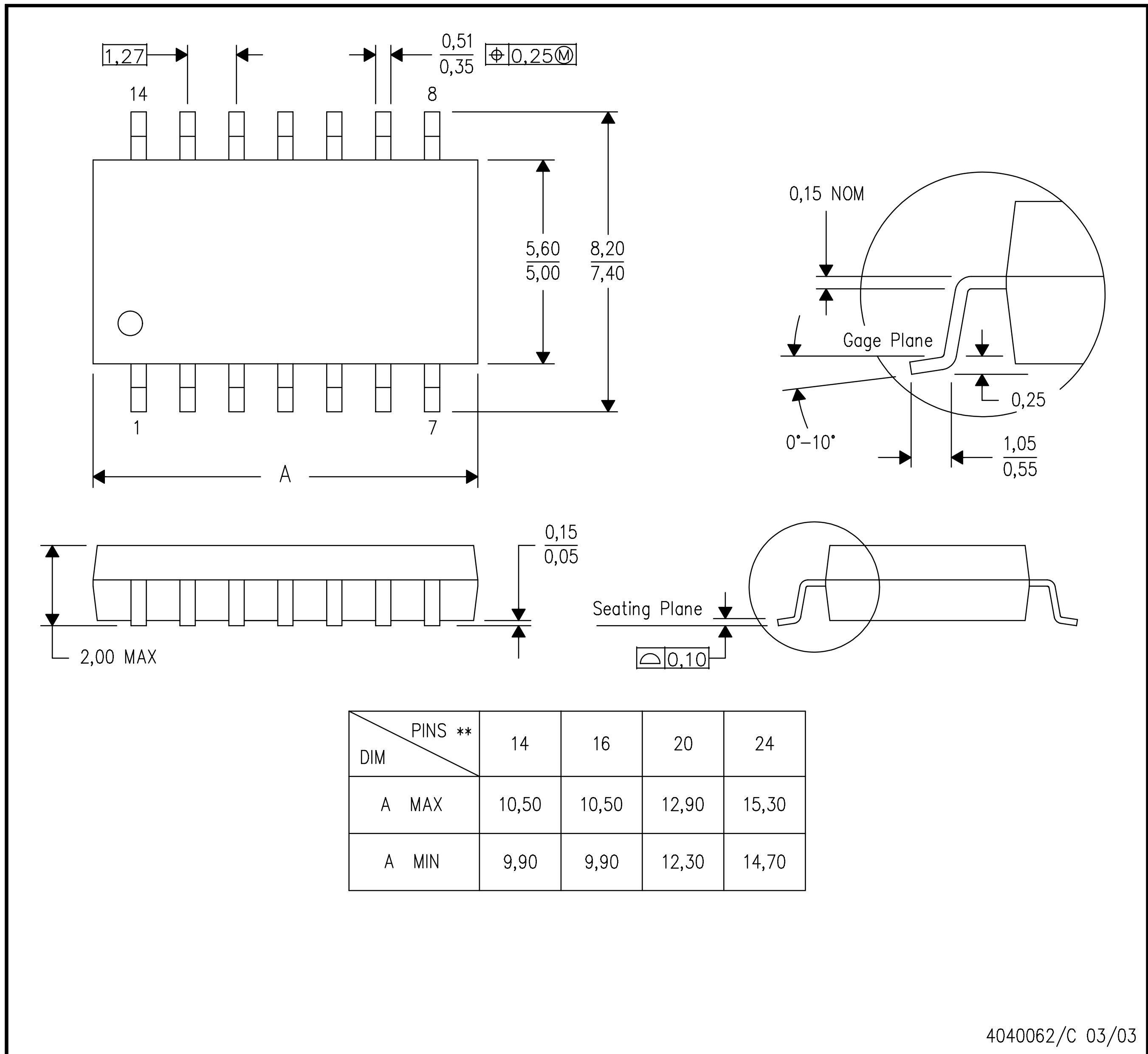
NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

MECHANICAL DATA

NS (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

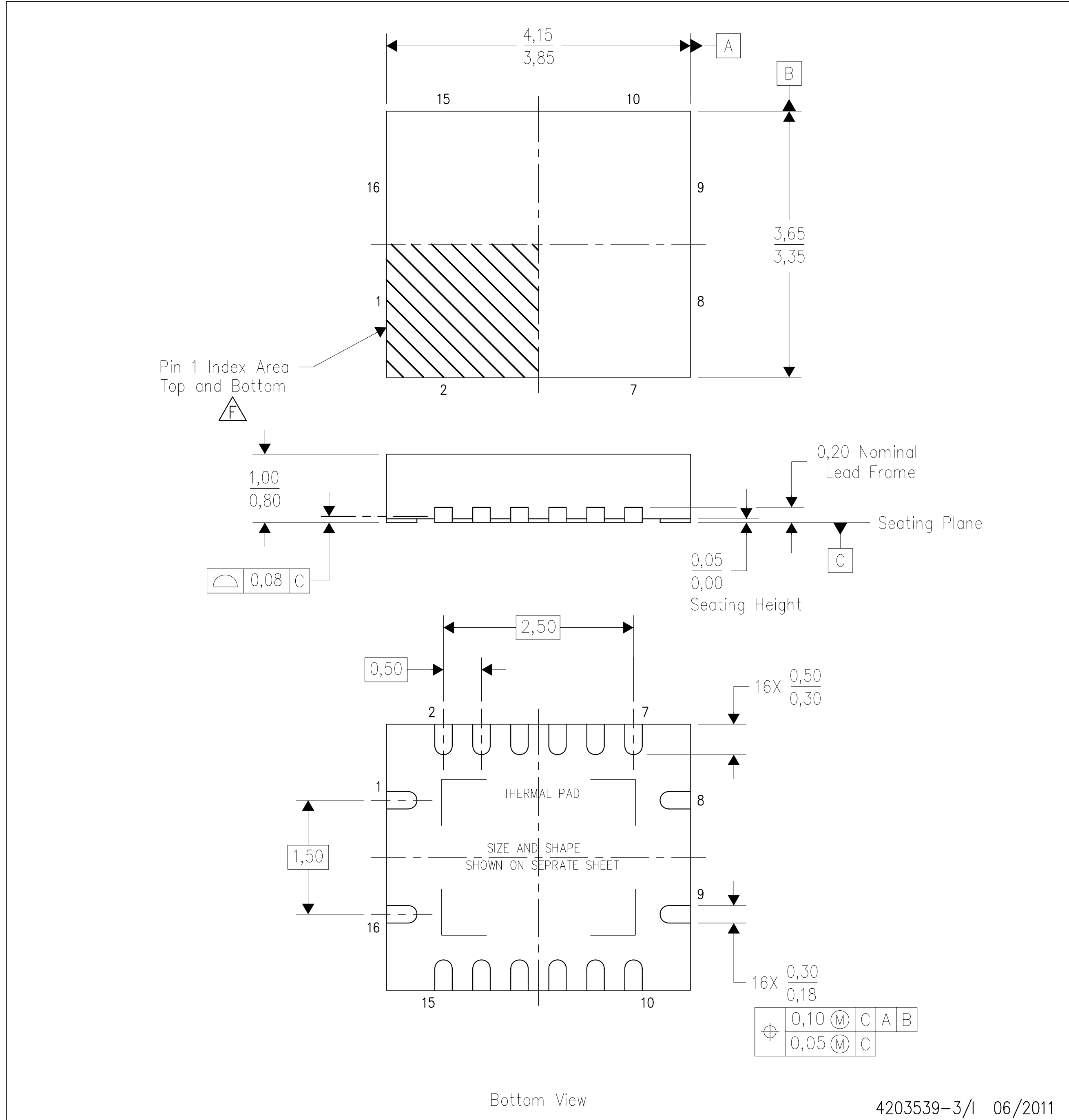
14-PINS SHOWN



DIM \ PINS **	14	16	20	24
A MAX	10,50	10,50	12,90	15,30
A MIN	9,90	9,90	12,30	14,70

NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

RGY (R-PVQFN-N16) PLASTIC QUAD FLATPACK NO-LEAD



NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
- B. This drawing is subject to change without notice.
- C. QFN (Quad Flatpack No-Lead) package configuration.
- D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
- E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
- F. Pin 1 identifiers are located on both top and bottom of the package and within the zone indicated. The Pin 1 identifiers are either a molded, marked, or metal feature.
- G. Package complies to JEDEC MO-241 variation BA.

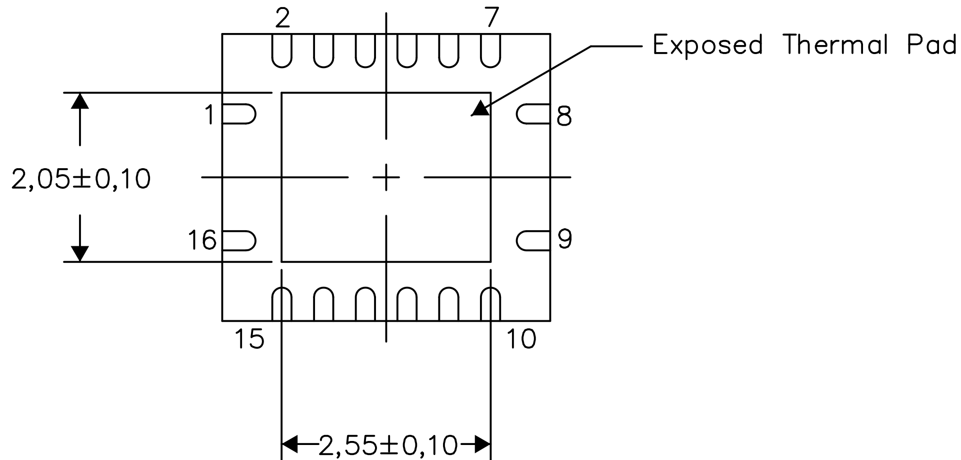
RGY (R–PVQFN–N16) PLASTIC QUAD FLATPACK NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.

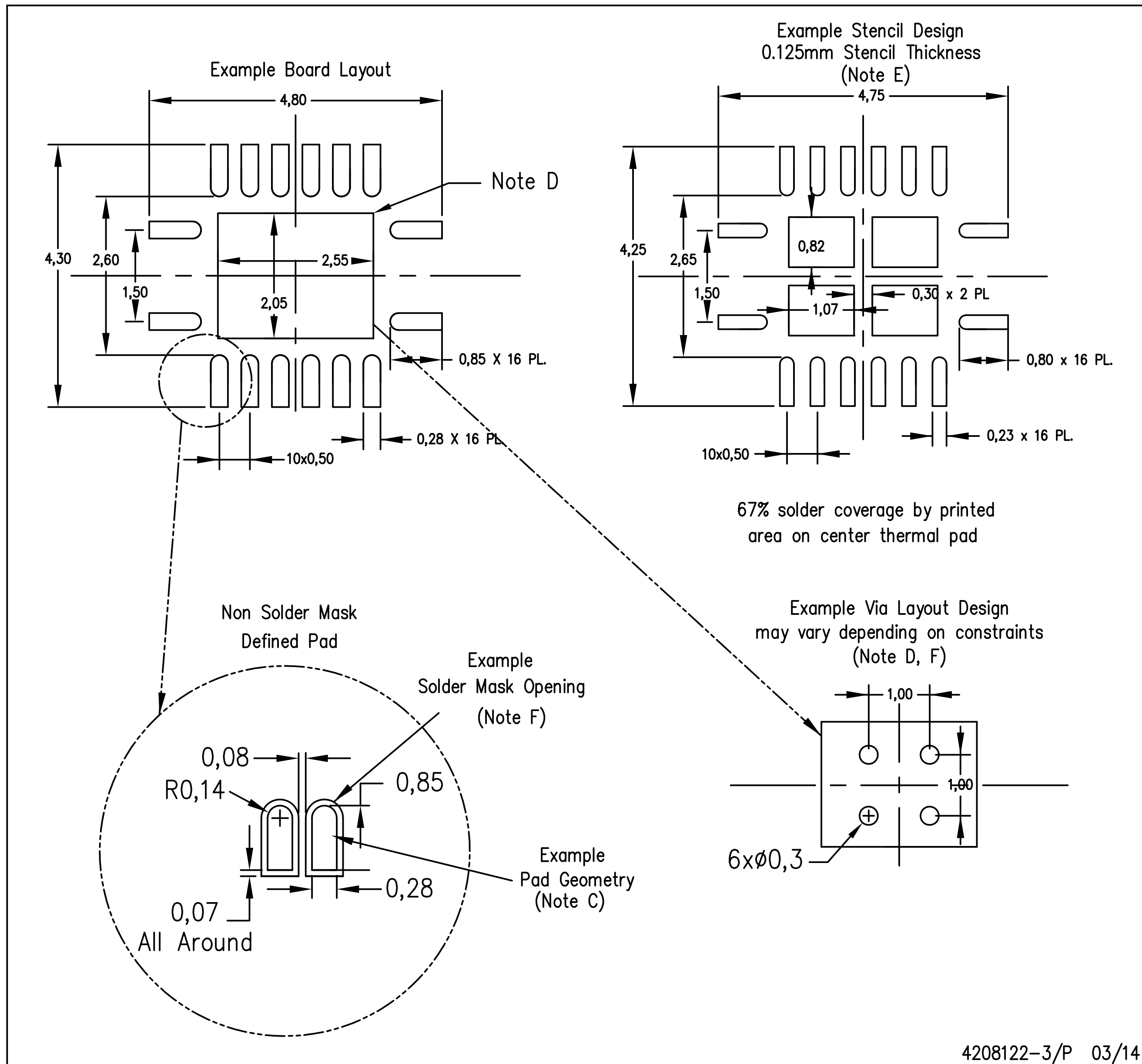


Bottom View

Exposed Thermal Pad Dimensions

4206353-3/P 03/14

NOTE: All linear dimensions are in millimeters



NOTES:

A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC-7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat-Pack QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.

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