# SN74LV166A 8 位并联负载移位寄存器

## 1 特性

- 工作范围为 2V 至 5.5V $V_{CC}$
- 电压为 5V 时，$t_{pd}$ 最大值为 10.5ns
- $V_{CC}$ = 3.3V、$T_A$ = 25°C 时，$V_{OLP}$（输出接地反弹）典型值小于 0.8V
- $V_{CC}$ = 3.3V、$T_A$ = 25°C 时，$V_{OHV}$（输出 $V_{OH}$ 下冲）典型值为 2.3V
- $I_{off}$ 支持局部断电模式运行
- 同步负载
- 直接覆盖清零
- 并行转串行转换
- 闩锁性能超过 100mA，符合 JESD 78 II 类规范

## 2 应用

- 输入扩展
- 8 位数据存储

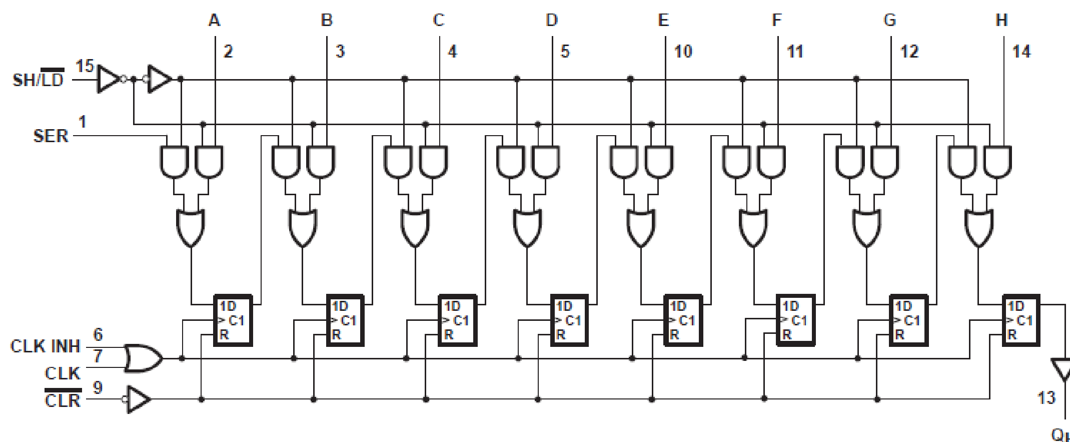
## 3 说明

'LV166A 器件是 8 位并行负载移位寄存器，旨在于 2V 至 5.5V $V_{CC}$ 下运行。

封装信息

| 器件型号 | 封装[1] | 封装尺寸（标称值） |
|---|---|---|
| SN74LV166A | D（SOIC，16） | 9.90mm × 3.90mm |
| | DB（SSOP，16） | 6.20mm × 5.30mm |
| | NS（SOP，16） | 10.3mm × 5.30mm |
| | PW（TSSOP，16） | 5.00mm × 4.40mm |
| | DGV（TVSOP，16） | 3.6mm × 4.4mm |

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。




功能方框图

本文档旨在为方便起见，提供有关 TI 产品中文版本的信息，以确认产品的概要。有关适用的官方英文版本的最新信息，请访问 www.ti.com，其内容始终优先。TI 不保证翻译的准确性和有效性。在实际设计之前，请务必参考最新版本的英文版本。
English Data Sheet: SCLS456

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## 4 Revision History

注：以前版本的页码可能与当前版本的页码不同

**Changes from Revision C (April 2005) to Revision D (March 2023)** **Page**

- 添加了*应用*、*封装信息* 表、*引脚功能* 表、*ESD 等级* 表、*热性能信息* 表、*器件功能模式*、*应用和实施* 部分、*电源相关建议* 部分、*布局* 部分、*器件和文档支持* 部分以及*机械、封装和可订购信息* 部分.......... 1


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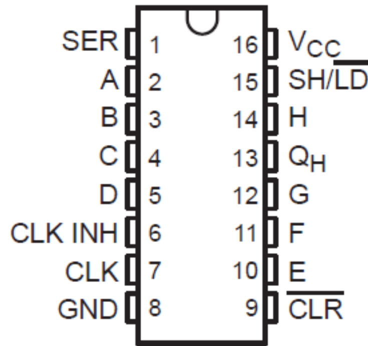
## 5 Pin Configuration and Functions




**D, DB, DGV, NS, or PW Package**
**16-Pin SOP, SOIC, SSOP, TSSOP, TVSOP**
**(Top View)**

**表 5-1. Pin Functions**

| PIN | | I/O | DESCRIPTION |
|---|---|---|---|
| NAME | NO. | | |
| SER | 1 | I | Serial Output |
| A | 2 | I | Parallel Input |
| B | 3 | I | Parallel Input |
| C | 4 | I | Parallel Input |
| D | 5 | I | Parallel Input |
| CLK | 7 | I | Clock input |
| GND | 8 | — | Ground |
| $\overline{CLR}$ | 9 | I | Clear input, active low |
| E | 10 | I | Parallel Input |
| F | 11 | I | Parallel Input |
| G | 12 | I | Parallel Input |
| $Q_H$ | 13 | O | $Q_H$ output |
| H | 14 | I | Parallel input H |
| SH/ $\overline{LD}$ | 15 | I | Shift/ load input, enable shifting when input is high, load data when input is low |
| $V_{CC}$ | 16 | — | Power Pin |

# 6 Specifications

## 6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)[1]

| | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| $V_{CC}$ | Supply voltage range | | –0.5 | 7 | V |
| $V_I$ | Input voltage range[1] | | –0.5 | 7 | |
| $V_O$ | Output voltage range applied in high or low state, [1] [2] | | −0.5 V | $V_{CC}$ + 0.5 V | |
| $V_O$ | Voltage range applied to any output in the power-off state[1] | | –0.5 | 7 | |
| $I_{IK}$ | Input clamp current[2] | $V_I < 0$ | | −20 | mA |
| $I_{OK}$ | Output clamp current[2] | $V_O < 0$ | | −50 | mA |
| $I_O$ | Continuous output current | $V_O = 0$ to $V_{CC}$ | | ±25 | mA |
| | Continuous current through $V_{CC}$ or GND | | | ±50 | mA |
| $T_{stg}$ | Storage temperature | | –65 | 150 | °C |

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under 节 6.3 is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

## 6.2 ESD Ratings

| | | | VALUE | UNIT |
|---|---|---|---|---|
| $V_{(ESD)}$ | Electrostatic discharge | Human-Body Model (A114-A)[1] | ±2000 | V |
| | | Charged-Device Model (C101) | ±1000 | |
| | | Machine Model (A115-A) | ±200 | |

(1) AEC Q100-002 indicate that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

## 6.3 Recommended Operating Conditions

| | | | SN74LV166A | | UNIT |
|---|---|---|---|---|---|
| | | | MIN | MAX | |
| $V_{CC}$ | Supply voltage | | 2 | 5.5 | V |
| $V_{IH}$ | High-level input voltage | $V_{CC}$ = 2 V | 1.5 | | V |
| | | $V_{CC}$ = 2.3 V to 2.7 V | $V_{CC}$ × 0.7 | | |
| | | $V_{CC}$ = 3 V to 3.6 V | $V_{CC}$ × 0.7 | | |
| | | $V_{CC}$ = 4.5 V to 5.5 V | $V_{CC}$ × 0.7 | | |
| $V_{IL}$ | Low-level input voltage | $V_{CC}$ = 2 V | | 0.5 | V |
| | | $V_{CC}$ = 2.3 V to 2.7 V | | $V_{CC}$ × 0.3 | |
| | | $V_{CC}$ = 3 V to 3.6 V | | $V_{CC}$ × 0.3 | |
| | | $V_{CC}$ = 4.5 V to 5.5 V | | $V_{CC}$ × 0.3 | |
| $V_I$ | Input voltage | | 0 | 5.5 | V |
| $V_O$ | Output voltage | | 0 | $V_{CC}$ | V |
| $I_{OH}$ | High-level output current | $V_{CC}$ = 2 V | | – 50 | µA |
| | | $V_{CC}$ = 2.3 V to 2.7 V | | – 2 | mA |
| | | $V_{CC}$ = 3 V to 3.6 V | | – 6 | |
| | | $V_{CC}$ = 4.5 V to 5.5 V | | – 12 | |
| $I_{OL}$ | Low-level output current | $V_{CC}$ = 2 V | | 50 | µA |
| | | $V_{CC}$ = 2.3 V to 2.7 V | | 2 | mA |
| | | $V_{CC}$ = 3 V to 3.6 V | | 6 | |
| | | $V_{CC}$ = 4.5 V to 5.5 V | | 12 | |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## 6.3 Recommended Operating Conditions (continued)

| | | | SN74LV166A | | UNIT |
|---|---|---|---|---|---|
| | | | MIN | MAX | |
| Δt/Δv | Input transition rise or fall rate | $V_{CC}$ = 2.3 V to 2.7 V | | 200 | ns/V |
| | | $V_{CC}$ = 3 V to 3.6 V | | 100 | |
| | | $V_{CC}$ = 4.5 V to 5.5 V | | 20 | |
| $T_A$ | Operating free-air temperature | | −40 | 85 | °C |

## 6.4 Thermal Information

| THERMAL METRIC | | D (SOIC) | DB (SSOP) | DGV (TVSOP) | NS (SO) | PW (TSSOP) | UNIT |
|---|---|---|---|---|---|---|---|
| | | 16 PINS | 16 PINS | 16 PINS | 16 PINS | 16 PINS | |
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance[1] | 73 | 82 | 120 | 64 | 108 | °C/W |

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC package thermal metrics* application report.

## 6.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | $V_{CC}$ | SN74LV166A | | | UNIT |
|---|---|---|---|---|---|---|
| | | | MIN | TYP | MAX | |
| $V_{OH}$ | $I_{OH}$ = −50 µA | 2 V to 5.5 V | $V_{CC}$−0.1 | | | V |
| | $I_{OH}$ = −2 mA | 2.3 V | 2 | | | |
| | $I_{OH}$ = −50 µA | 3 V | 2.48 | | | |
| | $I_{OH}$ = −6 mA | 4.5 V | 3.8 | | | |
| $V_{OL}$ | $I_{OH}$ = −12 mA | 2 V to 5.5 V | | | 0.1 | V |
| | | 2.3 V | | | 0.4 | |
| | | 3 V | | | 0.44 | |
| | $I_{OL}$ = 4 mA | 4.5 V | | | 0.55 | |
| $I_I$ | $V_I$ = $V_{CC}$ or 0 | 0 to 5.5 V | | | ± 1 | µA |
| $I_{CC}$ | $V_I$ = $V_{CC}$ or 0, $I_O$ = 0 | 5.5 V | | | 20 | µA |
| $I_{off}$ | | 0 | | | 5 | µA |
| $C_i$ | | 3.3 V | | 1.6 | | pF |

## 6.6 Timing Requirements, $V_{CC}$ = 2.5 V ± 0.2 V

over recommended operating free-air temperature range, $V_{cc}$ = 2.5 V ± 0.2 V (unless otherwise noted)

| | | | $T_A$ = 25°C | | SN74LV166A | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | |
| $t_w$ | Pulse duration | $\overline{CLR}$ low | 8 | | 9 | | ns |
| | | CLK high or low | 8.5 | | 9 | | |
| $t_{su}$ | Setup time | CLK INH before CLK ↑ | 7 | | 7 | | ns |
| | | Data before CLK ↑ | 6.5 | | 8.5 | | |
| | | SH/$\overline{LD}$ before CLK ↑ | 7 | | 8.5 | | |
| | | SER before CLK ↑ | 8.5 | | 9.5 | | |
| | | $\overline{CLR}$ ↑ inactive before CLK ↑ | 6 | | 7 | | |

### 6.6 Timing Requirements, $V_{CC}$ = 2.5 V ± 0.2 V (continued)

over recommended operating free-air temperature range, $V_{cc}$ = 2.5 V ± 0.2 V (unless otherwise noted)

| | | | $T_A$ = 25°C | | SN74LV166A | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | |
| $t_h$ | Hold time | Data after CLK ↑ | − 0.5 | | 0 | | ns |

### 6.7 Timing Requirements, $V_{CC}$ = 3.3 V ± 0.3 V

over recommended operating free-air temperature range, $V_{cc}$ = 3.3 V ± 0.3 V (unless otherwise noted)

| | | | $T_A$ = 25°C | | SN74LV166A | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | |
| $t_w$ | Pulse duration | $\overline{CLR}$ low | 6 | | 7 | | ns |
| | | CLK high or low | 6 | | 7 | | |
| $t_{su}$ | Setup time | CLK INH before CLK ↑ | 5 | | 5 | | ns |
| | | Data before CLK ↑ | 5 | | 6 | | |
| | | SH/$\overline{LD}$ before CLK ↑ | 5 | | 6 | | |
| | | SER before CLK ↑ | 5 | | 6 | | |
| | | $\overline{CLR}$ ↑ inactive before CLK ↑ | 4 | | 4 | | |
| $t_h$ | Hold time | Data after CLK ↑ | 0 | | 0 | | ns |

### 6.8 Timing Requirements, $V_{CC}$ = 5 V ± 0.5 V

over recommended operating free-air temperature range, $V_{cc}$ = 5 V ± 0.5 V (unless otherwise noted)

| | | | $T_A$ = 25°C | | SN74LV166A | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | |
| $t_w$ | Pulse duration | $\overline{CLR}$ low | 5 | | 5 | | ns |
| | | CLK high or low | 4 | | 4 | | |
| $t_{su}$ | Setup time | CLK INH before CLK ↑ | 3.5 | | 3.5 | | ns |
| | | Data before CLK ↑ | 4.5 | | 4.5 | | |
| | | SH/$\overline{LD}$ before CLK ↑ | 4 | | 4 | | |
| | | SER before CLK ↑ | 4 | | 4 | | |
| | | $\overline{CLR}$ ↑ inactive before CLK ↑ | 3.5 | | 3.5 | | |
| $t_h$ | Hold time | Data after CLK ↑ | 1 | | 1 | | ns |

### 6.9 Switching Characteristics, $V_{CC}$ = 2.5 V ± 0.2 V

over recommended operating free-air temperature range, $V_{CC}$ = 2.5 V ± 0.2 V (unless otherwise noted) (see Figure 6)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | TEST CONDITIONS | $T_A$ = 25°C | | | SN74LV166A | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN | TYP | MAX | MIN | MAX | |
| $f_{max}$ | | | $C_L$ = 15 pF | 50[1] | 105[1] | | 45 | | MHz |
| | | | $C_L$ = 50 pF | 40 | 80 | | 35 | | |
| $t_{PHL}$ | $\overline{CLR}$ | $Q_H$ | $C_L$ = 15 pF | | 8.8[1] | 16[1] | 1 | 18 | ns |
| $t_{pd}$ | CLK | | | | 9.2[1] | 19.8[1] | 1 | 22 | |
| $t_{PHL}$ | $\overline{CLR}$ | $Q_H$ | $C_L$ = 50 pF | | 11.3 | 19.5 | 1 | 22 | ns |
| $t_{pd}$ | CLK | | | | 11.8 | 23.3 | 1 | 26 | |


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1. On products compliant to MIL-PRF-38535, this parameter is not production tested.

## 6.10 Switching Characteristics, $V_{CC}$ = 3.3 V ± 0.3 V

over recommended operating free-air temperature range, $V_{CC}$ = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 6)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | TEST CONDITIONS | $T_A$ = 25°C | | | SN74LV166A | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN | TYP | MAX | MIN | MAX | |
| $f_{max}$ | | | $C_L$ = 15 pF | 65[1] | 150[1] | | 55 | | MHz |
| | | | $C_L$ = 50 pF | 60 | 120 | | 50 | | |
| $t_{PHL}$ | $\overline{CLR}$ | $Q_H$ | $C_L$ = 15 pF | | 6.3[1] | 12.5[1] | 1 | 15 | ns |
| $t_{pd}$ | CLK | | | | 6.6[1] | 15.4[1] | 1 | 18 | |
| $t_{PHL}$ | $\overline{CLR}$ | $Q_H$ | $C_L$ = 50 pF | | 7.9 | 16.3 | 1 | 18.5 | ns |
| $t_{pd}$ | CLK | | | | 8.3 | 18.9 | 1 | 21.5 | |

1. On products compliant to MIL-PRF-38535, this parameter is not production tested.

## 6.11 Switching Characteristics, $V_{CC}$ = 5 V ± 0.5 V

over recommended operating free-air temperature range, $V_{CC}$ = 5 V ± 0.5 V (unless otherwise noted) (see Figure 6)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | TEST CONDITIONS | $T_A$ = 25°C | | | SN74LV166A | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN | TYP | MAX | MIN | MAX | |
| $f_{max}$ | | | $C_L$ = 15 pF | 110[1] | 205[1] | | 90 | | MHz |
| | | | $C_L$ = 50 pF | 95 | 160 | | 85 | | |
| $t_{PHL}$ | $\overline{CLR}$ | $Q_H$ | $C_L$ = 15 pF | | 4.6[1] | 8.6[1] | 1 | 10 | ns |
| $t_{pd}$ | CLK | | | | 4.8[1] | 9.9[1] | 1 | 11.5 | |
| $t_{PHL}$ | $\overline{CLR}$ | $Q_H$ | $C_L$ = 50 pF | | 5.7 | 10.6 | 1 | 12 | ns |
| $t_{pd}$ | CLK | | | | 6.1 | 11.9 | 1 | 13.5 | |

1. On products compliant to MIL-PRF-38535, this parameter is not production tested.

## Timing Diagram

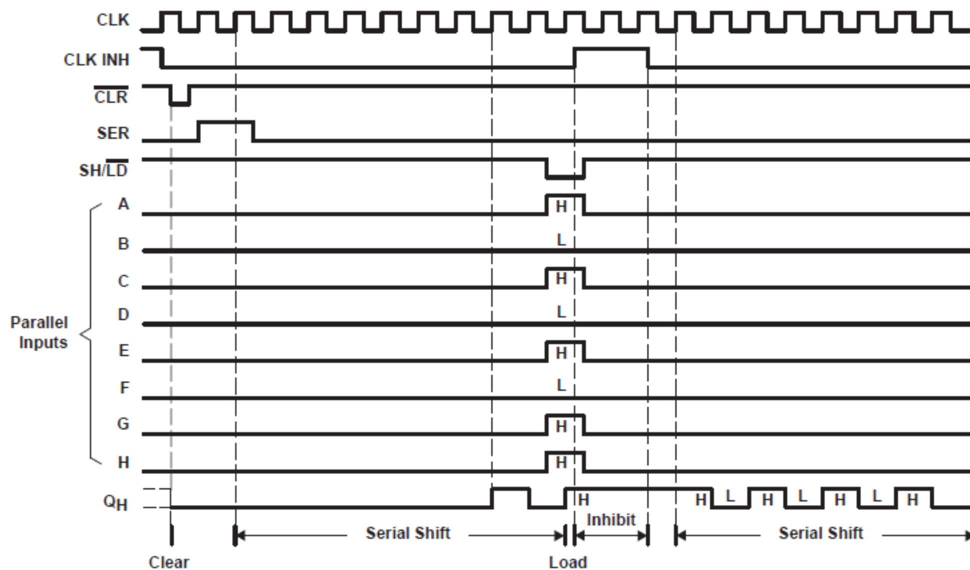


图 6-1. Typical Clear, Shift, Load, Inhibit, and Shift Sequence

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## 6.12 Operating Characteristics

$T_A$ = 25℃

| PARAMETER | | TEST CONDITIONS | | $V_{CC}$ | TYP | UNIT |
|---|---|---|---|---|---|---|
| $C_{pd}$ | Power dissipation capacitance | $C_L$ = 50 pF | f = 10 MHz | 3.3 V | 39.1 | pF |
| | | | | 5 V | 44.5 | |


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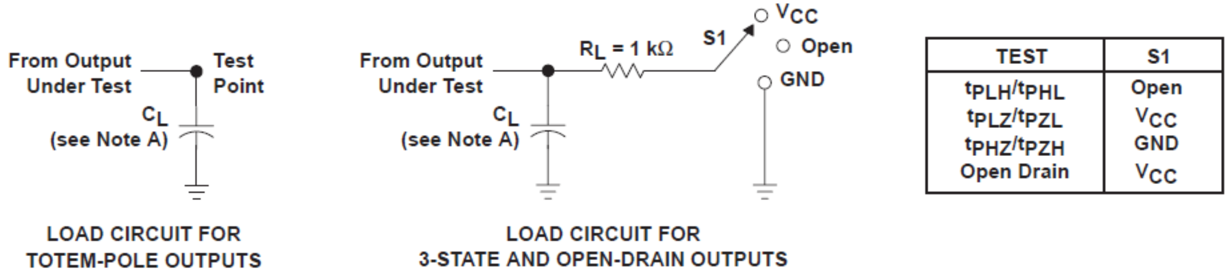
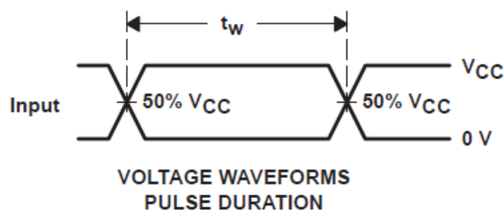
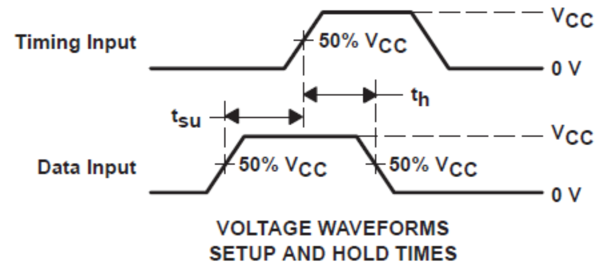
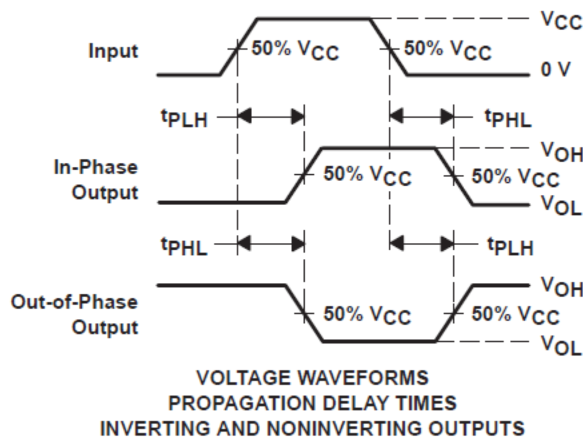
## 7 Parameter Measurement Information

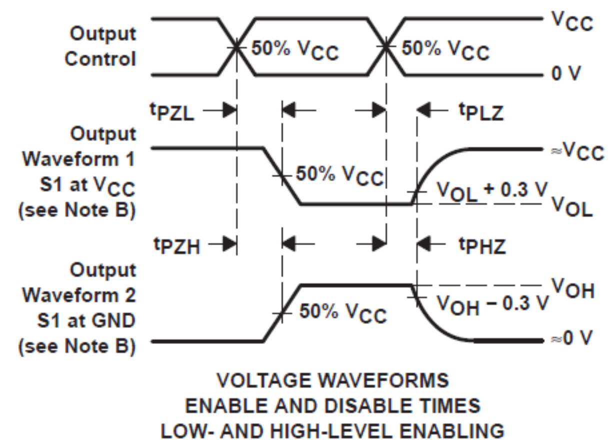



| TEST | S1 |
|---|---|
| $t_{PLH}/t_{PHL}$ | Open |
| $t_{PLZ}/t_{PZL}$ | $V_{CC}$ |
| $t_{PHZ}/t_{PZH}$ | GND |
| Open Drain | $V_{CC}$ |




A. $C_L$ includes probe and jig capacitance.

B. Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following charactersitics: PRR ⩽ 1 MHz, $Z_O$ = 50 Ω, $t_r$ = 6 ns, $t_f$ = 6 ns.

C. For clock inputs, $f_{max}$ is measured when the input duty cycle is 50%

D. The outputs are measured one at a time with one input transition per measurement.

E. tPLZ and tPHZ are the same as tdis.

F. tPZL and tPZH are the same as ten.

G. tPHL and tPLH are the same as tpd.

H. All parameters and waveforms are not applicable to all devices.

# 8 Detailed Description

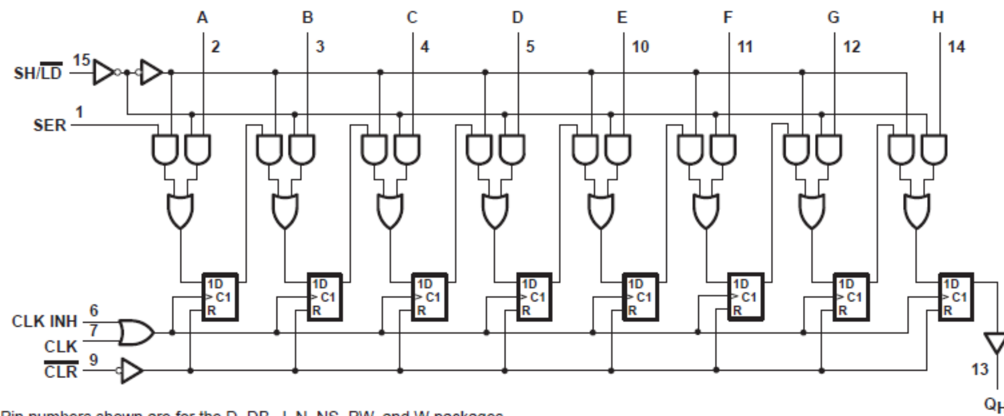
## 8.1 Overview

These parallel-in or serial-in, serial-out registers feature gated clock (CLK, CLK INH) inputs and an overriding clear ($\overline{\text{CLR}}$) input. The parallel-in or serial-in modes are established by the shift/load (SH/$\overline{\text{LD}}$) input. When high, SH/$\overline{\text{LD}}$ enables the serial (SER) data input and couples the eight flip-flops for serial shifting with each clock (CLK) pulse. When low, the parallel (broadside) data inputs are enabled, and synchronous loading occurs on the next clock pulse. During parallel loading, serial data flow is inhibited.

Clocking is accomplished on the low-to-high-level edge of CLK through a 2-input positive-NOR gate, permitting one input to be used as a clock-enable or clock-inhibit function. Holding either CLK or CLK INH high inhibits clocking; holding either low enables the other clock input. This allows the system clock to be free running, and the register can be stopped on command with the other clock input. CLK INH should be changed to the high level only when CLK is high. $\overline{\text{CLR}}$ overrides all other inputs, including CLK, and resets all flip-flops to zero.

These devices are fully specified for partial-power-down applications using $I_{off.}$ The $I_{off}$ circuitry disables the outputs, preventing damaging current backflow through the devices when they are powered down.

## 8.2 Functional Block Diagram




Pin numbers shown are for the D, DB, J, N, NS, PW, and W packages.

## 8.3 Device Functional Modes

**表 8-1. Function Table**

| INPUTS | | | | | | OUTPUTS | | |
|---|---|---|---|---|---|---|---|---|
| | | | | | | INTERNAL | | $Q_H$ |
| $\overline{\text{CLR}}$ | SH/$\overline{\text{LD}}$ | CLK INH | CLK | SER | PARALLEL A...H | $Q_A$ | $Q_B$ | |
| L | X | X | X | X | X | L | L | L |
| H | X | L | L | X | X | $Q_{A0}$ | $Q_{B0}$ | $Q_{H0}$ |
| H | L | L | ↑ | X | a...h | a | b | h |
| H | H | L | ↑ | H | X | H | $Q_{An}$ | $Q_{Gn}$ |
| H | H | L | ↑ | L | X | L | $Q_{An}$ | $Q_{Gn}$ |
| H | X | H | ↑ | X | X | $Q_{A0}$ | $Q_{B0}$ | $Q_{H0}$ |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# 9 Application and Implementation

备注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

## 9.1 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in the 节 6.1 table. Each $V_{CC}$ terminal should have a bypass capacitor to prevent power disturbance. For this device, a 0.1-μF capacitor is recommended. It is acceptable to parallel multiple bypass caps to reject different frequencies of noise. The 0.1-μF and 1-μF capacitors are commonly used in parallel. The bypass capacitor should be installed as close to the power terminals as possible for best results.

## 9.2 Layout

### 9.2.1 Layout Guidelines

In many cases, functions or parts of functions of digital logic devices are unused. Some examples are when only two inputs of a triple-input AND gate are used, or when only 3 of the 4 channels are used. Such input pins should not be left completely unconnected because the unknown voltages result in undefined operational states.

Specified in 节 9.2.1.1 are rules that must be observed under all circumstances. All unused inputs of digital logic devices must be connected to a high or low bias to prevent them from floating. The logic level that must be applied to any particular unused input depends on the function of the device. Generally they are tied to GND or $V_{CC}$, whichever makes more sense or is more convenient. It is recommended to float outputs unless the part is a transceiver. If the transceiver has an output enable pin, it disables the output section of the part when asserted. This pin keeps the input section of the I/Os from being disabled and floated.

#### *9.2.1.1 Layout Example*

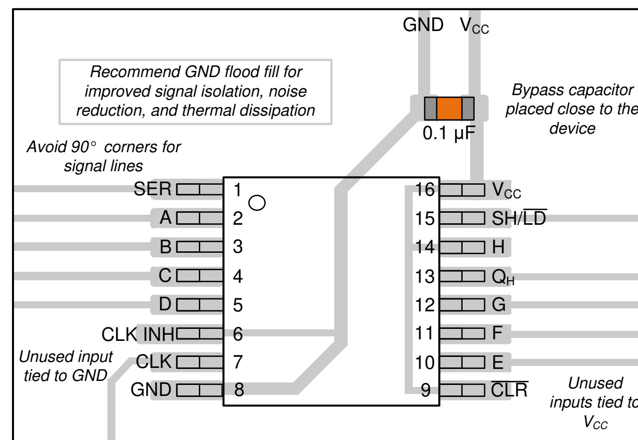


**图 9-1. Layout Example**

# 10 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

## 10.1 Documentation Support

### 10.1.1 Related Documentation

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

表 10-1. Related Links

| PARTS | PRODUCT FOLDER | SAMPLE & BUY | TECHNICAL DOCUMENTS | TOOLS & SOFTWARE | SUPPORT & COMMUNITY |
|---|---|---|---|---|---|
| SN74LV166A | Click here | Click here | Click here | Click here | Click here |

## 10.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates—including silicon errata—go to the product folder for your device on ti.com. In the upper right-hand corner, click the *Alert me* button. This registers you to receive a weekly digest of product information that has changed (if any). For change details, check the revision history of any revised document.

## 10.3 支持资源

TI E2E™ 支持论坛是工程师的重要参考资料，可直接从专家获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题可获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的《使用条款》。

## Trademarks

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## 10.4 静电放电警告

静电放电 (ESD) 会损坏这个集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

## 10.5 术语表

TI 术语表 本术语表列出并解释了术语、首字母缩略词和定义。

# 11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.


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## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead finish/ Ball material (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| SN74LV166AD | OBSOLETE | SOIC | D | 16 | | TBD | Call TI | Call TI | -40 to 85 | LV166A | |
| SN74LV166ADBR | ACTIVE | SSOP | DB | 16 | 2000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | LV166A | Samples |
| SN74LV166ADGVR | ACTIVE | TVSOP | DGV | 16 | 2000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | LV166A | Samples |
| SN74LV166ADR | ACTIVE | SOIC | D | 16 | 2500 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | LV166A | Samples |
| SN74LV166ANSR | ACTIVE | SOP | NS | 16 | 2000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | 74LV166A | Samples |
| SN74LV166APW | OBSOLETE | TSSOP | PW | 16 | | TBD | Call TI | Call TI | -40 to 85 | LV166A | |
| SN74LV166APWR | ACTIVE | TSSOP | PW | 16 | 2000 | RoHS & Green | NIPDAU \| SN | Level-1-260C-UNLIM | -40 to 85 | LV166A | Samples |

(1) The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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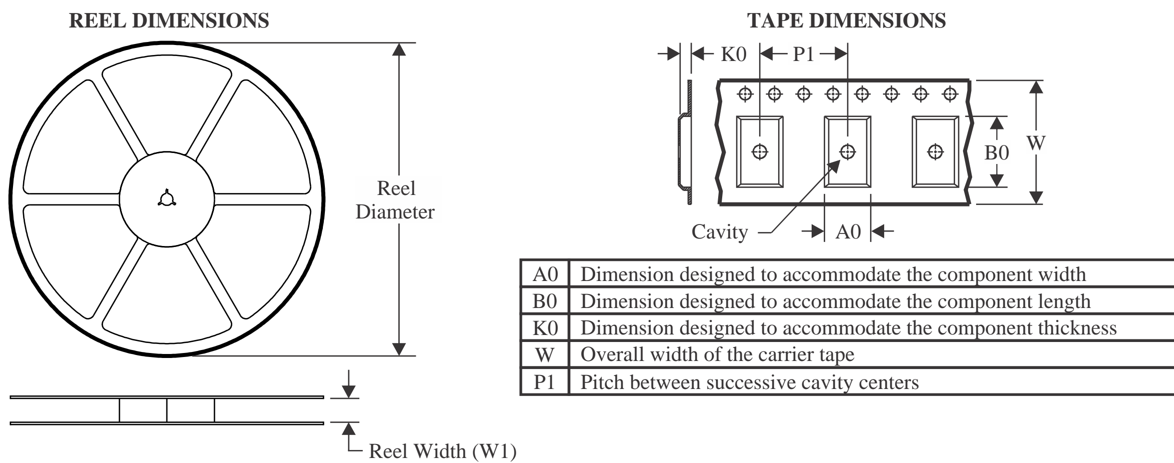
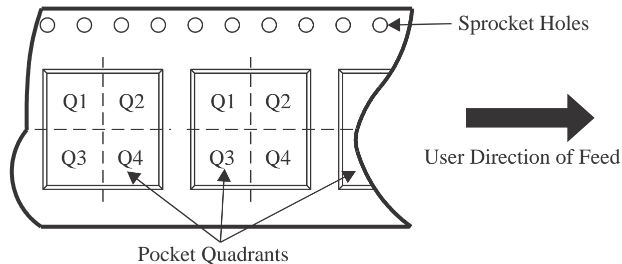
## TAPE AND REEL INFORMATION



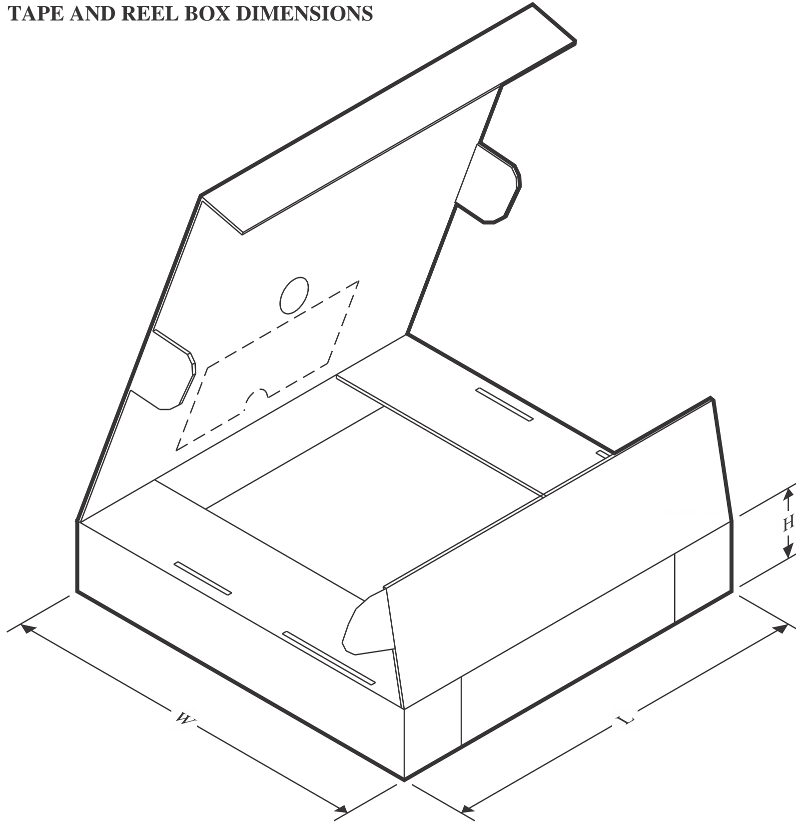

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| SN74LV166ADBR | SSOP | DB | 16 | 2000 | 330.0 | 16.4 | 8.35 | 6.6 | 2.4 | 12.0 | 16.0 | Q1 |
| SN74LV166ADGVR | TVSOP | DGV | 16 | 2000 | 330.0 | 12.4 | 6.8 | 4.0 | 1.6 | 8.0 | 12.0 | Q1 |
| SN74LV166ADR | SOIC | D | 16 | 2500 | 330.0 | 16.4 | 6.5 | 10.3 | 2.1 | 8.0 | 16.0 | Q1 |
| SN74LV166ANSR | SOP | NS | 16 | 2000 | 330.0 | 16.4 | 8.2 | 10.5 | 2.5 | 12.0 | 16.0 | Q1 |
| SN74LV166APWR | TSSOP | PW | 16 | 2000 | 330.0 | 12.4 | 6.9 | 5.6 | 1.6 | 8.0 | 12.0 | Q1 |
| SN74LV166APWR | TSSOP | PW | 16 | 2000 | 330.0 | 12.4 | 6.9 | 5.6 | 1.6 | 8.0 | 12.0 | Q1 |

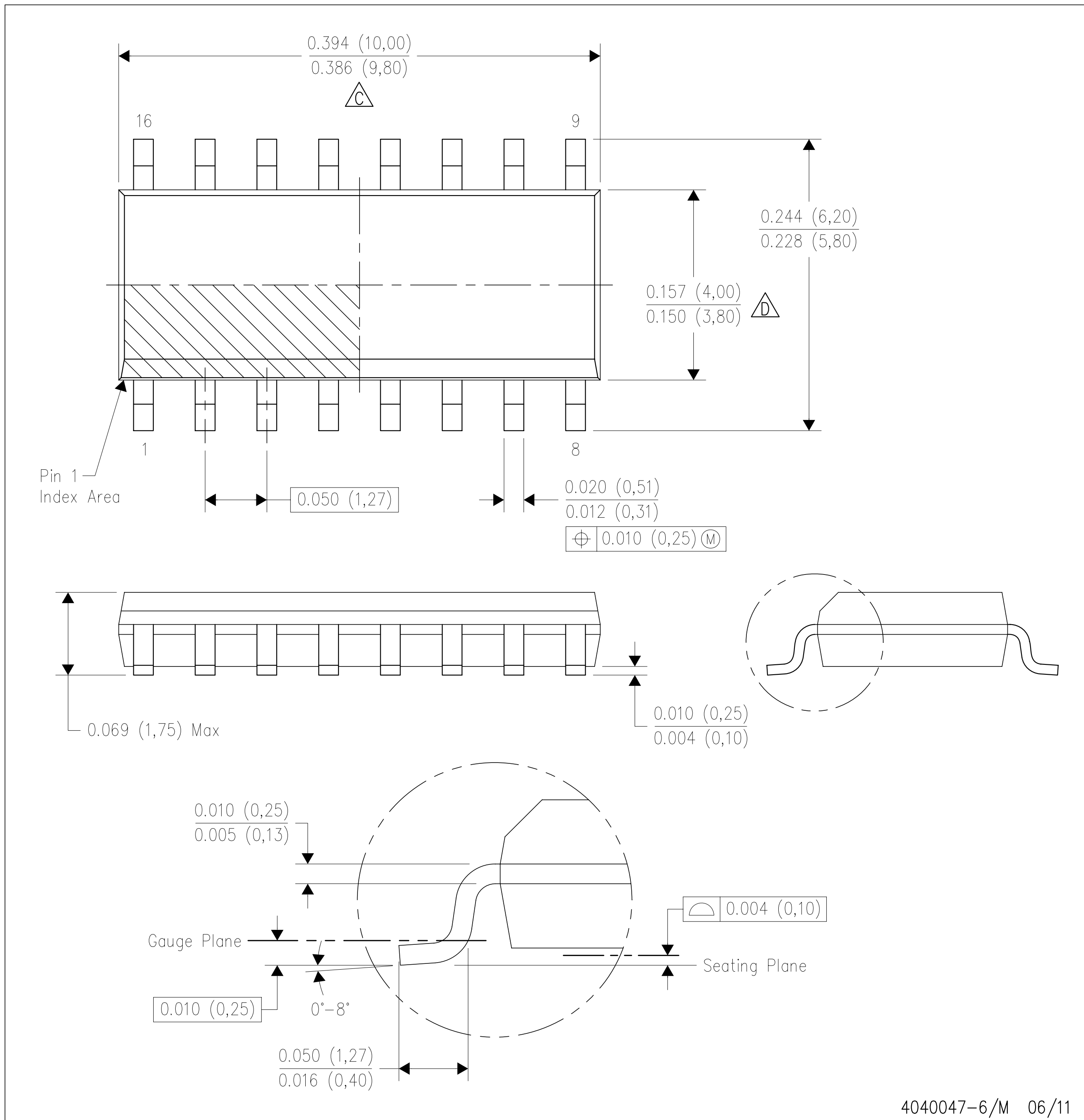
TAPE AND REEL BOX DIMENSIONS



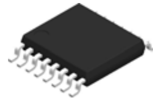

*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| SN74LV166ADBR | SSOP | DB | 16 | 2000 | 356.0 | 356.0 | 35.0 |
| SN74LV166ADGVR | TVSOP | DGV | 16 | 2000 | 356.0 | 356.0 | 35.0 |
| SN74LV166ADR | SOIC | D | 16 | 2500 | 340.5 | 336.1 | 32.0 |
| SN74LV166ANSR | SOP | NS | 16 | 2000 | 356.0 | 356.0 | 35.0 |
| SN74LV166APWR | TSSOP | PW | 16 | 2000 | 356.0 | 356.0 | 35.0 |
| SN74LV166APWR | TSSOP | PW | 16 | 2000 | 353.0 | 353.0 | 32.0 |

D (R–PDSO–G16) PLASTIC SMALL OUTLINE




NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS-012 variation AC.



6.6
6.2 TYP

A

PIN 1 INDEX AREA

14X 0.65

16

1

5.1
4.9
NOTE 3

2X
4.55

8

9

16X 0.30
0.19

0.1Ⓜ C A B

B

4.5
4.3
NOTE 4

SEATING PLANE

C

0.1 C

1.2 MAX

(0.15) TYP

SEE DETAIL A

0.25
GAGE PLANE

0.15
0.05

0° -8°

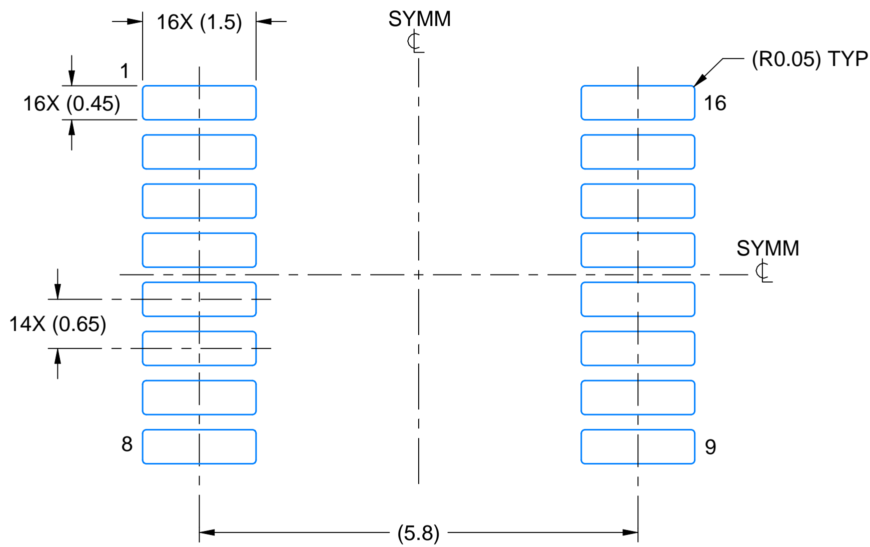
0.75
0.50

DETAIL A
TYPICAL

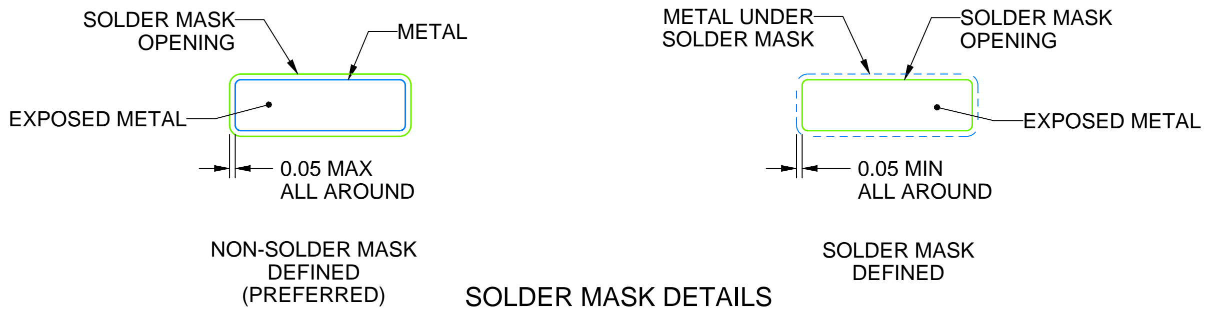
4220204/A 02/2017

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.




LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

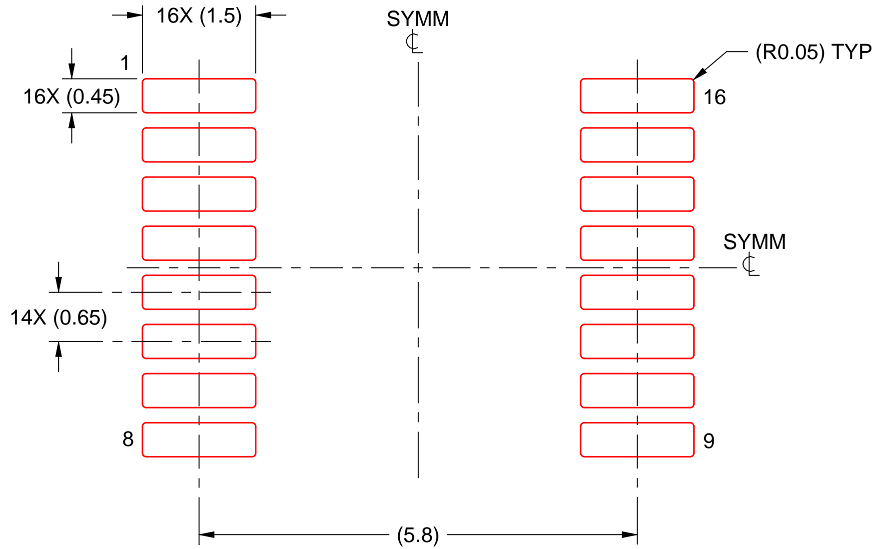



SOLDER MASK DETAILS

4220204/A 02/2017

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.




SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220204/A 02/2017

NOTES: (continued)

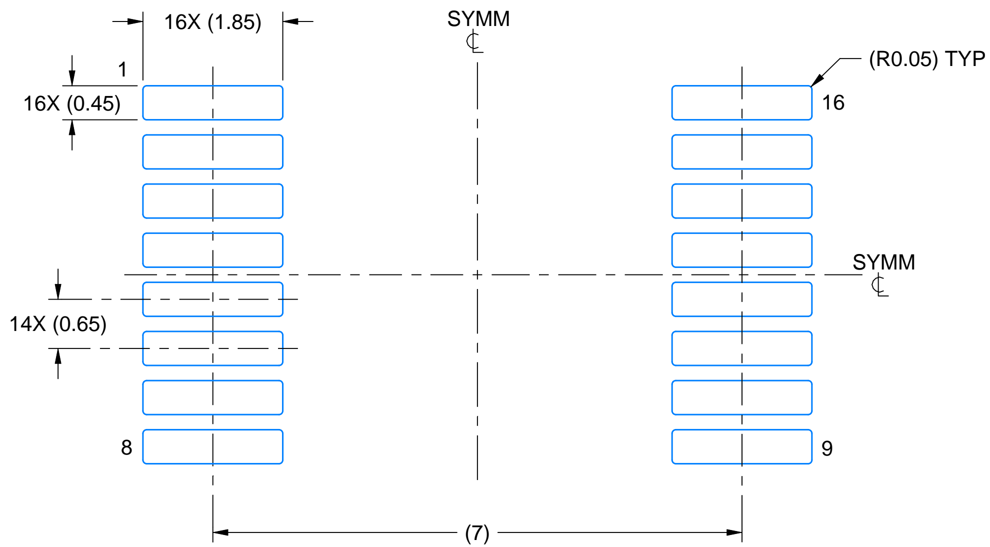
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

8.2
7.4 TYP
A
PIN 1 INDEX AREA
14X 0.65
16
1
2X
4.55
6.5
5.9
NOTE 3
8
9
16X 0.38
0.22
0.1 Ⓜ C A B
B
5.6
5.0
NOTE 4
C
0.1 C
SEATING
PLANE
0.25
0.09
SEE DETAIL A
0.25
GAGE PLANE
2 MAX
0° -8°
0.95
0.55
0.05 MIN
DETAIL A
TYPICAL

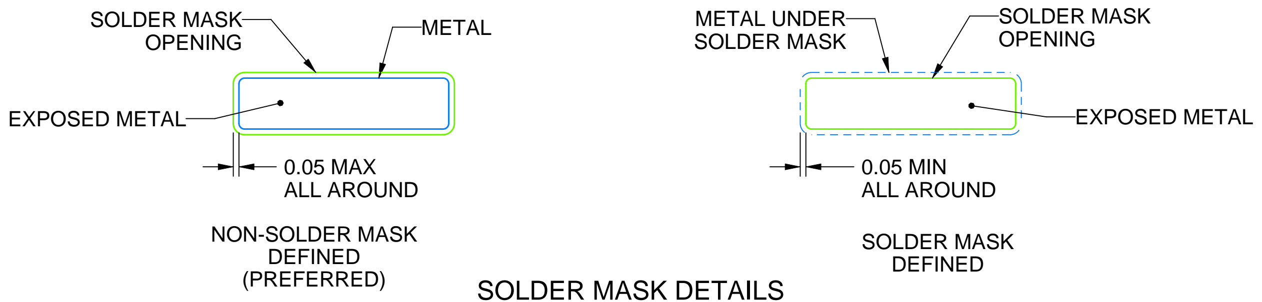
4220763/A 05/2022

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-150.




LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X




NON-SOLDER MASK DEFINED (PREFERRED)

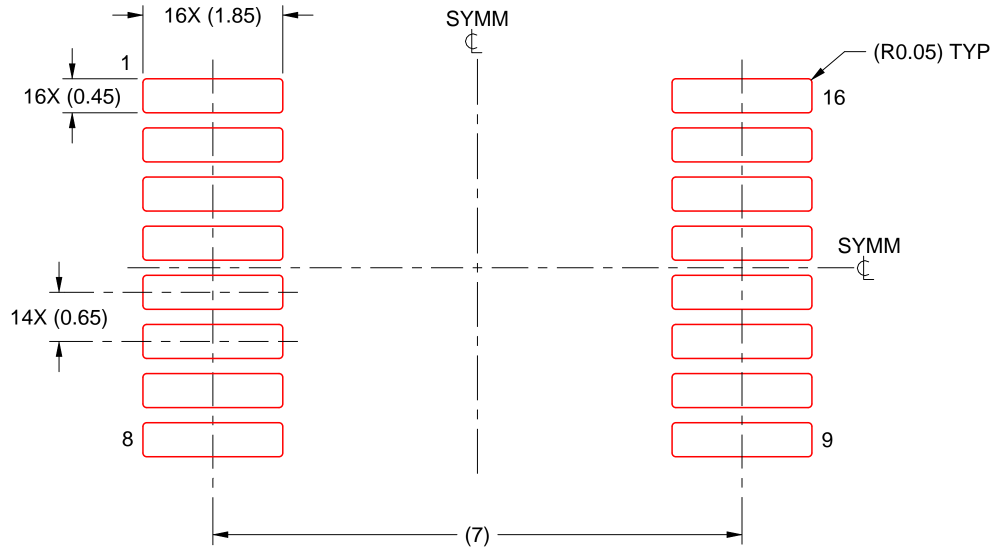
SOLDER MASK DEFINED

SOLDER MASK DETAILS

4220763/A 05/2022

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.




SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

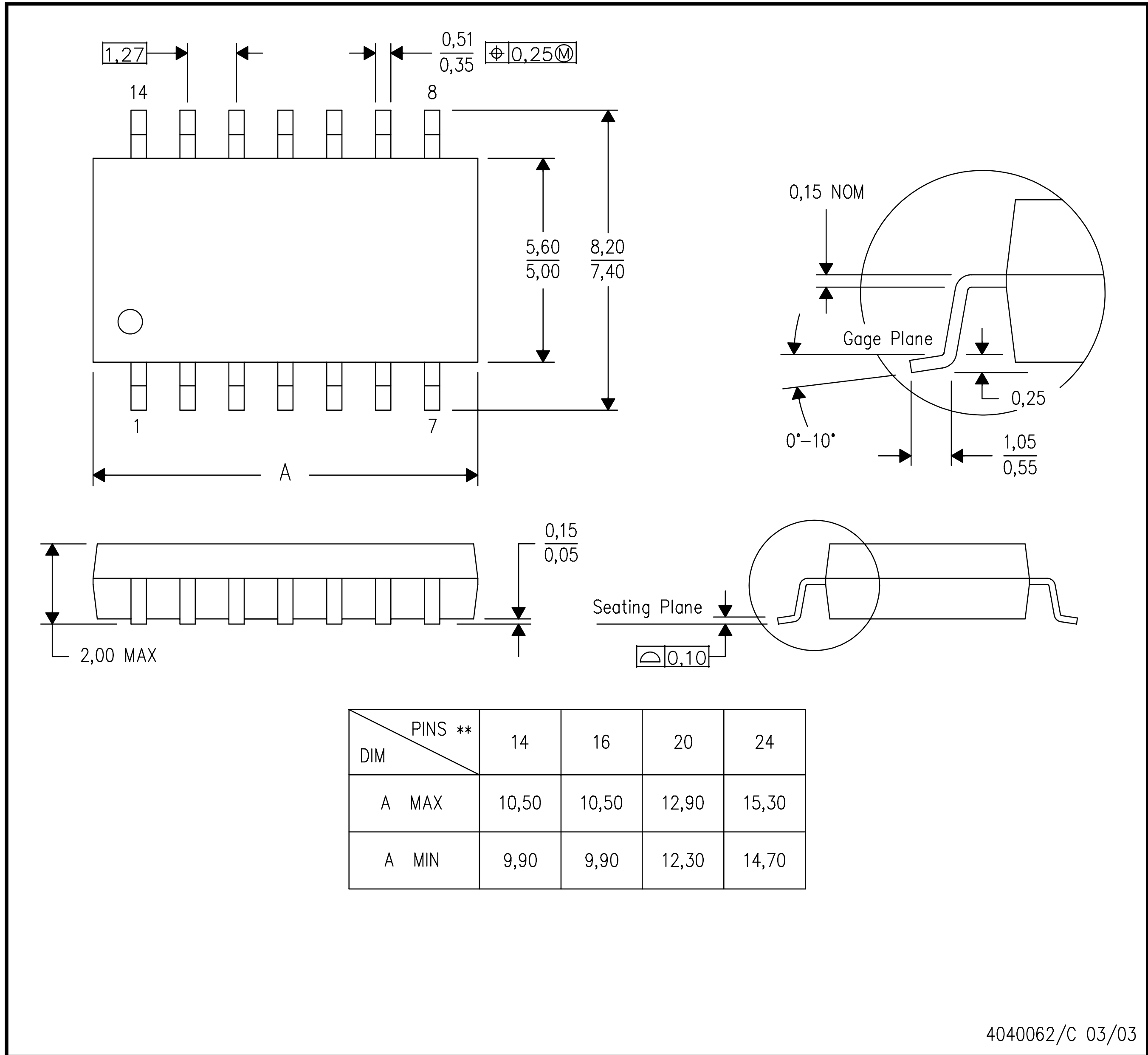
4220763/A 05/2022

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

**NS (R-PDSO-G**)** **PLASTIC SMALL-OUTLINE PACKAGE**

**14-PINS SHOWN**

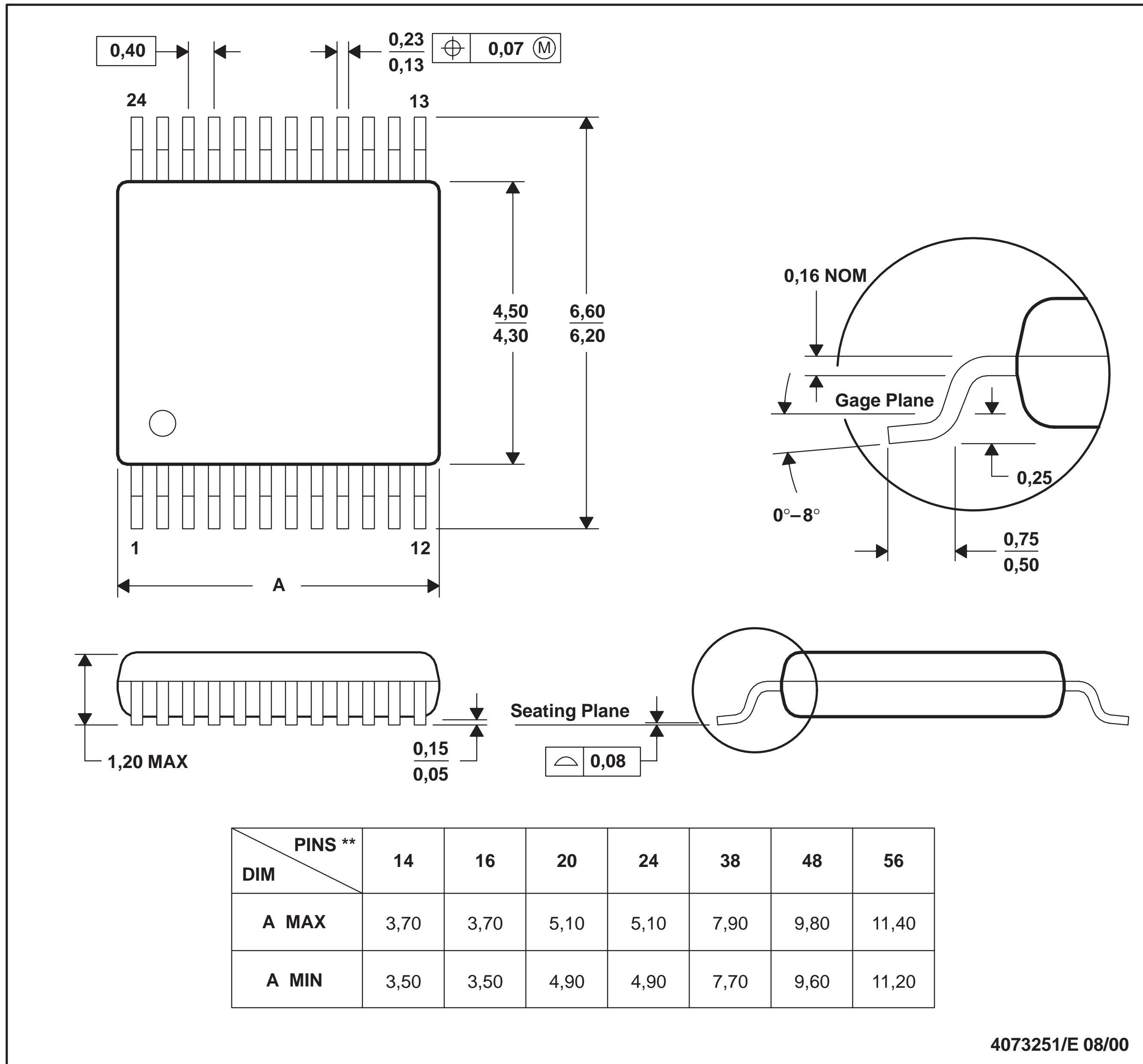



| DIM \ PINS ** | 14 | 16 | 20 | 24 |
|---|---|---|---|---|
| A MAX | 10,50 | 10,50 | 12,90 | 15,30 |
| A MIN | 9,90 | 9,90 | 12,30 | 14,70 |

NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

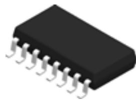
**DGV (R-PDSO-G**)** **PLASTIC SMALL-OUTLINE**

**24 PINS SHOWN**




| PINS ** / DIM | 14 | 16 | 20 | 24 | 38 | 48 | 56 |
|---|---|---|---|---|---|---|---|
| **A MAX** | 3,70 | 3,70 | 5,10 | 5,10 | 7,90 | 9,80 | 11,40 |
| **A MIN** | 3,50 | 3,50 | 4,90 | 4,90 | 7,70 | 9,60 | 11,20 |

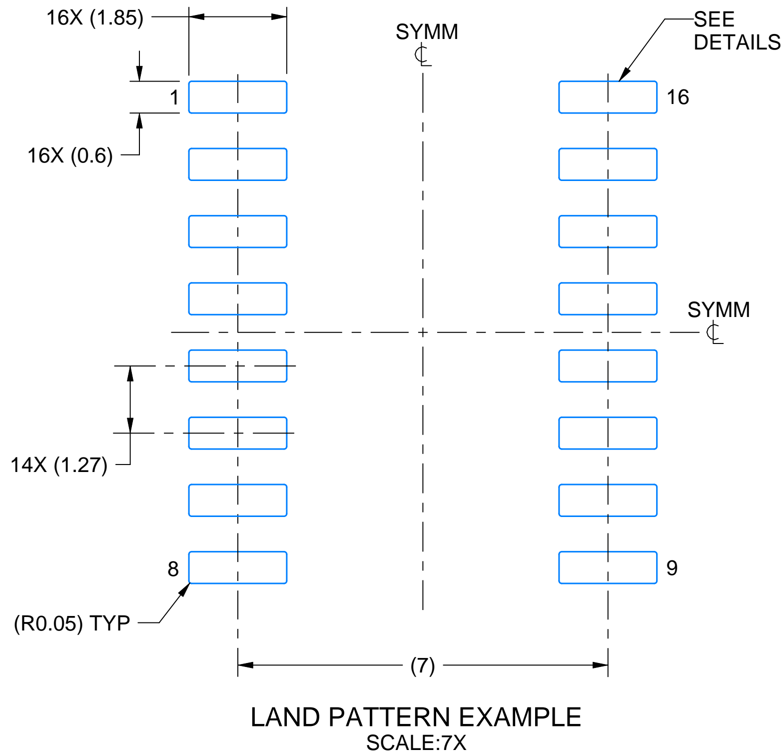
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.
D. Falls within JEDEC: 24/48 Pins – MO-153
14/16/20/56 Pins – MO-194



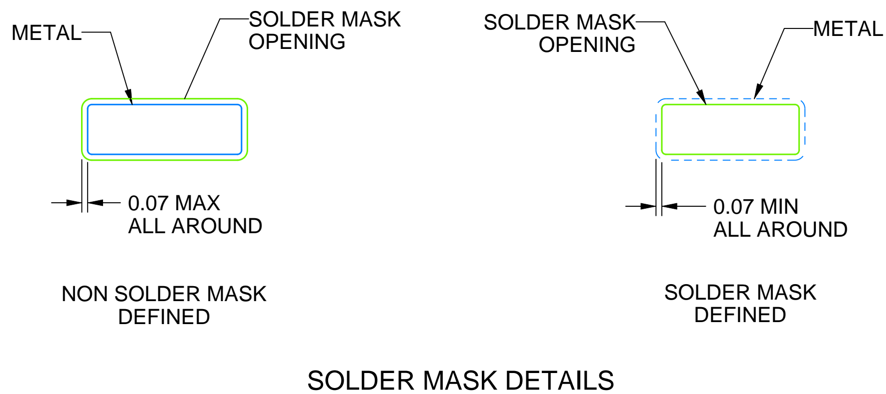


NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.




LAND PATTERN EXAMPLE
SCALE:7X




NON SOLDER MASK
DEFINED

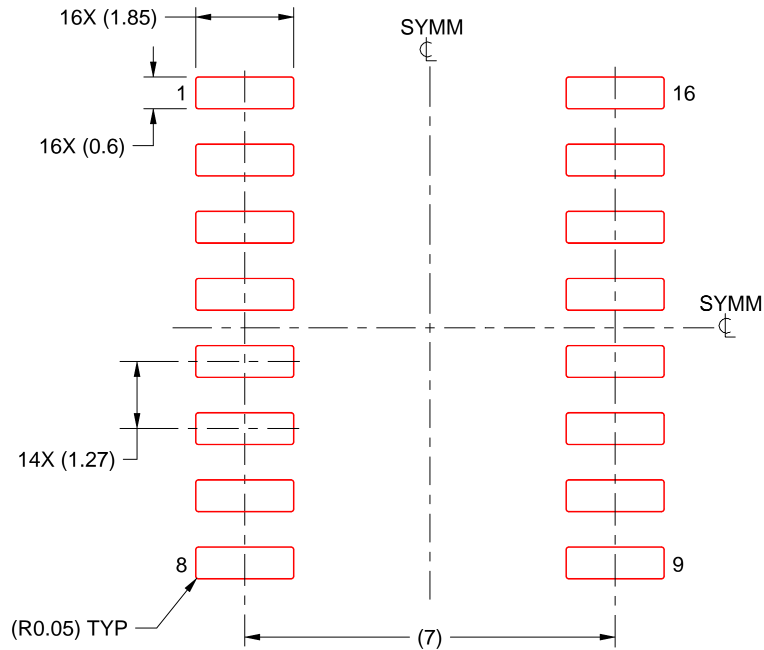
SOLDER MASK
DEFINED

SOLDER MASK DETAILS

4220735/A 12/2021

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.




SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:7X

4220735/A 12/2021

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

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