SN74LV1T86-Q1 汽车类单电源 2 输入异或门 CMOS 逻辑电平转换器

1 特性

- 符合面向汽车应用的 AEC-Q100 标准：
  - 器件温度等级 1：-40°C 至 +125°C
  - 器件 HBM ESD 分类等级 2
  - 器件 CDM ESD 分类等级 C4B
- 1.8V 至 5.5V 的宽工作电压范围
- 单电源电压转换器（参阅 *LVxT 增强输入电压*）：
  - 升压转换：
    - 1.2V 至 1.8V
    - 1.5V 至 2.5V
    - 1.8V 至 3.3V
    - 3.3V 至 5.0V
  - 降压转换：
    - 5.0V、3.3V、2.5V 至 1.8V
    - 5.0V、3.3V 至 2.5V
    - 5.0V 至 3.3V
- 5.5V 容限输入引脚
- 支持标准引脚排列
- 速率高达 150Mbps，具有 5V 或 3.3V V_{CC}
- 闩锁性能超过 250mA，符合 JESD 17 规范

2 应用

- 检测输入信号中的相位差
- 创建可选的反相器或缓冲器

3 说明

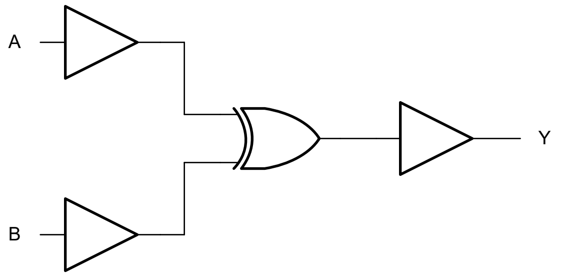
SN74LV1T86-Q1 是一个 2 输入异或门。它以正逻辑执行布尔函数 Y = A ⊕ B。输出电平以电源电压 (V_{CC}) 为基准，并支持 1.8V、2.5V、3.3V 和 5V CMOS 电平。

该输入经设计，具有较低阈值电路，支持较低电压 CMOS 输入的升压转换（例如 1.2V 输入转换为 1.8V 输出或 1.8V 输入转换为 3.3V 输出）。此外，5V 容限输入引脚可实现降压转换（例如 3.3V 转 2.5V 输出）。

封装信息

器件型号	封装[1]	封装尺寸[2]	封装尺寸[3]
SN74LV1T86-Q1	DCK（SC-70，5）	2mm × 2.1mm	2mm x 1.25mm
	DBV（SOT-23，5）	2.9mm × 2.8mm	2.9mm × 1.6mm

(1) 更多相关信息，请参阅第 11 节。
(2) 封装尺寸（长 × 宽）为标称值，并包括引脚（如适用）。
(3) 封装尺寸（长 × 宽）为标称值，不包括引脚。



简化逻辑图（正逻辑）

English Data Sheet: SCLS954

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4 Pin Configuration and Functions

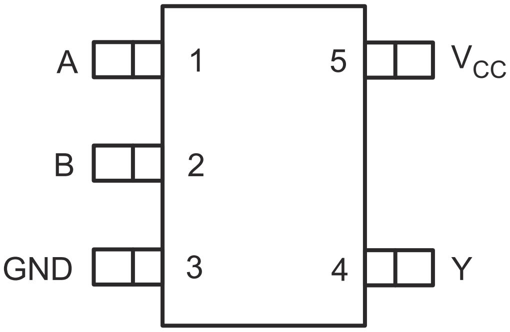

图 4-1. SN74LV1T86-Q1 DBV Package, 5-Pin SOT-23; DCK Package, 5-Pin SC-70 (Top View)

表 4-1. Pin Functions

PIN		TYPE[1]	DESCRIPTION
NAME	NO.		
A	1	I	Input A
B	2	I	Input B
GND	3	G	Ground
Y	4	O	Output Y
V_{CC}	5	P	Positive Supply

(1) I = input, O = output, I/O = input or output, G = ground, P = power.

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V_{CC}	Supply voltage		–0.5	7	V
V_I	Input voltage range		-0.5	7	V
V_O	Output voltage range		-0.5	V_{CC} + 0.5	V
V_O	Voltage range applied to any output in the high-impedance or power-off state		-0.5	4.6	V
I_{IK}	Input clamp current(2)	$V_I < 0$	–20		mA
I_{OK}	Output clamp current(2)	$V_O < 0$ or $V_O > V_{CC}$	–20	20	mA
I_O	Continuous output current	$V_O = 0$ to V_{CC}	–25	25	mA
I_O	Continuous output current through V_{CC} or GND		–50	50	mA
T_J	Junction temperature			150	°C
T_{stg}	Storage temperature		–65	150	°C

(1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. Absolute maximum ratings do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If briefly operating outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not sustain damage, but it may not be fully functional. Operating the device in this manner may affect device reliability, functionality, performance, and shorten the device lifetime.

(2) The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per AEC Q100-002(1) HBM ESD Classification Level 2	±2000	V
		Charged device model (CDM), per AEC Q100-011 CDM ESD Classification Level C4B	±1000	

(1) AEC Q100-002 indicate that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
V_{CC}	Supply voltage		1.6	5.5	V
V_I	Input voltage		0	5.5	V
V_O	Output voltage		0	V_{CC}	V
V_{IH}	High-level input voltage	V_{CC} = 1.65 V to 2 V	1.1		V
		V_{CC} = 2.25 V to 2.75 V	1.28		V
		V_{CC} = 3 V to 3.6 V	1.45		V
		V_{CC} = 4.5 V to 5.5 V	2.00		V
V_{IL}	Low-Level input voltage	V_{CC} = 1.65 V to 2 V		0.50	V
		V_{CC} = 2.25 V to 2.75 V		0.65	V
		V_{CC} = 3 V to 3.6 V		0.75	V
		V_{CC} = 4.5 V to 5.5 V		0.85	V
I_O	Output current	V_{CC} = 1.6 V to 2 V		±3	mA
		V_{CC} = 2.25 V to 2.75 V		±7	mA
		V_{CC} = 3.3 V to 5.0 V		±15	mA

5.3 Recommended Operating Conditions（续）

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
$\Delta t / \Delta v$	Input transition rise or fall rate	V_{CC} = 1.6 V to 5.0 V		20	ns/V
T_A	Operating free-air temperature		-40	125	C

5.4 Thermal Information

THERMAL METRIC(1)		SN74LV1T86-Q1		UNIT
		DBV (SOT-23)	DCK (SC70)	
		5 PINS	5 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	278.0	293.4	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	180.5	208.8	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	184.4	180.6	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	115.4	120.6	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	183.4	179.5	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

5.5 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	T_A = 25°C			-40°C to 125°C			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
V_{OH}	I_{OH} = -50 µA	1.65 V to 5.5 V	V_{CC}-0.1			V_{CC}-0.1			V
	I_{OH} = -2 mA	1.65 V	1.28	1.7(1)		1.21			
	I_{OH} = -3 mA	2.25 V	2	2.4(1)		1.93			
	I_{OH} = -5.5 mA	3.0 V	2.6	3.08(1)		2.49			
	I_{OH} = -8 mA	4.5 V	4.1	4.65(1)		3.95			
V_{OL}	I_{OH} = 50 µA	1.65 V to 5.5 V			0.1			0.1	V
	I_{OH} = 2 mA	1.65 V		0.1(1)	0.2			0.25	
	I_{OH} = 3 mA	2.25 V		0.1(1)	0.15			0.2	
	I_{OH} = 5.5 mA	3.0 V		0.2(1)	0.2			0.25	
	I_{OH} = 8 mA	4.5 V		0.3(1)	0.3			0.35	
I_{CC}	V_I = V_{CC} or GND, I_O = 0	5 V			1			10	µA
		3.3 V			1			10	
		2.5 V			1			10	
		1.8 V			1			10	
ΔI_{CC}	One input at 0.3 V or 3.4 V, other inputs at V_{CC} or GND	5.5 V			1.35			1.5	mA
	One input at 0.3 V or 1.1 V, other inputs at V_{CC} or GND	1.8 V			10			10	µA
I_I	V_I = 0 V to V_{CC}				0.12			±1	µA
C_i	V_I = V_{CC} or GND	3.3 V		2	10		2	10	pF
C_O	Vo = V_{CC} or GND	3.3 V		2.5			2.5		pF

5.5 Electrical Characteristics（续）

over operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	T_A = 25°C			-40°C to 125°C			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
C_{PD} (2) (3)	F = 1 MHz and 10 MHz	1.8 V		14					pF
		2.5 V		14					
		3.3 V		14					
		5.5 V		14					

(1) Typical value at nearest nominal voltage (1.8 V; 2.5 V; 3.3 V; 5 V)
(2) C_{PD} is used to determine the dynamic power consumption, per channel.
(3) $P_D = V_{CC}^2 \times F_I \times (C_{PD} + C_L)$ where F_I= input frequency, C_L= output load capacitance, V_{CC}= supply voltage

5.6 Switching Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	V_{CC}	T_A = 25°C			-40°C to 125°C			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
T_{PLH}	A or B	Y	CL = 15 pF	5 V		3.4	4.1	1	4.1	4.7	ns
T_{PHL}	A or B	Y	CL = 15 pF	5 V		3.4	4.1	1	4.1	4.7	ns
T_{PLH}	A or B	Y	CL = 50 pF	5 V		3.9	5.3	1	4.9	6.3	ns
T_{PHL}	A or B	Y	CL = 50 pF	5 V		3.9	5.3	1	4.9	6.3	ns
T_{PLH}	A or B	Y	CL = 15 pF	3.3 V		4.9	5.9	1	6	7.3	ns
T_{PHL}	A or B	Y	CL = 15 pF	3.3 V		4.9	5.9	1	6	7.3	ns
T_{PLH}	A or B	Y	CL = 50 pF	3.3 V		5.9	7.2	1	7.1	8.8	ns
T_{PHL}	A or B	Y	CL = 50 pF	3.3 V		5.9	7.2	1	7.1	8.8	ns
T_{PLH}	A or B	Y	CL = 15 pF	2.5 V		6.3	7.9	1	7.4	9.5	ns
T_{PHL}	A or B	Y	CL = 15 pF	2.5 V		6.3	7.9	1	7.4	9.5	ns
T_{PLH}	A or B	Y	CL = 50 pF	2.5 V		7.4	9.6	1	8.9	11.5	ns
T_{PHL}	A or B	Y	CL = 50 pF	2.5 V		7.4	9.6	1	8.9	11.5	ns
T_{PLH}	A or B	Y	CL = 15 pF	1.8 V		8.8	12.7	1	10.4	14.9	ns
T_{PHL}	A or B	Y	CL = 15 pF	1.8 V		8.8	12.7	1	10.4	14.9	ns
T_{PLH}	A or B	Y	CL = 50 pF	1.8 V		10.8	15.7	1	12.7	18.3	ns
T_{PHL}	A or B	Y	CL = 50 pF	1.8 V		10.8	15.7	1	12.7	18.3	ns

5.7 Typical Characteristics

T_A = 25°C (unless otherwise noted)

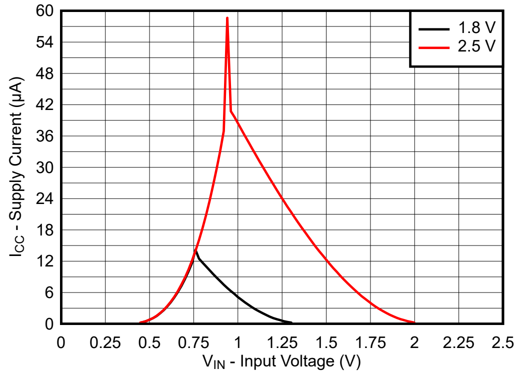

图 5-1. Supply Current Across Input Voltage 1.8-V and 2.5-V Supply

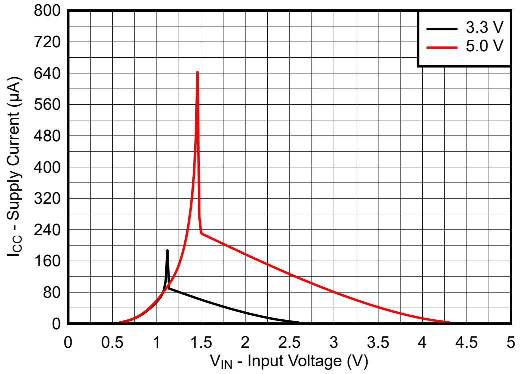

图 5-2. Supply Current Across Input Voltage 3.3-V and 5.0-V Supply

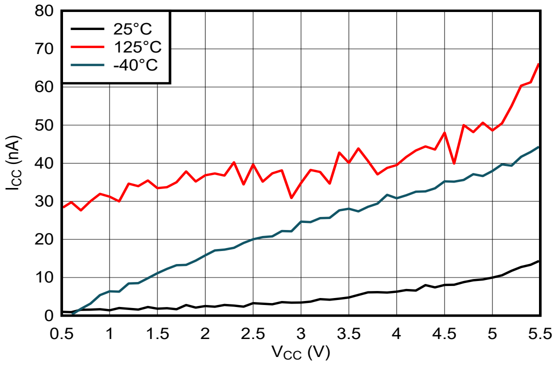

图 5-3. Supply Current Across Supply Voltage

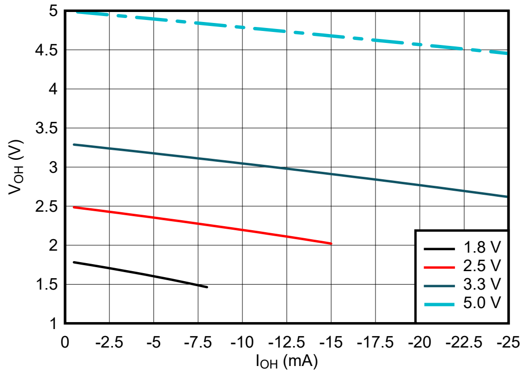

图 5-4. Output Voltage vs Current in HIGH State

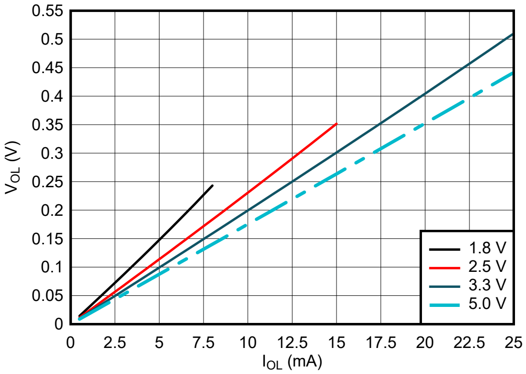

图 5-5. Output Voltage vs Current in LOW State

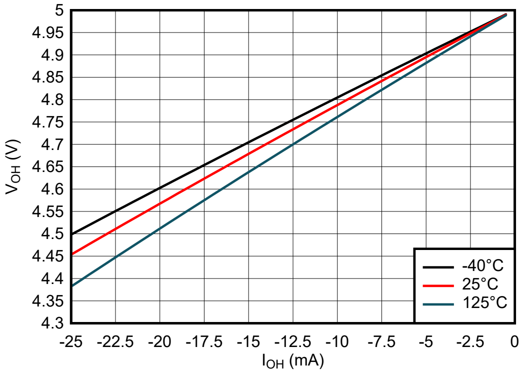

图 5-6. Output Voltage vs Current in HIGH State; 5-V Supply

5.7 Typical Characteristics (continued)

T_A = 25°C (unless otherwise noted)

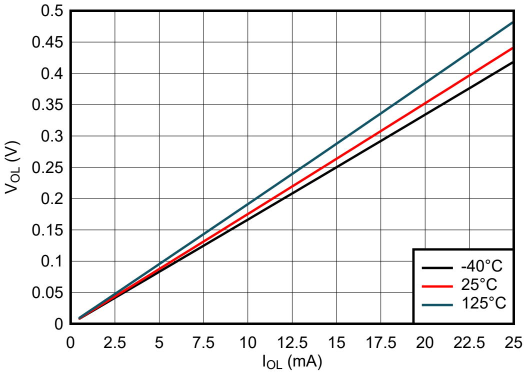

图 5-7. Output Voltage vs Current in LOW State; 5-V Supply

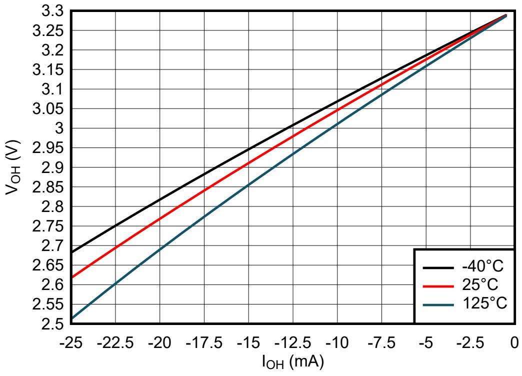

图 5-8. Output Voltage vs Current in HIGH State; 3.3-V Supply

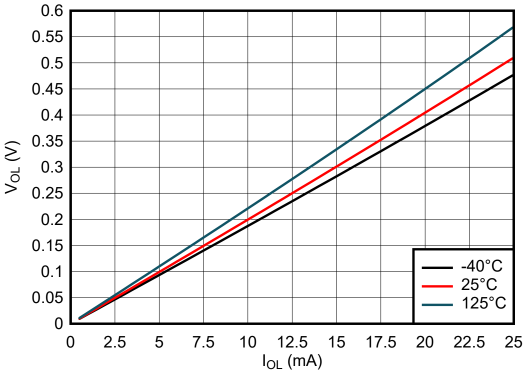

图 5-9. Output Voltage vs Current in LOW State; 3.3-V Supply

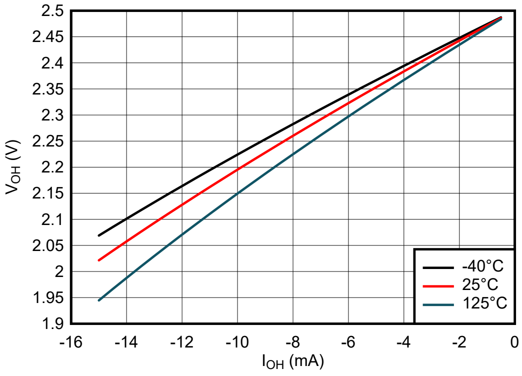

图 5-10. Output Voltage vs Current in HIGH State; 2.5-V Supply

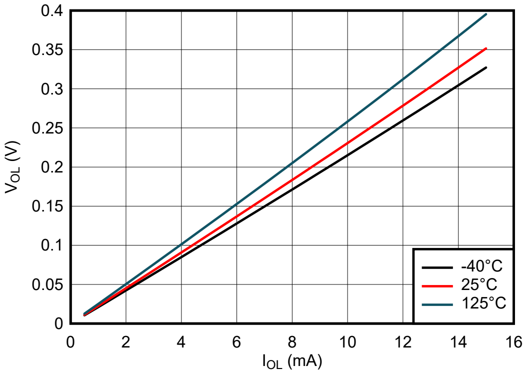

图 5-11. Output Voltage vs Current in LOW State; 2.5-V Supply

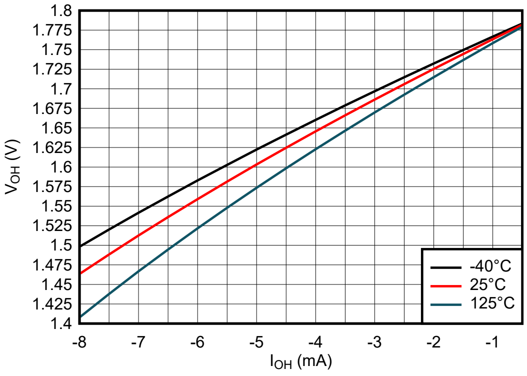

图 5-12. Output Voltage vs Current in HIGH State; 1.8-V Supply

5.7 Typical Characteristics (continued)

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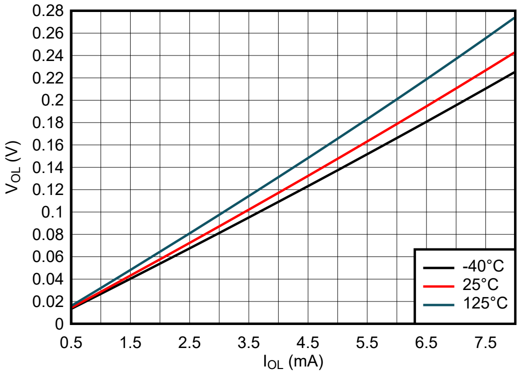


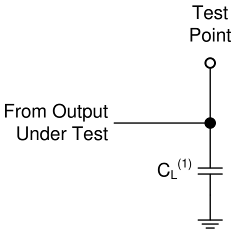
图 **5-13. Output Voltage vs Current in LOW State; 1.8-V Supply**

6 Parameter Measurement Information

Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: PRR ⩽ 1 MHz, Z_O = 50 Ω, t_t < 3 ns.

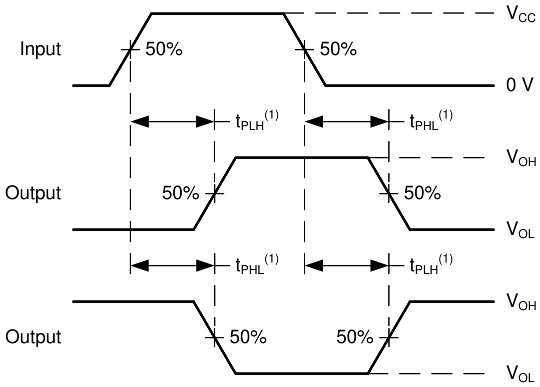
For clock inputs, f_{max} is measured when the input duty cycle is 50%.

The outputs are measured one at a time with one input transition per measurement.



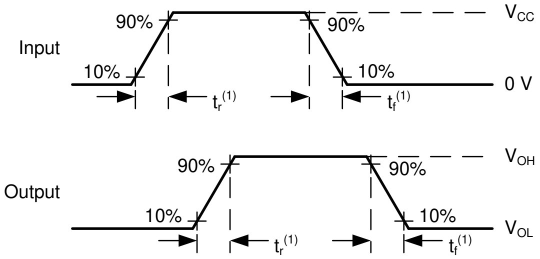
(1) C_L includes probe and test-fixture capacitance.

图 6-1. Load Circuit for Push-Pull Outputs



(1) The greater between t_{PLH} and t_{PHL} is the same as t_{pd}.

图 6-2. Voltage Waveforms Propagation Delays



(1) The greater between t_r and t_f is the same as t_t.

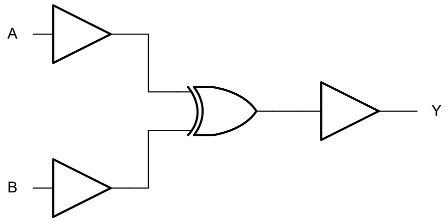
图 6-3. Voltage Waveforms, Input and Output Transition Times

7 Detailed Description

7.1 Overview

The SN74LV1T86-Q1 is a 2-input XOR Gates which performs the Boolean function $Y = A \oplus B$ in positive logic. The output level is referenced to the supply voltage (V_{CC}) and supports 1.8-V, 2.5-V, 3.3-V, and 5-V CMOS levels.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Balanced CMOS Push-Pull Outputs

This device includes balanced CMOS push-pull outputs. The term *balanced* indicates that the device can sink and source similar currents. The drive capability of this device may create fast edges into light loads, so routing and load conditions should be considered to prevent ringing. Additionally, the outputs of this device are capable of driving larger currents than the device can sustain without being damaged. It is important for the output power of the device to be limited to avoid damage due to overcurrent. The electrical and thermal limits defined in the *Absolute Maximum Ratings* must be followed at all times.

Unused push-pull CMOS outputs should be left disconnected.

7.3.2 LVxT Enhanced Input Voltage

The SN74LV1T86-Q1 belongs to TI's LVxT family of logic devices with integrated voltage level translation. This family of devices was designed with reduced input voltage thresholds to support up-translation, and inputs tolerant of signals with up to 5.5 V levels to support down-translation. The output voltage will always be referenced to the supply voltage (V_{CC}), as described in the *Electrical Characteristics* table. For proper functionality, input signals must remain at or below the specified $V_{IH(MIN)}$ level for a HIGH input state, and at or below the specified $V_{IL(MAX)}$ for a LOW input state. 图 7-1 shows the typical V_{IH} and V_{IL} levels for the LVxT family of devices, as well as the voltage levels for standard CMOS devices for comparison.

The inputs are high impedance and are typically modeled as a resistor in parallel with the input capacitance given in the *Electrical Characteristics*. The worst case resistance is calculated with the maximum input voltage, given in the *Absolute Maximum Ratings*, and the maximum input leakage current, given in the *Electrical Characteristics*, using Ohm's law ($R = V \div I$).

The inputs require that input signals transition between valid logic states quickly, as defined by the input transition time or rate in the *Recommended Operating Conditions* table. Failing to meet this specification will result in excessive power consumption and could cause oscillations. More details can be found in the *Implications of Slow or Floating CMOS Inputs* application report.

Do not leave inputs floating at any time during operation. Unused inputs must be terminated at V_{CC} or GND. If a system will not be actively driving an input at all times, then a pull-up or pull-down resistor can be added to provide a valid input voltage during these times. The resistor value will depend on multiple factors; however, a 10-kΩ resistor is recommended and will typically meet all requirements.

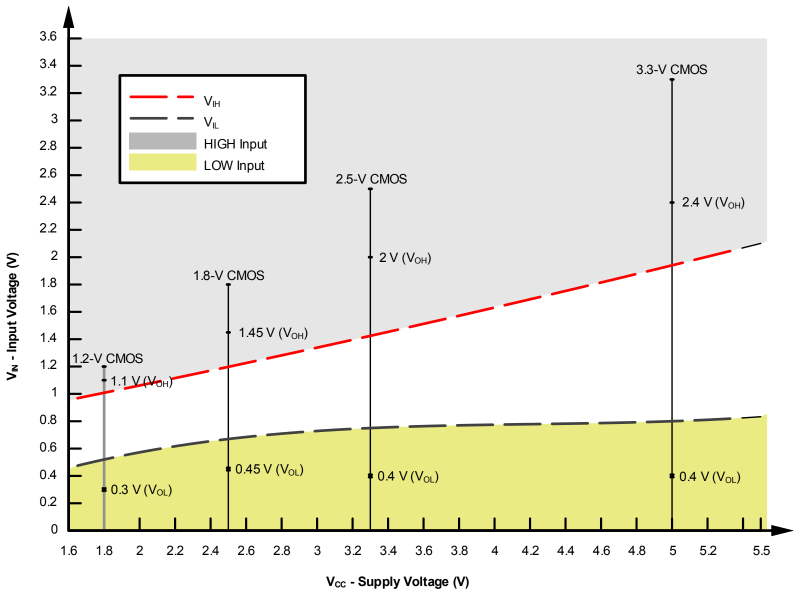


图 7-1. LVxT Input Voltage Levels

7.3.2.1 Down Translation

Signals can be translated down using the SN74LV1T86-Q1. The voltage applied at the V_{CC} will determine the output voltage and the input thresholds as described in the *Recommended Operating Conditions* and *Electrical Characteristics* tables.

When connected to a high-impedance input, the output voltage will be approximately V_{CC} in the HIGH state, and 0 V in the LOW state. As shown in 图 7-1, ensure that the input signals in the HIGH state are between $V_{IH(MIN)}$ and 5.5 V, and input signals in the LOW state are lower than $V_{IL(MAX)}$.

As shown in 图 7-2 for example, the standard CMOS inputs for devices operating at 5.0-V, 3.3-V or 2.5-V can be down-translated to match 1.8 V CMOS signals when operating from 1.8-V V_{CC}.

Down Translation Combinations are as follows:

- 1.8-V V_{CC} – Inputs from 2.5-V, 3.3-V, and 5.0-V
- 2.5-V V_{CC} – Inputs from 3.3-V and 5.0-V
- 3.3-V V_{CC} – Inputs from 5.0-V

7.3.2.2 Up Translation

Input signals can be up translated using the SN74LV1T86-Q1. The voltage applied at V_{CC} will determine the output voltage and the input thresholds as described in the *Recommended Operating Conditions* and *Electrical Characteristics* tables. When connected to a high-impedance input, the output voltage will be approximately V_{CC} in the HIGH state, and 0 V in the LOW state.

The inputs have reduced thresholds that allow for input HIGH state levels which are much lower than standard values. For example, standard CMOS inputs for a device operating at a 5-V supply will have a $V_{IH(MIN)}$ of 3.5 V. For the SN74LV1T86-Q1, $V_{IH(MIN)}$ with a 5-V supply is only 2 V, which would allow for up-translation from a typical 2.5-V to 5-V signals.

As shown in 图 7-2, ensure that the input signals in the HIGH state are above $V_{IH(MIN)}$ and input signals in the LOW state are lower than $V_{IL(MAX)}$.

Up Translation Combinations are as follows:

- 1.8-V V_{CC} – Inputs from 1.2-V
- 2.5-V V_{CC} – Inputs from 1.8-V

- 3.3-V V_{CC} – Inputs from 1.8- V and 2.5-V
- 5.0-V V_{CC} – Inputs from 2.5-V and 3.3-V

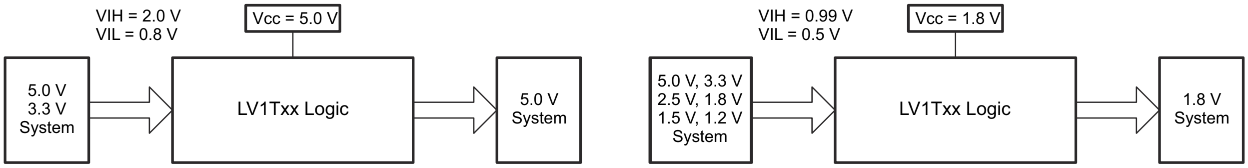


图 7-2. LVxT Up and Down Translation Example

7.3.3 Clamp Diode Structure

The outputs to this device have both positive and negative clamping diodes, and the inputs to this device have negative clamping diodes only as shown in 图 7-3.

> 小心
>
> Voltages beyond the values specified in the *Absolute Maximum Ratings* table can cause damage to the device. The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

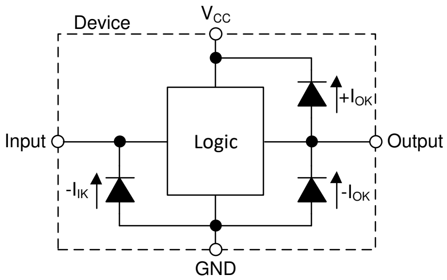


图 7-3. Electrical Placement of Clamping Diodes for Each Input and Output

7.4 Device Functional Modes

表 7-1 lists the functional modes of the SN74LV1T86-Q1.

表 7-1. Function Table

INPUTS(1)		OUTPUT Y
A	B	
L	L	L
L	H	H
H	L	H
H	H	L

(1) H = high voltage level, L = low voltage level, X = do not care, Z = high impedance

8 Application and Implementation

备注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

In this application, a 2-input XOR gate is used as a phase difference detector as shown in 图 8-1.

The SN74LV1T86-Q1 is used to identify phase difference between a reference clock and another input clock. Whenever the clock states are different, the XOR output will pulse HIGH until the clocks return to the same state. The output is fed into a low-pass filter to obtain a DC representation of the phase difference.

Typically, clock signals have fast transition rates, but additional filtering can be added to the clock signals which can lead to slower transitions rates. This makes the SN74LV1T86-Q1 an excellent choice for the application because it has Schmitt-trigger inputs that do not have input transition rate requirements.

8.2 Typical Application

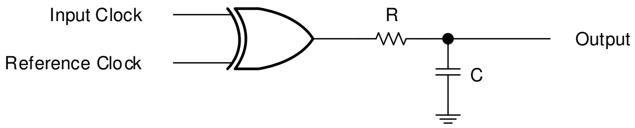


图 8-1. Typical Application Block Diagram

8.2.1 Design Requirements

8.2.1.1 Power Considerations

Ensure the desired supply voltage is within the range specified in the *Recommended Operating Conditions*. The supply voltage sets the electrical characteristics of the device as described in the *Electrical Characteristics* section.

The positive voltage supply must be capable of sourcing current equal to the total current to be sourced by all outputs of the SN74LV1T86-Q1 plus the maximum static supply current, I_{CC}, listed in the *Electrical Characteristics*, and any transient current required for switching. The logic device can only source as much current that is provided by the positive supply source. Be sure to not exceed the maximum total current through V_{CC} listed in the *Absolute Maximum Ratings*.

The ground must be capable of sinking current equal to the total current to be sunk by all outputs of the SN74LV1T86-Q1 plus the maximum supply current, I_{CC}, listed in the *Electrical Characteristics*, and any transient current required for switching. The logic device can only sink as much current that can be sunk into its ground connection. Be sure to not exceed the maximum total current through GND listed in the *Absolute Maximum Ratings*.

The SN74LV1T86-Q1 can drive a load with a total capacitance less than or equal to 50 pF while still meeting all of the data sheet specifications. Larger capacitive loads can be applied; however, it is not recommended to exceed 50 pF.

The SN74LV1T86-Q1 can drive a load with total resistance described by $R_L \geqslant V_O / I_O$, with the output voltage and current defined in the *Electrical Characteristics* table with V_{OH} and V_{OL}. When outputting in the HIGH state, the output voltage in the equation is defined as the difference between the measured output voltage and the supply voltage at the V_{CC} pin.

Total power consumption can be calculated using the information provided in the *CMOS Power Consumption and Cpd Calculation* application note.

Thermal increase can be calculated using the information provided in the *Thermal Characteristics of Standard Linear and Logic (SLL) Packages and Devices* application note.

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The maximum junction temperature, $T_{J(max)}$ listed in the *Absolute Maximum Ratings*, is an additional limitation to prevent damage to the device. Do not violate any values listed in the *Absolute Maximum Ratings*. These limits are provided to prevent damage to the device.

8.2.1.2 Input Considerations

Input signals must cross $V_{IL(max)}$ to be considered a logic LOW, and $V_{IH(min)}$ to be considered a logic HIGH. Do not exceed the maximum input voltage range found in the *Absolute Maximum Ratings*.

Unused inputs must be terminated to either V_{CC} or ground. The unused inputs can be directly terminated if the input is completely unused, or they can be connected with a pull-up or pull-down resistor if the input will be used sometimes, but not always. A pull-up resistor is used for a default state of HIGH, and a pull-down resistor is used for a default state of LOW. The drive current of the controller, leakage current into the SN74LV1T86-Q1 (as specified in the *Electrical Characteristics*), and the desired input transition rate limits the resistor size. A 10-kΩ resistor value is often used due to these factors.

The SN74LV1T86-Q1 has CMOS inputs and thus requires fast input transitions to operate correctly, as defined in the *Recommended Operating Conditions* table. Slow input transitions can cause oscillations, additional power consumption, and reduction in device reliability.

Refer to the *Feature Description* section for additional information regarding the inputs for this device.

8.2.1.3 Output Considerations

The positive supply voltage is used to produce the output HIGH voltage. Drawing current from the output will decrease the output voltage as specified by the V_{OH} specification in the *Electrical Characteristics*. The ground voltage is used to produce the output LOW voltage. Sinking current into the output will increase the output voltage as specified by the V_{OL} specification in the *Electrical Characteristics*.

Push-pull outputs that could be in opposite states, even for a very short time period, should never be connected directly together. This can cause excessive current and damage to the device.

Two channels within the same device with the same input signals can be connected in parallel for additional output drive strength.

Unused outputs can be left floating. Do not connect outputs directly to V_{CC} or ground.

Refer to the *Feature Description* section for additional information regarding the outputs for this device.

8.2.2 Detailed Design Procedure

1. Add a decoupling capacitor from V_{CC} to GND. The capacitor needs to be placed physically close to the device and electrically close to both the V_{CC} and GND pins. An example layout is shown in the *Layout* section.
2. Ensure the capacitive load at the output is ≤ 50 pF. This is not a hard limit; by design, however, it will optimize performance. This can be accomplished by providing short, appropriately sized traces from the SN74LV1T86-Q1 to one or more of the receiving devices.
3. Ensure the resistive load at the output is larger than $(V_{CC} / I_{O(max)})$ Ω. Doing this will not violate the maximum output current from the *Absolute Maximum Ratings*. Most CMOS inputs have a resistive load measured in MΩ; much larger than the minimum calculated previously.
4. Thermal issues are rarely a concern for logic gates; the power consumption and thermal increase, however, can be calculated using the steps provided in the application report, *CMOS Power Consumption and Cpd Calculation*.

8.2.3 Application Curves

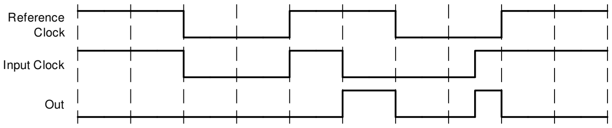

图 8-2. Application Timing Diagram

8.3 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in the *Recommended Operating Conditions*. Each V_{CC} terminal should have a good bypass capacitor to prevent power disturbance. A 0.1-μF capacitor is recommended for this device. It is acceptable to parallel multiple bypass capacitors to reject different frequencies of noise. The 0.1-μF and 1-μF capacitors are commonly used in parallel. The bypass capacitor should be installed as close to the power terminal as possible for best results, as shown in the following layout example.

8.4 Layout

8.4.1 Layout Guidelines

When using multiple-input and multiple-channel logic devices, inputs must never be left floating. In many cases, functions or parts of functions of digital logic devices are unused (for example, when only two inputs of a triple-input AND gate are used or only 3 of the 4 buffer gates are used). Such unused input pins must not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. All unused inputs of digital logic devices must be connected to a logic high or logic low voltage, as defined by the input voltage specifications, to prevent them from floating. The logic level that must be applied to any particular unused input depends on the function of the device. Generally, the inputs are tied to GND or V_{CC}, whichever makes more sense for the logic function or is more convenient.

8.4.2 Layout Example

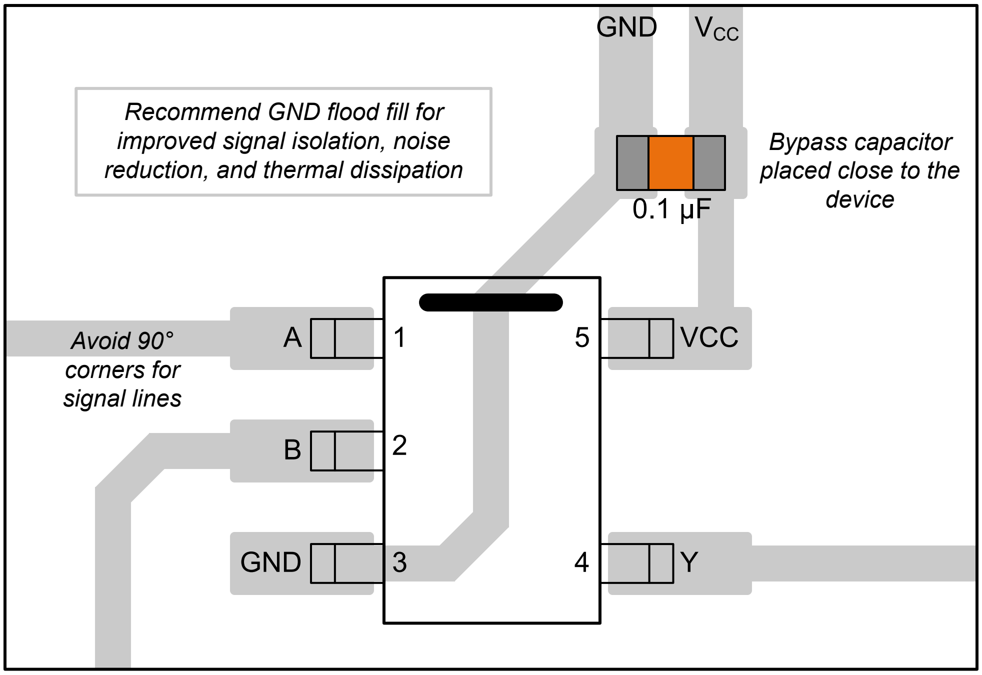

图 8-3. Example Layout for the SN74LV1T86-Q1

9 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

9.1 Documentation Support

9.1.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, *CMOS Power Consumption and Cpd Calculation* application note
- Texas Instruments, *Designing With Logic* application note
- Texas Instruments, *Thermal Characteristics of Standard Linear and Logic (SLL) Packages and Devices* application note
- Texas Instruments, *Implications of Slow or Floating CMOS Inputs* application note

9.2 接收文档更新通知

要接收文档更新通知，请导航至 ti.com 上的器件产品文件夹。点击*通知*进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

9.3 支持资源

TI E2E™ 中文支持论坛是工程师的重要参考资料，可直接从专家处获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题，获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的使用条款。

9.4 Trademarks

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9.5 静电放电警告

静电放电 (ESD) 会损坏这个集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

9.6 术语表

TI 术语表	本术语表列出并解释了术语、首字母缩略词和定义。

10 Revision History

Changes from Revision * (August 2023) to Revision A (January 2024) **Page**

- 向*封装信息*表中添加了 DBV 封装....................1
- Added DBV package to *Pin Configuration and Functions* section....................3
- Added thermal values for DBV package: RθJA = 278.0, RθJC(top) = 180.5, RθJB = 184.4, ΨJT = 115.4, ΨJB = 183.4, RθJC(bot) = N/A, all values in °C/W....................5

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74LV1T86QDBVRQ1	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	3BAH	Samples
SN74LV1T86QDCKRQ1	ACTIVE	SC70	DCK	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	1PO	Samples

[1] The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

[2] **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

[3] MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

[4] There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

[5] Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

[6] Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF SN74LV1T86-Q1 :

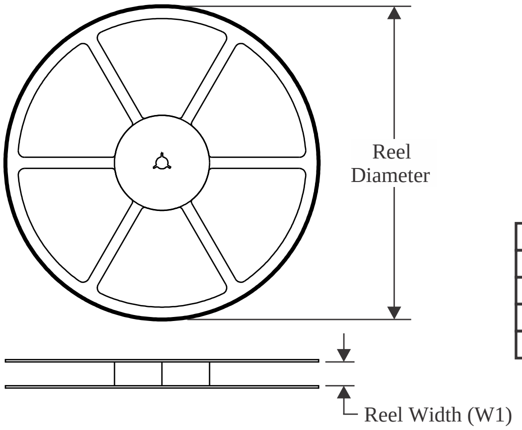
- Catalog : SN74LV1T86

NOTE: Qualified Version Definitions:

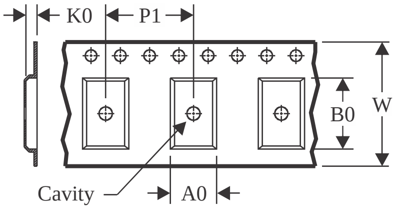
- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

REEL DIMENSIONS

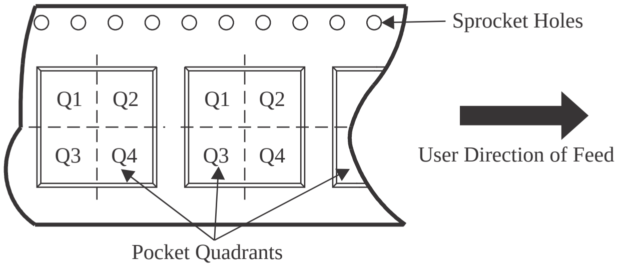


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

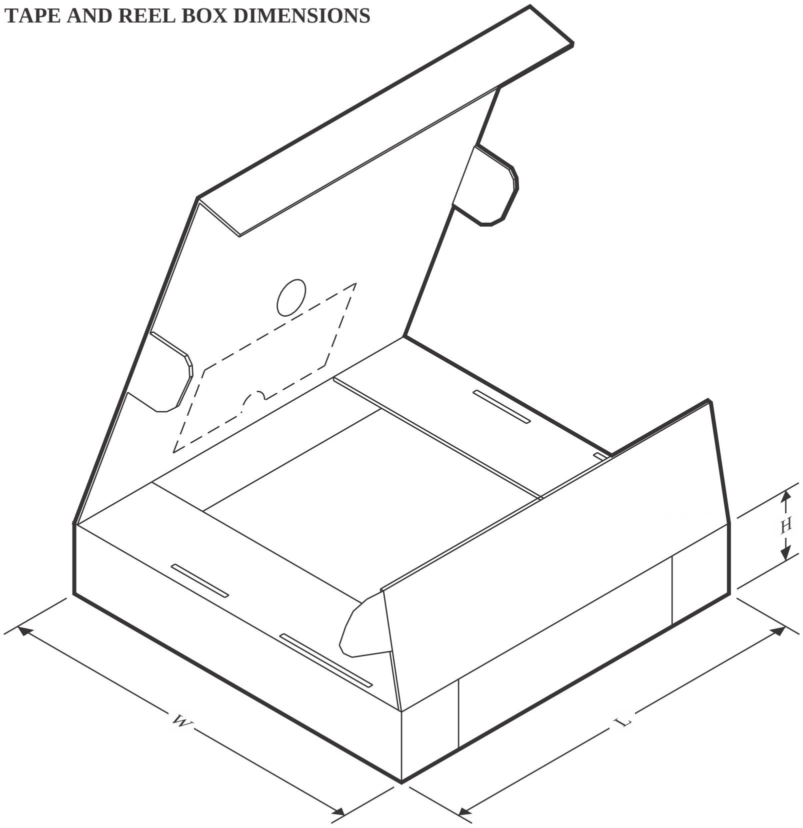
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

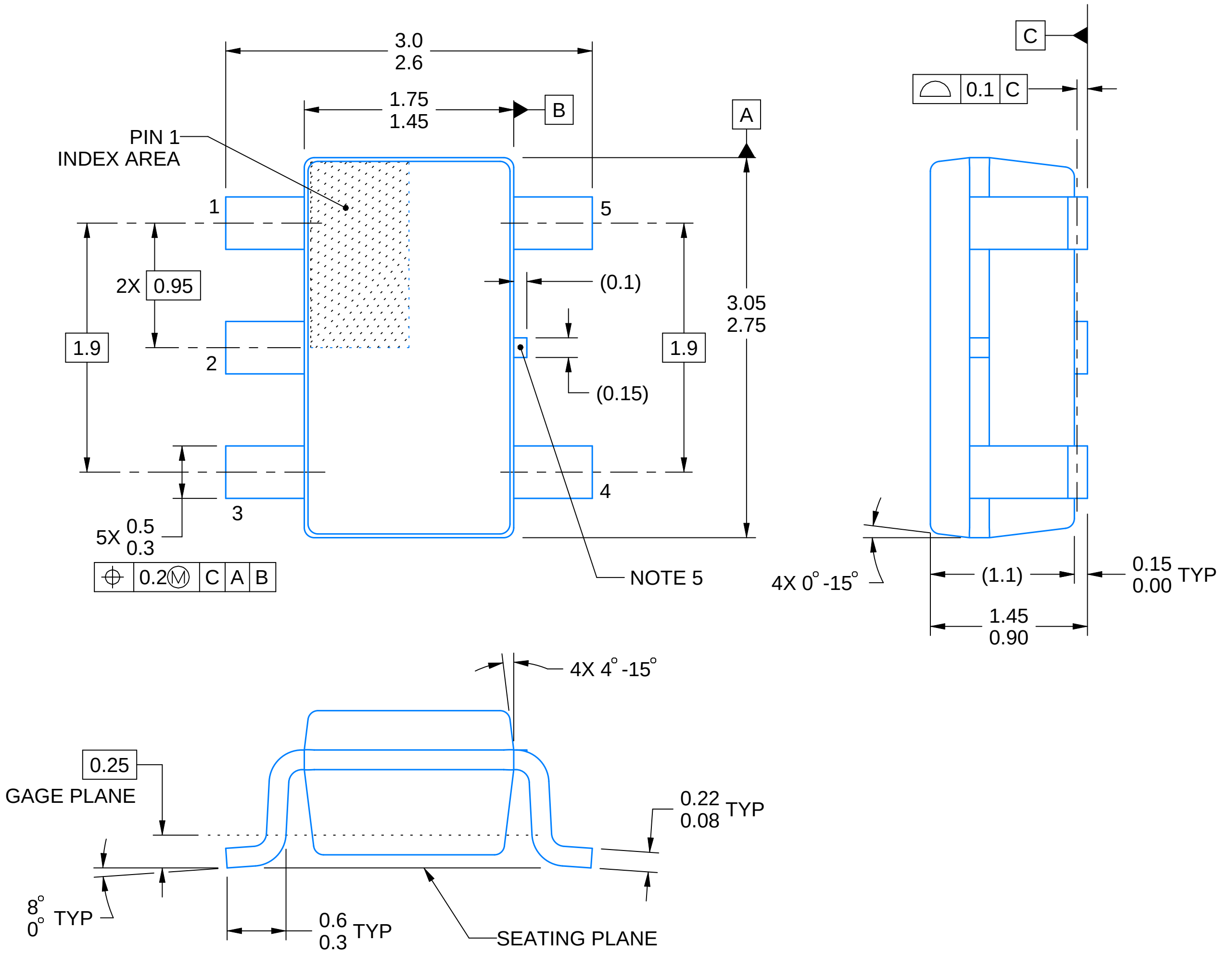
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LV1T86QDBVRQ1	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
SN74LV1T86QDCKRQ1	SC70	DCK	5	3000	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

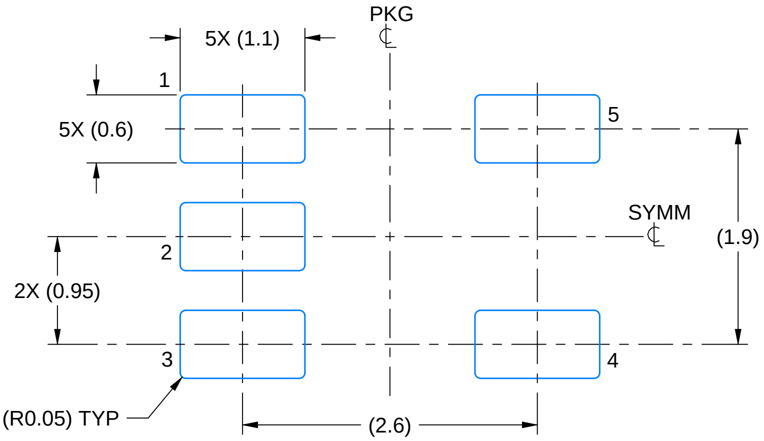
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LV1T86QDBVRQ1	SOT-23	DBV	5	3000	210.0	185.0	35.0
SN74LV1T86QDCKRQ1	SC70	DCK	5	3000	190.0	190.0	30.0



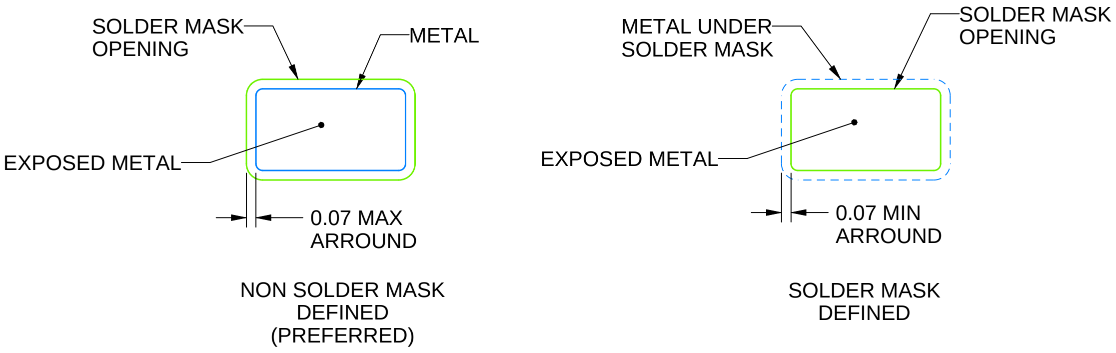
4214839/K 08/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.
5. Support pin may differ or may not be present.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



SOLDER MASK DETAILS

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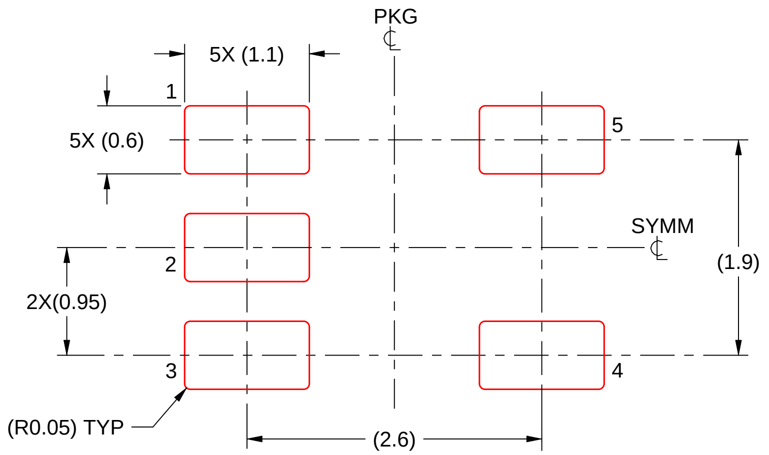
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214839/K 08/2024

NOTES: (continued)

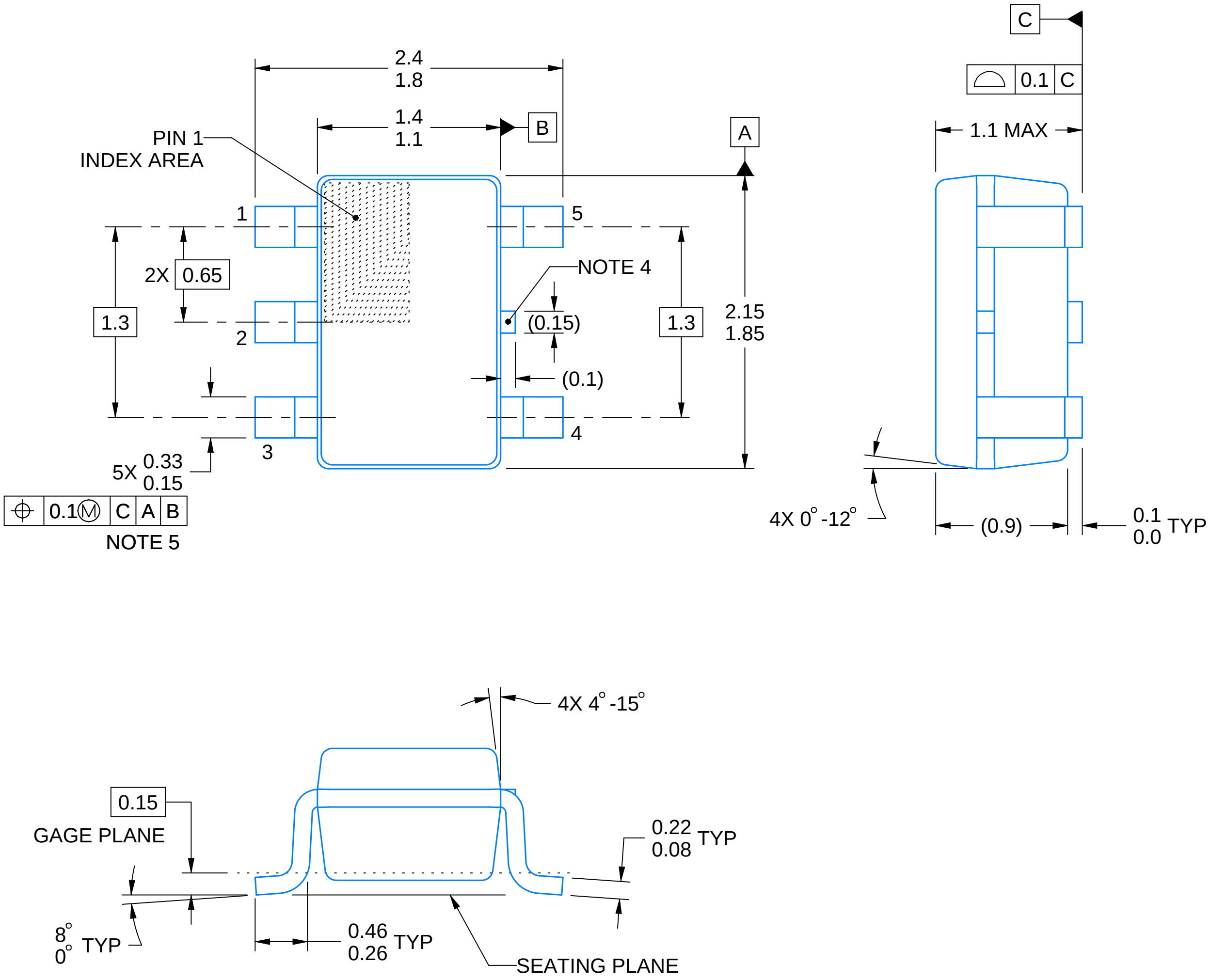
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

DCK0005A

PACKAGE OUTLINE

SOT - 1.1 max height

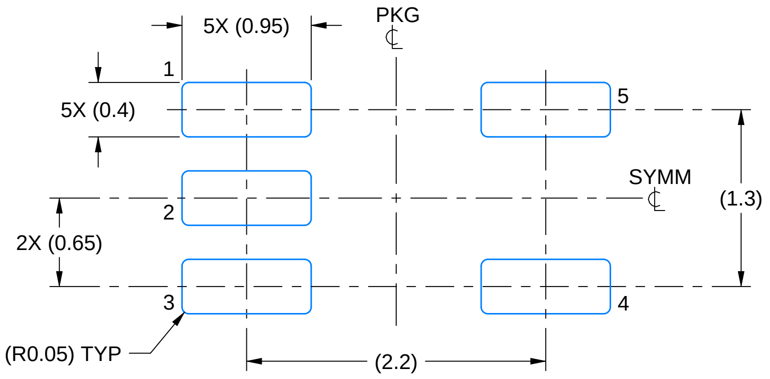
SMALL OUTLINE TRANSISTOR



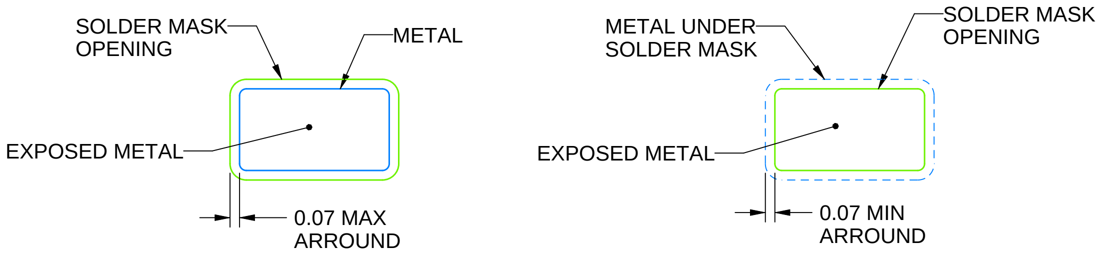
4214834/G 11/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-203.
4. Support pin may differ or may not be present.
5. Lead width does not comply with JEDEC.
6. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25mm per side



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:18X



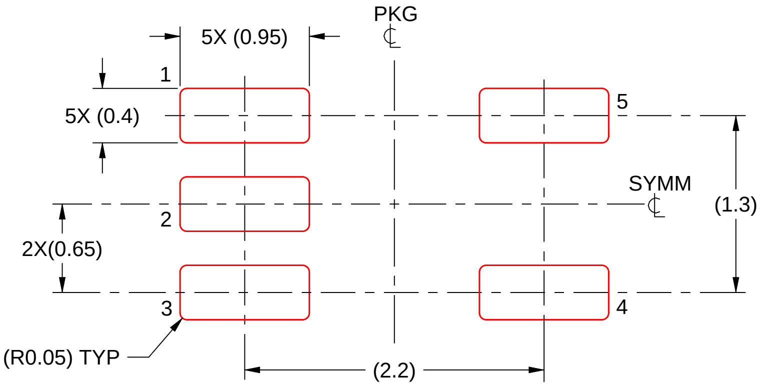
NON SOLDER MASK
DEFINED
(PREFERRED)

SOLDER MASK
DEFINED

SOLDER MASK DETAILS

NOTES: (continued)

7. Publication IPC-7351 may have alternate designs.
8. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 THICK STENCIL
SCALE:18X

NOTES: (continued)

9. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
10. Board assembly site may have different recommendations for stencil design.

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