

SN74LV4051A-Q1 汽车级 8 通道模拟多路复用器或多路解复用器

1 特性

- 符合汽车应用要求
- 具有符合 AEC-Q100 标准的下列特性：
 - 器件温度等级 1：-40°C 至 +125°C 环境温度范围
 - 器件 HBM ESD 分类等级 2
 - 器件 CDM ESD 分类等级 C4B
- 1.65V 至 5.5V V_{CC} 运行
- 所有端口上均支持以混合模式电压运行
- 高开关输出电压比
- 低开关串扰
- 单独的开关控制
- 极低输入电流
- 闩锁性能超过 100mA，符合 JESD 78 II 类规范

2 应用

- 汽车信息娱乐系统与仪表盘
- 远程信息处理、eCall

3 说明

这款 8 通道 CMOS 模拟多路复用器和多路解复用器可在 1.65V 至 5.5V V_{CC} 电压下运行。

SN74LV4051A-Q1 能够处理模拟和数字信号。每个通道允许在任意方向传输振幅高达 5.5V（峰值）的信号。

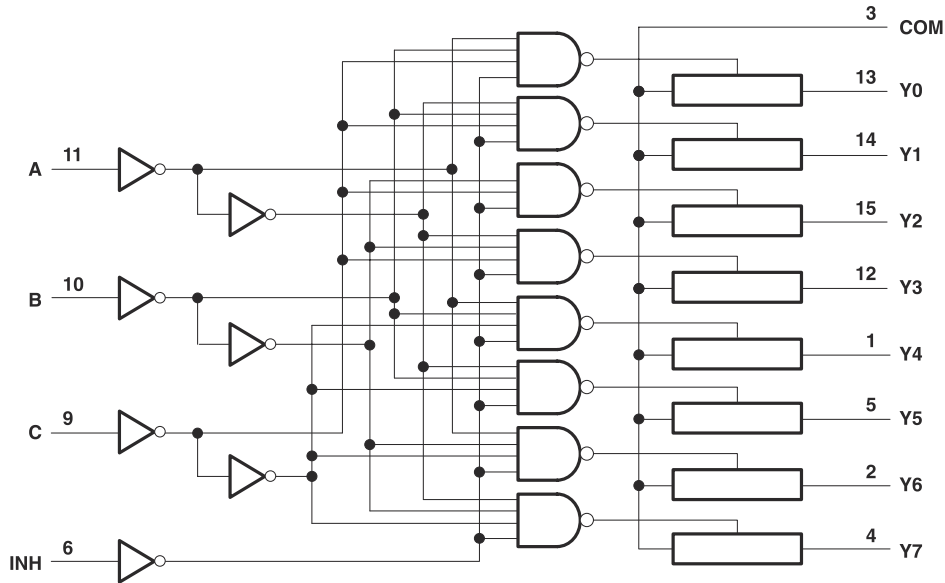
应用包括用于模数和数模转换系统的信号选通、斩波、调制/解调（调制解调器）以及信号多路复用。

封装信息

器件型号	封装 ⁽¹⁾	封装尺寸 ⁽²⁾
SN74LV4051A-Q1	PW (TSSOP , 16)	5mm × 6.4mm
	D (SOIC , 16)	9.9mm × 6mm
	DYY (SOT-23-THIN , 16)	4.2mm × 3.26mm

(1) 有关更多信息，请参阅节 11。

(2) 封装尺寸（长 × 宽）为标称值，并包括引脚（如适用）。



逻辑图（正逻辑）



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4 Pin Configuration and Functions

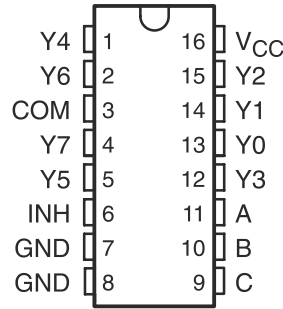


图 4-1. D, PW or DYY Package, 16-Pin SOIC, TSSOP, or SOT-23-THIN (Top View)

表 4-1. Pin Functions

PIN		TYPE ⁽¹⁾	DESCRIPTION
NAME	NO.		
Y4	1	I ⁽²⁾	Input to mux
Y6	2	I ⁽²⁾	Input to mux
COM	3	O ⁽²⁾	Output of mux
Y7	4	I ⁽²⁾	Input to mux
Y5	5	I ⁽²⁾	Input to mux
INH	6	I ⁽²⁾	Enables the outputs of the device. Logic low level will turn the outputs on, high level will turn them off.
GND	7	—	Ground
GND	8	—	Ground
C	9	I	Selector line for outputs (see § 7.4 for specific information)
B	10	I	Selector line for outputs (see § 7.4 for specific information)
A	11	I	Selector line for outputs (see § 7.4 for specific information)
Y3	12	I ⁽²⁾	Input to mux
Y0	13	I ⁽²⁾	Input to mux
Y1	14	I ⁽²⁾	Input to mux
Y2	15	I ⁽²⁾	Input to mux
Vcc	16	I	Device power input

(1) I = input, O = output

(2) These I/O descriptions represent the device when used as a multiplexer, when this device is operated as a demultiplexer pins Y0-Y7 may be considered outputs (O) and the COM pin may be considered inputs (I).

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾ ⁽³⁾

		MIN	MAX	UNIT
V_{CC}	Supply voltage	- 0.5	7.0	V
V_I	Logic input voltage range	- 0.5	7.0	V
V_{IO}	Switch I/O voltage range ⁽²⁾ ⁽³⁾	- 0.5	$V_{CC} + 0.5$	V
I_{IK}	Input clamp current	$V_I < 0$		mA
I_{IOK}	Switch IO diode clamp current	$V_{IO} < 0$ or $V_{IO} > V_{CC}$	50	mA
I_T	Switch continuous current	$V_{IO} = 0$ to V_{CC}	± 25	mA
	Continuous current through V_{CC} or GND		± 50	mA
T_{stg}	Storage temperature	- 65	150	°C

- (1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. Absolute maximum ratings do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If briefly operating outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not sustain damage, but it may not be fully functional. Operating the device in this manner may affect device reliability, functionality, performance, and shorten the device lifetime.
- (2) Pins are diode-clamped to the power-supply rails. Over voltage signals must be voltage and current limited to maximum ratings.
- (3) This value is limited to 5.5 V maximum

5.2 ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per AEC Q100-002 ⁽¹⁾	All pins	± 2000	V
$V_{(ESD)}$	Electrostatic discharge	Charged device model (CDM), per AEC Q100-011	All pins	± 500	V

- (1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

5.3 Thermal Information: SN74LV4051A-Q1

THERMAL METRIC ⁽¹⁾		SN74LV4051A-Q1	SN74LV4051A-Q1	UNIT
		PW (TSSOP)	DYY (SOT)	
		16 PINS	16 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	140.2	199.7	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	72.6	121.2	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	98.7	129.0	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	13.4	24.6	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	97.3	126.7	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

5.4 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

		MIN	NOM	MAX	UNIT
V _{CC}	Supply voltage	1 ⁽²⁾		5.5	V
V _{IH}	High-level input voltage, logic control inputs	V _{CC} = 1.65		5.5	V
		V _{CC} = 2 V	1.5	5.5	
		V _{CC} = 2.3 V to 2.7 V	V _{CC} × 0.7	5.5	
		V _{CC} = 3 V to 3.6 V	V _{CC} × 0.7	5.5	
		V _{CC} = 4.5 V to 5.5 V	V _{CC} × 0.7	5.5	
V _{IL}	Low-level input voltage, logic control inputs	V _{CC} = 1.65 V	0	0.4	V
		V _{CC} = 2	0	0.5	
		V _{CC} = 2.3V to 2.7V	0	V _{CC} × 0.3	
		V _{CC} = 3 V to 3.6 V	0	V _{CC} × 0.3	
		V _{CC} = 4.5 V to 5.5 V	0	V _{CC} × 0.3	
V _I	Logic control input voltage	0		5.5	V
V _{IO}	Switch input or output voltage	0		V _{CC}	V
Δt/ΔV	Logic input transition rise or fall rate	V _{CC} = 1.0 V to 2.0 V		500	ns/V
		V _{CC} = 2.0 V to 2.7 V		200	
		V _{CC} = 3 V to 3.6 V		100	
		V _{CC} = 4.5 V to 5.5 V		20	
T _A	Ambient temperature	- 40		125	°C

(1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to TI application report *Implications of Slow or Floating CMOS Inputs*, SCBA004.

(2) When using a V_{CC} of ≤1.2 V, it is recommended to use these devices only for transmitting digital signals. When supply voltage is near 1.2 V the analog switch ON resistance becomes very non-linear

5.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		Condition	T _A	V _{CC}	MIN	TYP	MAX	UNIT	
r _{ON}	ON-state switch resistance	I _T = 2 mA, V _I = V _{CC} or GND, V _{INH} = V _{IL}	25°C	1.65 V		60	150	Ω	
			- 40°C to 85°C			225			
			- 40°C to 125°C			225			
			25°C	2.3 V			38		180
			- 40°C to 85°C			225			
			- 40°C to 125°C			225			
			25°C	3 V			30		150
			- 40°C to 85°C			190			
			- 40°C to 125°C			190			
			25°C	4.5 V			22		75
			- 40°C to 85°C			100			
			- 40°C to 125°C			100			

5.5 Electrical Characteristics (续)

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	Condition	T _A	V _{CC}	MIN	TYP	MAX	UNIT
r _{ON(p)}	Peak ON-state resistance I _T = 2 mA, V _I = GND to V _{CC} , V _{INH} = V _{IL}	25°C	1.65 V		220	600	Ω
		-40°C to 85°C				700	
		-40°C to 125°C				700	
		25°C	2.3 V		113	500	
		-40°C to 85°C				600	
		-40°C to 125°C				600	
		25°C	3 V		54	180	
		-40°C to 85°C				225	
		-40°C to 125°C				225	
		25°C	4.5 V		31	100	
		-40°C to 85°C				125	
		-40°C to 125°C				125	
Δr _{ON}	Difference in ON-state resistance between switches I _T = 2 mA, V _I = GND to V _{CC} , V _{INH} = V _{IL}	25°C	1.65 V		3	40	Ω
		-40°C to 85°C				40	
		-40°C to 125°C				40	
		25°C	2.3 V		2.1	30	
		-40°C to 85°C				40	
		-40°C to 125°C				40	
		25°C	3 V		1.4	20	
		-40°C to 85°C				30	
		-40°C to 125°C				30	
		25°C	4.5 V		1.3	15	
		-40°C to 85°C				20	
		-40°C to 125°C				20	
I _{IH} I _{IL}	Control input current V _I = 5.5 V or GND	25°C	0 to 5.5 V	-0.1		0.1	μA
		-40°C to 85°C		-1		1	
		-40°C to 125°C		-2		2	
I _{S(off)}	OFF-state switch leakage current V _I = V _{CC} and V _O = GND, or V _I = GND and V _O = V _{CC} , V _{INH} = V _{IH}	25°C	5.5 V	-0.1		0.1	μA
		-40°C to 85°C		-1		1	
		-40°C to 125°C		-2		2	
I _{S(on)}	ON-state switch leakage current V _I = V _{CC} or GND, V _{INH} = V _{IL}	25°C	5.5 V	-0.1		0.1	μA
		-40°C to 85°C		-1		1	
		-40°C to 125°C		-2		2	
I _{CC}	Supply current V _I = V _{CC} or GND V _{INH} = 0 V	25°C	5.5 V		0.01		μA
		-40°C to 85°C				20	
		-40°C to 125°C				40	
C _{IC}	Control input capacitance f = 10 MHz	25°C	3.3 V		2		pF
C _{IS}	Common terminal capacitance f = 10 MHz	25°C	3.3 V		23.4		pF
C _{OS}	Switch terminal capacitance f = 10 MHz	25°C	3.3 V		5.7		pF

5.5 Electrical Characteristics (续)

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		Condition	T _A	V _{CC}	MIN	TYP	MAX	UNIT
C _F	Feedthrough capacitance	f = 10 MHz	25°C	3.3 V		0.5		pF
C _{PD}	Power dissipation capacitance	C _L = 50 pF, f = 10 MHz	25°C	3.3 V		5.9		pF

5.6 Timing Characteristics V_{CC} = 2.5 V ± 0.2 V

PARAMETER		FROM (INPUT)	TO (OUTPUT)	CONDITIONS	T _A	MIN	TYP	MAX	UNIT
t _{PLH} t _{PHL}	Propagation delay time	COM or Yn	Yn or COM	C _L = 15 pF	25°C		1.9	10	ns
					-40°C to 85°C			16	
					-40°C to 125°C			18	
t _{PZH} t _{PZL}	Enable delay time	INH	COM or Yn	C _L = 15 pF	25°C		6.6	18	ns
					-40°C to 85°C			23	
					-40°C to 125°C			25	
t _{PHZ} t _{PLZ}	Disable delay time	INH	COM or Yn	C _L = 15 pF	25°C		7.4	18	ns
					-40°C to 85°C			23	
					-40°C to 125°C			25	
t _{PLH} t _{PHL}	Propagation delay time	COM or Yn	Yn or COM	C _L = 50 pF	25°C		3.8	12	ns
					-40°C to 85°C			18	
					-40°C to 125°C			20	
t _{PZH} t _{PZL}	Enable delay time	INH	COM or Yn	C _L = 50 pF	25°C		7.8	28	ns
					-40°C to 85°C			35	
					-40°C to 125°C			35	
t _{PHZ} t _{PLZ}	Disable delay time	INH	COM or Yn	C _L = 50 pF	25°C		11.5	28	ns
					-40°C to 85°C			35	
					-40°C to 125°C			35	

5.7 Timing Characteristics V_{CC} = 3.3 V ± 0.3 V

PARAMETER		FROM (INPUT)	TO (OUTPUT)	CONDITIONS	T _A	MIN	TYP	MAX	UNIT
t _{PLH} t _{PHL}	Propagation delay time	COM or Yn	Yn or COM	C _L = 50 pF	25°C		2.5	9	ns
					-40°C to 85°C			12	
					-40°C to 125°C			14	
t _{PZH} t _{PZL}	Enable delay time	INH	COM or Yn	C _L = 50 pF	25°C		5.5	20	ns
					-40°C to 85°C			25	
					-40°C to 125°C			25	
t _{PHZ} t _{PLZ}	Disable delay time	INH	COM or Yn	C _L = 50 pF	25°C		8.8	20	ns
					-40°C to 85°C			25	
					-40°C to 125°C			25	

5.8 Timing Characteristics $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$

PARAMETER		FROM (INPUT)	TO (OUTPUT)	CONDITIONS	T_A	MIN	TYP	MAX	UNIT
t_{PLH} t_{PHL}	Propagation delay time	COM or Yn	Yn or COM	$C_L = 50\text{ pF}$	25°C	1.5	6	ns	
					-40°C to 85°C		8		
					-40°C to 125°C		10		
t_{PZH} t_{PZL}	Enable delay time	INH	COM or Yn	$C_L = 50\text{ pF}$	25°C	4	14	ns	
					-40°C to 85°C		18		
					-40°C to 125°C		18		
t_{PHZ} t_{PLZ}	Disable delay time	INH	COM or Yn	$C_L = 50\text{ pF}$	25°C	6.2	14	ns	
					-40°C to 85°C		18		
					-40°C to 125°C		18		

5.9 AC Characteristics

PARAMETER	FROM (INPUT)	TO (OUTPUT)	Device	CONDITIONS	MIN	TYP	MAX	UNIT
Frequency response (switch on)	COM or Yn	Yn or COM	SN74LV4051	$C_L = 50\text{ pF}$, $R_L = 600\ \Omega$, $F_{in} = 1\text{ MHz}$ (sine wave)	$V_{CC} = 2.3\text{ V}$	20	MHz	
					$V_{CC} = 3\text{ V}$	25		
					$V_{CC} = 4.5\text{ V}$	35		
Feedthrough attenuation (switch off)	COM or Yn	Yn or COM	ALL	$C_L = 50\text{ pF}$, $R_L = 600\ \Omega$, $F_{in} = 1\text{ MHz}$ (sine wave)	$V_{CC} = 2.3\text{ V}$	-45	dB	
					$V_{CC} = 3\text{ V}$	-45		
					$V_{CC} = 4.5\text{ V}$	-45		
Crosstalk (between any switches)	COM or Yn	Yn or COM	ALL	$C_L = 50\text{ pF}$, $R_L = 600\ \Omega$, $F_{in} = 1\text{ MHz}$ (sine wave)	$V_{CC} = 2.3\text{ V}$	20	mV	
					$V_{CC} = 3\text{ V}$	35		
					$V_{CC} = 4.5\text{ V}$	60		
Sine-wave distortion	COM or Yn	Yn or COM	ALL	$C_L = 50\text{ pF}$, $R_L = 10\text{ k}\Omega$, $F_{in} = 1\text{ kHz}$ (sine wave)	$V_I = 2\text{ V}_{p-p}$, $V_{CC} = 2.3\text{ V}$	0.1	%	
					$V_I = 2.5\text{ V}_{p-p}$, $V_{CC} = 3\text{ V}$	0.1		
					$V_I = 4\text{ V}_{p-p}$, $V_{CC} = 4.5\text{ V}$	0.1		

6 Parameter Measurement Information

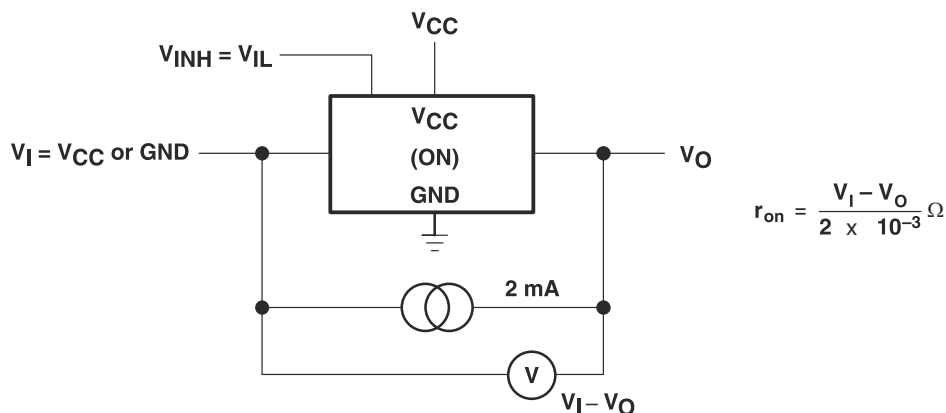


图 6-1. On-State Resistance Test Circuit

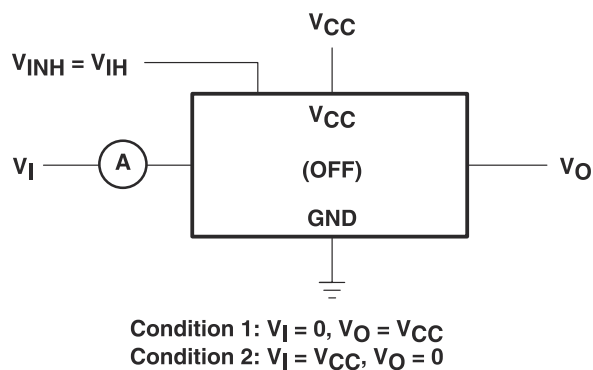


图 6-2. Off-State Switch Leakage-Current Test Circuit

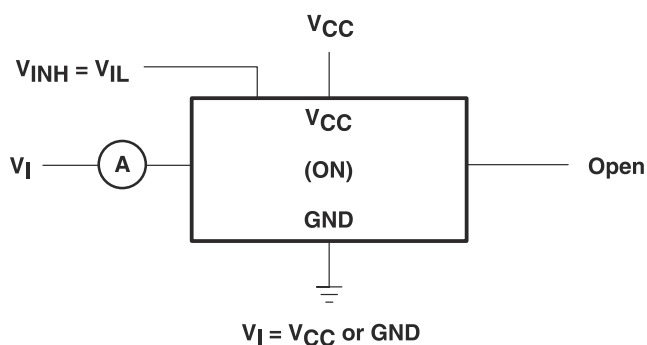


图 6-3. On-State Switch Leakage-Current Test Circuit

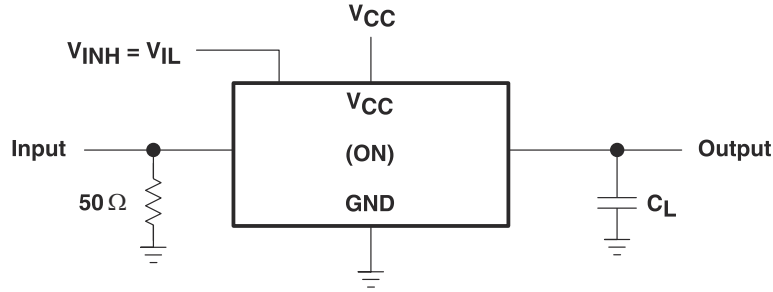
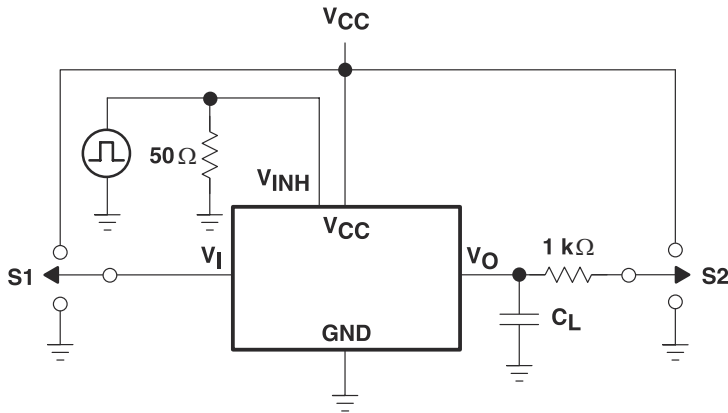


图 6-4. Propagation Delay Time, Signal Input to Signal Output



TEST	S1	S2
t_{PLZ}/t_{PZL}	GND	V_{CC}
t_{PHZ}/t_{PZH}	V_{CC}	GND

TEST CIRCUIT

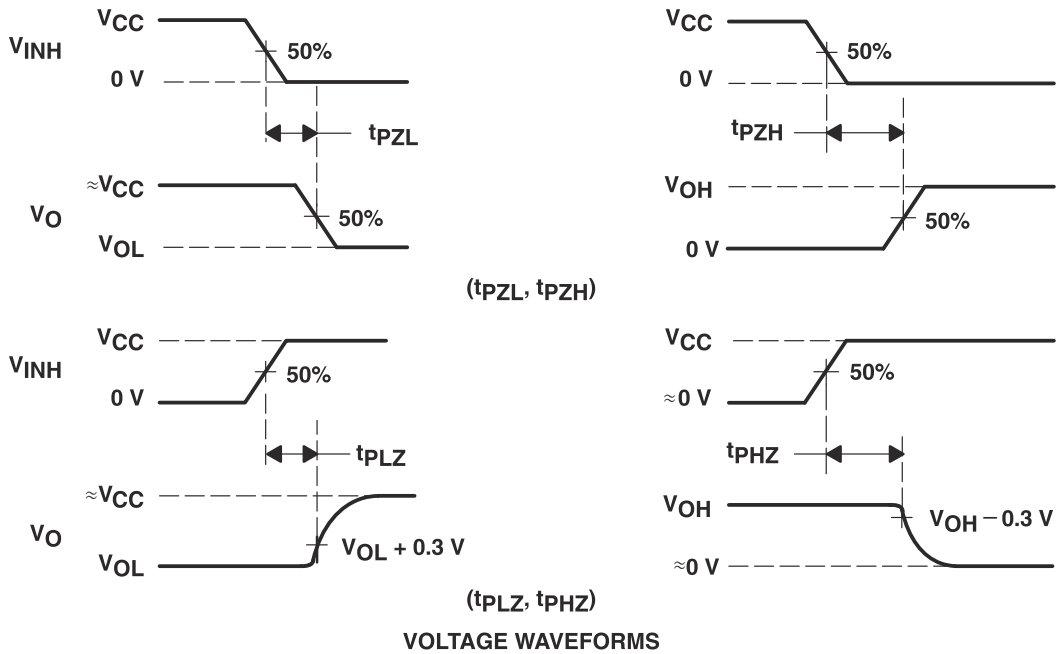
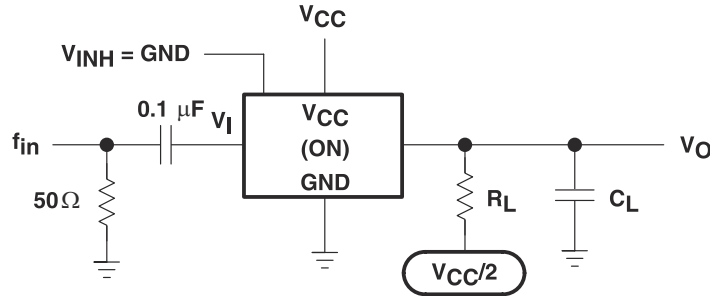


图 6-5. Switching Time (t_{PZL} , t_{PLZ} , t_{PZH} , t_{PHZ}), Control to Signal Output



NOTE A: f_{in} is a sine wave.

图 6-6. Frequency Response (Switch On)

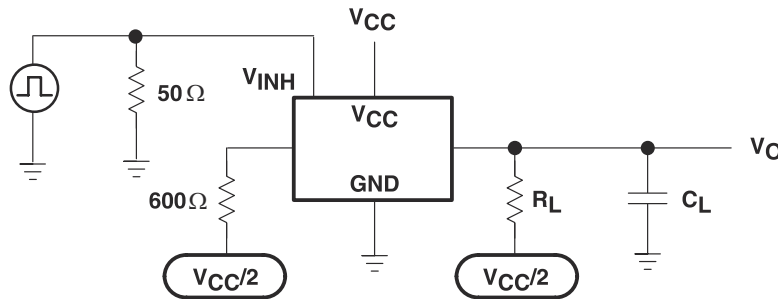


图 6-7. Crosstalk (Control Input, Switch Output)

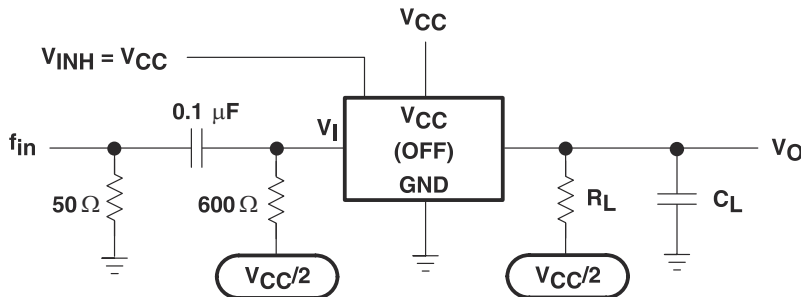


图 6-8. Feedthrough Attenuation (Switch Off)

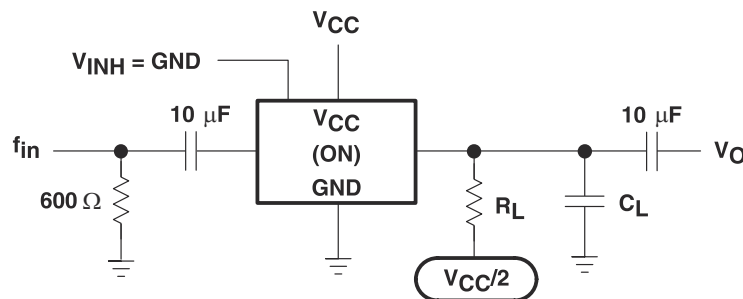


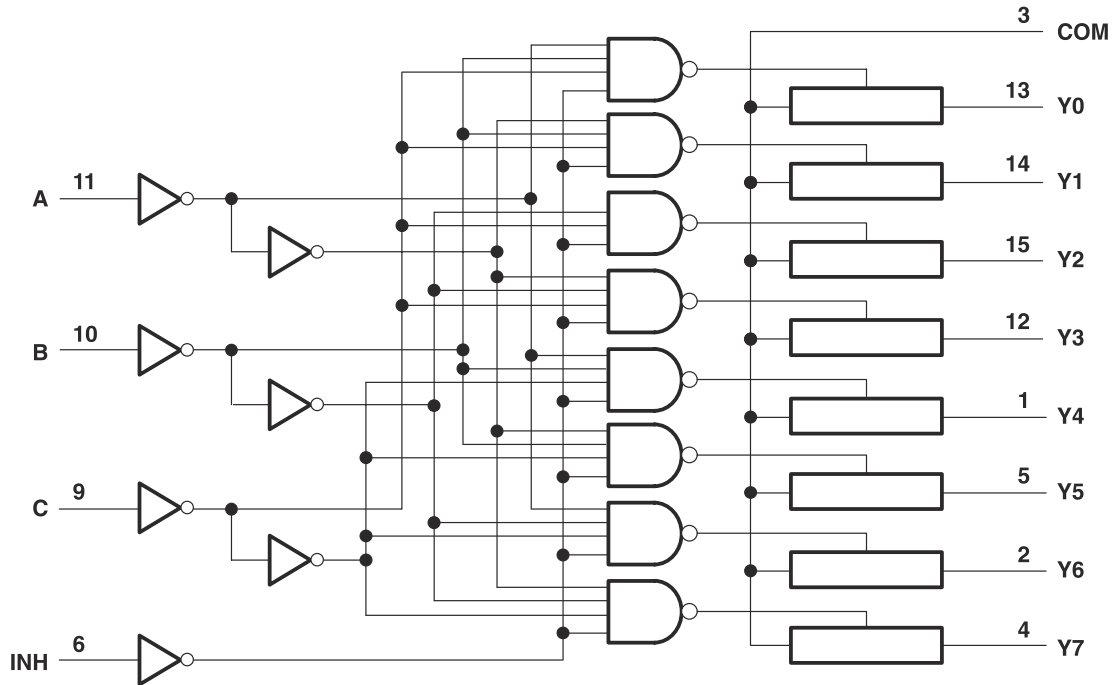
图 6-9. Sine-Wave Distortion

7 Detailed Description

7.1 Overview

This device is an 8-channel analog multiplexer. A multiplexer is used when several signals must share the same device or resource. This device allows the selection of one of these signals at a time, for analysis or propagation.

7.2 Functional Block Diagram



7.3 Feature Description

This device contains one 8-channel multiplexer for use in a variety of applications, and can also be configured as demultiplexer by using the COM pin as an input and the Yx pins as outputs. This device is qualified for automotive applications and has an extended temperature range of -40°C to 125°C (maximum depends on package type).

7.4 Device Functional Modes

表 7-1. Function Table

INPUTS				ON CHANNEL
INH	C	B	A	
L	L	L	L	Y0
L	L	L	H	Y1
L	L	H	L	Y2
L	L	H	H	Y3
L	H	L	L	Y4
L	H	L	H	Y5
L	H	H	L	Y6
L	H	H	H	Y7
H	X	X	X	None

8 Application and Implementation

备注

以下应用部分中的信息不属于 TI 器件规格的范围，TI 不担保其准确性和完整性。TI 的客户应负责确定器件是否适用于其应用。客户应验证并测试其设计，以确保系统功能。

8.1 Application Information

A multiplexer is used in applications where multiple signals share a resource. In the example below, several different sensors are connected to the analog-to-digital converter (ADC) of a microcontroller unit (MCU).

8.2 Typical Application

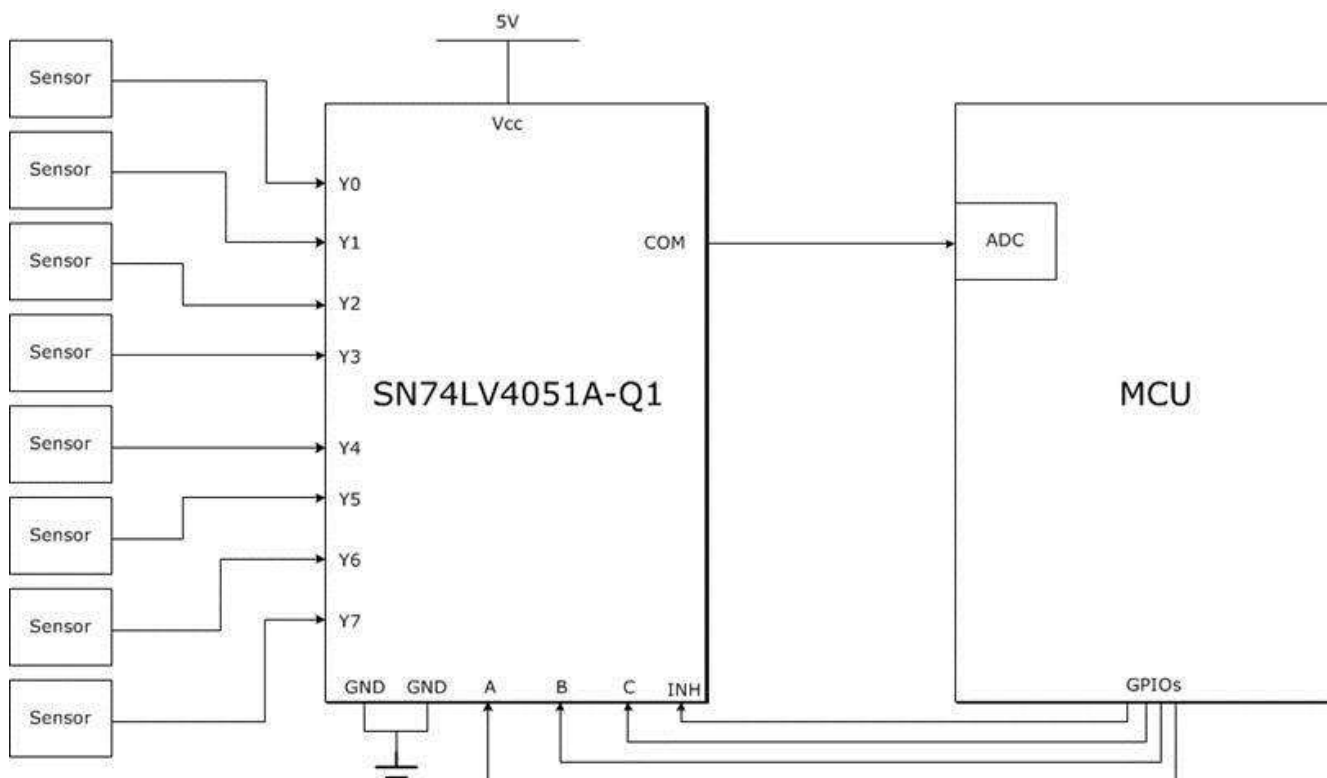


图 8-1. Example of Multiplexer Use With Analog Sensors and the ADC of an MCU

8.2.1 Design Requirements

Designing with the SN74LV4051A-Q1 device requires a stable input voltage between 2 V (see *Recommended Operating Conditions* for details) and 5.5V. Another important design consideration are the characteristics of the signal being multiplexed—ensure no important information is lost due to timing or incompatibility with this device.

8.2.2 Detailed Design Procedure

Processing eight different analog signals would normally require eight separate ADCs, but 图 8-1 shows how to achieve this using only one ADC and four GPIOs (general-purpose input/outputs).

8.3 Power Supply Recommendations

Most systems have a common 3.3V or 5V rail that can supply the Vcc pin of this device. If this is not available, a switched-mode power supply (SMPS) or a low dropout regulator (LDO) can supply this device from a higher voltage rail.

8.4 Layout

8.4.1 Layout Guidelines

TI recommends keeping the signal lines as short and as straight as possible. Incorporation of microstrip or stripline techniques is also recommended when signal lines are more than 1 inch long. These traces must be designed with a characteristic impedance of either 50Ω or 75Ω , as required by the application. Do not place this device too close to high-voltage switching components, as they may cause interference.

8.4.2 Layout Example

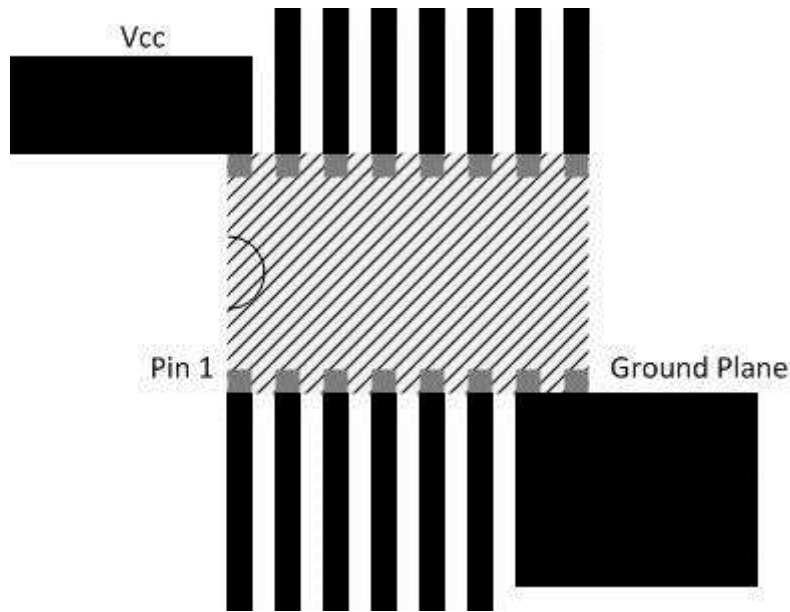


图 8-2. Layout Schematic

9 Device and Documentation Support

9.1 接收文档更新通知

要接收文档更新通知，请导航至 [ti.com](https://www.ti.com) 上的器件产品文件夹。点击 [通知](#) 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

9.2 支持资源

[TI E2E™ 中文支持论坛](#) 是工程师的重要参考资料，可直接从专家处获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题，获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的 [使用条款](#)。

9.3 Trademarks

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9.4 静电放电警告



静电放电 (ESD) 会损坏这个集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

9.5 术语表

[TI 术语表](#) 本术语表列出并解释了术语、首字母缩略词和定义。

10 Revision History

注：以前版本的页码可能与当前版本的页码不同

Changes from Revision G (September 2024) to Revision H (October 2024)	Page
• Added 50mA to the Switch IO diode clamp current.....	4

Changes from Revision F (June 2024) to Revision G (September 2024)	Page
• 添加了 DYY 封装和尺寸.....	1
• Added DYY package.....	3
• Added new VIH and VIL Specifications at 1.65V Vcc.....	6

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
CLV4051ATDWRG4Q1	NRND	SOIC	DW	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 105	L4051AQ	
CLV4051ATPWRG4Q1	OBSOLETE	TSSOP	PW	16		TBD	Call TI	Call TI	-40 to 105	L4051AQ	
SN74LV4051AQDYRQ1	ACTIVE	SOT-23-THIN	DYY	16	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LV4051Q	Samples
SN74LV4051AQPWRQ1	ACTIVE	TSSOP	PW	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	4051AQ1	Samples
SN74LV4051ATDRQ1	NRND	SOIC	D	16	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 105	L4051AQ	
SN74LV4051ATDWRQ1	NRND	SOIC	DW	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 105	L4051AQ	
SN74LV4051ATPWRQ1	ACTIVE	TSSOP	PW	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 105	L4051AQ	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF SN74LV4051A-Q1 :

- Catalog : [SN74LV4051A](#)
- Enhanced Product : [SN74LV4051A-EP](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Enhanced Product - Supports Defense, Aerospace and Medical Applications

TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CLV4051ATDWRG4Q1	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1
SN74LV4051AQDYRQ1	SOT-23-THIN	DYY	16	3000	330.0	12.4	4.8	3.6	1.6	8.0	12.0	Q3
SN74LV4051AQPWRQ1	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74LV4051ATDWRQ1	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1
SN74LV4051ATPWRQ1	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CLV4051ATDWRG4Q1	SOIC	DW	16	2000	350.0	350.0	43.0
SN74LV4051AQDYRQ1	SOT-23-THIN	DYY	16	3000	336.6	336.6	31.8
SN74LV4051AQPWRQ1	TSSOP	PW	16	2000	356.0	356.0	35.0
SN74LV4051ATDWRQ1	SOIC	DW	16	2000	350.0	350.0	43.0
SN74LV4051ATPWRQ1	TSSOP	PW	16	2000	356.0	356.0	35.0

D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
 - D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
 - E. Reference JEDEC MS-012 variation AC.



4220204/A 02/2017

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

EXAMPLE BOARD LAYOUT

PW0016A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



SOLDER MASK DETAILS

4220204/A 02/2017

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

PW0016A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

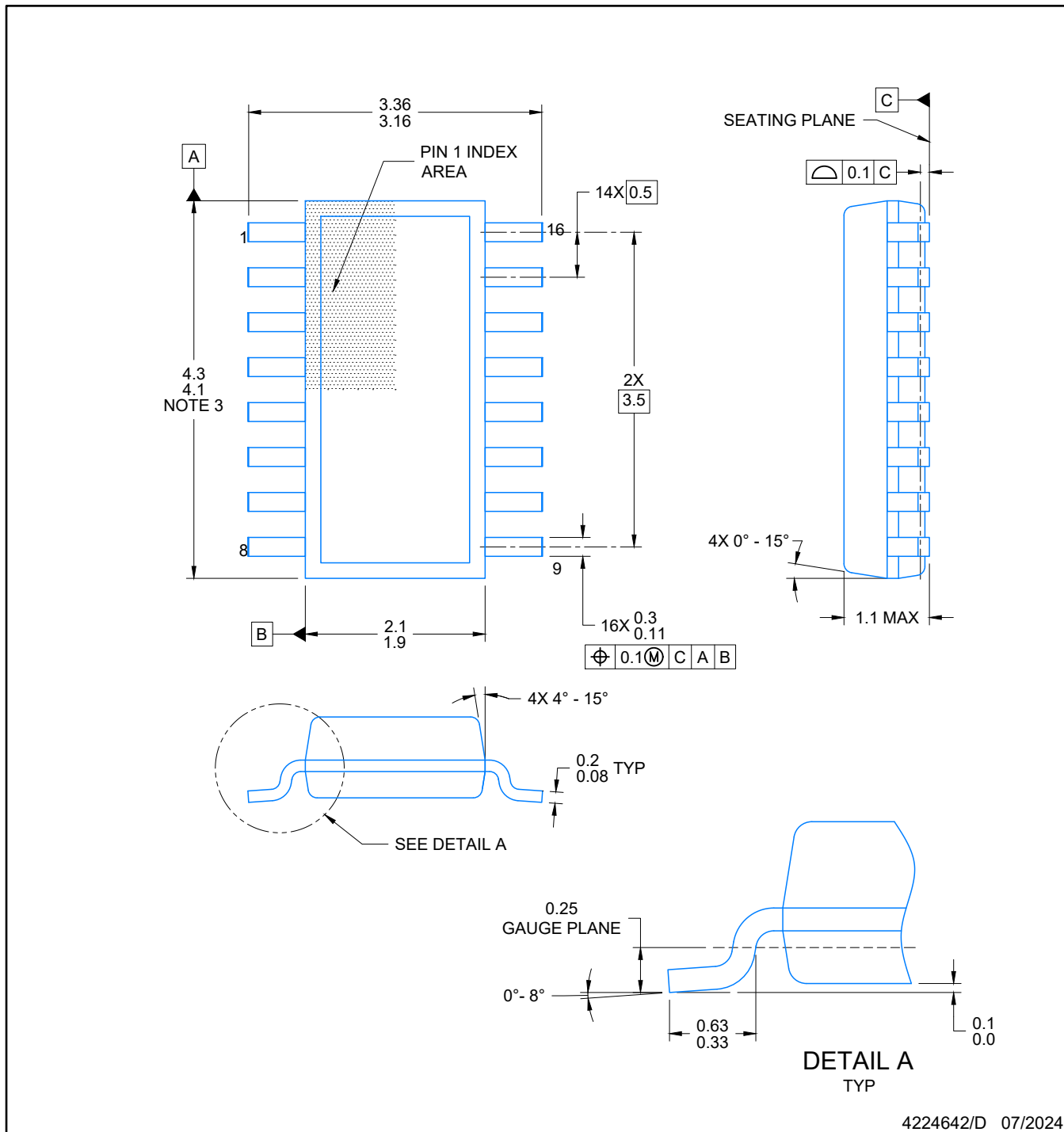


SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220204/A 02/2017

NOTES: (continued)

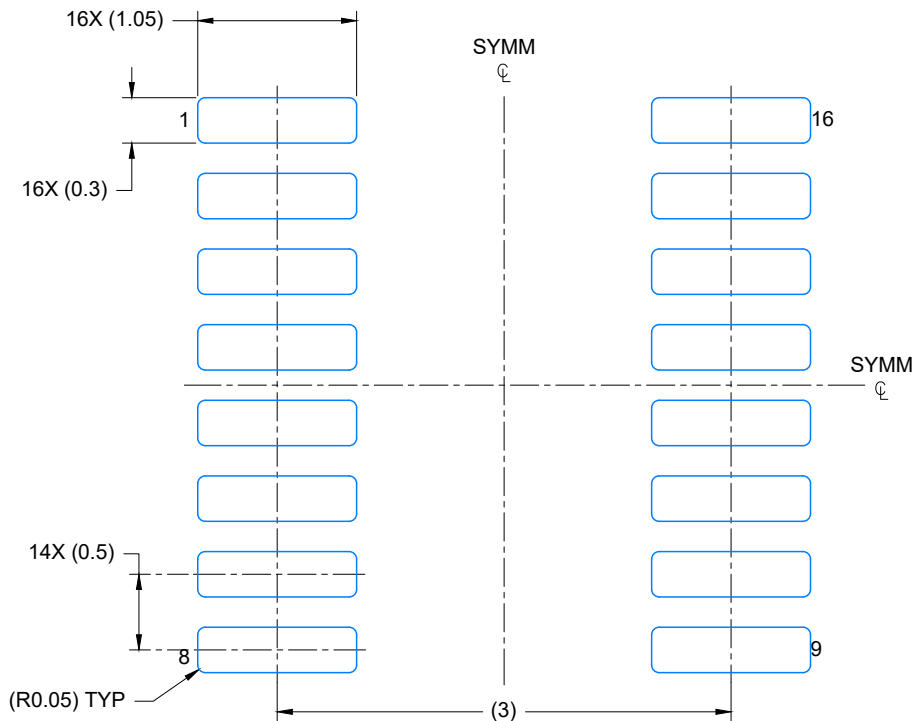
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.



4224642/D 07/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
5. Reference JEDEC Registration MO-345, Variation AA



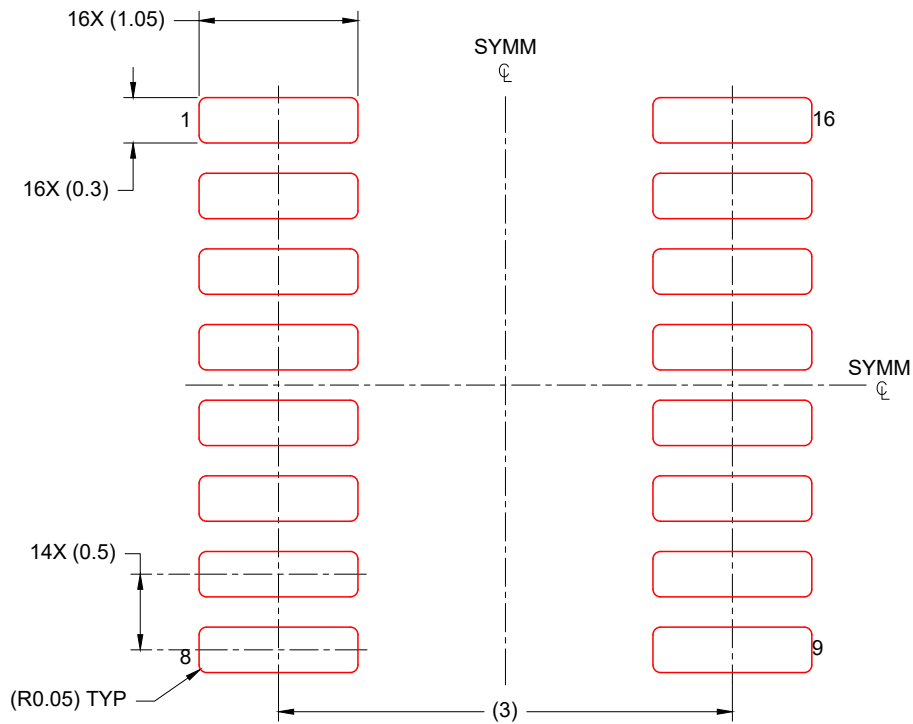
LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 20X



4224642/D 07/2024

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 20X

4224642/D 07/2024

NOTES: (continued)

- 8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 9. Board assembly site may have different recommendations for stencil design.

GENERIC PACKAGE VIEW

DW 16

SOIC - 2.65 mm max height

7.5 x 10.3, 1.27 mm pitch

SMALL OUTLINE INTEGRATED CIRCUIT

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4224780/A



DW0016A

PACKAGE OUTLINE

SOIC - 2.65 mm max height

SOIC



4220721/A 07/2016

NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.
5. Reference JEDEC registration MS-013.

EXAMPLE BOARD LAYOUT

DW0016A

SOIC - 2.65 mm max height

SOIC



LAND PATTERN EXAMPLE
SCALE:7X



SOLDER MASK DETAILS

4220721/A 07/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DW0016A

SOIC - 2.65 mm max height

SOIC



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:7X

4220721/A 07/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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