

# SN74LVC1404 Oscillator Driver for Crystal Oscillator or Ceramic Resonator

## 1 Features

- Available in the Texas Instruments NanoFree™ package
- Supports 5-V  $V_{CC}$  operation
- Inputs accept voltages to 5.5 V
- One buffered inverter with Schmitt-trigger input and two unbuffered inverters
- Integrated solution for oscillator applications
- Suitable for commonly used clock frequencies:
  - 15 kHz, 3.58 MHz, 4.43 MHz, 13 MHz, 25 MHz, 26 MHz, 27 MHz, 28 MHz
- Control input to disable the oscillator circuit
- Low power consumption (10- $\mu$ A Max  $I_{CC}$ ) in standby state
- $\pm 24$ -mA Output Drive at 3.3 V
- $I_{off}$  supports live insertion, partial-power-down mode, and back-drive protection
- Latch-up performance exceeds 100 mA Per JESD 78, Class II
- ESD protection exceeds JESD 22
  - 2000-V Human-body model (A114-A)
  - 200-V Machine model (A115-A)
  - 1000-V Charged-device model (C101)

## 2 Applications

- Servers
- PCs and notebooks
- Network switches
- Wearable health and fitness devices
- Telecom infrastructures
- Electronic points-of-sale

## 3 Description

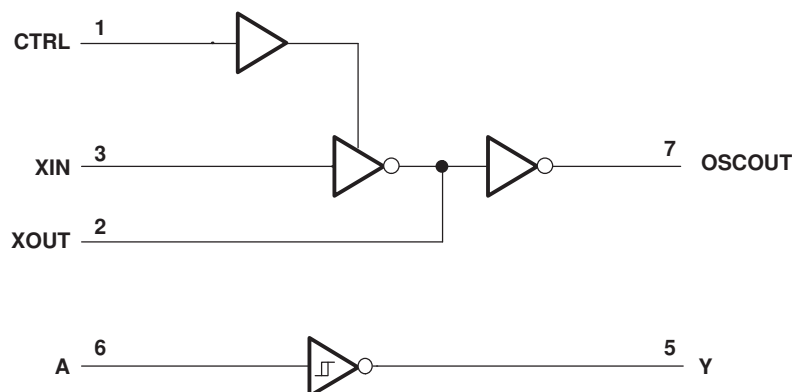
The SN74LVC1404 device consists of one inverter with a Schmitt-trigger input and two unbuffered inverters. It is designed for 1.65-V to 5.5-V  $V_{CC}$  operation.

**Device Information<sup>(1)</sup>**

PART NUMBER	PACKAGE	BODY SIZE (NOM)
SN74LVC1404DCT	SM8 (8)	2.95 mm x 2.80 mm
SN74LVC1404DCU	VSSOP (8)	2.30 mm x 2.00 mm
SN74LVC1404YZP	DSBGA (8)	1.88 mm x 0.88 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

## 4 Simplified Schematic



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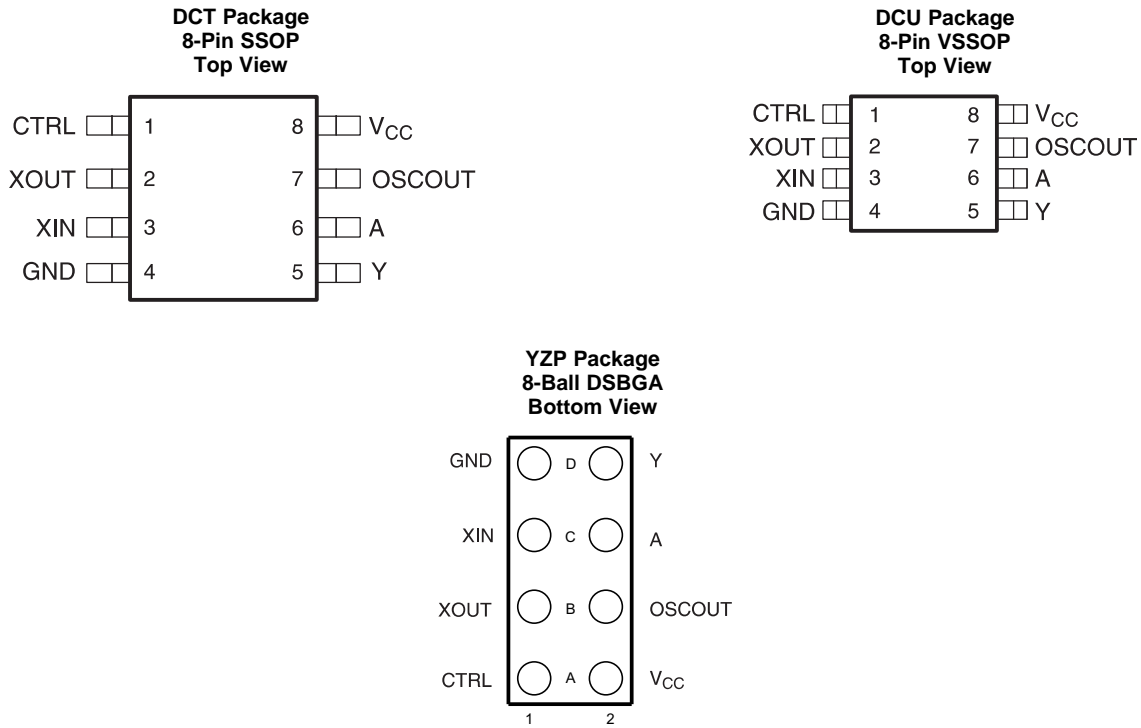
## 5 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision E (June 2014) to Revision F	Page
Formatted pinout figures for search capability	3
Corrected pin numbering for the DSBGA package to match the mechanical drawing	3
Changed ESD Ratings table format to comply with JEDEC standards	4
Added YZP $T_A$ MIN /MAX specs and package thermal information	5

Changes from Revision D (January 2007) to Revision E	Page
Updated document to new TI data sheet format	1
Removed Ordering Information table	1
Added Applications	1
Added Device Information table	1
Added Handling Ratings table	4
Changed MAX ambient temperature to $125^\circ\text{C}$	5
Added Thermal Information table	5
Added Typical Characteristics	7

## 6 Pin Configuration and Functions



See mechanical drawings for dimensions.

Drawings not to scale

### Pin Functions

PIN NO.			I/O	DESCRIPTION
DCT/DCU	YZP	NAME		
1	A1	CTRL	I	OSC Control
2	B1	XOUT	O	Crystal Connection Out
3	C1	XIN	I	Crystal Connection In
4	D1	GND	—	Ground
5	D2	Y	O	Schmitt Trigger Output
6	C2	A	I	Schmitt Trigger Input
7	B2	OSCOUT	O	Oscillator Output
8	A2	VCC	—	Power Supply

## 7 Specifications

### 7.1 Absolute Maximum Ratings<sup>(1)</sup>

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V <sub>CC</sub>	Supply voltage range		–0.5	6.5	V
V <sub>I</sub>	Input voltage range <sup>(2)</sup>	XIN, A, CTRL inputs	–0.5	6.5	V
V <sub>O</sub>	Voltage range applied to any output in the high-impedance or power-off state <sup>(2)</sup>	Y output	–0.5	6.5	V
V <sub>O</sub>	Voltage range applied to any output in the high or low state <sup>(2)(3)</sup>	XOUT, OSCOUT	–0.5	V <sub>CC</sub> + 0.5	V
I <sub>IK</sub>	Input clamp current	V <sub>I</sub> < 0		–50	mA
I <sub>OK</sub>	Output clamp current	V <sub>O</sub> < 0		–50	mA
I <sub>O</sub>	Continuous output current			±50	mA
	Continuous current through V <sub>CC</sub> or GND			±100	mA
T <sub>stg</sub>	Storage Temperature Range		–65	150	°C
T <sub>J</sub>	Junction Temperature			150	°C

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.
- (3) The value of V<sub>CC</sub> is provided in the *Recommended Operating Conditions* table.

### 7.2 ESD Ratings

			MAX	UNIT
V <sub>(ESD)</sub>	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins <sup>(1)</sup>	±2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins <sup>(2)</sup>	±1000	

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

### 7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

			MIN	MAX	UNIT
V <sub>CC</sub>	Supply voltage	Operating	1.65	5.5	V
		Data retention only	1.5		
V <sub>I</sub>	Input voltage (XIN, CTRL, A inputs)		0	5.5	V
V <sub>O</sub>	Output voltage (XOUT, OSCOUT, Y outputs)		0	V <sub>CC</sub>	V
I <sub>OH</sub>	High-level output current (OSCOUT, XOUT, Y outputs)	V <sub>CC</sub> = 1.65 V		−4	mA
		V <sub>CC</sub> = 2.3 V		−8	
		V <sub>CC</sub> = 3 V		−16	
				−24	
		V <sub>CC</sub> = 4.5 V		−32	
I <sub>OL</sub>	Low-level output current (OSCOUT, XOUT, Y outputs)	V <sub>CC</sub> = 1.65 V		4	mA
		V <sub>CC</sub> = 2.3 V		8	
		V <sub>CC</sub> = 3 V		16	
				24	
		V <sub>CC</sub> = 4.5 V		32	
I <sub>OL</sub> <sup>(2)</sup>	Low-level output current (XOUT)	V <sub>CC</sub> = 1.65 V		2	mA
Δt/Δv	Input transition rise and fall time (CTRL input)	V <sub>CC</sub> = 1.8 V ± 0.15 V		20	ns/V
		V <sub>CC</sub> = 2.5 V ± 0.2 V		20	
		V <sub>CC</sub> = 3.3 V ± 0.3 V		10	
		V <sub>CC</sub> = 5 V ± 0.5 V		5	
T <sub>A</sub>	Operating free-air temperature	DCU, DCT	−40	125	°C
		YZP	−40	85	

(1) All unused inputs of the device must be held at V<sub>CC</sub> or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number [SCBA004](#).

(2) CTRL = Low, XIN = GND

### 7.4 Thermal Information

THERMAL METRIC <sup>(1)</sup>		DCT	DCU	YZP	UNIT
		8 PINS	8 PINS	8 BALLS	
R <sub>θJA</sub>	Junction-to-ambient thermal resistance	184.8	198.4	97.5	°C/W
R <sub>θJC(top)</sub>	Junction-to-case (top) thermal resistance	115.3	73.5	1.1	
R <sub>θJB</sub>	Junction-to-board thermal resistance	97.3	77.1	26.3	
ψ <sub>JT</sub>	Junction-to-top characterization parameter	40.9	6.1	0.5	
ψ <sub>JB</sub>	Junction-to-board characterization parameter	96.3	76.7	26.2	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, [SPRA953](#).

## 7.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V <sub>CC</sub>	MIN	TYP <sup>(1)</sup>	MAX	UNIT
V <sub>T+</sub> Positive-going threshold	A input		1.65 V	0.79		1.16	V
			2.3 V	1.11		1.56	
			3 V	1.5		1.87	
			4.5 V	2.16		2.74	
			5.5 V	2.61		3.33	
V <sub>T-</sub> Negative-going threshold	A input		1.65 V	0.39		0.62	V
			2.3 V	0.58		0.87	
			3 V	0.84		1.14	
			4.5 V	1.41		1.79	
			5.5 V	1.87		2.29	
$\Delta V_T$ hysteresis (V <sub>T+</sub> – V <sub>T-</sub> )	A input		1.65 V	0.37		0.62	V
			2.3 V	0.48		0.77	
			3 V	0.56		0.87	
			4.5 V	0.71		1.04	
			5.5 V	0.71		1.11	
V <sub>OH</sub> <sup>(2)</sup>		I <sub>OH</sub> = –100 $\mu$ A	1.65 V to 5.5 V	V <sub>CC</sub> – 0.1			V
		I <sub>OH</sub> = –4 mA	1.65 V	1.2			
		I <sub>OH</sub> = –8 mA	2.3 V	1.9			
		I <sub>OH</sub> = –16 mA	3 V	2.4			
		I <sub>OH</sub> = –24 mA	3 V	2.3			
		I <sub>OH</sub> = –32 mA	4.5 V	3.8			
V <sub>OL</sub> <sup>(2)</sup>		I <sub>OL</sub> = 100 $\mu$ A	1.65 V to 5.5 V			0.1	V
		I <sub>OL</sub> = 4 mA	1.65 V			0.45	
		I <sub>OL</sub> = 8 mA	2.3 V			0.3	
		I <sub>OL</sub> = 16 mA	3 V			0.4	
		I <sub>OL</sub> = 24 mA	3 V			0.55	
		I <sub>OL</sub> = 32 mA	4.5 V			0.55	
V <sub>OL</sub>	XOUT	I <sub>OL</sub> = 100 $\mu$ A	1.65 V to 5.5 V	CTRL = Low, XIN = GND		0.1	V
		I <sub>OL</sub> = 2 mA				0.65	
I <sub>I</sub>	All inputs	V <sub>I</sub> = 5.5 V or GND	0 to 5.5 V			$\pm 5$	$\mu$ A
I <sub>off</sub>	Y output	V <sub>I</sub> or V <sub>O</sub> = 0 to 5.5 V	0			$\pm 10$	$\mu$ A
I <sub>CC</sub>		V <sub>I</sub> = V <sub>CC</sub> or GND, I <sub>O</sub> = 0	1.65 V to 5.5 V			10	$\mu$ A
$\Delta I_{CC}$	CTRL and A inputs	One input at V <sub>CC</sub> – 0.6 V, Other inputs at V <sub>CC</sub> or GND	3 V to 5.5 V			500	$\mu$ A
C <sub>i</sub>	CTRL and A inputs	V <sub>I</sub> = V <sub>CC</sub> or GND	3.3 V		3.5		pF
	XIN				6		

(1) All typical values are at V<sub>CC</sub> = 3.3 V, T<sub>A</sub> = 25°C.

(2) V<sub>IL</sub> = 0 V and V<sub>IH</sub> = V<sub>CC</sub> for XOUT and OSCOUT; the standard V<sub>T+</sub> and V<sub>T-</sub> levels should be applied for the Y output.

## 7.6 Switching Characteristics, $C_L = 15 \text{ pF}$

over recommended operating free-air temperature range (unless otherwise noted) (see [Figure 2](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 1.8 \text{ V}$ $\pm 0.15 \text{ V}$		$V_{CC} = 2.5 \text{ V}$ $\pm 0.2 \text{ V}$		$V_{CC} = 3.3 \text{ V}$ $\pm 0.3 \text{ V}$		$V_{CC} = 5 \text{ V}$ $\pm 0.5 \text{ V}$		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
$t_{pd}$	A	Y	2.8	15.1	1.6	5.7	1.5	4.6	0.9	4.4	ns
	XIN	XOUT	1.7	9.6	1	3.2	1.1	2.4	0.9	1.8	
		OSCOU	2.6	17.2	2	5.6	2	4.1	1.5	3.2	
	CTRL	XOUT	3	28.2	1.8	14.4	1.5	12.2	1.1	10.2	

## 7.7 Switching Characteristics, $C_L = 30 \text{ pF}$ or $50 \text{ pF}$

over recommended operating free-air temperature range (unless otherwise noted) (see [Figure 3](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 1.8 \text{ V}$ $\pm 0.15 \text{ V}$		$V_{CC} = 2.5 \text{ V}$ $\pm 0.2 \text{ V}$		$V_{CC} = 3.3 \text{ V}$ $\pm 0.3 \text{ V}$		$V_{CC} = 5 \text{ V}$ $\pm 0.5 \text{ V}$		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
$t_{pd}$	A	Y	3	17.3	1.8	7.4	1.8	6.4	1	5.3	ns
	XIN	XOUT	1.2	15.8	0.8	5.8	1	5.4	0.6	4.6	
		OSCOU	3.5	25.7	2.6	7.1	2.8	7.8	2	6.7	
	CTRL	XOUT	3.3	24.5	2.1	12	1.9	12.7	1.1	11.2	

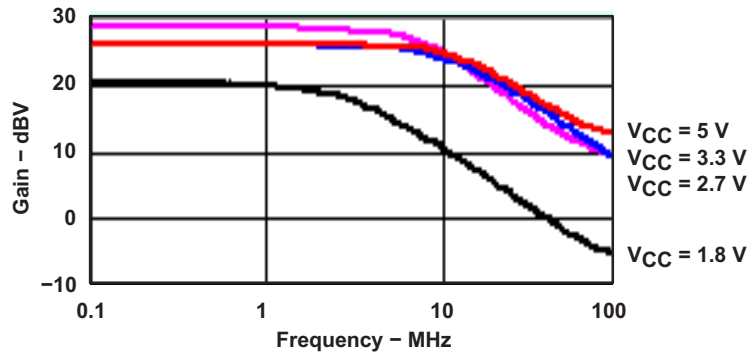
## 7.8 Operating Characteristics

$T_A = 25^\circ\text{C}$

PARAMETER	TEST CONDITIONS	$V_{CC} = 1.8 \text{ V}$	$V_{CC} = 2.5 \text{ V}$	$V_{CC} = 3.3 \text{ V}$	$V_{CC} = 5 \text{ V}$	UNIT
		TYP	TYP	TYP	TYP	
$C_{pd}$ Power dissipation capacitance	$f = 10 \text{ MHz}$	25	26	29	39	pF

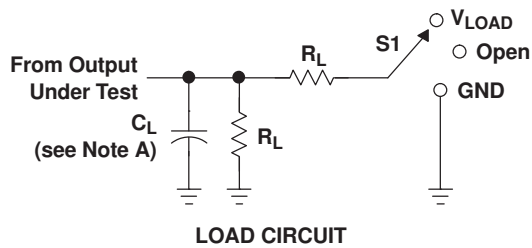
## 7.9 Typical Characteristics

[Figure 1](#) shows the open-loop-gain characteristics of the unbuffered inverter of the LVC1404 (that is, between XIN and XOUT). The device provides a high gain over a wide range of frequencies.



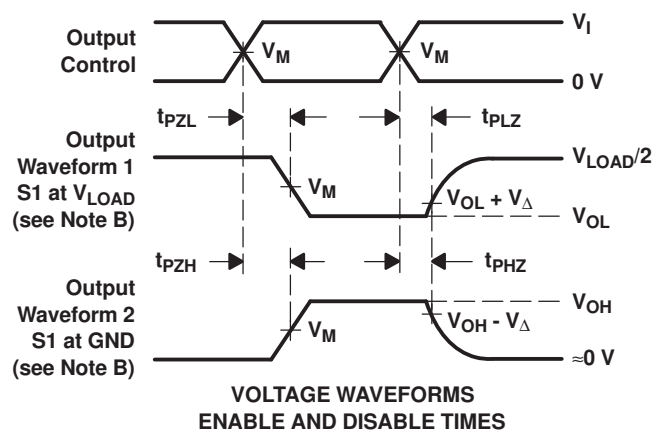
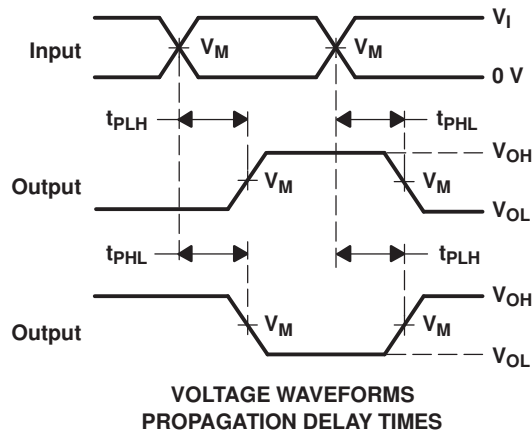
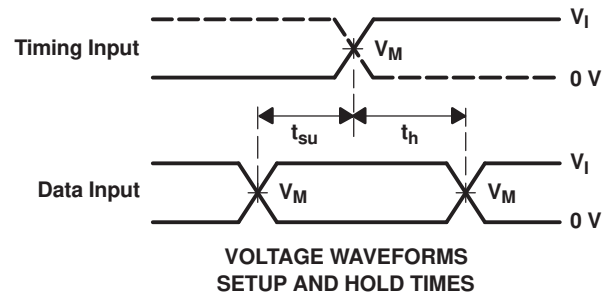
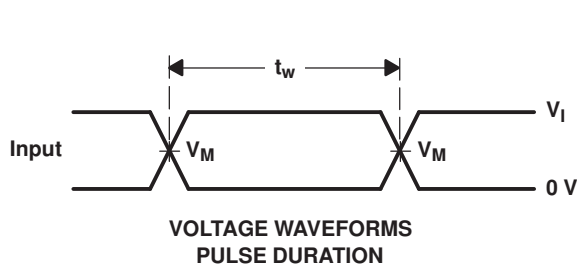
**Figure 1. Open-Loop-Gain Characteristics**

## 8 Parameter Measurement Information



TEST	S1
$t_{PLH}/t_{PHL}$	Open
$t_{PLZ}/t_{PZL}$	$V_{LOAD}$
$t_{PHZ}/t_{PZH}$	GND

$V_{CC}$	INPUTS		$V_M$	$V_{LOAD}$	$C_L$	$R_L$ (Except $t_{pZ}$ )	$R_L$ ( $t_{pZ}$ )	$V_{\Delta}$
	$V_I$	$t_r/t_f$						
$1.8\text{ V} \pm 0.15\text{ V}$	$V_{CC}$	$\leq 2\text{ ns}$	$V_{CC}/2$	$2 \times V_{CC}$	15 pF	1 M $\Omega$	1 k $\Omega$	0.15 V
$2.5\text{ V} \pm 0.2\text{ V}$	$V_{CC}$	$\leq 2\text{ ns}$	$V_{CC}/2$	$2 \times V_{CC}$	15 pF	1 M $\Omega$	1 k $\Omega$	0.15 V
$3.3\text{ V} \pm 0.3\text{ V}$	3 V	$\leq 2.5\text{ ns}$	1.5 V	6 V	15 pF	1 M $\Omega$	1 k $\Omega$	0.3 V
$5\text{ V} \pm 0.5\text{ V}$	$V_{CC}$	$\leq 2.5\text{ ns}$	$V_{CC}/2$	$2 \times V_{CC}$	15 pF	1 M $\Omega$	1 k $\Omega$	0.3 V

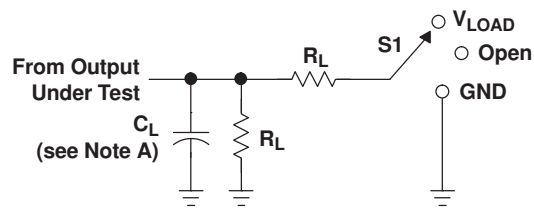


- NOTES:
- $C_L$  includes probe and jig capacitance.
  - Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
  - All input pulses are supplied by generators having the following characteristics:  $PRR \leq 10\text{ MHz}$ ,  $Z_O = 50\ \Omega$ .
  - The outputs are measured one at a time, with one transition per measurement.
  - $t_{PLZ}$  and  $t_{PHZ}$  are the same as  $t_{dis}$ .
  - $t_{PZL}$  and  $t_{PZH}$  are the same as  $t_{en}$ .
  - $t_{PLH}$  and  $t_{PHL}$  are the same as  $t_{pd}$ .
  - All parameters and waveforms are not applicable to all devices.

**Figure 2. Load Circuit and Voltage Waveforms**



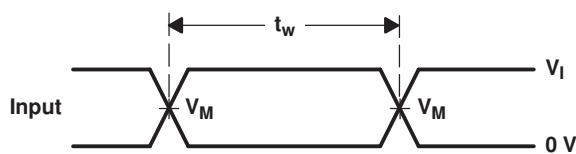
## Parameter Measurement Information (continued)



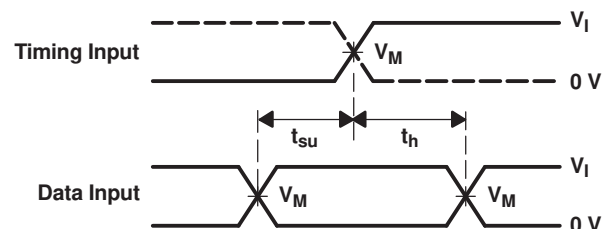
LOAD CIRCUIT

TEST	S1
$t_{PLH}/t_{PHL}$	Open
$t_{PLZ}/t_{PZL}$	$V_{LOAD}$
$t_{PHZ}/t_{PZH}$	GND

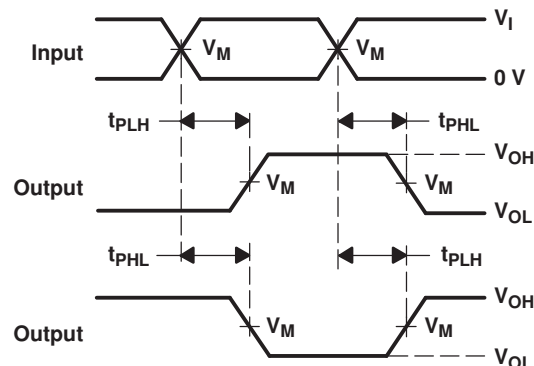
$V_{CC}$	INPUTS		$V_M$	$V_{LOAD}$	$C_L$	$R_L$	$V_{\Delta}$
	$V_I$	$t_r/t_f$					
$1.8\text{ V} \pm 0.15\text{ V}$	$V_{CC}$	$\leq 2\text{ ns}$	$V_{CC}/2$	$2 \times V_{CC}$	30 pF	1 k $\Omega$	0.15 V
$2.5\text{ V} \pm 0.2\text{ V}$	$V_{CC}$	$\leq 2\text{ ns}$	$V_{CC}/2$	$2 \times V_{CC}$	30 pF	500 $\Omega$	0.15 V
$3.3\text{ V} \pm 0.3\text{ V}$	3 V	$\leq 2.5\text{ ns}$	1.5 V	6 V	50 pF	500 $\Omega$	0.3 V
$5\text{ V} \pm 0.5\text{ V}$	$V_{CC}$	$\leq 2.5\text{ ns}$	$V_{CC}/2$	$2 \times V_{CC}$	50 pF	500 $\Omega$	0.3 V



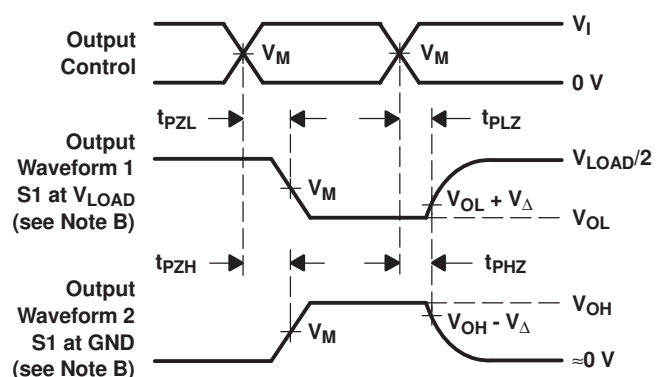
VOLTAGE WAVEFORMS  
PULSE DURATION



VOLTAGE WAVEFORMS  
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS  
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS  
ENABLE AND DISABLE TIMES

- NOTES:
- $C_L$  includes probe and jig capacitance.
  - Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
  - All input pulses are supplied by generators having the following characteristics:  $PRR \leq 10\text{ MHz}$ ,  $Z_O = 50\ \Omega$ .
  - The outputs are measured one at a time, with one transition per measurement.
  - $t_{PLZ}$  and  $t_{PHZ}$  are the same as  $t_{dis}$ .
  - $t_{PZL}$  and  $t_{PZH}$  are the same as  $t_{en}$ .
  - $t_{PLH}$  and  $t_{PHL}$  are the same as  $t_{pd}$ .
  - All parameters and waveforms are not applicable to all devices.

Figure 3. Load Circuit and Voltage Waveforms

## 9 Detailed Description

### 9.1 Overview

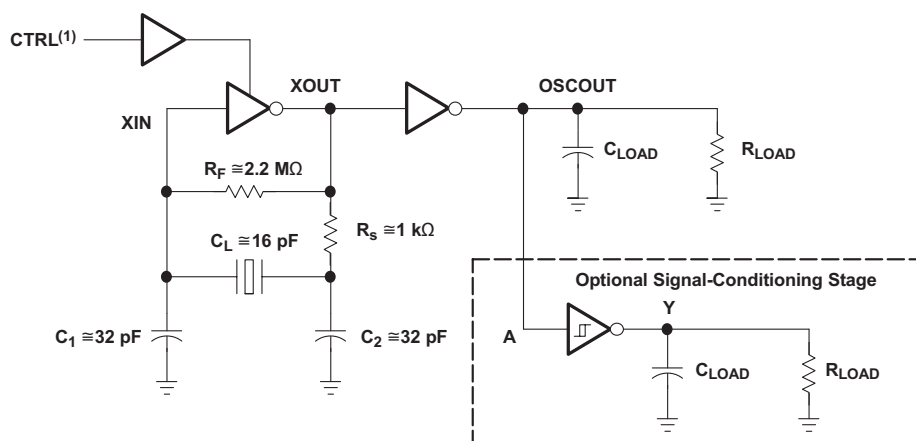
The SN74LVC1404 device consists of one inverter with a Schmitt-trigger input and two unbuffered inverters. It is designed for 1.65-V to 5.5-V  $V_{CC}$  operation.

XIN and XOUT pins can be connected to a crystal or resonator in oscillator applications. The SN74LVC1404 device provides an additional unbuffered inverter (OSCOUT) and a Schmitt-trigger input inverter for signal conditioning (see the [Functional Block Diagram](#)). The control (CTRL) input disables the oscillator circuit to reduce power consumption. The oscillator circuit is disabled and the XOUT output is set to low level when CTRL is low. To ensure the oscillator circuit remains disabled during power up or power down, CTRL should be connected to GND through a pulldown resistor. The minimum value of the resistor is determined by the current-sourcing capability of the driver.

This device is fully specified for partial-power-down applications using  $I_{off}$ . The  $I_{off}$  circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

NanoFree™ package technology is a major breakthrough in IC packaging concepts, using the die as the package.

### 9.2 Functional Block Diagram



### 9.3 Feature Description

- Wide operating voltage range
  - Operates from 1.65 V to 5.5 V
- Has buffered output and un-buffered output from oscillator
- Schmitt-trigger buffer
  - Allows for extra buffering of the oscillator output
- $I_{off}$  feature
  - Allows voltages on the inputs and outputs when  $V_{CC}$  is 0 V

## 9.4 Device Functional Modes

**Table 1. Function Table**

INPUTS		OUTPUTS	
CTRL	XIN	XOUT	OSCOUT
H	L	H	L
H	H	L	H
L	X	L	H

**Table 2. Function Table**

INPUT A	OUTPUT Y
L	H
H	L

## 10 Application and Implementation

### 10.1 Application Information

Figure 4 shows a typical application of the SN74LVC1404 device in a Pierce oscillator circuit. The output voltage can be conditioned further by connecting OSCOUT to the Schmitt-trigger input inverter. The Schmitt-trigger input inverter produces a rail-to-rail voltage waveform. The recommended load for the crystal, shown in this example, is 16 pF. The value of the recommended load ( $C_L$ ) can be found in the crystal manufacturer's data sheet. Values

of  $C_1$  and  $C_2$  are chosen so that  $C_L = \frac{C_1 C_2}{C_1 + C_2}$  and  $C_1 \neq C_2$ .  $R_S$  is the current-limiting resistor, and the value depends on the maximum power dissipation of the crystal. Generally, the recommended value of  $R_S$  is specified in the crystal manufacturer's data sheet and, usually, this value is approximately equal to the reactance of  $C_2$  at resonance frequency, that is,  $R_S = X_{C2}$ .  $R_F$  is the feedback resistor that is used to bias the inverter in the linear region of operation. Usually, the value is chosen to be within 1 M $\Omega$  to 10 M $\Omega$ .

### 10.2 Typical Application

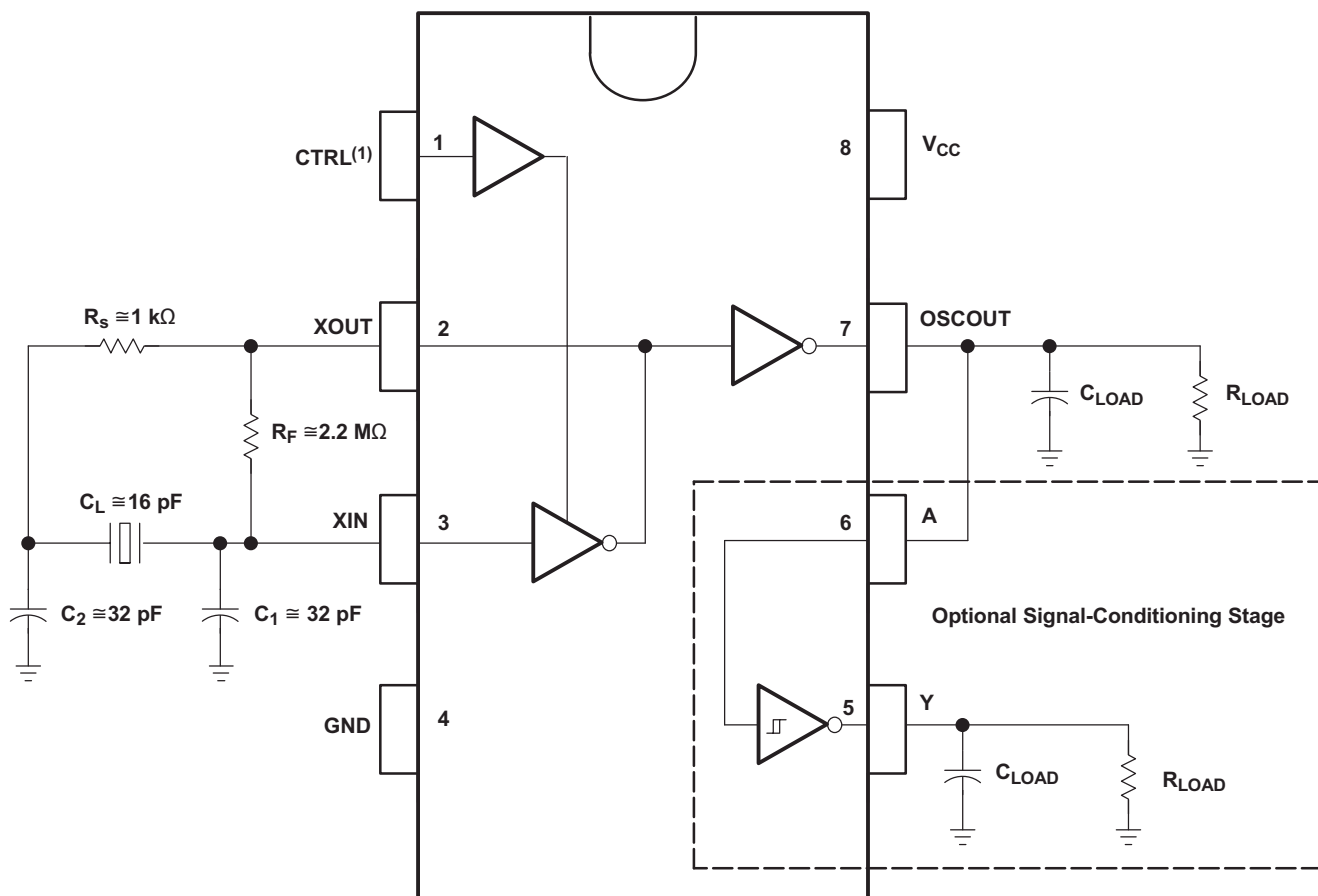


Figure 4. Typical Application Diagram

## Typical Application (continued)

### 10.2.1 Design Requirements

- The open-loop gain of the unbuffered inverter decreases as power-supply voltage decreases. This decreases the closed-loop gain of the oscillator circuit. The value of  $R_s$  can be decreased to increase the closed-loop gain, while maintaining the power dissipation of the crystal within the maximum limit.
- $R_s$  and  $C_2$  form a low-pass filter and reduce spurious oscillations. Component values can be adjusted, based on the desired cutoff frequency.
- $C_2$  can be increased over  $C_1$  to increase the phase shift and help in start-up of the oscillator. Increasing  $C_2$  may affect the duty cycle of the output voltage.
- At high frequency, phase shift due to  $R_s$  becomes significant. In this case,  $R_s$  can be replaced by a capacitor to reduce the phase shift.

### 10.2.2 Detailed Design Procedure

1. Recommended Input Conditions
  - Rise time and fall time specs: See  $(\Delta t/\Delta V)$  in the [Recommended Operating Conditions](#) table.
  - Specified high and low levels: See  $(V_{IH}$  and  $V_{IL})$  in the [Recommended Operating Conditions](#) table.
  - Inputs are overvoltage tolerant allowing them to go as high as 5.5 V at any valid  $V_{CC}$ .
2. Recommended Output Conditions
  - Load currents should not exceed 50 mA per output and 100 mA total for the part.
  - Outputs should not be pulled above  $V_{CC}$ .

#### 10.2.2.1 Testing

After the selection of proper component values, the oscillator circuit should be tested, using these components, to ensure that the oscillator circuit shows required performance over the recommended operating conditions.

- Without a crystal, the oscillator circuit should not oscillate. To check this, the crystal can be replaced by its equivalent parallel-resonant resistance.
- When the power-supply voltage drops, the closed-loop gain of the oscillator circuit reduces. Ensure that the circuit oscillates at the appropriate frequency at the lowest  $V_{CC}$  and highest  $V_{CC}$ .
- Ensure that the duty cycle, start-up time, and frequency drift over time is within the system requirements.

## Typical Application (continued)

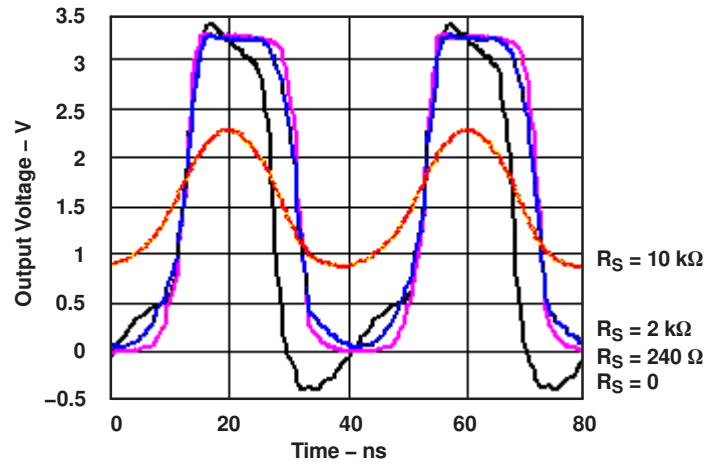
### 10.2.3 Application Curves

#### 10.2.3.1 LVC1404 in 25-MHz Crystal-Oscillator Circuit

$$C_1 \approx C_2 = 30 \text{ pF} \quad (1)$$

$$X_{C2} = 200 \, \Omega \text{ (capacitive reactance at resonance frequency, that is, 25 MHz)} \quad (2)$$

$$V_{CC} = 3.3 \text{ V} \quad (3)$$



**Figure 5. Effect of  $R_S$  on Oscillator Waveform (Frequency = 25 MHz)**

**Table 3. Effect of  $R_S$  on Duty Cycle and  $I_{CC}$  (Frequency = 25 MHz)**

$R_S$ ( $\Omega$ )	$I_{CC}$ (mA)	Positive Duty Cycle (%)
0	22.2	43
240	11.1	45.9
2 k	7.3	47.3
10 k	8.6	46.7

### 10.2.3.2 LVC1404 in 10-MHz Crystal-Oscillator Circuit

$C_1 \approx C_2 = 30 \text{ pF}$  (4)

$X_{C2} = 480 \Omega$  (capacitive reactance at resonance frequency, that is, 10 MHz) (5)

$V_{CC} = 3.3 \text{ V}$  (6)

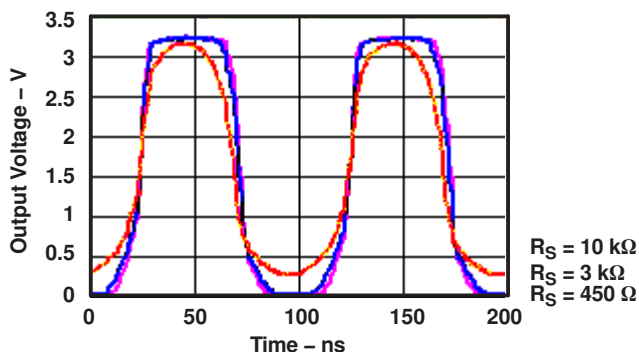


Figure 6. Effect of  $R_S$  on Oscillator Waveform (Frequency = 10 MHz)

Table 4. Effect of  $R_S$  on Duty Cycle and  $I_{CC}$   
(Frequency = 10 MHz)

$R_S$ ( $\Omega$ )	$I_{CC}$ (mA)	Positive Duty Cycle (%)
450	6.9	40
3 k	8.4	47.6
10 k	15.1	43.9

### 10.2.3.3 LVC1404 in 2-MHz Crystal-Oscillator Circuit

$C_1 \approx C_2 = 30 \text{ pF}$  (7)

$X_{C2} = 2.4 \text{ k}\Omega$  (capacitive reactance at resonance frequency, that is, 2 MHz) (8)

$V_{CC} = 3.3 \text{ V}$  (9)

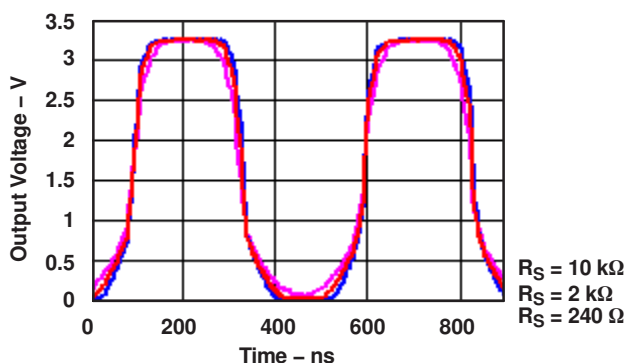


Figure 7. Effect of  $R_S$  on Oscillator Waveform (Frequency = 2 MHz)

Table 5. Effect of  $R_S$  on Duty Cycle and  $I_{CC}$   
(Frequency = 2 MHz)

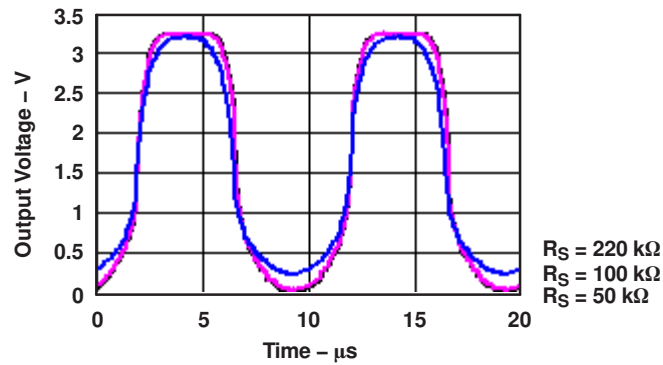
$R_S$ ( $\Omega$ )	$I_{CC}$ (mA)	Positive Duty Cycle (%)
240	11.1	45.9
2 k	7.3	47.3
10 k	8.6	46.7

### 10.2.3.4 LVC1404 in 100-kHz Crystal-Oscillator Circuit

$$C_1 \approx C_2 = 30 \text{ pF} \quad (10)$$

$$X_{C2} = 48 \text{ k}\Omega \text{ (capacitive reactance at resonance frequency, that is, 100 kHz)} \quad (11)$$

$$V_{CC} = 3.3 \text{ V} \quad (12)$$



**Figure 8. Effect of  $R_S$  on Oscillator Waveform (Frequency = 100 kHz)**

**Table 6. Effect of  $R_S$  on Duty Cycle and  $I_{CC}$  (Frequency = 100 kHz)**

$R_S$ ( $\Omega$ )	$I_{CC}$ (mA)	Positive Duty Cycle (%)
50 k	9	46.4
100 k	9.5	46.1
220 k	13.7	44.3



## 11 Power Supply Recommendations

The power supply can be any voltage between the MIN and MAX supply voltage rating located in the [Recommended Operating Conditions](#) table.

Each  $V_{CC}$  pin should have a good bypass capacitor to prevent power disturbance. For devices with a single supply, 0.1  $\mu\text{f}$  is recommended; if there are multiple  $V_{CC}$  pins, then 0.01  $\mu\text{f}$  or 0.022  $\mu\text{f}$  is recommended for each power pin. It is acceptable to parallel multiple bypass caps to reject different frequencies of noise. A 0.1  $\mu\text{f}$  and a 1  $\mu\text{f}$  are commonly used in parallel. The bypass capacitor should be installed as close to the power pin as possible for best results.

## 12 Layout

### 12.1 Layout Guidelines

When using multiple-bit logic devices, inputs should never float.

In many cases, functions or parts of functions of digital logic devices are unused, for example, when only two inputs of a triple-input AND gate are used or only 3 of the 4 buffer gates are used. Such input pins should not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. [Figure 9](#) specifies the rules that must be observed under all circumstances. All unused inputs of digital logic devices must be connected to a high or low bias to prevent them from floating. The logic level that should be applied to any particular unused input depends on the function of the device. Generally they will be tied to GND or  $V_{CC}$ , whichever makes more sense or is more convenient. It is generally acceptable to float outputs, unless the part is a transceiver. If the transceiver has an output enable pin, it will disable the output section of the part when asserted. This will not disable the input section of the I/Os, so they cannot float when disabled.

### 12.2 Layout Example

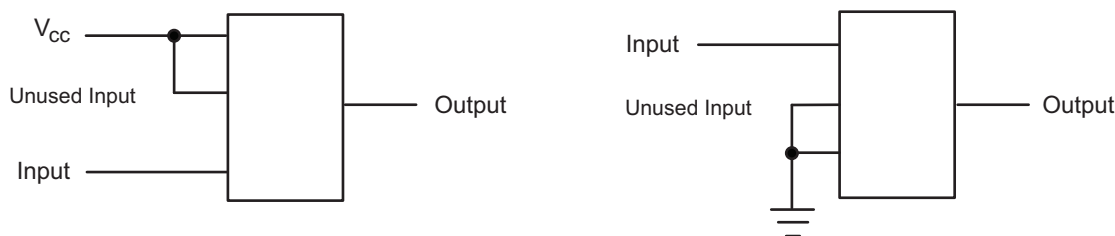


Figure 9. Layout Diagram

## 13 Device and Documentation Support

### 13.1 Trademarks

NanoFree is a trademark of Texas Instruments.  
All other trademarks are the property of their respective owners.

### 13.2 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

### 13.3 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

## 14 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

## PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package   Pins	Package qty   Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
<a href="#">SN74LVC1404DCTR</a>	Active	Production	SSOP (DCT)   8	3000   LARGE T&R	Yes	NIPDAU   SN	Level-1-260C-UNLIM	-40 to 125	(2W85, CA4) (R, Z)
SN74LVC1404DCTR.B	Active	Production	SSOP (DCT)   8	3000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	(2W85, CA4) (R, Z)
<a href="#">SN74LVC1404DCUR</a>	Active	Production	VSSOP (DCU)   8	3000   LARGE T&R	Yes	NIPDAU   SN	Level-1-260C-UNLIM	-40 to 125	(CA4J, CA4R)
SN74LVC1404DCUR.B	Active	Production	VSSOP (DCU)   8	3000   LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	(CA4J, CA4R)
SN74LVC1404DCUR1G4.B	Active	Production	VSSOP (DCU)   8	3000   LARGE T&R	-	Call TI	Call TI	-40 to 125	
<a href="#">SN74LVC1404YZPR</a>	Active	Production	DSBGA (YZP)   8	3000   LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 85	44N
SN74LVC1404YZPR.B	Active	Production	DSBGA (YZP)   8	3000   LARGE T&R	Yes	SNAGCU	Level-1-260C-UNLIM	-40 to 85	44N

<sup>(1)</sup> **Status:** For more details on status, see our [product life cycle](#).

<sup>(2)</sup> **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

<sup>(3)</sup> **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

<sup>(4)</sup> **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

<sup>(5)</sup> **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

<sup>(6)</sup> **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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## TAPE AND REEL INFORMATION



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LVC1404DCTR	SSOP	DCT	8	3000	180.0	12.4	3.15	4.35	1.55	4.0	12.0	Q3
SN74LVC1404DCTR	SSOP	DCT	8	3000	180.0	13.0	3.35	4.5	1.55	4.0	12.0	Q3
SN74LVC1404DCUR	VSSOP	DCU	8	3000	178.0	9.0	2.25	3.35	1.05	4.0	8.0	Q3
SN74LVC1404DCUR	VSSOP	DCU	8	3000	180.0	8.4	2.25	3.35	1.05	4.0	8.0	Q3
SN74LVC1404YZPR	DSBGA	YZP	8	3000	178.0	9.2	1.02	2.02	0.63	4.0	8.0	Q1

## TAPE AND REEL BOX DIMENSIONS



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LVC1404DCTR	SSOP	DCT	8	3000	190.0	190.0	30.0
SN74LVC1404DCTR	SSOP	DCT	8	3000	182.0	182.0	20.0
SN74LVC1404DCUR	VSSOP	DCU	8	3000	180.0	180.0	18.0
SN74LVC1404DCUR	VSSOP	DCU	8	3000	202.0	201.0	28.0
SN74LVC1404YZPR	DSBGA	YZP	8	3000	220.0	220.0	35.0



4225266/A 09/2014

## NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-187 variation CA.

# EXAMPLE BOARD LAYOUT

DCU0008A

VSSOP - 0.9 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 25X



4225266/A 09/2014

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.

6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

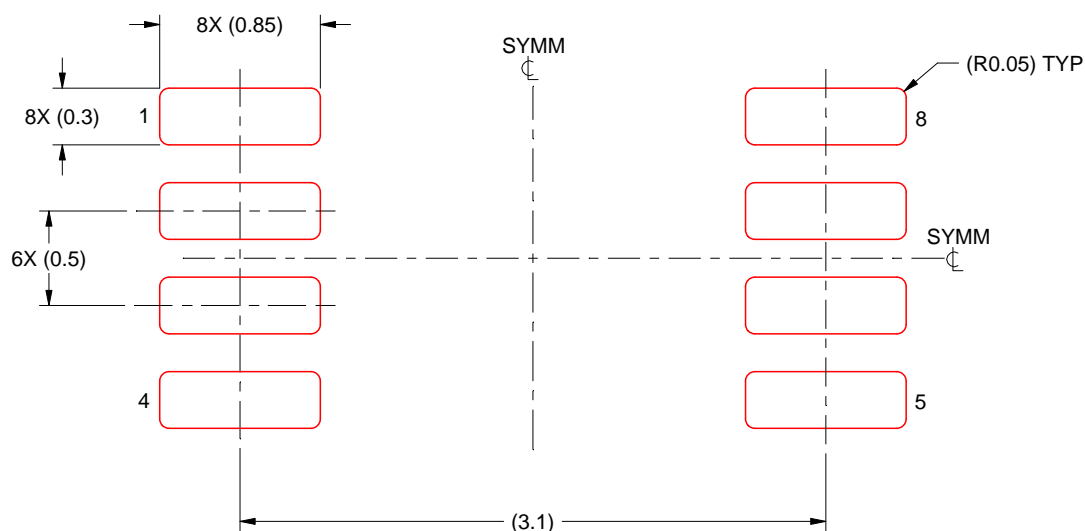


## EXAMPLE STENCIL DESIGN

DCU0008A

VSSOP - 0.9 mm max height

SMALL OUTLINE PACKAGE



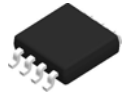
SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE: 25X

4225266/A 09/2014

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

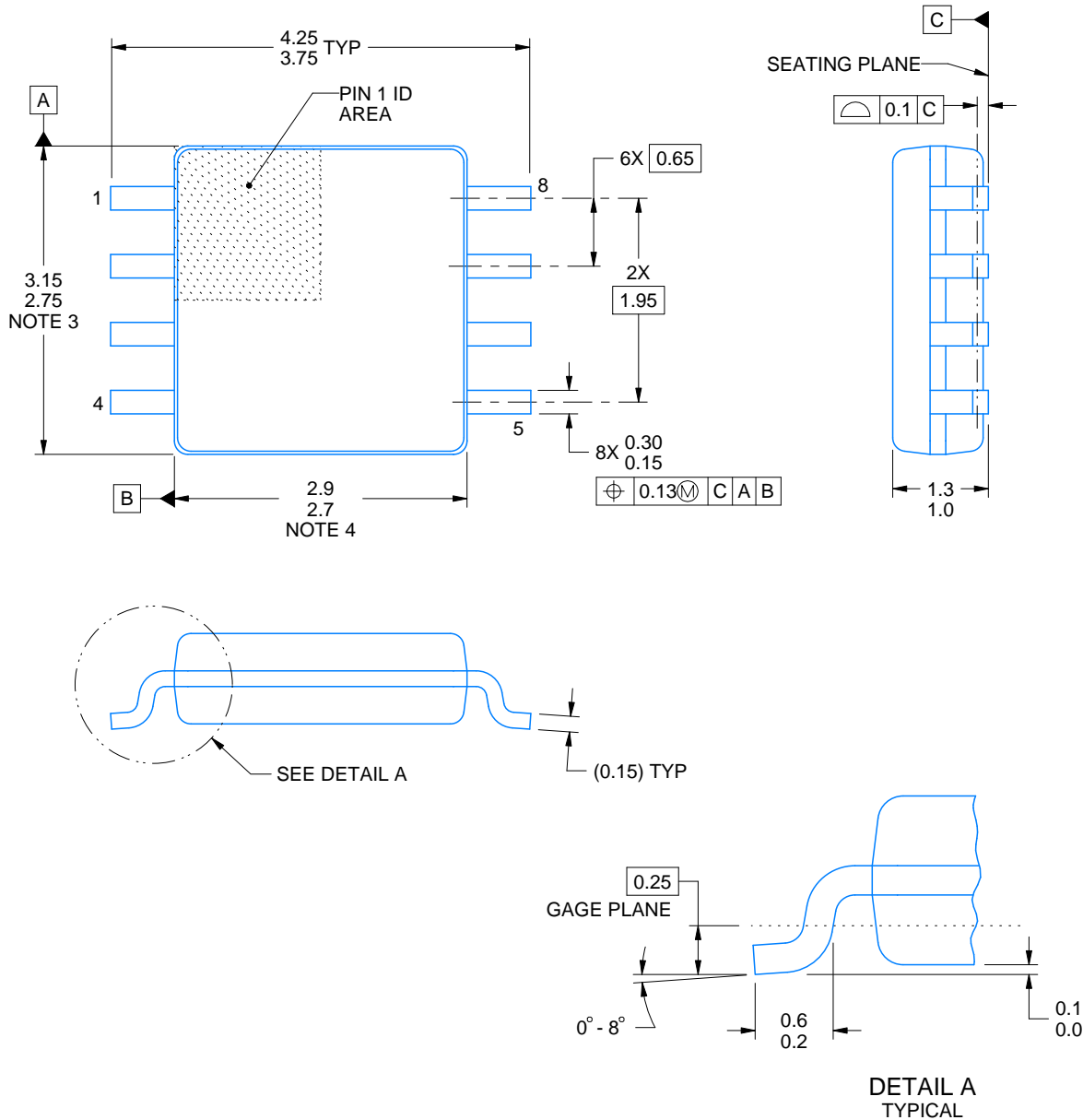
DCT0008A



## PACKAGE OUTLINE

SSOP - 1.3 mm max height

SMALL OUTLINE PACKAGE



4220784/C 06/2021

### NOTES:

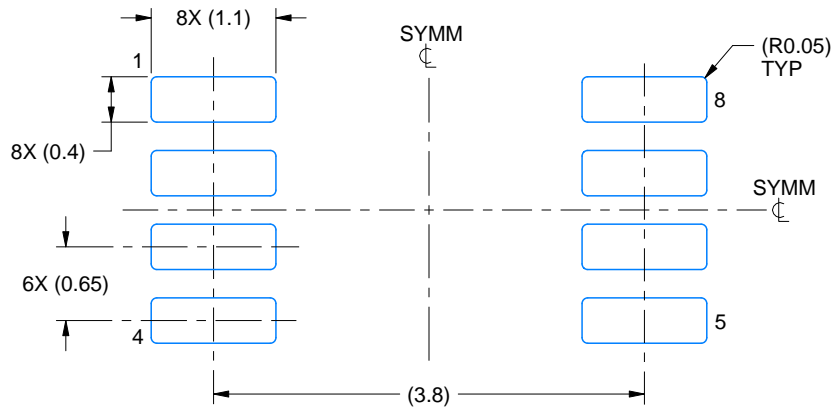
1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.

# EXAMPLE BOARD LAYOUT

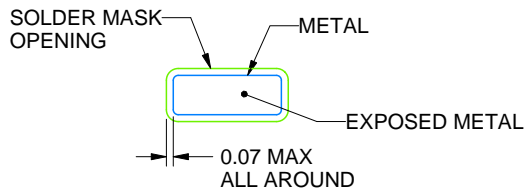
DCT0008A

SSOP - 1.3 mm max height

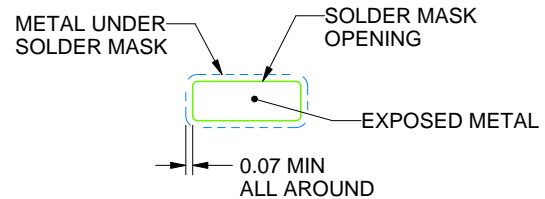
SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE:15X



NON SOLDER MASK  
DEFINED



SOLDER MASK  
DEFINED

SOLDER MASK DETAILS

4220784/C 06/2021

NOTES: (continued)

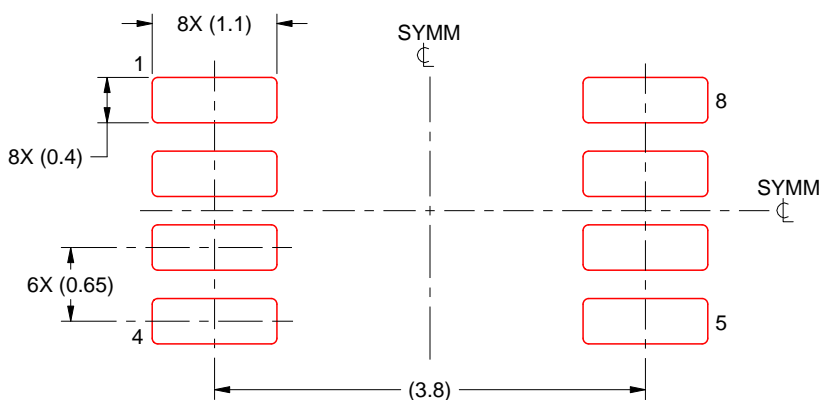
5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

## EXAMPLE STENCIL DESIGN

DCT0008A

SSOP - 1.3 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:15X

4220784/C 06/2021

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

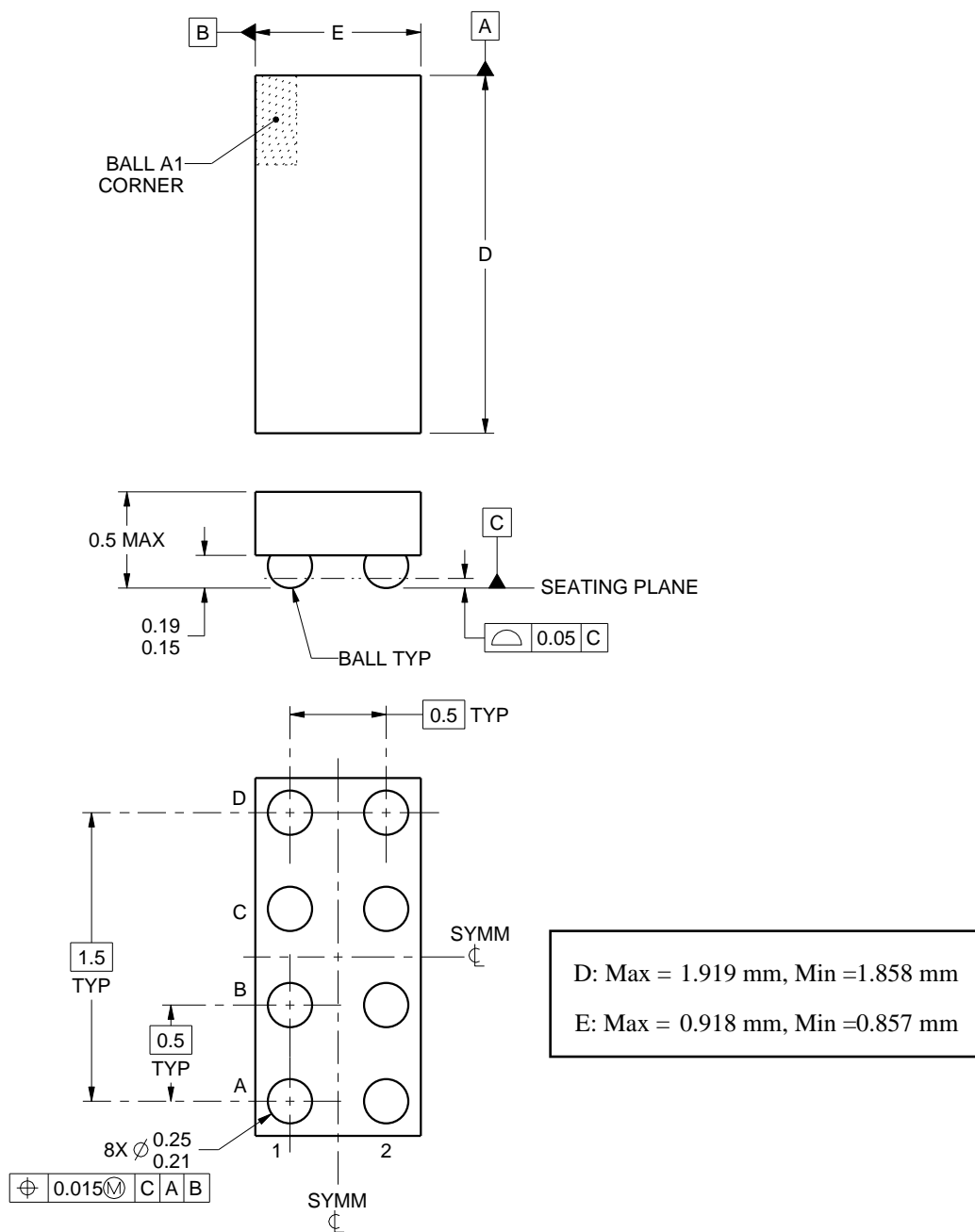
YZP0008



# PACKAGE OUTLINE

DSBGA - 0.5 mm max height

DIE SIZE BALL GRID ARRAY



4223082/A 07/2016

## NOTES:

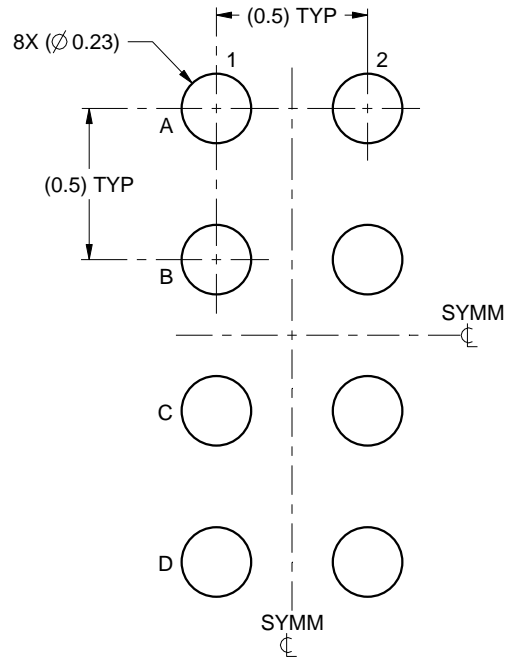
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

# EXAMPLE BOARD LAYOUT

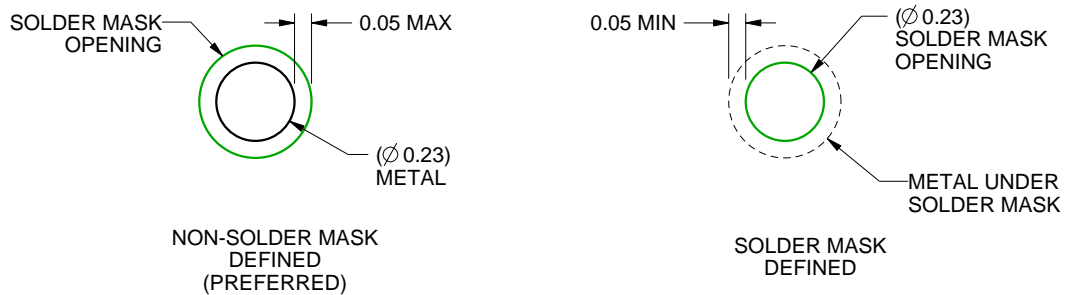
YZP0008

DSBGA - 0.5 mm max height

DIE SIZE BALL GRID ARRAY



LAND PATTERN EXAMPLE  
SCALE:40X



SOLDER MASK DETAILS  
NOT TO SCALE

4223082/A 07/2016

NOTES: (continued)

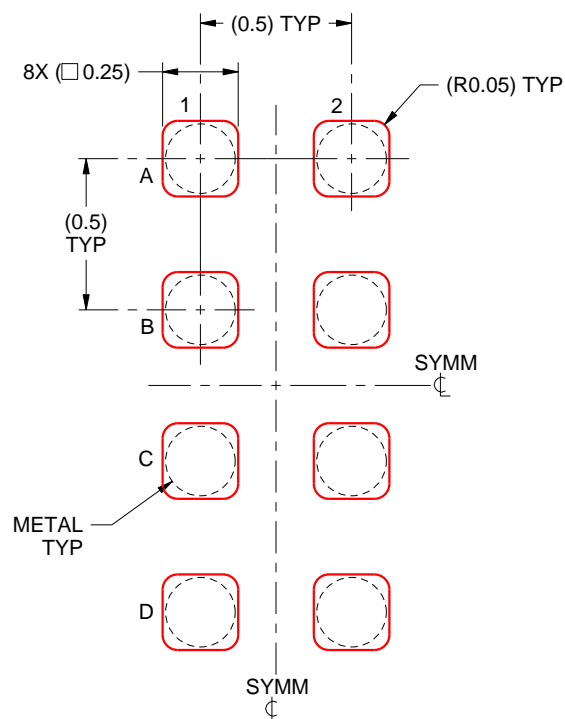
- Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. For more information, see Texas Instruments literature number SNVA009 ([www.ti.com/lit/snva009](http://www.ti.com/lit/snva009)).

## EXAMPLE STENCIL DESIGN

YZP0008

DSBGA - 0.5 mm max height

DIE SIZE BALL GRID ARRAY



SOLDER PASTE EXAMPLE  
BASED ON 0.1 mm THICK STENCIL  
SCALE:40X

4223082/A 07/2016

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

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Last updated 10/2025