

SN74LVC32A-Q1 汽车级四路双输入正或门

1 特性

- 符合汽车应用要求
- 工作电压范围为 2V 至 3.6V
- 输入电压高达 5.5V
- 电压为 3.3V 时, t_{pd} 最大值为 3.8ns
- V_{OLP} (输出接地反弹) 典型值 $< 0.8V$ ($V_{CC} = 3.3V$, $T_A = 25^\circ C$)
- V_{OHV} (输出 V_{OH} 下冲) 典型值 $> 2V$ ($V_{CC} = 3.3V$, $T_A = 25^\circ C$)

2 说明

SN74LVC32A-Q1 四路双输入正或门可在 2.7V 至 3.6V V_{CC} 电压下运行。

该器件以正逻辑执行布尔函数 $Y = A + B$ or $Y = \overline{\overline{A} \cdot \overline{B}}$ 。

输入可以由 3.3V 或 5V 器件驱动。此功能允许在 3.3V/5V 的混合系统环境中将该器件用作转换器。

封装信息

| 器件型号 | 封装 ⁽¹⁾ | 封装尺寸 ⁽²⁾ | 封装尺寸 ⁽³⁾ |
|---------------|-------------------|---------------------|---------------------|
| SN74LVC32A-Q1 | BQA (WQFN , 14) | 3mm × 2.5mm | 3mm × 2.5mm |
| | D (SOIC , 14) | 8.65mm × 6mm | 8.65mm × 3.9mm |
| | PW (TSSOP , 14) | 5mm × 6.4mm | 5mm × 4.4mm |

(1) 更多相关信息, 请参阅第 10 节。

(2) 封装尺寸 (长 × 宽) 为标称值, 并包括引脚 (如适用)。

(3) 封装尺寸 (长 × 宽) 为标称值, 不包括引脚。



逻辑图, 每个逻辑门 (正逻辑)



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3 Pin Configuration and Functions

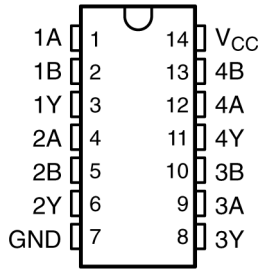


图 3-1.

D or PW Package, 14-Pin SOIC or TSSOP (Top View)

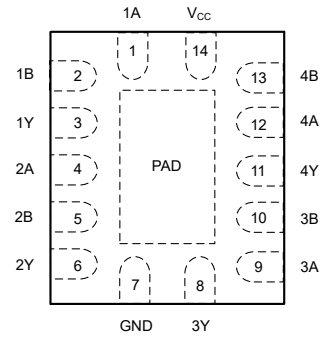


图 3-2. SN74LVC32A-Q1 BQA Package, 14-PIN WQFN (Top View)

表 3-1. Pin Functions

| PIN | | TYPE ⁽¹⁾ | DESCRIPTION |
|------------------------------------|-----|---------------------|---|
| NAME | NO. | | |
| 1A | 1 | I | Channel 1, Input A |
| 1B | 2 | I | Channel 1, Input B |
| 1Y | 3 | O | Channel 1, Output Y |
| 2A | 4 | I | Channel 2, Input A |
| 2B | 5 | I | Channel 2, Input B |
| 2Y | 6 | O | Channel 2, Output Y |
| GND | 7 | — | Ground |
| 3Y | 8 | O | Channel 3, Output Y |
| 3A | 9 | I | Channel 3, Input A |
| 3B | 10 | I | Channel 3, Input B |
| 4Y | 11 | O | Channel 4, Output Y |
| 4A | 12 | I | Channel 4, Input A |
| 4B | 13 | I | Channel 4, Input B |
| V _{CC} | 14 | — | Positive Supply |
| Thermal Information ⁽²⁾ | | — | The thermal pad can be connected to GND or left floating. Do not connect to any other signal or supply. |

(1) Signal Types: I = Input, O = Output, I/O = Input or Output, P = Power Supply, G = Ground.

(2) For BQA package only.

4 Specifications

4.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)

| | | MIN | MAX | UNIT |
|------------------|---|--------------------|-----------------------|------|
| V _{CC} | Supply voltage range | -0.5 | 6.5 | V |
| V _I | Input voltage range ⁽¹⁾ | -0.5 | 6.5 | V |
| V _O | Output voltage range ^{(1) (2)} | -0.5 | V _{CC} + 0.5 | V |
| I _{IK} | Input clamp current | V _I < 0 | -50 | mA |
| I _{OK} | Output clamp current | V _O < 0 | -50 | mA |
| I _O | Continuous output current | | ±50 | mA |
| | Continuous current through V _{CC} or GND | | ±100 | mA |
| T _{stg} | Storage temperature range | -65 | 150 | °C |

(1) The input and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.

(2) The value of V_{CC} is provided in the recommended operating conditions table.

4.2 ESD Ratings

| | | VALUE | UNIT |
|--------------------|---|-------|------|
| V _(ESD) | Human body model (HBM), per AEC Q100-002 ⁽¹⁾ | ±2000 | V |
| | Charged device model (CDM), per AEC Q100-011 | ±1000 | V |

(1) AEC Q100-002 indicates that HBM stressing must be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

4.3 Recommended Operating Conditions

| | | MIN | MAX | UNIT | |
|-----------------|------------------------------------|--------------------------------|-----------------|------|---|
| V _{CC} | Supply voltage | Operating | 2 | 3.6 | V |
| | | Data retention only | 1.5 | | |
| V _{IH} | High-level input voltage | V _{CC} = 2.7V to 3.6V | | V | |
| V _{IL} | Low-level input voltage | V _{CC} = 2.7V to 3.6V | | V | |
| V _I | Input voltage | 0 | 5.5 | V | |
| V _O | Output voltage | 0 | V _{CC} | V | |
| I _{OH} | High-level output current | V _{CC} = 2.7V | -12 | mA | |
| | | V _{CC} = 3V | -24 | | |
| I _{OL} | Low-level output current | V _{CC} = 2.7V | 12 | mA | |
| | | V _{CC} = 3V | 24 | | |
| Δt/Δv | Input transition rise or fall rate | | 7 | ns/V | |
| T _A | Operating free-air temperature | -40 | 125 | °C | |

4.4 Thermal Information

| THERMAL METRIC ⁽¹⁾ | | SN74LVC32A-Q1 | | | UNIT |
|-------------------------------|--|---------------|----------|------------|------|
| | | BQA (WQFN) | D (SOIC) | PW (TSSOP) | |
| | | 14 PINS | 14 PINS | 14 PINS | |
| R _{θJA} | Junction-to-ambient thermal resistance | 102.3 | 127.8 | 150.8 | °C/W |

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC package thermal metrics](#) application report.

4.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | V _{CC} | MIN | TYP ⁽¹⁾ | MAX | UNIT |
|------------------|---|-----------------|-----------------------|--------------------|------|------|
| V _{OH} | I _{OH} = -100μA | 2.7V to 3.6V | V _{CC} - 0.2 | | | V |
| | I _{OH} = -12mA | 2.7V | 2.2 | | | |
| | | 3V | 2.4 | | | |
| | I _{OH} = -24mA | 3V | 2.2 | | | |
| V _{OL} | I _{OL} = 100μA | 2.7V to 3.6V | | | 0.2 | V |
| | I _{OL} = 12mA | 2.7V | | | 0.4 | |
| | | 3V | | | 0.55 | |
| | I _{OL} = 24mA | 3V | | | | |
| I _I | V _I = 5.5V or GND | 3.6V | | | ±5 | μA |
| I _{CC} | V _I = V _{CC} or GND, I _O = 0 | 3.6V | | | 10 | μA |
| ΔI _{CC} | One input at V _{CC} - 0.6V, Other inputs at V _{CC} or GND | 2.7V to 3.6V | | | 500 | μA |
| C _i | V _I = V _{CC} or GND | 3.3V | | 5 | | pF |

(1) All typical values are at V_{CC} = 3.3V, T_A = 25°C.

4.6 Switching Characteristics

over recommended operating free-air temperature range (unless otherwise noted) (see [Load Circuit and Voltage Waveforms](#))

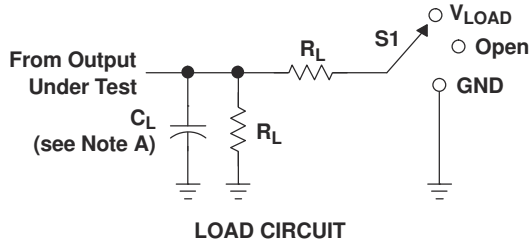
| PARAMETER | FROM (INPUT) | TO (OUTPUT) | V _{CC} = 2.7V | | V _{CC} = 3.3V ± 0.3V | | UNIT |
|-----------------|--------------|-------------|------------------------|-----|-------------------------------|-----|------|
| | | | MIN | MAX | MIN | MAX | |
| t _{pd} | A or B | Y | | 4.4 | 1 | 3.8 | ns |

4.7 Operating Characteristics

T_A = 25°C

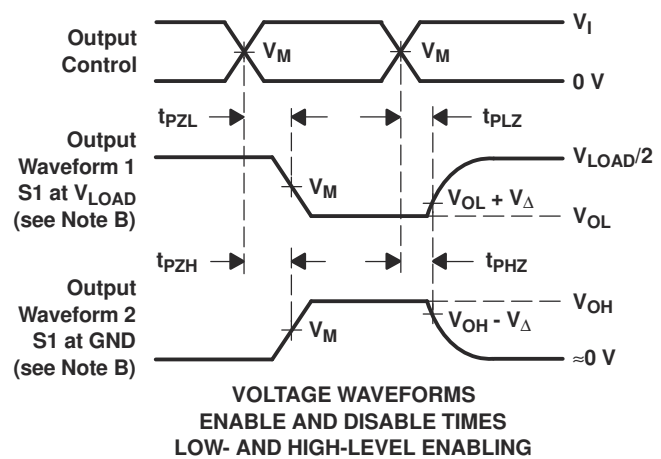
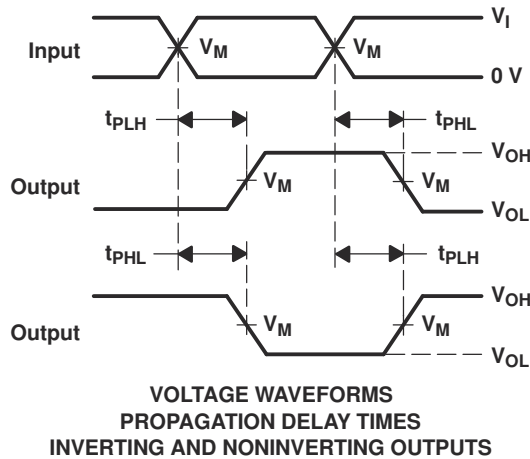
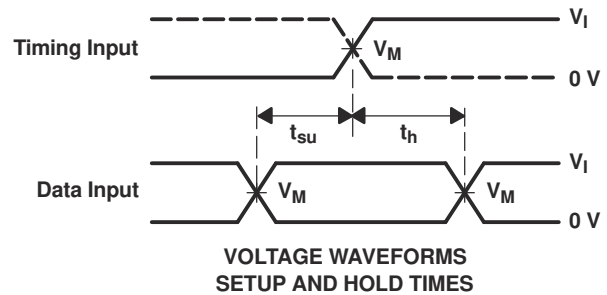
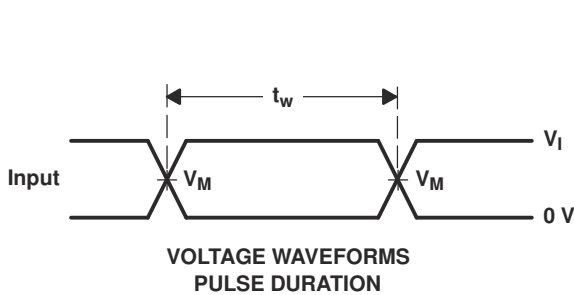
| PARAMETER | TEST CONDITIONS | V _{CC} = 2.5V | | V _{CC} = 3.3V | | UNIT |
|-----------------|--|------------------------|------|------------------------|------|------|
| | | TYP | TYP | TYP | TYP | |
| C _{pd} | Power dissipation capacitance per gate | f = 10MHz | 10.6 | | 12.5 | pF |

5 Parameter Measurement Information



| TEST | S1 |
|-------------------|------------|
| t_{PLH}/t_{PHL} | Open |
| t_{PLZ}/t_{PZL} | V_{LOAD} |
| t_{PHZ}/t_{PZH} | GND |

| V_{CC} | INPUTS | | V_M | V_{LOAD} | C_L | R_L | V_{Δ} |
|-------------------|--------|---------------|-------|------------|-------|--------------|--------------|
| | V_I | t_r/t_f | | | | | |
| 2.7 V | 2.7 V | ≤ 2.5 ns | 1.5 V | 6 V | 50 pF | 500 Ω | 0.3 V |
| 3.3 V \pm 0.3 V | 2.7 V | ≤ 2.5 ns | 1.5 V | 6 V | 50 pF | 500 Ω | 0.3 V |



- NOTES:
- A. C_L includes probe and jig capacitance.
 - B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
 - C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_O = 50 \Omega$.
 - D. The outputs are measured one at a time, with one transition per measurement.
 - E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - F. t_{PZL} and t_{PZH} are the same as t_{en} .
 - G. t_{PLH} and t_{PHL} are the same as t_{pd} .
 - H. All parameters and waveforms are not applicable to all devices.

图 5-1. Load Circuit and Voltage Waveforms

6 Detailed Description

6.1 Overview

The device performs the Boolean function $Y = A + B$ or $Y = \overline{\overline{A} \cdot \overline{B}}$ in positive logic.

Inputs can be driven from either 3.3-V or 5-V devices. This feature allows the use of this device as a translator in a mixed 3.3-V/5-V system environment.

6.2 Functional Block Diagram



图 6-1. Logic Diagram, Each Gate (Positive Logic)

6.3 Device Functional Modes

Function Table
(Each Gate)

| INPUTS | | OUTPUT Y |
|--------|---|-------------|
| A | B | |
| H | X | H |
| X | H | H |
| L | L | L |

7 Application and Implementation

备注

以下应用部分中的信息不属于 TI 器件规格的范围，TI 不担保其准确性和完整性。TI 的客户应负责确定器件是否适用于其应用。客户应验证并测试其设计，以确保系统功能。

7.1 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in the *Recommended Operating Conditions*. Each V_{CC} terminal should have a good bypass capacitor to prevent power disturbance. A 0.1- μF capacitor is recommended for this device. It is acceptable to parallel multiple bypass caps to reject different frequencies of noise. The 0.1- μF and 1- μF capacitors are commonly used in parallel. The bypass capacitor should be installed as close to the power terminal as possible for best results, as shown in given example layout image.

7.2 Layout

7.2.1 Layout Guidelines

When using multiple-input and multiple-channel logic devices inputs must never be left floating. In many cases, functions or parts of functions of digital logic devices are unused; for example, when only two inputs of a triple-input AND gate are used or only 3 of the 4 buffer gates are used. Such unused input pins must not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. All unused inputs of digital logic devices must be connected to a logic high or logic low voltage, as defined by the input voltage specifications, to prevent them from floating. The logic level that must be applied to any particular unused input depends on the function of the device. Generally, the inputs are tied to GND or V_{CC} , whichever makes more sense for the logic function or is more convenient.

7.2.2 Layout Example

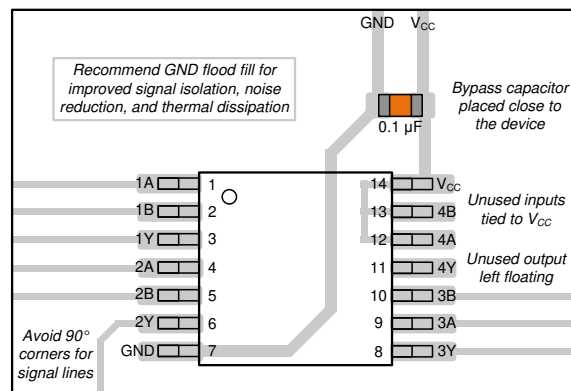


图 7-1. Example Layout for the SN74LVC32A-Q1

8 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

8.1 Documentation Support (Analog)

8.1.1 Related Documentation

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

表 8-1. Related Links

| PARTS | PRODUCT FOLDER | SAMPLE & BUY | TECHNICAL DOCUMENTS | TOOLS & SOFTWARE | SUPPORT & COMMUNITY |
|---------------|----------------------------|----------------------------|----------------------------|----------------------------|----------------------------|
| SN74LVC32A-Q1 | Click here | Click here | Click here | Click here | Click here |

8.2 接收文档更新通知

要接收文档更新通知，请导航至 ti.com 上的器件产品文件夹。点击 [通知](#) 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

8.3 支持资源

TI E2E™ [中文支持论坛](#) 是工程师的重要参考资料，可直接从专家处获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题，获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的 [使用条款](#)。

8.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.
所有商标均为其各自所有者的财产。

8.5 静电放电警告



静电放电 (ESD) 会损坏这个集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

8.6 术语表

[TI 术语表](#) 本术语表列出并解释了术语、首字母缩略词和定义。

9 Revision History

注：以前版本的页码可能与当前版本的页码不同

| Changes from Revision D (May 2024) to Revision E (December 2024) | Page |
|--|------|
| • Updated R θ JA value: D = 86 to 127.8, all values in °C/W | 4 |

| Changes from Revision C (March 2024) to Revision D (May 2024) | Page |
|--|------|
| • Updated R θ JA value: PW = 113 to 150.8, all values in °C/W | 4 |

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead finish/ Ball material (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|--------------------|---------------|--------------|-----------------|------|-------------|-----------------|--------------------------------------|----------------------|--------------|-------------------------|-------------------------|
| SN74LVC32AQDRQ1 | ACTIVE | SOIC | D | 14 | 2500 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | LVC32AQ | Samples |
| SN74LVC32AQPWRG4Q1 | ACTIVE | TSSOP | PW | 14 | 2000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | LVC32AQ | Samples |
| SN74LVC32AQPWRQ1 | ACTIVE | TSSOP | PW | 14 | 2000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | LVC32AQ | Samples |
| SN74LVC32AWBQARQ1 | ACTIVE | WQFN | BQA | 14 | 3000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | LVC32Q | Samples |

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSELETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer:The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and

continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF SN74LVC32A-Q1 :

- Catalog : [SN74LVC32A](#)
- Enhanced Product : [SN74LVC32A-EP](#)
- Military : [SN54LVC32A](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Enhanced Product - Supports Defense, Aerospace and Medical Applications
- Military - QML certified for Military and Defense Applications

TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|--------------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| SN74LVC32AQPWRG4Q1 | TSSOP | PW | 14 | 2000 | 330.0 | 12.4 | 6.9 | 5.6 | 1.6 | 8.0 | 12.0 | Q1 |
| SN74LVC32AQPWRQ1 | TSSOP | PW | 14 | 2000 | 330.0 | 12.4 | 6.9 | 5.6 | 1.6 | 8.0 | 12.0 | Q1 |
| SN74LVC32AWBQARQ1 | WQFN | BQA | 14 | 3000 | 180.0 | 12.4 | 2.8 | 3.3 | 1.1 | 4.0 | 12.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|--------------------|--------------|-----------------|------|------|-------------|------------|-------------|
| SN74LVC32AQPWRG4Q1 | TSSOP | PW | 14 | 2000 | 356.0 | 356.0 | 35.0 |
| SN74LVC32AQPWRQ1 | TSSOP | PW | 14 | 2000 | 356.0 | 356.0 | 35.0 |
| SN74LVC32AWBQARQ1 | WQFN | BQA | 14 | 3000 | 210.0 | 185.0 | 35.0 |

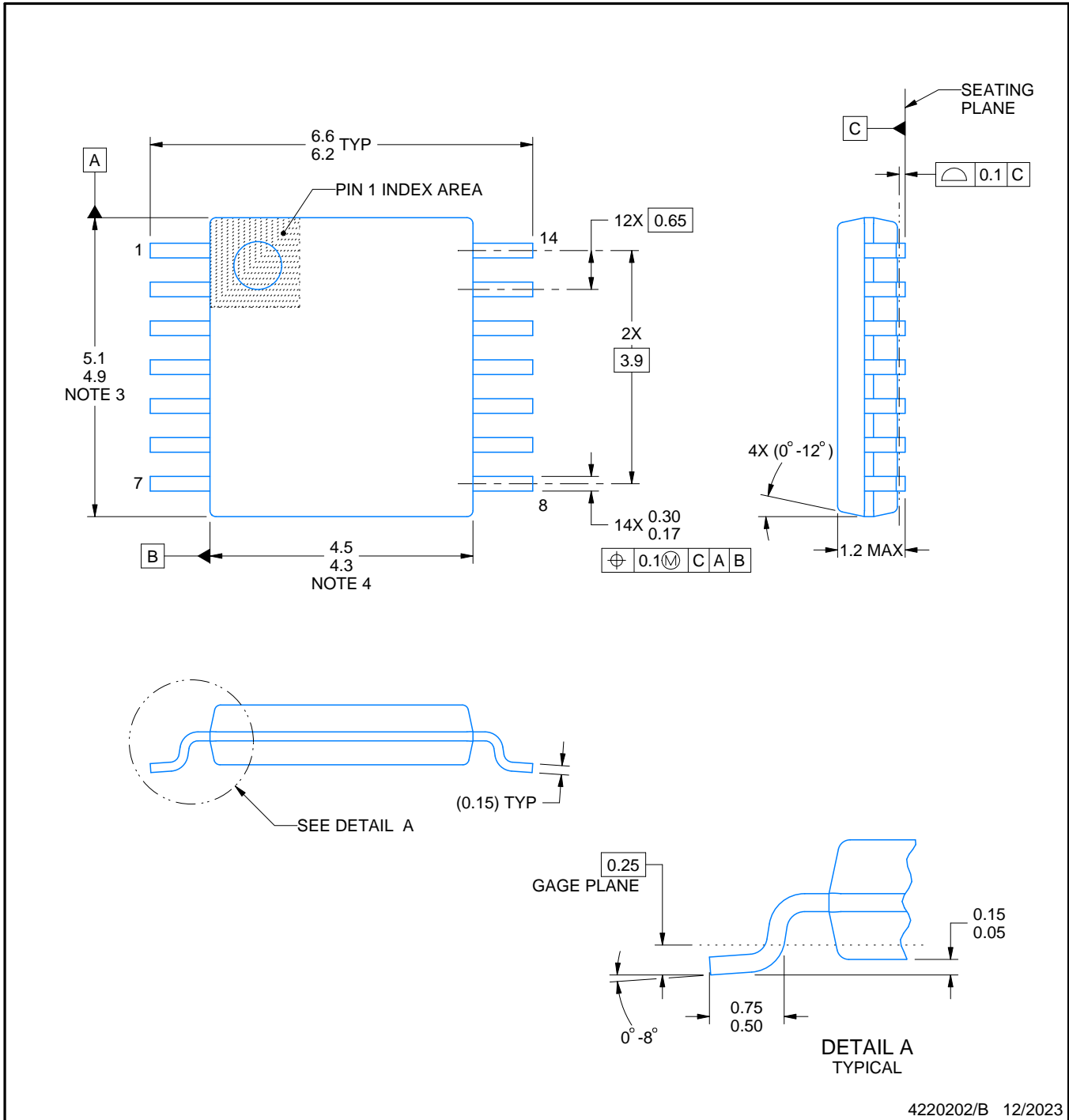
PW0014A



PACKAGE OUTLINE

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

EXAMPLE BOARD LAYOUT

PW0014A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



4220202/B 12/2023

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

PW0014A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220202/B 12/2023

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

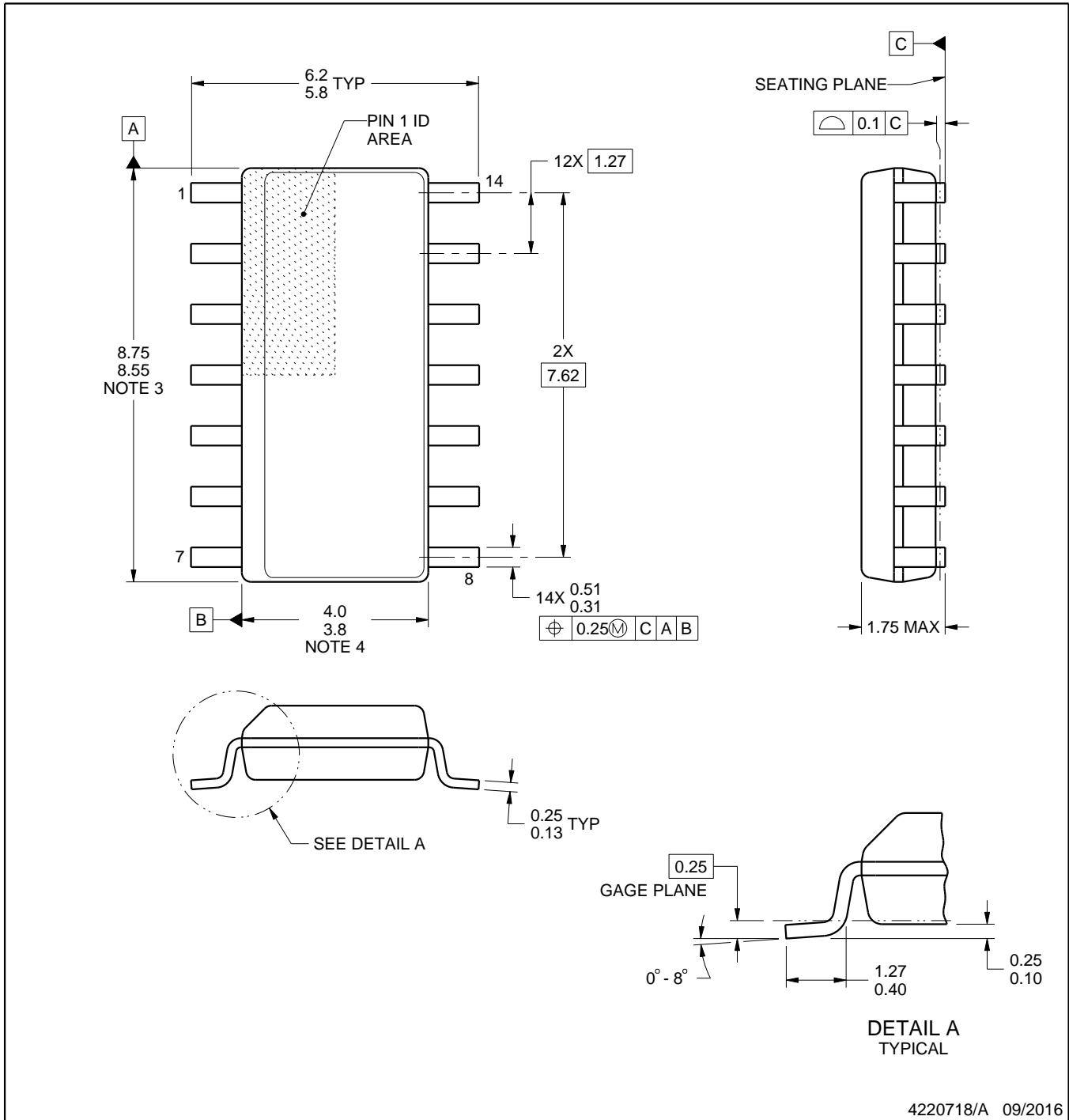
D0014A



PACKAGE OUTLINE

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



4220718/A 09/2016

NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm, per side.
5. Reference JEDEC registration MS-012, variation AB.

EXAMPLE BOARD LAYOUT

D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE
SCALE:8X



SOLDER MASK DETAILS

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NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:8X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

GENERIC PACKAGE VIEW

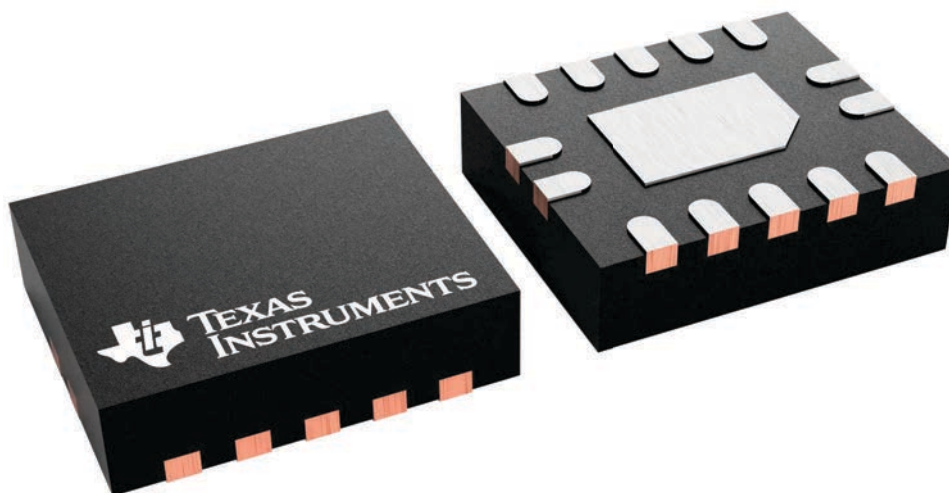
BQA 14

WQFN - 0.8 mm max height

2.5 x 3, 0.5 mm pitch

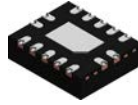
PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4227145/A

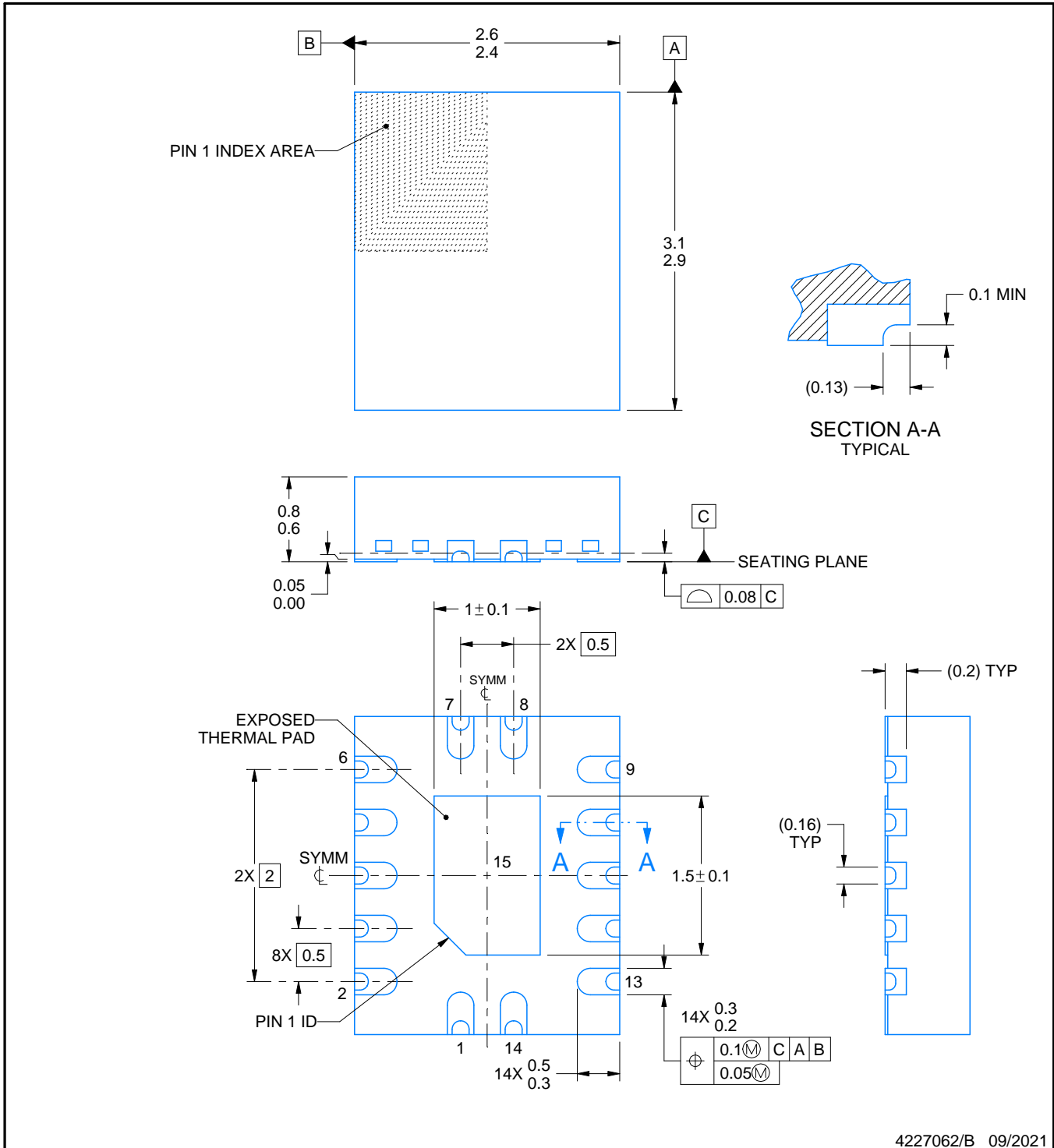
BQA0014B



PACKAGE OUTLINE

WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



NOTES:

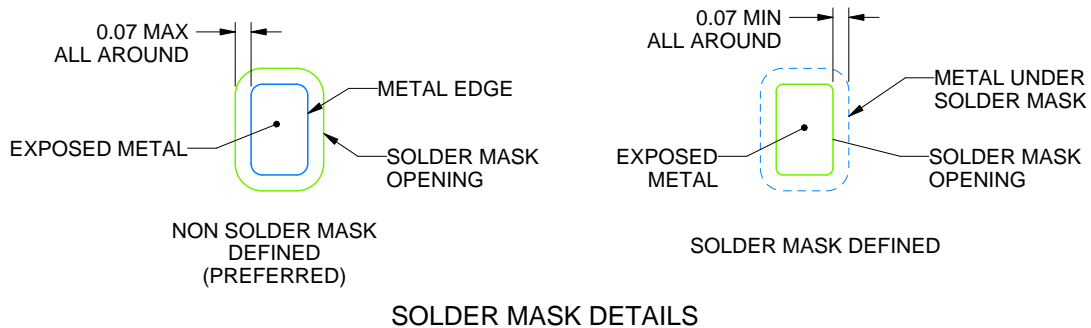
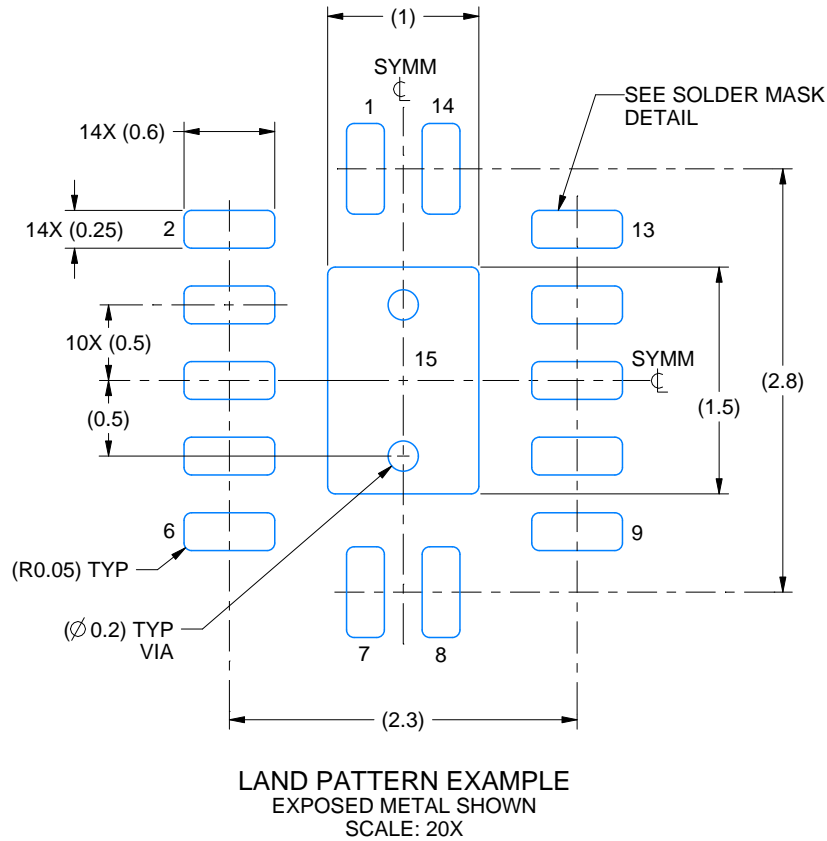
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

EXAMPLE BOARD LAYOUT

BQA0014B

WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



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NOTES: (continued)

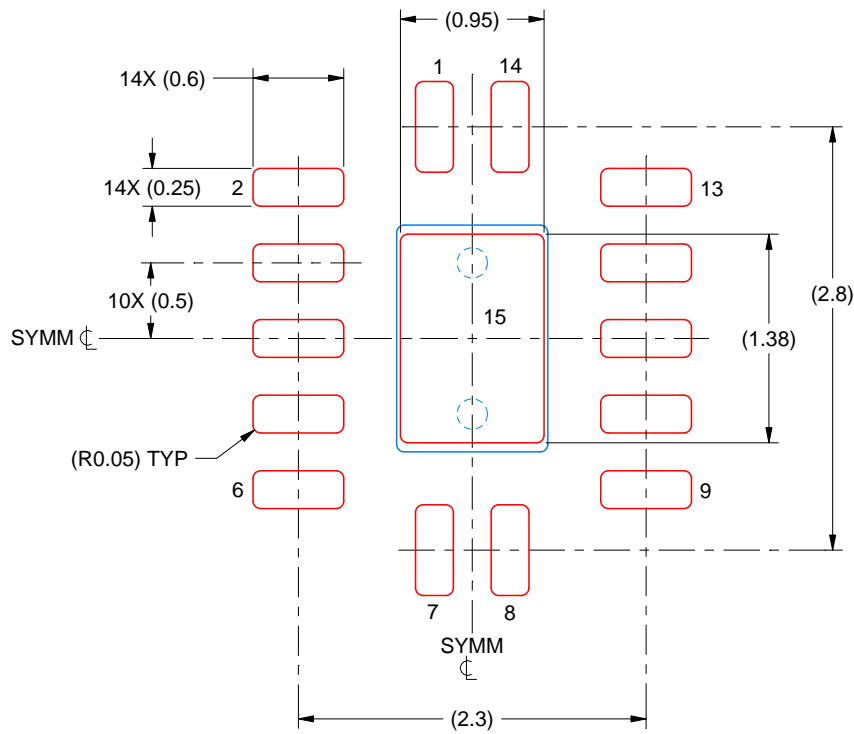
4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/sluea271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

BQA0014B

WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 MM THICK STENCIL
SCALE: 20X

EXPOSED PAD 15
87% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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